THE DATASHEET OF

A8302SETTR-T

Dual LNB Supply and Control Voltage Regulators

FEATURES AND BENEFITS

- Integrated boost MOSFET, current sensing, and compensation
- Configurable boost capacitor option through I²C™ control register: ceramic or electrolytic
- Two switching frequency settings programmable through I²C™ control register (563 kHz and 939 kHz)
- Adjustable LNB output current limit from 250 to 950 mA
  - Covers a wide array of application requirements
  - Minimizes component sizing to fit each application
  - For startup, reconfiguration, and continuous output
  - Optional temporary increased current limit (+25%)
  - Internal gate drive output BFGATEx for bypass FET used in DiSEqC™ applications

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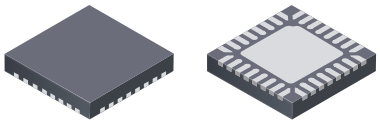
PACKAGE: 32-contact MLP/QFN with exposed thermal pad (suffix ET)



5 mm × 5 mm × 0.90 mm
not to scale

DESCRIPTION

The A8302 is a dual-channel low-noise block converter regulator (LNBR). The A8302 consists of a monolithic linear and switching voltage regulator, specifically designed to provide the power and the interface signals to an LNB down converter via coaxial cable in satellite TV receivers systems. The A8302 requires few external components, with the boost switch and compensation circuitry integrated inside of the device. The boost converter switching frequency and user-controlled current limit minimize the size of the passive filtering components. User controlled current limit and two switching frequency settings allow to optimize size of passive filtering components.

A sleep pin is available to maximize power savings and to quickly shut down the device if needed, without using I²C™ control.

The A8302 has integrated tone detection capability and the internal driver allows full two-way DiSEqC™ communications. For DiSEqC™ communication, the IC provides an internal 22 kHz tone that is gated with the TONECTRLx pin or accepts an external 22 kHz tone through the TONECTRLx pin.

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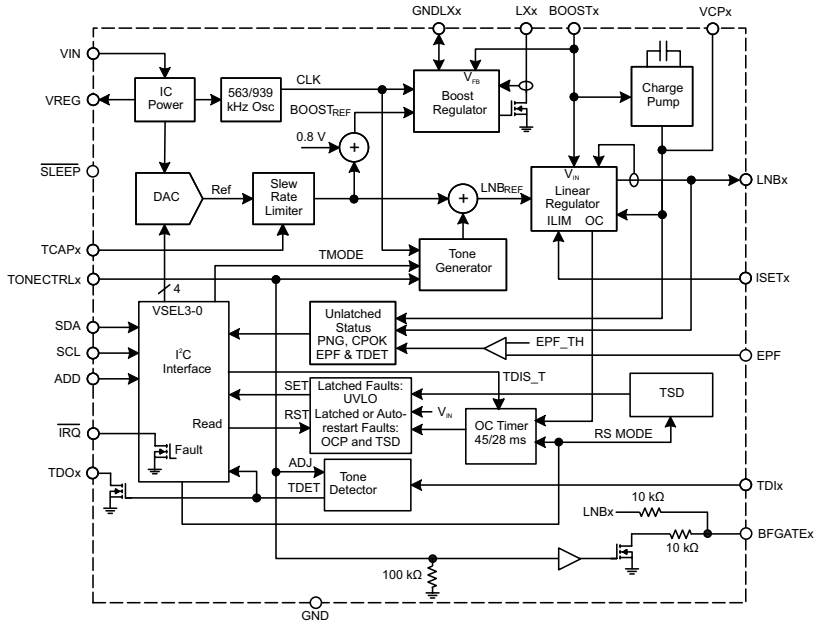
Functional Block Diagram

(One of two channels shown, *x* in pin name indicates channel: 1 or 2)



FEATURES AND BENEFITS (continued)

- Boost peak current limit scales with LNB current limit setting
- Early Power Failure (EPF) warning
- SINK_DIS bit to control maximum output reverse current
- 8 programmable LNB output voltage (DAC) levels
- LNB overcurrent limit protection and TSD with auto-restart or latched
- LNB transition times configurable by external capacitor
- Built-in 22 kHz tone oscillator facilitates DiSEqC™ tone encoding
  - Tone generation does not require additional external components
- Diagnostic features: PNGx,TDETx, BOOSTxH and EPF
- Dynamic tone detect amplitude and frequency transmit/receive thresholds
- Extensive protection features: UVLO, TSD, OCPx, and CPOKx
- Sleep mode with shutdown current < 15 µA (typ)

DESCRIPTION (continued)

The A8302 offers Early Power Failure (EPF) warning, which helps to initiate shutdown routines. The A8302 maximum output reverse current can be set using the SINK_DIS bit.

A comprehensive set of fault registers are provided, which comply with all the common standards, including overcurrent, thermal shutdown, undervoltage, and power not good.

The device uses a 2-wire bidirectional serial interface, compatible with the I²C™ standard, that operates up to 400 kHz.

The A8302 is supplied in a 5 mm × 5 mm, 32-contact, lead (Pb) free QFN package (suffix ET), with 100% matte tin plated leadframe.

Selection Guide

Part Number	Packing[1]	Description
A8302SETTR-T[2]	7 in. reel, 1500 pieces/reel 12 mm carrier tape	ET package, QFN surface mount 5 mm × 5 mm × 0.90 mm nominal height

[1]Contact Allegro for additional packing options.
[2]Leadframe plating 100% matte tin.

Absolute Maximum Ratings

Characteristic	Symbol	Conditions	Rating	Unit
Load Supply Voltage, VIN Pin	V_{IN}		25	V
Output Current[1]	I_{OUT}		Internally Limited	A
Output Voltage; BOOSTx and BFGATEx Pins			–0.3 to 43	V
LNBx Pin[2]		Surge	–1.0 to 43	V
LXx Pin			–0.3 to 30	V
VCPx Pin			–0.3 to 48	V
Logic Input Voltage			–0.3 to 5.5	V
Logic Output Voltage			–0.3 to 5.5	V
EPF and VREG Pins			–0.3 to 6	V
Operating Ambient Temperature	T_A	Range S; T_A(max) depends on thermal design; overriding factor is T_J(max)	–20 to 85	°C
Junction Temperature	T_J(max)		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

[1]Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current ratings, or a junction temperature, T_J, of 150°C.
[2]See application schematics 3 and 4 on pages 38 and 40.

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Thermal Characteristics: May require derating at maximum conditions

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	4-layer PCB based on JEDEC standard	30	°C/W

*Additional thermal information available on the Allegro website

Table of Contents

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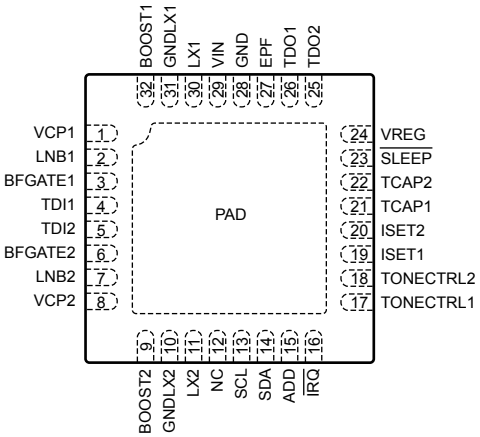
Pinout Diagram



Terminal List Table

Number	Name	Function
1	VCP1	Channel 1 gate supply voltage
2	LNB1	Channel 1 output voltage to LNB
3	BFGATE1	Channel 1 gate driver point for the external P-channel bypass MOSFET
4	TDI1	Channel 1 Tone Detect input
5	TDI2	Channel 2 Tone Detect input
6	BFGATE2	Channel 2 gate driver point for the external P-channel bypass MOSFET
7	LNB2	Channel 2 output voltage to LNB
8	VCP2	Channel 2 gate supply voltage
9	BOOST2	Tracking supply voltage to channel 2 linear regulator
10	GNDLX2	Channel 2 boost switch ground
11	LX2	Channel 2 internal boost switch drain node
12	NC	No connect
13	SCL	I²C-compatible clock input
14	SDA	I²C-compatible data input/output
15	ADD	Address select
16	$\overline{\text{IRQ}}$	Interrupt request output
17	TONECONTRL1	Apply a 22 kHz tone or tone on-and-off signal to enable/disable internal tone of channel1
18	TONECONTRL2	Apply a 22 kHz tone or tone on-and-off signal to enable/disable internal tone of channel2
19	ISET1	Terminal for external resistor that sets the LNB1 current limit
20	ISET2	Terminal for external resistor that sets the LNB2 current limit
21	TCAP1	Capacitor for setting the rise and fall time of the LNB1 output
22	TCAP2	Capacitor for setting the rise and fall time of the LNB2 output
23	$\overline{\text{SLEEP}}$	Disables LNB output, boost, I²C communication, and charge pump, to reduce input quiescent current to <15 µA
24	VREG	Analog supply
25	TDO2	Open-drain logic output that transitions low when a 22 kHz tone is present at the TDI2 pin
26	TDO1	Open-drain logic output that transitions low when a 22 kHz tone is present at the TDI1 pin
27	EPF	Early Power Failure warning comparator output
28	GND	Signal ground
29	VIN	Input supply voltage
30	LX1	Channel 1 internal boost switch drain node
31	GNDLX1	Channel 1 boost switch ground
32	BOOST1	Tracking supply voltage to channel 1 linear regulator
–	PAD	Exposed pad for thermal dissipation; connect to the ground plane

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ELECTRICAL CHARACTERISTICS[1] at T_A = 25°C, V_{IN} = 10 to 16 V, ● as noted[2], unless noted otherwise

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
General							
Output Voltage Accuracy	V_{OUTx}	V_{IN} = 12 V, I_{OUTx} = 10 mA, see table 3a for DAC settings	●	–2	–	2	%
Load Regulation	$\Delta V_{OUTx(Load)}$	V_{IN} = 12 V, V_{OUTx} = 13.667 V, ΔI_{OUTx} = 10 to 700 mA	●	–	75	120	mV
		V_{IN} = 12 V, V_{OUTx} = 19.000 V, ΔI_{OUTx} = 10 to 700 mA	●	–	85	150	mV
Line Regulation	$\Delta V_{OUTx(Line)}$	V_{IN} = 10 to 16 V, V_{OUTx} = 13.667 V, I_{OUTx} = 10 mA	●	–10	0	10	mV
		V_{IN} = 10 to 16 V, V_{OUTx} = 19.000 V, I_{OUTx} = 10 mA	●	–10	0	10	mV
Supply Current	$I_{IN(OFF)}$	ENB1 and ENB2 bits = 0, V_{IN} = 12 V		–	7	–	mA
	$I_{IN(ON)}$	ENB1 and ENB2 bits = 1, V_{IN} = 12 V, V_{OUTx} = 19 V, I_{LOAD} = 10 mA, TONECTRLx = 0		–	65	–	mA
		ENB1 and ENB2 bits = 1, V_{IN} = 12 V, V_{OUTx} = 19 V, I_{LOAD} = 10 mA, TONECTRLx = 1		–	85	–	mA
		$\overline{SLEEP}$ = 0 V, V_{IN} = 12 V, TONECTRLx = 0		–	–	15	µA
Boost Switch On Resistance	$R_{DS(on)BOOST}$	I_{LOAD} = 450 mA		–	300	–	mΩ
Switching Frequency	f_{SW}	FSW bit = 0		507	563	619	kHz
		FSW bit = 1		845	939	1032	kHz
Minimum COntrollable On-Time	$t_{ON(min)}$			–	85	–	ns
Linear Regulator Voltage Drop	ΔV_{REGx}	$V_{BOOSTx} – V_{LNBx}$, no tone signal, I_{LOAD} = 700 mA		600	800	1000	mV
TCAPx Pin Current	I_{CHGx}	TCAP capacitor (CTCAP in application drawings) charging		–13	–10	–7	µA
	$I_{DISCHGx}$	TCAP capacitor (CTCAP in application drawings) discharging		7	10	13	µA
Output Voltage Rise Time[3]	$t_{r(VLNB)}$	For V_{LNBx} 13→19 V; CTCAP (see application drawings) = 100 nF, I_{LOADx} = 700 mA		–	10	–	ms
Output Voltage Pull-Down Time[3]	$t_{f(VLNB)}$	For V_{LNBx} 19→13 V; C_{LOAD} = 100 µF, I_{LOADx} = 0 mA, SINK_DIS bit = 0		–	20	–	ms

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ELECTRICAL CHARACTERISTICS[1] (continued) at T_A = 25°C, V_{IN} = 10 to 16 V, ● as noted[2], unless noted otherwise

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Output Reverse Current	I_{RLNBx}	ENBx bit = 0		–	2	4	mA
		SINK_DIS bit = 1, ENBx bit = 1, TONECTRLx = 0		–	7	10	mA
		SINK_DIS bit = 0, ENBx bit = 1, TONECTRLx = 0, $\lvert V_{LNBx} - V_{SELx} \rvert$ < 1.5 V		–	25	40	mA
		SINK_DIS bit = 0, ENBx bit = 1, TONECTRLx = 1, $\lvert V_{LNBx} - V_{SELx} \rvert$ <1.5 V		–	60	85	mA
		SINK_DIS bit = 0, ENBx bit = 1, TONECTRLx = 0 or 1, $\lvert V_{LNBx} - V_{SELx} \rvert$ > 1.5 V		–	7	10	mA
LNBx Off Current	$I_{LNBx(OFF)}$	V_{IN} = 16 V		–	–	10	µA
General (continued)							
Ripple and Noise on LNBx Output[4]	$V_{ripn(pp)}$	20 MHz BWL; reference circuit shown in Functional Block diagram; contact Allegro for additional information on application circuit board design		–	30	–	mV_{PP}
VREG Voltage	V_{VREG}	V_{IN} = 10 V		4.97	5.25	5.53	V
ISETx Voltage	V_{ISETx}	V_{IN} = 10 V		3.4	3.5	3.6	V
TCAPx Voltage	V_{TCAPx}	V_{IN} = 10 V, V_{OUTx} = 13.667 V		–	2.28	–	V
		V_{IN} = 10 V, V_{OUTx} = 19.000 V		–	3.17	–	V
Protection Circuitry							
Output Overcurrent Limit[5]	$I_{OUTx(MAX)}$	R_{SETx} = 100 kΩ	●	220	300	380	mA
		R_{SETx} = 37.4 kΩ	●	720	800	880	mA
Overcurrent Disable Time	t_{DIS}	TDIS_T bit = 1		–	45	–	ms
		TDIS_T bit = 0		–	28	–	ms
Overcurrent Re-Enable Time	t_{REN}	RSMODE bit = 1		–	1	–	s
Boost MOSFET Current Limit	$I_{BOOSTx(MAX)}$	R_{SETx} = 100 kΩ		1300	1800	2300	mA
		R_{SETx} = 37.4 kΩ		2800	3300	3800	mA
VIN Undervoltage Lockout Threshold	V_{UVLO}	V_{IN} falling		8.05	8.35	8.65	V
VIN Turn-On Threshold	$V_{IN(th)}$	V_{IN} rising		8.40	8.70	9.00	V
I²C™ Undervoltage Lockout Threshold	V_{UVLO_I2C}	V_{IN} falling		–	5.5	–	V
I²C™ Turn-On Threshold	$V_{IN(th)\_I2C}$	V_{IN} rising		–	5.7	–	V
Undervoltage Hysteresis	$V_{UVLOHYS}$			–	350	–	mV
Thermal Shutdown Threshold[3]	T_J			–	165	–	°C

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ELECTRICAL CHARACTERISTICS[1] (continued) at T_A = 25°C, V_{IN} = 10 to 16 V, ● as noted[2], unless noted otherwise

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Thermal Shutdown Hysteresis[3]	ΔT_J			–	20	–	°C
Power Not Good (Low)	PNG_{xLOSET}	With respect to V_{LNBx} setting; V_{LNBx} low, PNG_x bit set to 1		88	91	94	%
	$PNG_{xLORESET}$	With respect to V_{LNBx} setting; V_{LNBx} low, PNG_x bit reset to 0		92	95	98	%
Power Not Good (Low) Hysteresis	PNG_{xLOHYS}	With respect to V_{LNBx} setting		–	4	–	%
Power Not Good (High)	PNG_{xHISET}	With respect to V_{LNBx} setting; V_{LNBx} high, PNGx bit set to 1		106	109	112	%
	$PNG_{xHIRESET}$	With respect to V_{LNBx} setting; V_{LNBx} high, PNGx bit reset to 0		102	105	108	%
Power Not Good (High) Hysteresis	PNG_{xHIHYS}	With respect to V_{LNBx} setting		–	4	–	%
Tone							
Amplitude	$V_{TONE(PP)x}$	I_{LNBx} = 0 to 700 mA, C_{LNBx} = 750 nF	●	500	700	900	mV_{PP}
Frequency	f_{TONEx}		●	20	22	24	kHz
Duty Cycle	D_{TONEx}			40	50	60	%
Rise Time	$t_{r(TONE)x}$			5	10	15	µs
Fall Time	$t_{f(TONE)x}$			5	10	15	µs
Tone Detection							
Amplitude	$V_{TDX(PP)x}$	Tone transmit		500	700	900	mV_{PP}
	$V_{TDR(PP)x}$	Tone receive, 22 kHz sine wave		250	650	900	mV_{PP}
Reject Amplitude, Low	$V_{TD(XMT)Lx}$	Tone transmit		–	–	250	mV_{PP}
	$V_{TD(RCV)Lx}$	Tone receive, 22 kHz sine wave		–	–	100	mV_{PP}
Reject Amplitude, High	$V_{TD(XMT)Hx}$	Tone transmit		–	–	1.1	V_{PP}
	$V_{TD(RCV)Hx}$	Tone receive, 22 kHz sine wave		–	–	1.1	V_{PP}
Frequency Capture	$f_{TD(RCV)x}$	Tone receive, 650 mV_{PP} sine wave		17	22	27	kHz
	$f_{TD(XMT)x}$	Tone transmit, 650 mV_{PP} sine wave		20	22	24	kHz
Frequency Reject, Low	$f_{TD(RCV)Lx}$	Tone receive, 650 mV_{PP} sine wave		12	14	–	kHz
	$f_{TD(XMT)Lx}$	Tone transmit, 650 mV_{PP} sine wave		15	17	–	kHz
Frequency Reject, High	$f_{TD(RCV)Hx}$	Tone receive, 650 mV_{PP} sine wave		–	34	37	kHz
	$f_{TD(XMT)Hx}$	Tone transmit, 650 mV_{PP} sine wave		–	30	33	kHz
Detection Delay	t_{DETx}	Tone receive, 650 mV_{PP}, 22 kHz sine wave		–	1.5	3	cycle
TDI Input Impedance	Z_{TDIx}			–	8.6	–	kΩ
TDO Output Voltage	$V_{TDO(L)x}$	Tone present, I_{LOAD} = 3 mA		–	–	0.4	V

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ELECTRICAL CHARACTERISTICS[1] (continued) at T_A = 25°C, V_{IN} = 10 to 16 V, ● as noted[2], unless noted otherwise

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
TDO Output Leakage	I_{TDOx}	Tone absent, 0 V < V_{TDO} < 5 V	–	–	10	µA
EPF Pin Threshold	V_{EPF_TH}	V_{IN} voltage falling	–	3.325	–	V
EPF Threshold Hysteresis	$V_{EPF\_TH\_hys}$		–	175	–	mV
BFGATE/LNB Voltage	V_{BFG_ON}	TONECTRLx = high	–	50	–	%
	V_{BFG_OFF}	TONECTRLx = low	–	99	–	%
Tone Control (TONECTRL pin)						
Logic Input	$V_{TNCTL(H)x}$		2.0	–	–	V
	$V_{TNCTL(L)x}$		–	–	0.8	V
Input Leakage Current	$I_{TNCTL(lkg)x}$		−1	–	1	µA
Sleep Mode Control ($\overline{SLEEP}$ pin)						
Logic Input	$V_{SLP(H)}$		2.0	–	–	V
	$V_{SLP(L)}$		–	–	0.8	V
Input Leakage Current	$I_{SLP(lkg)}$		–	50	–	µA
I²C™- Compatible Interface						
Logic Input (SDA and SCL pins)	$V_{SCL(L)}$		–	–	0.8	V
	$V_{SCL(H)}$		2.0	–	–	V
Logic Input Hysteresis	$V_{I2CIHYS}$		–	150	–	mV
Logic Input Current	I_{I2CI}	V_{I2CI} = 0 to 5 V	–10	<±1.0	10	µA
Logic Output Voltage (SDA and $\overline{IRQ}$ pins)	$V_{I2COUT(L)}$	I_{LOAD} = 3 mA	–	–	0.4	V
Logic Output Leakage Current (SDA and $\overline{IRQ}$ pins)	I_{I2CLKG}	$V_{I2COUT(L)}$ = 0 to 5 V	–	–	10	µA
SCL Clock Frequency	f_{CLK}		–	–	400	kHz
I²C™ Address Setting						
ADD Pin Voltage for Address 0001 000	Address1		0	–	0.7	V
ADD Pin Voltage for Address 0001 001	Address2		1.3	–	1.7	V
ADD Pin Voltage for Address 0001 010	Address3		2.3	–	2.7	V
ADD Pin Voltage for Address 0001 011	Address4		3.0	–	5.0	V

[1]Operation at 16 V may be limited by power loss in the linear regulator.
[2]Indicates specifications guaranteed from 0 ≤ T_J ≤ 125°C (min), design goal is 0 ≤ T_J ≤ 150°C.
[3]Guaranteed by worst case process simulations and system characterization. Not production tested.
[4]LNB output ripple and noise are dependent on component selection and PCB layout. Refer to the application schematic drawings and the PCB layout recommendations. Not production tested.
[5]Current from the LNB output may be limited by the choice of BOOST components.

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Functional Description

Boost Converter/Linear Regulator

The A8302 solution contains two tracking current-mode boost converters and Linear regulators. The boost converter tracks the requested LNB voltage to within 800 mV, to minimize power dissipation. Under conditions where the input voltage, V_{BOOSTx}, is greater than the output voltage, V_{LNBx}, the linear regulator must drop the differential voltage. When operating in these conditions, care must be taken to ensure that the safe operating temperature range of the A8302 is not exceeded.

The A8302 has internal pulse-by-pulse current limiting on the boost converter and DC current limiting on the LNB output to protect the IC against output short to GND faults.

Boost Converter Operation Under Light Load

At extremely light load or no load, if the BOOSTx voltage tries to exceed the BOOSTx target voltage, the boost converter operates with minimum on-time. The BOOSTx settling voltage depends on: supply voltage, boost inductance, minimum on-time, switching frequency, output power, as well as power loss in the boost inductor, capacitor, and the A8302. If the BOOSTx voltage tries to exceed 23.7 V, the optionally enabled adjustable sink is turned on. This internal sink helps to avoid pulse skipping and audible noise with ceramic capacitors on BOOSTx. The internal sink on BOOSTx gradually increases from 0 mA proportional to the result of V_{BOOSTx} – 23.7 V, and the sink current reaches a maximum value of 17.9 mA when V_{BOOSTx} reaches 27 V. Beyond this, if the BOOSTx voltage tries to exceed 27 V, the internal sink current on BOOSTx will be held at 17.9 mA till V_{BOOSTx} reaches 28 V. Beyond this, if the BOOSTx voltage tries to exceed 28 V, the A8302 enters into pulse skipping with 350 mV hysteresis. During pulse skipping the internal sink on BOOSTx is turned off when BOOSTx stops switching.

The optional internal sink on BOOSTx is enabled/disabled by setting/resetting Control Register 0 bit 7(SINK_NL). This bit is common to both channels. When the SINK_NL bit is set to 1, the adjustable internal sink is enabled. When the SINK_NL bit is set to 0, the internal sink on BOOSTx is disabled.

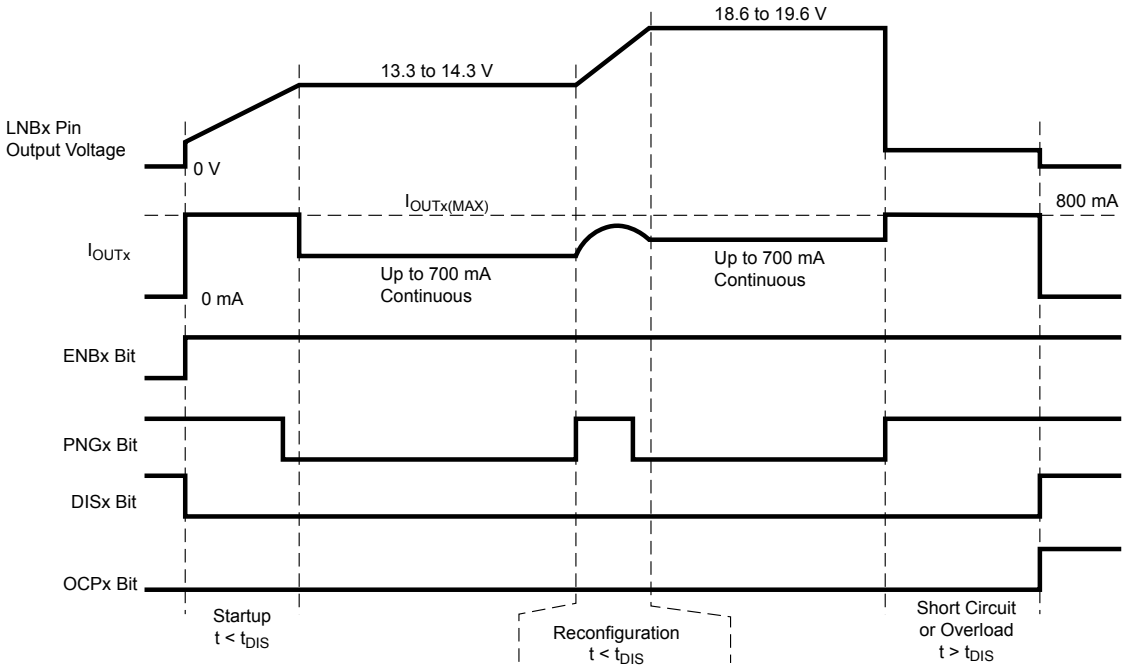

Figure 1. Startup, reconfiguration, and short circuit operation using R_{SETx} = 37.4 kΩ, and a capacitive load (OCPx_25P bit = 0)

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Multiple Outputs

In the case that two or more set top box LNB outputs are connected together by the customer (such as with a splitter), it is possible that one output could be programmed at a higher voltage than the other. This would cause a voltage on one output that is higher than its programmed voltage (for example, 19 V on the output of a 13 V programmed voltage). The output with the highest voltage will effectively turn off the other outputs. As soon as this voltage is reduced below the value of the other outputs, the A8302 output will auto-recover to its programmed levels.

Charge Pump

Generates a supply voltage above the internal tracking regulator output to drive the linear regulator control.

LNBx and BOOSTx Current Limits Setting

The LNB output current limit, $I_{OUTx(MAX)}$ can be set by connecting a resistor (RSETx) from the ISETx pin to GND as shown in the applications schematics. The LNBx current limit can be set from 300 to 1000 mA, corresponding to an R_{SETx} value of 100 to 30 kΩ, respectively. See figure 1 for a typical circuit timing example.

The LNBx output current limit can be set as high as 1000 mA (by selecting an R_{SETx} of 30 kΩ), but care should be taken not to exceed the thermal limit of the package, or thermal shutdown (TSD) will occur. The typical LNB output current limit can be set according to the following equation:

$$I_{OUTx(MAX)} = 29{,}925 / R_{SETx} ,$$

where $I_{OUTx(MAX)}$ is in mA and R_{SETx} is in kΩ.

If the voltage at the ISETx pin is 0 V (that is, shorted to GND), $I_{OUTx(MAX)}$ will be clamped to a moderately high value, 1.2 A. Care should be taken to ensure that ISETx is not inadvertently grounded. If no resistor is connected to the ISETx pin (that is, if ISETx is open-circuit), $I_{OUT(MAX)}$ will be set to approximately zero amps and the A8302 will not support any load (OCP will occur prematurely).

The BOOSTx pulse-by-pulse current limit, $I_{BOOSTx(MAX)}$, is automatically scaled along with the LNBx output current limit. The typical BOOSTx current limit is set according to the following equation:

$$I_{BOOSTx(MAX)} = 3.0 \times I_{OUTx(MAX)} + 900 \text{ (mA)} ,$$

where both $I_{BOOSTx(MAX)}$ and $I_{OUTx(MAX)}$ are in mA.

Automatically scaling the BOOSTx current limit allows the designer to choose the lowest possible saturation current of the boost inductor, reducing its physical size and PCB area, thus minimizing cost.

Protection

The A8302 has a wide range of protection features and fault diagnostics which are detailed in the Status Register section.

Undervoltage Lockout (UVLO)

The Undervoltage Lockout (UVLO) comparator monitors the voltage at the VIN pin and keeps the regulator disabled if the voltage is below the lockout threshold, $V_{IN(th)}$. The UVLO comparator incorporates enough hysteresis, $V_{UVLOHYS}$, to prevent on-off cycling of the regulator due to IR drops in the VIN path during heavy loading or during startup.

Overload and Short Circuit Handling

The A8302 protects the IC against output overload and short circuit. The short circuit disable timer is controlled with the TDIS_T bit. If this bit is set to 1, the IC allows an overcurrent condition to persist up to 45 ms and if this bit is set to 0, the maximum overcurrent time allowed is 28 ms. The A8302 provides the option either to latch or to auto-restart on fault. If the RSMODE bit is set to 1, with an overcurrent condition that exceeds typically 45 ms (TDIS_T set to 1) or 28 ms (TDIS_T set to 0), the IC turns off output for 1 s and then auto-restarts with the previous settings. This hiccup mode continues as long as output current is greater than the OCP level. The device returns to normal operation when the fault is removed. If RSMODE is set to 0, the IC turns off after t_{DIS} time expires, and remains latched. Figures 2a and 2b explain overcurrent protection operation with RSMODE at 1 and at 0.

The A8302 has an optional 25% bump up on the current limit for t_{dis} /4 period. This feature is enabled/disabled by setting or resetting Control Register 2 bits 0 and 1 for channel 1 and channel 2 respectively. When this bit is enabled, the output current limit is 25% more than the set current limit, or 1000 mA (max), for both limits a minimum of t_{dis} /4 period. After the t_{dis}/4 period, the output current limit comes down to the set limit and the OCPx_25P bit is reset to zero, The user must set this bit again to enable the 25% bump up at the next current limit event. If the OCPx_25P bit is zero when LNBx output is shorted to ground, the LNBx output current will be clamped to $I_{OUTx(MAX)}$. If the short circuit condition lasts for more than 45 ms, the A8302 will be disabled and the OCPx bit will be set. Refer to figures 16a and 16b.

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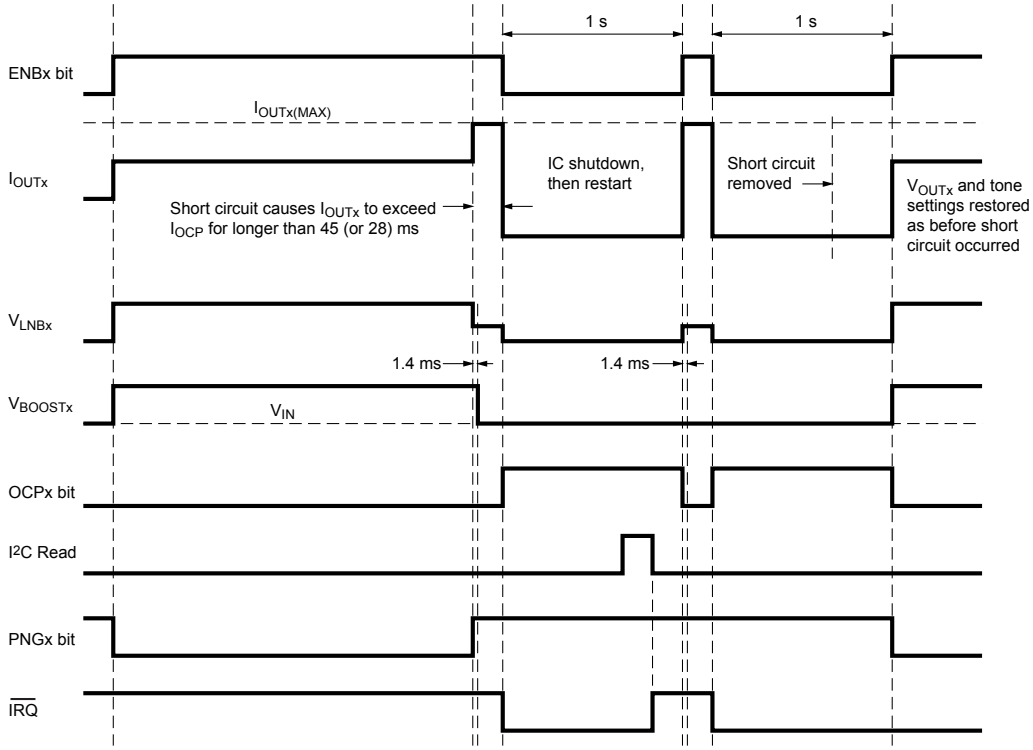

Figure 2a. $\overline{IRQ}$ and Fault Clearing in Response to Overcurrent (OCP) with auto-retry enabled (RSMODE = 1) and an OCP delay of 45 (or 28) ms (TDIS_T = 1 (or 0)). $\overline{IRQ}$ transitions to low at an OCP fault and is reset by an I²C Read sequence. The OCP bit clears automatically after 1 s, and the device restarts with the previous settings. This hiccup mode continues as long as the output current is greater than the OCP level. The device returns to normal operation when the fault is removed.

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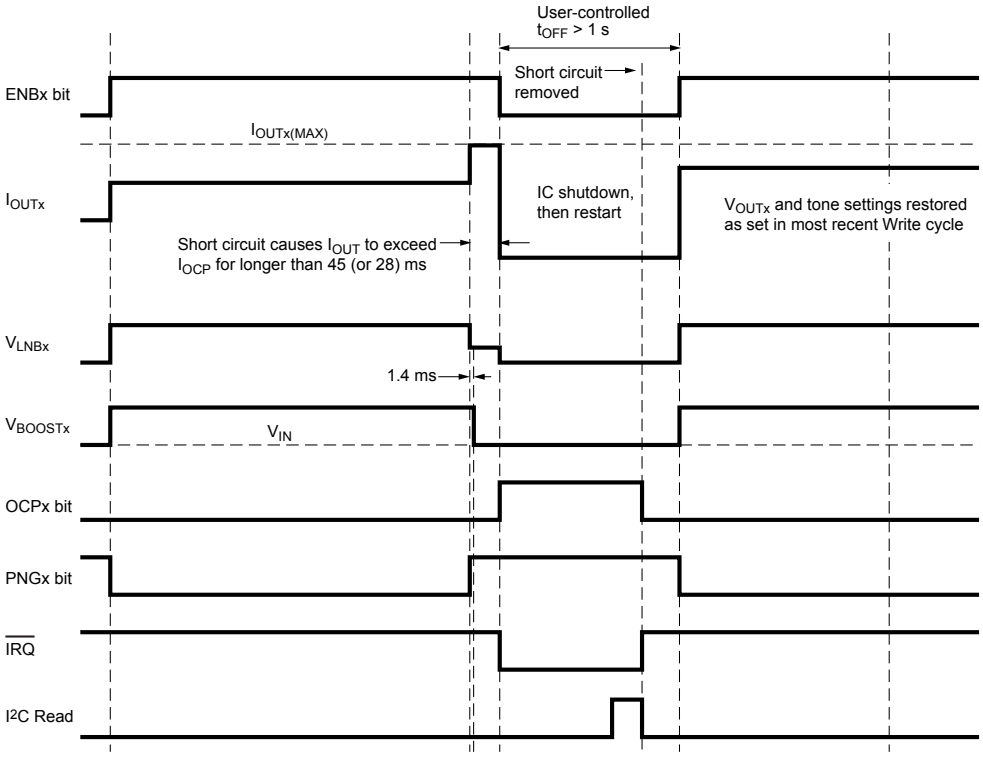

Figure 2b. $\overline{IRQ}$ and Fault Clearing in Response to Overcurrent (OCP) with latch mode (RSMODE = 0) and an OCP delay of 45 (or 28) ms (TDIS_T = 1(or 0)). $\overline{IRQ}$ transitions low at an overcurrent fault, and an I²C Read sequence clears the OCP bit and $\overline{IRQ}$. An I²C Write sequence is required to reenable the part. The retry wait time should be longer than 1 s, to prevent TSD.

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Switching Frequency Selection

The A8302 offers two switching frequencies: 563 kHz and 939 kHz. High switching frequency allows minimizing the component size, which also increases switching losses. Use a high switching frequency setting to optimize component size and take care of A8302 power dissipation. High switching frequency is preferred for low output current applications. Where the A8302 power dissipation is of a concern, use a low switching frequency setting. Refer to application schematic section for details. Switching frequency is adjusted using Control Register 0, bit 4. User program should select a correct switching frequency setting for which the hardware is designed.

Compensation Network Selection

The A8302 is designed to work with ceramic or electrolytic capacitors on BOOST output. Boost loop compensation required is different for ceramic and electrolytic capacitor options. The proper compensation network is selected by setting Control Register 0, bit 5. User program should select a correct compensation network setting based on the boost capacitor selection.

When V_{IN} goes below UVLO level, all control registers are reset to default value, that is, 0. The user must write proper bits upon each power-up. Application based bits all are bunched into Control Register 0, which are normally not required to change during operation. Switching frequency, compensation network, and overcurrent disable delay bits must not be changed during operation.

Slew Rate Control

During either startup, or when the output voltage at the LNBx pin is transitioning, the output voltage rise and fall times can be set by the value of the capacitor connected from the TCAPx pin to GND (CTCAPx in the applications schematics). Note that during start-up, the BOOSTx pin is pre-charged to the input voltage minus a diode voltage drop. As a result, the slew rate control for the BOOSTx pin occurs from this voltage. See figure 3.

The value of CTCAPx can be calculated using the following formula:

$$\text{CTCAPx} = (I_{\text{TCAPx}} \times 6) / \text{SR} \ ,$$

where SR is the required slew rate of the LNB output voltage, in V/s, and I_{TCAPx} is the TCAPx pin current specified in the Electrical Characteristics table. The recommended value for CTCAPx, 100 nF, should provide satisfactory operation for most applications.

The minimum value of CTCAPx is 10 nF. There is no theoretical maximum value of CTCAPx however too large a value will probably cause the voltage transition specification to be exceeded. Tone generation is unaffected by the value of CTCAPx .

Pull-Down Rate

In applications that have to operate at very light loads and that require large load capacitances (in the order of tens to hundreds of microfarads), set the SINK_DIS bit to 0, so the output linear

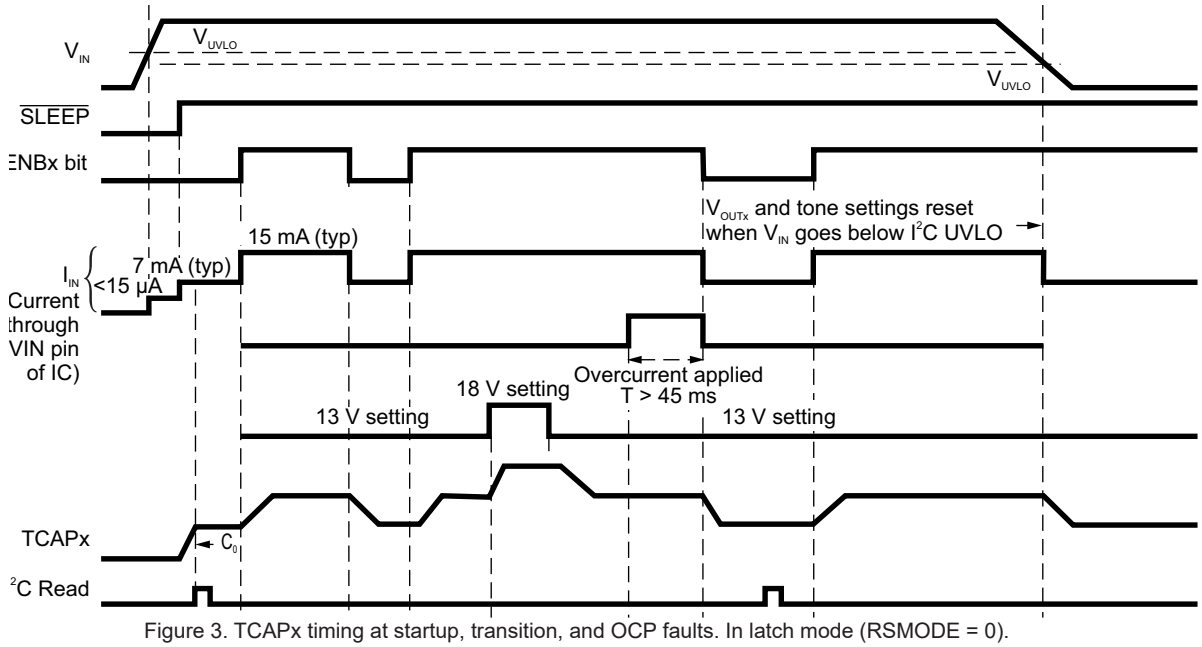

Figure 3. TCAPx timing at startup, transition, and OCP faults. In latch mode (RSMODE = 0).

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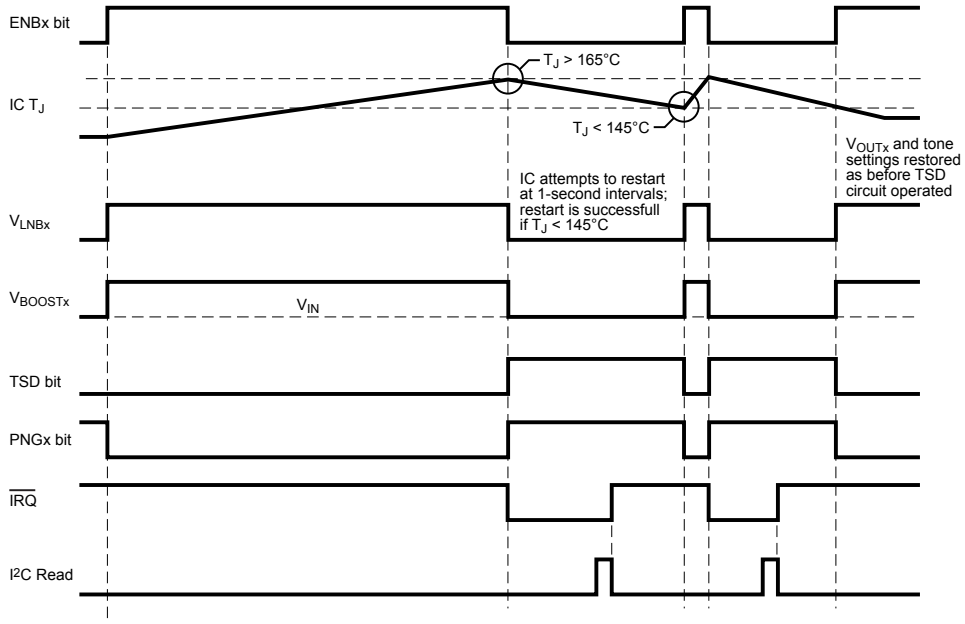

Figure 4a. $\overline{IRQ}$ and Fault Clearing in Response to Overtemperature (TSD) with auto-retry (RSMODE = 1). If for any reason the junction temperature exceeds 165°C (typ), the device LNBx output and the boost converter are disabled. The IC attempts to restart at 1-second intervals, but the LNBx output restarts only when T_J cools below 145°C. The $\overline{IRQ}$ pin resets on an I²C Read sequence, and the TSD bit resets along with an LNBx output restart.

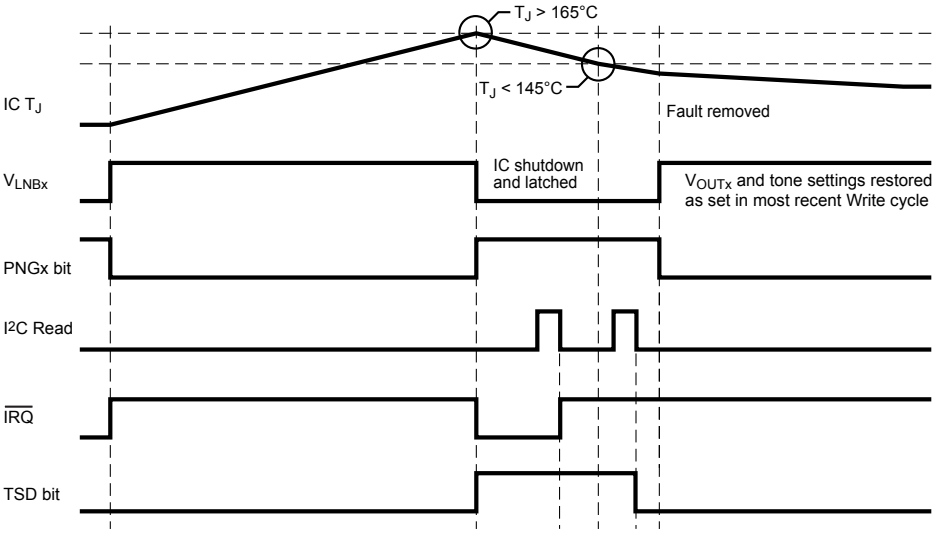

Figure 4b. $\overline{IRQ}$ and Fault Clearing in Response to Overtemperature (TSD) with latch mode (RSMODE = 0). $\overline{IRQ}$ transitions low after TSD fault, and an I²C Read sequence immediately resets the $\overline{IRQ}$ pin. The TSD bit is cleared by an I²C Read sequence only after the device has cooled to a T_J below 145°C. An I²C Write sequence is required to reenable the device.

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stage provides approximately 25 mA of pull-down capability. This ensures that the LNBx output voltage is ramped from 18 to 13 V in a reasonable amount of time. When the tone is on, the output linear stage increases its pull-down capability to approximately 60 mA. This ensures that the tone signal meets all specifications, even with no load on the on the LNBx output.

Thermal Shutdown (TSD)

The A8302 protects the IC against overheating. If junction temperature exceeds 165°C (typ), LNBx output and the boost converter output are disabled until T_J cools below 145°C. The A8302 provides the option either to latch or to auto-restart on fault. If the RSMODE bit is set to 1, the A8302 IC attempts to restart at 1-second intervals, but restart is successful only with T_J < 145°C. This hiccup mode continues as long as T_J > 145°C. The device returns to normal operation when the fault is removed. If RSMODE is set to 0, the IC turns off, and remains latched. Figures 4a and 4b explain thermal shutdown protection operation with RSMODE at 1 and at 0.

SINK_DIS Mode Selection

The A8302 SINK_DIS bit allows to select the maximum output reverse current. When the SINK_DIS bit is set to 1, the maximum LNBx back feed current, I_{RLNBx}, is less than 10 mA. When the outputs of the LNBx converters are shorted, a 10 mA back feed current will prevent loading of one converter output by another converter output.

Sleep Mode

The A8302 includes a sleep mode that instantly turns off the LNBx output and resets the internal Control register to its default (power-on) state. When the $\overline{\text{SLEEP}}$ pin is low, the A8302 will draw $I_{IN(OFF)}$ less than 15 µA from the input supply.

In-Rush Current

At startup or during an LNB Reconfiguration event, a transient surge current above the normal DC operating level can be provided by the A8302. This current increase can be as high as the set output current.

Tone Generation

The A8302 offers two options for tone generation (figure 5). The TONECTRLx pin with the TMODE control bit provides the necessary control. The TMODE bit controls whether the tone source is internal or external.

When the internal source is used (TMODE bit set to 0), the tone is gated with the TONECTRLx pin. The internal tone frequency is 22 kHz. Note: This tone can be generated under no-load conditions and does not require an external DiSEqC™ filter.

When the TMODE bit is set to 1, an external 22-kHz tone signal can be applied to the TONECTRLx pin. This tone frequency appears at the LNBx output. V_{OUTx} reaches the V_{LNBref} level after TONECTRLx has been low for longer than 42 µs.

Tone Detection

A 22-kHz tone detector is provided in the A8302. The detector extracts the 22 kHz signal from the AC-coupled TDIx pin and provides it as an open-drain logic output at the TDOx pin. Also, when a tone is present, the TDET bit in the Status register is set to 1 and can be seen via the I²C interface. The tone detection delay is typically shorter than 1.5 cycles.

The tone detector dynamically adjusts its amplitude and frequency thresholds depending on whether the A8302 is transmitting or receiving a tone signal. If the A8302 is transmitting, the tone detect amplitude threshold is relatively high and the acceptable frequency range is tight. This provides a high quality tone signal is always generated by the A8302. Conversely,

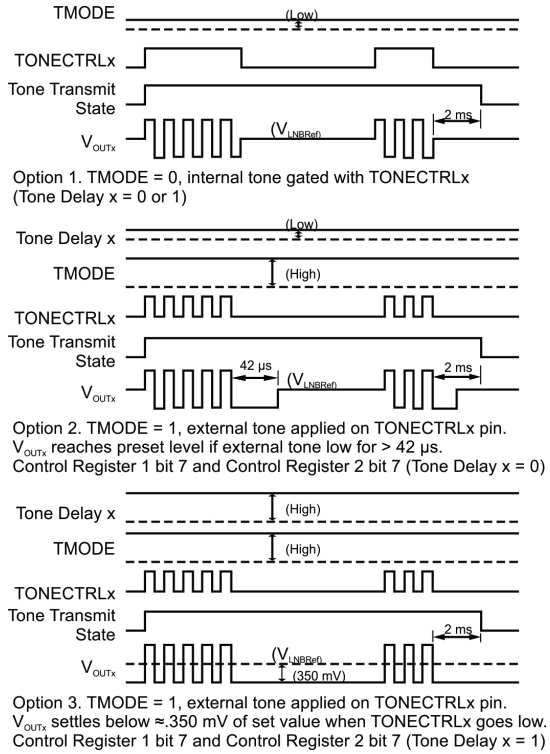

Figure 5. Options for tone generation

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if the A8302 is receiving, the tone detect amplitude threshold is reduced and the acceptable frequency range is increased slightly. This provides the A8302 has maximum sensitivity to remotely generated tone signals that may be degraded by long lengths of coaxial cable. The Electrical Characteristics table of this datasheet documents the guaranteed specifications of the tone detector and how they are adjusted by tone transmission or receiving mode.

To help in the understanding, typical tone detector operation is shown graphically in figures 6a and 6b. The shaded areas in figure 6a indicate the accept range of the detector when TONECTRLx is a logic high (transmit) and a logic low (receive). The shaded areas in figure 6b indicate the reject range of the detector when TONECTRLx is a logic high (transmit) and a logic low (receive).

Early Power Failure Warning (EPF)

The EPF signal gives the microcontroller early warning that the supply voltage is falling below the EPF threshold value, so the microcontroller can start to shed non-critical loads (such as the LNBR) and begin its shutdown routines.

When the voltage on the EPF pin falls below V_{EPF_TH}, the EPF bit is set and IRQ is pulled low. When the EPF pin voltage goes above $V_{EPF\_TH} + V_{EPF\_TH\_hys}$, the EPF bit is reset after the programmed delay. The EPF bit resets automatically when the EPF pin voltage goes above $V_{EPF\_TH} + V_{EPF\_TH\_hys}$.

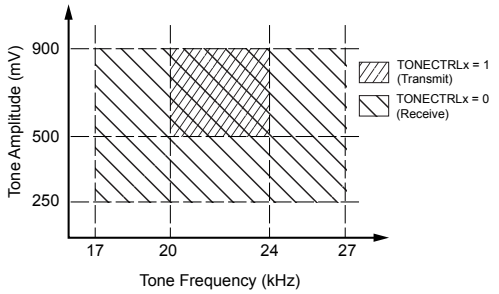

Figure 6a. Accept ranges of Tone Detection feature

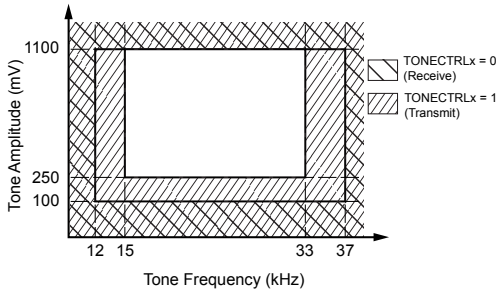

Figure 6b. Reject ranges of Tone Detection feature

The delay between when the EPF pin voltage goes to $V_{EPF\_TH} + V_{EPF\_TH\_hys}$ and when the EPF bit is reset, is programmed by the EPF0 and EPF1 bits. See table 3b for description.

The following examples explain selection of resistors R1 and R2 to set the EPF warning when V_{IN} falls to 10.5 V or 7 V.

Case 1: EPF warning when V_{IN} falls to 10.5 V

Assume:

Nominal Input Voltage = 12 V,

V_{EPF_TH} = 3.5 V,

$V_{EPF\_TH\_hys}$ = 0.175 V, and

EPF_TH1 (V_{IN} corresponding to setting EPF bit) = 10.5 V.

Given:

$V_{EPF\_TH} = EPF\_TH1 \times R_2/(R_1 + R_2)$, where

$R_2/(R_1 + R_2) = 3.5/10.5 = 1/3$, then

choose R2 = 10 kΩ, R1 = 20 kΩ.

Given:

$V_{EPF\_TH} = EPF\_TH2 \times R_2/(R_1 + R_2)$, then

EPF_TH2 (V_{IN} corresponding to resetting EPF bit) = 11 V

Case2: EPF warning when V_{IN} falls to 7 V

Assume:

Nominal Input Voltage = 12 V,

V_{EPF_TH} = 3.5 V,

$V_{EPF\_TH\_hys}$ = 0.175 V, and

EPF_TH1 (V_{IN} corresponding to setting EPF bit) = 7 V.

Given:

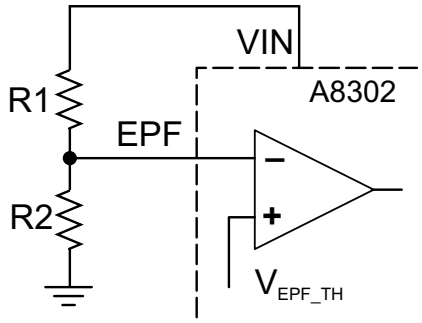

Figure 7. Example circuit for Early Power Failure feature

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$V_{EPF\_TH} = EPF\_TH1 \times R_2 / (R_1 + R_2)$, where

$R_2 / (R_1 + R_2) = 3.5 / 7 = 1 / 2$, then

choose R2 = 10 kΩ, R1 = 10 kΩ.

Given:

$V_{EPF\_TH} + V_{EPF\_TH\_hys} = EPF\_TH2 \times R_2 / (R_1 + R_2)$

EPF_TH2 (V_{IN} corresponding to resetting EPF bit) = 7.35 V.

Cable Disconnect Detection

A8302 does not go to pulse skipping if the BOOSTx voltage settles below 28V(typ), this facilitates increased boost voltage can be used to detect the cable disconnect . If the given application and supply voltage will ensure BOOSTxH voltage exceed 23.7V (typ) at no -load , Status register 1 bits BOOSTxH can be used for cable disconnect detection .

For the application requirements shown in schematic 3 and 4 at Vin= 12+/-5% , Boost voltage is expected to exceed 23.7V and which sets status register 1 bits BOOSTxH to high. Host controller can decode these bits t for the cable disconnect detection.

In the applications where Boost voltage cannot exceed 23.7V (typ) at no-load , A simple potential divider connection on BOOST, as shown in Figure 8, is used to sense the BOOST voltage. When the voltage on EPF pin is below V_{EPF_TH} , the EPF bit is set to 1. When voltage on the EPF pin exceeds $V_{EPF\_TH} + V_{EPF\_TH\_hys}$, the EPF bit is reset to 0. The combination of Rc1 and Rc2 is selected such that, when the cable is disconnected, the voltage on the EPF pin exceeds $V_{EPF\_TH} + V_{EPF\_TH\_hys}$ and resets the EPF bit to 0; otherwise the EPF bit is set to 1.

To enable the cable disconnect test, set the LNB output voltage to 13.333 V and read the Status register bit. If the EPF bit is reset, the cable is disconnected, otherwise the cable is connected. When the cable disconnect feature is used, the EPF pin senses the BOOST voltage, so the Early Power Failure warning (EPF) feature cannot be used.

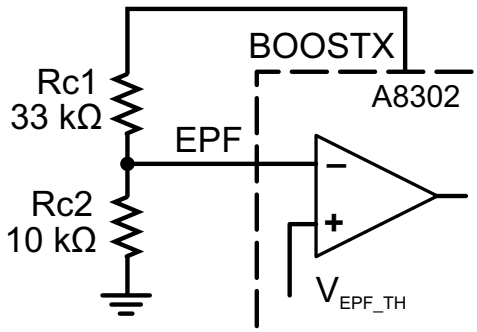

Figure 8. Cable Disconnect Detection

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Component Selection

Boost Inductor

The A8302 is designed to operate with a boost inductor value of either 10 µH ±30% (Set Fsw bit =0) or 4.7 µH ±30% (Set Fsw bit =1) with a DCR less than 75 mΩ. The error amplifier loop compensation, current sense gain, and PWM slope compensation were chosen for this value of inductor. The boost inductor must be able to support the peak currents required to maintain the maximum LNBx output current without saturating. Figure 9a can be used to determine the peak current in the inductor given the LNBx load current. The curve labeled Typical uses VIN = 12 V, VBOOST = 20 V, L = 10 µH, and f = 563 kHz, while the curve labeled Maximum assumes VIN = 10.8 V, VBOOST = 21 V, L = 7 µH, and f = 507 kHz.

Figure 9b can be used to determine the peak current in the inductor tor given the LNBx load current. The curve labeled Typical uses VIN = 12 V, VBOOST = 20 V, L = 4.7 µH, and f = 939 kHz, while the curve labeled Maximum assumes VIN = 10.8 V, VBOOST = 21 V, L = 3.3 µH, and f = 845 kHz

Boost Ceramic Capacitor Option

The A8302 can be configured to operate with two or three, high-quality ceramic capacitors on the boost node. Allegro recommends capacitors that are rated at least 35 V, ±10%, X7R, 1210

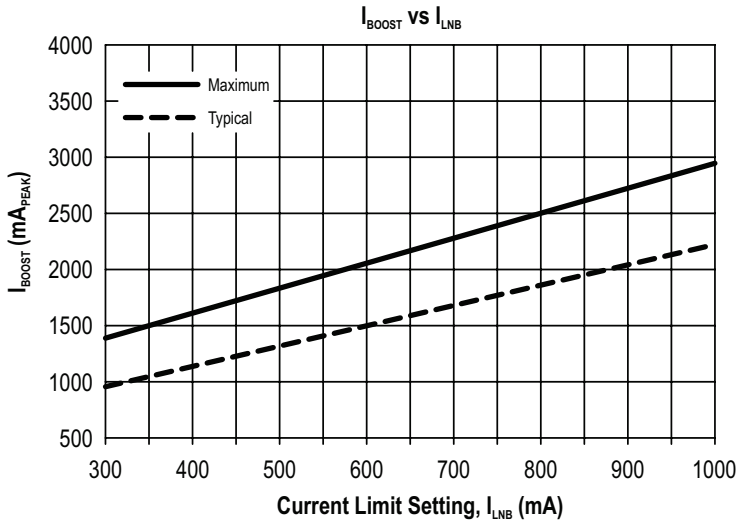

Figure 9a. Boost inductor peak current versus ILNB for the A8302 (L= 10uH, Fsw bit =0)

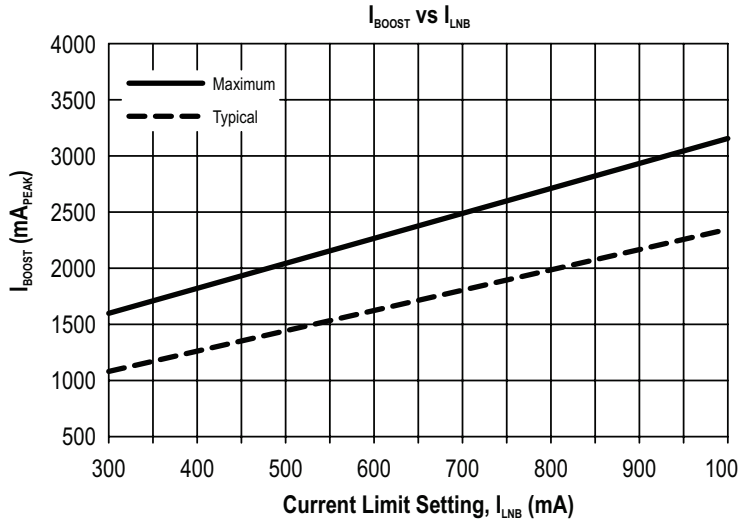

Figure 9b. Boost inductor peak current versus ILNB for the A8302 (L= 4.7uH, Fsw bit =1)

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Table 1a. Recommended Boost Capacitor Characteristics for Ceramic Capacitor Option

Quantity of Capacitors in Parallel	Value of Each Capacitor (µF)	Tolerance (%)	Rating (V)	Temperature Coefficient of Capacitance	Size
3	4.7	±10	50	X7R	1210
2	10	±10	35	X7R	1210

Table 1b. Recommended Boost Capacitor Characteristics for Electrolytic Capacitor Option

Quantity of Capacitors in Parallel	Value of Each Capacitor (µF)	Tolerance (%)	Rating (V)	Temperature Coefficient of Capacitance	Size
1	100	±25	35	–	–

size. Physically smaller capacitors, such as the 0603 and 0805, with lower temperature ratings, such as X5R and Z5U, should be avoided.

The nominal boost capacitance should total 14.1 to 20 µF. Allegro recommends either three 4.7 µF or two 10 µF capacitors, with the characteristics shown in table 1.

Figure 10 provides typical and maximum values of rms current required for a given LNR current:

Rating	V_{IN} (V)	V_{OUT} (V)	L (µH)	f_{SW} (kHz)
Typical	12	19	10	563
Maximum	9	20	7	507

Two possible ceramic based capacitor solutions have been presented. Other capacitor combinations are certainly possible, such as a very low ESR electrolytic capacitor in parallel with several microfarads of ceramic capacitance. However, there are two critical requirements that must be satisfied: 1) the zero formed by the electrolytic capacitor and its ESR should be at least 1 decade higher than the 0 dB crossover of the boost loop (typically around 25 kHz), and 2) the ceramic capacitors must eliminate the high frequency switching spikes/edges in the boost voltage, or the LNB output noise will be too high.

Boost Electrolytic Capacitor Option

The A8302 can be configured to operate with a low-ESR electrolytic boost capacitor of 100 µF ±25%. The ESR of the boost capacitor must be less than 150 mΩ or the boost converter will be unstable. General purpose electrolytic capacitors that do not specify an ESR should be avoided. Allegro recommends an electrolytic capacitor that is rated to support at least 35 V and has an rms current rating to support the maximum LNBx load. Figure 9 can be used to determine the necessary rms current rating of the boost capacitor given the LNBx load current.

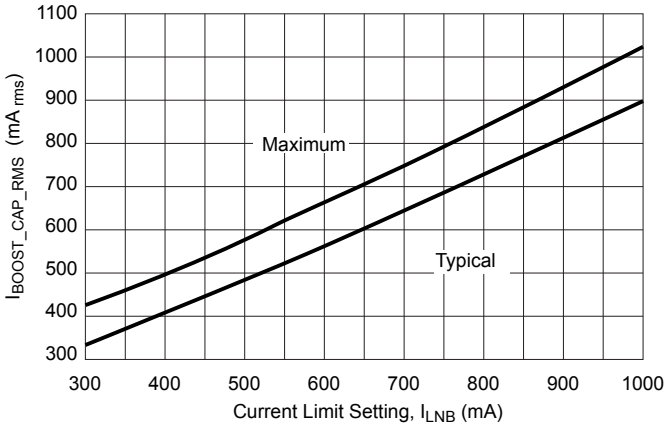

Figure 10. Boost capacitor rms current versus I_{LNB}

BOOSTx Filtering and LNBx Noise

The LNBx output noise depends on the amount of high-frequency noise at the BOOSTx pin. To minimize the high-frequency noise at the BOOSTx pin, the ceramic capacitors should be placed as close as possible to the BOOSTx pin.

Surge Components

Set-top–box suppliers have increased their surge specifications to require surge to failure of the TVS, or ±4000 V, whichever

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occurs first. These increased surge voltages produce significantly more current in both the external circuitry and the A8302. Allegro surge testing has shown that the SMDJ20A and LNBTVS6-221 usually fail at approximately 43 V, so all of the LNBR output components (ceramic capacitors, diodes, and so forth) should support at least 50 V.

To protect at these higher voltage/current levels three modifications must be made:

• For increased positive surge, the shunting diode from the LNBx pin to the BOOSTx pin (D3, 3 A/40 V) is no longer adequate to protect the body diode of the output stage. This diode must be increased to a 3 A/50 V device and be located so that it is in series with the BOOSTx pin as shown in application schematics 3 and 4. In this position D3 will block surge current to the majority of the boost capacitance, but the 1 µF ceramic capacitor will still filter the high frequency switching noise.

• For increased negative surge, the relatively small clamping diode (D2) from the LNBx pin to ground is no longer adequate. This diode must be increased from a 1 A / 40 V, SOD123 device to a 3 A / 50 V, SMA.

• For a DiSEqC 1.0 application, a 0.47 Ω / 1% / 0.25 W series resistor must be added as shown in the application schematics. The 0.47 Ω rating could be reduced if there is enough equivalent resistance in any series output components such as jumpers, inductors, or PCB traces. Every application will have its own surge requirements and the surge solution can be changed. However, Allegro strongly recommends incorporating a form of surge protection to prevent any pin of the A8302 from exceeding its Absolute Maximum voltage ratings shown in this datasheet.

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I²C™-Compatible Interface

The I²C™ interface is used to access the internal Control and Status registers of the A8302. This is a serial interface that uses two lines, serial clock (SCL) and serial data (SDA), connected to a positive supply voltage via a current source or a pull-up resistor. Data is exchanged between a microcontroller (master) and the A8302 (slave). The master always generates the SCL signal. Either the master or the slave can generate the SDA signal. The SDA and SCL lines from the A8302 are open-drain signals, so multiple devices may be connected to the I²C™ bus. When the bus is free, both the SDA and the SCL lines are high.

SDA and SCL Signals

SDA can only be changed while SCL is low. SDA must be stable while SCL is high. However, an exception is made when an I²C™ Start or Stop condition is encountered. See the I²C™ Communications section for further details.

Acknowledge (AK) Bit

The Acknowledge (AK) bit indicates a valid transmission and can be used in two ways. First, if the slave successfully receives eight bits of either an address or control data, it pulls the SDA line low (AK set to 0) for the ninth SCL pulse to signal a valid transmission to the master. Second, if the master successfully receives eight bits of status data from the A8302, it pulls the SDA line low for the ninth SCL pulse to signal a valid transmission to the slave. The recipient (either the master or the slave) should set the AK bit high (AK set to 1, also referred to as NAK) for the ninth SCL pulse if eight bits of data were not received successfully.

Acknowledge Bit During a Write Sequence

When the master sends control data (writes) to the A8302 there are three cases where AK bits are sent by the A8302. First, the A8302 uses the AK bit to indicate reception of a valid seven-bit chip address plus a Read/Write bit (with R/W set to 0 for a Write). Second, the A8302 uses the AK bit to indicate reception of a valid eight-bit Control register address. Third, the A8302 uses the AK bit to indicate reception of eight bits of control data. This protocol is shown in figure 11a.

Acknowledge Bit During a Read Sequence

When the master reads status data from the A8302 there are four cases where AK bits are sent: three are sent by the A8302 and one is sent by the master. First, the A8302 uses the AK bit to indicate reception of a valid seven-bit chip address plus a Read/Write bit (with R/W set to 0 for a Write). Second, the A8302 uses the AK bit to indicate reception of a valid eight-bit Status register address. Third, the A8302 uses the AK bit to indicate reception of a valid seven-bit chip address plus a Read/Write bit (with R/W set to 1 for a Read). Finally, the master uses the AK bit to indicate receiving eight bits of status data from the A8302. This protocol is shown in figure 11b.

I²C™ Communications

I²C™ Start and Stop Conditions

The I²C™ Start condition is defined by a negative edge on the SDA line while SCL is high. Conversely, the Stop condition is defined by a positive edge on the SDA line while SCL is high. The Start and Stop conditions are shown in figures 10a and 10b. It is possible for a Start or Stop condition to occur at

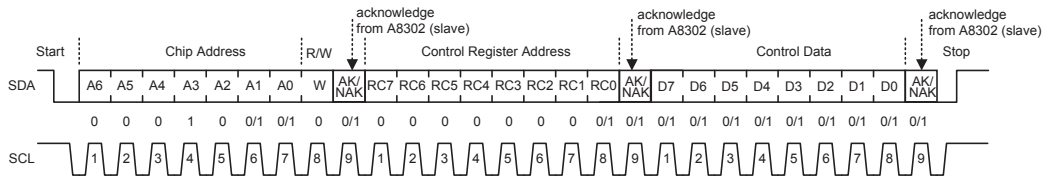

Figure 11a. I²C™ Interface Write to Control registers sequence

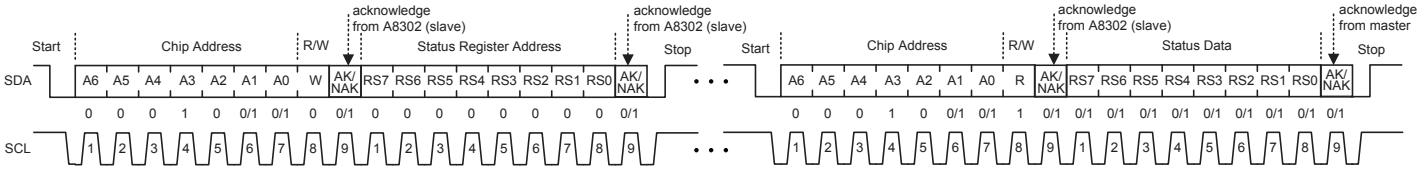

Figure 11b. I²C™ Interface Read from Status register sequence

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any time during a data transfer. If either a Start or Stop condition is encountered during a data transfer, the A8302 will respond by resetting the data transfer sequence.

I²C™ Write Sequence Description

Writing to the A8302 Control register requires transmission of a total of 27 bits: three 8-bit bytes of data plus an AK bit after each byte. The Write sequence to the A8302 Control registers is shown in figure 10a. Writing to the A8302 Control registers requires: an I²C™ Start condition, a chip address with the R/W bit set to 0, the Control register address, the control data, and an I²C™ Stop condition as follows:

• The Chip Address cycle consists of a total of nine bits: seven bits of chip address (A6 to A0) plus one R/W bit (set to 0 to indicate a Write) from the master, followed by an AK bit (set to 0 to indicate reception of a valid chip address) from the slave. The cycle begins with a Start condition. The chip address must be transmitted MSB (A6) first. The first five bits of the A8302 chip address (A6 to A2) are fixed as 00010. The remaining two bits (A1 and A0) are used to select one of four possible A8302 chip addresses. The DC voltage on the ADD pin programs the chip address. See the Electrical Characteristics table for the ADD pin voltages and the corresponding chip addresses.

• The Control Register Address cycle consists of a total of nine bits: eight bits of Control register address (RC7 to RC0) from the master followed by an AK bit (set to 0 to indicate reception of a valid register address) from the slave. The Control register address must be transmitted MSB (RC7) first. The A8302 has two Control registers, with register addresses of 0000 0000 and 0000 0001.

• The Control Data cycle consists of a total of nine bits: eight bits of control data (D7 to D0) from the master, followed by an AK bit (set to 0 to indicate reception of eight valid bits) from the slave. The control data must be transmitted MSB (D7) first. The Control registers bits are identified in the Control Registers section of this datasheet. The cycle concludes with a Stop condition.

I²C™ Read Sequence Description

Reading from the A8302 Status register requires transmission of a total of 36 bits: four 8-bit bytes of data, plus an AK bit after each byte. The Read sequence from the A8302 Status register is shown in figure 10b. Reading the A8302 Status register requires: an I²C™ Start condition, a chip address with the R/W bit set to 0, the Status register address, an I²C™ Stop condition, an I²C™ Start condition, a repeat of the chip address with the R/W bit set to 1, the status data, and an I²C™ Stop condition, as follows:

• The Chip Address cycle is identical to the Chip Address cycle previously described for the Write sequence.

• The Status Register Address cycle consists of a total of nine bits: eight bits of Status register address (RS7 to RS0) from the master, followed by an AK bit from the slave. The Status register address must be transmitted MSB (RS7) first. The A8302 has only one Status register, so the Status register address is fixed at 0000 0000. The cycle concludes with a Stop condition.

• The Repeat Chip Address cycle is identical to the Chip Address cycle previously described for the Write sequence.

• The Status Data cycle consists of a total of nine bits: eight bits of status data (RD7 to RD0) from the slave, followed by an AK bit from the master. The status data is transmitted MSB (RD7) first. The Status register bits are identified in the Status Registers section of this datasheet. The cycle concludes with a Stop condition.

Interrupt Request ($\overline{\text{IRQ}}$) Pin

The A8302 provides an interrupt request pin, $\overline{\text{IRQ}}$, which is an open-drain, active low output. This output may be connected to a common IRQ line with a suitable external pull-up resistor and can be used with other I²C™ compatible devices to request attention from the master controller.

The $\overline{\text{IRQ}}$ output becomes active (logic low) when the A8302 recognizes a fault condition. The fault conditions that will force $\overline{\text{IRQ}}$ active include Early Power Failure (EPF), undervoltage lockout (UVLO), overcurrent protection (OCP), and thermal

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shutdown (TSD). The UVLO, OCP (RSMODE bit set to 0), and TSD (RSMODE bit set to 0) faults are latched in the Status register and are not unlatched until the A8302 Status register is successfully transmitted to the master controller (an AK bit must be received from the master). See the description in the Status Register section and figure 12 for further details.

When the master device receives an interrupt, it should address all slaves connected to the interrupt line in sequence and read the Status register of each to determine which device is requesting attention.

The LNBx output disable (DISx bit set to 1) and Power Not Good (PNGx bit set to 1) conditions do not cause an interrupt. and are not latched in the Status register.

Figures 12, 13, 14, and 15 show the fault handling timing for UVLO in various conditions: startup and shutdown, and relative V_{REF}, V_{IN}, and EPF conditions.

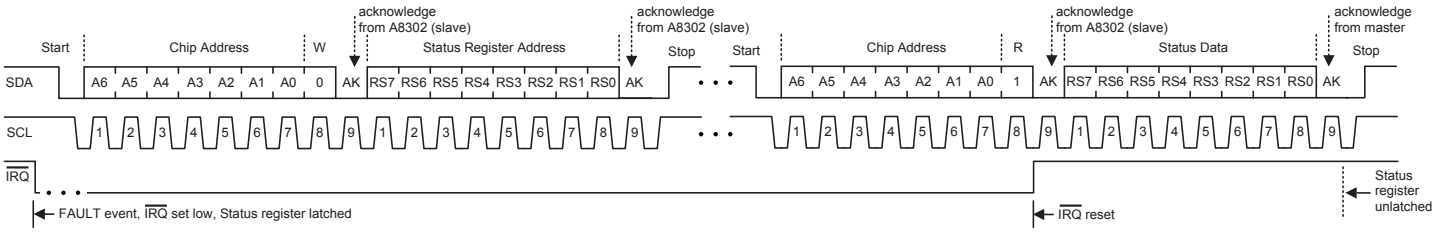

Figure 12. I²C™ Interface Read from Status register sequence. The $\overline{IRQ}$ pin is reset to high when the A8302 acknowledges it is being read. The Status register is unlatched when the master acknowledges the status data from the A8302.

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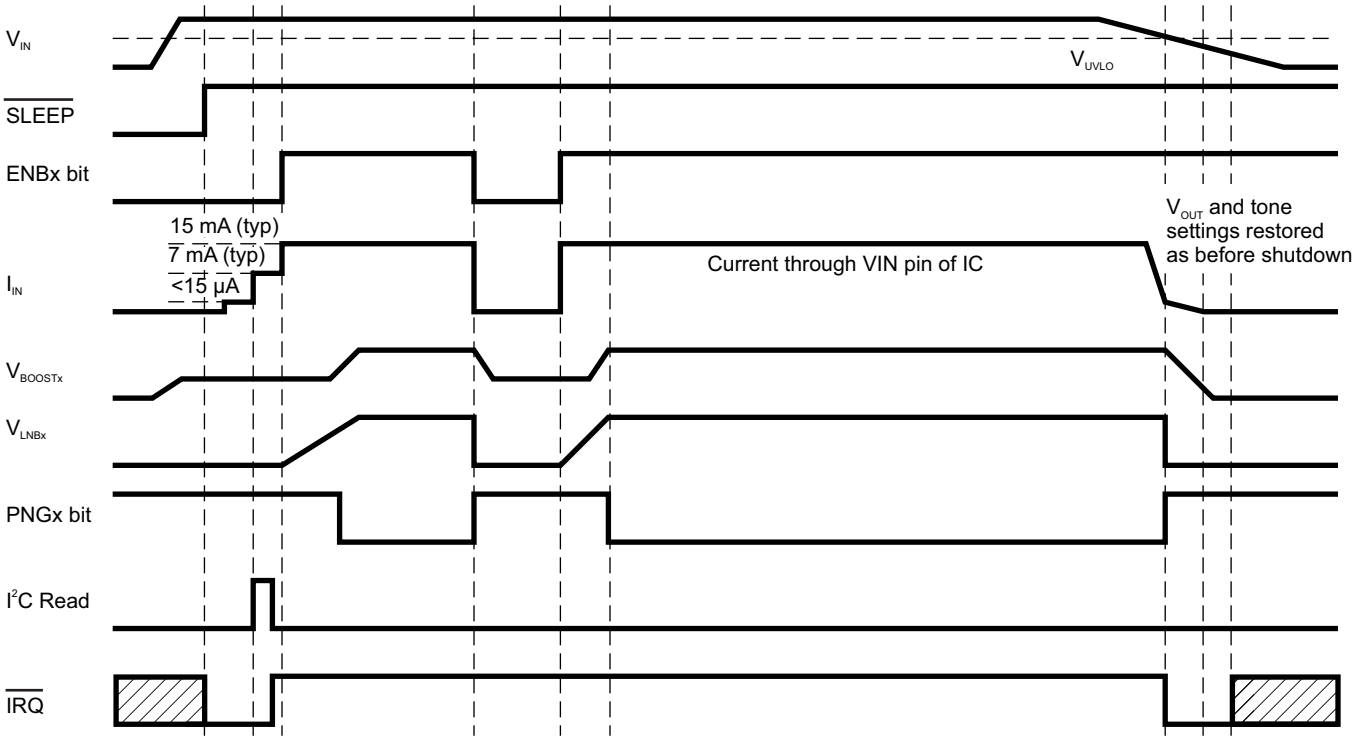

Figure 13. Startup and Shutdown Cases. $\overline{IRQ}$ and Fault Clearing in Response to Undervoltage at VIN (UVLO). If $\overline{IRQ}$ transitions low because of a latched fault, the LNBx output does not respond to the ENBx bit. An I²C™ Read sequence is required to clear any latched fault and reset the $\overline{IRQ}$ to logic high. An I²C™ Read is required after a UVLO fault.

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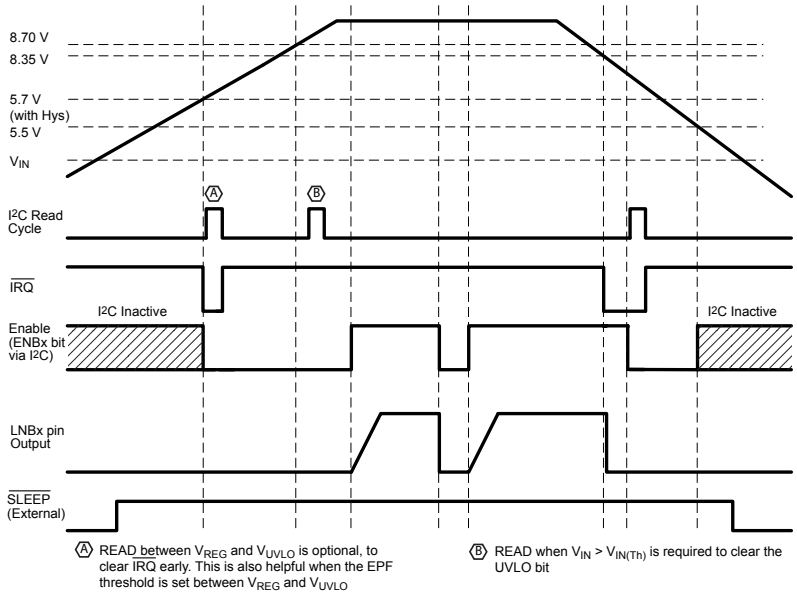

Figure 14a. I²C and $\overline{\text{IRQ}}$ operate down to $V_{IN} > V_{REG}$ (V_{REG} is 5.25 V typical), LNBx and BOOSTx operate from $V_{IN(th)}$. When V_{IN} exceeds V_{REG} (5.25 V typical), $\overline{\text{IRQ}}$ transitions low because of the UVLO fault, and an I²C Read sequence will clear the $\overline{\text{IRQ}}$ fault. While powering down, when V_{IN} falls below V_{UVLO}, $\overline{\text{IRQ}}$ becomes low, LNBx and BOOSTx turn off, and I²C becomes inactive when V_{IN} falls below V_{REG}.

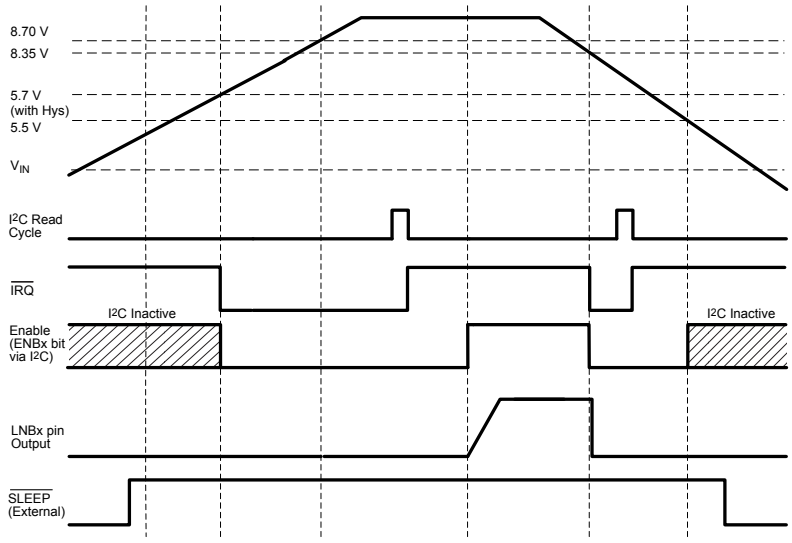

Figure 14b. $\overline{\text{IRQ}}$ is cleared when V_{IN} is already above $V_{IN(th)}$. As the ENBx bit is already set high, LNBx starts rising immediately after an I²C Read sequence.

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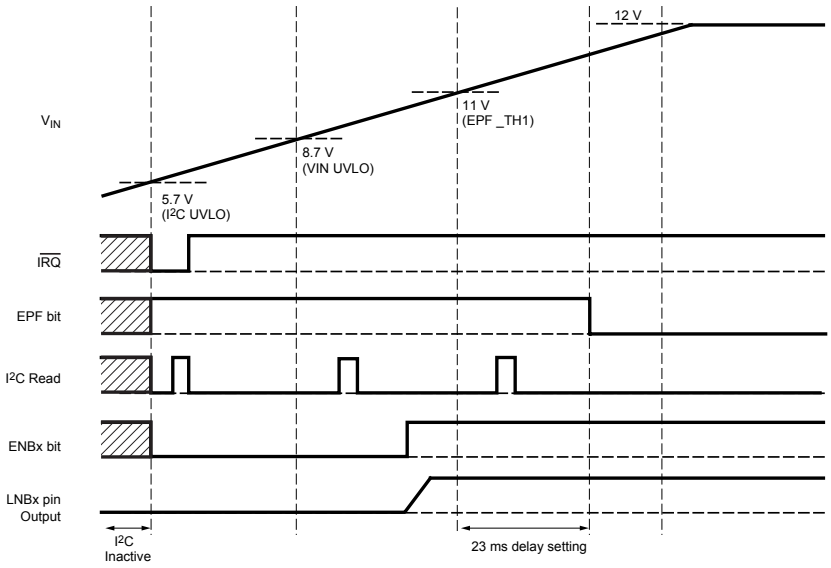

Figure 15a. EPF pin threshold greater than V_{UVLO}. When V_{IN} is rising. $\overline{IRQ}$ transitions low immediately after V_{IN} goes above V_{REG} (typical), and $\overline{IRQ}$ is cleared immediately by an I²C Read sequence. After V_{IN} goes above $V_{IN(th)}$ and is followed by an I²C Read sequence, the UVLO bit is cleared and the LNB voltage goes up. After V_{IN} goes above EPF_TH1, the EPF bit is cleared, after the delay specified by the EPF0 and EPF1 bits.

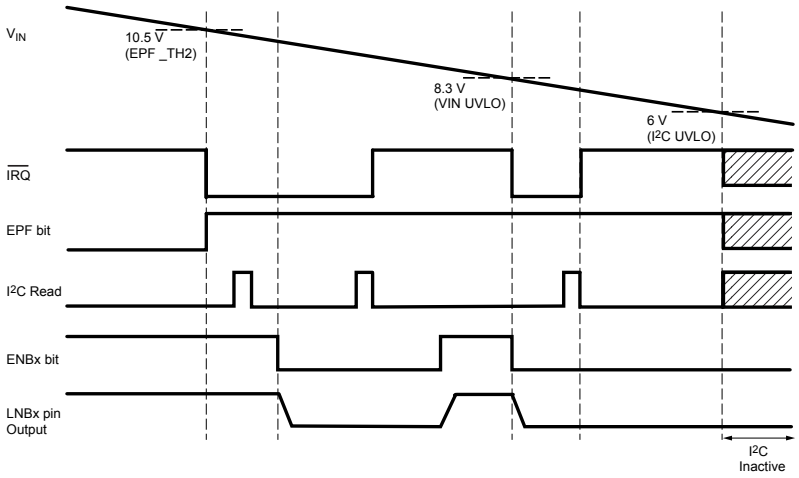

Figure 15b. EPF pin threshold greater than V_{UVLO}. When V_{IN} falls below EPF_TH2. $\overline{IRQ}$ transitions low and the EPF bit is set high. The I²C Read sequence releases $\overline{IRQ}$. When V_{IN} falls below V_{UVLO}, $\overline{IRQ}$ transitions low, LNBx voltage goes down, and once again the I²C Read sequence clears $\overline{IRQ}$.

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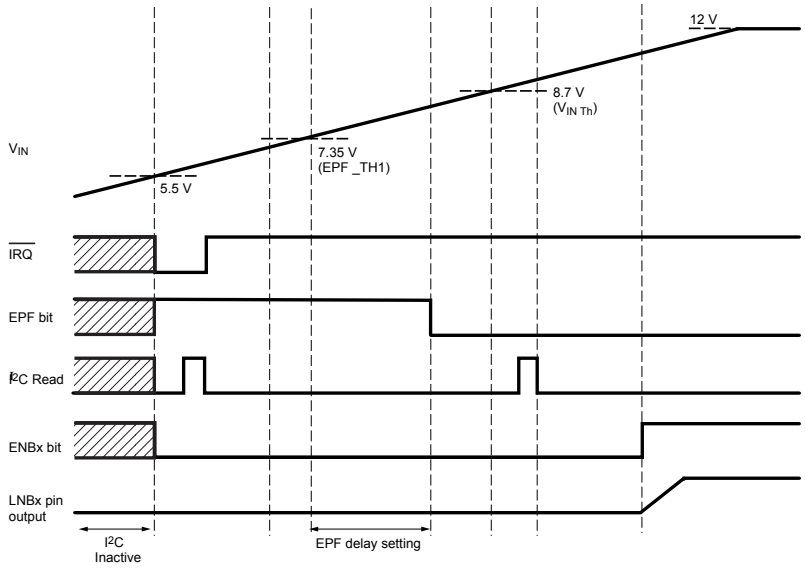

Figure 16a. EPF pin threshold greater than V_{REG} and less than V_{UVLO}. When V_{IN} is rising, $\overline{IRQ}$ transitions low immediately after V_{IN} goes above V_{REG}, and $\overline{IRQ}$ is cleared immediately by an I²C Read sequence. After V_{IN} goes above EPF_TH1, the EPF bit is cleared after the delay specified by the EPF0 and EPF1 bits. When V_{IN} goes above $V_{IN(th)}$ and is followed by an I²C Read sequence, the UVLO bit is cleared and LNBx voltage goes up.

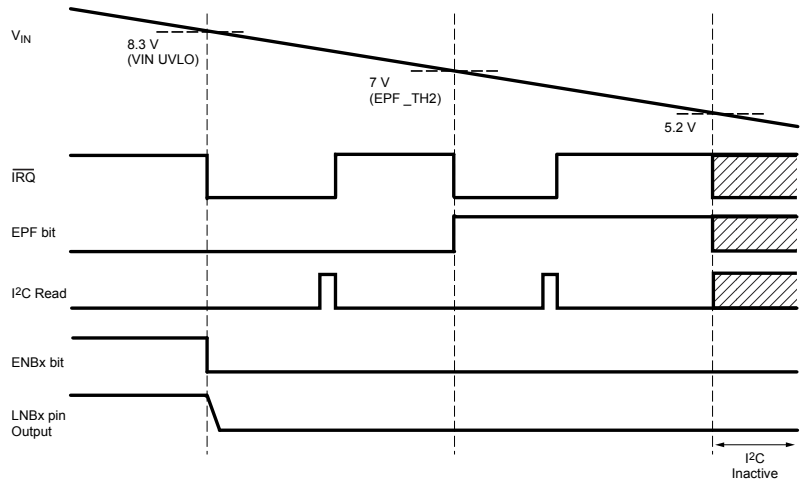

Figure 16b. EPF pin threshold greater than V_{REG} and less than V_{UVLO}. When V_{IN} falls below V_{UVLO}, $\overline{IRQ}$ transitions low and an I²C Read sequence releases $\overline{IRQ}$. When V_{IN} falls below EPF_TH , $\overline{IRQ}$ will not go low.

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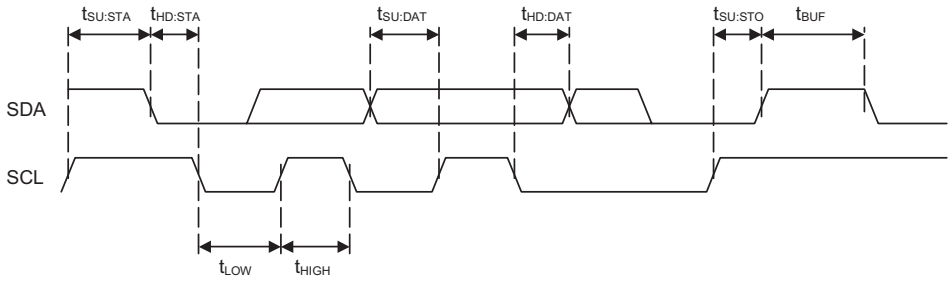
I²C™-Compatible Interface Timing Diagram



I²C™-Compatible Timing Requirements

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Bus Free Time Between Stop/Start	t_{BUF}	1.3	–	–	µs
Hold Time Start Condition	$t_{HD:STA}$	0.6	–	–	µs
Setup Time for Start Condition	$t_{SU:STA}$	0.6	–	–	µs
SCL Low Time	t_{LOW}	1.3	–	–	µs
SCL High Time	t_{HIGH}	0.6	–	–	µs
Data Setup Time	$t_{SU:DAT}$	100	–	–	ns
Data Hold Time*	$t_{HD:DAT}$	0	–	900	ns
Setup Time for Stop Condition	$t_{SU:STO}$	0.6	–	–	µs
Output Fall Time ($V_{fI2COut(H)}$ to $V_{fI2COut(L)}$)	$t_{fI2COut}$	–	–	250	ns

*For $t_{HD:DAT}$(min), the master device must provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the SCL signal falling edge. Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.

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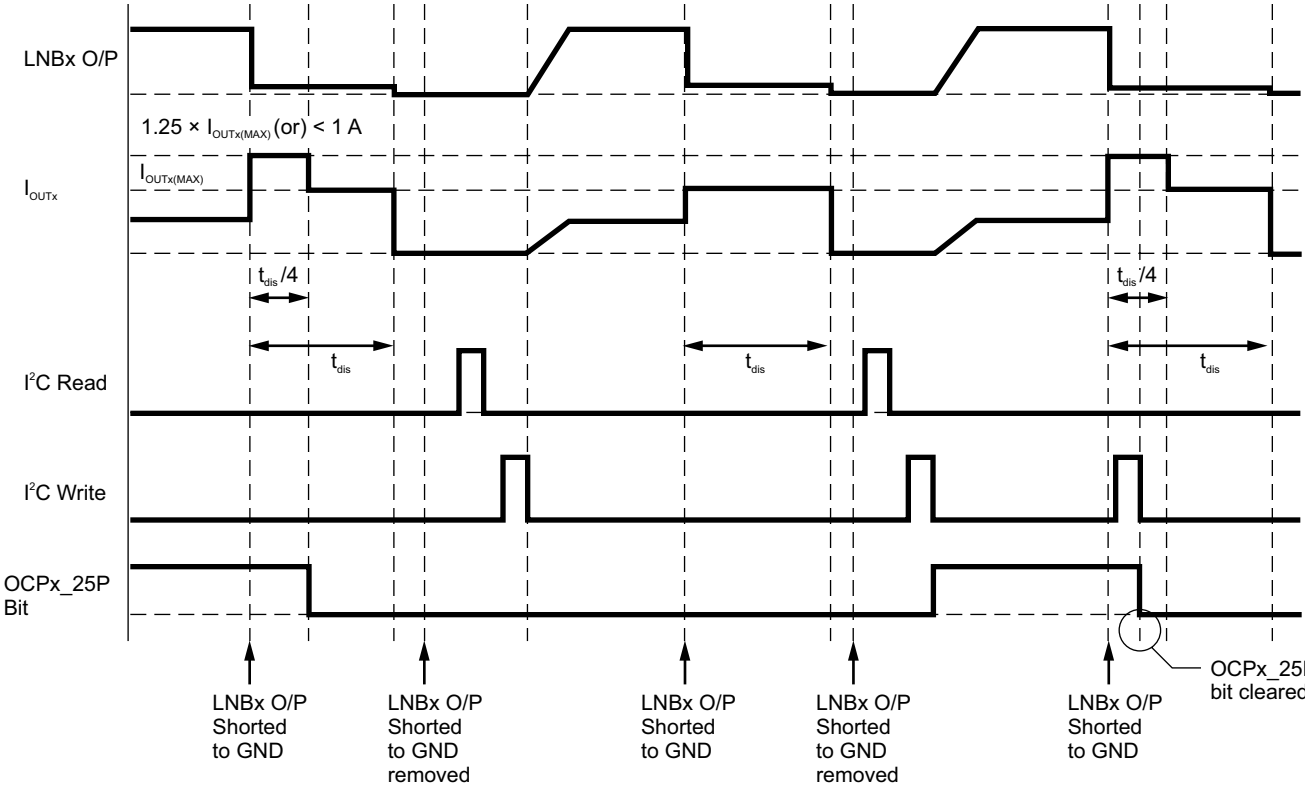

Figure 17a. Initial 25% current limit bump up with OCPx_25P bit enabled, disabled, and changed during current limit condition with OCP period > t_{dis} .

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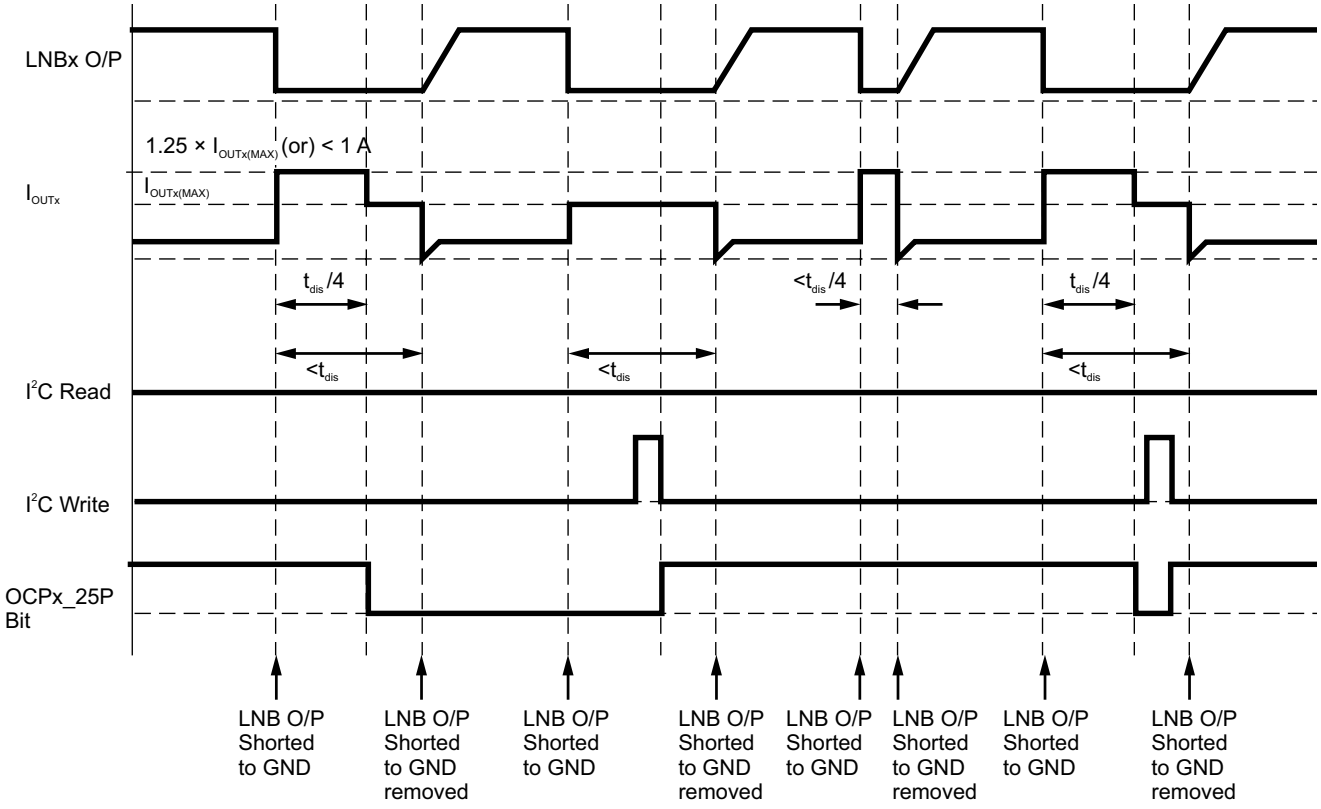

Figure 17b. Initial 25% current limit bump up with OCPx_25P bit enabled, disabled, and changed during current limit condition with OCP period < t_{dis} .

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Control Registers (I²C™-Compatible Write Register)

All main functions of the A8302 are controlled through the I²C™ compatible interface via the 8-bit Control registers. Tables 2a, 2b, and 2c show the functionality and bit definitions of the Control registers. At power-up, the Control registers are initialized to all 0s.

Table 2a. Control Register 0 Definition
Control (Write) Register Address [RC7:RC0] = 0000 0000

Bit	Name	Function	Description
0	TMODE	Controls tone mode	0: Internal tone, gated with TONECTRLx pin 1: External 22 kHz logic pulse, on TONECTRLx pin
1	TDIS_T	Controls overcurrent disable delay*	0: Set overcurrent disable timeout to 28 ms 1: Set overcurrent disable timeout to 45 ms
2	EPF0	When V_{IN} is rising, these two bits determine the EPF bit setting delay. (See table 3b for EPF bit delay setting options.)	
3	EPF1		
4	FSW	Switching frequency setting*	0: 563 kHz 1: 939 kHz
5	COMP	Switching between compensation networks*	0: Ceramic 1: Electrolytic
6	RSMODE	Fault restart mode	0: Latch mode. IC latches after tDIS period on OCP or TSD; user enable required to restart 1: Auto restart mode if OCP or TSD cleared
7	SINK_NL	Turn on/off internal adjustable sink on BOOSTx	0: Disable sink on BOOSTx 1: Enable sink on BOOSTx

*Ensure the selected bit setting matches the hardware design.

Table 2b. Control Register 1 Definition
Control (Write) Register Address [RC7:RC0] = 0000 0001

Bit	Name	Function	Description
0	VSEL01	LNB1 output voltage control (see table 3a for available output voltage selections)	The available voltages provide levels for all the common standards plus the ability to add line compensation; VSEL01 is the LSB and VSEL31 is the MSB to the internal DAC
1	VSEL11		
2	VSEL21		
3	VSEL31		
4	ENB1	Turns the LNB1 output on or off	0: Disable LNB1 output 1: Enable LNB1 output
5	OCP1_25P	25% bump up over current limit for channel 1, for $t_{dis}/4$ period; bit resets automatically after $t_{dis}/4$ period	0 : Bump up off 1 : Bump up on
6	SINK_DIS 1	SINK_DIS mode setting for channel 1	0: Maximum Output Reverse Current, I_{RLNBx} , is 70 mA 1: Maximum Output Reverse Current, I_{RLNBx} , is 10 mA
7	Tone Delay 1	In the External Tone Generation option (TMODE = 1), LNB1 voltage can be reset back to the target value with a 42 µs delay, or can be set to ≈350 mV below the target value without a delay, by using this bit.	0: (Default) LNB1 voltage will be reset back to the target after a delay of 42 µs from the last TONECONTRL1 falling edge. 1: Tone will turn off with out a delay and the LNB1 voltage will stay at ≈350 mV below the target.

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Table 2c. Control Register 2 Definition
Control (Write) Register Address [RC7:RC0] = 0000 0010

Bit	Name	Function	Description
0	VSEL02	LNB2 output voltage control (see table 3a for available output voltage selections)	The available voltages provide levels for all the common standards plus the ability to add line compensation; VSEL02 is the LSB and VSEL32 is the MSB to the internal DAC
1	VSEL12		
2	VSEL22		
3	VSEL32		
4	ENB2	Turns the LNB2 output on or off	0: Disable LNB2 output 1: Enable LNB2 output
5	OCP2_25P	25% bump up over current limit for channel 2, for $t_{dis}/4$ period; bit resets automatically after $t_{dis}/4$ period	0 : Bump up off 1 : Bump up on
6	SINK_DIS 2	SINK_DIS mode setting for channel 2	0: Maximum Output Reverse Current, I_{RLNBx} , is 70 mA 1: Maximum Output Reverse Current, I_{RLNBx} , is 10 mA
7	Tone Delay 2	In the External Tone Generation option (TMODE = 1), LNB2 voltage can be reset back to the target value with a 42 µs delay, or can be set to ≈350 mV below the target value without a delay, by using this bit.	0: (Default) LNB2 voltage will be reset back to the target after a delay of 42 µs from the last TONECONTRL2 falling edge. 1: Tone will turn off without a delay and the LNB2 voltage will stay at ≈350 mV below the target.

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Table 3a. Output Voltage Amplitude Selection

VSEL3	VSEL2	VSEL1	VSEL0	LNB (V)
0	0	1	0	13.333
0	0	1	1	13.667
0	1	0	1	14.333
0	1	1	1	15.667
1	0	1	1	18.667
1	1	0	0	19.000
1	1	0	1	19.333
1	1	1	0	19.667

Table 3b. EPF Delay Selection

EPF1	EPF0	Delay (ms)
0	0	0
0	1	11.5
1	0	46
1	1	92

Status Registers (I²C™-Compatible Read Register)

The Status registers bits are described in tables 5a and 5b. The main fault conditions: Early Power Failure (EPF), undervoltage (UVLO), overcurrent (OCP), and thermal shutdown (TSD) are all indicated by setting the relevant bits in the Status register. For these fault cases (for OCP and TSD, only if the RSMODE bit is set to 0), after the bit is set, it remains latched until the I²C™ master has successfully read the A8302, assuming the fault has been resolved.

The undervoltage lockout (UVLO) bit indicates either V_{IN} is below V_{UVLO}, or V_{REG} is out of regulation. UVLO disables the LNBx output and forces $\overline{IRQ}$ low. UVLO is a latched fault and can only be cleared by performing an I²C™ Read sequence.

The Disable bit (DISx) indicates the status of the LNBx output. The DISx bit is set when either a fault occurs (UVLO, OCP, TSD, or CPOK) or when the LNBx output is turned off using the Enable bit (ENBx) via the I²C™ interface. The DISx bit is latched and is only reset when there are no faults and the A8302 output is turned back on using the Enable (ENBx) bit via the I²C™ interface.

The Power Not Good (PNGx), Charge Pump OK (CPOKx), and Tone Detect (TDETx) bits are set based on the conditions sensed at the LNBx output, VCPx, and Tone Detect Input (TDIx) pins, respectively. These bits are not latched and, unlike the other fault bits, may become reset without an I²C™ read sequence. The PNGx, CPOKx, and TDETx bits are continuously updated.

The BOOSTxH bit is set when the BOOSTx voltage exceeds 23.7 V. This bit can be used to detect cable disconnect, provided at the lowest supply voltage BOOSTx voltage should exceed 23.7 V.

There are three methods to detect when the Status register changes: responding to the interrupt request ($\overline{IRQ}$) pin going low, continuously polling the Status register via the I²C™ interface, or detecting a fault condition external to the A8302 and performing a diagnostic poll of the A8302. In any case, the master should read and re-read the Status register until the status changes.

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Table 4. Status Registers Bit Descriptions

Name	Description
DISx	The DISx bit is set to 1 when the A8302 is disabled, (ENBx bit = 0) or there is a fault: UVLO, OCPx, CPOKx, or TSD.
CPOKx	If the CPOKx bit is set to 0, the internal charge pump is not operating correctly (VCPx). If the charge pump voltage is too low, the LNBx output is disabled and the DISx bit is set to 1.
OCPx	The OCPx bit will be set to 1 if the LNBx output current exceeds the overcurrent threshold ($I_{OUT(MAX)}$) for more than the overcurrent disable time (t_{DIS}). If the OCPx bit is set to 1, then the DISx bit is also set to 1.
TRIMS	Factory use only.
PNGx	The PNGx bit is set to 1 when the A8302 is enabled and the LNBx output voltage is either too low or too high (nominally ±9% from the LNBx DAC setting). Set to 0 when the A8302 is enabled and the LNBx voltage is within the acceptable range (nominally ±5% from the LNBx DAC setting).
TDETx	The TDETx bit is set to 1 if a tone is detected at the TDIx pin that is within the specified voltage and frequency ranges. If TCTRLx = 1, the tone is being transmitted by the A8302, and the tone detect low threshold is determined by $V_{TD(XMT)L}$. If If TCTRLx = 0, it is assumed the tone is being received from an external source, and the tone detect low threshold is determined by $V_{TD(RCV)L}$.
TSD	The TSD bit is set to 1 if the A8302 has detected an overtemperature condition. If the TSD bit is set to 1, then the DISx bit is also set to 1.
UVLO	The UVLO bit is set to 1 if either the voltage at the VIN pin or the voltage at the VREG pin is too low. If the UVLO bit is set to 1, then the DISx bit is also set to 1.
BOOSTxH	The BOOSTxH bit is set to 1 when the voltage on BOOSTx exceeds 23.7 V. This bit automatically resets when BOOSTx voltage goes below 23.6 V. This bit has no effect on $\overline{IRQ}$.
EPF	The EPF bit is set to 1 when the voltage on the EPF pin falls below V_{EPF_TH}. Also, IRQ\ is pulled low. When the EPF pin voltage goes above $V_{EPF\_TH} + V_{EPF\_TH\_Hys}$, the EPF bit is reset to 0 after the delay selected by the EPF0 and EPF1 bits in the Control registers.

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Table 5a. Status Register 0 Definition and IRQ Operation

Status (Read) Register Address [RS7:RS0] = 0000 0000

Bit	Name	Function	Latched?	Reset Condition	Effect on $\overline{IRQ}$ Pin
0	DIS1	LNB1 output disabled	Yes	LNB1 enabled and no faults	None
1	DIS2	LNB2 output disabled	Yes	LNB2 enabled and no faults	None
2	OCP1	LNB1 overcurrent	Auto-retry (RSMODE = 1)	OCP reset after every 1 s; IC enabled if fault is removed	$\overline{IRQ}$ set low; I²C Read sequence resets to high
			Latch (RSMODE = 0)	I²C Read sequence required after removing the fault	
3	OCP2	LNB2 overcurrent	Auto-retry (RSMODE = 1)	OCP reset after every 1 s; IC enabled if fault is removed	$\overline{IRQ}$ set low; I²C Read sequence resets to high
			Latch (RSMODE = 0)	I²C Read sequence required after removing the fault	
4	PNG1	LNB1 Power Not Good	No	LNB1 voltage within range	None
5	PNG2	LNB2 Power Not Good	No	LNB2 voltage within range	None
6	UVLO	V_{IN} or V_{REG} undervoltage	Yes	I²C Read sequence and V_{IN} > 9.0 V	$\overline{IRQ}$ set low; I²C Read sequence resets to high
7	TSD	Thermal shutdown	Auto-retry (RSMODE = 1)	TSD reset after every 1 s; reset happens only if fault is removed	$\overline{IRQ}$ set low; I²C Read sequence resets to high
			Latch (RSMODE = 0)	I²C Read sequence required after removing the fault	

Table 5b. Status Register 1 Definition and IRQ Operation

Status (Read) Register Address [RS7:RS0] = 0000 0001

Bit	Name	Function	Latched?	Reset Condition	Effect on $\overline{IRQ}$ Pin
0	CPOK1	LNB1 charge pump OK	No	$V_{CP1} > V_{BOOST1} + 5$ V	None
1	CPOK2	LNB2 charge pump OK	No	$V_{CP2} > V_{BOOST2} + 5$ V	None
2	TDET1	LNB1 tone detect	No	Tone removed from LNB1 pin	None
3	TDET2	LNB2 tone detect	No	Tone removed from LNB2 pin	None
4	EPF	Early Power Failure warning (V_{IN} < EPF threshold)	No	V_{IN} > EPF_TH1	$\overline{IRQ}$ set low; I²C Read sequence resets to high
5	TRIMS	Trim bits locked	Yes	None	None
6	BOOST1H	Boost1 Voltage Monitor	No	V_{BOOST1} < 23.6 V	None
7	BOOST2H	Boost2 Voltage Monitor	No	V_{BOOST2} < 23.6 V	None

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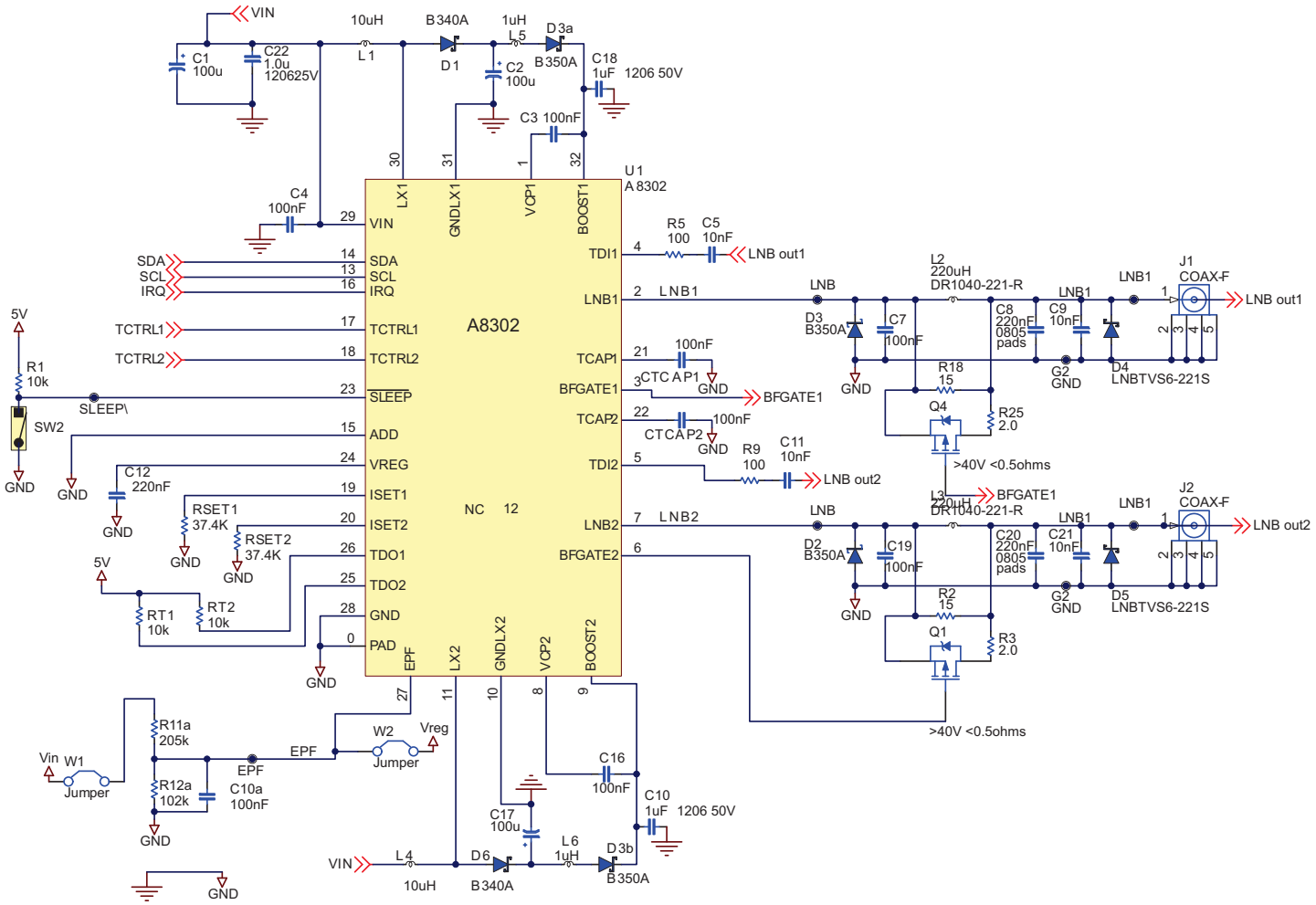
Application Information



PGND and GND form a single point ground at U 1

See table 6 for bill of materials

Schematic 1. A8302 application circuit using electrolytic capacitors on BOOST and 563 kHz switching frequency. I_{OUT}(max) = 800 mA.

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Table 6. Component Selection Table for Schematic 1

Reference Designators	Description	Footprint	Qty.	Manufacturer	Manufacturer P/N	Purchase P/N
C1,C2,C17	Electrolytic Capacitor, 100 µF, 35 V, 8x10.2 mm, ESR=80 mΩ, I_{ripple} = 850 mA	SMT 8 mm x 10.2 mm	3	Panasonic	EEE-FP1V101AP	PCE4442CT-ND
C3,C4,C7,C16,C19,C10a,CTCAP1,CTCAP2,	Capacitor, Ceramic, 100 nF, 25 V, 10%, X7R	0603	8	Murata Panasonic	GRM188R71H104KA93D ECJ-1VB1E104K	490-1519-1-ND PCC2277CT-ND
C5,C9,C11,C21	Capacitor, Ceramic, 10 nF, 50 V, 10%, X7R	0603	4	Murata	GRM188R71H103KA01D	490-1512-1-ND
C8,C12,C20	Capacitor, Ceramic, 220 nF, 25 V, 10%, X7R	0603	3	Taiyo Yuden	TMK107B7224KA-T	587-1246-1-ND
C22	Capacitor, Ceramic, 1 µF, 25 V, 10%, X5R	0603	1	Taiyo Yuden	TMK107BJ105KA-T	587-1248-1-ND
C10,C18	Capacitor, Ceramic, 1 µF, 50 V, 10%, X7R	1206	2	Murata	GRM31CR71H105KA61L	490-3908-1-ND
D1,D6	Schottky diode, 40 V, 3 A, 0.7 V_f at 10 A	SMA	1	Diodes, Inc. Diodes, Inc. Central Semi	B340A-13-F B340A-13-F CMSH3-40MA	B340A-FDICT-ND 621-B340A-F Request samples
D2,D3,D3a,D3b	Schottky diode, 50 V, 3 A	SMA	6	Diodes, Inc. Diodes, Inc.	B350A-13-F B350A-13-F	B350A-FDICT-ND 621-B350A-F
D4,D5	TVS, 20 Vrms at 1 µA, 3000 W, SMC	SMC	2	Littelfuse ST ST	SMDJ20A LNBTVS6-221S LNBTVS6-221S	Request Samples 497-4998-1-ND 511-LNBTVS6-221S
J1,J2	Connector, F-type, right angle, PCB mount	Thru-Hole	2	Amphenol	531-40047-3	523-531-40047-3
L1,L4	Inductor, 10 µH, ±30%, 3.8 Arms 4.4 A_{sat}, 26 mΩ	10.3 mm x 10.5 mm x 4 mm	2	Cooper Bussman	DR1040-100-R	513-1399-1-ND
L2,L3	Inductor, 220 µH, ±30%, 0.92 A_{sat}, 530 mΩ	10.3 mm x 10.5 mm x 4 mm	2	Cooper Bussman	DR1040-221-R	513-1408-1-ND 704-DR1040-221-R
L5,L6	Inductor, 1 µH, ±20%, 1.0 A (min), <100 mΩ Note: Not Required with Ceramic Capacitor option	1206	2	Kemet Murata TDK	LB3218-T1R0MK LQM31PN1R0M00L MLP3216S1R0L	80-LB3218-T1R0MK 490-4039-1-ND Request Samples
Q1,Q4	PMOS, ENH, 60 V, 1.5 A, 0.45 Ω at 4.5 V	SOT23	2	Vishay Diodes, Inc	SI2309DS-T1-E3 ZXMP6A13FTA	SI2309DS-T1-E3CT-ND ZXMP6A13FCT-ND
R1,RT1,RT2	Resistor, 10 kΩ, 1/10 W, 1%, 0603	0603	3			
R2,R18	Resistor, 15 Ω, 1/10 W, 1%, 0603	0603 part 1206 pads	2			
R3,R25	Resistor, 2 Ω, 1/10 W, 1% or 5%, 0603	0603	2			
R5,R9	Resistor, 100 Ω, 1/10 W, 1%, 0603	0603	2			
R11a	Resistor, 205 kΩ, 1/10 W, 1%, 0603	0603	1			
R12a	Resistor, 102 kΩ, 1/10 W, 1%, 0603	0603	1			
RSET1,RSET2	Resistor, 37.4 kΩ, 1/10 W, 1%, 0603	0603	2			
SW2	DIP Switch, 1 pos	SMT	1	C & K Components	SDA01H0SBR	CKN9490CT-ND
U1	A8302, Dual LNB Supply and Control IC	MLP-32 5 mm x 5 mm	1	Allegro MicroSystems		
W1,W2	Header, 2-position, 0.1 spacing	Thru-Hole	2	Sullins Harwin	PEC36SAAN M20-9773646	S1012E-36-ND 855-M20-9773646

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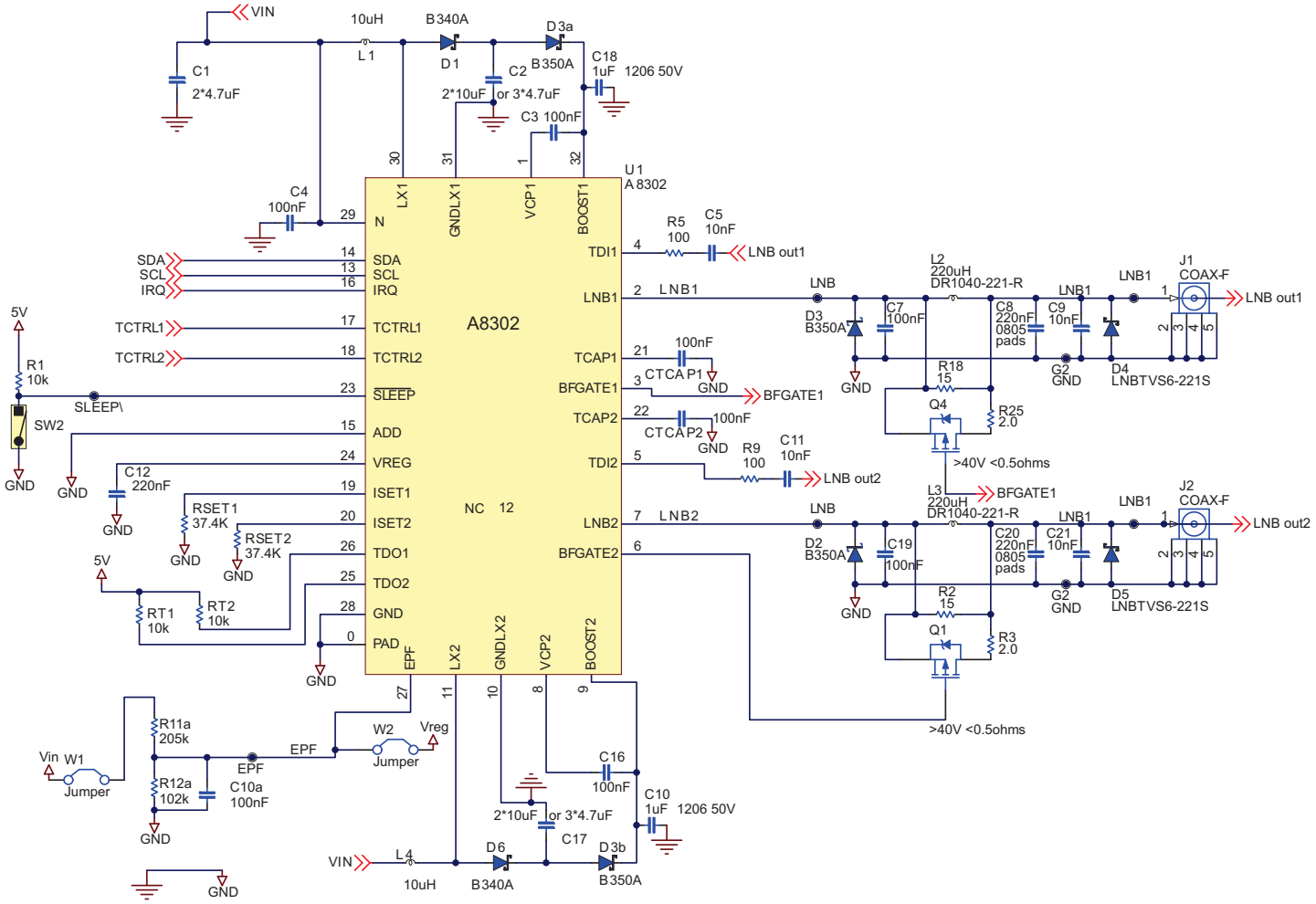

See table 7 for bill of materials

Schematic 2. A8302 application circuit using ceramic capacitors on BOOST and 563 kHz switching frequency. I_{OUT}(max) = 800 mA.

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Table 7. Component Selection Table for Schematic 2

Reference Designators	Description	Footprint	Qty.	Manufacturer	Manufacturer P/N	Purchase P/N
C1	Capacitor, Ceramic, 4.7 µF, 25 V, 10%, X7R	1206	2	Murata TDK AVX	GRM31CR71E475KA88L C3216X7R1E475K 12063C475KAT2A	490-1809-1-ND 445-1606-1-ND 478-5996-1-ND
C2,C17	Capacitor, Ceramic, 10 µF, 35 V, 10%, X7R	1210	4	Murata	GRM32ER7YA106KA12L	490-5314-1-ND
C3,C4,C7,C16,C19,C10a,CTCAP1,CTCAP2,	Capacitor, Ceramic, 100 nF, 25 V, 10%, X7R	0603	8	Murata Panasonic	GRM188R71H104KA93D ECJ-1VB1E104K	490-1519-1-ND PCC2277CT-ND
C5,C9,C11,C21	Capacitor, Ceramic, 10 nF, 50 V, 10%, X7R	0603	4	Murata	GRM188R71H103KA01D	490-1512-1-ND
C8,C12,C20	Capacitor, Ceramic, 220 nF, 25 V, 10%, X7R	0603	3	Taiyo Yuden	TMK107B7224KA-T	587-1246-1-ND
C22	Capacitor, Ceramic, 1 µF, 25 V, 10%, X5R	0603	1	Taiyo Yuden	TMK107BJ105KA-T	587-1248-1-ND
C10,C18	Capacitor, Ceramic, 1 µF, 50 V, 10%, X7R	1206	2	Murata	GRM31CR71H105KA61L	490-3908-1-ND
D1,D6	Schottky diode, 40 V, 3 A, 0.7 V_f at 10 A	SMA	1	Diodes, Inc. Diodes, Inc. Central Semi	B340A-13-F B340A-13-F CMSH3-40MA	B340A-FDICT-ND 621-B340A-F Request samples
D2,D3,D3a,D3b	Schottky diode, 50 V, 3 A	SMA	6	Diodes, Inc. Diodes, Inc.	B350A-13-F B350A-13-F	B350A-FDICT-ND 621-B350A-F
D4,D5	TVS, 20 Vrms at 1 µA, 3000 W, SMC	SMC	2	Littelfuse ST ST	SMDJ20A LNBTVS6-221S LNBTVS6-221S	Request Samples 497-4998-1-ND 511-LNBTVS6-221S
J1,J2	Connector, F-type, right angle, PCB mount	Thru-Hole	2	Amphenol	531-40047-3	523-531-40047-3
L1,L4	Inductor, 10 µH, ±30%, 3.8 Arms, 4.4 A_{sat}, 26 mΩ	10.3 mm x 10.5 mm x 4 mm	2	Cooper Bussman	DR1040-100-R	513-1399-1-ND
L2,L3	Inductor, 220 µH, ±30%, 0.92 A_{sat}, 530 mΩ	10.3 mm x 10.5 mm x 4 mm	2	Cooper Bussman	DR1040-221-R	513-1408-1-ND 704-DR1040-221-R
Q1,Q4	PMOS, ENH, 60 V, 1.5 A, 0.45 Ω at 4.5 V	SOT23	2	Vishay Diodes, Inc	SI2309DS-T1-E3 ZXMP6A13FTA	SI2309DS-T1-E3CT-ND ZXMP6A13FCT-ND
R1,RT1,RT2	Resistor, 10 kΩ, 1/10 W, 1%, 0603	0603	3			
R2,R18	Resistor, 15 Ω, 1/10 W, 1%, 0603	0603 part 1206 pads	2			
R3,R25	Resistor, 2 Ω, 1/10 W, 1% or 5%, 0603	0603	2			
R5,R9	Resistor, 100 Ω, 1/10 W, 1%, 0603	0603	2			
R11a	Resistor, 205 kΩ, 1/10 W, 1%, 0603	0603	2			
R12a	Resistor, 102 kΩ, 1/10 W, 1%, 0603	0603	1			
RSET1,RSET2	Resistor, 37.4 kΩ, 1/10 W, 1%, 0603	0603	2			
SW2	DIP Switch, 1 pos	SMT	1	C & K Components	SDA01H0SBR	CKN9490CT-ND
U1	A8302, Dual LNB Supply and Control IC	MLP-32 5 mm x 5 mm	1	Allegro MicroSystems		
W1,W2	Header, 2-position, 0.1 spacing	Thru-Hole	2	Sullins Harwin	PEC36SAAN M20-9773646	S1012E-36-ND 855-M20-9773646

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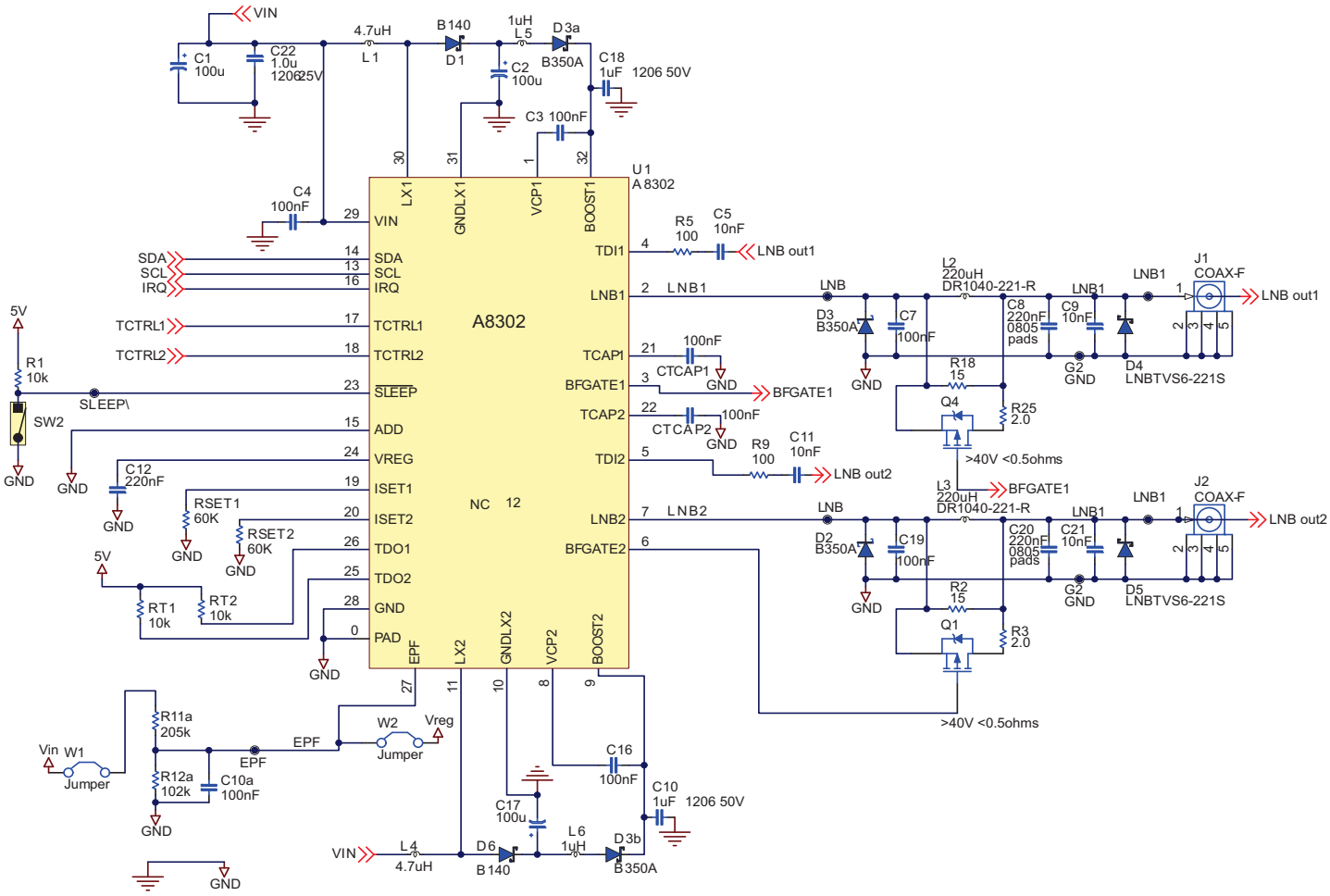

PGND and GND form a single point ground at U 1

See table 8 for bill of materials

Schematic 3. A8302 application circuit using electrolytic capacitors on BOOST and 939 kHz switching frequency. I_{out}(max) = 500 mA.

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Table 8. Component Selection Table for Schematic 3

Reference Designators	Description	Footprint	Qty.	Manufacturer	Manufacturer P/N	Purchase P/N
C1,C2,C17	Electrolytic Capacitor, 100 µF, 25 V, 6x11.2 mm, ESR ≤ 130 mΩ, I_{ripple} ≥ 450 mA, Thru-hole	6 mm diameter, 2.5 or 3.5 mm lead spacing	3	Panasonic	EEU-FM1E101	P12924-ND
C3,C4,C7,C16,C19,C10a,CTCAP1,CTCAP2,	Capacitor, Ceramic, 100 nF, 25 V, 10%, X7R	0603	8	Murata Panasonic	GRM188R71H104KA93D ECJ-1VB1E104K	490-1519-1-ND PCC2277CT-ND
C5,C9,C11,C21	Capacitor, Ceramic, 10 nF, 50 V, 10%, X7R	0603	4	Murata	GRM188R71H103KA01D	490-1512-1-ND
C8,C12,C20	Capacitor, Ceramic, 220 nF, 25 V, 10%, X7R	0603	3	Taiyo Yuden	TMK107B7224KA-T	587-1246-1-ND
C22	Capacitor, Ceramic, 1 µF, 25 V, 10%, X5R	0603	1	Taiyo Yuden	TMK107BJ105KA-T	587-1248-1-ND
C10,C18	Capacitor, Ceramic, 1 µF, 50 V, 10%, X7R	1206	2	Murata	GRM31CR71H105KA61L	490-3908-1-ND
D1,D6	Schottky diode, 40 V, 1 A	SOD-123	1	Diodes, Inc Central Semi	B140HW-7 CMMSH1-40	B140HWDICT-ND Request Samples
D2,D3,D3a,D3b	Schottky diode, 50 V, 3 A	SMA	6	Diodes, Inc. Diodes, Inc.	B350A-13-F B350A-13-F	B350A-FDICT-ND 621-B350A-F
D4,D5	TVS, 20 Vrms at 1 µA, 3000 W, SMC	SMC	2	Littelfuse ST ST	SMDJ20A LNBTVS6-221S LNBTVS6-221S	Request Samples 497-4998-1-ND 511-LNBTVS6-221S
J1,J2	Connector, F-type, right angle, PCB mount	Thru-Hole	2	Amphenol	531-40047-3	523-531-40047-3
L1,L4	Inductor, 4.7 µH, ±20%, 2.9 Arms, 3.5 A_{sat}, 33 mΩ	7.60 mm x 7.60 mm x 3.55 mm	2	Cooper Bussman	DRA73-4R7-R	283-3617-1-ND
L2,L3	Inductor, 220 µH, ±30%, 0.92 A_{sat}, 530 mΩ	10.3 mm x 10.5 mm x 4 mm	2	Cooper Bussman	DR1040-221-R	513-1408-1-ND 704-DR1040-221-R
L5,L6	Inductor, 1 µH, ±20%, 1.0 A(min), <100 mΩ Note: Not Required with Ceramic Capacitor option	1206	2	Kemet Murata TDK	LB3218-T1R0MK LQM31PN1R0M00L MLP3216S1R0L	80-LB3218-T1R0MK 490-4039-1-ND Request Samples
Q1,Q4	PMOS, ENH, 60 V, 1.5 A, 0.45 Ω at 4.5 V	SOT23	2	Vishay Diodes, Inc	SI2309DS-T1-E3 ZXMP6A13FTA	SI2309DS-T1-E3CT-ND ZXMP6A13FCT-ND
R1,RT1,RT2	Resistor, 10 kΩ, 1/10 W, 1%, 0603	0603	3			
R2,R18	Resistor, 15 Ω, 1/10 W, 1%, 0603	0603 part 1206 pads	2			
R3,R25	Resistor, 2 Ω, 1/10 W, 1% or 5%, 0603	0603	2			
R5,R9	Resistor, 100 Ω, 1/10 W, 1%, 0603	0603	2			
R11a	Resistor, 205 kΩ, 1/10 W, 1%, 0603	0603	1			
R12a	Resistor, 102 kΩ, 1/10 W, 1%, 0603	0603	1			
RSET1,RSET2	Resistor, 60 kΩ, 1/10 W, 1%, 0603	0603	2			
SW2	DIP Switch, 1 pos	SMT	1	C & K Components	SDA01H0SBR	CKN9490CT-ND
U1	A8302, Dual LNB Supply & Control IC	MLP-32 5 mm x 5 mm	1	Allegro MicroSystems		
W1,W2	Header, 2-position, 0.1 spacing	Thru-Hole	2	Sullins Harwin	PEC36SAAN M20-9773646	S1012E-36-ND 855-M20-9773646

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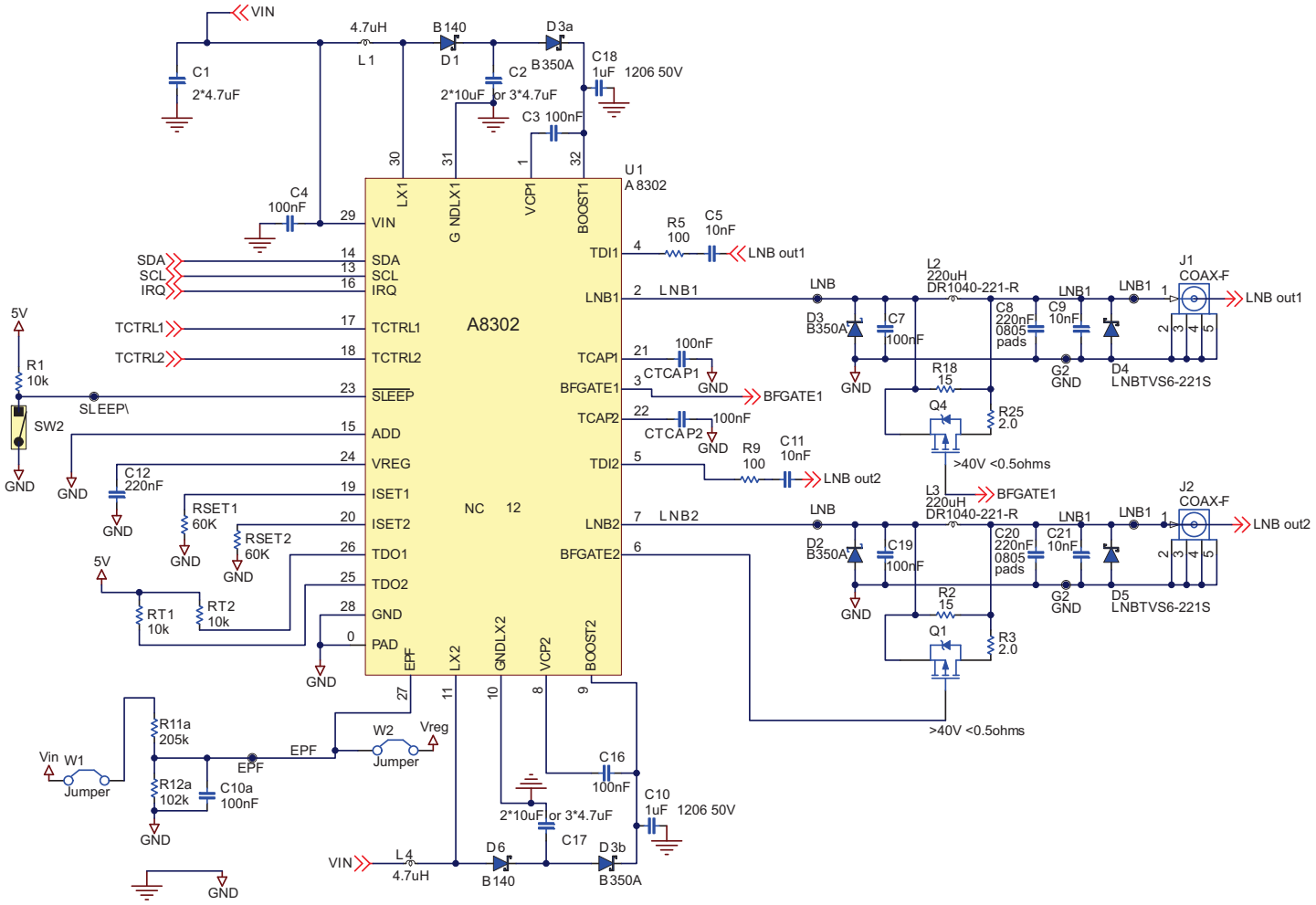

PGND and GND form a single point ground at U1

See table 9 for bill of materials

Schematic 4. A8302 application circuit using ceramic capacitors on BOOST and 939 kHz switching frequency . I_{out}(max) = 500 mA.

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Table 9. Component Selection Table for Schematic 4

Reference Designators	Description	Footprint	Qty.	Manufacturer	Manufacturer P/N	Purchase P/N
C1	Capacitor, Ceramic, 4.7 µF, 25 V, 10%, X7R	1206	2	Murata TDK AVX	GRM31CR71E475KA88L C3216X7R1E475K 12063C475KAT2A	490-1809-1-ND 445-1606-1-ND 478-5996-1-ND
C2,C17	Capacitor, Ceramic, 10 µF, 35 V, 10%, X7R	1210	4	Murata	GRM32ER7YA106KA12L	490-5314-1-ND
C3,C4,C7,C16,C19,C10a,CTCAP1,CTCAP2,	Capacitor, Ceramic, 100 nF, 25 V, 10%, X7R	0603	8	Murata Panasonic	GRM188R71H104KA93D ECJ-1VB1E104K	490-1519-1-ND PCC2277CT-ND
C5,C9,C11,C21	Capacitor, Ceramic, 10 nF, 50 V, 10%, X7R	0603	4	Murata	GRM188R71H103KA01D	490-1512-1-ND
C8,C12,C20	Capacitor, Ceramic, 220 nF, 25 V, 10%, X7R	0603	3	Taiyo Yuden	TMK107B7224KA-T	587-1246-1-ND
C22	Capacitor, Ceramic, 1 µF, 25 V, 10%, X5R	0603	1	Taiyo Yuden	TMK107BJ105KA-T	587-1248-1-ND
C10,C18	Capacitor, Ceramic, 1 µF, 50 V, 10%, X7R	1206	2	Murata	GRM31CR71H105KA61L	490-3908-1-ND
D1,D6	Schottky diode, 40 V, 1 A	SOD-123	1	Diodes, Inc Central Semi	B140HW-7 CMMSH1-40	B140HWDICT-ND Request Samples
D2,D3,D3a,D3b	Schottky diode, 50 V, 3 A	SMA	6	Diodes, Inc. Diodes, Inc.	B350A-13-F B350A-13-F	B350A-FDICT-ND 621-B350A-F
D4,D5	TVS, 20 Vrms at 1 µA, 3000 W, SMC	SMC	2	Littelfuse ST ST	SMDJ20A LNBTVS6-221S LNBTVS6-221S	Request Samples 497-4998-1-ND 511-LNBTVS6-221S
J1,J2	Connector, F-type, right angle, PCB mount	Thru-Hole	2	Amphenol	531-40047-3	523-531-40047-3
L1,L4	Inductor, 4.7 µH, ±20%, 2.9 Arms, 3.5 A_{sat}, 33 mΩ	7.60 mm x 7.60 mm x 3.55 mm	2	Cooper Bussman	DRA73-4R7-R	283-3617-1-ND
L2,L3	Inductor, 220 µH, ±30%, 0.92 A_{sat}, 530 mΩ	10.3 mm x 10.5 mm x 4 mm	2	Cooper Bussman	DR1040-221-R	513-1408-1-ND 704-DR1040-221-R
Q1,Q4	PMOS, ENH, 60 V, 1.5 A, 0.45 Ω at 4.5 V	SOT23	2	Vishay Diodes, Inc	SI2309DS-T1-E3 ZXMP6A13FTA	SI2309DS-T1-E3CT-ND ZXMP6A13FCT-ND
R1,RT1,RT2	Resistor, 10 kΩ, 1/10 W, 1%, 0603	0603	3			
R2,R18	Resistor, 15 Ω, 1/10 W, 1%, 0603	0603 part 1206 pads	2			
R3,R25	Resistor, 2 Ω, 1/10 W, 1% or 5%, 0603	0603	2			
R5,R9	Resistor, 100 Ω, 1/10 W, 1%, 0603	0603	2			
R11a	Resistor, 205 kΩ, 1/10 W, 1%, 0603	0603	2			
R12a	Resistor, 102 kΩ, 1/10 W, 1%, 0603	0603	1			
RSET1,RSET2	Resistor, 60 kΩ, 1/10 W, 1%, 0603	0603	2			
SW2	DIP Switch, 1 pos	SMT	1	C & K Components	SDA01H0SBR	CKN9490CT-ND
U1	A8302, Dual LNB Supply amd Control IC	MLP-32 5 mm x 5 mm	1	Allegro MicroSystems		
W1,W2	Header, 2-position, 0.1 spacing	Thru-Hole	2	Sullins Harwin	PEC36SAAN M20-9773646	S1012E-36-ND 855-M20-9773646

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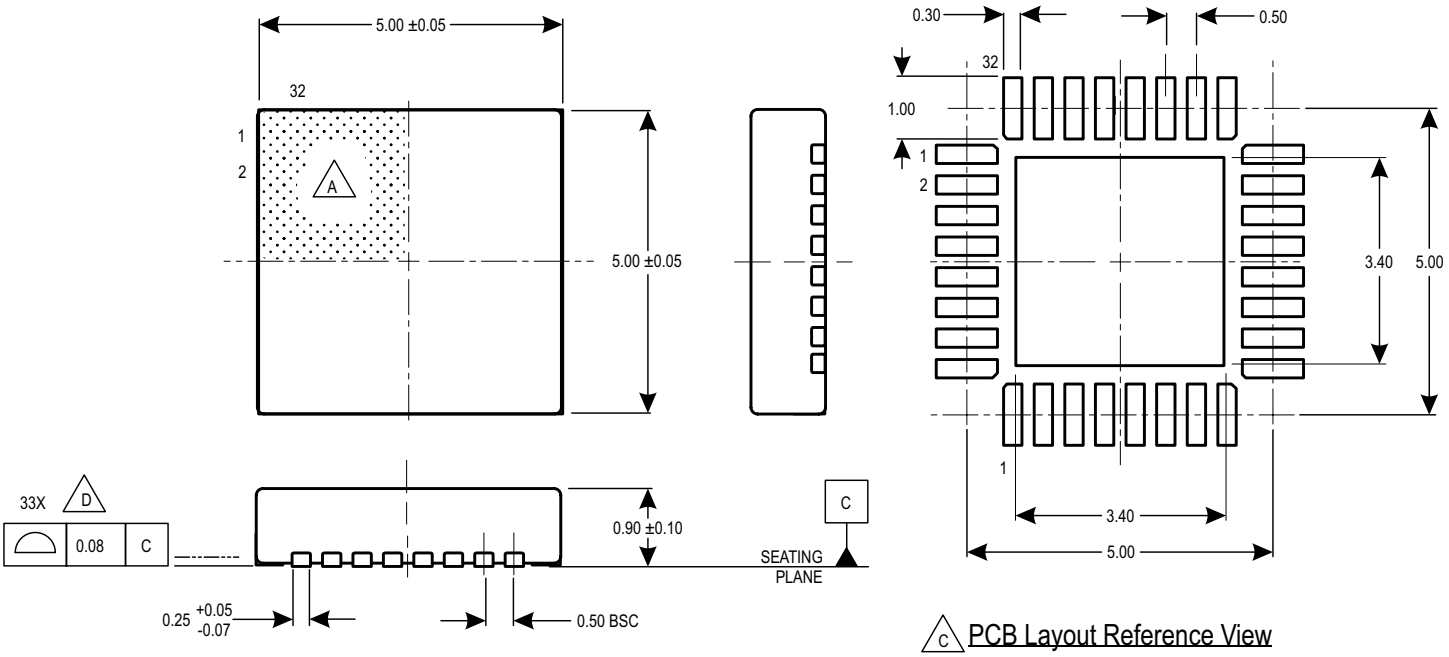
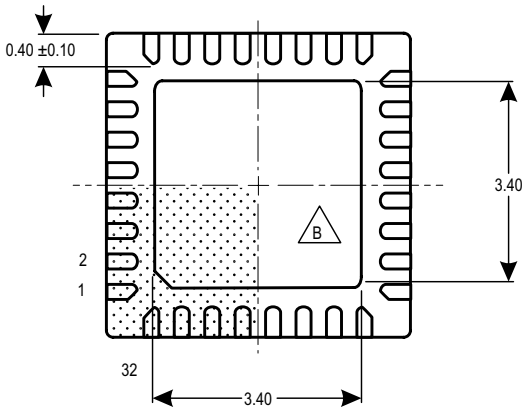
Package ET 32-Pin QFN
with Exposed Thermal Pad

For Reference Only – Not for Tooling Use

(Reference JEDEC MO-220VHHD-5)
Dimensions in millimeters – NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



C PCB Layout Reference View



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P500X500X100-33V6M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

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REVISION HISTORY

Number	Date	Description
–	June 13, 2014	Initial release
1	January 11, 2016	Corrected Terminal List Table (page 4)
2	May 15, 2020	Minor editorial updates

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