THE DATASHEET OF

AD8513AR-REEL

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Precision, Very Low Noise, Low Input Bias Current, Wide Bandwidth JFET Operational Amplifiers

Date Sheet

AD8510/AD8512/AD8513

FEATURES

- Fast settling time: 500 ns to 0.1%
- Low offset voltage: 400 µV maximum
- Low T_CV_{OS}: 1 µV/°C typical
- Low input bias current: 25 pA typical at V_S = ±15 V
- Dual-supply operation: ±5 V to ±15 V
- Low noise: 8 nV/√Hz typical at f = 1 kHz
- Low distortion: 0.0005%
- No phase reversal
- Unity-gain stable

APPLICATIONS

- Instrumentation
- Multipole filters
- Precision current measurement
- Photodiode amplifiers
- Sensors
- Audio

PIN CONFIGURATIONS

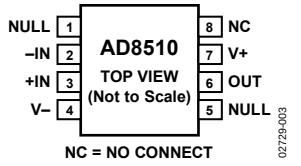

Figure 1. 8-Lead MSOP (RM Suffix)

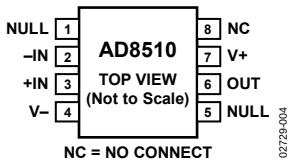

Figure 2. 8-Lead SOIC_N (R Suffix)

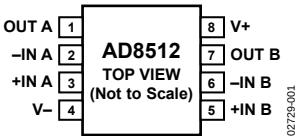

Figure 3. 8-Lead MSOP (RM Suffix)

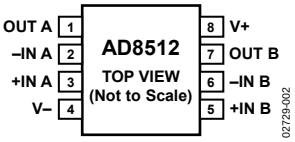

Figure 4. 8-Lead SOIC_N (R Suffix)

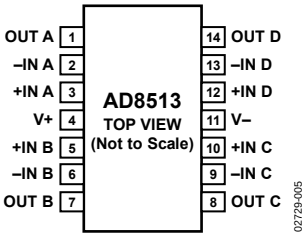

Figure 5. 14-Lead SOIC_N (R Suffix)

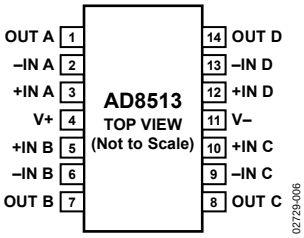

Figure 6. 14-Lead TSSOP (RU Suffix)

GENERAL DESCRIPTION

The AD8510/AD8512/AD8513 are single-, dual-, and quad-precision JFET amplifiers that feature low offset voltage, input bias current, input voltage noise, and input current noise.

The combination of low offsets, low noise, and very low input bias currents makes these amplifiers especially suitable for high impedance sensor amplification and precise current measurements using shunts. The combination of dc precision, low noise, and fast settling time results in superior accuracy in medical instruments, electronic measurement, and automated test equipment. Unlike many competitive amplifiers, the AD8510/AD8512/AD8513 maintain their fast settling performance even with substantial capacitive loads. Unlike many older JFET amplifiers, the AD8510/AD8512/AD8513 do not suffer from output phase reversal when input voltages exceed the maximum common-mode voltage range.

Fast slew rate and great stability with capacitive loads make the AD8510/AD8512/AD8513 a perfect fit for high performance filters. Low input bias currents, low offset, and low noise result in a wide dynamic range of photodiode amplifier circuits. Low noise and distortion, high output current, and excellent speed make the AD8510/AD8512/AD8513 great choices for audio applications.

The AD8510/AD8512 are both available in 8-lead narrow SOIC_N and 8-lead MSOP packages. MSOP-packaged devices are only available in tape and reel. The AD8513 is available in 14-lead SOIC_N and TSSOP packages.

The AD8510/AD8512/AD8513 are specified over the −40°C to +125°C extended industrial temperature range.

Rev. K
Document Feedback
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REVISION HISTORY

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SPECIFICATIONS

At V_S = ±5 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage (B Grade)[1]	V_{OS}			0.08	0.4	mV
		−40°C < T_A < +125°C			0.8	mV
Offset Voltage (A Grade)	V_{OS}			0.1	0.9	mV
		−40°C < T_A < +125°C			1.8	mV
Input Bias Current	I_B			21	75	pA
		−40°C < T_A < +85°C			0.7	nA
		−40°C < T_A < +125°C			7.5	nA
Input Offset Current	I_{OS}			5	50	pA
		−40°C < T_A < +85°C			0.3	nA
		−40°C < T_A < +125°C			0.5	nA
Input Capacitance						
Differential				12.5		pF
Common Mode				11.5		pF
Input Voltage Range			−2.0		+2.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −2.0 V to +2.5 V	86	100		dB
Large-Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = −3 V to +3 V	65	107		V/mV
Offset Voltage Drift (B Grade)[1]	$\Delta V_{OS}/\Delta T$			0.9	5	µV/°C
Offset Voltage Drift (A Grade)	$\Delta V_{OS}/\Delta T$			1.7	12	µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ	4.1	4.3		V
Output Voltage Low	V_{OL}	R_L = 10 kΩ, −40°C < T_A < +125°C		−4.9	−4.7	V
Output Voltage High	V_{OH}	R_L = 2 kΩ	3.9	4.2		V
Output Voltage Low	V_{OL}	R_L = 2 kΩ, −40°C < T_A < +125°C		−4.9	−4.5	V
Output Voltage High	V_{OH}	R_L = 600 Ω	3.7	4.1		V
Output Voltage Low	V_{OL}	R_L = 600 Ω, −40°C < T_A < +125°C		−4.8	−4.2	V
Output Current	I_{OUT}		±40	±54		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V	86	130		dB
Supply Current/Amplifier	I_{SY}					
AD8510/AD8512/AD8513		V_O = 0 V		2.0	2.3	mA
AD8510/AD8512		−40°C < T_A < +125°C			2.5	mA
AD8513		−40°C < T_A < +125°C			2.75	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		20		V/µs
Gain Bandwidth Product	GBP			8		MHz
Settling Time	t_S	To 0.1%, 0 V to 4 V step, G = +1		0.4		µs
Total Harmonic Distortion (THD) + Noise	THD + N	1 kHz, G = +1, R_L = 2 kΩ		0.0005		%
Phase Margin	φ_M			44.5		Degrees
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 10 Hz		34		nV/√Hz
		f = 100 Hz		12		nV/√Hz
		f = 1 kHz		8.0	10	nV/√Hz
		f = 10 kHz		7.6		nV/√Hz
Peak-to-Peak Voltage Noise	e_n p-p	0.1 Hz to 10 Hz bandwidth		2.4	5.2	µV p-p

[1] AD8510/AD8512 only.

ELECTRICAL CHARACTERISTICS

At V_S = ±15 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage (B Grade)[1]	V_{OS}			0.08	0.4	mV
		−40°C < T_A < +125°C			0.8	mV
Offset Voltage (A Grade)	V_{OS}			0.1	1.0	mV
		−40°C < T_A < +125°C			1.8	mV
Input Bias Current	I_B			25	80	pA
		−40°C < T_A < +85°C			0.7	nA
		−40°C < T_A < +125°C			10	nA
Input Offset Current	I_{OS}			6	75	pA
		−40°C < T_A < +85°C			0.3	nA
		−40°C < T_A < +125°C			0.5	nA
Input Capacitance						
Differential				12.5		pF
Common Mode				11.5		pF
Input Voltage Range			−13.5		+13.0	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −12.5 V to +12.5 V	86	108		dB
Large-Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_{CM} = 0 V, V_O = −13.5 V to +13.5 V	115	196		V/mV
Offset Voltage Drift (B Grade)[1]	$\Delta V_{OS}/\Delta T$			1.0	5	µV/°C
Offset Voltage Drift (A Grade)	$\Delta V_{OS}/\Delta T$			1.7	12	µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ	+14.0	+14.2		V
Output Voltage Low	V_{OL}	R_L = 10 kΩ, −40°C < T_A < +125°C		−14.9	−14.6	V
Output Voltage High	V_{OH}	R_L = 2 kΩ	+13.8	+14.1		V
Output Voltage Low	V_{OL}	R_L = 2 kΩ, −40°C < T_A < +125°C		−14.8	−14.5	V
Output Voltage High	V_{OH}	R_L = 600 Ω	+13.5	+13.9		V
		R_L = 600 Ω, −40°C < T_A < +125°C	+11.4			V
Output Voltage Low	V_{OL}	R_L = 600 Ω		−14.3	−13.8	V
		R_L = 600 Ω, −40°C < T_A < +125°C			−12.1	V
Output Current	I_{OUT}			±70		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V	86			dB
Supply Current/Amplifier	I_{SY}					
AD8510/AD8512/AD8513		V_O = 0 V		2.2	2.5	mA
AD8510/AD8512		−40°C < T_A < +125°C			2.6	mA
AD8513		−40°C < T_A < +125°C			3.0	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		20		V/µs
Gain Bandwidth Product	GBP			8		MHz
Settling Time	t_S	To 0.1%, 0 V to 10 V step, G = +1		0.5		µs
		To 0.01%, 0 V to 10 V step, G = +1		0.9		µs
Total Harmonic Distortion (THD) + Noise	THD + N	1 kHz, G = +1, R_L = 2 kΩ		0.0005		%
Phase Margin	φ_M			52		Degrees

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 10 Hz		34		nV/√Hz
		f = 100 Hz		12		nV/√Hz
		f = 1 kHz		8.0	10	nV/√Hz
		f = 10 kHz		7.6		nV/√Hz
Peak-to-Peak Voltage Noise	e_n p-p	0.1 Hz to 10 Hz bandwidth		2.4	5.2	µV p-p

[1] AD8510/AD8512 only.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	±18 V
Input Voltage	$\pm V_S$
Output Short-Circuit Duration to GND	Observe derating curves
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Electrostatic Discharge (Human Body Model)	2000 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 4. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}	Unit
8-Lead MSOP (RM)	210	45	°C/W
8-Lead SOIC_N (R)	120	43	°C/W
14-Lead SOIC_N (R)	120	36	°C/W
14-Lead TSSOP (RU)	180	35	°C/W

[1] θ_{JA} is specified for worst case conditions, that is, θ_{JA} is specified for device soldered in circuit board for surface-mount packages.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

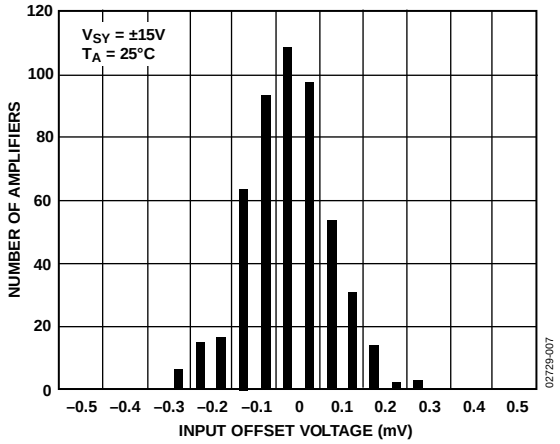


Figure 7. Input Offset Voltage Distribution

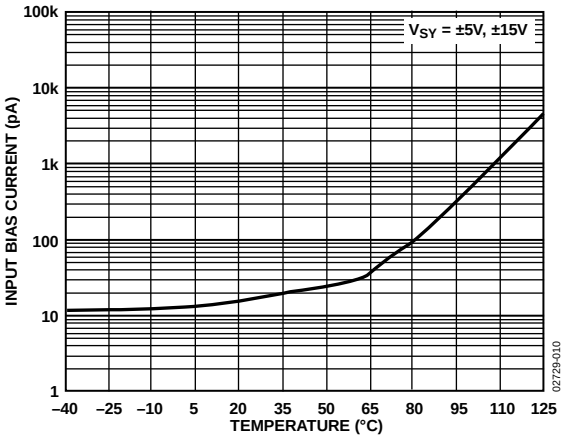


Figure 10. Input Bias Current vs. Temperature

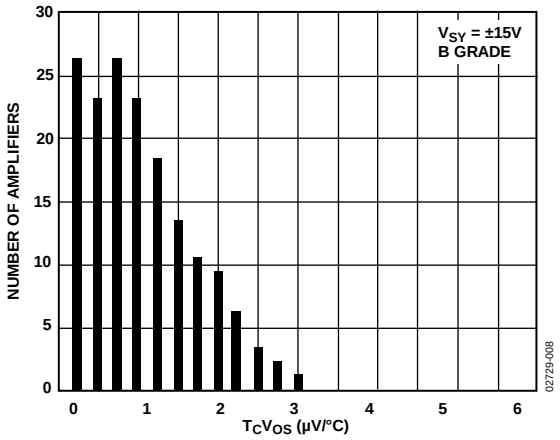


Figure 8. AD8510/AD8512 T_CV_{OS} Distribution

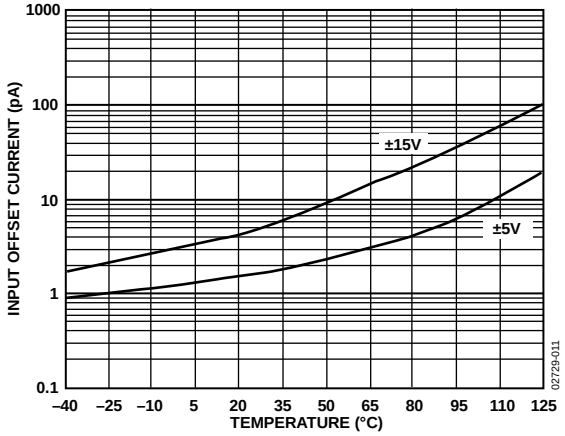


Figure 11. Input Offset Current vs. Temperature

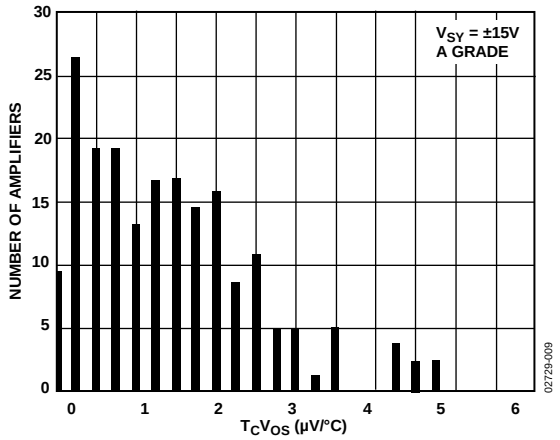


Figure 9. AD8510/AD8512 T_CV_{OS} Distribution

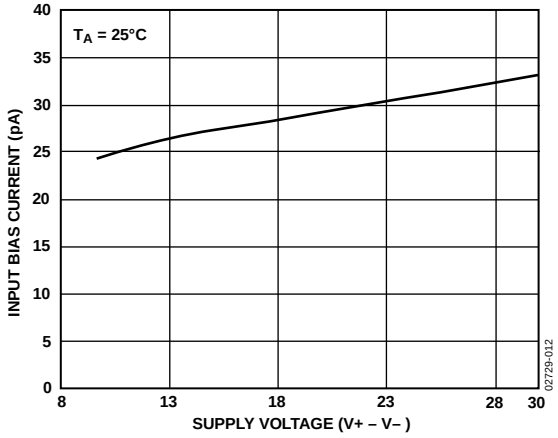


Figure 12. Input Bias Current vs. Supply Voltage

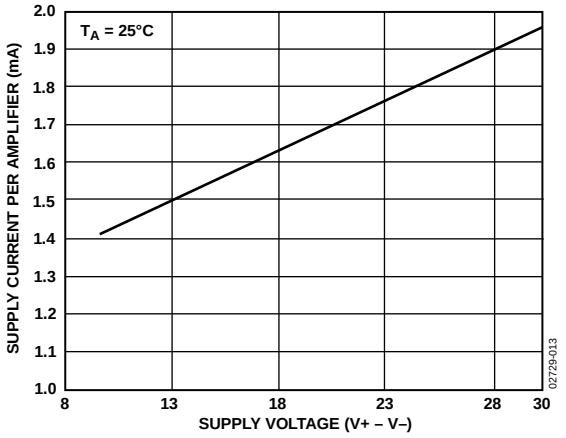


Figure 13. AD8512 Supply Current per Amplifier vs. Supply Voltage

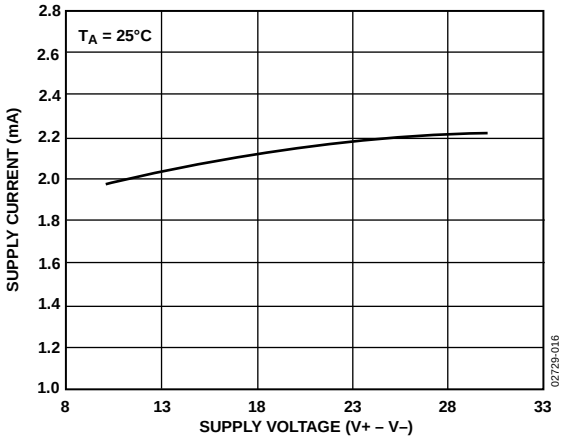


Figure 16. AD8510 Supply Current vs. Supply Voltage

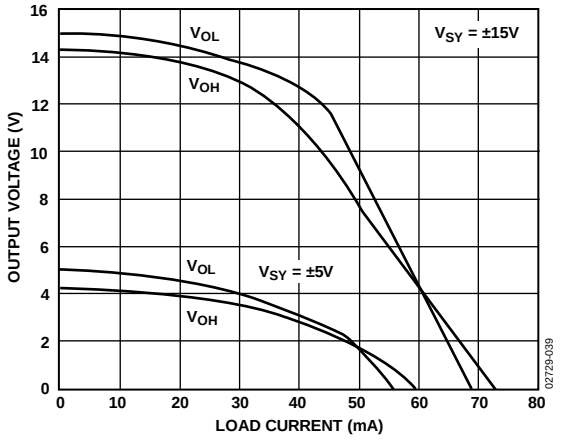


Figure 14. Output Voltage vs. Load Current

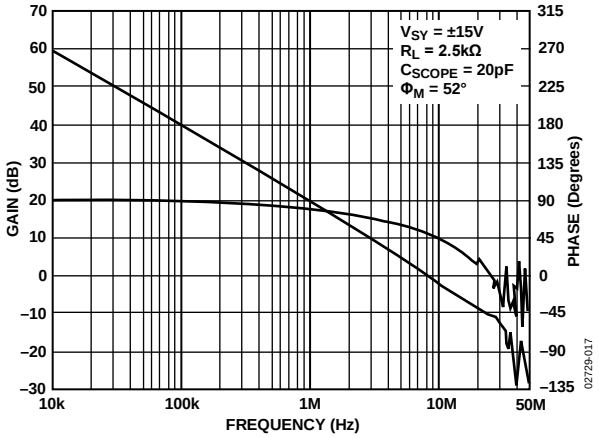


Figure 17. Open-Loop Gain and Phase vs. Frequency

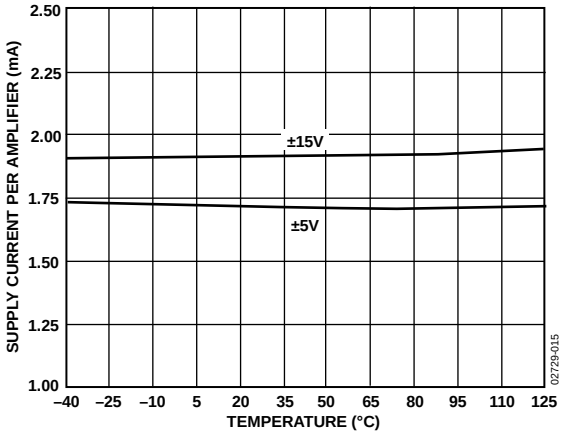


Figure 15. AD8512 Supply Current per Amplifier vs. Temperature

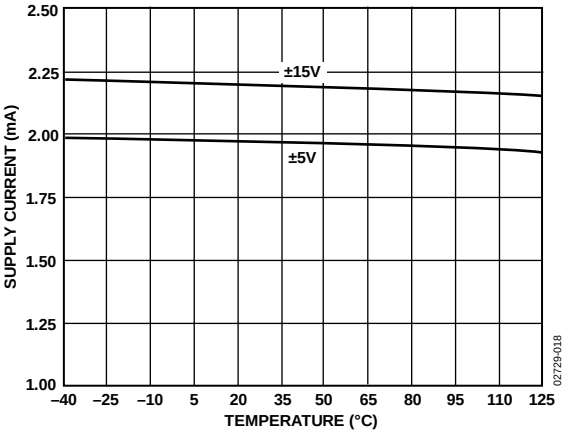


Figure 18. AD8510 Supply Current vs. Temperature

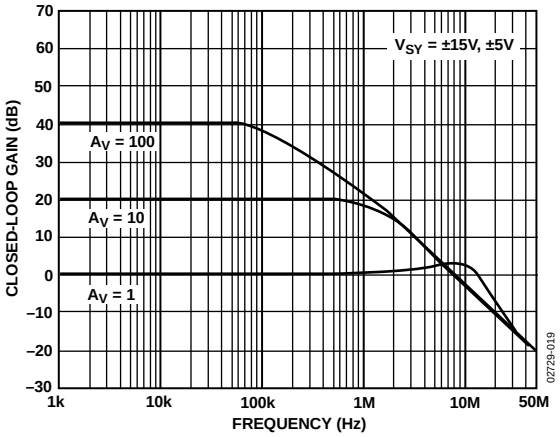


Figure 19. Closed-Loop Gain vs. Frequency

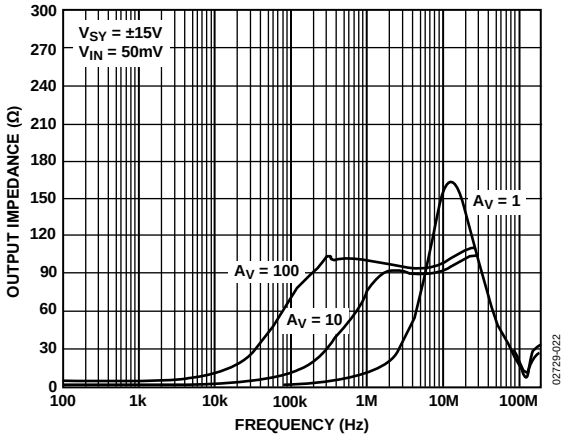


Figure 22. Output Impedance vs. Frequency

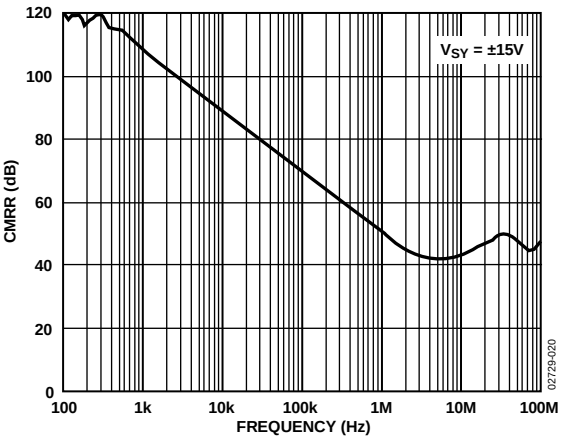


Figure 20. CMRR vs. Frequency

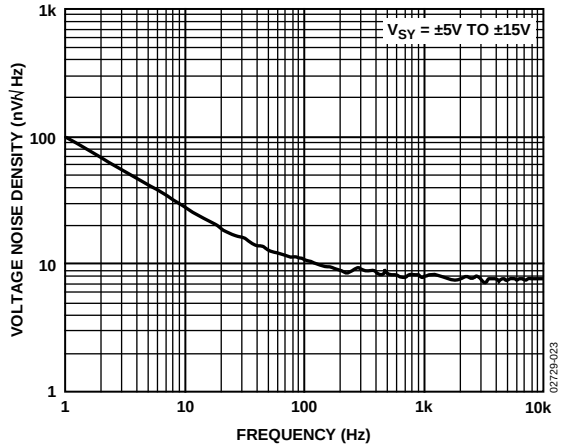


Figure 23. Voltage Noise Density vs. Frequency

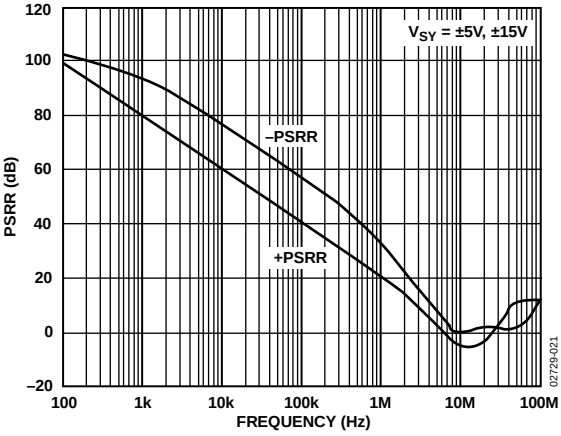


Figure 21. PSRR vs. Frequency

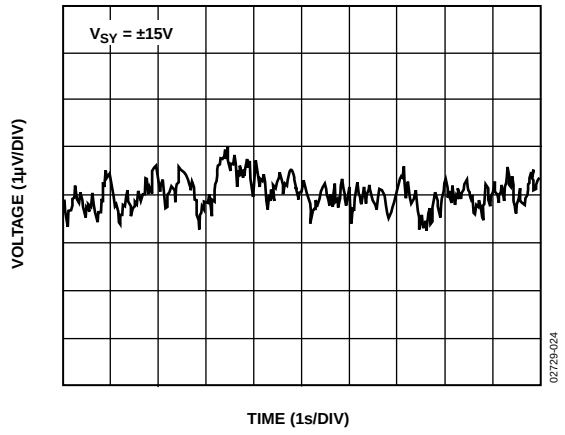


Figure 24. 0.1 Hz to 10 Hz Input Voltage Noise

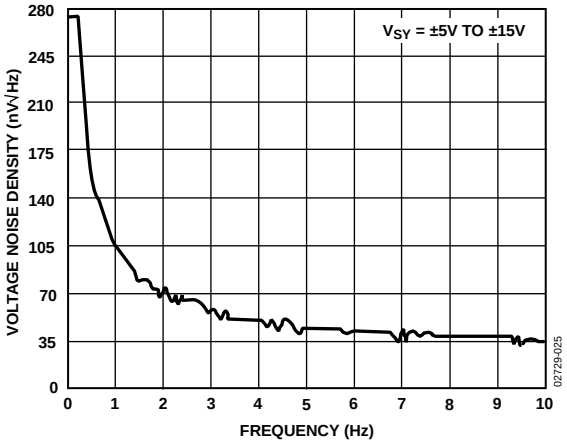


Figure 25. Voltage Noise Density vs. Frequency

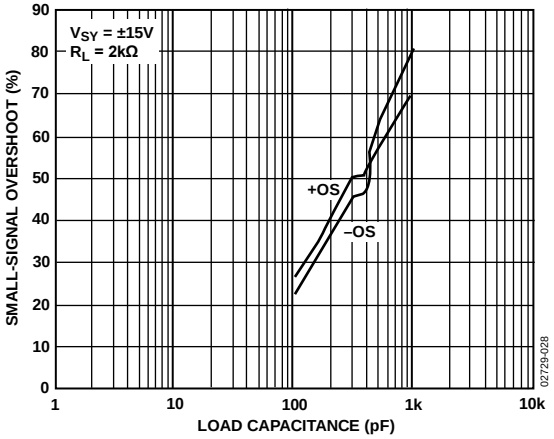


Figure 28. Small-Signal Overshoot vs. Load Capacitance

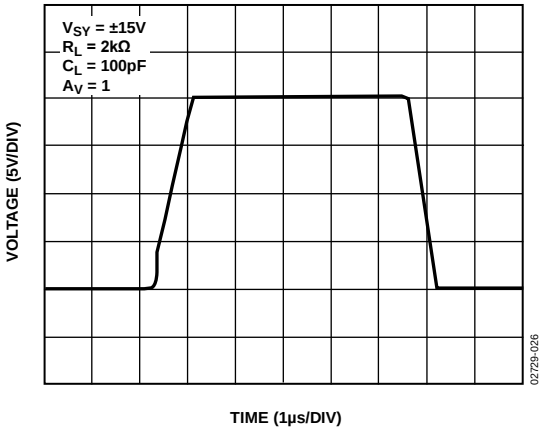


Figure 26. Large-Signal Transient Response

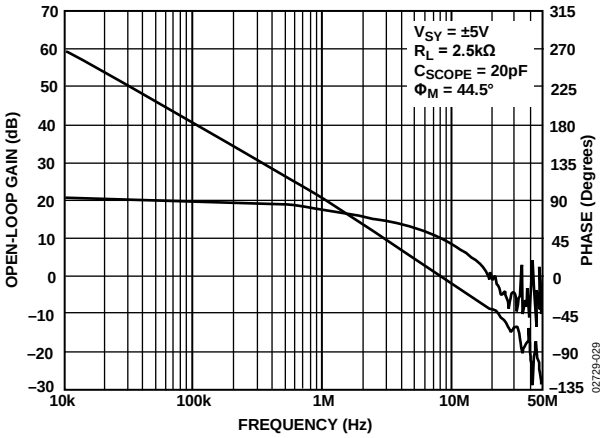


Figure 29. Open-Loop Gain and Phase vs. Frequency

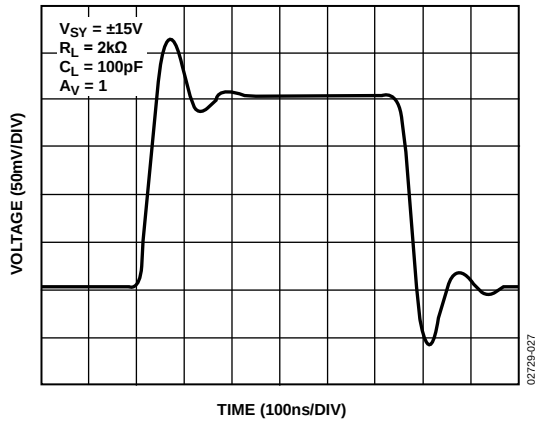


Figure 27. Small-Signal Transient Response

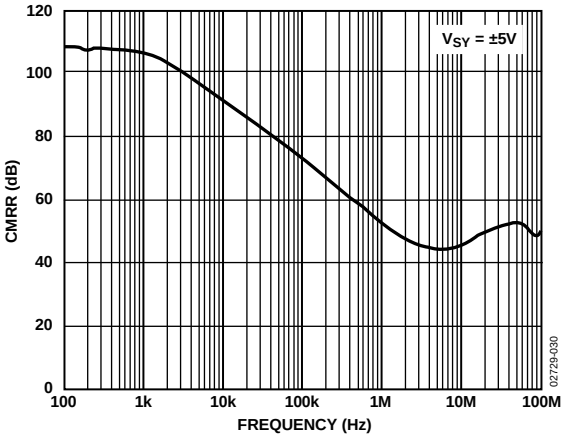


Figure 30. CMRR vs. Frequency

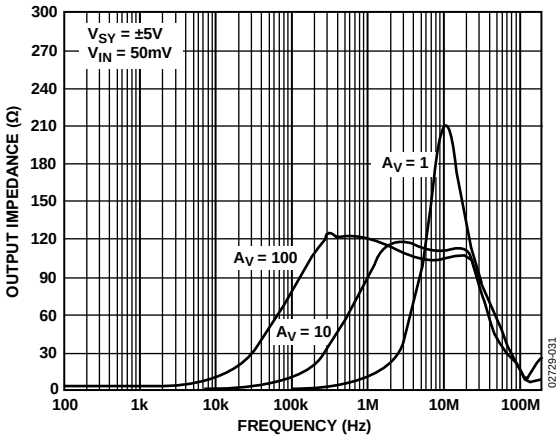


Figure 31. Output Impedance vs. Frequency

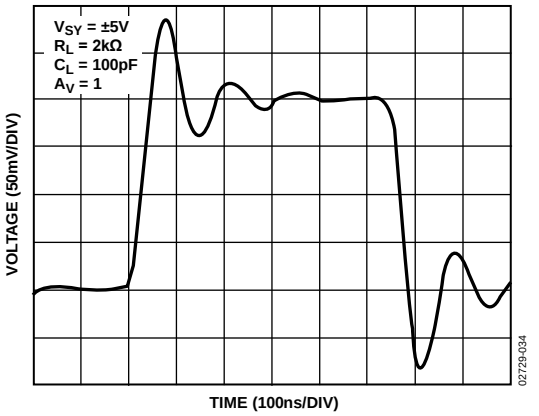


Figure 34. Small-Signal Transient Response

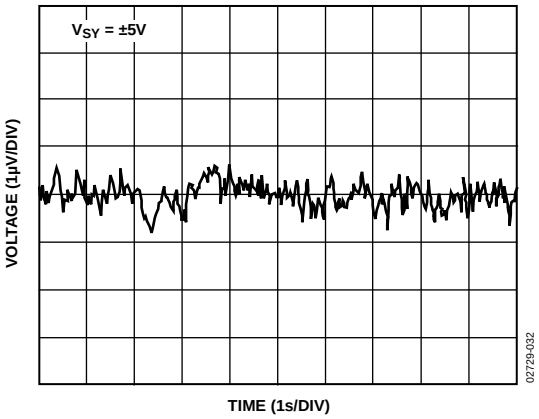


Figure 32. 0.1 Hz to 10 Hz Input Voltage Noise

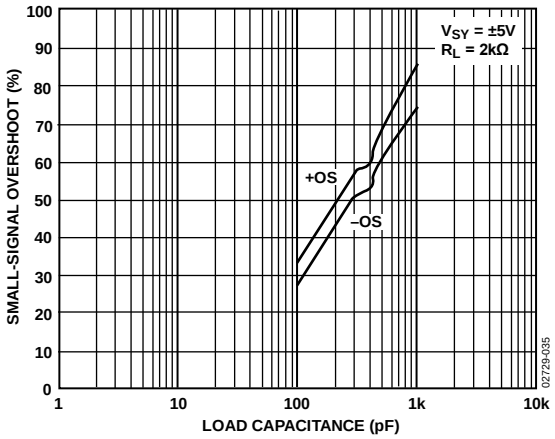


Figure 35. Small-Signal Overshoot vs. Load Capacitance

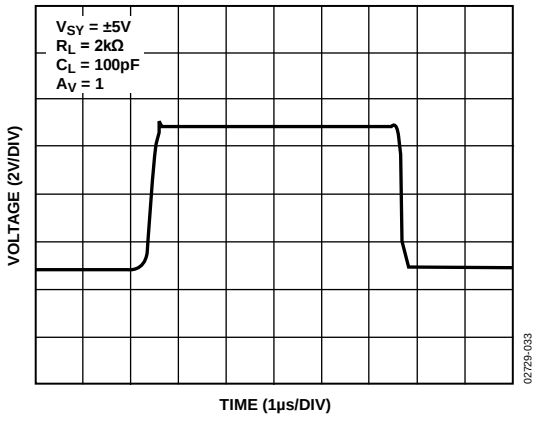


Figure 33. Large-Signal Transient Response

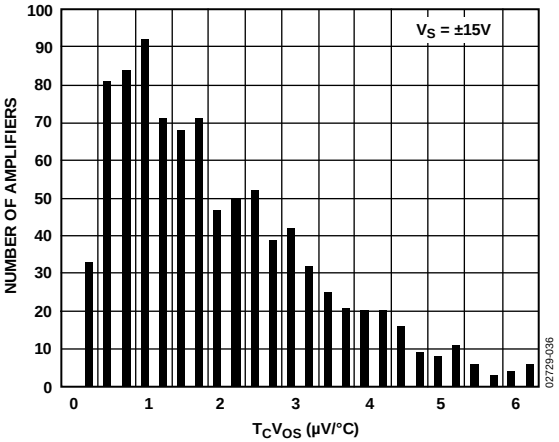


Figure 36. AD8513 T_CV_{OS} Distribution

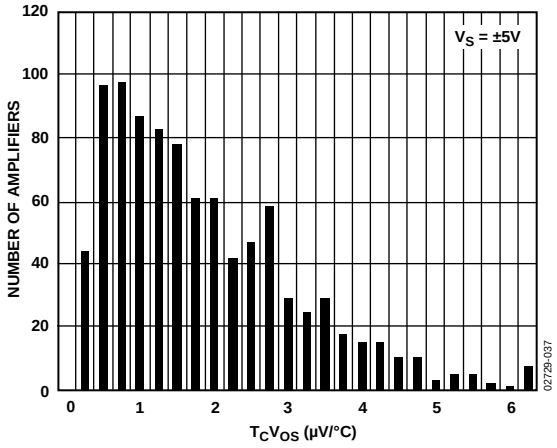


Figure 37. AD8513 T_CV_{OS} Distribution

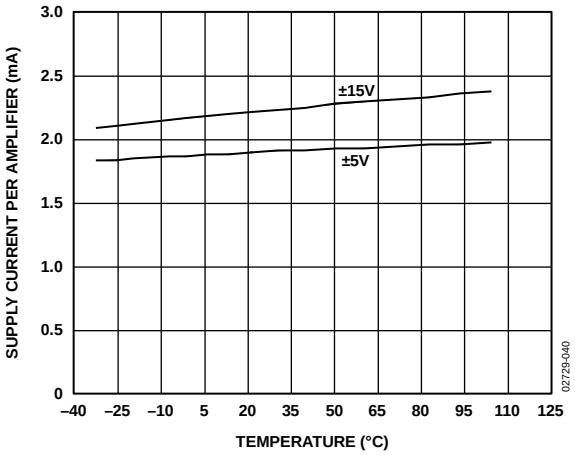


Figure 39. AD8513 Supply Current per Amplifier vs. Temperature

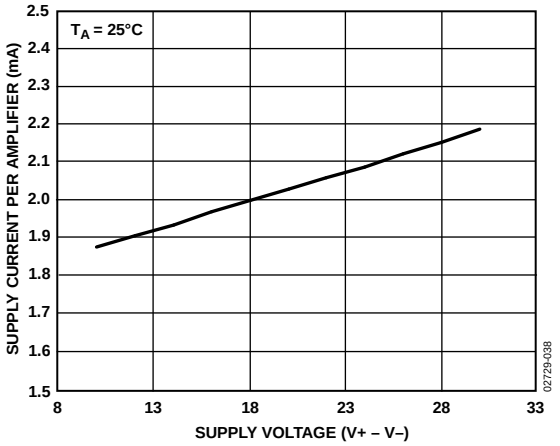


Figure 38. AD8513 Supply Current per Amplifier vs. Supply Voltage

GENERAL APPLICATION INFORMATION

INPUT OVERVOLTAGE PROTECTION

The AD8510/AD8512/AD8513 have internal protective circuitry that allows voltages as high as 0.7 V beyond the supplies to be applied at the input of either terminal without causing damage. For higher input voltages, a series resistor is necessary to limit the input current. The resistor value can be determined from the formula

$$\frac{V_{IN} - V_S}{R_S} \leq 5 \text{ mA}$$

With a very low offset current of <0.5 nA up to 125°C, higher resistor values can be used in series with the inputs. A 5 kΩ resistor protects the inputs from voltages as high as 25 V beyond the supplies and adds less than 10 μV to the offset.

OUTPUT PHASE REVERSAL

Phase reversal is a change of polarity in the transfer function of the amplifier. This can occur when the voltage applied at the input of an amplifier exceeds the maximum common-mode voltage.

Phase reversal can cause permanent damage to the device and can result in system lockups. The AD8510/AD8512/AD8513 do not exhibit phase reversal when input voltages are beyond the supplies.

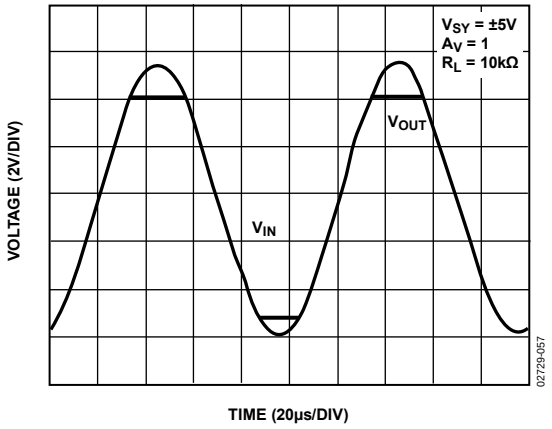


Figure 40. No Phase Reversal

TOTAL HARMONIC DISTORTION (THD) + NOISE

The AD8510/AD8512/AD8513 have low THD and excellent gain linearity, making these amplifiers great choices for precision circuits with high closed-loop gain and for audio application circuits. Figure 41 shows that the AD8510/AD8512/AD8513 have approximately 0.0005% of total distortion when configured in positive unity gain (the worst case) and driving a 100 kΩ load.

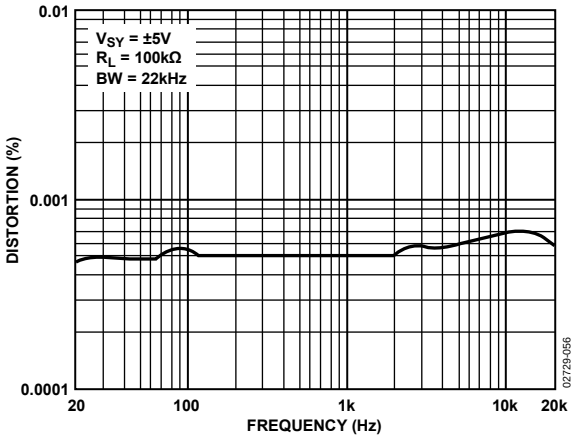


Figure 41. THD + N vs. Frequency

TOTAL NOISE INCLUDING SOURCE RESISTORS

The low input current noise and input bias current of the AD8510/AD8512/AD8513 make them the ideal amplifiers for circuits with substantial input source resistance. Input offset voltage increases by less than 15 nV per 500 Ω of source resistance at room temperature. The total noise density of the circuit is

$$e_{nTOTAL} = \sqrt{e_n^2 + (i_n R_S)^2 + 4kTR_S}$$

where:
e_n is the input voltage noise density of the devices.
i_n is the input current noise density of the devices.
R_S is the source resistance at the noninverting terminal.
k is Boltzmann's constant (1.38×10^{-23} J/K).
T is the ambient temperature in Kelvin (T = 273 + °C).

For R_S < 3.9 kΩ, e_n dominates and $e_{nTOTAL} \approx e_n$. The current noise of the AD8510/AD8512/AD8513 is so low that its total density does not become a significant term unless R_S is greater than 165 MΩ, an impractical value for most applications.

The total equivalent rms noise over a specific bandwidth is expressed as

$$e_{nTOTAL} = e_{nTOTAL}\sqrt{BW}$$

where BW is the bandwidth in hertz.

Note that the previous analysis is valid for frequencies larger than 150 Hz and assumes flat noise above 10 kHz. For lower frequencies, flicker noise (1/f) must be considered.

SETTLING TIME

Settling time is the time it takes the output of the amplifier to reach and remain within a percentage of its final value after a pulse is applied at the input. The AD8510/AD8512/AD8513 settle to within 0.01% in less than 900 ns with a step of 0 V to 10 V in unity gain. This makes each of these devices an excellent choice as a buffer at the output of DACs whose settling time is typically less than 1 µs.

In addition to the fast settling time and fast slew rate, low offset voltage drift and input offset current maintain the full accuracy of 12-bit converters over the entire operating temperature range.

OVERLOAD RECOVERY TIME

Overload recovery, also known as overdrive recovery, is the time it takes the output of an amplifier to recover to its linear region from a saturated condition. This recovery time is particularly important in applications where the amplifier must amplify small signals in the presence of large transient voltages.

Figure 42 shows the positive overload recovery of the AD8510/AD8512/AD8513. The output recovers in approximately 200 ns from a saturated condition.

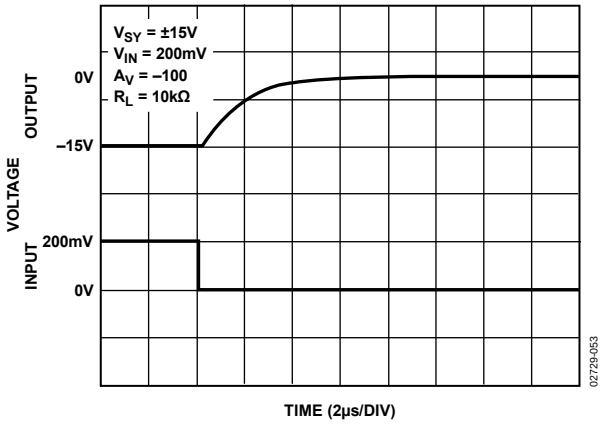


Figure 42. Positive Overload Recovery

The negative overdrive recovery time shown in Figure 43 is less than 200 ns.

In addition to the fast recovery time, the AD8510/AD8512/AD8513 show excellent symmetry of the positive and negative recovery times. This is an important feature for transient signal rectification because the output signal is kept equally undistorted throughout any given period.

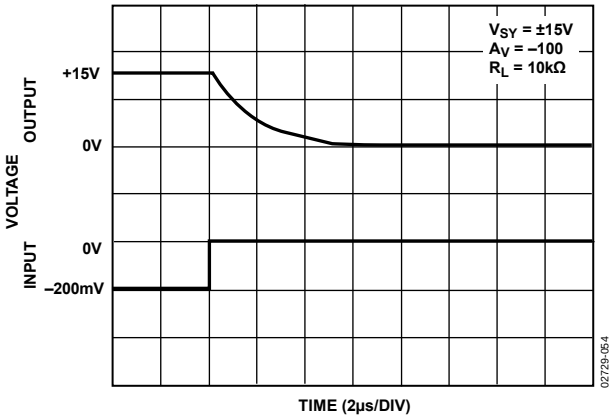


Figure 43. Negative Overload Recovery

CAPACITIVE LOAD DRIVE

The AD8510/AD8512/AD8513 are unconditionally stable at all gains in inverting and noninverting configurations. Each device is capable of driving a capacitive load of up to 1000 pF without oscillation in unity gain using the worst case configuration.

However, as with most amplifiers, driving larger capacitive loads in a unity-gain configuration can cause excessive overshoot and ringing, or even oscillation. A simple snubber network significantly reduces the amount of overshoot and ringing. The advantage of this configuration is that the output swing of the amplifier is not reduced, because R_S is outside the feedback loop.

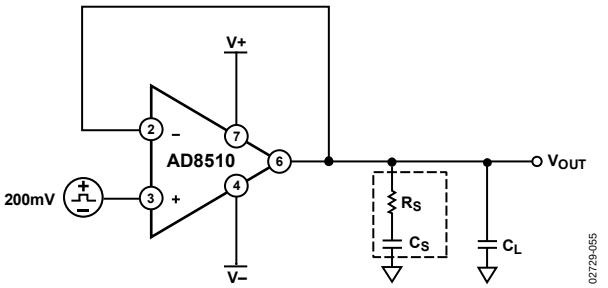


Figure 44. Snubber Network Configuration

Figure 45 shows a scope plot of the output of the AD8510/AD8512/AD8513 in response to a 400 mV pulse. The circuit is configured in positive unity gain (worst case) with a load experience of 500 pF.

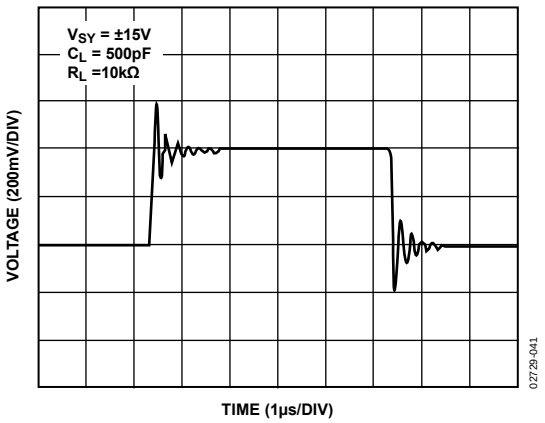


Figure 45. Capacitive Load Drive Without Snubber

When the snubber circuit is used, the overshoot is reduced from 55% to less than 3% with the same load capacitance. Ringing is virtually eliminated, as shown in Figure 46.

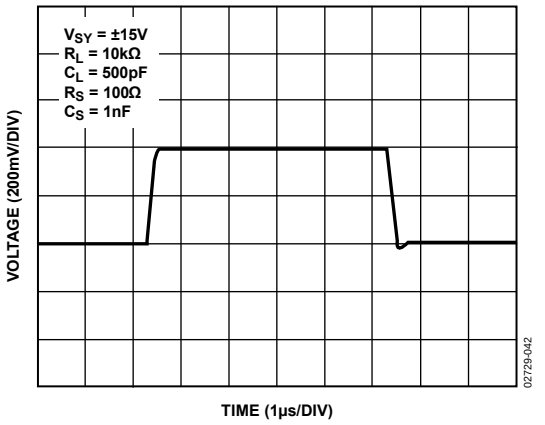


Figure 46. Capacitive Load with Snubber Network

Optimum values for R_S and C_S depend on the load capacitance and input stray capacitance and are determined empirically. Table 5 shows a few values that can be used as starting points.

Table 5. Optimum Values for Capacitive Loads

C_{LOAD}	R_S (Ω)	C_S
500 pF	100	1 nF
2 nF	70	100 pF
5 nF	60	300 pF

OPEN-LOOP GAIN AND PHASE RESPONSE

In addition to their impressive low noise, low offset voltage, and offset current, the AD8510/AD8512/AD8513 have excellent loop gain and phase response even when driving large resistive and capacitive loads.

Compared with Competitor A (see Figure 48) under the same conditions, with a 2.5 kΩ load at the output, the AD8510/AD8512/AD8513 have more than 8 MHz of bandwidth and a phase margin of more than 52°.

Competitor A, on the other hand, has only 4.5 MHz of bandwidth and 28° of phase margin under the same test conditions. Even with a 1 nF capacitive load in parallel with the 2 kΩ load at the output, the AD8510/AD8512/AD8513 show much better response than Competitor A, whose phase margin is degraded to less than 0, indicating oscillation.

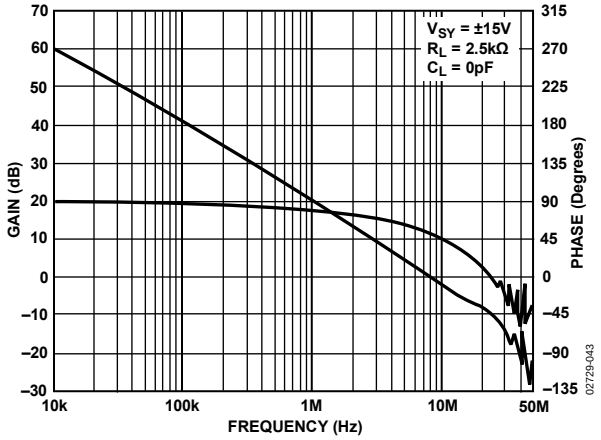


Figure 47. Frequency Response of the AD8510/AD8512/AD8513

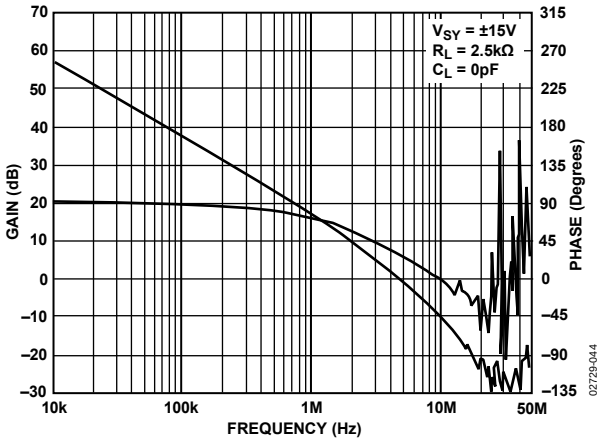


Figure 48. Frequency Response of Competitor A

PRECISION RECTIFIERS

Rectifying circuits are used in a multitude of applications. One of the most popular uses is in the design of regulated power supplies, where a rectifier circuit is used to convert an input sinusoid to a unipolar output voltage.

However, there are some potential problems with amplifiers used in this manner. When the input voltage (V_{IN}) is negative, the output is zero, and the magnitude of V_{IN} is doubled at the inputs of the op amp. If this voltage exceeds the power supply voltage, it can permanently damage some amplifiers. In addition, the op amp must come out of saturation when V_{IN} is negative. This delays the output signal because the amplifier requires time to enter its linear region.

Although the AD8510/AD8512/AD8513 have a very fast overdrive recovery time, which makes them great choices for the rectification of transient signals, the symmetry of the positive and negative recovery times is also important to keep the output signal undistorted.

Figure 49 shows the test circuit of the rectifier. The first stage of the circuit is a half-wave rectifier. When the sine wave applied at the input is positive, the output follows the input response. During the negative cycle of the input, the output tries to swing negative to follow the input, but the power supply restrains it to zero. In a similar fashion, the second stage is a follower during the positive cycle of the sine wave and an inverter during the negative cycle.

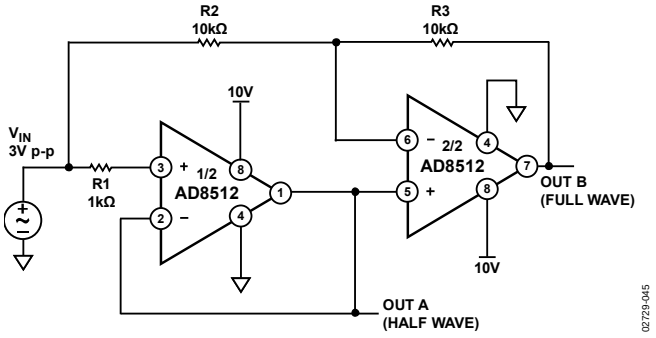


Figure 49. Half-Wave and Full-Wave Rectifiers

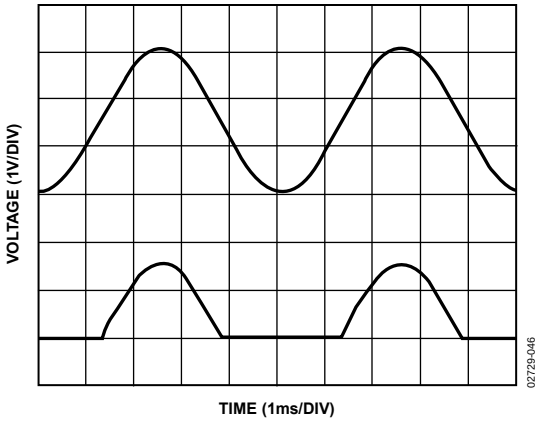


Figure 50. Half-Wave Rectifier Signal (OUT A in Figure 49)

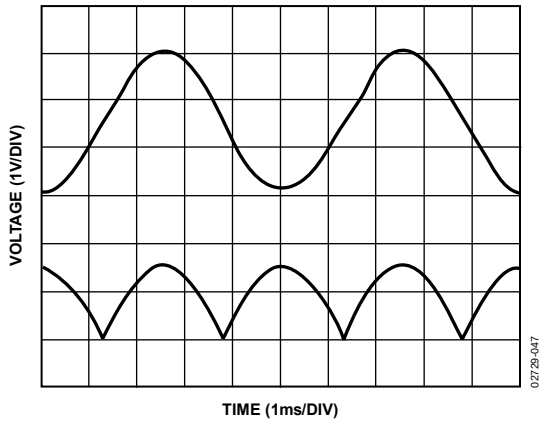


Figure 51. Full-Wave Rectifier Signal (OUT B in Figure 49)

I-V CONVERSION APPLICATIONS

Photodiode Circuits

Common applications for I-V conversion include photodiode circuits where the amplifier is used to convert a current emitted by a diode placed at the positive input terminal into an output voltage.

The AD8510/AD8512/AD8513's low input bias current, wide bandwidth, and low noise make them each an excellent choice for various photodiode applications, including fax machines, fiber optic controls, motion sensors, and bar code readers.

The circuit shown in Figure 52 uses a silicon diode with zero bias voltage. This is known as a photovoltaic mode; this configuration limits the overall noise and is suitable for instrumentation applications.

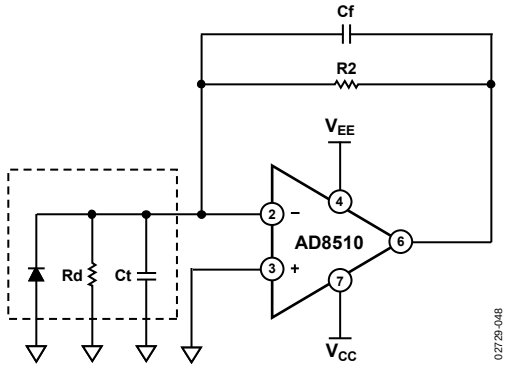


Figure 52. Equivalent Preamplifier Photodiode Circuit

A larger signal bandwidth can be attained at the expense of additional output noise. The total input capacitance (Ct) consists of the sum of the diode capacitance (typically 3 pF to 4 pF) and the amplifier's input capacitance (12 pF), which includes external parasitic capacitance. Ct creates a pole in the frequency response that can lead to an unstable system. To ensure stability and optimize the bandwidth of the signal, a capacitor is placed in the feedback loop of the circuit shown in Figure 52. It creates a zero and yields a bandwidth whose corner frequency is 1/(2π(R2Cf)).

The value of R2 can be determined by the ratio

V/I_D

where:
V is the desired output voltage of the op amp.
I_D is the diode current.

For example, if I_D is 100 μA and a 10 V output voltage is desired, R2 can be 100 kΩ. Rd (see Figure 52) is a junction resistance that drops typically by a factor of 2 for every 10°C increase in temperature.

A typical value for Rd is 1000 MΩ. Because Rd >> R2, the circuit behavior is not impacted by the effect of the junction resistance. The maximum signal bandwidth is

$$f_{MAX} = \sqrt{\frac{ft}{2\pi R2Ct}}$$

where *ft* is the unity-gain frequency of the amplifier.

Cf can be calculated by

$$Cf = \sqrt{\frac{Ct}{2\pi R2\,ft}}$$

where *ft* is the unity-gain frequency of the op amp, and it achieves a phase margin, φ_M, of approximately 45°.

A higher phase margin can be obtained by increasing the value of Cf. Setting Cf to twice the previous value yields approximately $\varphi_M = 65°$ and a maximal flat frequency response, but it reduces the maximum signal bandwidth by 50%.

Using the previous parameters with a $Cf \approx 1$ pF, the signal bandwidth is approximately 2.6 MHz.

Signal Transmission Applications

One popular signal transmission method uses pulse-width modulation. High data rates can require a fast comparator rather than an op amp. However, the need for sharp, undistorted signals can favor using a linear amplifier.

The AD8510/AD8512/AD8513 make excellent voltage comparators. In addition to a high slew rate, the AD8510/AD8512/AD8513 have a very fast saturation recovery time. In the absence of feedback, the amplifiers are in open-loop mode (very high gain). In this mode of operation, they spend much of their time in saturation.

The circuit shown in Figure 53 was used to compare two signals of different frequencies, namely a 100 Hz sine wave and a 1 kHz triangular wave. Figure 54 shows a scope plot of the resulting output waveforms. A pull-up resistor (typically 5 kΩ) can be connected from the output to V_{CC} if the output voltage needs to reach the positive rail. The trade-off is that power consumption is higher.

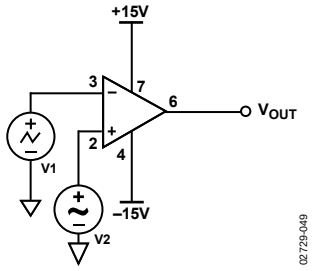


Figure 53. Pulse-Width Modulator

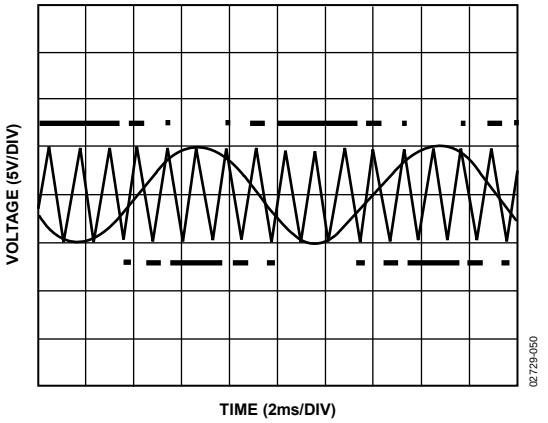


Figure 54. Pulse-Width Modulation

Crosstalk

Crosstalk, also known as channel separation, is a measure of signal feedthrough from one channel to another on the same IC. The AD8512/AD8513 have a channel separation of better than −90 dB for frequencies up to 10 kHz and of better than −50 dB for frequencies up to 10 MHz. Figure 56 shows the typical channel separation behavior between Amplifier A (driving amplifier) and each of the following: Amplifier B, Amplifier C, and Amplifier D.

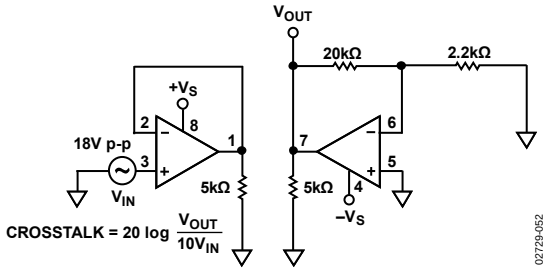


Figure 55. Crosstalk Test Circuit

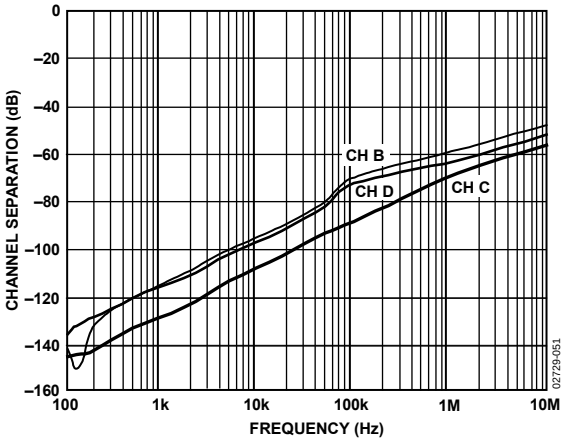


Figure 56. Channel Separation

The AD8510 single has two additional active terminals that are not present on the AD8512 dual or AD8513 quad devices. These pins are labeled null and are used for fine adjustment of the input offset voltage. Although the guaranteed maximum offset voltage at room temperature is 400 µV and over the −40°C to +125°C range is 800 mV maximum, this offset voltage can be reduced by adding a potentiometer to the null pins as shown in Figure 57. With the 20 kΩ potentiometer shown, the adjustment range is approximately ±3.5 mV. The potentiometer parallels low value resistors in the drain circuit of the JFET differential input pair and allows unbalancing of the drain currents to change the offset voltage. If offset adjustment is not required, these pins must be left unconnected.

Caution must be used when adding adjusting potentiometers to any op amp with this capability for several reasons. First, there is gain from these nodes to the output; therefore, capacitive coupling from noisy traces to these nodes injects noise into the signal path. Second, the temperature coefficient of the potentiometer does not match the temperature coefficient of the internal resistors, so the offset voltage drift with temperature is slightly affected. Third, this provision is for adjusting the offset voltage of the op amp, not for adjusting the offset of the overall system. Although it is tempting to decrease the value of the potentiometer to attain more range, this adversely affects the dc and ac parameters. Instead, increase the potentiometer to 50 kΩ to decrease the range if needed.

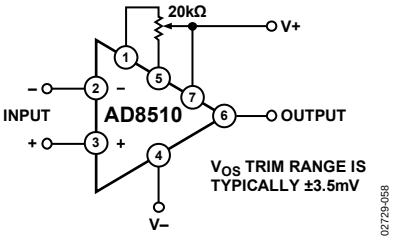
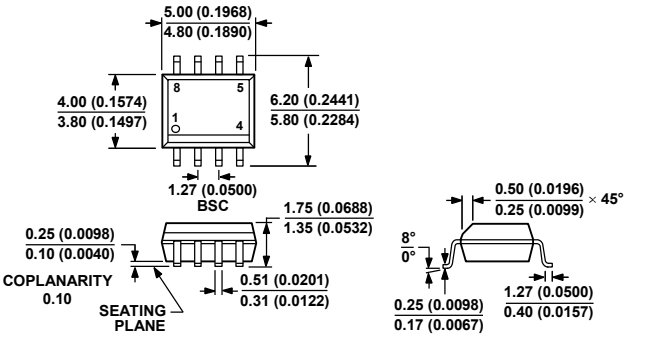


Figure 57. Optional Offset Nulling Circuit

OUTLINE DIMENSIONS



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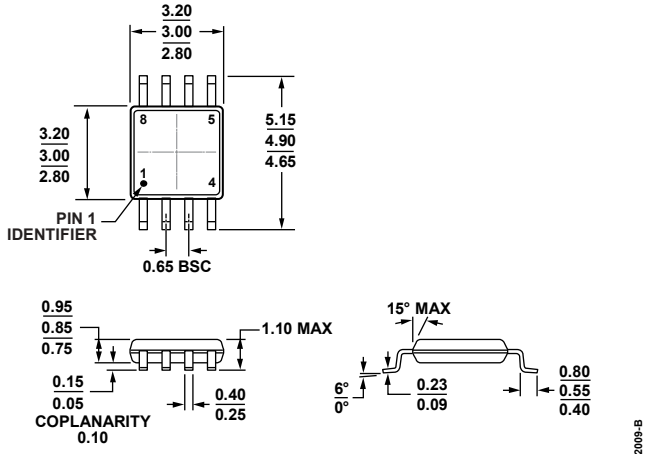
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

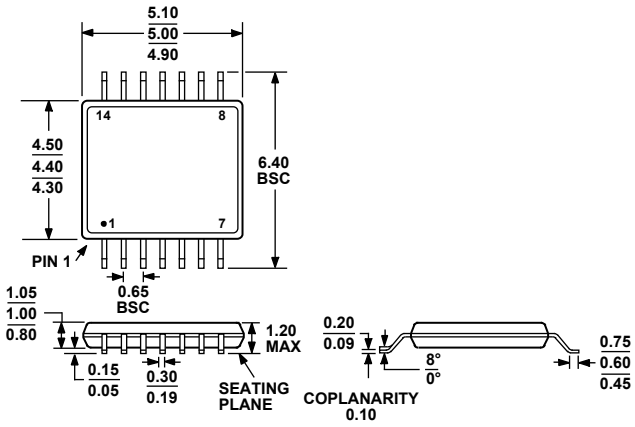
Figure 58. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-187-AA

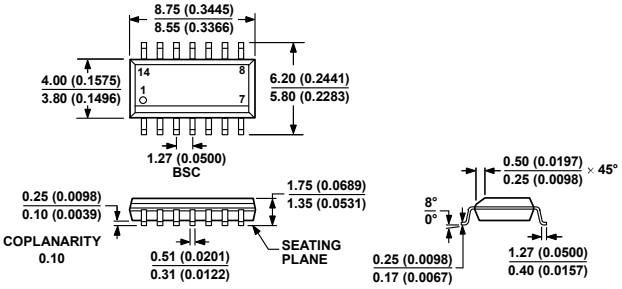
10-07-2009-B

Figure 59. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 60. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters



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060506-A

Figure 61. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-14)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Marking Code
AD8510ARMZ-REEL	−40°C to +125°C	8-Lead MSOP	RM-8	B7A#
AD8510ARMZ	−40°C to +125°C	8-Lead MSOP	RM-8	B7A#
AD8510ARZ	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8510ARZ-REEL	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8510ARZ-REEL7	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8510BRZ	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8510BRZ-REEL	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8510BRZ-REEL7	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8512ARMZ-REEL	−40°C to +125°C	8-Lead MSOP	RM-8	B8A#
AD8512ARMZ	−40°C to +125°C	8-Lead MSOP	RM-8	B8A#
AD8512ARZ	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8512ARZ-REEL	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8512ARZ-REEL7	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8512BRZ	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8512BRZ-REEL	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8512BRZ-REEL7	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8513ARZ	−40°C to +125°C	14-Lead SOIC_N	R-14	
AD8513ARZ-REEL	−40°C to +125°C	14-Lead SOIC_N	R-14	
AD8513ARZ-REEL7	−40°C to +125°C	14-Lead SOIC_N	R-14	
AD8513ARUZ	−40°C to +125°C	14-Lead TSSOP	RU-14	
AD8513ARUZ-REEL	−40°C to +125°C	14-Lead TSSOP	RU-14	

[1] Z = RoHS Compliant Part, # denotes RoHS compliant product may be top or bottom marked.

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