THE DATASHEET OF

ADP3330ART-3.6-RL

High Accuracy, Ultralow I_Q, 200 mA, SOT-23, anyCAP Low Dropout Regulator

Data Sheet **ADP3330**

FEATURES

- High accuracy over line and load
  - ±0.7% at +25°C
  - ±1.4% over temperature
- Ultralow dropout voltage: 140 mV (typical) at 200 mA
- Requires only C_{OUT}= 0.47 µF for stability
- anyCAP = stable with any type of capacitor, including multilayer ceramic capacitors (MLCC)
- Current and thermal limiting
- Low noise
- Low shutdown current: <2 µA
- 2.9 V to 12 V supply range
- –40°C to +85°C ambient temperature range
- Ultrasmall, thermally enhanced, chip-on-lead™ 6-lead SOT-23 package

APPLICATIONS

- Cell phones
- Notebook and palmtop computers
- Battery-powered systems
- PCMCIA regulators
- Bar code scanners
- Camcorders and cameras

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM

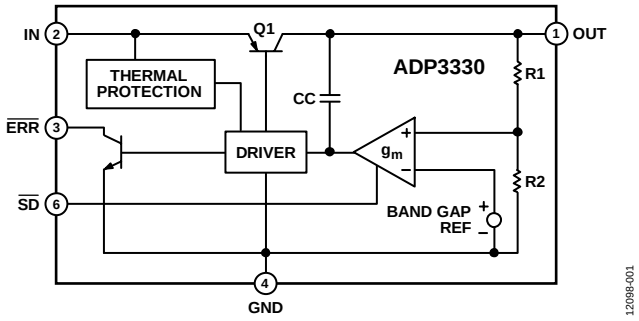

Figure 1.

GENERAL DESCRIPTION

The ADP3330 is a member of the Analog Devices, Inc., precision low dropout (LDO) anyCAP® voltage regulator family of products. The ADP3330 operates with an input voltage range of 2.9 V to 12 V and delivers a load current up to 200 mA. The ADP3330 stands out from the conventional LDOs with a novel architecture and an enhanced process that enables it to offer performance advantages and higher output current than its competition. Its patented design requires only a minimum output capacitor of 0.47 µF for stability. This device is insensitive to output capacitor equivalent series resistance (ESR), and is stable with any good quality capacitor, including ceramic (MLCC) types for space restricted applications. The ADP3330 achieves exceptional accuracy of ±0.7% at room temperature and ±1.4% over temperature, line and load variations. The dropout voltage of the ADP3330 is only 140 mV (typical) at 200 mA. This device also includes a safety current limit, thermal overload protection, and a shutdown feature. In shutdown mode, the ground current is reduced to less than 2 µA. The ADP3330 has an ultralow ground current 34 µA (typical) in light load situations.

The 6-lead SOT-23 package has been thermally enhanced using Analog Devices proprietary chip-on-lead feature to maximize power dissipation.

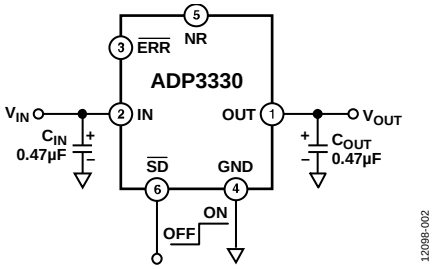

Figure 2. Typical Application Circuit

Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

5/15—Rev. B to Rev. C

Changes to General Description Section ... 1
Changes to Chip-On-Lead Package Section ... 11
Changes to Ordering Guide ... 14

5/14—Rev. A to Rev. B

Updated Format ... Universal
Changed 0.47 mF to 0.47 µF, Features Section ... 1
Changes to General Description Section ... 1
Changed −2.5 V to 2.5 V, ADP3330-xx Section ... 3
Changes to Table 1 ... 3
Changes to Table 2 ... 4
Changes to Figure 4 Caption through Figure 7 Caption ... 7
Changes to Figure 10, Figure 13 Caption, Figure 14 Caption, and Figure 15 ... 8
Changes to Figure 16, Figure 17, and Figure 19 Caption ... 9
Changes to Printed Circuit Board (PCB) Layout Considerations Section, and Low Power, Low Dropout Applications Section ... 12
Updated Outline Dimensions ... 14
Changes to Ordering Guide ... 14

8/99—Rev. 0 to Rev. A

SPECIFICATIONS

ADP3330

At T_A = −40°C to +85°C, V_{IN} = 7 V, C_{IN} = 0.47 µF, C_{OUT} = 0.47 µF, unless otherwise noted. Ambient temperature of 85°C corresponds to a junction temperature of 125°C under typical full load test conditions. Application stable with no load. The following specifications apply to all voltage options except 2.5 V.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT VOLTAGE ACCURACY	V_{OUT}	V_{IN} = V_{OUTNOM} + 0.25 V to 12 V, I_L = 0.1 mA to 200 mA, T_A = 25°C	−0.7		+0.7	%
		V_{IN} = V_{OUTNOM} + 0.25 V to 12 V, I_L = 0.1 mA to 150 mA, T_A = −40°C to +85°C	−1.4		+1.4	%
		V_{IN} = V_{OUTNOM} + 0.25 V to 12 V, I_L = 0.1 mA to 200 mA, T_A = −20°C to +85°C	−1.4		+1.4	%
LINE REGULATION	$\Delta V_O/\Delta V_{IN}$	V_{IN} = V_{OUTNOM} + 0.25 V to 12 V, T_A = 25°C		0.04		mV/V
LOAD REGULATION	$\Delta V_O/\Delta I_L$	I_L = 0.1 mA to 200 mA, T_A = 25°C		0.04		mV/mA
GROUND CURRENT	I_{GND}	I_L = 200 mA, T_A = −20°C to +85°C		1.6	4.0	mA
		I_L = 150 mA		1.2	3.1	mA
		I_L = 50 mA		0.4	1.1	mA
		I_L = 0.1 mA		34	50	µA
GROUND CURRENT IN DROPOUT	I_{GND}	V_{IN} = V_{OUTNOM} − 100 mV, I_L = 0.1 mA		37	55	µA
DROPOUT VOLTAGE	V_{DROP}	V_{OUT} = 98% of V_{OUTNOM}				
		I_L = 200 mA, T_A = −20°C to +85°C		140	230	mV
		I_L = 150 mA		110	170	mV
		I_L = 10 mA		42	60	mV
		I_L = 1 mA		25	50[1]	mV
PEAK LOAD CURRENT	I_{LDPK}	V_{IN} = V_{OUTNOM} + 1 V		300		mA
OUTPUT NOISE[2]	V_{NOISE}	f = 10 Hz to 100 kHz, C_L = 10 µF, I_L = 200 mA, C_{NR} = 10 nF, V_{OUT} = 3 V		47		µV rms
		f = 10 Hz to 100 kHz, C_L = 10 µF, I_L = 200 mA, C_{NR} = 0 nF, V_{OUT} = 3 V		95		µV rms
SHUTDOWN THRESHOLD	V_{THSD}	On	2.0			V
		Off			0.4	V
SHUTDOWN PIN INPUT CURRENT	I_{SD}	V_{IN} = 12 V, 0 V<$\overline{SD}$ ≤12 V		1.9	9	µA
		0 V <$\overline{SD}$ ≤5 V		1.4	6	µA
GROUND CURRENT IN SHUTDOWN MODE	I_{GNDSD}	$\overline{SD}$ = 0 V, V_{IN} = 12 V		0.01	2	µA
OUTPUT CURRENT IN SHUTDOWN MODE	I_{OSD}	T_A = 25°C at V_{IN} = 12 V			1	µA
		T_A = 85°C at V_{IN} = 12 V			2	µA
ERROR PIN OUTPUT LEAKAGE	I_{EL}	V_{EO} = 5 V			1	µA
ERROR PIN OUTPUT LOW VOLTAGE	V_{EOL}	I_{SINK} = 400 µA		0.19	0.40	V

[1] Application stable with no load.
[2] See Figure 21 and Applications Information section for additional information.

ADP3330-2.5

At T_A = −40°C to +85°C, V_{IN} = 7 V, C_{IN} = 0.47 µF, C_{OUT} = 0.47 µF, unless otherwise noted. Ambient temperature of +85°C corresponds to a junction temperature of +125°C under typical full load test conditions. Application stable with no load.

Table 2.

Parameter	Symbol	Test Conditions/Conditions	Min	Typ	Max	Unit
OUTPUT VOLTAGE ACCURACY	V_{OUT}	V_{IN} = 2.9 V to 12 V, I_L = 0.1 mA to 200 mA, T_A = 25°C	−0.7		+0.7	%
		V_{IN} = 2.9 V to 12 V, I_L = 0.1 mA to 150 mA, T_A = −40°C to +85°C	−1.4		+1.4	%
		V_{IN} = 2.9 V to 12 V, I_L = 0.1 mA to 200 mA, T_A = −20°C to +85°C	−1.4		+1.4	%
LINE REGULATION	$\Delta V_O/\Delta V_{IN}$	V_{IN} = 2.9 V to 12 V, T_A = 25°C		0.04		mV/V
LOAD REGULATION	$\Delta V_O/\Delta I_L$	I_L = 0.1 mA to 200 mA, T_A = 25°C		0.04		mV/mA
GROUND CURRENT	I_{GND}	I_L = 200 mA, T_A = −20°C to +85°C		1.6	4.0	mA
		I_L = 150 mA		1.2	3.1	mA
		I_L = 50 mA		0.4	1.1	mA
		I_L = 0.1 mA		34	50	µA
GROUND CURRENT IN DROPOUT	I_{GND}	V_{IN} = V_{OUTNOM} − 100 mV, I_L = 0.1 mA		37	55	µA
DROPOUT VOLTAGE	V_{DROP}	V_{OUT} = 98% of V_{OUTNOM}				
		I_L = 200 mA, T_A = −20°C to +85°C		140	230	mV
		I_L = 150 mA		110	170	mV
		I_L = 10 mA		42	60	mV
		I_L = 1 mA		25	50[1]	mV
PEAK LOAD CURRENT	I_{LDPK}	V_{IN} = V_{OUTNOM} + 1 V		300		mA
OUTPUT NOISE[2]	V_{NOISE}	f = 10 Hz to 100 kHz, C_L = 10 µF, I_L = 200 mA, C_{NR} = 10 nF, V_{OUT} = 3 V		47		µV rms
		f = 10 Hz to 100 kHz, C_L = 10 µF, I_L = 200 mA, C_{NR} = 0 nF, V_{OUT} = 3 V		95		µV rms
SHUTDOWN THRESHOLD	V_{THSD}	On	2.0			V
		Off			0.4	V
SHUTDOWN PIN INPUT CURRENT	I_{SD}	V_{IN} = 12 V, 0 V<$\overline{SD}$ ≤12 V		1.9	9	µA
		0 V <$\overline{SD}$ ≤5 V		1.4	6	µA
GROUND CURRENT IN SHUTDOWN MODE	I_{GNDSD}	$\overline{SD}$ = 0 V, V_{IN} = 12 V		0.01	2	µA
OUTPUT CURRENT IN SHUTDOWN MODE	I_{OSD}	T_A = 25°C at V_{IN} = 12 V			1	µA
		T_A = 85°C at V_{IN} = 12 V			2	µA
ERROR PIN OUTPUT LEAKAGE	I_{EL}	V_{EO} = 5 V			1	µA
ERROR PIN OUTPUT LOW VOLTAGE	V_{EOL}	I_{SINK} = 400 µA		0.19	0.40	V

[1] Application stable with no load.
[2] See Figure 21 and Applications Information section for additional information.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Input Supply Voltage	−0.3 V to +16 V
Shutdown Input Voltage	−0.3 V to +16 V
Power Dissipation	Internally limited
Operating Ambient Temperature Range	−40°C to +85°C
Operating Junction Temperature Range	−40°C to +125°C
θ_{JA} (4-Layer Board)	165°C/W
θ_{JA} (2-Layer Board)	190°C/W
Storage Temperature Range	−65°C to +150°C
Lead Temperature (not a range)	
(Soldering 10 seconds)	300°C
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

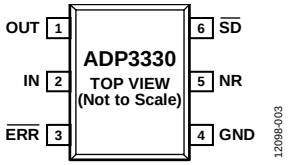

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUT	Output of the Regulator. Bypass to ground with a 0.47 µF or larger capacitor.
2	IN	Regulator Input.
3	$\overline{ERR}$	Open Collector Output. This pin goes low to indicate that the output is about to go out of regulation.
4	GND	Ground Pin.
5	NR	Noise Reduction Pin. This pin is used for further reduction of output noise (see the Applications Information section). Do not connect if this pin is not used.
6	$\overline{SD}$	Active Low Shutdown Pin. Connect to ground to disable the regulator output. When shutdown is not used, this pin must be connected to the input pin.

TYPICAL PERFORMANCE CHARACTERISTICS

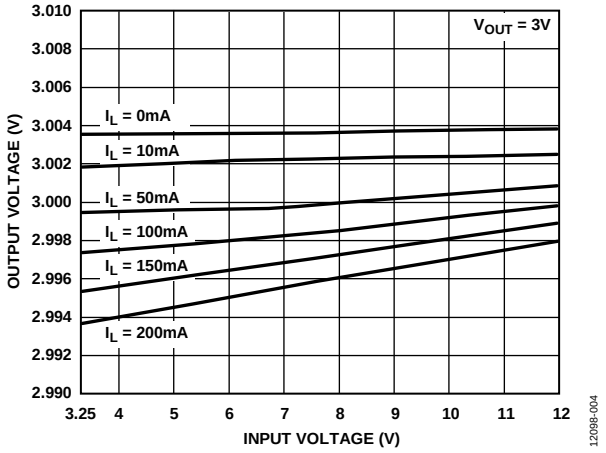

Figure 4. Line Regulation Output Voltage vs. Input Voltage

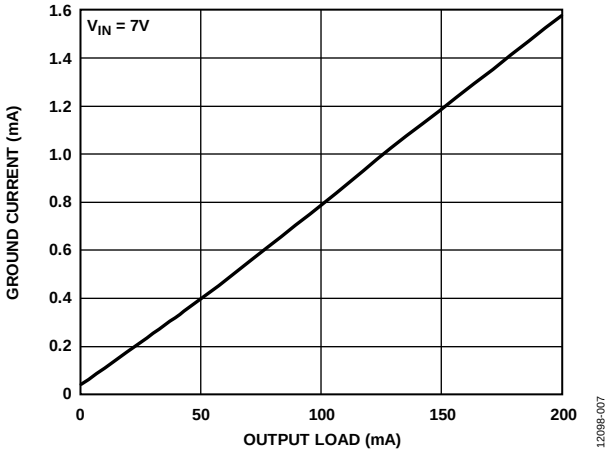

Figure 7. Ground Current vs. Output Current

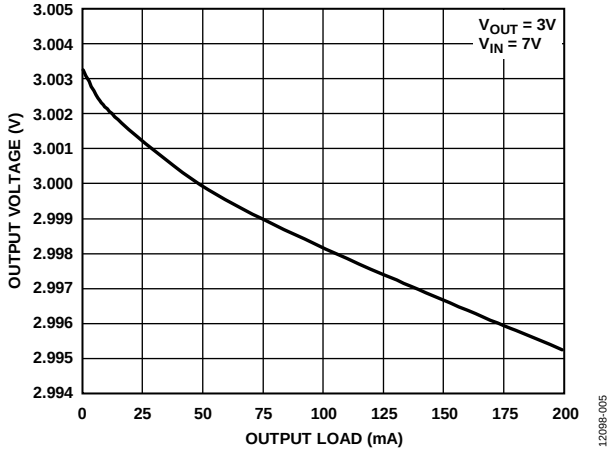

Figure 5. Output Voltage vs. Output Current

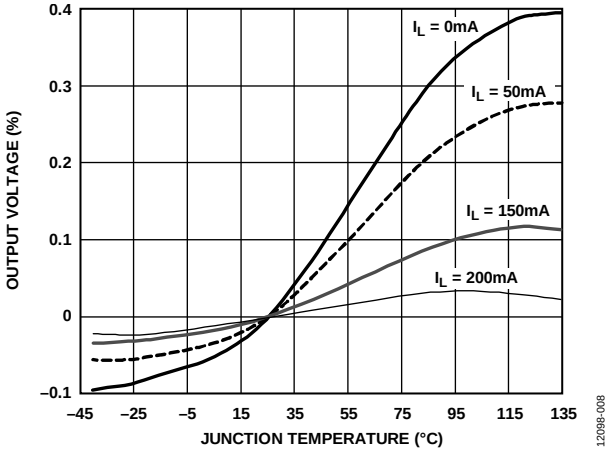

Figure 8. Output Voltage Variation Percent vs. Junction Temperature

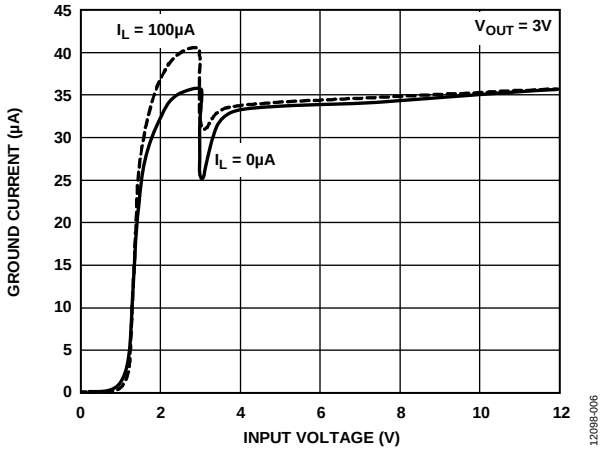

Figure 6. Ground Current vs. Input Voltage

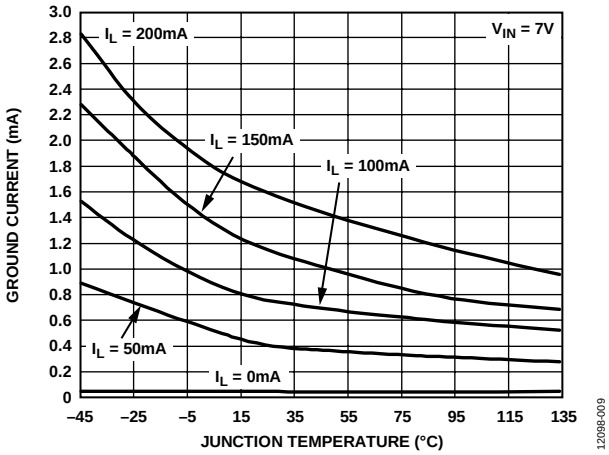

Figure 9. Ground Current vs. Junction Temperature

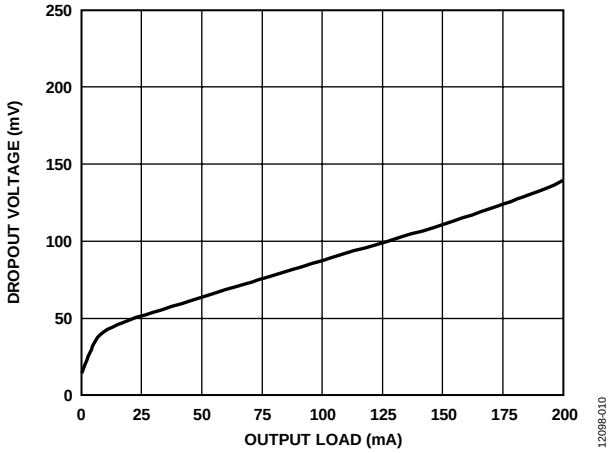

Figure 10. Dropout Voltage vs. Output Current

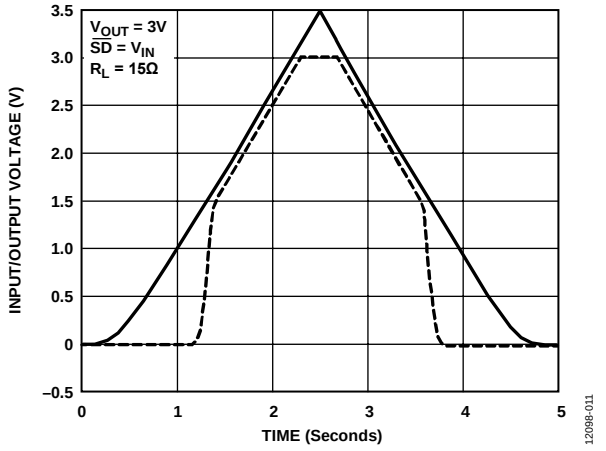

Figure 11. Power-Up/Power-Down

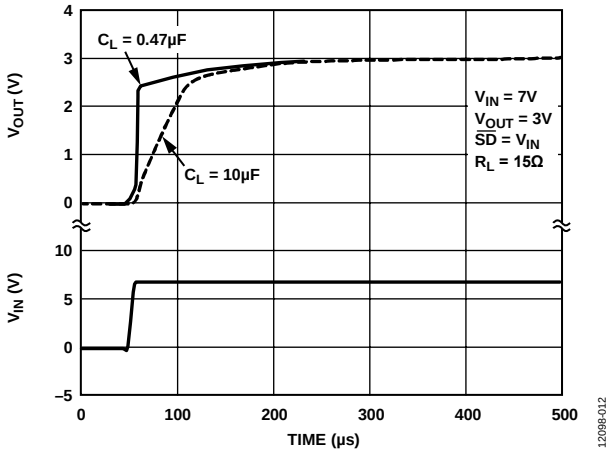

Figure 12. Power-Up Response

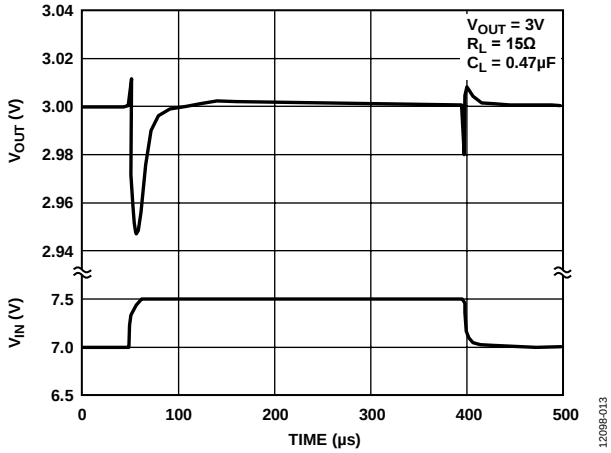

Figure 13. Line Transient Response, C_L = 0.47 µF

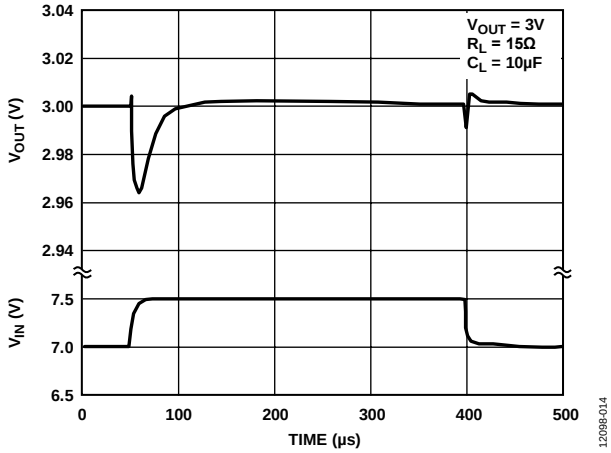

Figure 14. Line Transient Response, C_L = 10 µF

Figure 15. Load Transient Response, C_L = 0.47 µF

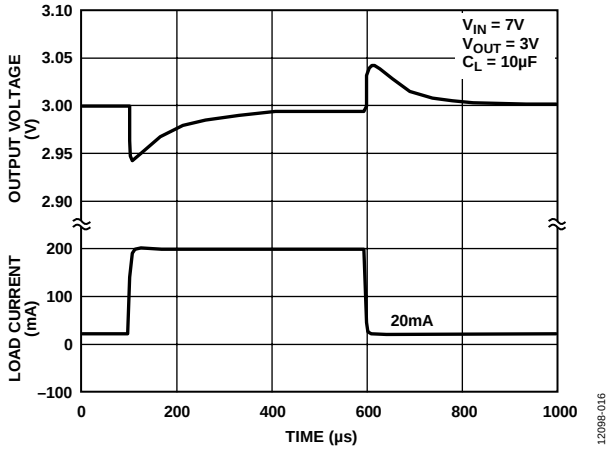

Figure 16. Load Transient Response, C_L = 10 µF

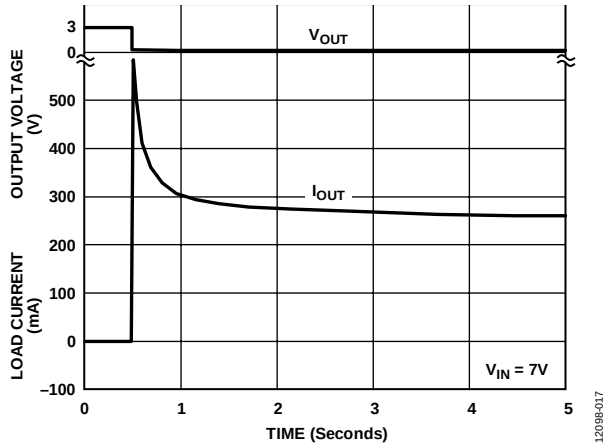

Figure 17. Short-Circuit Current

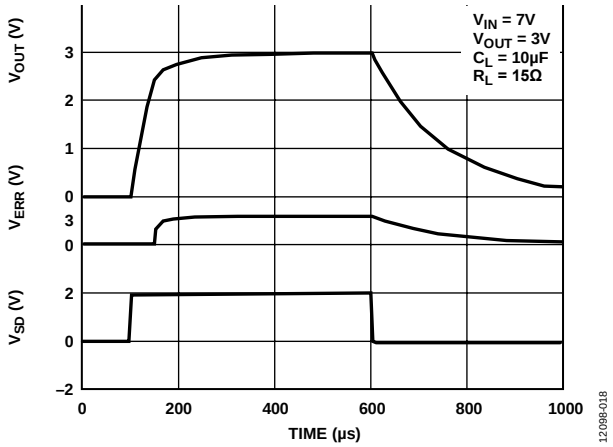

Figure 18. Turn On/Turn Off Response

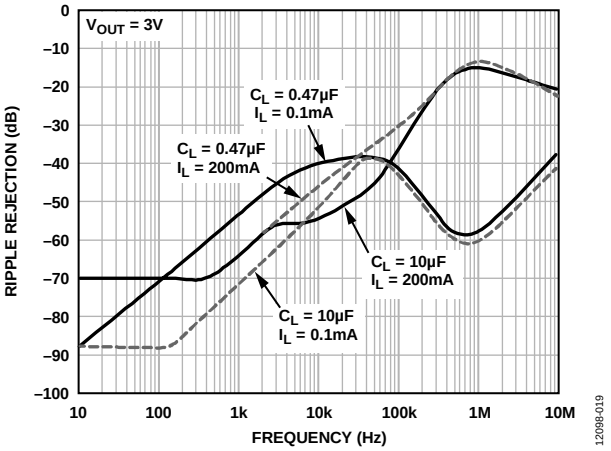

Figure 19. Power Supply Ripple Rejection vs. Frequency

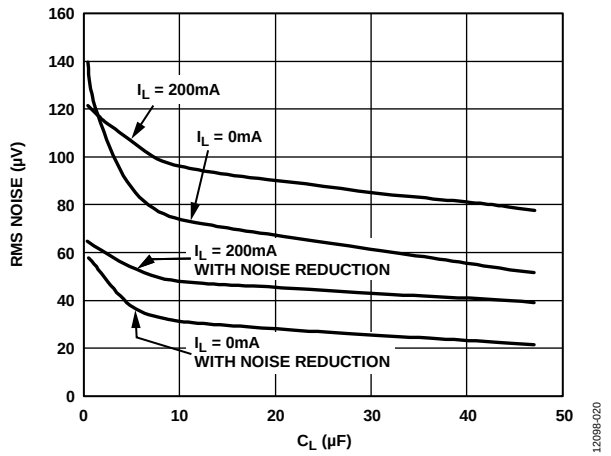

Figure 20. RMS Noise vs. C_L (10 Hz to100 kHz)

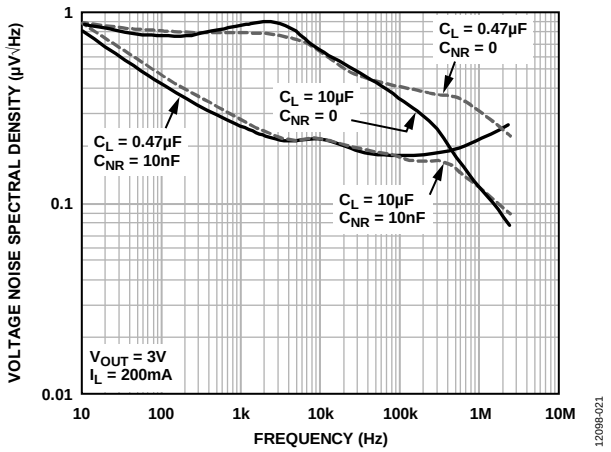

Figure 21. Output Noise Density

THEORY OF OPERATION

The anyCAP low dropout (LDO) ADP3330 uses a single control loop for regulation and reference functions. The output voltage is sensed by a resistive voltage divider consisting of R1 and R2, which is varied to provide the available output voltage options. Feedback is taken from this network by way of a series diode (D1) and a second resistor divider (R3 and R4) to the input of an amplifier.

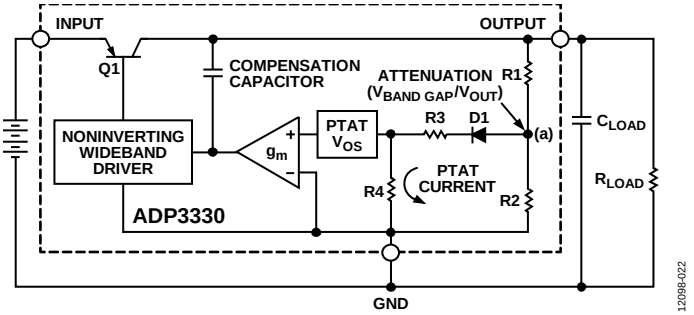

Figure 22. Functional Block Diagram

A very high gain error amplifier is used to control this loop. The amplifier is constructed in such a way that, at equilibrium, the amplifier produces a large, temperature proportional input offset voltage that is repeatable and very well controlled. The temperature proportional offset voltage is combined with the complementary diode voltage to form a virtual band gap voltage, implicit in the network, although it never appears explicitly in the circuit. Ultimately, this patented design makes it possible to control the loop with only one amplifier. This technique also improves the noise characteristics of the amplifier by providing more flexibility on the trade-off of noise sources that leads to a low noise design.

The R1, R2 divider is chosen in the same ratio as the band gap voltage to the output voltage. Although the R1, R2 resistor divider is loaded by the D1 diode and a second divider consisting of R3 and R4, the values are chosen to produce a temperature stable output. This unique arrangement specifically corrects the loading of the divider so that the typical error resulting from base current loading in conventional circuits is avoided.

The patented amplifier controls a new and unique noninverting driver that drives the pass transistor, Q1. The use of this noninverting driver enables the frequency compensation to include the load capacitor in a pole splitting arrangement to achieve reduced sensitivity to the value, type, and ESR of the load capacitance.

Most LDOs place strict requirements on the range of ESR values for the output capacitor because they are difficult to stabilize, due to the uncertainty of load capacitance and resistance. Moreover, the ESR value required to keep conventional LDOs stable changes depending on load and temperature. These ESR limitations make designing with LDOs more difficult because of their unclear specifications and extreme variations over temperature.

The ADP3330 anyCAP LDO overcomes these limitations. It can be used with virtually any good quality capacitor, with no constraint on the minimum ESR. The innovative design allows the circuit to be stable with just a small 0.47 µF capacitor on the output. Additional advantages of the pole splitting scheme include superior line noise rejection and very high regulator gain, which leads to excellent line and load regulation. An impressive ±1.4% accuracy is guaranteed over line, load and temperature.

Additional features of the circuit include current limit, thermal shutdown, and noise reduction. Compared to standard solutions that give warning after the output has lost regulation, the ADP3330 provides improved system performance by enabling the $\overline{\text{ERR}}$ pin to give warning just before the device loses regulation.

When the temperature of the chip rises to more than 165°C, the circuit activates a soft thermal shutdown, indicated by a signal low on the $\overline{\text{ERR}}$ pin, to reduce the current to a safe level.

APPLICATIONS INFORMATION

CAPACITOR SELECTION

Output Capacitors

As with any micropower device, output transient response is a function of the output capacitance. The ADP3330 is stable with a wide range of capacitor values, types, and ESR (anyCAP). A capacitor as low as 0.47 µF is all that is needed for stability; larger capacitors can be used if high output current surges are anticipated. The ADP3330 is stable with extremely low ESR capacitors (ESR ≈ 0), such as MLCC or OSCON. Note that the effective capacitance of some capacitor types may fall less than the minimum at cold temperature. Ensure that the capacitor provides more than 0.47 µF at minimum temperature.

Input Bypass Capacitor

An input bypass capacitor is not strictly required, but it is advisable in any application involving long input wires or high source impedance. Connecting a 0.47 µF capacitor from IN to GND reduces the sensitivity of the circuit to printed circuit board (PCB) layout. If a larger value output capacitor is used, a larger value input capacitor is also recommended.

NOISE REDUCTION

A noise reduction capacitor (C_{NR}) can be used to further reduce the noise by 6 dB to 10 dB (see Figure 23). Low leakage capacitors in the 10 pF to 500 pF range provide the best performance. Carefully connect to this node to avoid noise pickup from external sources because the noise reduction pin (NR) is internally connected to a high impedance node. The pad connected to this pin must be as small as possible and long PCB traces are not recommended.

When adding a noise reduction capacitor, use the following guidelines:

- Maintain a minimum load current of 1 mA when not in shutdown.
- For C_{NR} values greater than 500 pF, add a 100 kΩ series resistor (R_{NR}).

It is important to note that as C_{NR} increases, the turn on time is delayed. When C_{NR} values are greater than 1 nF, this delay may be in the order of several milliseconds.

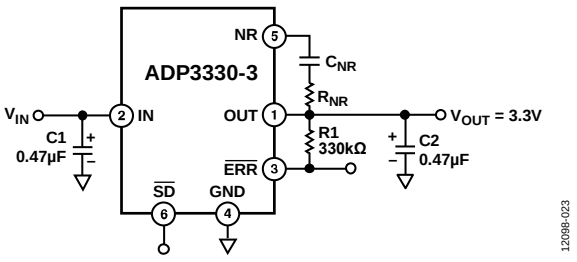

Figure 23. Noise Reduction Circuit

CHIP-ON-LEAD PACKAGE

The ADP3330 uses a Chip-on-Lead package design (protected by U.S. Patent 5929514 A) to ensure the best thermal performance in the 6-lead SOT-23 footprint. In a standard 6-lead SOT-23 package, the majority of the heat flows out of the ground pin. The Chip-on-Lead package uses an electrically isolated die attachment that allows all pins to contribute to the heat conduction. This technique reduces the thermal resistance to 190°C/W on a 2-layer board as compared to >230°C/W for a standard SOT-23 lead frame. Figure 24 and Figure 25 show the difference between the standard 6-lead SOT-23 and the Chip-on-Lead lead frames.

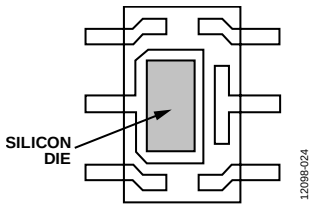

Figure 24. Normal 6-Lead SOT-23 Package

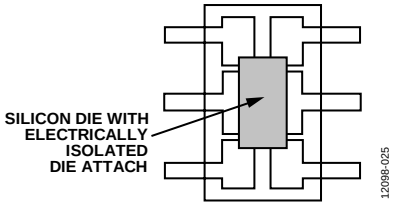

Figure 25. Thermally Enhanced, Chip-on-Lead Package

THERMAL OVERLOAD PROTECTION

The ADP3330 is protected against damage due to excessive power dissipation by its thermal overload protection circuit, which limits the die temperature to a maximum of 165°C. Under extreme conditions, (that is, high ambient temperature and power dissipation) where die temperature starts to rise more than 165°C, the output current decreases until the die temperature has dropped to a safe level. The output current is restored when the die temperature is reduced.

Current and thermal limit protections protect the device against accidental overload conditions. For normal operation, device power dissipation must be externally limited so that the junction temperatures do not exceed 125°C.

CALCULATING JUNCTION TEMPERATURE

Device power dissipation is calculated as follows:

$$P_D = (V_{IN} - V_{OUT}) I_{LOAD} + (V_{IN}) I_{GND}$$

where:
I_{LOAD} and I_{GND} are load current and ground current.
V_{IN} and V_{OUT} are input and output voltages, respectively.

Assuming I_{LOAD} = 200 mA, I_{GND} = 4 mA, V_{IN} = 4.2 V, and V_{OUT} = 3.0 V, the device power dissipation is the following:

$$P_D = (4.2 - 3.0)\ 200\ mA + 4.2\ (4\ mA) = 257\ mW$$

The proprietary package used in the ADP3330 has a thermal resistance of 165°C/W, significantly lower than the standard 6-lead SOT-23 package. Assuming a 4-layer board, the junction temperature rise above ambient temperature is approximately equal to

$$\Delta T_{JA} = 0.257\ W \times 165°C/W = 42.4°C$$

To limit the maximum junction temperature to 125°C, maximum allowable ambient temperature is

$$T_{A\ MAX} = 125°C - 42.4°C = 82.6°C$$

PRINTED CIRCUIT BOARD (PCB) LAYOUT CONSIDERATIONS

All packages rely on the traces of the PCB to conduct heat away from the package.

In standard packages, the dominant component of the heat resistance path is the plastic between the die attach pad and the individual leads. In typical thermally enhanced packages, one or more of the leads are fused to the die attach pad, significantly decreasing this component. To make the improvement meaningful, however, a significant copper area on the PCB must be attached to these fused pins.

The patented chip-on-lead frame design of the ADP3330 uniformly minimizes the value of the dominant portion of the thermal resistance. It ensures that heat is conducted away by all of the package pins and yields a very low 165°C/W thermal resistance for the 6-lead SOT-23 package. Low thermal resistance is achieved without any special board layout requirements, just the normal traces connected to the leads, and yields a 17% improvement in heat dissipation capability as compared to a standard 6-lead SOT-23 package. The thermal resistance can be decreased by approximately an additional 10% by attaching a few square cm of copper area to the V_{IN} pin of the ADP3330 package.

It is not recommended to use solder mask or silkscreen on the PCB traces adjacent to the pins of the ADP3330 because it increases the junction to ambient thermal resistance of the package.

ERROR FLAG DROPOUT DETECTOR

The ADP3330 maintains its output voltage over a wide range of load, input voltage, and temperature conditions. If the output is about to lose regulation by reducing the supply voltage less than the combined regulated output and dropout voltages, the $\overline{ERR}$ flag is activated. The $\overline{ERR}$ output is an open collector that is driven low.

When the $\overline{ERR}$ output is set, the hysteresis of the $\overline{ERR}$ flag keeps the output low until a small margin of the operating range is restored either by raising the supply voltage or reducing the load.

SHUTDOWN MODE

Applying a TTL high signal to the shutdown ($\overline{SD}$) pin, or tying the $\overline{SD}$ pin to the input pin, turns the output on. Pulling the $\overline{SD}$ pin down to 0.4 V or below, or tying the $\overline{SD}$ pin to ground, turns the output off (we do not do all caps for emphasis). In shutdown mode, the ground current is reduced to much less than 1 µA.

LOW POWER, LOW DROPOUT APPLICATIONS

The ADP3330 is well suited for applications such as cell phone handsets that require low ground current and low dropout voltage features. The ADP3330 typically draws 34 µA under light load situations (that is, load current = 100 µA), which results in low power consumption when the cell phone is in standby mode.

Figure 26 shows an application in which the ADP3330 is used in a handset to provide 2.75 V nominal output voltage. The cell phone is powered from a 3 cell NiCd or 1 cell Li-Ion battery. The ADP3330 guarantees an accuracy of 1.4%, even when the input/output differential is merely 250 mV (worst case). Therefore, the voltage output is regulated and within specification even when the battery voltage has reached its end of discharge voltage of 3 V. The output voltage never falls less than 2.7 V, even under worst case load and temperature conditions. The low dropout feature coupled with the high accuracy of the ADP3330 ensures that the system is reliably powered until the end of the life of the battery, which results in increased system talk time.

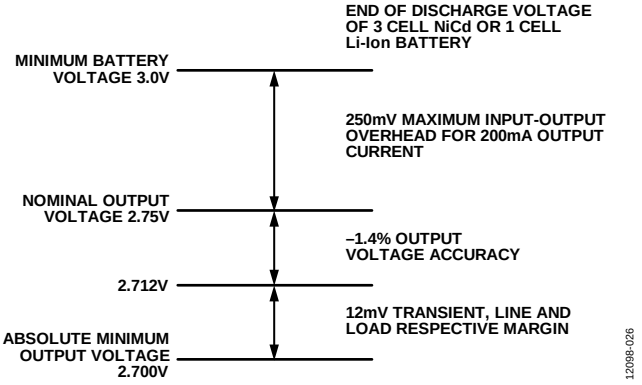

Figure 26. LDO Budgeting for a 3 Cell NiCd/1 Cell Li-Ion Supply

APPLICATION CIRCUITS

CROSSOVER SWITCH

The circuit in Figure 27 shows how two ADP3330s can be used to form a mixed supply voltage system. The output switches between two different levels selected by an external digital input. Output voltages can be any combination of voltages that are included in the Ordering Guide.

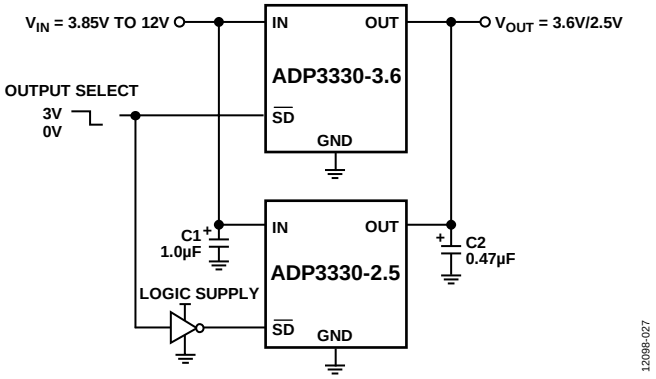

Figure 27. Crossover Switch

HIGHER OUTPUT CURRENT

The ADP3330 can source up to 200 mA at room temperature without any heat-sink, or pass transistor. If higher current is needed, an appropriate pass transistor can be used, as in Figure 28, to increase the output current to 1 A.

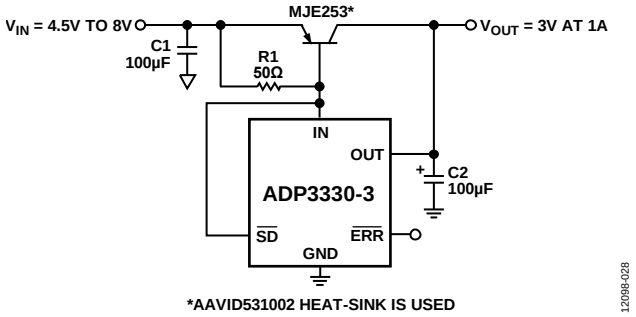

Figure 28. High Output Current Linear Regulator

OUTLINE DIMENSIONS

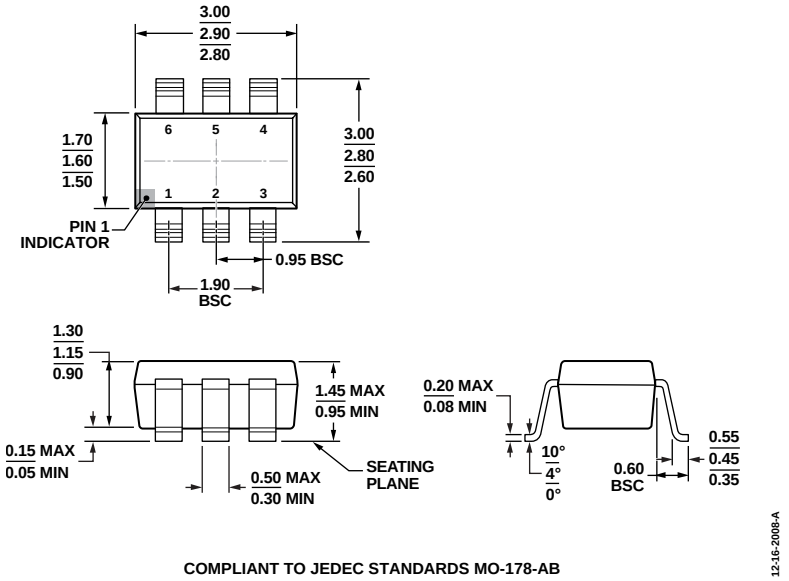

Figure 29. 6-Lead Small Outline Transistor Package [SOT-23]
RJ-6
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Voltage Output (V)	Package Description	Package Option[2]	Branding
ADP3330ARTZ-2.5-R7	−40°C to +85°C	2.5	6-Lead SOT-23	RJ-6	L1B
ADP3330ARTZ-2.75R7	−40°C to +85°C	2.75	6-Lead SOT-23	RJ-6	L2B
ADP3330ARTZ-2.75RL	−40°C to +85°C	2.75	6-Lead SOT-23	RJ-6	L2B
ADP3330ARTZ-2.85R7	−40°C to +85°C	2.85	6-Lead SOT-23	RJ-6	L3B
ADP3330ARTZ-3-RL7	−40°C to +85°C	3.0	6-Lead SOT-23	RJ-6	L4B
ADP3330ARTZ3.3-RL7	−40°C to +85°C	3.3	6-Lead SOT-23	RJ-6	L5B
ADP3330ARTZ-3.6-R7	−40°C to +85°C	3.6	6-Lead SOT-23	RJ-6	L6B
ADP3330ARTZ-5-RL7	−40°C to +85°C	5.0	6-Lead SOT-23	RJ-6	L8B

[1] Z = RoHS Compliant Part.
[2] Contact the factory for the availability of other output voltage options.

NOTES

NOTES

D12098-0-5/15(C)

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View ADP3330ART-3.6-RL on WIN SOURCE
- Analog Devices Inc. Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management