



**THE DATASHEET OF  
AON4407L**



**AON4407L**
**P-Channel Enhancement Mode Field Effect Transistor**
**General Description**

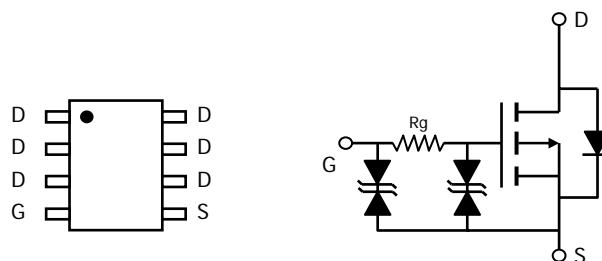
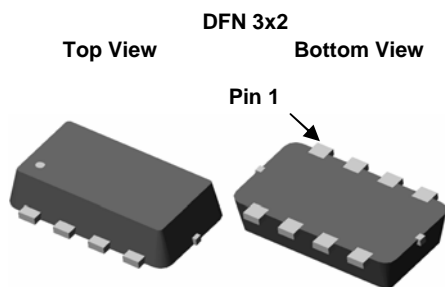
The AON4407L uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 1.8V. This device is suitable for use as a load switch.

- RoHS Compliant
- Halogen Free

**Features**

$V_{DS} (V) = -12V$   
 $I_D = -9 A \quad (V_{GS} = -4.5V)$   
 $R_{DS(ON)} < 20m\Omega \quad (V_{GS} = -4.5V)$   
 $R_{DS(ON)} < 25m\Omega \quad (V_{GS} = -2.5V)$   
 $R_{DS(ON)} < 31m\Omega \quad (V_{GS} = -1.8V)$

**ESD Protected!**


**Absolute Maximum Ratings  $T_A=25^\circ C$  unless otherwise noted**

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	-12	V
Gate-Source Voltage	$V_{GS}$	$\pm 8$	V
Continuous Drain Current	$I_D$	$T_A=25^\circ C$	A
		$T_A=70^\circ C$	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	-60	
Power Dissipation <sup>B</sup>	$P_D$	$T_A=25^\circ C$	W
		$T_A=70^\circ C$	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ C$

**Thermal Characteristics**

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	42	50	$^\circ C/W$
Maximum Junction-to-Ambient <sup>A,D</sup>		Steady State	74	90
Maximum Junction-to-Lead	$R_{\theta JL}$	25	30	$^\circ C/W$

Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$I_D=-250\mu\text{A}$ , $V_{GS}=0\text{V}$	-12			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=-12\text{V}$ , $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			-1 -5	$\mu\text{A}$
$I_{GSS}$	Gate-Body leakage current	$V_{DS}=0\text{V}$ , $V_{GS}=\pm 8\text{V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$ , $I_D=-250\mu\text{A}$	-0.35	-0.5	-0.85	V
$I_{D(ON)}$	On state drain current	$V_{GS}=-4.5\text{V}$ , $V_{DS}=-5\text{V}$	-60			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=-4.5\text{V}$ , $I_D=-9\text{A}$ $T_J=125^\circ\text{C}$		16.5	20	m $\Omega$
				22	26	
		$V_{GS}=-2.5\text{V}$ , $I_D=-8.5\text{A}$		20	25	m $\Omega$
		$V_{GS}=-1.8\text{V}$ , $I_D=-7.5\text{A}$		24	31	m $\Omega$
	$V_{GS}=-1.5\text{V}$ , $I_D=-7\text{A}$		29	38	m $\Omega$	
$g_{FS}$	Forward Transconductance	$V_{DS}=-5\text{V}$ , $I_D=-9\text{A}$		45		S
$V_{SD}$	Diode Forward Voltage	$I_S=-1\text{A}$ , $V_{GS}=0\text{V}$		-0.53	-1	V
$I_S$	Maximum Body-Diode Continuous Current				-2.5	A
<b>DYNAMIC PARAMETERS</b>						
$C_{ISS}$	Input Capacitance	$V_{GS}=0\text{V}$ , $V_{DS}=-6\text{V}$ , $f=1\text{MHz}$		1740	2100	pF
$C_{OSS}$	Output Capacitance			334		
$C_{RSS}$	Reverse Transfer Capacitance			200		
$R_g$	Gate resistance	$V_{GS}=0\text{V}$ , $V_{DS}=0\text{V}$ , $f=1\text{MHz}$		1.3	1.7	k $\Omega$
<b>SWITCHING PARAMETERS</b>						
$Q_g$	Total Gate Charge	$V_{GS}=-4.5\text{V}$ , $V_{DS}=-6\text{V}$ , $I_D=-9\text{A}$		19	23	nC
$Q_{gs}$	Gate Source Charge			4.5		
$Q_{gd}$	Gate Drain Charge			5.3		
$t_{D(on)}$	Turn-On Delay Time	$V_{GS}=-4.5\text{V}$ , $V_{DS}=-6\text{V}$ , $R_L=0.67\Omega$ , $R_{GEN}=3\Omega$		240		ns
$t_r$	Turn-On Rise Time			580		
$t_{D(off)}$	Turn-Off Delay Time			7		
$t_f$	Turn-Off Fall Time			4.2		
$t_{rr}$	Body Diode Reverse Recovery Time	$I_F=-9\text{A}$ , $dI/dt=100\text{A}/\mu\text{s}$		22	27	ns
$Q_{rr}$	Body Diode Reverse Recovery Charge	$I_F=-9\text{A}$ , $dI/dt=100\text{A}/\mu\text{s}$		17		nC

A. The value of  $R_{\theta JA}$  is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The value in any given application depends on the user's specific board design.

B. The power dissipation  $P_D$  is based on  $T_{J(MAX)}=150^\circ\text{C}$ , using  $\leq 10\text{s}$  junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)}=150^\circ\text{C}$ . Ratings are based on low frequency and duty cycles to keep initial  $T_J=25^\circ\text{C}$ .

D. The  $R_{\theta JA}$  is the sum of the thermal impedance from junction to lead  $R_{\theta JL}$  and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using  $<300\mu\text{s}$  pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, assuming a maximum junction temperature of  $T_{J(MAX)}=150^\circ\text{C}$ . The SOA curve provides a single pulse rating.

Rev 0: Aug 2008

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

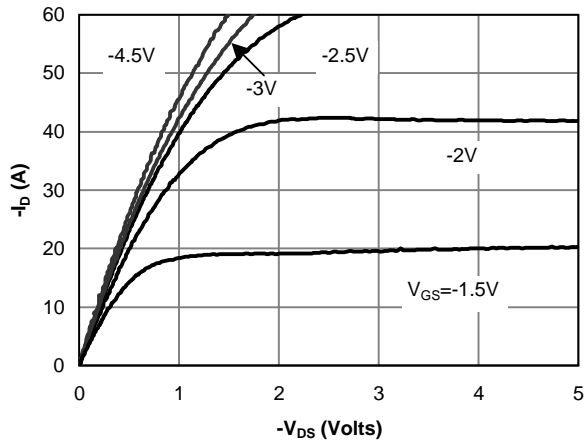


Figure 1: On-Region Characteristics(Note E)

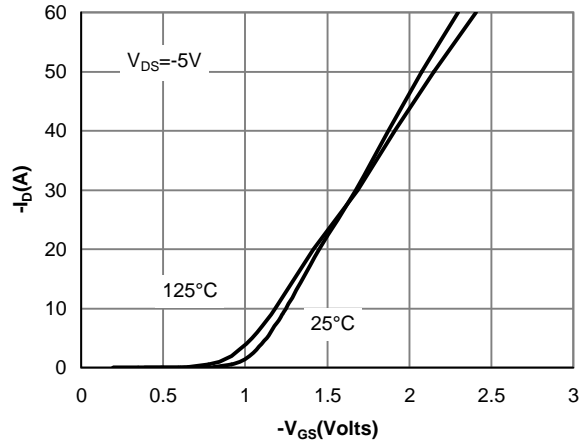


Figure 2: Transfer Characteristics(Note E)

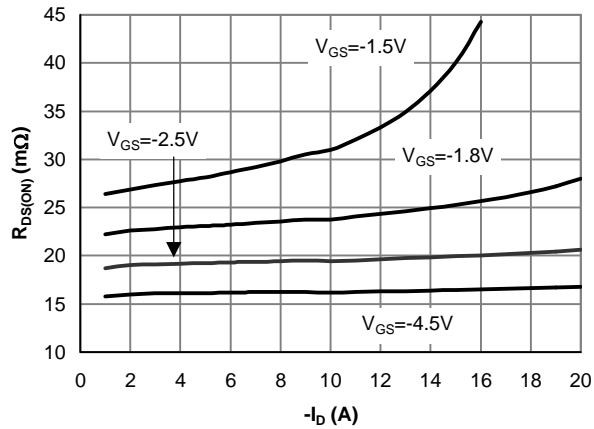


Figure 3: On-Resistance vs. Drain Current and Gate Voltage(Note E)

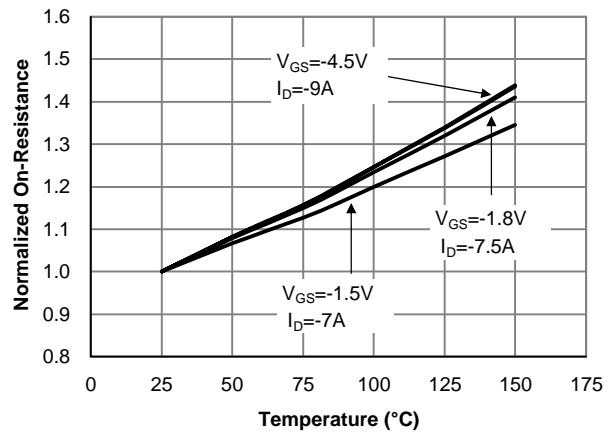


Figure 4: On-Resistance vs. Junction Temperature(Note E)

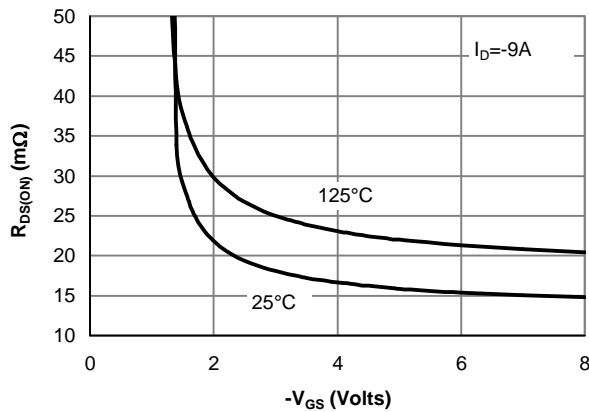


Figure 5: On-Resistance vs. Gate-Source Voltage(Note E)

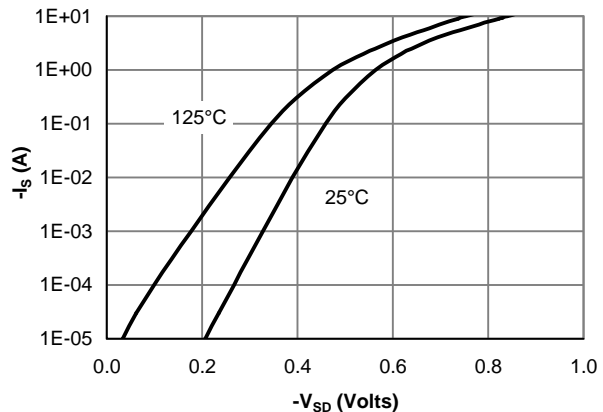


Figure 6: Body-Diode Characteristics(Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

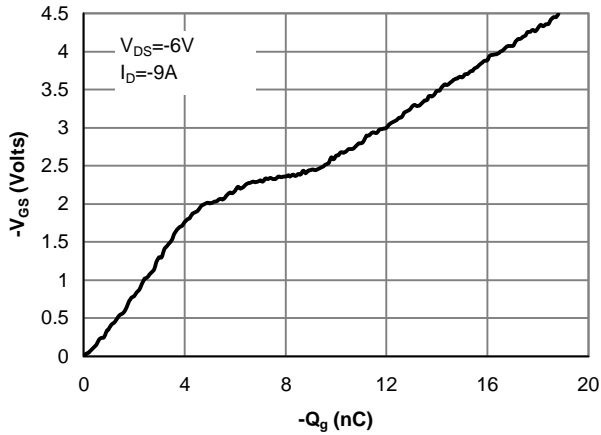


Figure 7: Gate-Charge Characteristics

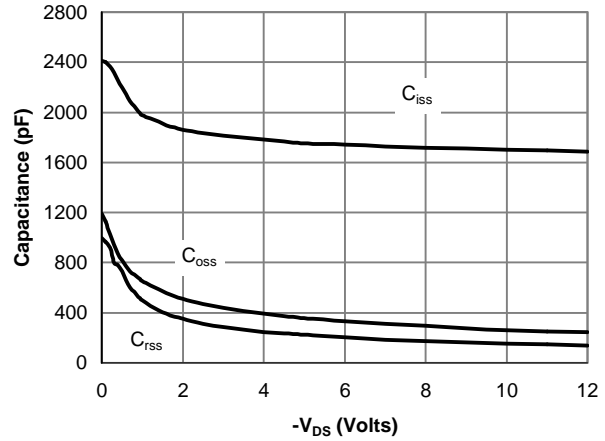


Figure 8: Capacitance Characteristics

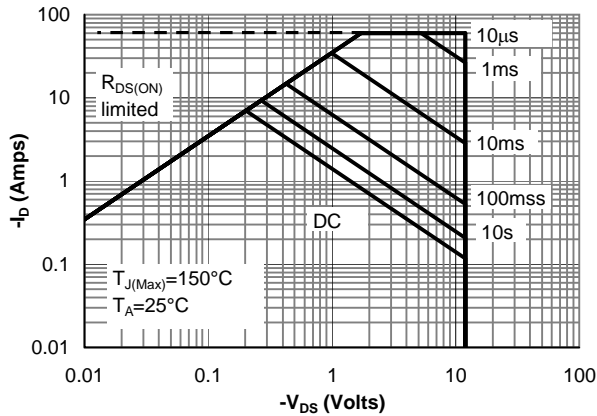


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

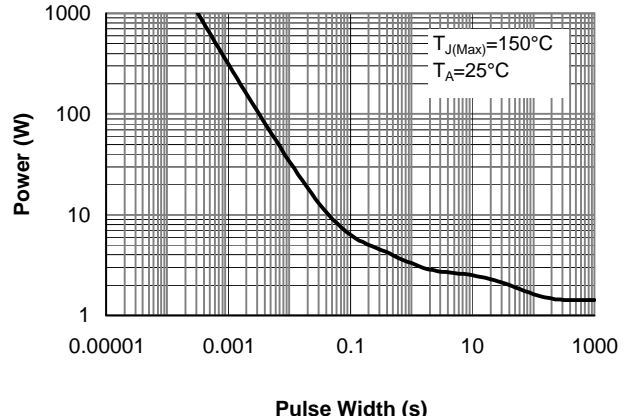


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

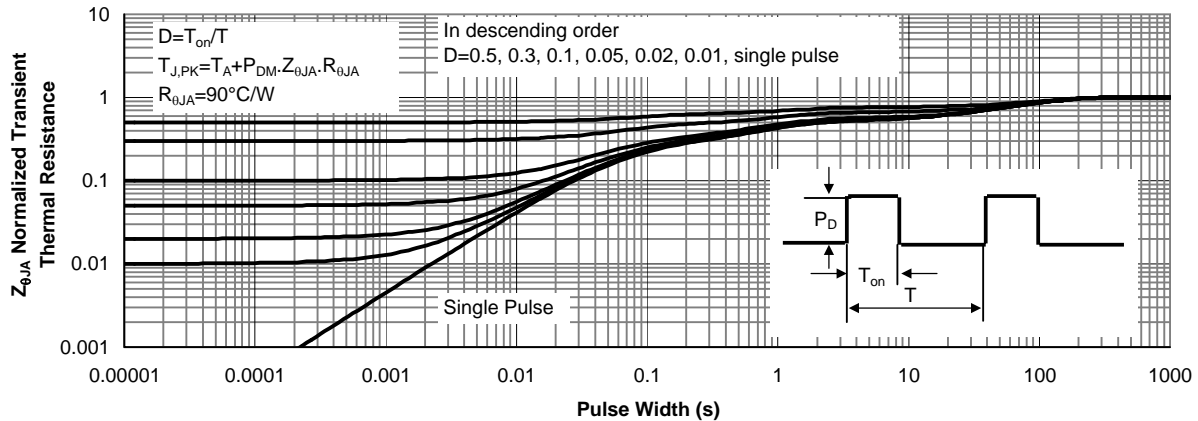
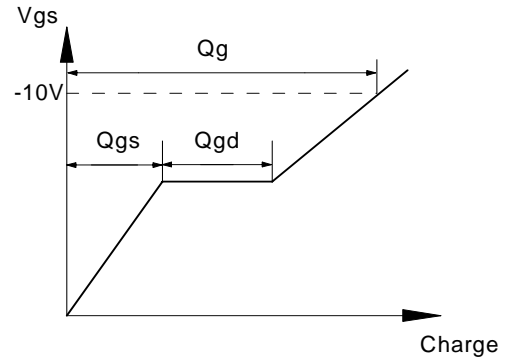
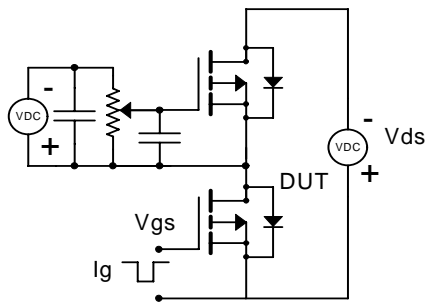
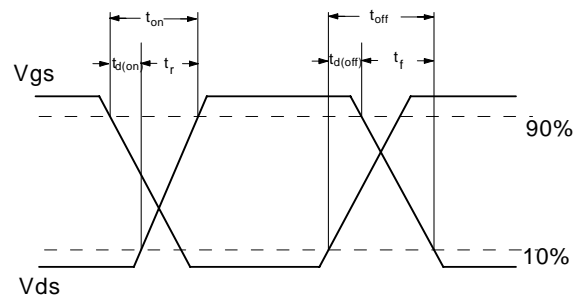
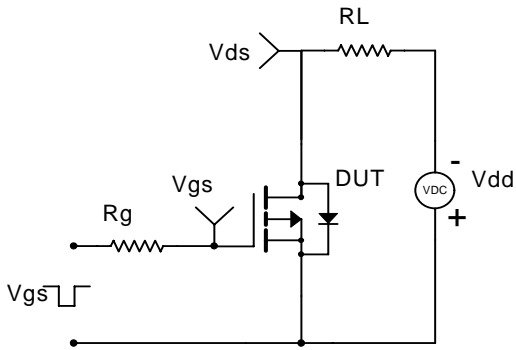


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

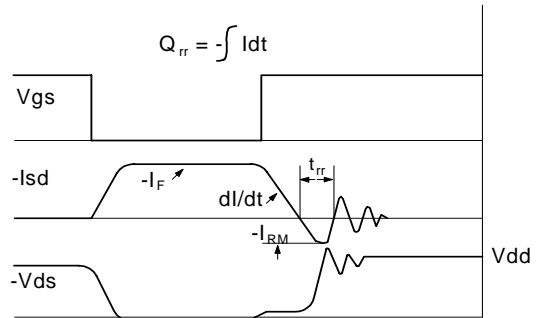
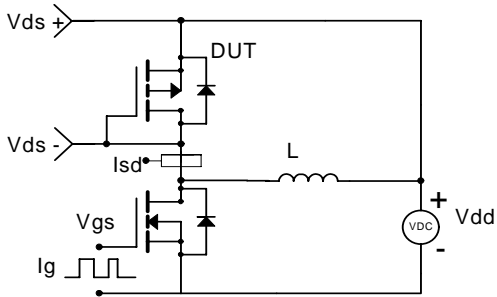
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



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