THE DATASHEET OF

AS1918V-T

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AS1916 - AS1918

Microprocessor Supervisory Circuits with Manual Reset and Watchdog

1 General Description

The AS1916 - AS1918 microprocessor supervisory circuits were designed to generate a reset when the monitored supply voltage falls below a factory-trimmed threshold. The reset remains asserted for a minimum timeout period after the supply voltage stabilizes.

Guaranteed to be in the correct state for VCC higher than +1.0V, these devices are ideal for portable and battery-powered systems with strict monitoring requirements.

The devices feature factory-trimmed thresholds to monitor a supply voltage between 1.8 and 3.6V.

The devices are available with the reset output types listed in Table 1.

Table 1. Standard Products

Model	Reset Output Type
AS1916	Active-Low Push/Pull
AS1917	Active-High Push/Pull
AS1918	Active-Low Open-Drain

The AS1916 - AS1918 include a manual-reset input for systems that never fully power down the microprocessor.

Additionally, these devices feature a watchdog timer to help ensure that the processor is operating within proper code boundaries.

The AS1916 - AS1918 are available in a 5-pin SOT23 package.

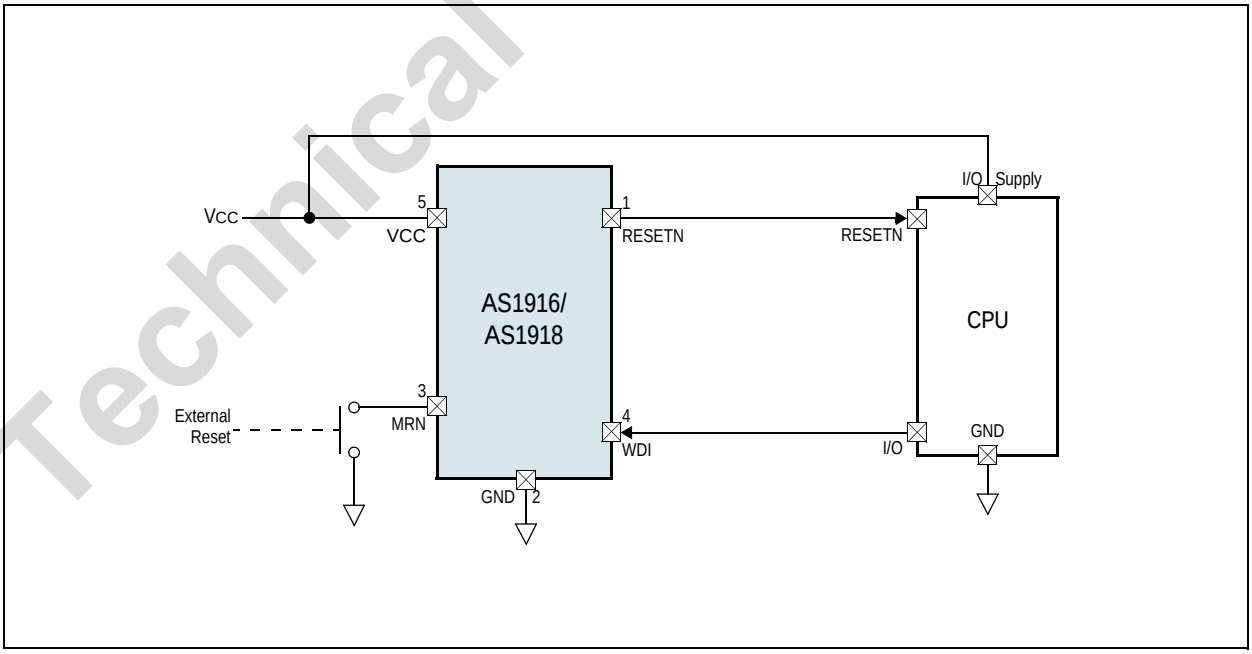
2 Key Features

- VCC Supervisory Range: +1.8 to +3.6V
- Guaranteed Reset Valid Down to VCC = +1.0V
- Reset Timeout Delay: 215ms
- Manual Reset Input
- Three Reset Output Types
  - Active-Low Push/Pull (AS1916)
  - Active-High Push/Pull (AS1917)
  - Active-Low Open-Drain (AS1918)
- Watchdog Timeout Period: 1.5s
- Immune to Fast Negative VCC Transients
- External Components Not Required
- Operating Temperature Range: -40 to +125°C
- 5-pin SOT23 Package

3 Applications

The devices are ideal for portable and battery-powered systems, embedded controllers, intelligent instruments, automotive systems, and critical CPU monitoring applications.

Figure 1. Typical Application Diagram



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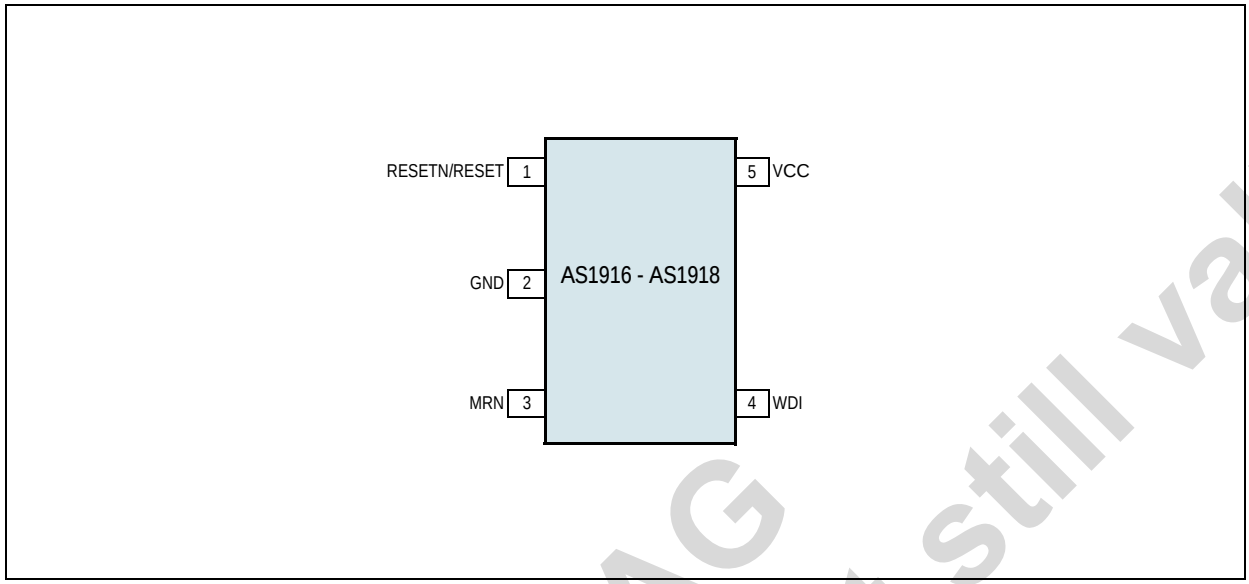
4 Pin Assignments

Figure 2. Pin Assignments (Top View)



4.1 Pin Descriptions

Table 2. Pin Descriptions

Pin Number	Pin Name	Description
1	RESETN	**Active-Low Reset Output** (AS1916, AS1918). The RESETN signal toggles from high to low when V_{CC}, or MRN is pulled low, or the watchdog triggers a reset. This output signal remains low for the reset timeout period after all supervised voltages exceed their reset threshold, or MRN goes low to high, or the watchdog triggers a reset.
	RESET	**Active-High Reset Output** (AS1917). The RESET signal toggles from low to high when V_{CC}, or MRN is pulled low, or the watchdog triggers a reset. This output signal remains high for the reset timeout period (see t_{RP} on page 4) after all supervised voltages exceed their reset threshold, or MRN goes low to high, or the watchdog triggers a reset.
2	GND	**Ground**
3	MRN	**Active-Low Manual Reset Input**. Pulling this pin low asserts a reset. This pin is connected to the internal 50kΩ pullup to V_{CC}. This reset remains active as long as MRN is low and for the reset timeout period (see t_{RP} on page 4) after MRN goes high. **Note:** If the manual reset feature is not used, this pin should be unconnected or connected to V_{CC}.
4	WDI	**Watchdog Input**. If WDI remains high or low for longer than the watchdog timeout period (see t_{WD} on page 5), the internal watchdog timer period expires and a reset is triggered for the reset timeout period (see t_{RP} on page 4). The internal watchdog timer clears whenever a reset is a asserted or when WDI senses a rising or falling edge. **Note:** To disable the watchdog feature, this pin must be unconnected or connected to a tri-state buffer output. WDI must be low or unconnected (tristate) during the reset timeout period tRP, (see Figure 11 on page 8).
5	VCC	**Supervised Voltage Input**. This pin serves as the supervised supply voltage input.

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5 Absolute Maximum Ratings

Stresses beyond those listed in Table 3 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device rel11iability.

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Electrical Parameters				
VCC to GND	-0.3	+5.0	V	
Open-Drain RESETN	-0.3	+7.0	V	
Push/Pull RESET, RESETN	-0.3	VCC + 0.3	V	
MRN, WDI to GND	-0.3	VCC + 0.3	V	
Input Current (VCC)		20	mA	
Output Current (RESET, RESETN)		20	mA	
Continuous Power Dissipation				
Continuous Power Dissipation (TAMB = +70ºC)		696	mW	Derate 8.7mW/ºC above +70ºC
Temperature Ranges and Storage Conditions				
Junction Temperature		+150	ºC	
Storage Temperature Range	-55	+150	ºC	
Package Body Temperature		+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).
Humidity non-condensing	5	85	%	
Moisture Sensitive Level	1			Represents a max. floor life time of unlimited

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6 Electrical Characteristics

VCC = +2.7 to +3.6V for AS19xx-T/S/R, VCC = +2.1 to +2.75V for AS19xx- Z/Y, VCC = +1.53 to +2.0V for AS19xx-W/V; Typical values @ TAMB = +25ºC (unless otherwise specified).

Table 4. Electrical Characteristics

Symbol	Parameter[1]	Conditions		Min	Typ	Max	Units
TAMB	Operating Temperature Range			-40		+125	ºC
VCC	Operating Voltage Range	TAMB = 0 to +85ºC		1.0		3.6	V
		TAMB = -40 to +125ºC		1.2		3.6	
ICC	VCC Supply Current (MRN and WDI Not Connected)	VCC = +3.6V, No Load, TAMB = -40ºC to +85ºC			5.5	12	µA
		VCC = +3.6V, No Load, TAMB = -40 to +125ºC				19	
VTH	VCC Reset Threshold (VCC Falling)	TAMB = -40 to +85ºC	AS19xx-T	2.994	3.08	3.154	V
		TAMB = -40 to +125ºC		2.972		3.179	
		TAMB = -40 to +85ºC	AS19xx-S	2.848	2.93	3.000	
		TAMB = -40 to +125ºC		2.827		3.024	
		TAMB = -40 to +85ºC	AS19xx-R	2.556	2.63	2.693	
		TAMB = -40 to +125ºC		2.538		2.714	
		TAMB = -40 to +85ºC	AS19xx-Z	2.255	2.32	2.376	
		TAMB = -40 to +125ºC		2.239		2.394	
		TAMB = -40 to +85ºC	AS19xx-Y	2.129	2.19	2.243	
		TAMB = -40 to +125ºC		2.113		2.260	
		TAMB = -40 to +85ºC	AS19xx-W	1.623	1.67	1.710	
		TAMB = -40 to +125ºC		1.612		1.723	
		TAMB = -40 to +85ºC	AS19xx-V	1.536	1.58	1.618	
		TAMB = -40 to +125ºC		1.525		1.631	
	Reset Threshold Temperature Coefficient				60		ppm/ºC
	Reset Threshold Hysteresis				8 x VTH		mV
tRD	VCC to Reset Output Delay	VCC = VTH to (VTH - 100mV)			55		µs
tRP	Reset Timeout Period	TAMB = -40 to +85ºC		140	215	280	ms
		TAMB = -40 to +125ºC		100		320	
VOL	RESETN Output Low (Push/Pull or Open-Drain)	VCC ≥ 1.0V, ISINK = 50µA, Reset Asserted, TAMB = 0 to +85ºC				0.3	V
		VCC ≥ 1.2V, ISINK = 100µA, Reset Asserted				0.3	
		VCC ≥ 2.55V, ISINK = 1.2mA, Reset Asserted				0.3	
		VCC ≥ 3.3V, ISINK = 3.2mA, Reset Asserted				0.4	
VOH	RESETN Output High (Push/Pull Only)	VCC ≥ 1.8V, ISOURCE = 200µA, Reset Not Asserted		0.8 x VCC			V
		VCC ≥ 3.15V, ISOURCE = 500µA, Reset Not Asserted		0.8 x VCC			
		VCC ≥ 3.3V, ISOURCE = 800µA, Reset Not Asserted		0.8 x VCC			
ILKG	Open-Drain RESETN Output Leakage Current	RESETN Not Asserted				1.0	µA
		TAMB = +25ºC				0.2	

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Table 4. Electrical Characteristics

Symbol	Parameter[1]	Conditions	Min	Typ	Max	Units
V_{OH}	RESET Output High (Push/Pull Only)	$V_{CC} \geq 1.0V$, $I_{SOURCE} = 1\mu A$, Reset Asserted, T_{AMB} = 0 to +85ºC	0.8 x V_{CC}			V
		$V_{CC} \geq 1.50V$, $I_{SOURCE} = 100\mu A$, Reset Asserted	0.8 x V_{CC}			
		$V_{CC} \geq 2.55V$, $I_{SOURCE} = 500\mu A$, Reset Asserted	0.8 x V_{CC}			
		$V_{CC} \geq 3.3V$, $I_{SOURCE} = 800\mu A$, Reset Asserted	0.8 x V_{CC}			
V_{OL}	RESET Output Low (Push/Pull Only)	$V_{CC} \geq 1.8V$, $I_{SINK} = 500\mu A$, Reset Asserted			0.3	V
		$V_{CC} \geq 3.15V$, $I_{SINK} = 1.2mA$, Reset Asserted			0.3	
		$V_{CC} \geq 3.3V$, $I_{SINK} = 3.2mA$, Reset Asserted			0.4	
Manual Reset Input						
V_{IL}	MRN Input voltage				0.3 x V_{CC}	V
V_{IH}			0.7 x V_{CC}			
	MRN Minimum Input Pulse		1			µs
	MRN Transient Rejection			90		ns
	MRN to Reset Delay			130		ns
	MRN Pullup Resistance		25	50	75	kΩ
Watchdog Input						
t_{WD}	Watchdog Timeout Period	T_{AMB} = -40 to +85ºC	1.12	1.5	2.4	s
		T_{AMB} = -40 to +125ºC	0.80		2.60	
t_{WDI}	WDI Pulse Width [2]		20			ns
V_{IL}	WDI Input Voltage				0.3 x V_{CC}	V
V_{IH}			0.7 x V_{CC}			
I_{WDI}	WDI Input Current	WDI = V_{CC}, Time Average		80	160	µA
		WDI = 0, Time Average	-20	-11		

1. Over-temperature limits are guaranteed by design and not production tested. Devices tested at +25ºC.
2. Guaranteed by design and not production tested.

Note: All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

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7 Typical Operating Characteristics

TAMB = +25ºC (unless otherwise specified).

Figure 3. Normalized Reset Threshold Delay vs. Temperature Active-Low (Typ)

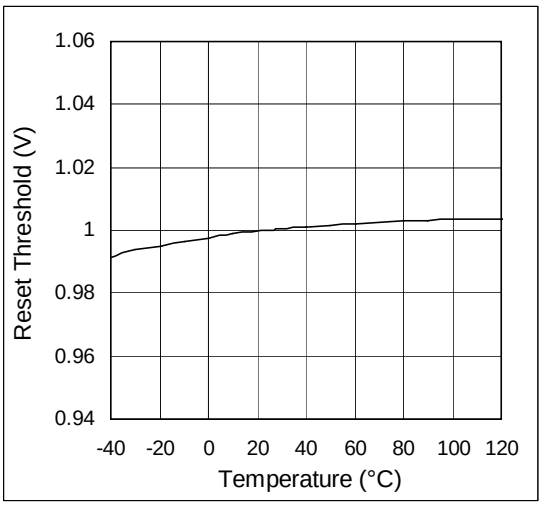


Figure 4. VOUT vs. VCC, VTH = 1.58V

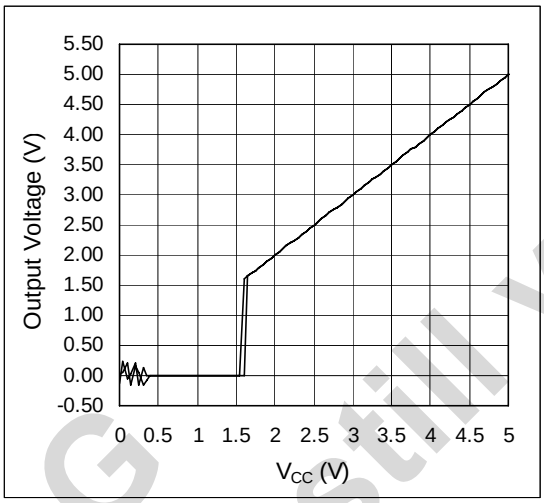


Figure 5. Reset Timeout Period vs. Temperature

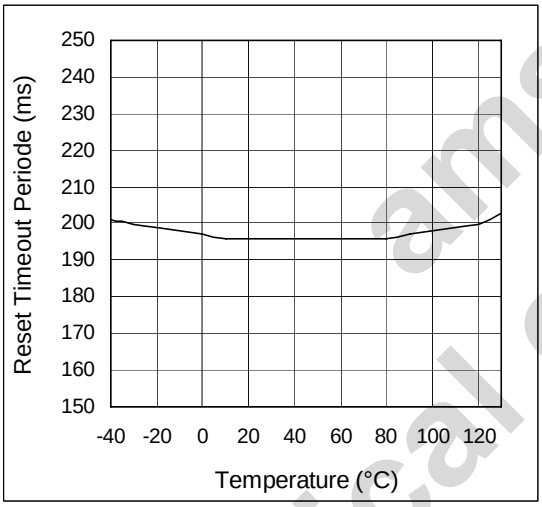


Figure 6. Supply Current vs. Temperature

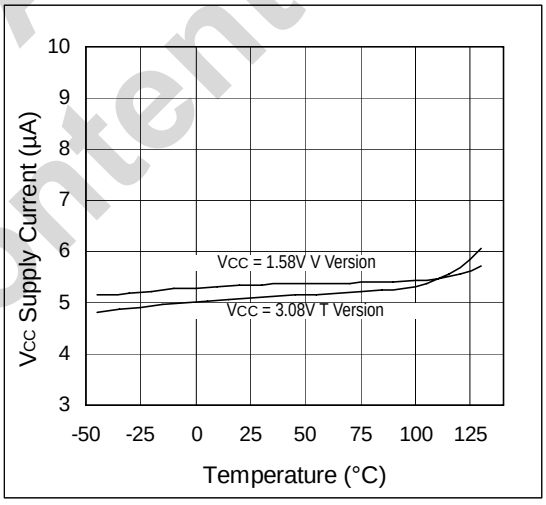


Figure 7. VOH vs. ISOURCE; VCC = 3.2V

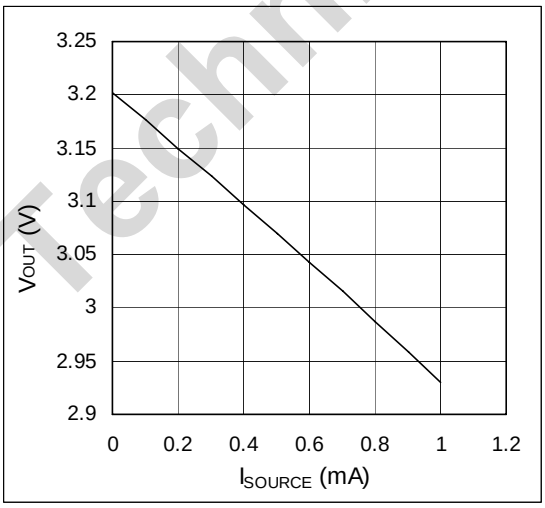
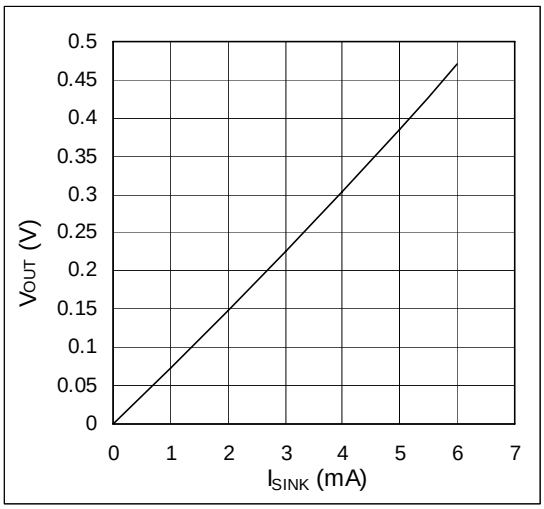


Figure 8. VOL vs. ISINK; VCC = 3.2V



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8 Detailed Description

The AS1916 - AS1918 supervisory circuits were designed to generate a reset when the monitored supply voltage falls below its factory-trimmed trip threshold (see V_{TH} on page 4), and to maintain the reset for a minimum timeout period (see t_{RP} on page 4) after the supply has stabilized.

The integrated watchdog timer (see Watchdog Input on page 8) helps mitigate against bad programming code or clock signals, and/or poor peripheral response.

The active-low manual reset input (see Manual Reset Input on page 8) allows for an externally activated system reset.

8.1 RESET/RESETN

Whenever the monitored supply voltage falls below its reset threshold, the RESET output asserts low or the RESETN output asserts high. Once the monitored voltage has stabilized, an internal timer keeps the reset asserted for the reset timeout period (t_{RP}). After the t_{RP} period, the RESET/RESETN output returns to its original state (see Figure 10).

Figure 9. Functional Diagram of V_{CC} Supervisory Application

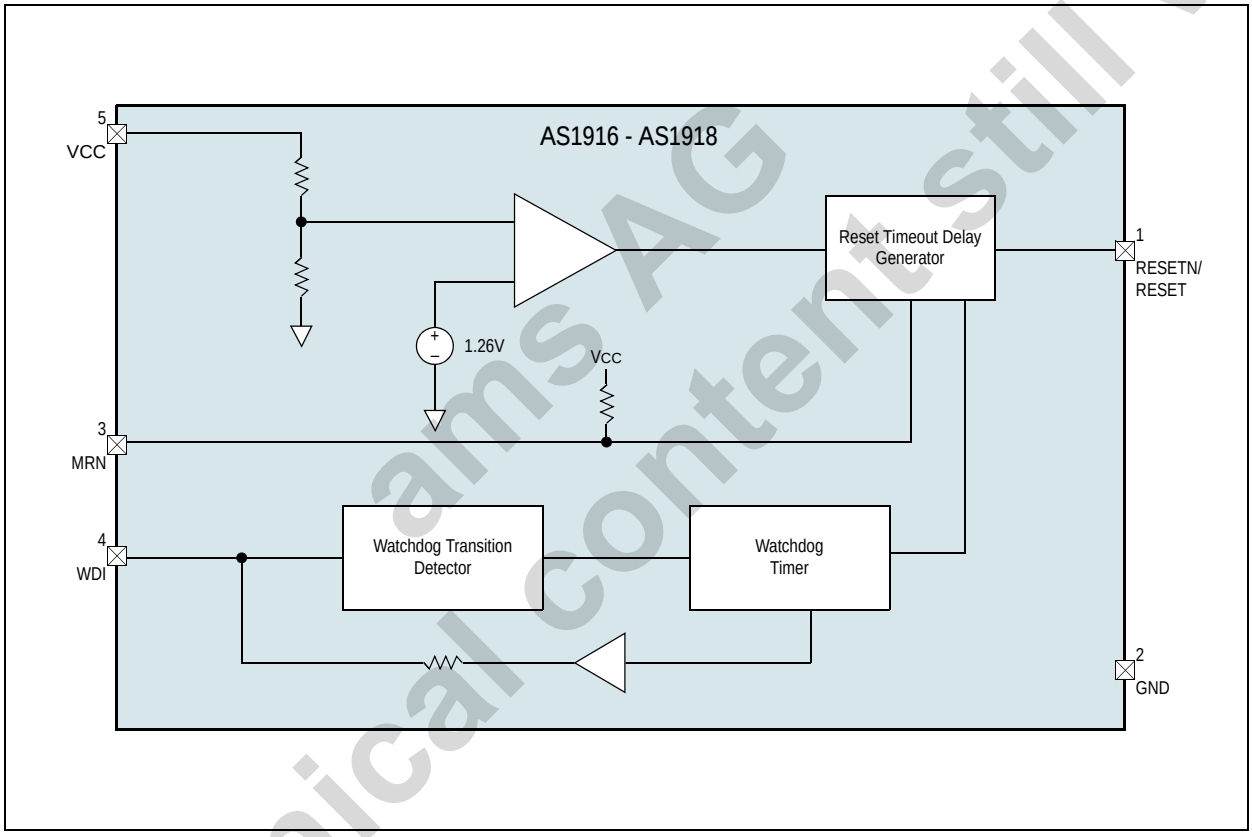
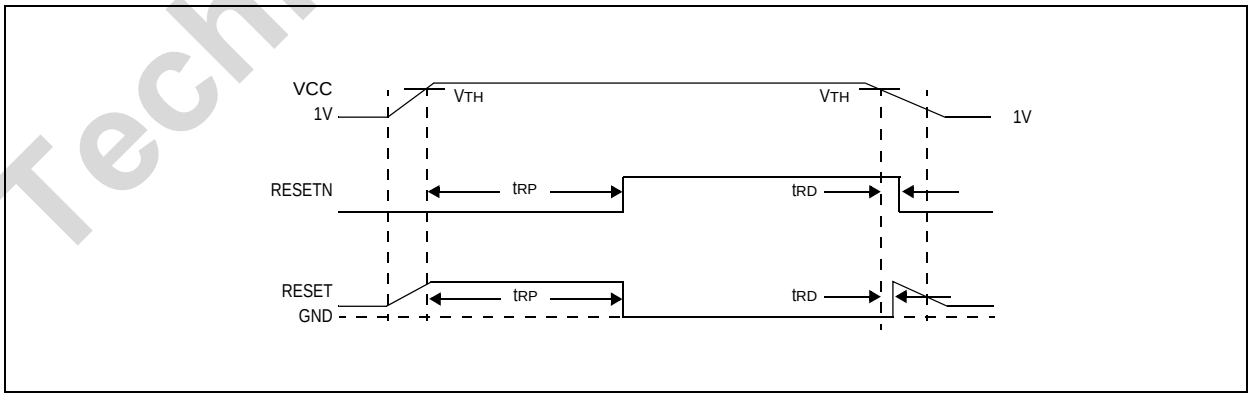


Figure 10. Reset Timing Diagram



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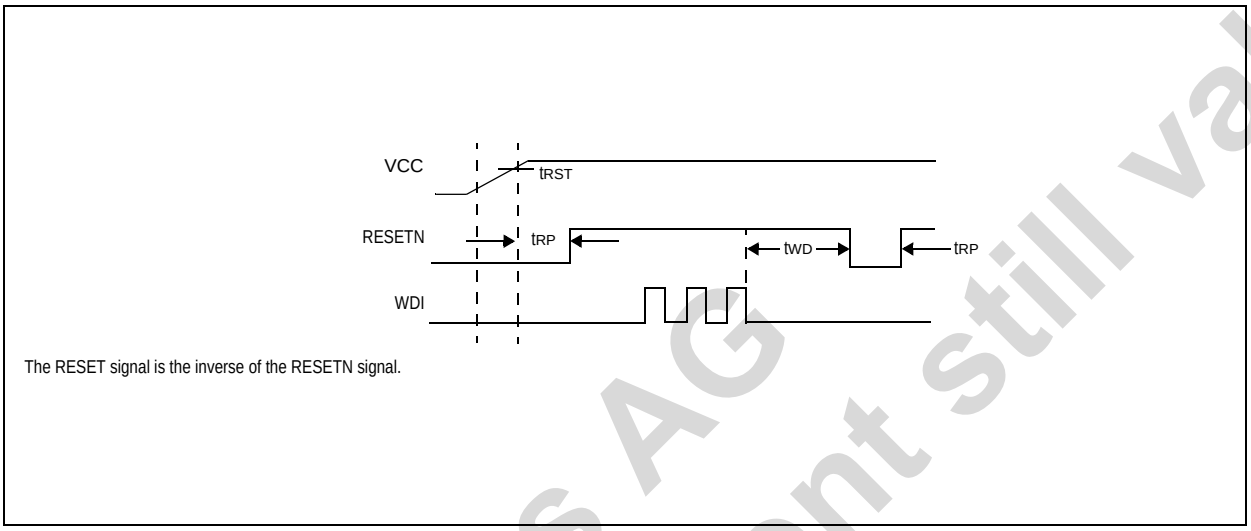
8.2 Watchdog Input

The integrated watchdog feature can be used to monitor processor activity via pin WDI, and can detect pulses as short as 50ns. The watchdog requires that the processor toggle the watchdog logic input at regular intervals, within a specified minimum timeout period (1.5s, typ). A reset is asserted for the reset timeout period. As long as reset is asserted, the timer remains cleared and is not incremented. When reset is deasserted, the watchdog timer starts counting (Figure 11).

Note: The watchdog timer can be cleared with a reset pulse or by toggling WDI.

Figure 11. Watchdog Timing Relationship



The watchdog is internally driven low during most (87.5%) of the watchdog timeout period (see tWD on page 5) and high for the rest of the watchdog timeout period. When pin WDI is left unconnected, this internal driver clears the watchdog timer every 1.4s. When WDI is tri-stated or is not connected, the maximum allowable leakage current is 10µA and the maximum allowable load capacitance is 200pF.

Note: The watchdog function can be disabled by leaving pin WDI unconnected or connecting it to a tri-state output buffer.

8.3 Manual Reset Input

The active-low pin MRN is used to force a manual reset. This input can be driven by CMOS logic levels or with open-drain collector outputs.

Pulling MRN low asserts a reset which will remain asserted as long as MRN is kept low, and for the timeout period (see tRP on page 4) after MRN goes high (140ms min). The manual reset circuitry has an internal 50kΩ pullup resistor, thus it can be left open if not used.

To create a manual-reset circuit, connect a normally open momentary switch from pin MRN to GND (see Figure 1 on page 1); external debounce circuitry is not required in this configuration.

If MRN is driven via long cables or the device is used in a noisy environment, a 0.1µF capacitor between pin MRN and GND will provide additional noise immunity.

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9 Application Information

9.1 Watchdog Input Current

The watchdog input is driven through an internal buffer and an internal series resistor from the watchdog timer (see Figure 11 on page 8). When pin WDI is left unconnected (watchdog disabled), the watchdog timer is serviced within the watchdog timeout period (see t_{WD} on page 5) by a low-high-low pulse from the counter chain.

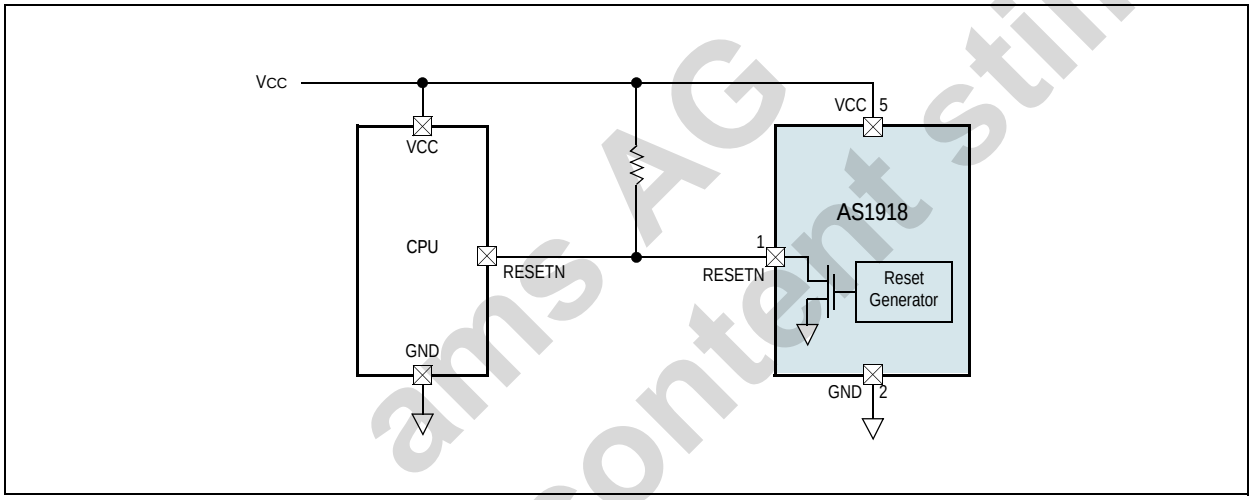
For minimum watchdog input current (minimum overall power consumption), pull WDI low for most of the watchdog timeout period, pulsing it low-high-low once within the first 7/8 (87.5%) of the watchdog timeout period to reset the watchdog timer.

Note: If WDI is externally driven high for the majority of the timeout period, up to 160µA can flow into pin WDI.

9.2 Interfacing to Bi-Directional CPU Reset Pins

Since the reset output of the AS1918 is open drain, this device interfaces easily with processors that have bi-directional reset pins. Connecting the processor reset output directly to the AS1918 RESETN pin with a single pullup resistor (see Figure 12) allows the AS1918 to assert a reset.

Figure 12. AS1918 RESETN-to-CPU Bi-Directional Reset Pin



9.3 Fast Negative-Going Transients

Fast, negative-going V_{CC} transients normally do not require the CPU to be shutdown. The AS1916 - AS1918 are virtually immune to such transients. Resets are issued to the CPU during power-up, powerdown, and brownout conditions.

Note: V_{CC} transients that go 100mV below the reset threshold and last ≤ 55µs typically will not assert a reset pulse.

9.4 Valid Reset to V_{CC} = 0

The AS1916 - AS1918 are guaranteed to operate properly down to V_{CC} = 1V.

For AS1916 and AS1917 applications requiring valid reset levels down to V_{CC} = 0, a pulldown resistor to active-low outputs and a pullup resistor to active-high outputs will ensure that the reset line is valid during the interval where the reset output can no longer sink or source current.

9.5 Watchdog Tips

Careful consideration should be taken when implementing the AS1916 - AS1918 watchdog feature.

One method of supervising software code execution is to set/reset the watchdog input at different places in the code, rather than pulsing the watchdog input high-low-high or low-high-low. This method avoids a loop condition in which the watchdog timer would continue to be reset inside the loop, preventing the watchdog from ever timing out.

Figure 13 shows a flowchart where the input/output driving the watchdog is set high at the beginning of the routine, set low at the beginning of every subroutine, then set high again when the routine returns to the beginning. If the routine should hang in a subroutine, the problem would quickly be corrected, since the I/O is continually set low and the watchdog timer is allowed to time out, causing a reset or interrupt to be issued (see Watchdog Input Current on page 9). This method results in higher averaged WDI input current over time than a case where WDI is held low for the majority (87.5%) of the timeout period and periodically pulsing it low-high-low.

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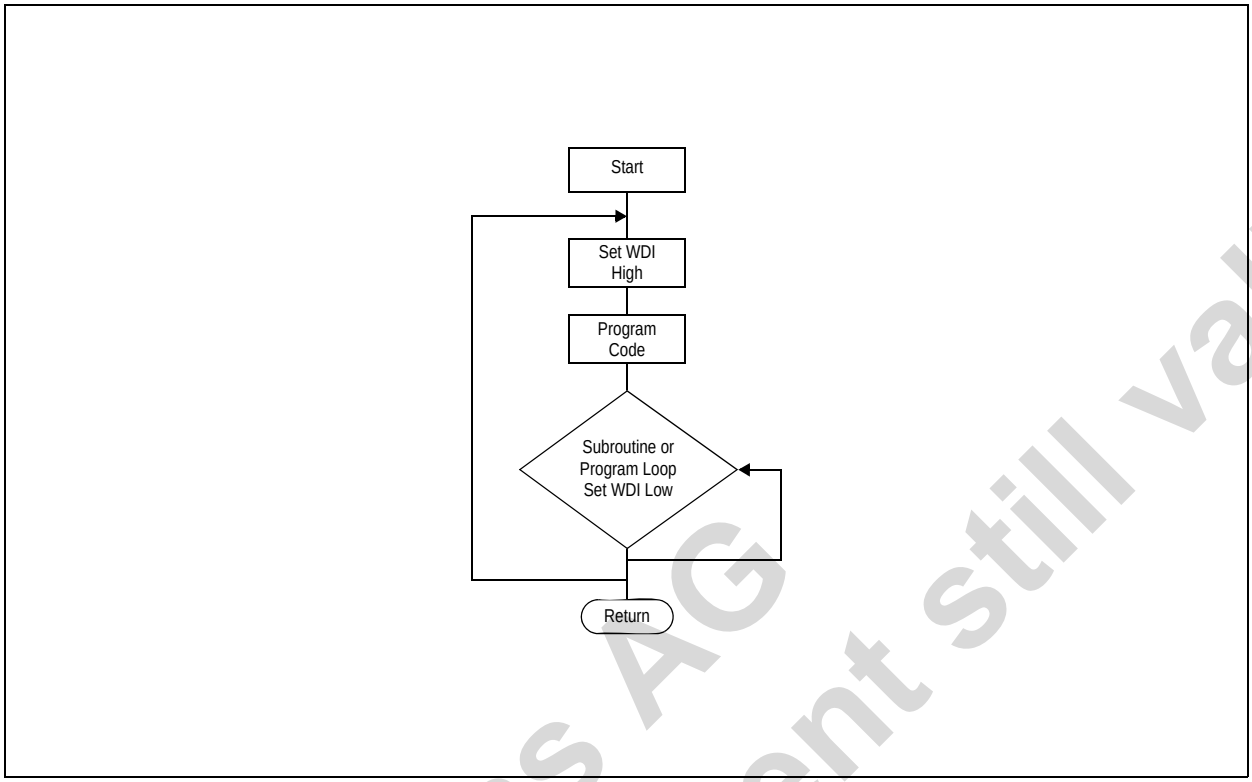
Figure 13. Example Watchdog Programming Flowchart



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10 Package Drawings and Markings

Figure 14. 5-pin SOT23 Marking

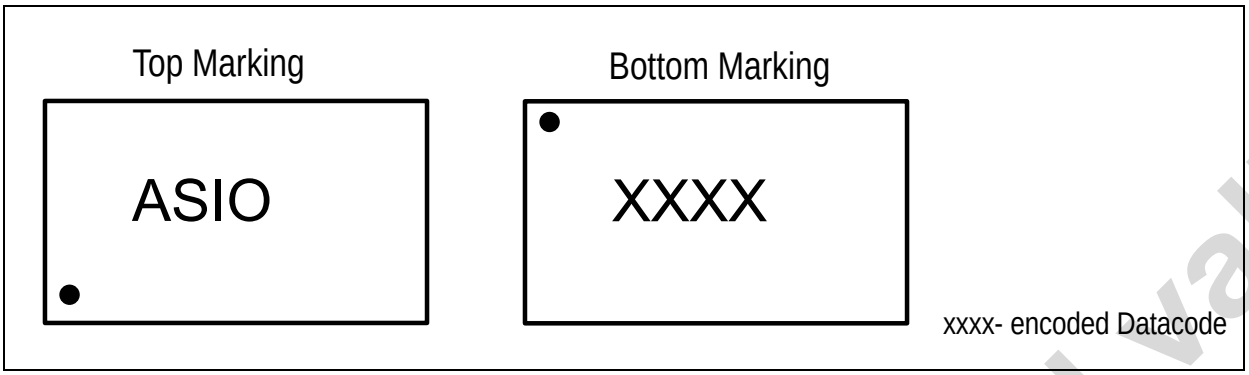

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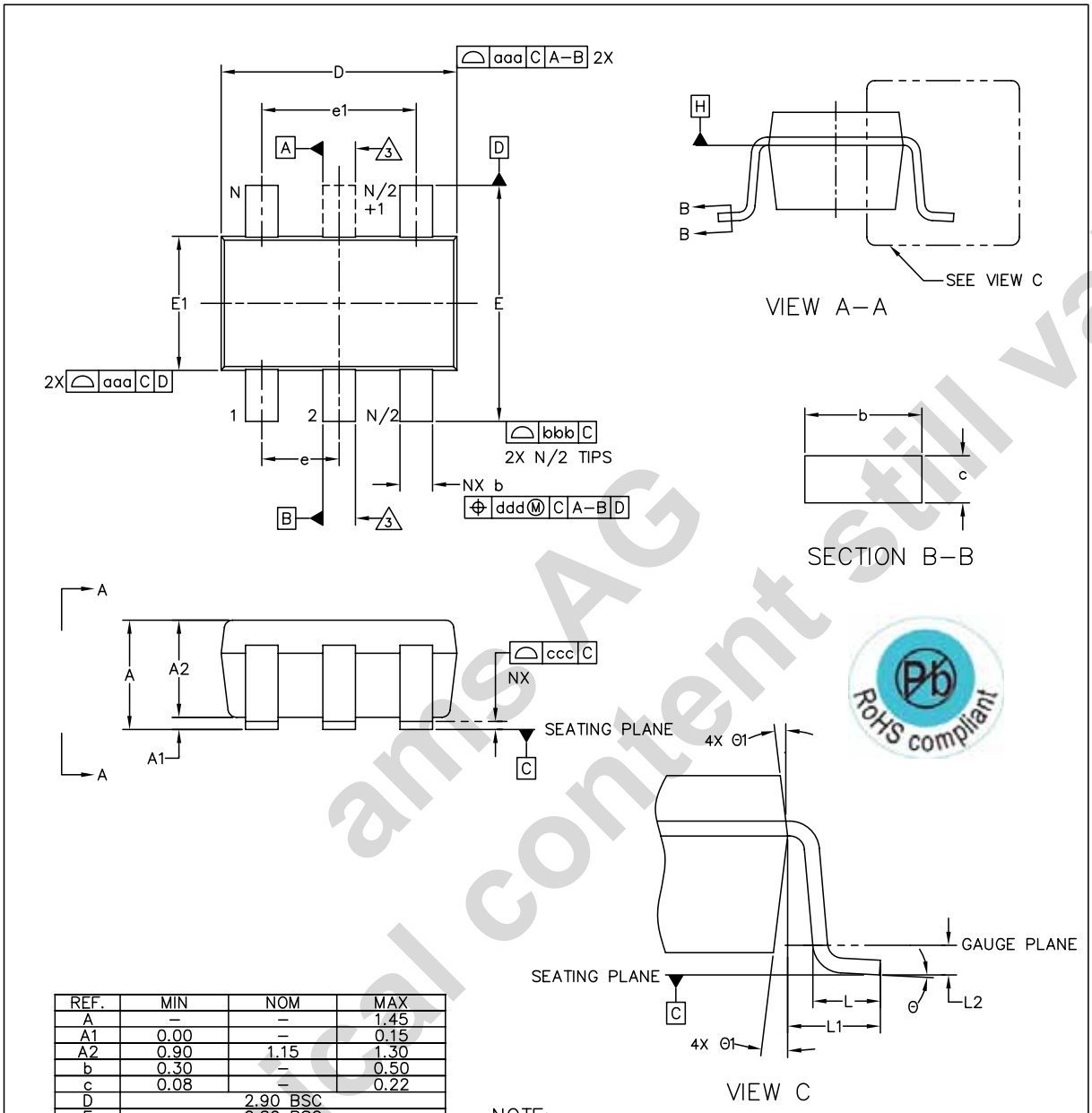
Figure 15. 5-pin SOT23 Package



REF.	MIN	NOM	MAX
A	–	–	1.45
A1	0.00	–	0.15
A2	0.90	1.15	1.30
b	0.30	–	0.50
c	0.08	–	0.22
D		2.90 BSC	
E		2.80 BSC	
E1		1.60 BSC	
e		0.95 BSC	
e1		1.90 BSC	
L	0.30	0.45	0.60
L1		0.60 REF	
L2		0.25 BSC	
θ	0°	4°	8°
θ1	5°	10°	15°
aaa	–	0.15	–
bbb	–	0.20	–
ccc	–	0.10	–
ddd	–	0.20	–
N		5	

NOTE:

1. DIMENSIONS & TOLERANCEING CONFIRM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGELS ARE IN DEGREES.
3. DATUMS A & B TO BE DETERMINED AT DATUM H.

austriamicrosystems a leap ahead in analog			ASSEMBLY ENGINEERING	
DRAWN RH8	DATE 2010.12.21	REV. N/C	TITLE SOT23, 5 LEAD	REFERENCE DOCUMENT JEDEC MO – 178 LATEST REVISION
CHECKED GBO	DATE 2010.12.21		DRAWING NO. JEZ	UNIT
APPROVED MKR	DATE 2010.12.21	SHEET 1 OF 1	DIMENSION AND TOLERANCE	SCALE NOT IN SCALE

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11 Ordering Information

The devices are available as the standard products shown in Table 5.

Table 5. Ordering Information

Ordering Code	Marking	Description	Threshold	Delivery Form	Package
AS1916S-T	ASIO	Active-Low Push/Pull Supervisory Circuit with Watchdog and Manual Reset	2.93V	Tape and Reel	5-pin SOT23
AS1916R-T	ASIP	Active-Low Push/Pull Supervisory Circuit with Watchdog and Manual Reset	2.63V	Tape and Reel	5-pin SOT23
AS1916Z-T	ASIQ	Active-Low Push/Pull Supervisory Circuit with Watchdog and Manual Reset	2.32V	Tape and Reel	5-pin SOT23
AS1916V-T	ASIR	Active-Low Push/Pull Supervisory Circuit with Watchdog and Manual Reset	1.58V	Tape and Reel	5-pin SOT23
AS1917S-T	ASIS	Active High Push/Pull Supervisory Circuit with Watchdog and Manual Reset	2.93V	Tape and Reel	5-pin SOT23
AS1917R-T	ASIT	Active High Push/Pull Supervisory Circuit with Watchdog and Manual Reset	2.63V	Tape and Reel	5-pin SOT23
AS1917Z-T	ASIU	Active High Push/Pull Supervisory Circuit with Watchdog and Manual Reset	2.32V	Tape and Reel	5-pin SOT23
AS1917V-T	ASIV	Active High Push/Pull Supervisory Circuit with Watchdog and Manual Reset	1.58V	Tape and Reel	5-pin SOT23
AS1918S-T	ASIW	Active-Low Open Drain Supervisory Circuit with Watchdog and Manual Reset	2.93V	Tape and Reel	5-pin SOT23
AS1918R-T	ASIX	Active-Low Open Drain Supervisory Circuit with Watchdog and Manual Reset	2.63V	Tape and Reel	5-pin SOT23
AS1918Z-T	ASIY	Active-Low Open Drain Supervisory Circuit with Watchdog and Manual Reset	2.32V	Tape and Reel	5-pin SOT23
AS1918V-T	ASIZ	Active-Low Open Drain Supervisory Circuit with Watchdog and Manual Reset	1.58V	Tape and Reel	5-pin SOT23

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