



**THE DATASHEET OF  
AUIRFSL8403**



**Features**

- Advanced Process Technology
- New Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified \*

**Description**

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and wide variety of other applications.

**Applications**

- Electric Power Steering (EPS)
- Battery Switch
- Start/Stop Micro Hybrid
- Heavy Loads
- DC-DC Converter

**Ordering Information**

Base part number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRFL8403	TO-262	Tube	50	AUIRFL8403
AUIRFS8403	D2Pak	Tube	50	AUIRFS8403
		Tape and Reel Left	800	AUIRFS8403TRL
		Tape and Reel Right	800	AUIRFS8403TRR

**Absolute Maximum Ratings**

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T<sub>A</sub>) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited)	123	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited)	87	
I <sub>DM</sub>	Pulsed Drain Current ①	492	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Maximum Power Dissipation	99	W
	Linear Derating Factor	0.66	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	V
T <sub>J</sub>	Operating Junction and	-55 to + 175	°C
T <sub>STG</sub>	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

**Avalanche Characteristics**

E <sub>AS</sub> (Thermally limited)	Single Pulse Avalanche Energy ②	111	mJ
E <sub>AS</sub> (tested)	Single Pulse Avalanche Energy Tested Value ③	160	
I <sub>AR</sub>	Avalanche Current ①	See Fig. 14, 15 , 24a, 24b	A
E <sub>AR</sub>	Repetitive Avalanche Energy ①		mJ

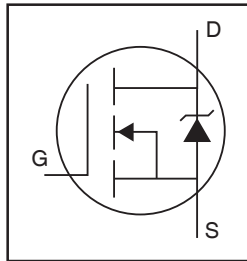
**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case ②	—	1.52	°C/W
R <sub>θJA</sub>	Junction-to-Ambient (PCB Mount) D2 Pak	—	40	

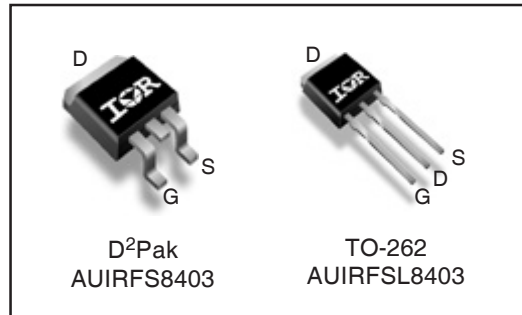
HEXFET® is a registered trademark of International Rectifier.

\*Qualification standards can be found at <http://www.irf.com/>

HEXFET® Power MOSFET



V <sub>DSS</sub>	40V
R <sub>DS(on)</sub> typ.	2.6mΩ
	max.
I <sub>D</sub> (Silicon Limited)	123A



G	D	S
Gate	Drain	Source

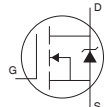
**Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.033	—	V/°C	Reference to $25^\circ\text{C}, I_D = 5mA$ ⓐ
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	2.6	3.3	mΩ	$V_{GS} = 10V, I_D = 70A$ ⓑ
$V_{GS(th)}$	Gate Threshold Voltage	2.2	3.0	3.9	V	$V_{DS} = V_{GS}, I_D = 100\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 40V, V_{GS} = 0V$
		—	—	150		$V_{DS} = 40V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{OSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
$R_G$	Internal Gate Resistance	—	1.6	—	Ω	

**Dynamic @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	269	—	—	S	$V_{DS} = 10V, I_D = 70A$
$Q_g$	Total Gate Charge	—	62	93	nC	$I_D = 70A$
$Q_{gs}$	Gate-to-Source Charge	—	16	—		$V_{DS} = 20V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	20	—		$V_{GS} = 10V$ ⓐ
$Q_{sync}$	Total Gate Charge Sync. ( $Q_g - Q_{gd}$ )	—	42	—		$I_D = 70A, V_{DS} = 0V, V_{GS} = 10V$
$t_{d(on)}$	Turn-On Delay Time	—	10	—	ns	$V_{DD} = 26V$
$t_r$	Rise Time	—	77	—		$I_D = 70A$
$t_{d(off)}$	Turn-Off Delay Time	—	26	—		$R_G = 1\Omega$
$t_f$	Fall Time	—	43	—		$V_{GS} = 10V$ ⓐ
$C_{iss}$	Input Capacitance	—	3183	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	475	—		$V_{DS} = 25V$
$C_{riss}$	Reverse Transfer Capacitance	—	331	—		$f = 1.0\text{ MHz}$ , See Fig. 5
$C_{oss\text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)	—	596	—		$V_{GS} = 0V, V_{DS} = 0V\text{ to }32V$ ⓑ, See Fig. 11
$C_{oss\text{ eff. (TR)}}$	Effective Output Capacitance (Time Related)	—	688	—		$V_{GS} = 0V, V_{DS} = 0V\text{ to }32V$ ⓑ

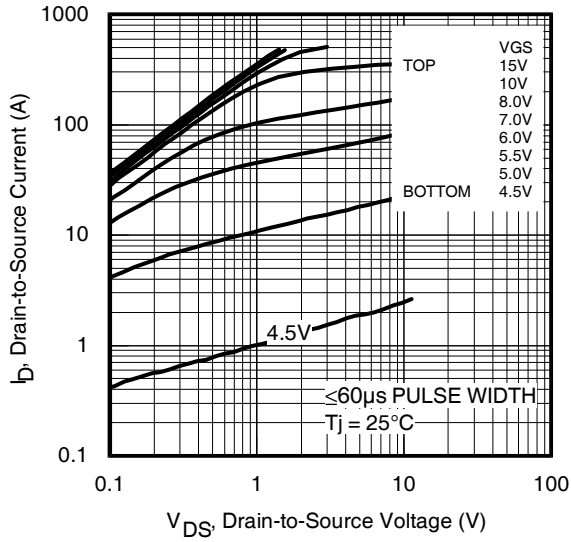
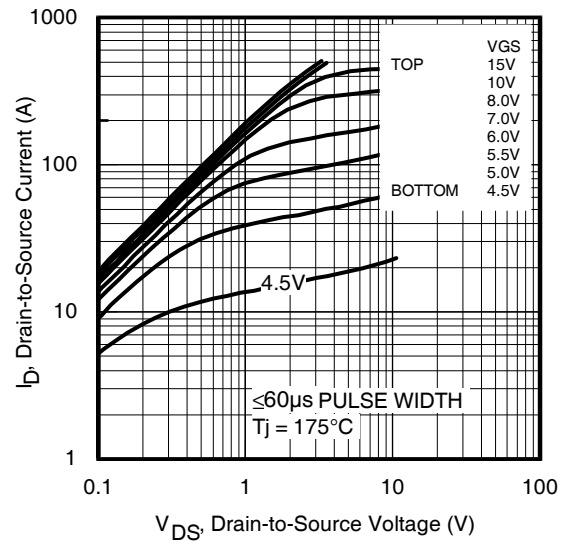
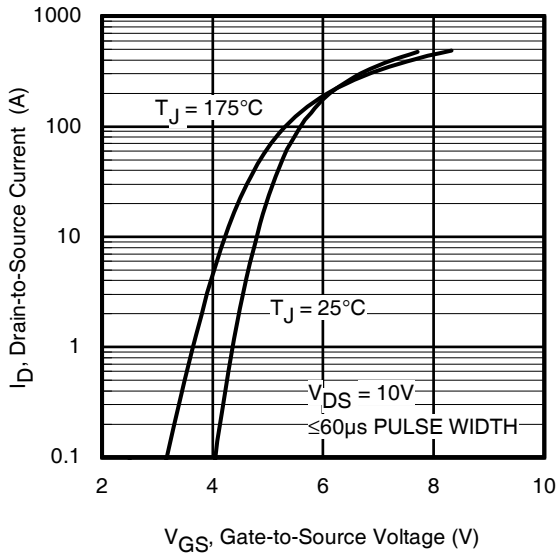
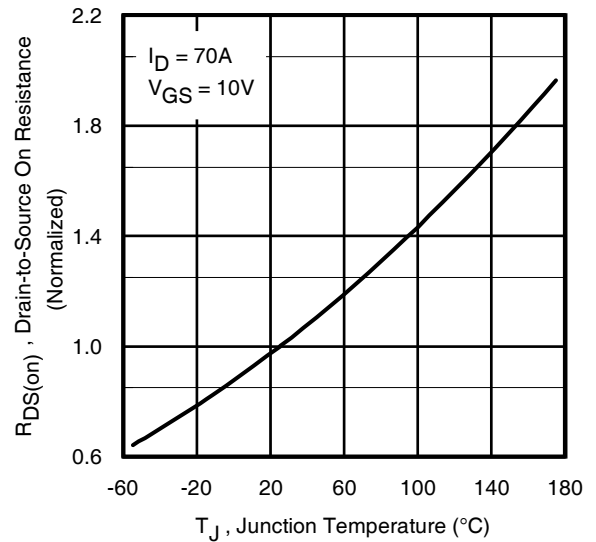
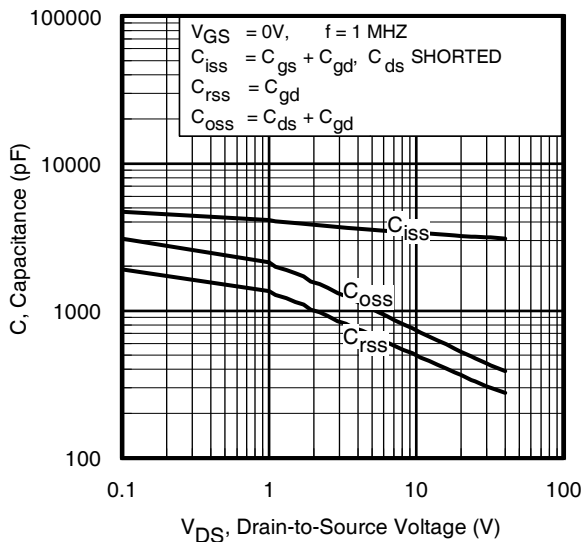
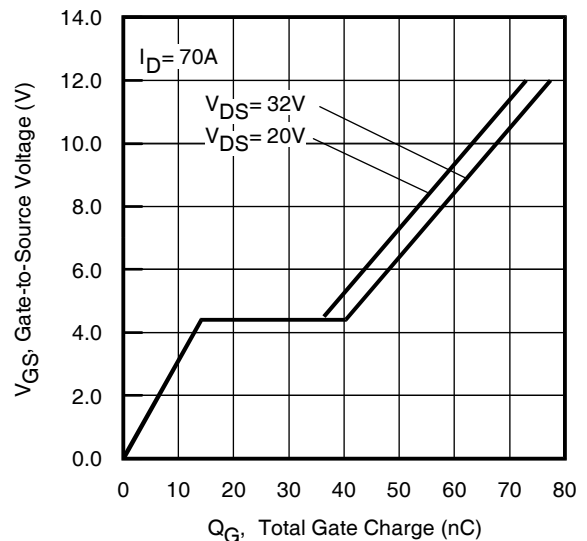
**Diode Characteristics**

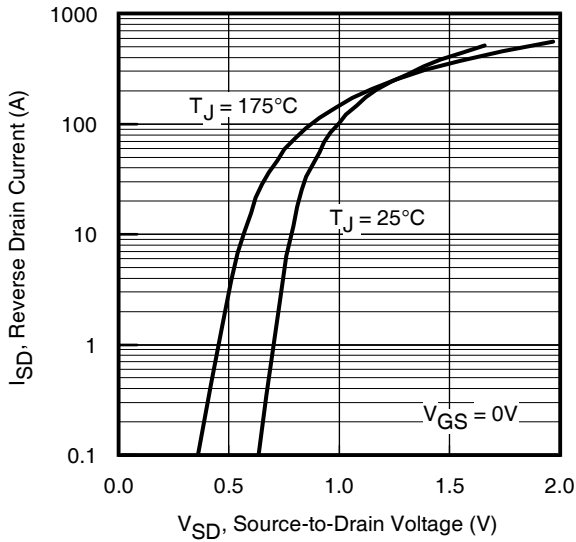
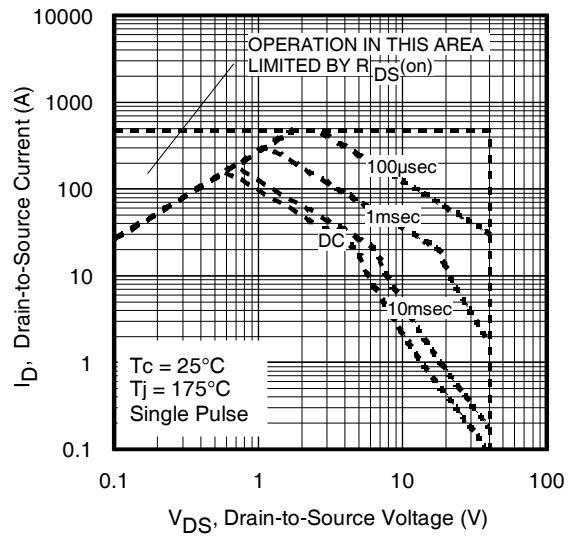
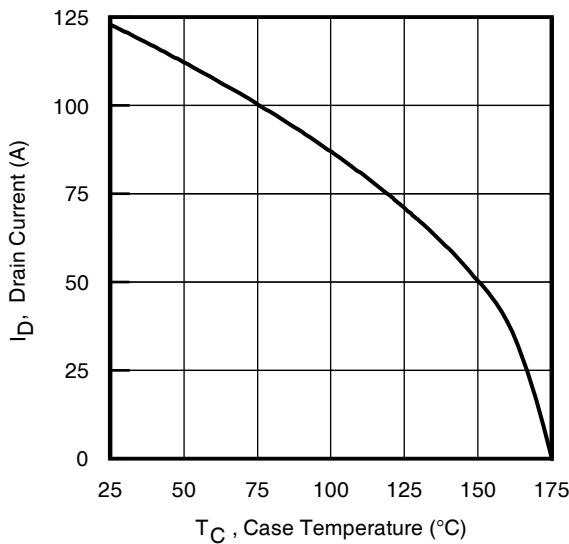
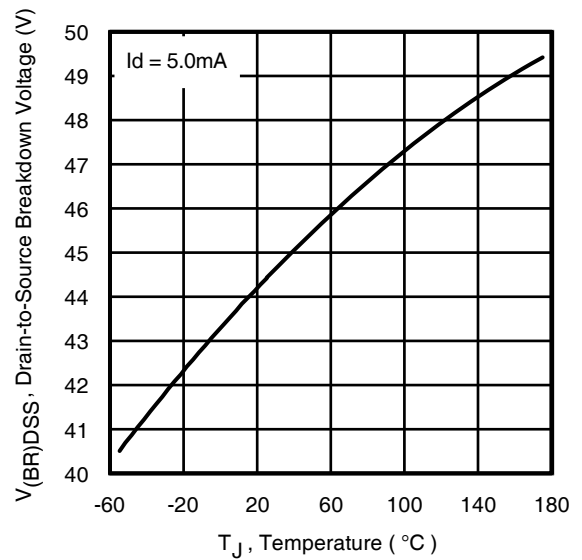
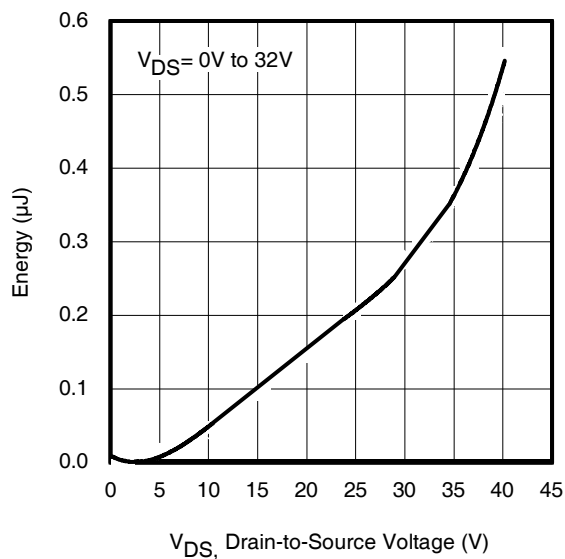
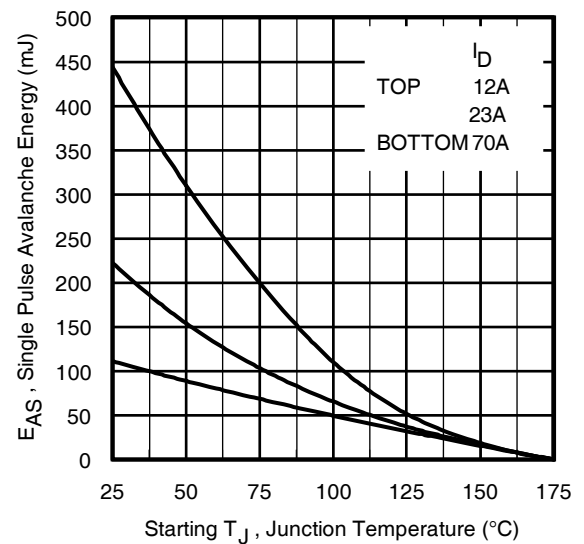
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	118	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ⓐ	—	—	472		
$V_{SD}$	Diode Forward Voltage	—	0.9	1.3	V	$T_J = 25^\circ\text{C}, I_S = 70A, V_{GS} = 0V$ ⓐ
dv/dt	Peak Diode Recovery ⓑ	—	7.6	—	V/ns	$T_J = 175^\circ\text{C}, I_S = 70A, V_{DS} = 40V$
$t_{rr}$	Reverse Recovery Time	—	22	—	ns	$T_J = 25^\circ\text{C}$
		—	24	—		$T_J = 125^\circ\text{C}$
$Q_{rr}$	Reverse Recovery Charge	—	15	—	nC	$T_J = 25^\circ\text{C}$
		—	15	—		$T_J = 125^\circ\text{C}$
$I_{RRM}$	Reverse Recovery Current	—	1.0	—	A	$T_J = 25^\circ\text{C}$

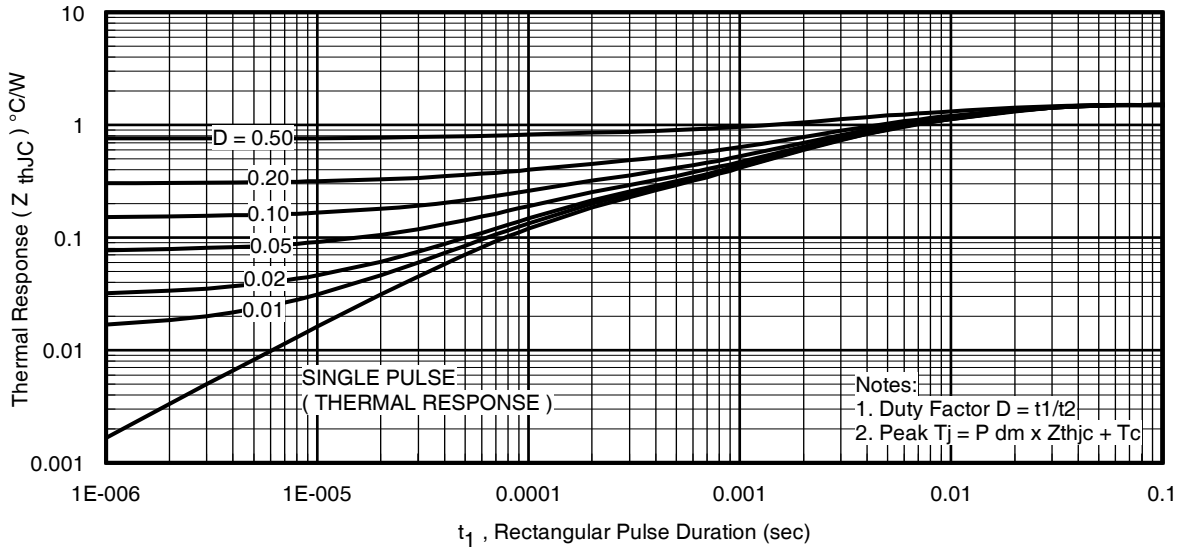
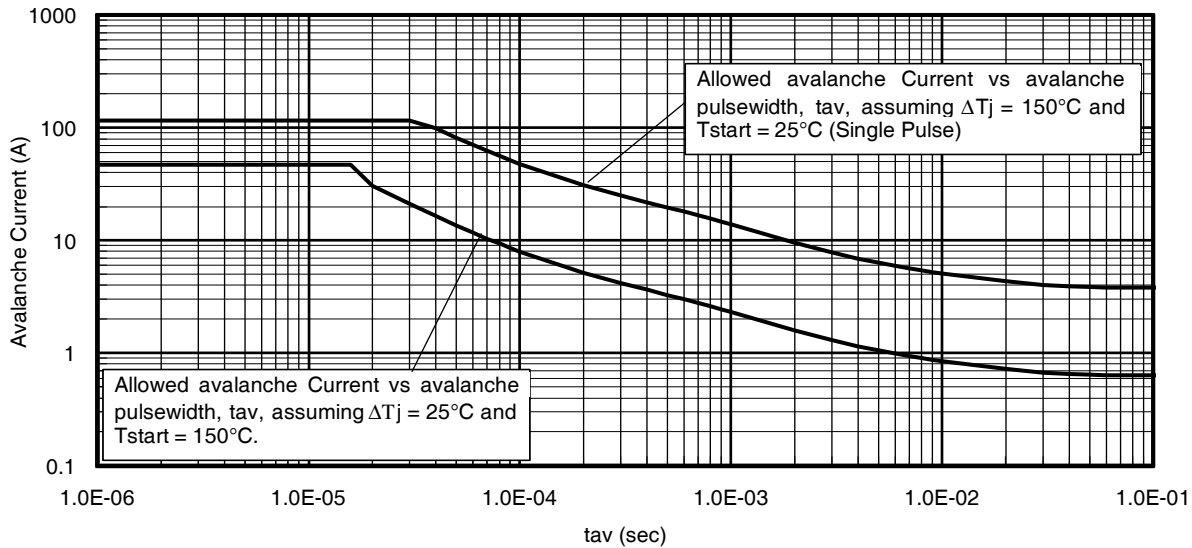
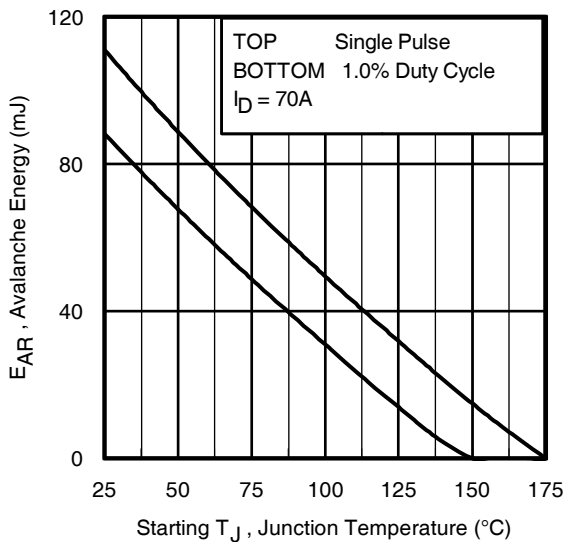
**Notes:**

- ⓐ Repetitive rating; pulse width limited by max. junction temperature.
- ⓑ Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.046\text{mH}, R_G = 50\Omega$ ,  $I_{AS} = 70A, V_{GS} = 10V$ .
- ⓒ  $I_{SD} \leq 70A, di/dt \leq 1174A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^\circ\text{C}$ .
- ⓓ Pulse width  $\leq 400\mu s$ ; duty cycle  $\leq 2\%$ .
- ⓔ  $C_{oss\text{ eff. (TR)}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

- ⓕ  $C_{oss\text{ eff. (ER)}}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⓖ  $R_\theta$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .
- ⓗ This value determined from sample failure population, starting  $T_J = 25^\circ\text{C}, L = 0.046\text{mH}, R_G = 50\Omega, I_{AS} = 70A, V_{GS} = 10V$ .


**Fig 1. Typical Output Characteristics**

**Fig 2. Typical Output Characteristics**

**Fig 3. Typical Transfer Characteristics**

**Fig 4. Normalized On-Resistance vs. Temperature**

**Fig 5. Typical Capacitance vs. Drain-to-Source Voltage**

**Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage**


**Fig 7.** Typical Source-Drain Diode Forward Voltage

**Fig 8.** Maximum Safe Operating Area

**Fig 9.** Maximum Drain Current vs. Case Temperature

**Fig 10.** Drain-to-Source Breakdown Voltage

**Fig 11.** Typical  $C_{OSS}$  Stored Energy

**Fig 12.** Maximum Avalanche Energy vs. Drain Current

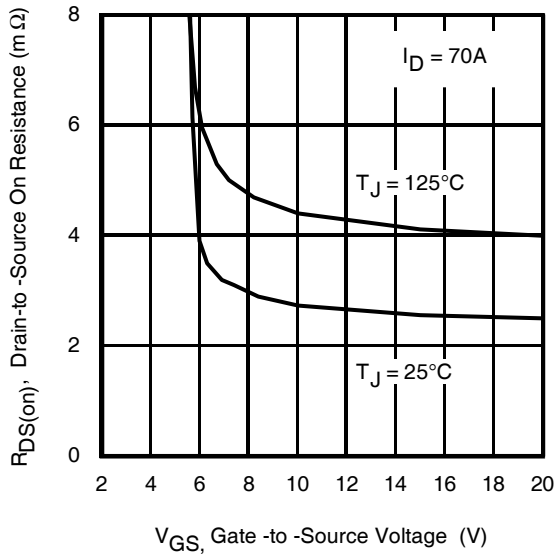
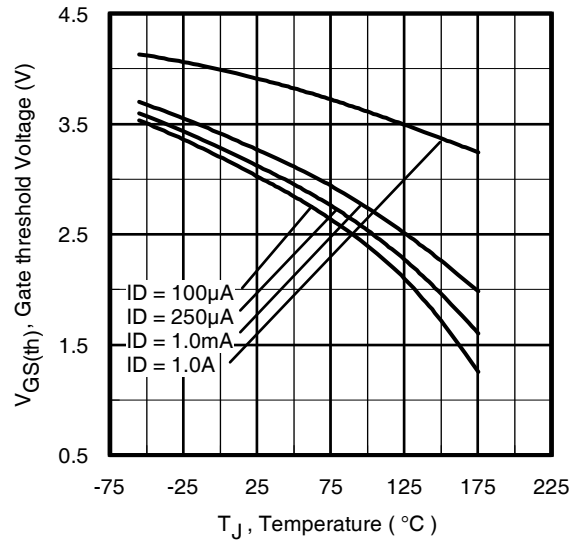
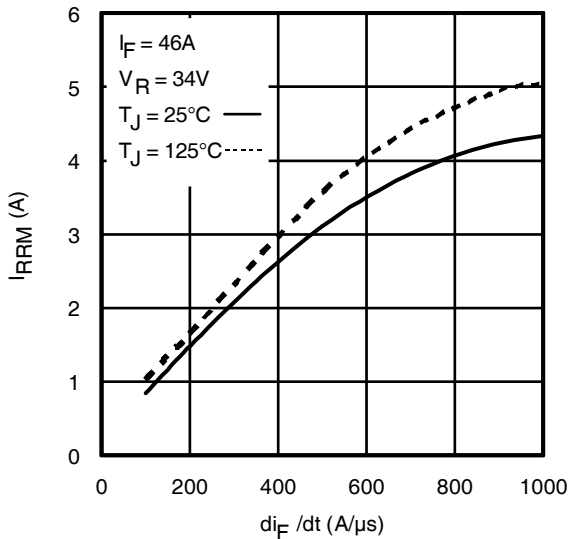
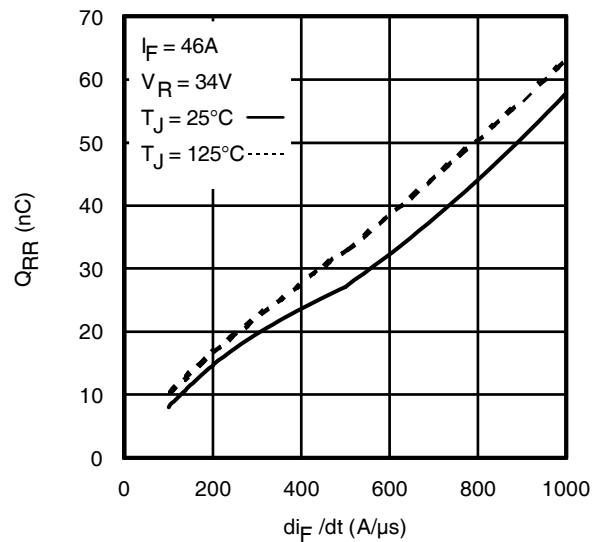
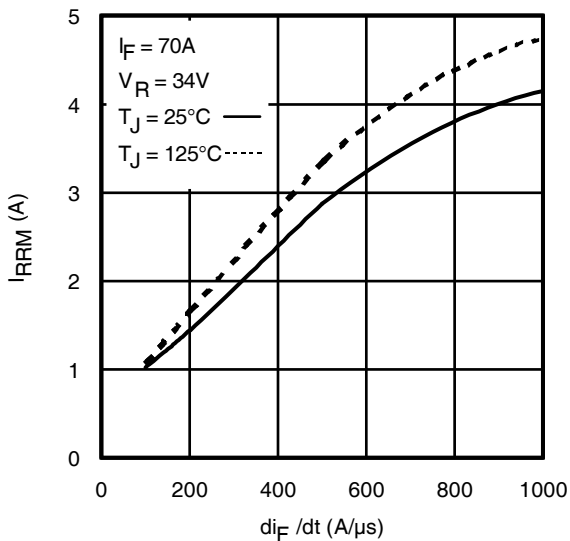
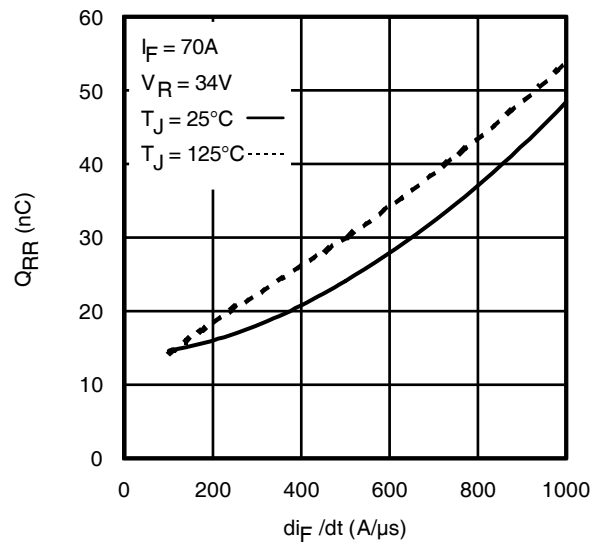

**Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case**

**Fig 14. Typical Avalanche Current vs. Pulsewidth**

**Fig 15. Maximum Avalanche Energy vs. Temperature**
**Notes on Repetitive Avalanche Curves , Figures 14, 15  
(For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 24a, 24b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2 \Delta T / [ 1.3 \cdot BV \cdot Z_{th} ]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$


**Fig 16.** On-Resistance vs. Gate Voltage

**Fig 17.** Threshold Voltage vs. Temperature

**Fig. 18 -** Typical Recovery Current vs.  $di_f/dt$ 

**Fig. 19 -** Typical Stored Charge vs.  $di_f/dt$ 

**Fig. 20 -** Typical Recovery Current vs.  $di_f/dt$ 

**Fig. 21 -** Typical Stored Charge vs.  $di_f/dt$

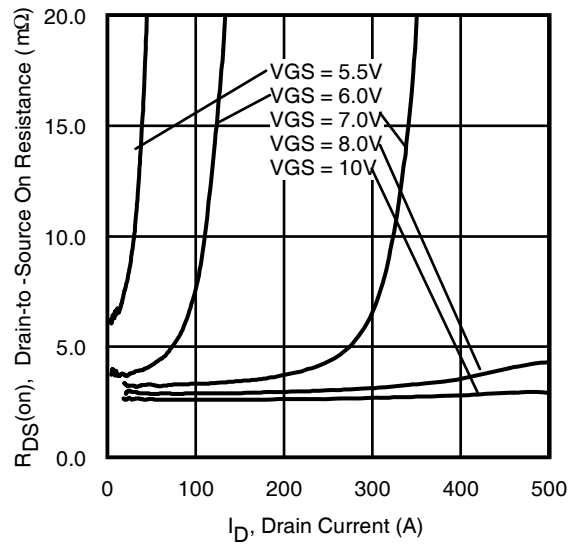
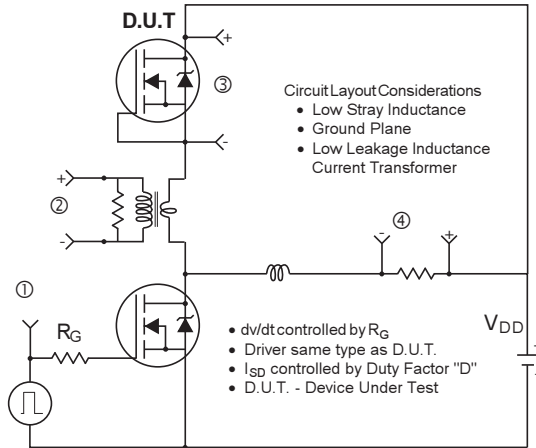
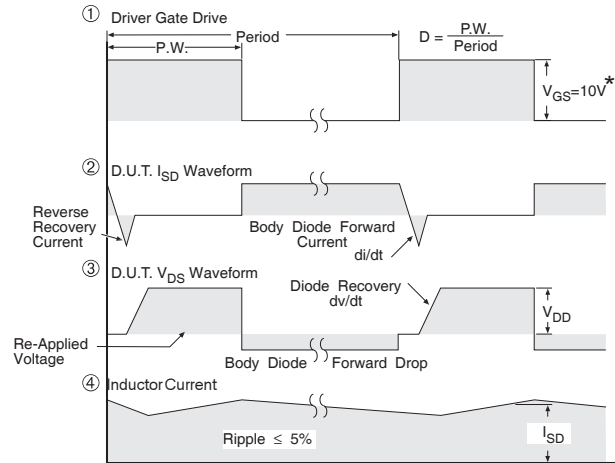


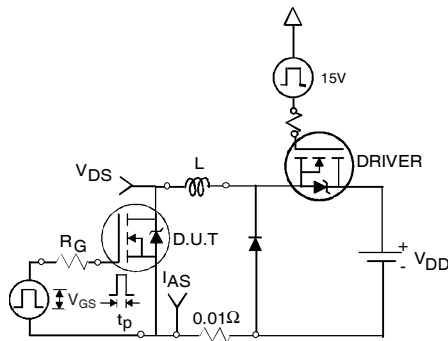
Fig 22. Typical On-Resistance vs. Drain Current



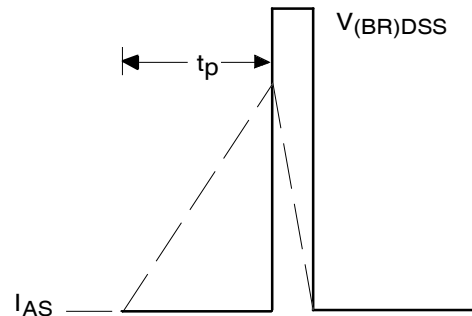
**Fig 23. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs**



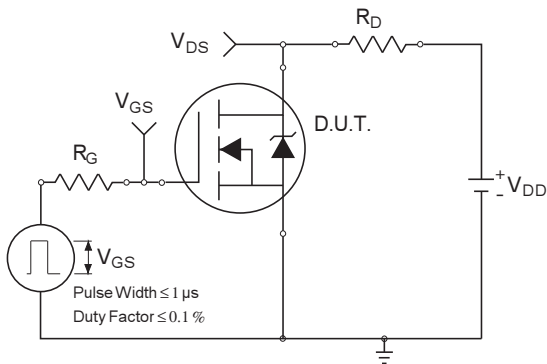
\*  $V_{GS} = 5V$  for Logic Level Devices



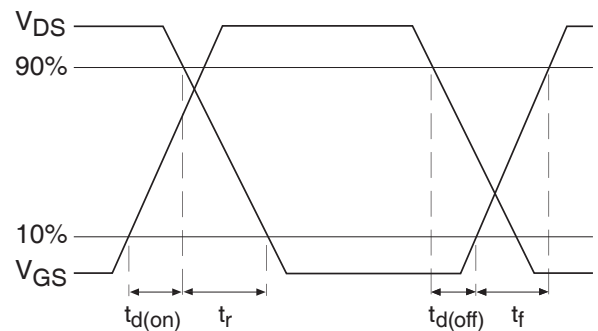
**Fig 24a. Unclamped Inductive Test Circuit**



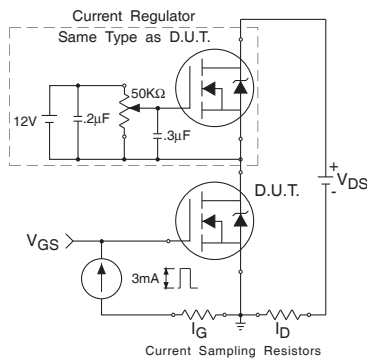
**Fig 24b. Unclamped Inductive Waveforms**



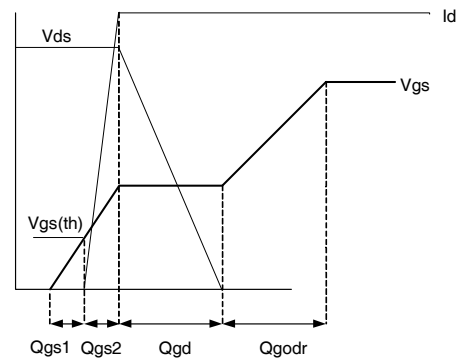
**Fig 25a. Switching Time Test Circuit**



**Fig 25b. Switching Time Waveforms**

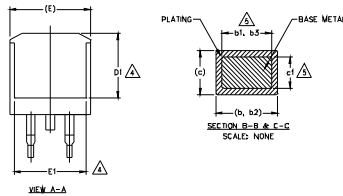
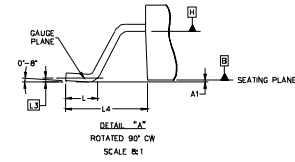
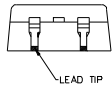
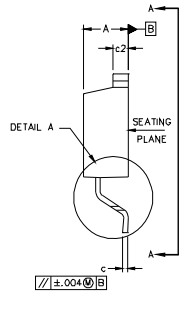
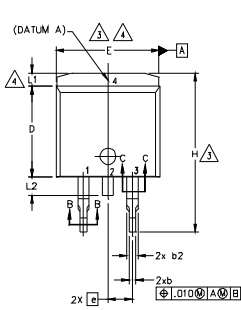


**Fig 26a. Gate Charge Test Circuit**



**Fig 26b. Gate Charge Waveform**

## D<sup>2</sup>Pak Package Outline (Dimensions are shown in millimeters (inches))


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245	-	4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	-	1.65	-	.066	4
L2	1.27	1.78	-	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	

**LEAD ASSIGNMENTS**
**HEXFET**

- 1.- GATE
- 2, 4.- DRAIN
- 3.- SOURCE

**IGBTs, CoPACK**

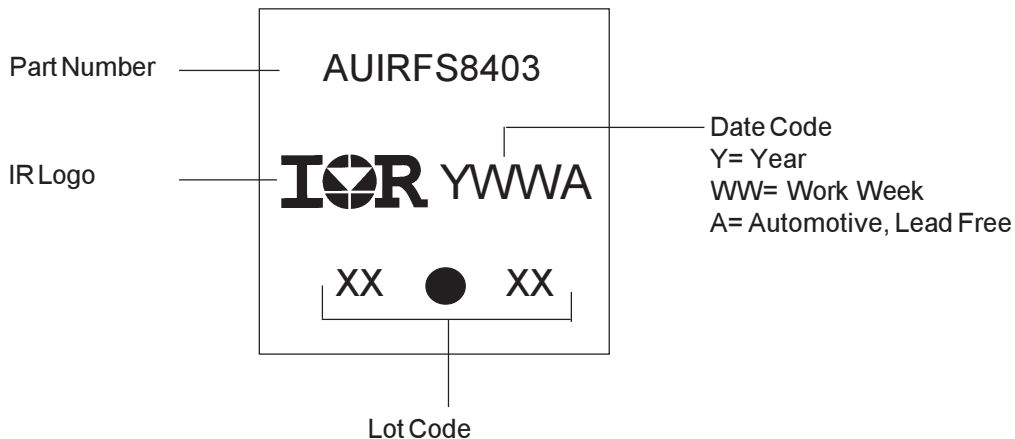
- 1.- GATE
- 2, 4.- COLLECTOR
- 3.- EMITTER

**DIODES**

- 1.- ANODE \*
- 2, 4.- CATHODE
- 3.- ANODE

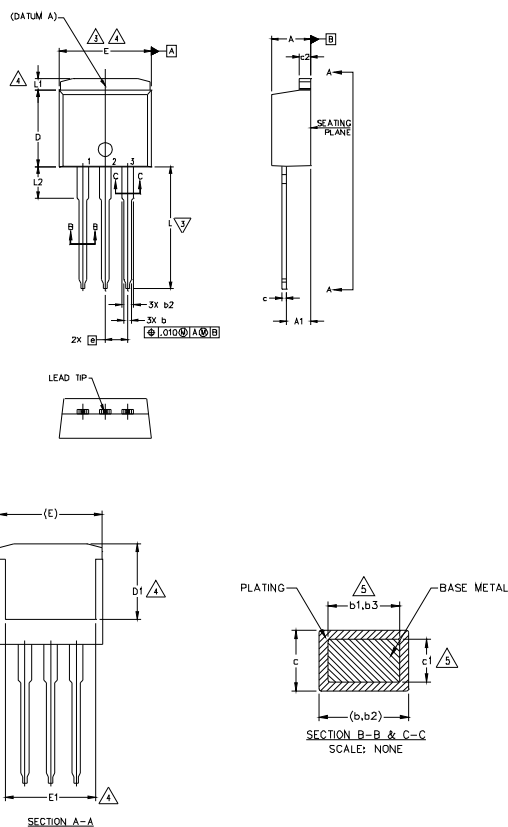
\* PART DEPENDENT.

## D<sup>2</sup>Pak Part Marking Information



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

## TO-262 Package Outline ( Dimensions are shown in millimeters (inches))



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245	-	4
e	2.54 BSC		.100 BSC		
L	13.46	14.10	.530	.555	
L1	-	1.65	-	.065	4
L2	3.56	3.71	.140	.146	

LEAD ASSIGNMENTS

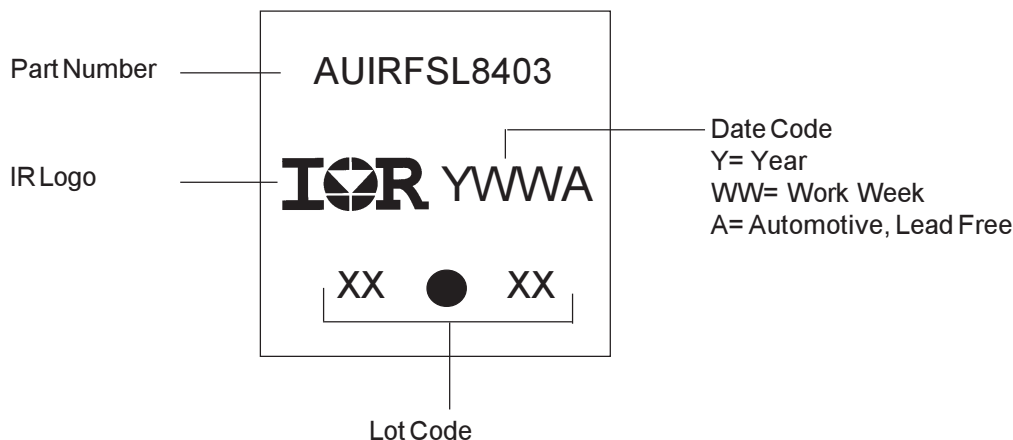
HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

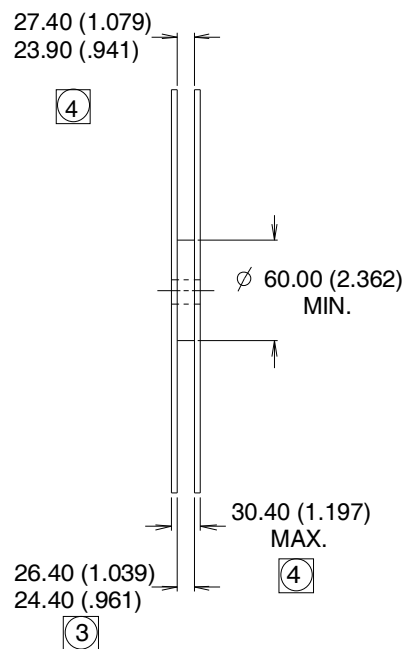
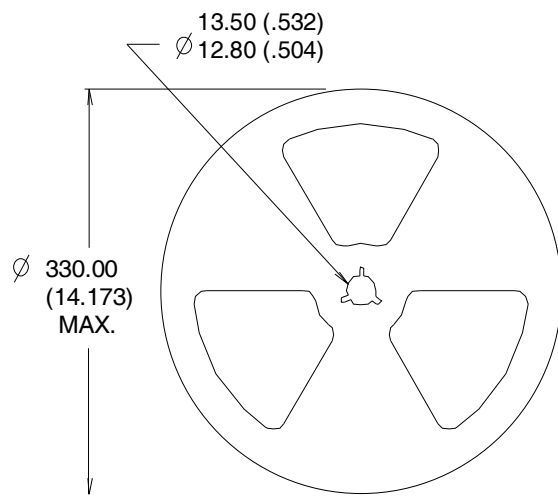
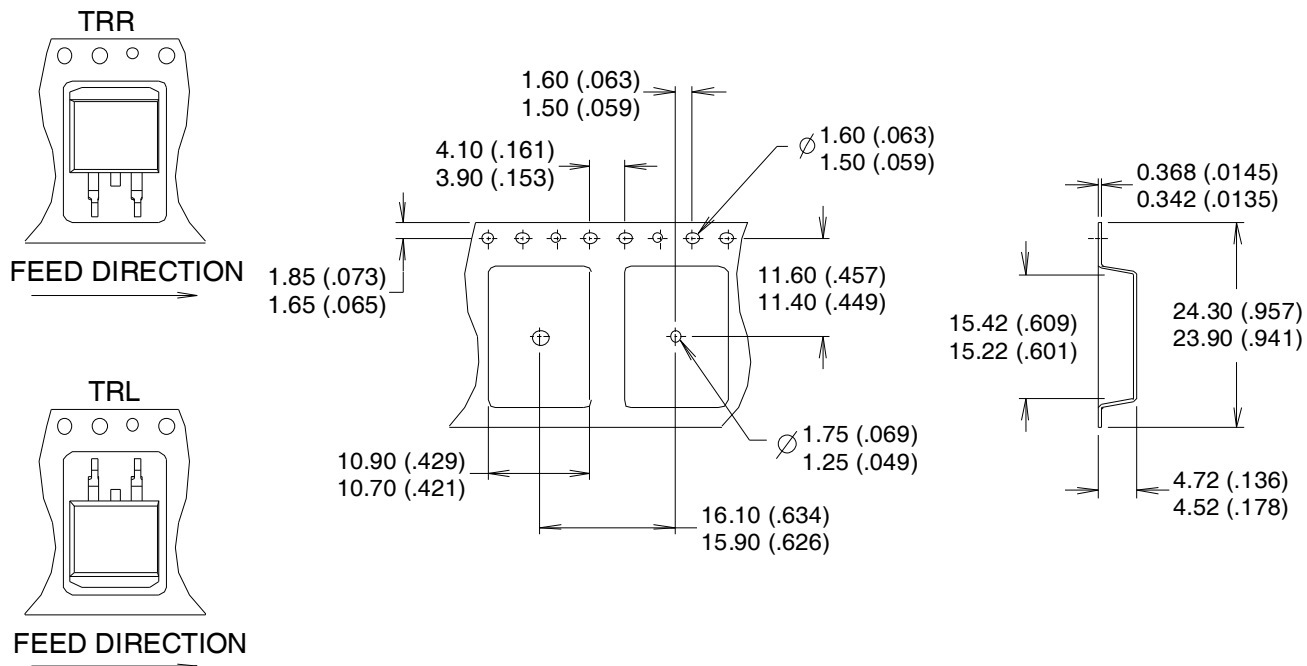
## TO-262 Part Marking Information



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

## D<sup>2</sup>Pak (TO-263AB) Tape & Reel Information

Dimensions are shown in millimeters (inches)



**NOTES :**

1. CONFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
- ③ DIMENSION MEASURED @ HUB.
- ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
<b>Moisture Sensitivity Level</b>		3L-D <sup>2</sup> PAK	MSL1
		3L-TO-262-PAK	N/A
<b>ESD</b>	Machine Model	Class M4 (+/- 600) <sup>††</sup> AEC-Q101-002	
	Human Body Model	Class H1C (+/- 2000) <sup>††</sup> AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 2000) <sup>††</sup> AEC-Q101-005	
<b>RoHS Compliant</b>		Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/>

†† Highest passing voltage.

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