



**THE DATASHEET OF  
BLF13H9LS750PU**



# BLF13H9L750P; BLF13H9LS750P

Power LDMOS transistor

Rev. 1 — 20 September 2018

AMPLEON

Product data sheet

## 1. Product profile

### 1.1 General description

750 W LDMOS power transistor in SOT539 push pull package for accelerator applications at a frequency of 1.3 GHz.

**Table 1. Typical performance**

Typical RF performance at  $T_{case} = 25\text{ °C}$ ;  $t_p = 300\text{ }\mu\text{s}$ ;  $\delta = 10\%$ ;  $I_{Dq} = 200\text{ mA}$ ; in a class-AB demo circuit.

Test signal	f (GHz)	V <sub>DS</sub> (V)	P <sub>L</sub> (W)	G <sub>p</sub> (dB)	$\eta_D$ (%)
pulsed RF	1.3	50	750	19	62
CW	1.3	50	700	17	62.5

### 1.2 Features and benefits

- High efficiency
- Excellent ruggedness
- Excellent thermal stability
- Easy power control
- Integrated dual sided ESD protection enables excellent off-state isolation
- High flexibility with respect to pulse formats
- Internally matched for ease of use
- For RoHS compliance see the product details on the Ampleon website

### 1.3 Applications

- Accelerator applications at the frequency of 1.3 GHz

## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
<b>BLF13H9L750P (SOT539A)</b>			
1	drain1		 sym117
2	drain2		
3	gate1		
4	gate2		
5	source <a href="#">[1]</a>		
<b>BLF13H9LS750P (SOT539B)</b>			
1	drain1		 sym117
2	drain2		
3	gate1		
4	gate2		
5	source <a href="#">[1]</a>		

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF13H9L750P	-	flanged balanced ceramic package; 2 mounting holes; 4 leads	SOT539A
BLF13H9LS750P	-	earless flanged balanced ceramic package; 4 leads	SOT539B

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Min	Max	Unit
$V_{DS}$	drain-source voltage	-	108	V
$V_{GS}$	gate-source voltage	-8	+11	V
$T_{stg}$	storage temperature	-65	+150	°C
$T_j$	junction temperature <a href="#">[1]</a>	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-case)}$	thermal impedance from junction to case	$T_{case} = 85\text{ °C}; P_L = 650\text{ W}$	0.15	K/W
$Z_{th(j-case)}$	transient impedance from junction to case	$T_{case} = 85\text{ °C}; P_L = 750\text{ W}$		
		$t_p = 100\text{ }\mu\text{s}; \delta = 10\text{ }\%$	0.045	K/W
		$t_p = 200\text{ }\mu\text{s}; \delta = 10\text{ }\%$	0.048	K/W
		$t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$	0.049	K/W
		$t_p = 100\text{ }\mu\text{s}; \delta = 20\text{ }\%$	0.056	K/W

## 6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 2.4\text{ mA}$	108	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 240\text{ mA}$	1.5	2.0	2.5	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}$	-	-	2.8	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	41	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 10\text{ V}; V_{DS} = 0\text{ V}$	-	-	280	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 8.5\text{ A}$	-	90	-	$\text{m}\Omega$

Table 7. RF characteristics

Test signal: pulsed RF;  $t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$ ; RF performance at  $V_{DS} = 50\text{ V}; I_{Dq} = 200\text{ mA}; T_{case} = 25\text{ °C}$ ; unless otherwise specified, in a class-AB production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_L = 750\text{ W}$	16.6	19	-	dB
$\eta_D$	drain efficiency	$P_L = 750\text{ W}$	55	62	-	%
$RL_{in}$	input return loss	$P_L = 750\text{ W}$	-	-10	-	dB
$P_{droop(pulse)}$	pulse droop power	$P_L = 750\text{ W}$	-	0.0	0.3	dB
$P_{L(1dB)}$	output power at 1 dB gain compression		650	700	-	W
$P_{L(2dB)}$	output power at 2 dB gain compression		-	800	-	W

## 7. Test information

### 7.1 Ruggedness in class-AB operation

The BLF13H9L750P and BLF13H9LS750P are capable of withstanding a load mismatch corresponding to  $V_{SWR} = 10 : 1$  through all phases under the following conditions:

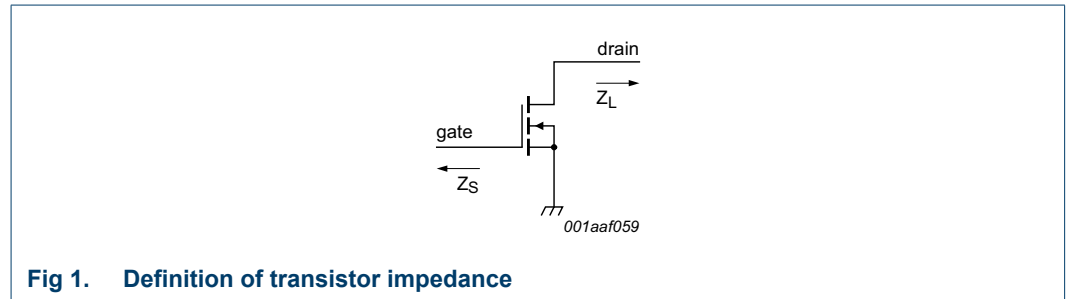
$V_{DS} = 50\text{ V}; I_{Dq} = 200\text{ mA}; P_L = 750\text{ W}; t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$ .

7.2 Impedance information

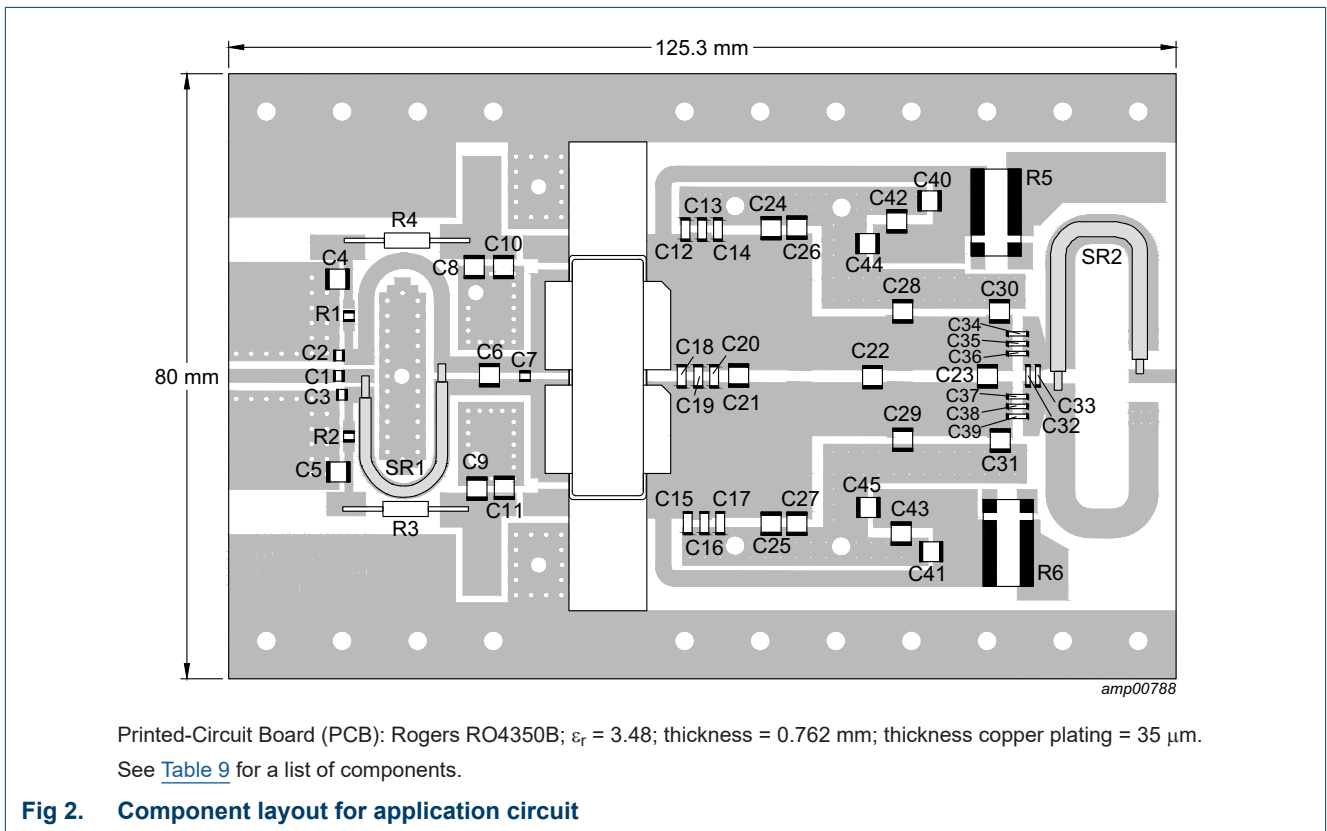
Table 8. Typical impedance (one section)

f (GHz)	Z <sub>S</sub> [1] (Ω)	Z <sub>L</sub> [1] (Ω)
1.3	3.1 – j5.5	0.95 – j0.5

[1] Z<sub>S</sub> and Z<sub>L</sub> defined in Figure 1.



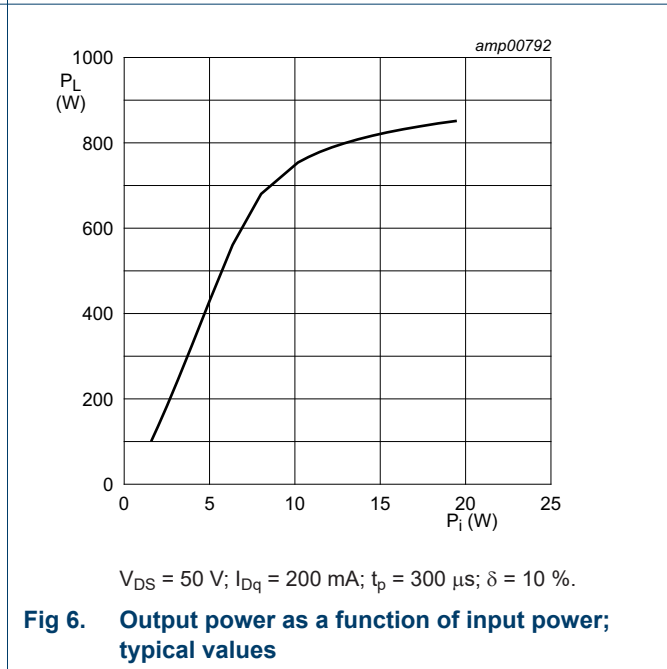
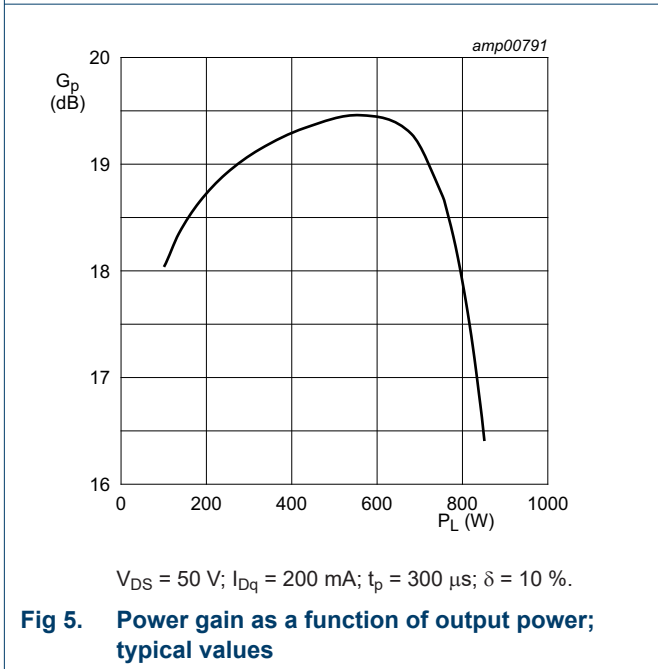
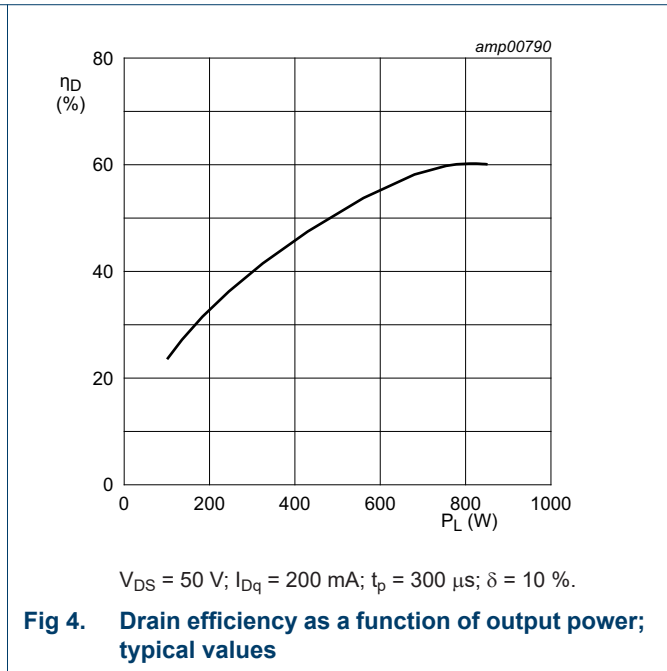
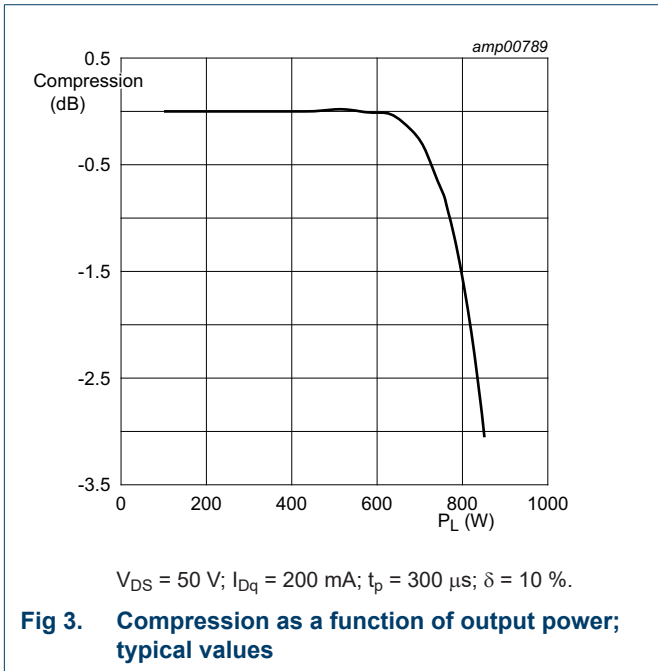
7.3 Test circuit

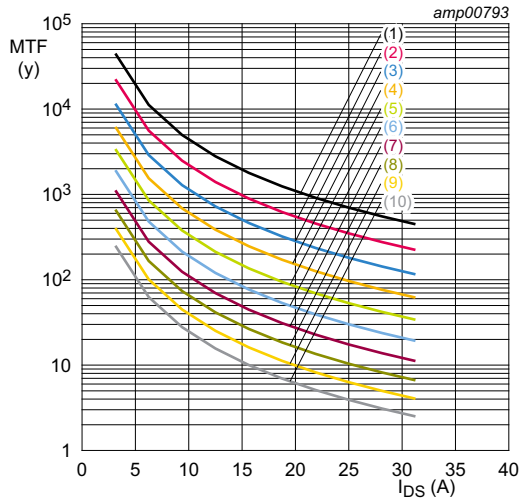


**Table 9. List of components**  
See [Figure 2](#) for component layout.

Component	Description	Value	Remarks
C1, C34, C35, C36	multilayer ceramic chip capacitor	62 pF	ATC 800B
C2, C3	multilayer ceramic chip capacitor	43 pF	ATC 800B
C4, C5	multilayer ceramic chip capacitor	4.7 $\mu$ F	TDK: C4532X7R1E475MT020U
C6	multilayer ceramic chip capacitor	4.3 pF	ATC 800B
C7	multilayer ceramic chip capacitor	3.6 pF	ATC 800B
C8, C9, C42, C43	multilayer ceramic chip capacitor	1.0 nF	ATC 100B
C10, C11, C44, C45	multilayer ceramic chip capacitor	10 $\mu$ F	Murata: GRM55DR61H106KA88L
C12, C13, C15, C16, C23	multilayer ceramic chip capacitor	2.0 pF	ATC 800B
C14, C17, C26, C27	multilayer ceramic chip capacitor	0.5 pF	ATC 800B
C18, C19	multilayer ceramic chip capacitor	2.2 pF	ATC 800B
C20	multilayer ceramic chip capacitor	1.9 pF	ATC 800B
C21, C22, C28, C29	multilayer ceramic chip capacitor	1.0 pF	ATC 100B
C24, C25	multilayer ceramic chip capacitor	0.3 pF	ATC 100B
C30, C31	multilayer ceramic chip capacitor	2.4 pF	ATC 800B
C32	multilayer ceramic chip capacitor	0.7 pF	ATC 800B
C33	multilayer ceramic chip capacitor	1.3 pF	ATC 800B
C37, C38, C39, C40, C41	multilayer ceramic chip capacitor	62 pF	ATC 800B
SR1	coax	25 $\Omega$ , 34 mm	
SR2	coax	35 $\Omega$ , 34 mm	UT-141C-35-TP
R1, R2	resistor	5.1 $\Omega$	SMD 0603
R3, R4	resistor	100 $\Omega$ , 0.6 W	
R5, R6	resistor	10 m $\Omega$	FC4L110R010FER

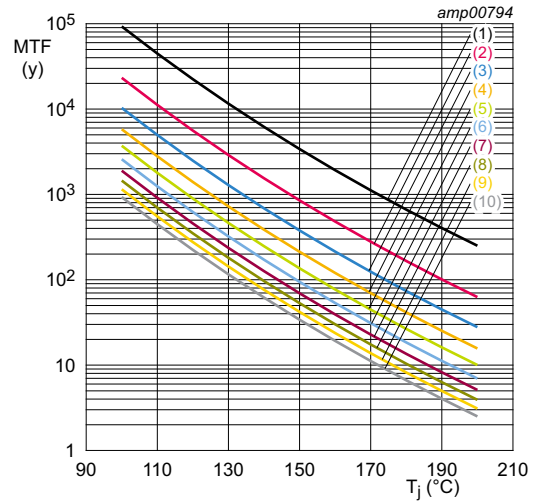
7.4 Graphical data





- (1)  $T_j = 110\text{ }^\circ\text{C}$
- (2)  $T_j = 120\text{ }^\circ\text{C}$
- (3)  $T_j = 130\text{ }^\circ\text{C}$
- (4)  $T_j = 140\text{ }^\circ\text{C}$
- (5)  $T_j = 150\text{ }^\circ\text{C}$
- (6)  $T_j = 160\text{ }^\circ\text{C}$
- (7)  $T_j = 170\text{ }^\circ\text{C}$
- (8)  $T_j = 180\text{ }^\circ\text{C}$
- (9)  $T_j = 190\text{ }^\circ\text{C}$
- (10)  $T_j = 200\text{ }^\circ\text{C}$

**Fig 7. MTF as a function of drain-source current; typical values**



- (1)  $I_{DS} = 3.13\text{ A}$
- (2)  $I_{DS} = 6.25\text{ A}$
- (3)  $I_{DS} = 9.38\text{ A}$
- (4)  $I_{DS} = 12.50\text{ A}$
- (5)  $I_{DS} = 15.63\text{ A}$
- (6)  $I_{DS} = 18.75\text{ A}$
- (7)  $I_{DS} = 21.88\text{ A}$
- (8)  $I_{DS} = 25.00\text{ A}$
- (9)  $I_{DS} = 28.13\text{ A}$
- (10)  $I_{DS} = 31.25\text{ A}$

**Fig 8. MTF as a function of junction temperature; typical values**

8. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads

SOT539A

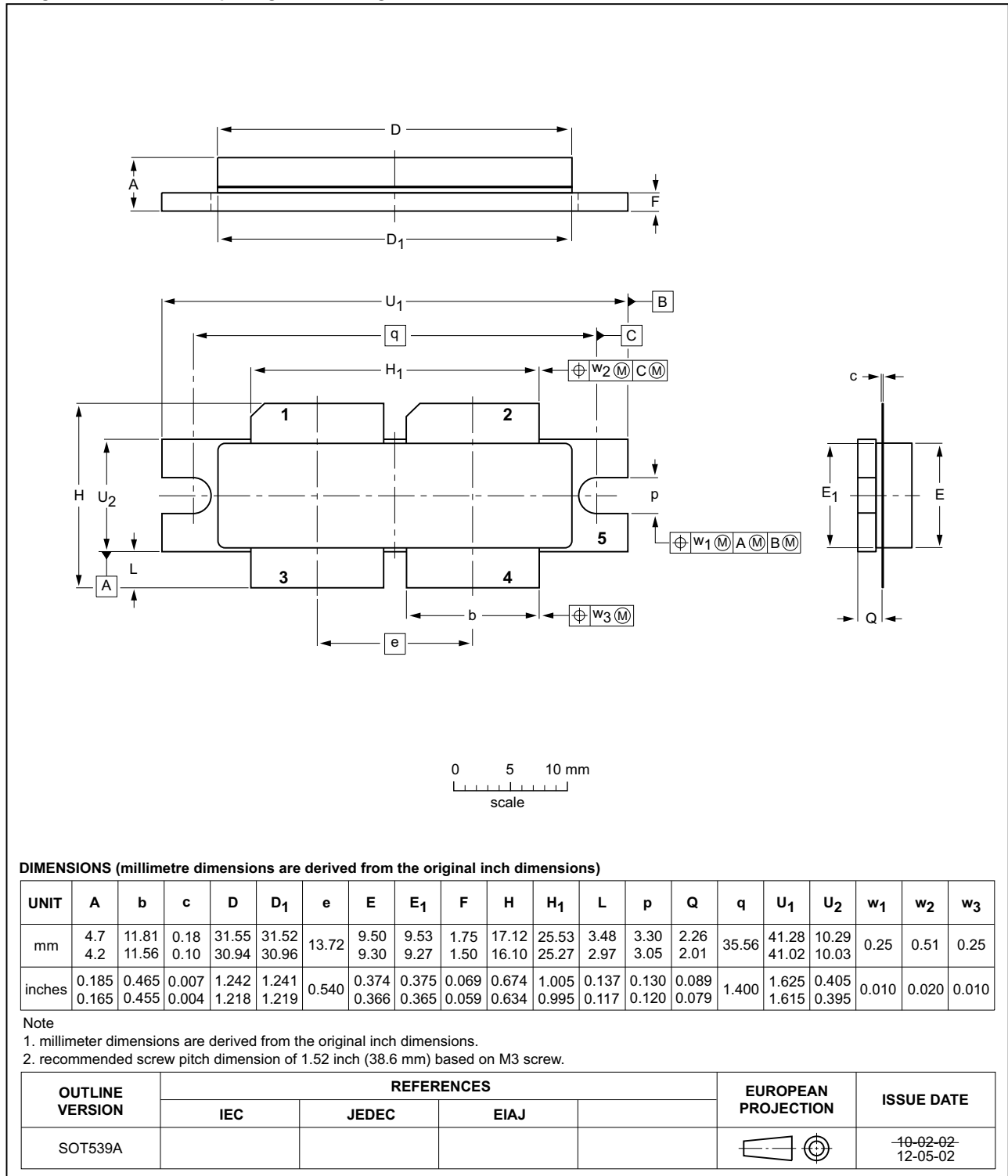


Fig 9. Package outline SOT539A

Earless flanged balanced ceramic package; 4 leads

SOT539B

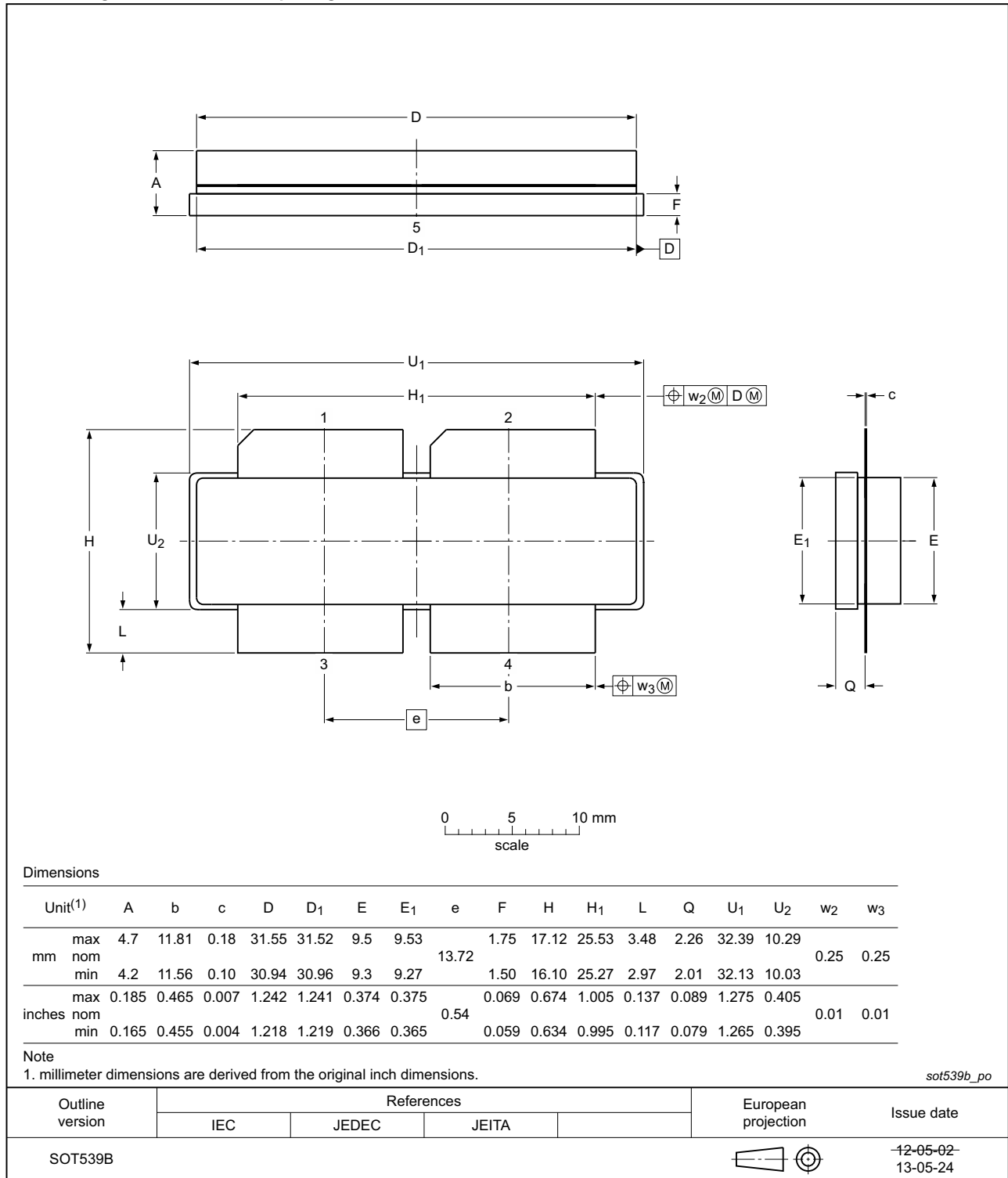



Fig 10. Package outline SOT539B

## 9. Handling information

CAUTION	
	<p>This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.</p> <p>Such precautions are described in the <i>ANSI/ESD S20.20</i>, <i>IEC/ST 61340-5</i>, <i>JESD625-A</i> or equivalent standards.</p>

**Table 10. ESD sensitivity**

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A <sup>[1]</sup>
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 <sup>[2]</sup>

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

## 10. Abbreviations

**Table 11. Abbreviations**

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VSWR	Voltage Standing Wave Ratio

## 11. Revision history

**Table 12. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF13H9L750P_13H9LS750P v.1	20180920	Product data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[2] The term 'short data sheet' is explained in section "Definitions".

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