THE DATASHEET OF

BLL9G1214L-600U

BLL9G1214L-600; BLL9G1214LS-600

LDMOS L-band radar power transistor

Rev. 2 — 6 November 2018

Product data sheet

1. Product profile

1.1 General description

600 W LDMOS power transistor for L-band radar applications in the frequency range from 1.2 GHz to 1.4 GHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C; t_p = 300 µs; δ = 10 %; I_{Dq} = 400 mA; in a class-AB demo test circuit.

Test signal	f	V_{DS}	$P_{L(3dB)}$	G_p	η_D
	(GHz)	(V)	(W)	(dB)	(%)
pulsed RF	1.2 to 1.4	32	600	19	60

1.2 Features and benefits

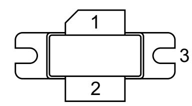
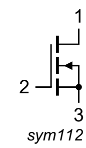
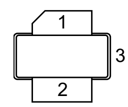
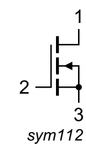
- High efficiency
- Excellent ruggedness
- Designed for L-band operation
- Excellent thermal stability
- Easy power control
- Integrated dual sided ESD protection enables excellent off-state isolation
- High flexibility with respect to pulse formats
- Internally matched for ease of use
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- L-band radar applications in the frequency range from 1.2 GHz to 1.4 GHz

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLL9G1214L-600 (SOT502A)			
1	drain		
2	gate		
3	source [1]		
BLL9G1214LS-600 (SOT502B)			
1	drain		
2	gate		
3	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLL9G1214L-600	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT502A
BLL9G1214LS-600	-	earless flanged ceramic package; 2 leads	SOT502B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Min	Max	Unit
V_{DS}	drain-source voltage	-	65	V
V_{GS}	gate-source voltage	–6	+13	V
T_{stg}	storage temperature	–65	+150	°C
T_j	junction temperature [1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability. For details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-mb)}$	transient thermal impedance from junction to mounting base	T_{case} = 85 °C; P_L = 600 W		
		t_p = 100 μs; δ = 10 %	0.11	K/W
		t_p = 300 μs; δ = 10 %	0.15	K/W
		t_p = 500 μs; δ = 10 %	0.17	K/W
		t_p = 100 μs; δ = 20 %	0.15	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 4.5 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 450 mA	1.5	2	2.5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	5	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	87	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	400	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 450 mA	-	4.2	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 15.75 A	-	0.026	-	Ω

Table 7. RF characteristics

Test signal: pulsed RF; t_p = 300 μs; δ = 10 %; RF performance at V_{DS} = 32 V; I_{Dq} = 400 mA; T_{case} = 25 °C; unless otherwise specified, in a class-AB production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 600 W	16.8	19	-	dB
η_D	drain efficiency	P_L = 600 W	56	60	-	%
RL_{in}	input return loss	P_L = 600 W	-	−7	-	dB
$P_{droop(pulse)}$	pulse droop power	P_L = 600 W	-	0.2	0.5	dB
t_r	rise time	P_L = 600 W	-	6	50	ns
t_f	fall time	P_L = 600 W	-	6	50	ns
$P_{L(2dB)}$	output power at 2 dB gain compression		-	575	-	W

7. Test information

7.1 Ruggedness in class-AB operation

The BLL9G1214L-600 and BLL9G1214LS-600 are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 32 V; I_{Dq} = 400 mA; P_L = 600 W; t_p = 300 μs; δ = 10 %.

7.2 Impedance information

Table 8. Typical impedance

f	Z_S	Z_L
(GHz)	(Ω)	(Ω)
1.2	1.23 – j5.79	1.14 – j1.39
1.3	7.10 – j3.33	1.62 – j1.63
1.4	1.31 – j1.89	2.36 – j1.56

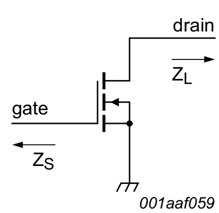
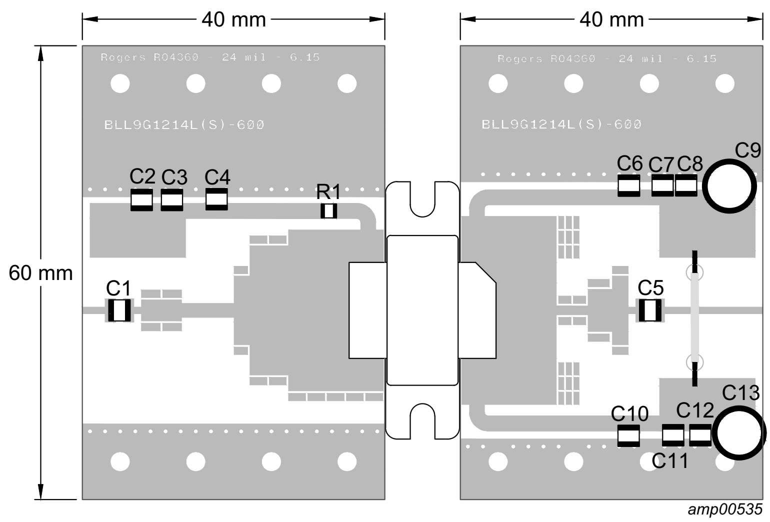


Fig 1. Definition of transistor impedance

7.3 Test circuit



Printed-Circuit Board (PCB): Rogers 4360; thickness = 0.61 mm; ε_r = 6.15; thickness of copper plating = 35 μm

See Table 9 for a list of components.

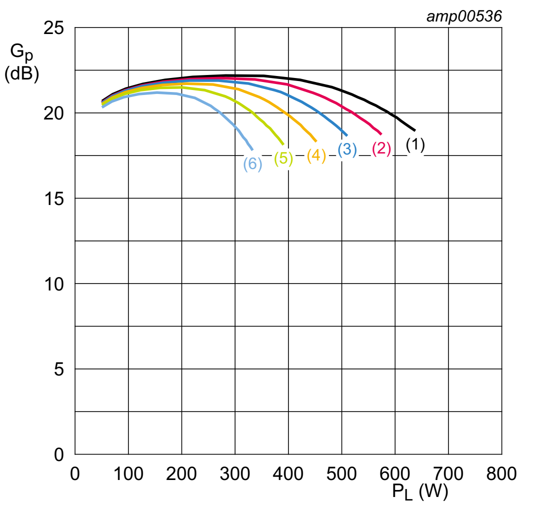
Fig 2. Component layout for class-AB production test circuit

Table 9. List of components

For test circuit see Figure 2.

Component	Description	Value	Remarks
C1, C4, C5, C6, C10	multilayer ceramic chip capacitor	56 pF	ATC 100B
C2, C8, C12	multilayer ceramic chip capacitor	10 μF	Murata: GRM55DR61H106KA88L
C3, C7, C11	multilayer ceramic chip capacitor	910 pF	ATC 100B
C9, C13	electrolytic capacitor	100 μF, 63 V	
R1	resistor	5 Ω	SMD 0603

7.4 Graphical data



I_{Dq} = 400 mA; t_p = 300 μs; δ = 10 %; f = 1300 MHz.

(1) V_{DS} = 32 V

(2) V_{DS} = 30 V

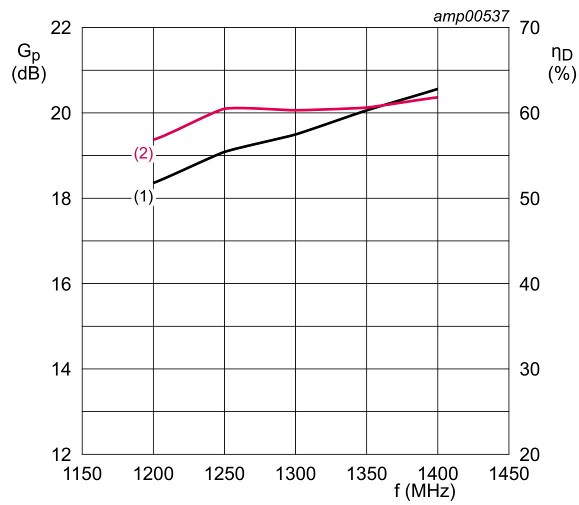
(3) V_{DS} = 28 V

(4) V_{DS} = 26 V

(5) V_{DS} = 24 V

(6) V_{DS} = 22 V

Fig 3. Power gain as a function of output power; typical values

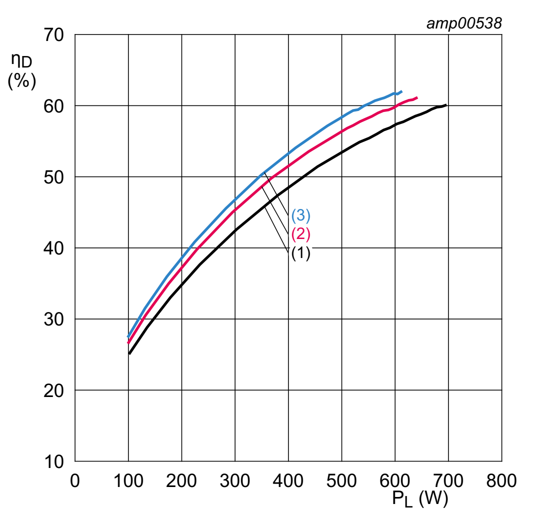


V_{DS} = 32 V; I_{Dq} = 400 mA; t_p = 300 μs; δ = 10 %; P_L = 600 W.

(1) gain

(2) efficiency

Fig 4. Power gain and drain efficiency as function of frequency; typical values



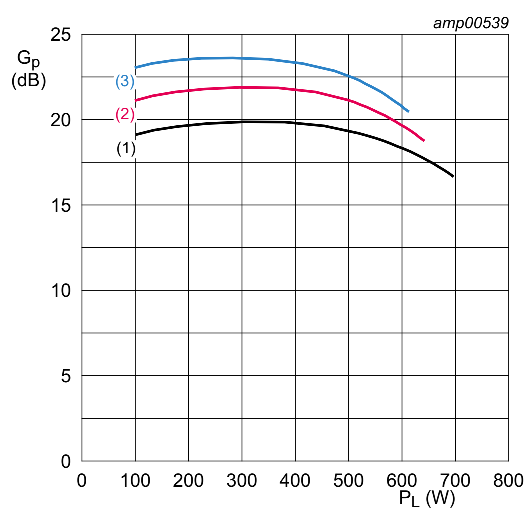
V_{DS} = 32 V; I_{Dq} = 400 mA; t_p = 300 μs; δ = 10 %.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 5. Drain efficiency as a function of output power; typical values



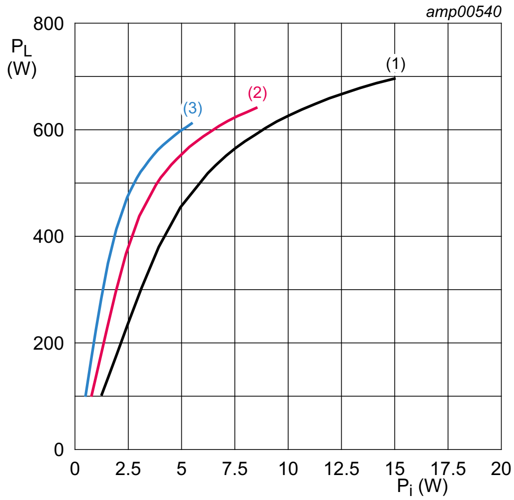
V_{DS} = 32 V; I_{Dq} = 400 mA; t_p = 300 μs; δ = 10 %.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 6. Power gain as a function of output power; typical values



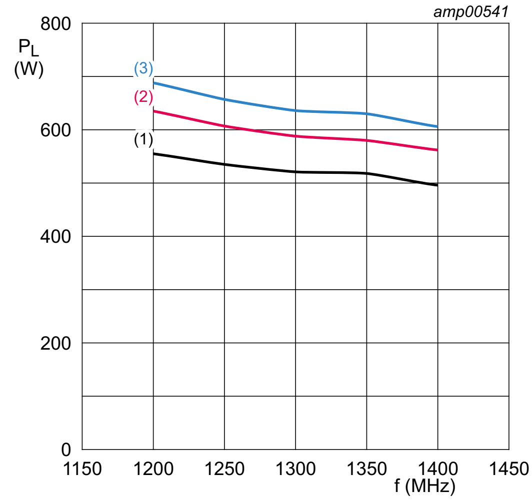
V_{DS} = 32 V; I_{Dq} = 400 mA; t_p = 300 μs; δ = 10 %.

(1) f = 1200 MHz

(2) f = 1300 MHz

(3) f = 1400 MHz

Fig 7. Output power as a function of input power; typical values



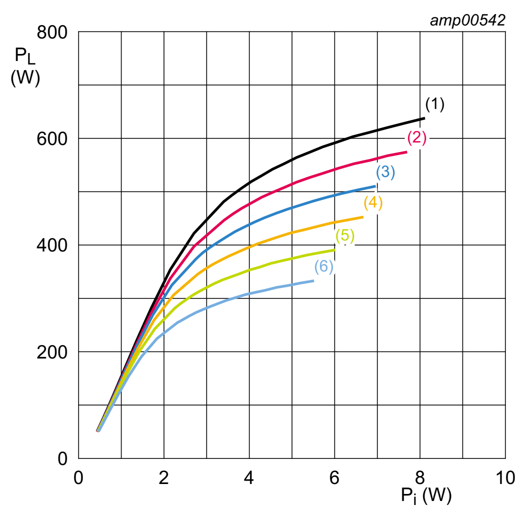
V_{DS} = 32 V; I_{Dq} = 400 mA; t_p = 300 μs; δ = 10 %.

(1) $P_{L(1dB)}$

(2) $P_{L(2dB)}$

(3) $P_{L(3dB)}$

Fig 8. Output power as a function of frequency; typical values



I_{Dq} = 400 mA; t_p = 300 μs; δ = 10 %; f = 1300 MHz.

(1) V_{DS} = 32 V

(2) V_{DS} = 30 V

(3) V_{DS} = 28 V

(4) V_{DS} = 26 V

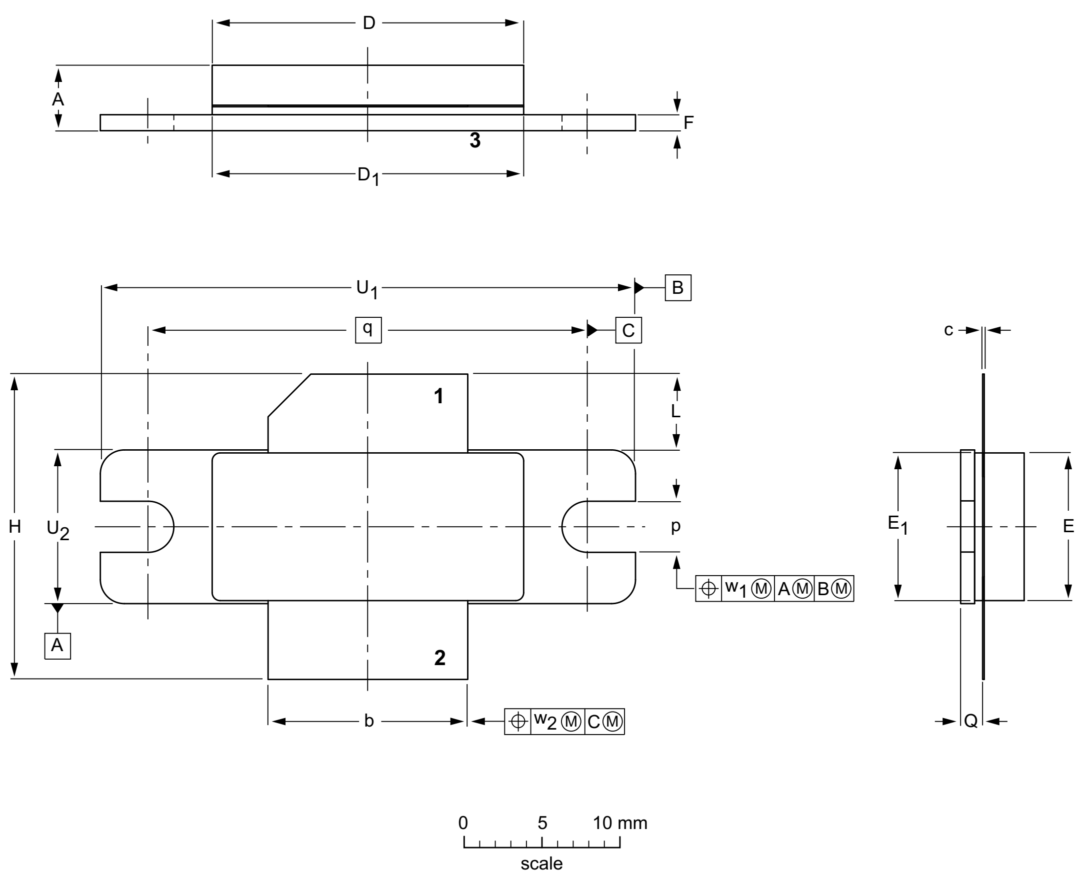
(5) V_{DS} = 24 V

(6) V_{DS} = 22 V

Fig 9. Output power as a function of input power; typical values

8. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads **SOT502A**



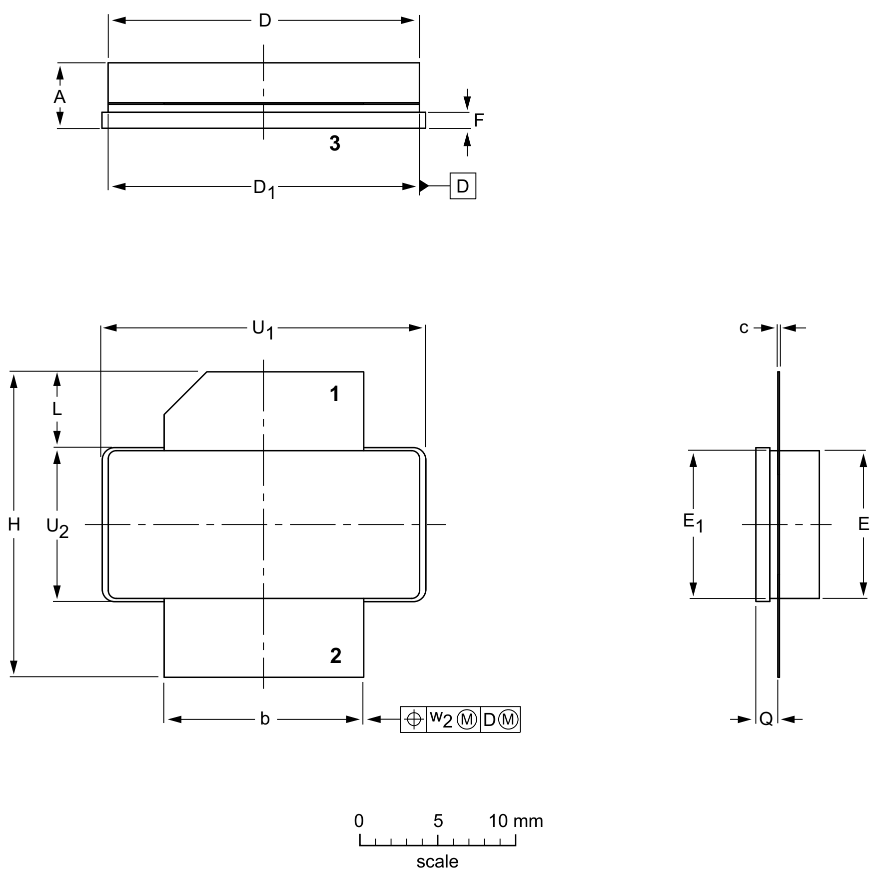
DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	w_1	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502A						~~03-01-10~~ 12-05-02

Fig 10. Package outline SOT502A

Earless flanged ceramic package; 2 leads **SOT502B**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502B						~~07-05-09~~ 12-05-02

Fig 11. Package outline SOT502B

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 10. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
L-band	Long wave Band
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLL9G1214L-600_LS-600 v.2	20181106	Product data sheet	-	BLL9G1214L-600_LS-600 v.1
Modifications	• Figure 4 on page 6: corrected value P_L to 600 W			
BLL9G1214L-600_LS-600 v.1	20171127	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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