



**THE DATASHEET OF  
BSZ440N10NS3GATMA1**



## MOSFET

Metal Oxide Semiconductor Field Effect Transistor

## OptiMOS™

OptiMOS™3 Power-Transistor, 100 V  
BSZ440N10NS3 G

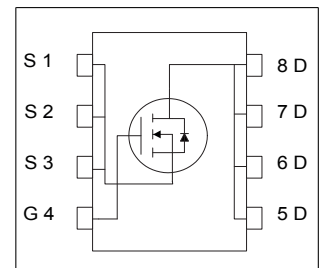
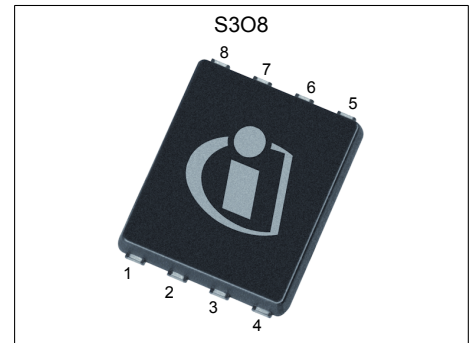
## Data Sheet

Rev. 2.1  
Final

## 1 Description

### Features

- Very low gate charge for high frequency applications
- Optimized for dc-dc conversion
- N-channel, normal level
- Excellent gate charge x  $R_{DS(on)}$  product (FOM)
- Very low on-resistance  $R_{DS(on)}$
- 150 °C operating temperature
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC<sup>1)</sup> for target application
- Halogen-free according to IEC61249-2-21



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	100	V
$R_{DS(on),max}$	44	mΩ
$I_D$	18	A



Type / Ordering Code	Package	Marking	Related Links
BSZ440N10NS3 G	PG-TSDSON-8	440N10N	-

<sup>1)</sup> J-STD20 and JESD22

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## 2 Maximum ratings

at  $T_j = 25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**  
at 25 °C

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	$I_D$	-	-	18 11 5.3	A	$T_C=25\text{ °C}$ $T_C=100\text{ °C}$ $T_A=25\text{ °C}, R_{thJA}=50\text{ K/W}^1)$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	72	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	17	mJ	$I_D=12\text{ A}, R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	29	W	$T_C=25\text{ °C}$
Operating and storage temperature	$T_j, T_{stg}$	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

## 3 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	4.3	K/W	-
Thermal resistance, junction - ambient, 6 cm <sup>2</sup> cooling area <sup>1)</sup>	$R_{thJA}$	-	-	50	K/W	-

<sup>1)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

<sup>2)</sup> see figure 3

## 4 Electrical characteristics

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2	2.7	3.5	V	$V_{DS}=V_{GS}$ , $I_D=12\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.01 10	1 100	$\mu\text{A}$	$V_{DS}=100\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ }^\circ\text{C}$ $V_{DS}=100\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ }^\circ\text{C}$
Gate-source leakage current	$I_{GSS}$	-	1	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	38 48	44 86	m $\Omega$	$V_{GS}=10\text{ V}$ , $I_D=12\text{ A}$ $V_{GS}=6\text{ V}$ , $I_D=6\text{ A}$
Gate resistance	$R_G$	-	1.5	-	$\Omega$	-
Transconductance	$g_{fs}$	8	15	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$ , $I_D=12\text{ A}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance <sup>1)</sup>	$C_{iss}$	-	480	640	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=50\text{ V}$ , $f=1\text{ MHz}$
Output capacitance <sup>1)</sup>	$C_{oss}$	-	87	120	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=50\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance	$C_{riss}$	-	6	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=50\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	4.3	-	ns	$V_{DD}=50\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=6\text{ A}$ , $R_G=1.6\text{ }\Omega$
Rise time	$t_r$	-	1.8	-	ns	$V_{DD}=50\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=6\text{ A}$ , $R_G=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	9.1	-	ns	$V_{DD}=50\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=6\text{ A}$ , $R_G=1.6\text{ }\Omega$
Fall time	$t_f$	-	2.0	-	ns	$V_{DD}=50\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=6\text{ A}$ , $R_G=1.6\text{ }\Omega$

**Table 6 Gate charge characteristics<sup>2)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	2.2	-	nC	$V_{DD}=50\text{ V}$ , $I_D=6\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	$Q_{gd}$	-	1.3	-	nC	$V_{DD}=50\text{ V}$ , $I_D=6\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	$Q_{sw}$	-	2.0	-	nC	$V_{DD}=50\text{ V}$ , $I_D=6\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total <sup>1)</sup>	$Q_g$	-	6.8	9.1	nC	$V_{DD}=50\text{ V}$ , $I_D=6\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	4.5	-	V	$V_{DD}=50\text{ V}$ , $I_D=6\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Output charge <sup>1)</sup>	$Q_{oss}$	-	9.0	12	nC	$V_{DD}=50\text{ V}$ , $V_{GS}=0\text{ V}$

<sup>1)</sup> Defined by design. Not subject to production test.

<sup>2)</sup> See "Gate charge waveforms" for parameter definition

**Table 7 Reverse diode**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	18	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	72	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	1	1.2	V	$V_{GS}=0\text{ V}, I_F=18\text{ A}, T_J=25\text{ °C}$
Reverse recovery time	$t_{rr}$	-	44	-	ns	$V_R=50\text{ V}, I_F=6\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	$Q_{rr}$	-	61	-	nC	$V_R=50\text{ V}, I_F=6\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$

## 5 Electrical characteristics diagrams

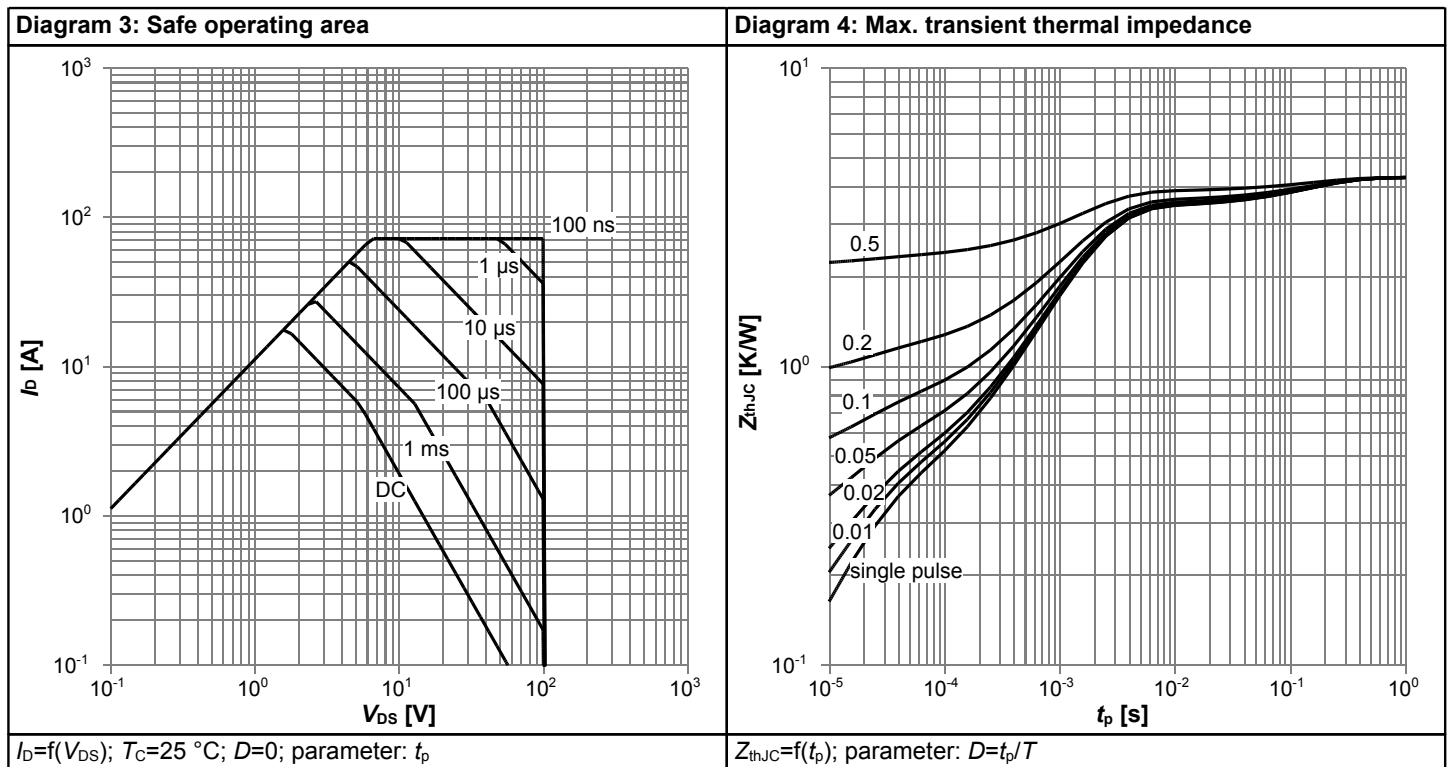
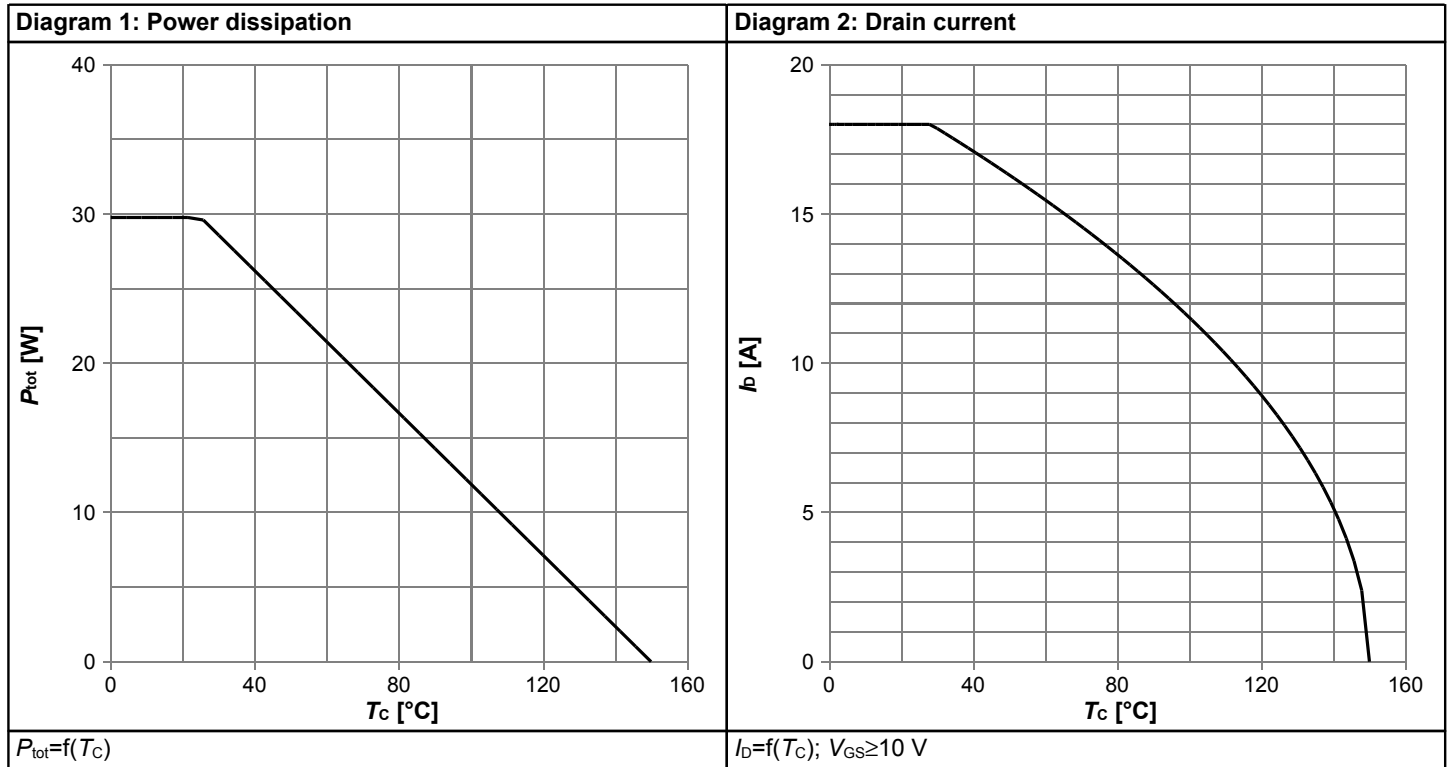
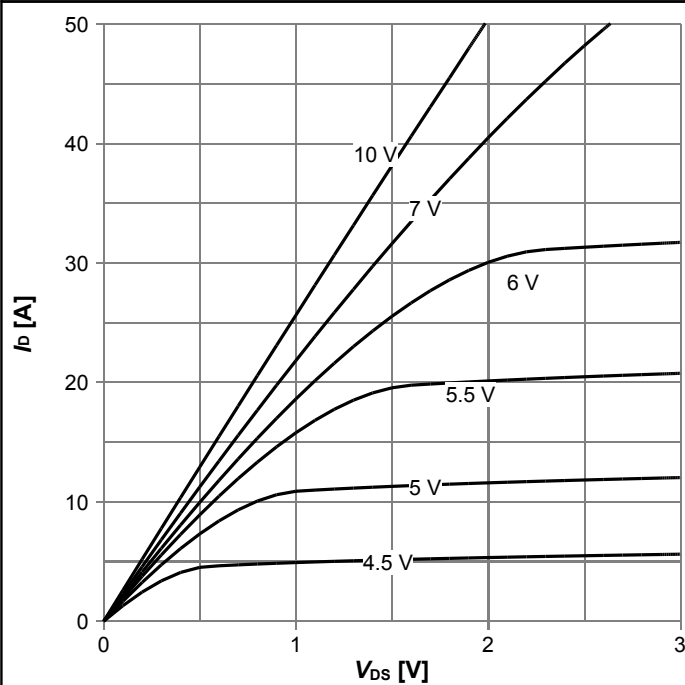
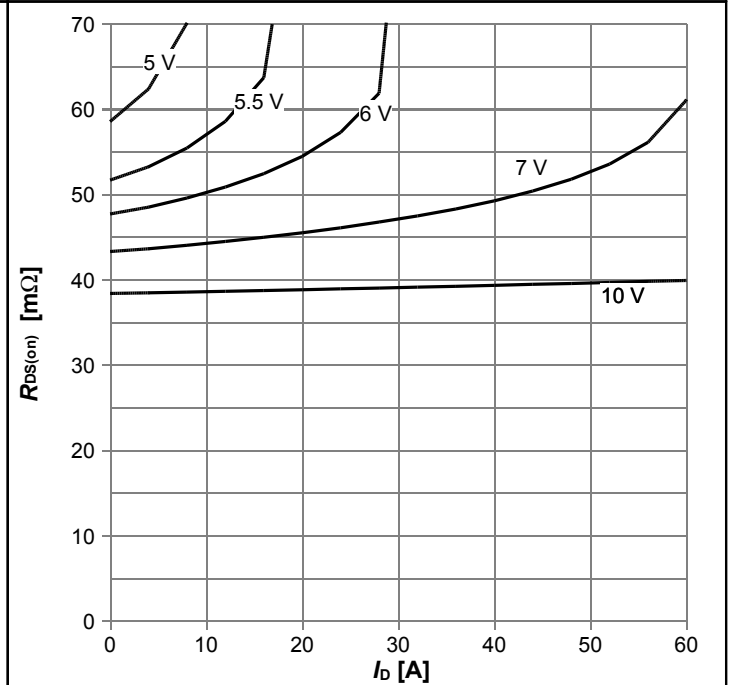


Diagram 5: Typ. output characteristics



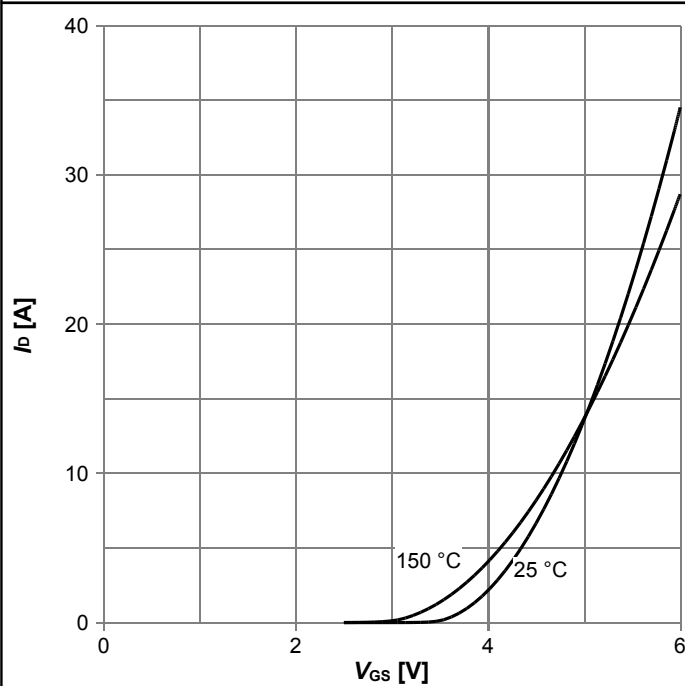
$I_D=f(V_{DS}); T_j=25\text{ }^\circ\text{C};$  parameter:  $V_{GS}$

Diagram 6: Typ. drain-source on resistance



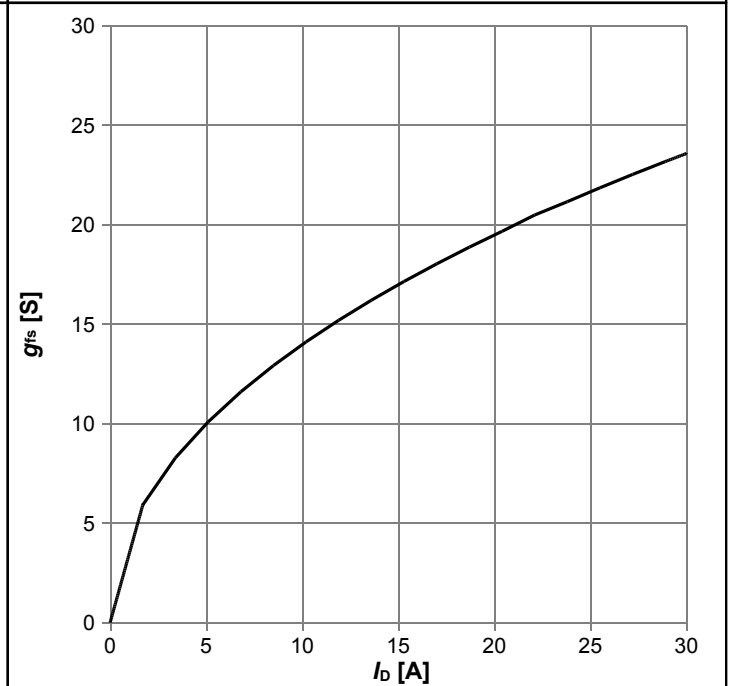
$R_{DS(on)}=f(I_D); T_j=25\text{ }^\circ\text{C};$  parameter:  $V_{GS}$

Diagram 7: Typ. transfer characteristics



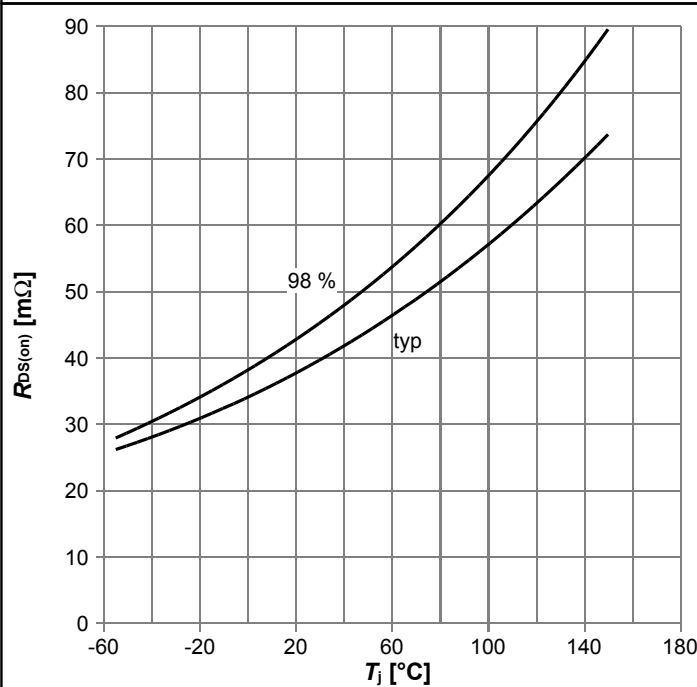
$I_D=f(V_{GS}); |V_{DS}|>2|I_D|R_{DS(on)max};$  parameter:  $T_j$

Diagram 8: Typ. forward transconductance



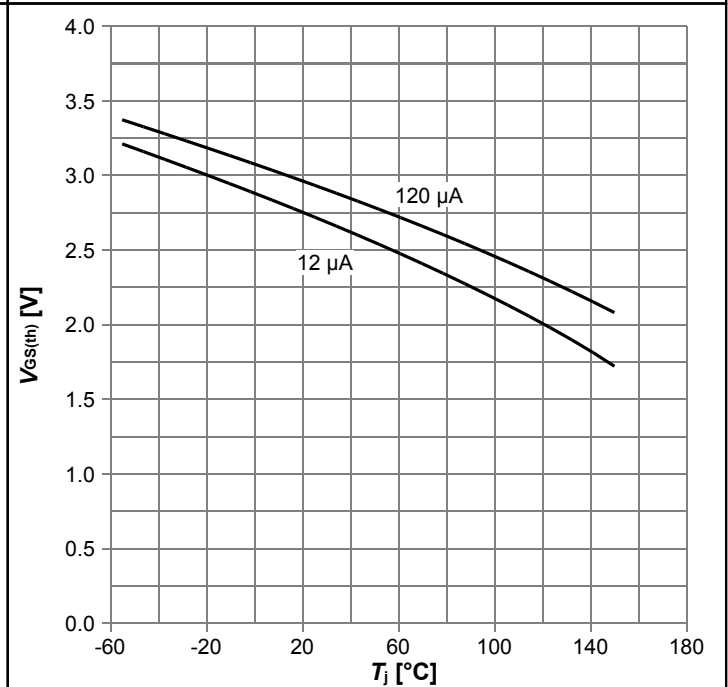
$g_{fs}=f(I_D); T_j=25\text{ }^\circ\text{C}$

Diagram 9: Drain-source on-state resistance



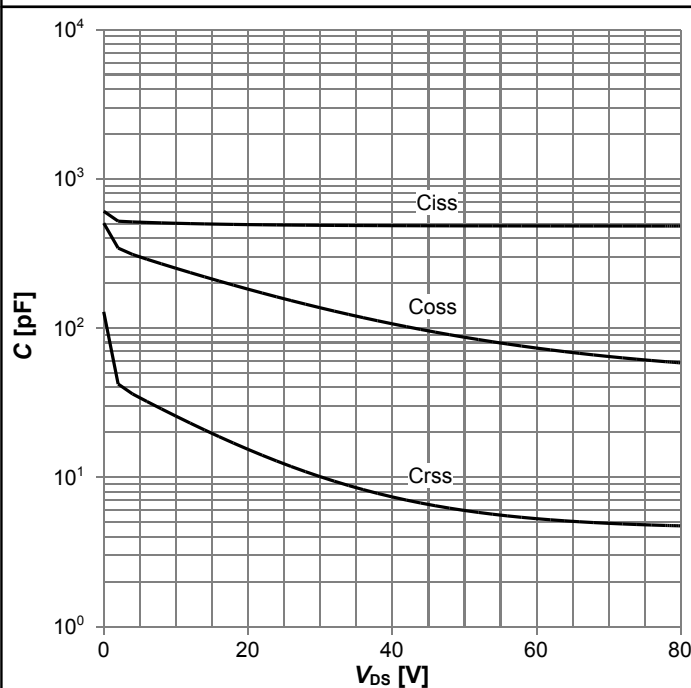
$R_{DS(on)}=f(T_j)$ ;  $I_D=12\text{ A}$ ;  $V_{GS}=10\text{ V}$

Diagram 10: Typ. gate threshold voltage



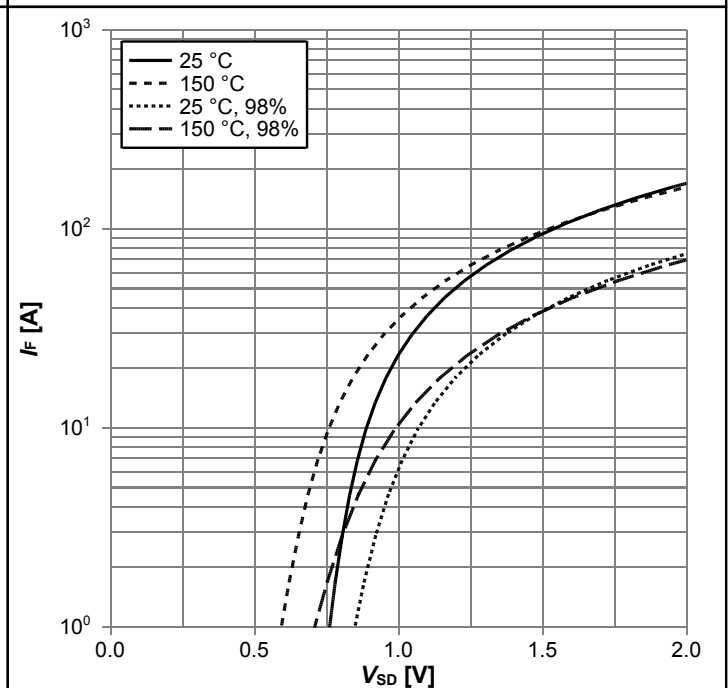
$V_{GS(th)}=f(T_j)$ ;  $V_{GS}=V_{DS}$ ; parameter:  $I_D$

Diagram 11: Typ. capacitances



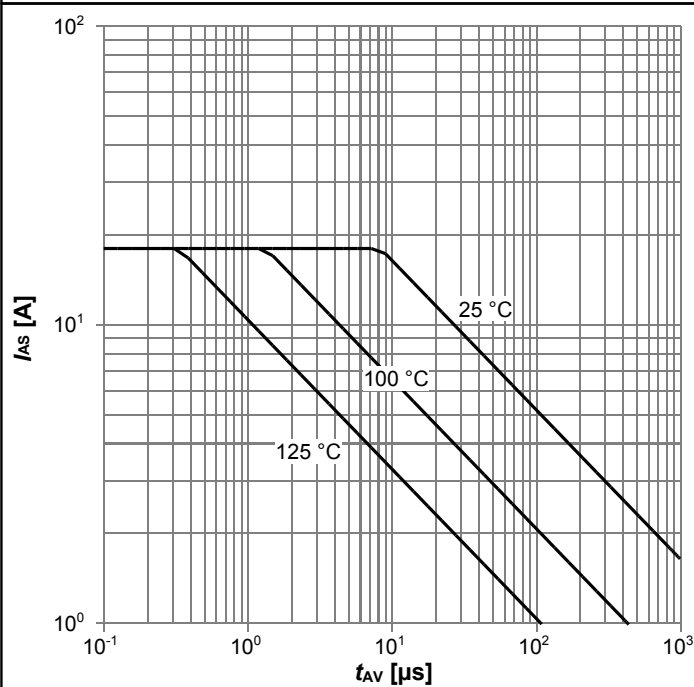
$C=f(V_{DS})$ ;  $V_{GS}=0\text{ V}$ ;  $f=1\text{ MHz}$

Diagram 12: Forward characteristics of reverse diode



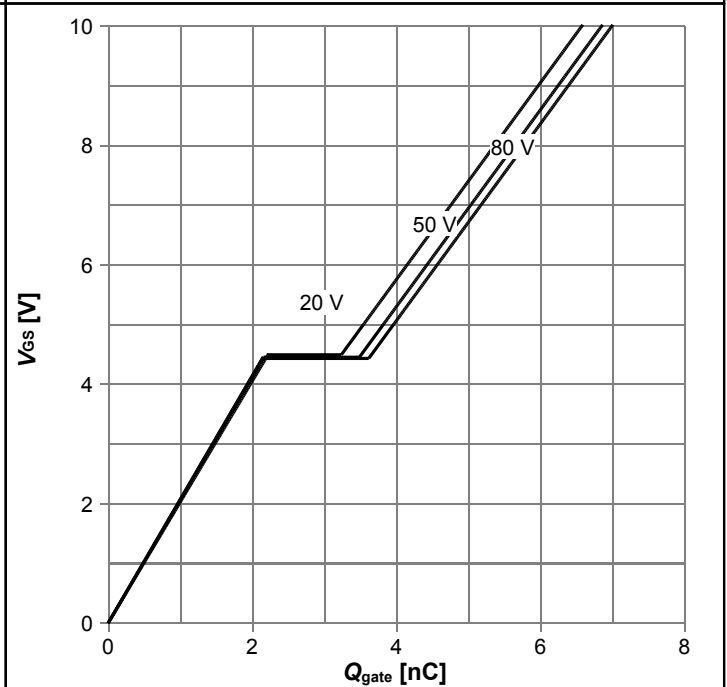
$I_F=f(V_{SD})$ ; parameter:  $T_j$

Diagram 13: Avalanche characteristics



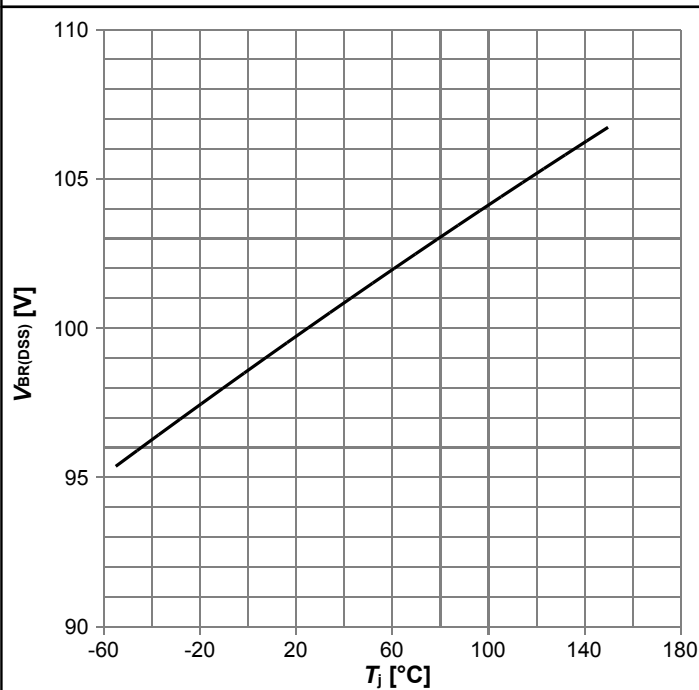
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$ ; parameter:  $T_{j(start)}$

Diagram 14: Typ. gate charge



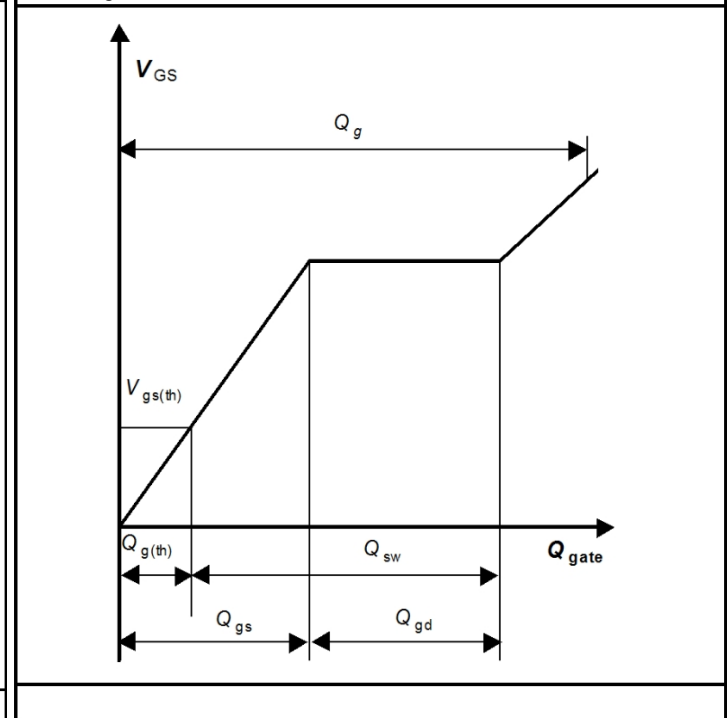
$V_{GS}=f(Q_{gate}); I_D=6$  A pulsed; parameter:  $V_{DD}$

Diagram 15: Drain-source breakdown voltage

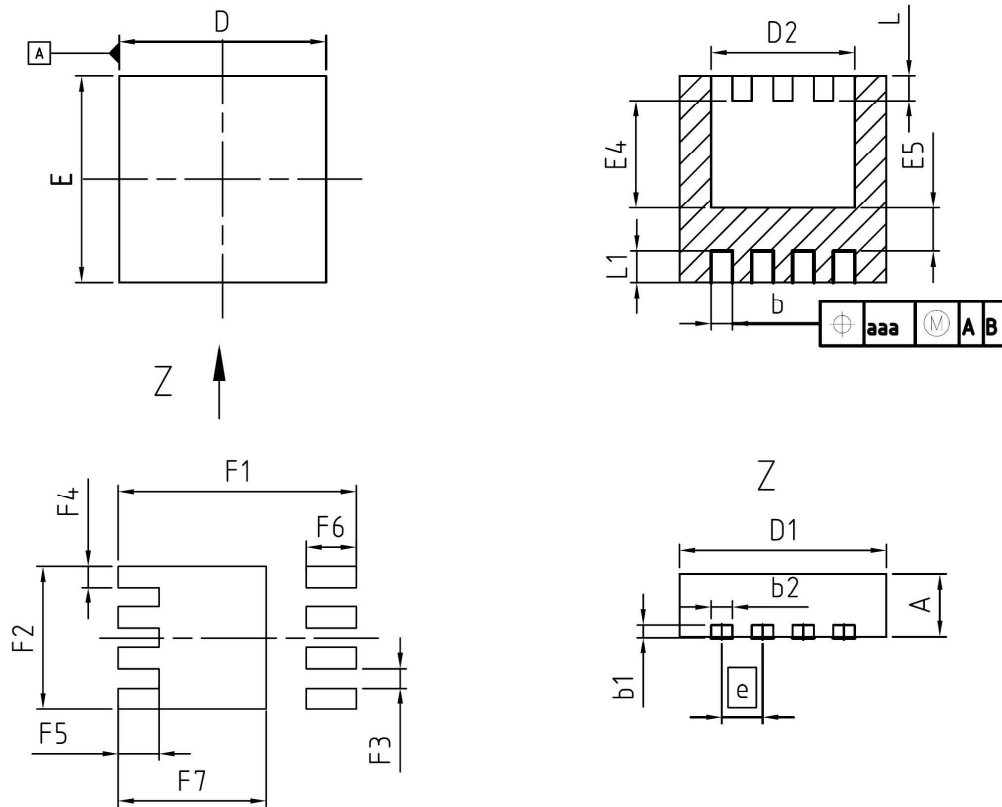


$V_{BR(DSS)}=f(T_j); I_D=1$  mA

Gate charge waveforms



## 6 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.24	0.44	0.009	0.017
b1	0.10	0.30	0.004	0.012
b2	0.20	0.44	0.008	0.017
D=D1	3.20	3.40	0.126	0.134
D2	2.15	2.45	0.085	0.096
E	3.20	3.40	0.126	0.134
E4	1.60	1.81	0.063	0.071
E5	0.59	0.86	0.023	0.034
e	0.65		0.026	
N	8		8	
L	0.30	0.56	0.012	0.022
L1	0.33	0.60	0.013	0.024
aaa	0.25		0.010	
F1	3.80		0.150	
F2	2.29		0.090	
F3	0.31		0.012	
F4	0.34		0.013	
F5	0.65		0.026	
F6	0.80		0.031	
F7	2.36		0.093	

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REVISION  
02

Figure 1 Outline PG-TSDSON-8, dimensions in mm/inches

## Revision History

BSZ440N10NS3 G

**Revision: 2015-02-06, Rev. 2.1**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.1	2015-02-06	Insert pin numbered package drawing and trr and Qrr values

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