THE DATASHEET OF

CHL8103-11CRT

FEATURES

- Dual output 2/3/4+1-phase PWM Controller (CHL8102/03/04) and single output 3-phase PWM Controller (CHL8113)
- Easiest layout and fewest pins in the industry
- Footprint compatible with CHL8325A/B (CHL8103/4)
- Fully supports Intel® VR12 (CHL8103/04/13) and AMD® SVI with dual OCP & programmable addressing (CHL8103/04)
- I2C interface for configuration & telemetry
- Pin programmable I2C address (CHL8103/04/13)
- Overclocking support with I2C voltage override and Vmax setting
- Flexible I2C bus security features
- I2C security enable pin (CHL8103/04/13)
- Independent loop switching frequencies from 200kHz to 1.2MHz per phase
- IR Efficiency Shaping with Dynamic Phase Control (DPC)
- 1-phase & Active Diode Emulation modes for light load efficiency
- IR Adaptive Transient Algorithm (ATA) on both loops minimizes output bulk capacitors and system cost
- Per-Loop Fault Protection: OVP, UVP, OCP
- Thermal Protection (OTP) and VRHOT# flag (CHL8103/04/13)
- Multiple time programmable (MTP) memory for custom configuration
- Compatible with IR ATL and 3.3V tri-state Drivers
- 3.3V +10%/-15% supply voltage; 0ºC to 85ºC operation
- Pb-Free, RoHS, QFN packages

APPLICATIONS

- Intel® VR12 & AMD® SVI based systems
- High Performance Desktops CPU VRs
- Value Servers CPU & DDR Memory VRs

DESCRIPTION

The CHL8102/03/04 are dual-loop, digital multi-phase buck controllers designed for CPU voltage regulation. The CHL8113 is a single-loop, digital multiphase buck controller ideal for Server DDR memory voltage regulation. They are fully compliant with the Intel® VR12 and AMD® SVI (CHL8103/04) specifications.

The CHL8102/03/04/13 includes IR Efficiency Shaping Technology to deliver exceptional efficiency at minimum cost across the entire load range. IR Dynamic Phase Control adds/drops active phases based upon load current and can be configured to enter 1-phase operation and diode emulation mode automatically or by command.

IR's unique Adaptive Transient Algorithm (ATA), based on proprietary non-linear digital PWM algorithms, minimizes output bulk capacitors and Multiple Time Programmable (MTP) storage saves pins and enables a small package size. Device configuration and fault parameters are easily defined using the IR Digital Power Design Center (DPDC) GUI and stored in on-chip MTP.

The CHL8102/03/04/13 provides extensive OVP, UVP, OCP and OTP fault protection and the CHL8103/04/13 includes thermistor based temperature sensing with VRHOT signal.

The CHL8102/03/04/13 includes numerous features like register diagnostics for fast design cycles and platform differentiation, truly simplifying VRD design and enabling fastest time-to-market (TTM) with "set-and-forget" methodology.

PIN DIAGRAM

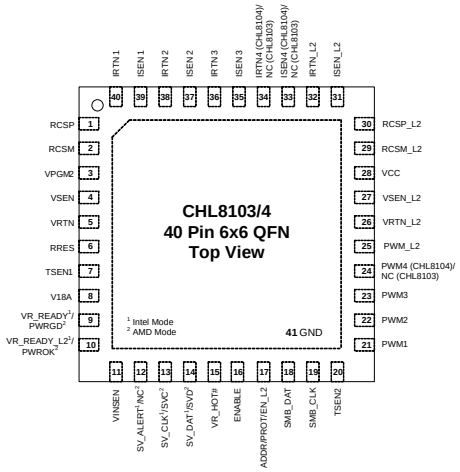
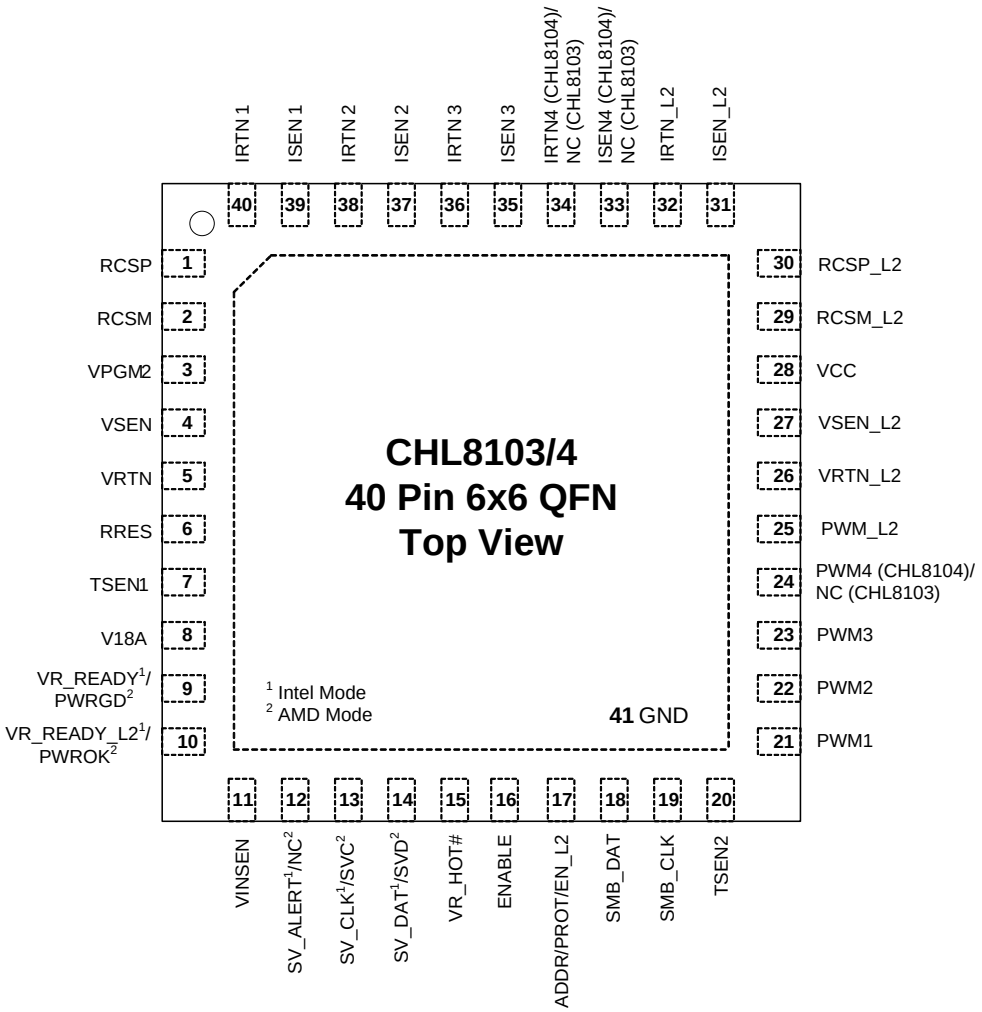


Figure 1: CHL8103/04 Package Top View

PIN DIAGRAM ENLARGED



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