



**THE DATASHEET OF
DMN2008LFU-7**



DUAL N-CHANNEL ENHANCEMENT MODE MOSFET
Product Summary

BV _{DSS}	R _{DS(ON)} Max	I _D MAX T _A = +25°C
20V	5.4mΩ @ V _{GS} = 4.5V	14.5A
	6.2mΩ @ V _{GS} = 4.0V	13.5A
	6.4mΩ @ V _{GS} = 3.7V	13.0A
	7.5mΩ @ V _{GS} = 3.1V	12.0A
	9.6mΩ @ V _{GS} = 2.5V	10.5A

Features

- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- ESD Protected Gate
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Description

This new generation MOSFET is designed to minimize the on-state resistance (R_{DS(ON)}), yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- Power Management Functions
- Battery Pack
- Load Switch

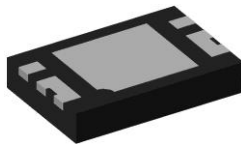
Mechanical Data

- Case: U-DFN2030-6 (Type B)
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: – NiPdAu over Copper Leadframe. Solderable per MIL-STD-202, Method 208 ^(e4)
- Terminal Connections: See Diagram Below
- Weight: 0.012 grams (Approximate)

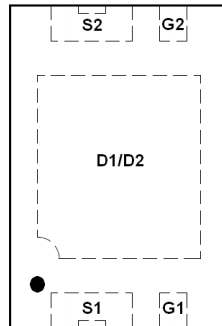
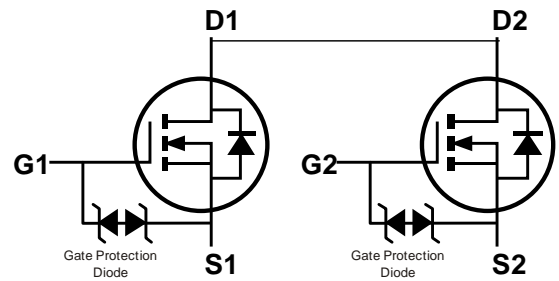


ESD PROTECTED

U-DFN2030-6 (Type B)



Bottom View


 Top View
Pin-Out


Equivalent Circuit

Ordering Information (Note 4)

Part Number	Case	Packaging
DMN2008LFU-7	U-DFN2030-6 (Type B)	3,000/Tape & Reel
DMN2008LFU-13	U-DFN2030-6 (Type B)	10,000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information


N28 = Product Type Marking Code
 YYWW = Date Code Marking
 YY = Last Two Digits of Year (ex: 18 for 2018)
 WW = Week Code (01 to 53)

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	20	V
Gate-Source Voltage	V_{GSS}	± 12	V
Continuous Drain Current (Note 6) $V_{GS} = 4.5\text{V}$	I_D	$T_A = +25^\circ\text{C}$ Steady State	14.5
		$T_A = +70^\circ\text{C}$	11.5
Maximum Continuous Body Diode Forward Current (Note 6)	I_S	2.2	A
Pulsed Drain Current (10 μs Pulse, Duty Cycle = 1%)	I_{DM}	75	A
Avalanche Current (Note 7) $L = 0.1\text{mH}$	I_{AS}	10	A
Avalanche Energy (Note 7) $L = 0.1\text{mH}$	E_{AS}	20	mJ

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P_D	1.0	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	123	$^\circ\text{C/W}$
Total Power Dissipation (Note 6)	P_D	1.7	W
Thermal Resistance, Junction to Ambient (Note 6)	$R_{\theta JA}$	73	$^\circ\text{C/W}$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12	$^\circ\text{C/W}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	20	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
Zero Gate Voltage Drain Current $T_J = +25^\circ\text{C}$	I_{DSS}	—	—	1.0	μA	$V_{DS} = 16\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 9.6\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(TH)}$	0.5	—	1.5	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(ON)}$	3.5	4.7	5.4	m Ω	$V_{GS} = 4.5\text{V}, I_D = 5.5\text{A}$
		3.6	4.8	6.2		$V_{GS} = 4.0\text{V}, I_D = 5.5\text{A}$
		3.7	4.9	6.4		$V_{GS} = 3.7\text{V}, I_D = 5.5\text{A}$
		3.8	5.1	7.5		$V_{GS} = 3.1\text{V}, I_D = 5.5\text{A}$
		3.9	5.7	9.6		$V_{GS} = 2.5\text{V}, I_D = 5.5\text{A}$
Diode Forward Voltage	V_{SD}	—	0.7	1.2	V	$V_{GS} = 0\text{V}, I_S = 11\text{A}$
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{ISS}	—	1,418	—	pF	$V_{DS} = 10\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Output Capacitance	C_{OSS}	—	323	—	pF	
Reverse Transfer Capacitance	C_{RSS}	—	106	—	pF	
Gate Resistance	R_g	—	465	—	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$
Total Gate Charge ($V_{GS} = 4.5\text{V}$)	Q_g	—	18.7	—	nC	
Total Gate Charge ($V_{GS} = 10\text{V}$)	Q_{g10}	—	42.3	—	nC	
Gate-Source Charge	Q_{gs}	—	3.2	—	nC	
Gate-Drain Charge	Q_{gd}	—	4.4	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	277	—	ns	$V_{DD} = 16\text{V}, I_D = 5.5\text{A}, V_{GS} = 4.5\text{V}, R_g = 6\Omega$
Turn-On Rise Time	t_R	—	653	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	1,989	—	ns	
Turn-Off Fall Time	t_F	—	1,208	—	ns	
Reverse Recovery Time	t_{RR}	—	492	—	ns	
Reverse Recovery Charge	Q_{RR}	—	908	—	nC	$I_F = 11\text{A}, di/dt = 100\text{A}/\mu\text{s}$

- Notes:
- Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
 - Device mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate.
 - I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep $T_J = +25^\circ\text{C}$.
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to product testing.

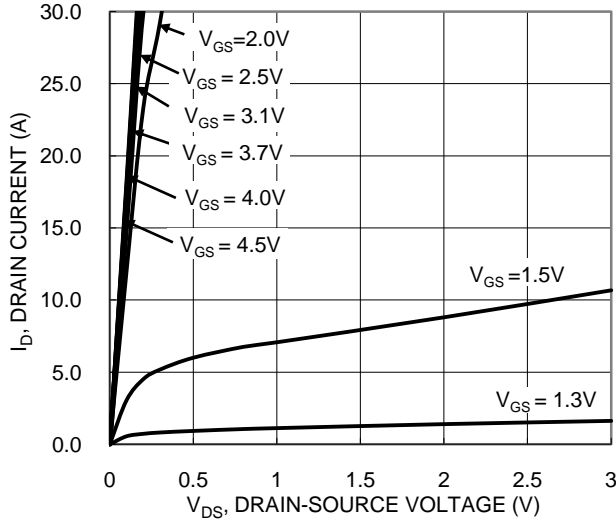


Figure 1. Typical Output Characteristic

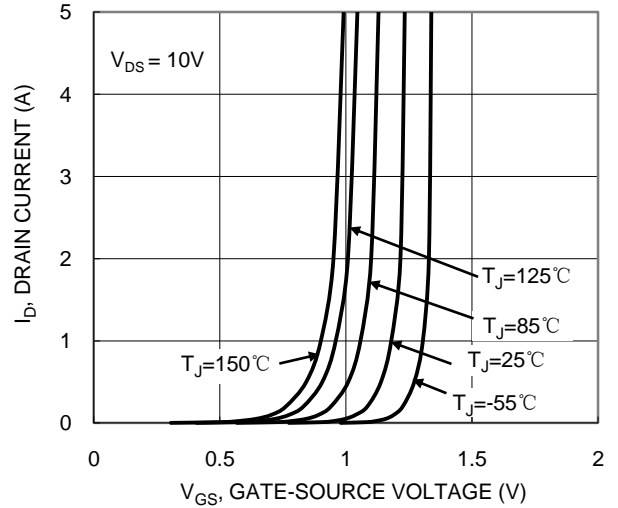


Figure 2. Typical Transfer Characteristic

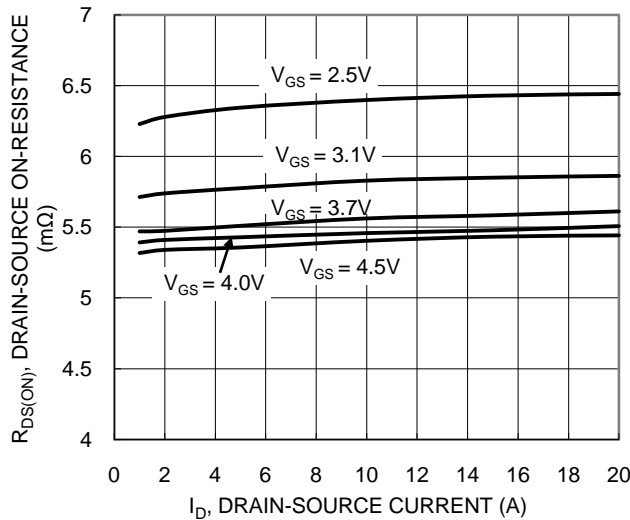


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

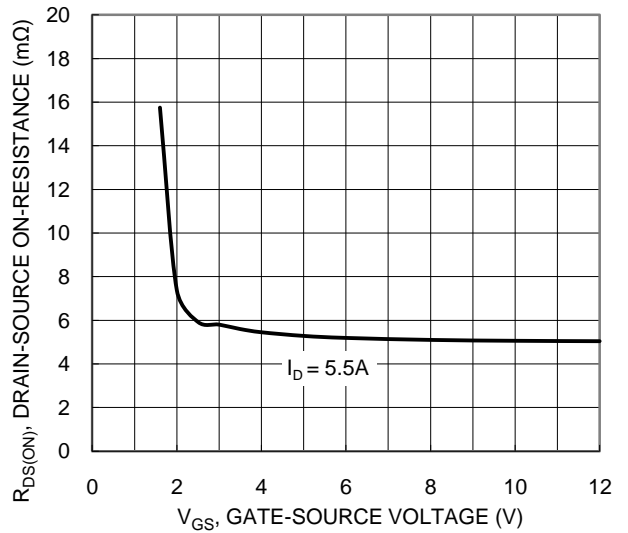


Figure 4. Typical Transfer Characteristic

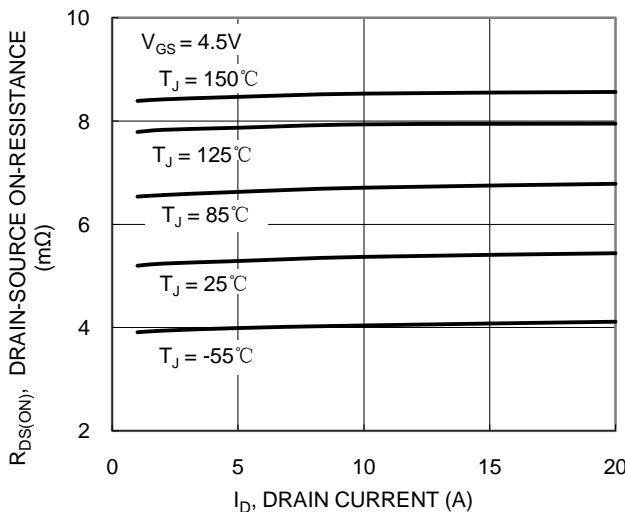


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

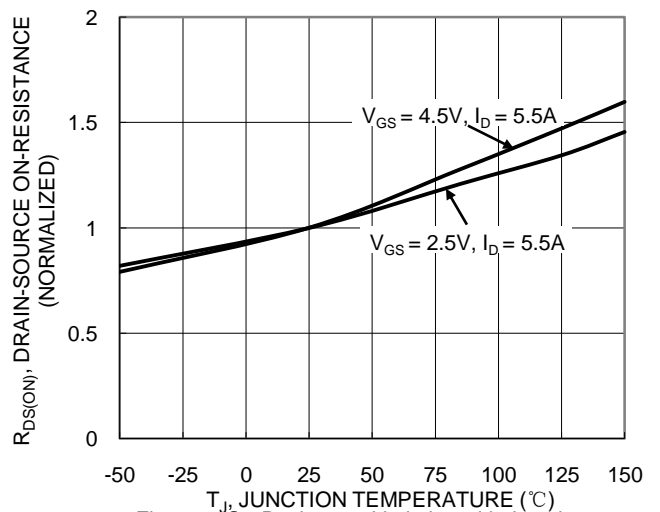


Figure 6. On-Resistance Variation with Junction Temperature

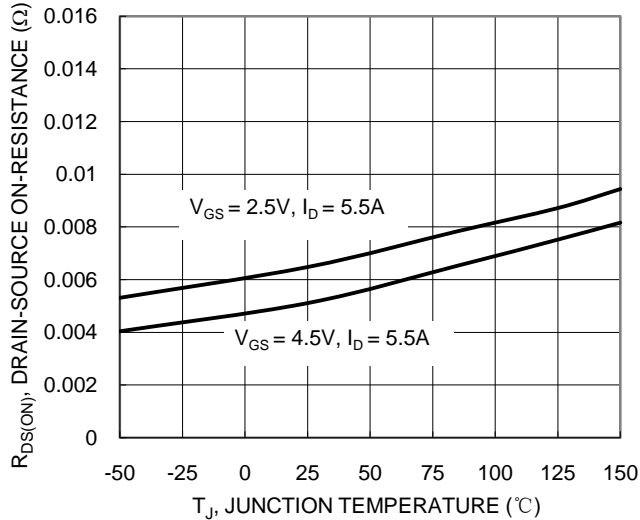


Figure 7. On-Resistance Variation with Junction Temperature

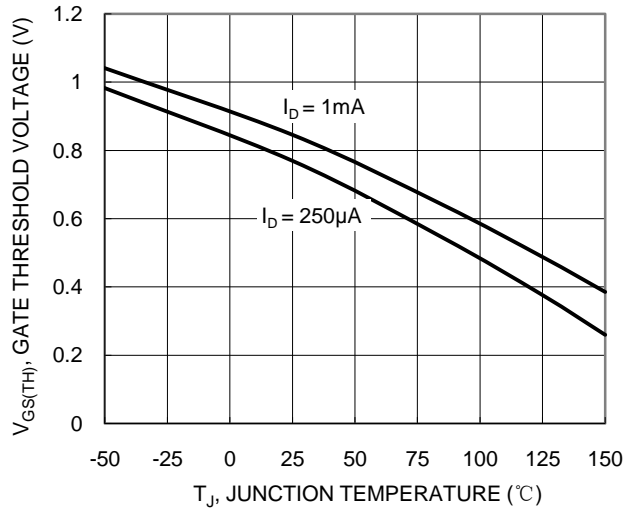


Figure 8. Gate Threshold Variation vs. Junction Temperature

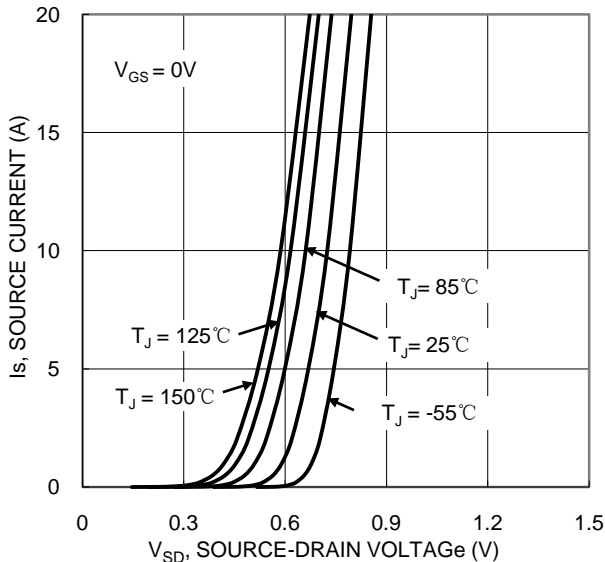


Figure 9. Diode Forward Voltage vs. Current

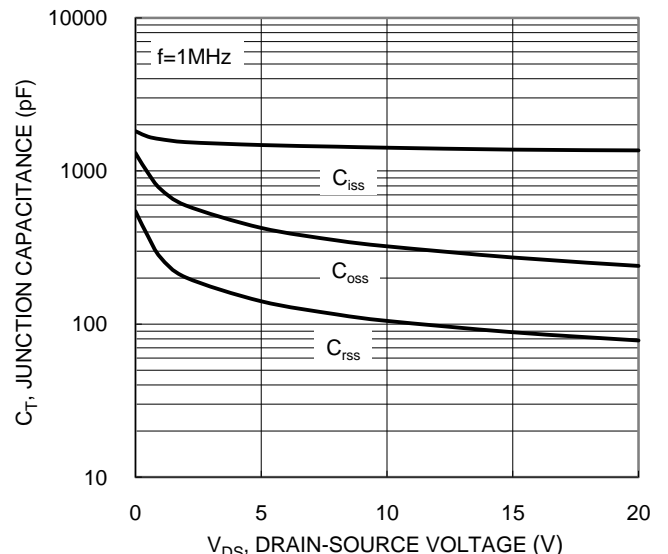


Figure 10. Typical Junction Capacitance

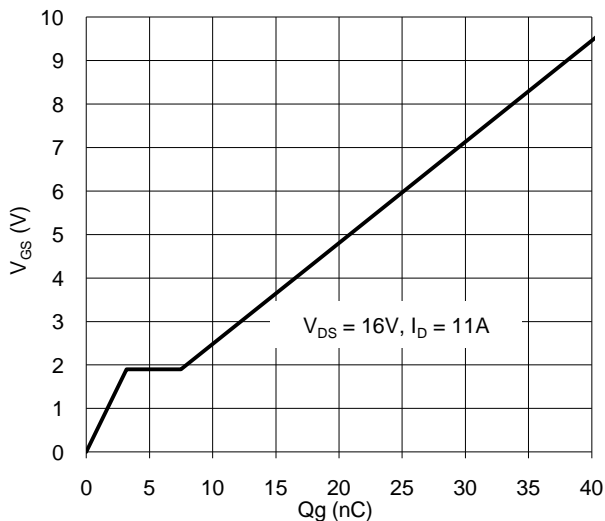


Figure 11. Gate Charge

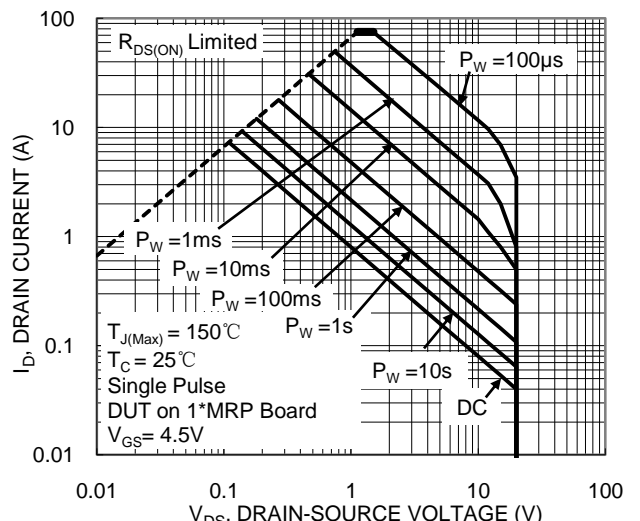


Figure 12. SOA, Safe Operation Area

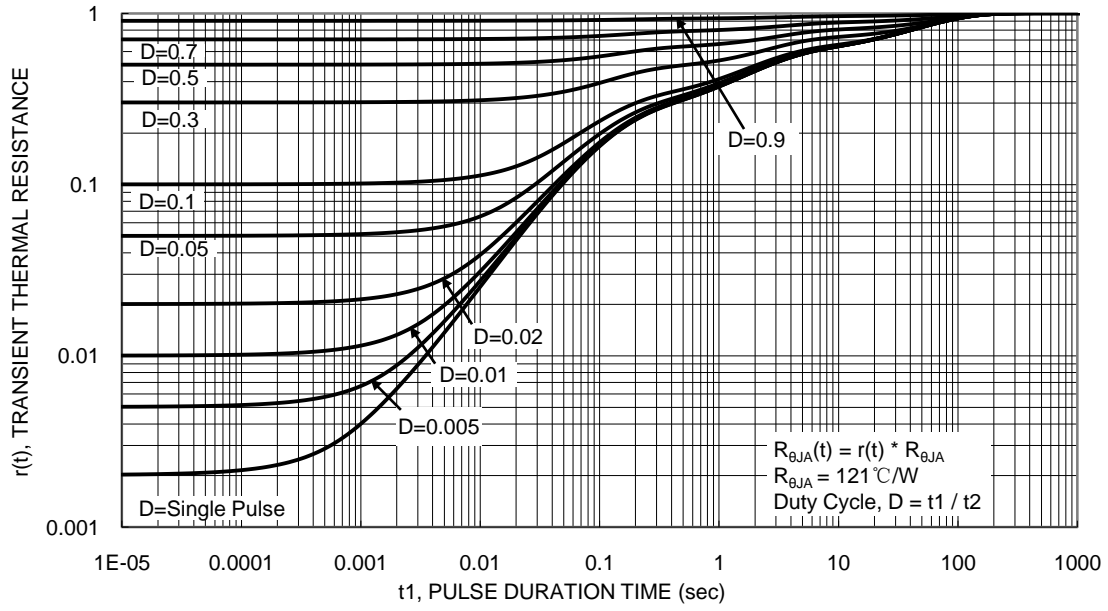
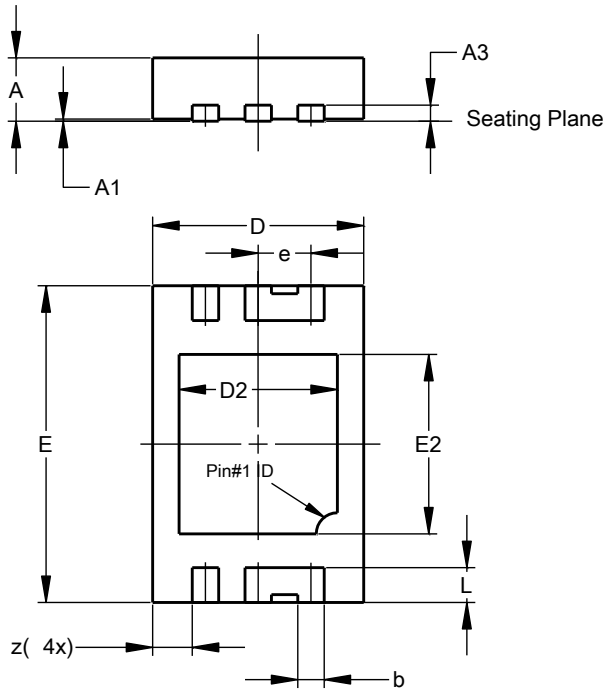


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

U-DFN2030-6 (Type B)

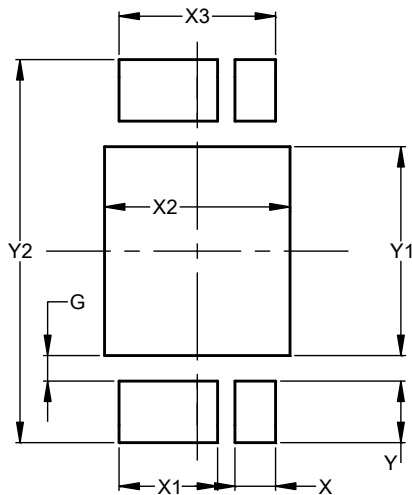


U-DFN2030-6 (Type B)			
Dim	Min	Max	Typ
A	0.55	0.65	0.60
A1	0.00	0.05	0.02
A3	-	-	0.15
b	0.20	0.30	0.25
D	1.95	2.05	2.00
D2	1.40	1.60	1.50
E	2.95	3.05	3.00
E2	1.65	1.75	1.70
e	-	-	0.50
L	0.28	0.38	0.33
z	-	-	0.375
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

U-DFN2030-6 (Type B)



Dimensions	Value (in mm)
G	0.220
X	0.350
X1	0.850
X2	1.600
X3	1.350
Y	0.530
Y1	1.800
Y2	3.300

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