THE DATASHEET OF

DS3164

www.win-source.net 0086-755-83957316

DS3161/DS3162/DS3163/DS3164 Single/Dual/Triple/Quad ATM/Packet PHYs for DS3/E3/STS-1

www.maxim-ic.com

GENERAL DESCRIPTION

The DS3161, DS3162, DS3163, and DS3164 (DS316x) integrate ATM cell/HDLC packet processor(s) with DS3/E3 framer(s) to map/demap ATM cells or packets into as many as four DS3/E3 digital lines with DS3-framed, E3-framed, or clear-channel data streams on per-port basis.

APPLICATIONS

Access Concentrators
SONET/SDH ADM
SONET/SDH Muxes
PBXs
Digital Cross Connect
Test Equipment
Routers and Switches
Integrated Access Device (IAD)
Multiservice Access Platform (MSAP)
Multiservice Protocol Platform (MSPP)
ATM and Frame Relay Equipment
PDH Multiplexer/ Demultiplexer

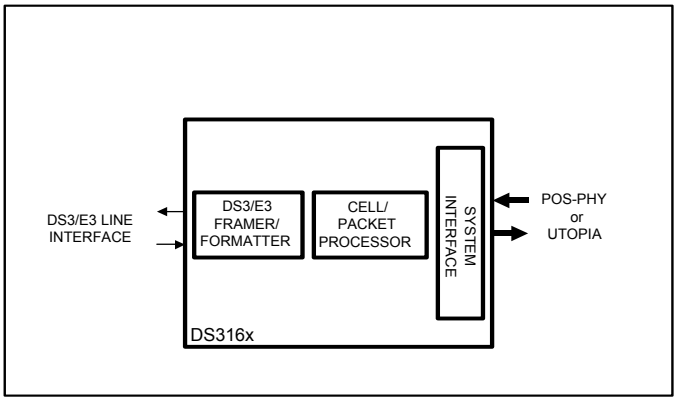
ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS3161	0°C to +70°C	400 TE-PBGA (27mm x 27mm, 1.27mm pitch)
DS3161N	-40°C to +85°C	400 TE-PBGA (27mm x 27mm, 1.27mm pitch)
DS3162	0°C to +70°C	400 TE-PBGA (27mm x 27mm, 1.27mm pitch)
DS3162N	-40°C to +85°C	400 TE-PBGA (27mm x 27mm, 1.27mm pitch)
DS3163	0°C to +70°C	400 TE-PBGA (27mm x 27mm, 1.27mm pitch)
DS3163N	-40°C to +85°C	400 TE-PBGA (27mm x 27mm, 1.27mm pitch)
DS3164	0°C to +70°C	400 TE-PBGA (27mm x 27mm, 1.27mm pitch)
DS3164N	-40°C to +85°C	400 TE-PBGA (27mm x 27mm, 1.27mm pitch)

Note: *Add the "+" suffix for the lead-free package option.*

POS-PHY and POS-PHY Level 3 are trademarks of PMC-Sierra, Inc.

FUNCTIONAL DIAGRAM



FEATURES

- Single (DS3161), Dual (DS3162), Triple (DS3163), or Quad (DS3164) ATM/Packet PHYs for DS3, E3, and Clear-Channel 52Mbps (CC52)
- Pin Compatible for Ease of Port Density Migration in the Same PC Board Platform
- Each Port Independently Configurable
- Universal PHYs Map ATM Cells and/or HDLC Packets into DS3 or E3 Data Streams
- UTOPIA L2/L3 or POS-PHY™ L2/L3 or SPI-3 Interface with 8-, 16-, or 32-Bit Bus Width
- 66MHz UTOPIA L3 and POS-PHY L3 Clock
- 52MHz UTOPIA L2 and POS-PHY L2 Clock
- Ports Independently Configurable for Cell or Packet Traffic in POS-PHY Bus Modes
- Direct, PLCP, DSS, and Clear-Channel Cell Mapping
- Direct and Clear-Channel Packet Mapping
- On-Chip DS3 (M23 or C-Bit) and E3 (G.751 or G.832) Framer(s)
- Ports Independently Configurable for DS3, E3 (Full or Subrate) or Arbitrary Framing Protocols Up to 52Mbps
- Programmable (Externally Controlled or Internally Finite State Machine Controlled) Subrate DS3/E3

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

FEATURES (continued)

- Full-Featured DS3/E3/PLCP Alarm Generation and Detection
- Built-In HDLC Controllers with 256-Byte FIFOs for Insertion/Extraction of DS3 PMDL, G.751 Sn Bit, and G.832 NR/GC Bytes and PLCP NR/GC Bytes
- On-Chip BERTs for PRBS and Repetitive Pattern Generation, Detection, and Analysis
- Large Performance-Monitoring Counters for Accumulation Intervals of at Least 1 Second
- Flexible Overhead Insertion/Extraction Ports for DS3, E3, and PLCP Framers
- Pin and Software Compatible with DS3181–DS3184 Single–Quad ATM/Packet PHYs with Built-In LIUs and DS3171–DS3174 Single–Quad DS3/E3 Single-Chip Transceivers—Framers and LIUs

DETAILED DESCRIPTION

The DS3161 (single), DS3162 (dual), DS3163 (triple), and DS3164 (quad) PHYs perform all the functions necessary for mapping/demapping ATM cells and/or packets into as many as four DS3 (44.736Mbps) framed, E3 (34.368Mbps) framed, or 52Mbps clear-channel data streams. Dedicated cell processor and packet processor blocks prepare outgoing cells or packets for transmission and check incoming cells or packets upon arrival. Built-in DS3/E3 framers transmit and receive cell/packet data in properly formatted M23 DS3, C-bit DS3, G.751 E3, or G.832 E3 data streams. PLCP framers provide legacy ATM transmission-convergence support. DSS scrambling is performed for clear-channel ATM cell support. With integrated hardware support for both cells and packets, the DS316x DS3/E3 ATM/Packet PHYs provide system-on-chip solutions (from DS3/E3/STS-1 digital lines to ATM/Packet UTOPIA/POS-PHY Level 2/3 system switch) for universal high-density line cards in the unchannelized DS3/E3/clear-channel DS3 ATM/Packet applications. Unused functions can be powered down to reduce device power. The DS316x ATM/Packet PHYs with embedded framers conform to the telecommunications standards listed in Section 4.

1 BLOCK DIAGRAM

Figure 1-1 shows the functional block diagram of one channel ATM/Packet PHY.

Figure 1-1. DS316x Functional Block Diagram

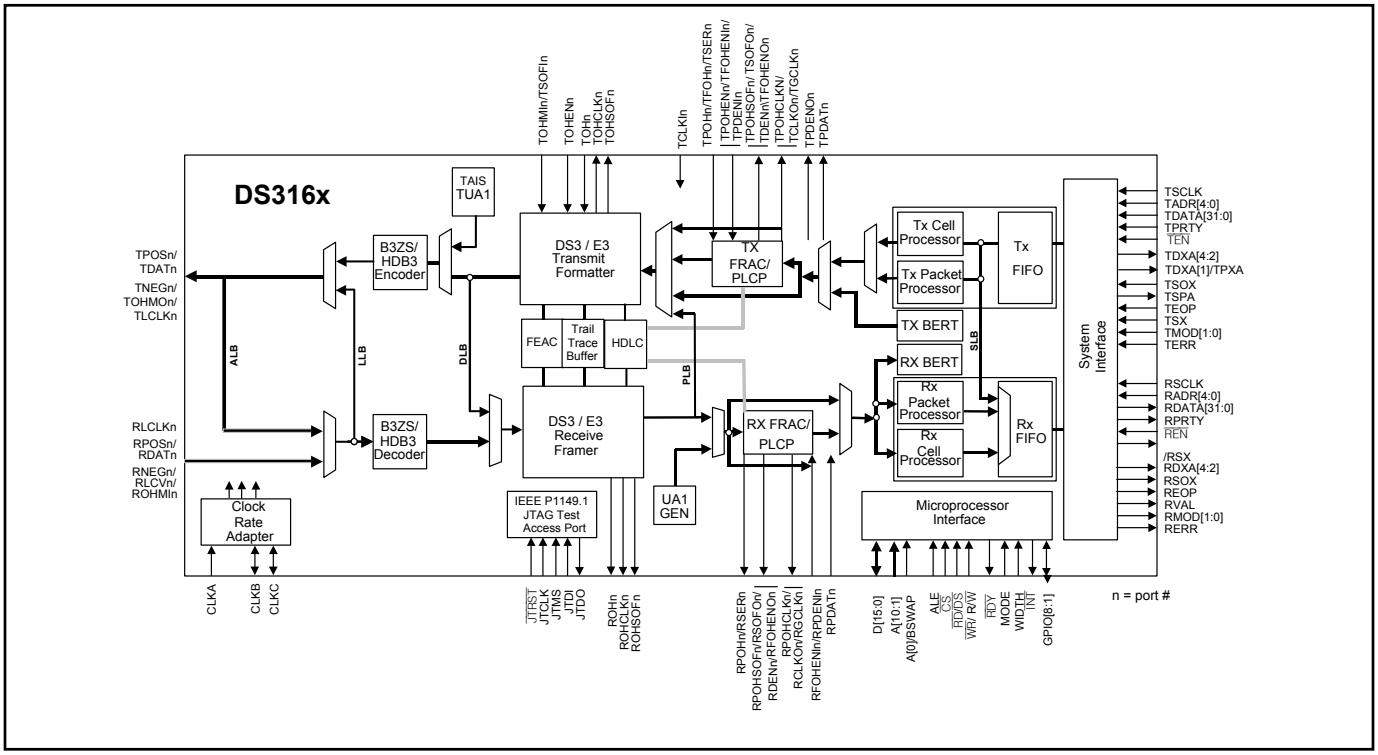


TABLE OF CONTENTS

1 BLOCK DIAGRAM 2

2 APPLICATIONS 14

3 FEATURE DETAILS 16

3.1 Global Features ... 16
3.2 Receive DS3/E3 Framer Features ... 17
3.3 Receive PLCP Framer Features ... 17
3.4 Receive Cell Processor Features ... 17
3.5 Receive Packet Processor Features ... 18
3.6 Receive FIFO Features ... 18
3.7 Receive System Interface Features ... 18
3.8 Transmit System Interface Features ... 18
3.9 Transmit FIFO Features ... 18
3.10 Transmit Cell Processor Features ... 18
3.11 Transmit Packet Processor Features ... 19
3.12 Transmit PLCP Formatter Features ... 19
3.13 Transmit DS3/E3 Formatter Features ... 19
3.14 Clock Rate Adapter Features ... 19
3.15 HDLC Overhead Controller Features ... 20
3.16 FEAC Controller Features ... 20
3.17 Trail Trace Buffer Features ... 20
3.18 Bit Error Rate Tester (BERT) Features ... 20
3.19 Loopback Features ... 20
3.20 Microprocessor Interface Features ... 20
3.21 Subrate Features (Fractional DS3/E3) ... 21
3.22 Test Features ... 21

4 STANDARDS COMPLIANCE 22

5 ACRONYMS AND GLOSSARY 24

6 MAJOR OPERATIONAL MODES 25

6.1 DS3/E3 ATM/Packet Mode ... 25
6.2 DS3/E3 ATM/Packet—OHM Mode ... 26
6.3 DS3/E3 Internal Fractional (Subrate) ATM/Packet Mode ... 27
6.4 DS3/E3 External Fractional (Subrate) ATM/Packet Mode ... 28
6.5 DS3/E3 Flexible External Fractional (Subrate) Mode Configuration Mode ... 29
6.6 DS3/E3 G.751 PLCP ATM Mode ... 30
6.7 DS3/E3 G.751 PLCP ATM—OHM Mode ... 31
6.8 Clear-Channel ATM/Packet Mode ... 33
6.9 Clear-Channel ATM/Packet—OHM Mode ... 34
6.10 Clear-Channel Octet Aligned ATM/Packet—OHM Mode ... 35

7 MAJOR LINE INTERFACE OPERATING MODES 36

7.1 HDB3/B3ZS/AMI Line Interface Mode ... 36
7.2 UNI Line Interface Mode ... 37
7.3 UNI Line Interface—OHM Mode ... 38

8 PIN DESCRIPTIONS 39

8.1 Short Pin Descriptions ... 39
8.2 Detailed Pin Descriptions ... 44
8.3 Pin Functional Timing ... 62
8.3.1 Line I/O ... 62
8.3.2 DS3/E3 Framing and PLCP Overhead Functional Timing ... 65
8.3.3 Internal (IFRAC) and External (XFRAC) Fractional DS3/E3 Overhead Functional Timing ... 68
8.3.4 Flexible Fractional (FFRAC) DS3/E3 Overhead Interface Functinal Timing ... 69
8.3.5 UTOPIA/POS-PHY/SPI-3 System Interface Functional Timing ... 71

8.3.6 Microprocessor Interface Functional Timing 85
8.3.7 JTAG Functional Timing 90
9 INITIALIZATION AND CONFIGURATION 91
9.1 MONITORING AND DEBUGGING 93
9.1.1 Cell/Packet FIFO 93
9.1.2 Cell Processor 93
9.1.3 Packet Processor 93
10 FUNCTIONAL DESCRIPTION 94
10.1 PROCESSOR BUS INTERFACE 94
10.1.1 8/16-Bit Bus Widths 94
10.1.2 Ready Signal ($\overline{RDY}$) 94
10.1.3 Byte Swap Modes 94
10.1.4 Read-Write/Data Strobe Modes 94
10.1.5 Clear on Read/Clear on Write Modes 94
10.1.6 Global Write Method 95
10.1.7 Interrupt and Pin Modes 95
10.1.8 Interrupt Structure 95
10.2 CLOCKS 97
10.2.1 Line Clock Modes 97
10.2.2 Sources of Clock Output Pin Signals 98
10.2.3 Line I/O Pin Timing Source Selection 99
10.2.4 Clock Structures On Signal IO Pins 102
10.2.5 Gapped Clocks 102
10.3 RESET AND POWER-DOWN 103
10.4 GLOBAL RESOURCES 105
10.4.1 Clock Rate Adapter (CLAD) 105
10.4.2 8 kHz Reference Generation 107
10.4.3 One-Second Reference Generation 109
10.4.4 General-Purpose I/O Pins 109
10.4.5 Performance Monitor Counter Update Details 111
10.4.6 Transmit Manual Error Insertion 111
10.5 PER PORT RESOURCES 112
10.5.1 Loopbacks 112
10.5.2 Loss Of Signal Propagation 114
10.5.3 AIS Logic 114
10.5.4 Loop Timing Mode 116
10.5.5 HDLC Overhead Controller 116
10.5.6 Trail Trace 117
10.5.7 BERT 117
10.5.8 Fractional Payload Controller 117
10.5.9 PLCP/Fractional port pins 117
10.5.10 Framing Modes 121
10.5.11 Mapping Modes 123
10.5.12 Line Interface Modes 127
10.6 UTOPIA/POS-PHY/SPI-3 SYSTEM INTERFACE 128
10.6.1 General Description 128
10.6.2 Features 128
10.6.6 System Interface Bus Controller 129
10.7 ATM CELL / HDLC PACKET PROCESSING 134
10.7.1 General Description 134
10.7.2 Features 134
10.7.3 Transmit Cell/Packet Processor 135
10.7.4 Receive Cell/Packet Processor 135
10.7.5 Cell Processor 136
10.7.6 Packet Processor 141
10.7.7 FIFO 143

10.7.8 System Loopback *145*
10.8 DS3/E3 PLCP FRAMER 146
10.8.1 General Description *146*
10.8.2 Features *146*
10.8.3 Transmit PLCP Frame Processor *147*
10.8.4 Receive PLCP Frame Processor *147*
10.8.5 Transmit DS3 PLCP Frame Processor *147*
10.8.6 Receive DS3 PLCP Frame Processor *150*
10.8.7 Transmit E3 PLCP Frame Processor *151*
10.8.8 Receive E3 PLCP Frame Processor *154*
10.9 FRACTIONAL PAYLOAD CONTROLLER 156
10.9.1 General Description *156*
10.9.2 Features *156*
10.9.3 Transmit Fractional Interface *157*
10.9.4 Transmit Fractional Controller *157*
10.9.5 Receive Fractional Interface *157*
10.9.6 Receive Fractional Controller *157*
10.10 DS3/E3 FRAMER / FORMATTER 159
10.10.1 General Description *159*
10.10.2 Features *159*
10.10.3 Transmit Formatter *160*
10.10.4 Receive Framer *160*
10.10.5 C-bit DS3 Framer/Formatter *165*
10.10.6 M23 DS3 Framer/Formatter *167*
10.10.7 G.751 E3 Framer/Formatter *170*
10.10.8 G.832 E3 Framer/Formatter *172*
10.10.9 Clear-Channel Frame Processor *177*
10.11 HDLC OVERHEAD CONTROLLER 177
10.11.1 General Description *177*
10.11.2 Features *178*
10.11.3 Transmit FIFO *178*
10.11.4 Transmit HDLC Overhead Processor *179*
10.11.5 Receive HDLC Overhead Processor *179*
10.11.6 Receive FIFO *180*
10.12 TRAIL TRACE CONTROLLER 181
10.12.1 General Description *181*
10.12.2 Features *182*
10.12.3 Functional Description *182*
10.12.4 Transmit Data Storage *182*
10.12.5 Transmit Trace ID Processor *183*
10.12.6 Transmit Trail Trace Processing *183*
10.12.7 Receive Trace ID Processor *183*
10.12.8 Receive Trail Trace Processing *183*
10.12.9 Receive Data Storage *184*
10.13 FEAC CONTROLLER 184
10.13.1 General Description *184*
10.13.2 Features *185*
10.13.3 Functional Description *185*
10.14 LINE ENCODER/DECODER 186
10.14.1 General Description *186*
10.14.2 Features *187*
10.14.3 B3ZS/HDB3 Encoder *187*
10.14.4 Transmit Line Interface *188*
10.14.5 Receive Line Interface *188*
10.14.6 B3ZS/HDB3 Decoder *188*
10.15 BERT 190
10.15.1 General Description *190*

10.15.2 Features *190*
10.15.3 Configuration and Monitoring *190*
10.15.4 Receive Pattern Detection *191*
10.15.5 Transmit Pattern Generation *193*
11 OVERALL REGISTER MAP **194**
12 REGISTER MAPS AND DESCRIPTIONS **197**
12.1 REGISTERS BIT MAPS 197
12.1.1 Global Register Bit Map *197*
12.1.2 HDLC Register Bit Map *200*
12.1.3 T3 Register Bit Map *202*
12.1.4 E3 G.751 Register Bit Map *203*
12.1.5 E3 G.832 Register Bit Map *204*
12.1.6 Clear-Channel Register Bit Map *205*
12.1.7 Fractional Register Bit Map *205*
12.1.8 Transmit Cell Processor Bit Map *208*
12.1.9 Transmit Packet Processor Bit Map *208*
12.2 GLOBAL REGISTERS 211
12.2.1 Register Bit Descriptions *212*
12.3 UTOPIA/POS-PHY SYSTEM INTERFACE 220
12.3.1 Transmit System Interface *220*
12.3.2 Receive System Interface Register Map *221*
12.4 PER PORT COMMON 224
12.4.1 Register Bit Descriptions *224*
12.5 BERT 236
12.5.1 BERT Register Map *236*
12.5.2 BERT Register Bit Descriptions *237*
12.6 B3ZS/HDB3 LINE ENCODER/DECODER 245
12.6.1 Transmit Side Line Encoder/Decoder Register Map *245*
12.6.2 Receive Side Line Encoder/Decoder Register Map *246*
12.7 HDLC 250
12.7.1 HDLC Transmit Side Register Map *250*
12.7.2 HDLC Receive Side Register Map *254*
12.8 FEAC CONTROLLER 258
12.8.1 FEAC Transmit Side Register Map *258*
12.8.2 FEAC Receive Side Register Map *261*
12.9 TRAIL TRACE 264
12.9.1 Trail Trace Transmit Side *264*
12.9.2 Trail Trace Receive Side Register Map *266*
12.10 DS3/E3 FRAMER 270
12.10.1 Transmit DS3 ..... *270*
12.10.2 Receive DS3 Register Map *272*
12.10.3 Transmit G.751 E3 ..... *280*
12.10.4 Receive G.751 E3 Register Map *282*
12.10.5 Transmit G.832 E3 Register Map *287*
12.10.6 Receive G.832 E3 Register Map *290*
12.10.7 Transmit Clear Channel *298*
12.10.8 Receive Clear Channel *299*
12.11 FRACTIONAL DS3/E3 301
12.11.1 Fractional Transmit Side Register Map *301*
12.11.2 Fractional Receive Side Register Map *303*
12.12 DS3/E3 PLCP 305
12.12.1 Transmit Side PLCP *305*
12.12.2 Receive Side PLCP Register Map *309*
12.13 FIFO REGISTERS 318
12.13.1 Transmit FIFO Register Map *318*
12.13.2 Receive FIFO Register Map *322*

12.14 CELL/PACKET PROCESSOR 325
12.14.1 Transmit Cell Processor Register Map 325
12.14.2 Receive Cell Processor 333
12.14.3 Transmit Packet Processor Register Map 345
12.14.4 Receive Packet Processor Register Map 350
13 JTAG INFORMATION 361
13.1 JTAG DESCRIPTION 361
13.2 JTAG TAP CONTROLLER STATE MACHINE DESCRIPTION 361
13.3 JTAG INSTRUCTION REGISTER AND INSTRUCTIONS 364
13.4 JTAG ID CODES 365
13.5 JTAG FUNCTIONAL TIMING 365
13.6 I/O PINS 365
14 PIN ASSIGNMENT 366
15 PACKAGE MECHANICAL DIMENSIONS 370
15.1 400-LEAD TE-PBGA (27MM X 27MM, 1.27MM PITCH) (56-G6003-003) 370
16 PACKAGE THERMAL INFORMATION 371
17 DC ELECTRICAL CHARACTERISTICS 372
18 AC TIMING CHARACTERISTICS 374
18.1 FRACTIONAL PORT CHARACTERISTICS 376
18.2 LINE INTERFACE AC CHARACTERISTICS 376
18.3 MISC PIN AC CHARACTERISTICS 377
18.4 OVERHEAD PORT AC CHARACTERISTICS 377
18.5 SYSTEM INTERFACE AC CHARACTERISTICS 378
18.6 MICRO INTERFACE AC CHARACTERISTICS 380
18.7 CLAD JITTER CHARACTERISTICS 383
18.8 JTAG INTERFACE AC CHARACTERISTICS 383
19 REVISION HISTORY 384

LIST OF FIGURES

Figure 1-1. DS316x Functional Block Diagram 2
Figure 2-1. Four-Port Unchannelized ATM over DS3/E3/CC52 Line Card 14
Figure 2-2. Four-Port Unchannelized HDLC over DS3/E3/CC52 Line Card 15
Figure 6-1. DS3/E3 ATM/Packet Mode 25
Figure 6-2. DS3/E3 ATM/Packet—OHM Mode 26
Figure 6-3. DS3/E3 Internal Fractional ATM/Packet Mode 27
Figure 6-4. DS3/E3 External Fractional ATM/Packet Mode 28
Figure 6-5. DS3/E3 Flexible External Fractional Mode 29
Figure 6-6. DS3/E3 G.751 PLCP ATM Mode 30
Figure 6-7. DS3/E3 G.751 PLCP ATM—OHM Mode 32
Figure 6-8. Clear-Channel ATM/Packet Modes 33
Figure 6-9. Clear-Channel ATM/Packet—OHM Mode 34
Figure 6-10. Clear-Channel Octet Aligned ATM/Packet—OHM Mode 35
Figure 7-1. HDB3/B3ZS/AMI Line Interface Mode 36
Figure 7-2. UNI Line Interface Mode 37
Figure 7-3. UNI Line Interface—OHM Mode 38
Figure 8-1. TX Line I/O B3ZS Functional Timing Diagram 62
Figure 8-2. TX Line I/O HDB3 Functional Timing Diagram 62
Figure 8-3. RX Line I/O B3ZS Functional Timing Diagram 63
Figure 8-4. RX Line I/O HDB3 Functional Timing Diagram 63
Figure 8-5. TX Line I/O UNI OHM Functional Timing Diagram 64
Figure 8-6. TX Line I/O UNI Octet Aligned OHM Functional Timing Diagram 64
Figure 8-7. RX Line I/O OHM UNI Functional Timing Diagram 65
Figure 8-8. RX Line I/O UNI Octet Aligned OHM Functional Timing Diagram 65
Figure 8-9. DS3 Framing Receive Overhead Port Timing 65
Figure 8-10. E3 G.751 Framing Receive Overhead Port Timing 65
Figure 8-11. E3 G.832 Framing Receive Overhead Port Timing 66
Figure 8-12. DS3 Framing Transmit Overhead Port Timing 66
Figure 8-13. E3 G.751 Framing Transmit Overhead Port Timing 66
Figure 8-14. E3 G.832 Framing Transmit Overhead Port Timing 66
Figure 8-15. DS3 PLCP Receive Overhead Port Timing 67
Figure 8-16. E3 G.751 PLCP Receive Overhead Port Timing 67
Figure 8-17. DS3 PLCP Transmit Overhead Port Timing 67
Figure 8-18. E3 G.751 PLCP Transmit Overhead Port Timing 67
Figure 8-19. External (XFRAC) Transmit Fractional Timing 68
Figure 8-20. External (XFRAC) Receive Fractional Timing 68
Figure 8-21. Internal (IFRAC) Transmit Fractional Timing 68
Figure 8-22. Internal (IFRAC) Receive Fractional Timing 69
Figure 8-23. Transmit Flexible Fractional (FFRAC) Timing 69
Figure 8-24. Receive Flexible Fractional (FFRAC) Timing 70
Figure 8-25. UTOPIA Level 2 Transmit Cell Transfer Direct Mode 71
Figure 8-26. UTOPIA Level 2 Receive Cell Transfer Direct Mode 72
Figure 8-27. UTOPIA Level 2 Transmit Multiple Cell Transfer Polled Mode 73
Figure 8-28. UTOPIA Level 2 Receive Multiple Cell Transfer Polled Mode 74
Figure 8-29. UTOPIA Level 2 Receive Unexpected Multiple Cell Transfer 75
Figure 8-30. UTOPIA Level 3 Transmit Multiple Cell Transfer Direct Mode 76
Figure 8-31. UTOPIA Level 3 Transmit Multiple Cell Transfer Polled Mode 77
Figure 8-32: UTOPIA Level 3 Receive Multiple Cell Transfer Direct Mode 78
Figure 8-33. UTOPIA Level 3 Receive Multiple Cell Transfer Polled Mode 79
Figure 8-34. Transmit Multiple Packet Transfer to Different PHY ports (Direct Status Mode) 80
Figure 8-35. POS-PHY Level 2 Receive Multiple Packet Transfer from Different PHY Ports/Devices (Direct Status Mode) 81
Figure 8-36. POS-PHY Level 2 Transmit Multiple Packet Transfer to Different PHY Ports (Polled Status Mode) 82
Figure 8-37. POS-PHY Level 2 Receive Multiple Packet Transfer (Polled Status Mode) 83
Figure 8-38. POS-PHY Level 3 Transmit Multiple Packet Transfer In-Band Addressing 84

Figure 8-39. POS-PHY Level 3 Receive Multiple Packet Transfer In-Band Addressing 85
Figure 8-40. 16-Bit Mode Write 86
Figure 8-41. 16-Bit Mode Read 86
Figure 8-42. 8-Bit Mode Write 87
Figure 8-43. 8-Bit Mode Read 87
Figure 8-44. 16-Bit Mode without Byte Swap 88
Figure 8-45. 16-Bit Mode with Byte Swap 88
Figure 8-46. Clear Status Latched Register on Read 89
Figure 8-47. Clear Status Latched Register on Write 89
Figure 8-48. RDY Signal Functional Timing Writes 90
Figure 8-49. RDY Signal Functional Timing Read 90
Figure 10-1. Interrupt Structure 96
Figure 10-2. Internal TX Clock 99
Figure 10-3. Example I/O Pin Clock Muxing 102
Figure 10-4. Reset Sources 104
Figure 10-5. CLAD Block 106
Figure 10-6. 8KREF Logic 109
Figure 10-7. Performance Monitor Update Logic 111
Figure 10-8. Transmit Error Insert Logic 112
Figure 10-9. Loopback Modes 113
Figure 10-10. AIS Signal Flow 115
Figure 10-11. DS3 C-bit or DS3 M23 (with C-bit generation) Frame 123
Figure 10-12. DS3 PLCP Frame 124
Figure 10-13. DS3 M23 (with C-bits used as payload) Frame 125
Figure 10-14. E3 G.751 Frame 125
Figure 10-15. E3 PLCP Frame 126
Figure 10-16. Example E3 G.751 Internal Fractional Frame 126
Figure 10-17. E3 G.832 Frame 127
Figure 10-18. System Interface Functional Diagram 128
Figure 10-19. Normal Packet Format in 32-Bit Mode 129
Figure 10-20. Normal Packet Format in 16-Bit Mode 129
Figure 10-21. Byte Reordered Packet Format in 32-Bit Mode 129
Figure 10-22. Byte Reordered Packet Format in 16-Bit Mode 130
Figure 10-23. ATM Cell / HDLC Packet Functional Diagram 134
Figure 10-24. Receive DSS Scrambler Synchronization State Diagram 138
Figure 10-25. Cell Delineation State Diagram 139
Figure 10-26. HEC Error Monitoring State Diagram 140
Figure 10-27. Cell Format for 53-Byte Cell With 32-Bit Data Bus 140
Figure 10-28. Cell Format for 52-Byte Cell With 32-Bit Data Bus 141
Figure 10-29. PLCP Framer Functional Diagram 146
Figure 10-30. DS3 PLCP Frame Format 148
Figure 10-31. DS3 PLCP G1 Byte Format 148
Figure 10-32. E3 PLCP Frame Format 152
Figure 10-33. E3 PLCP G1 Byte Format 152
Figure 10-34. Fractional Payload Controller Detailed Block Diagram 156
Figure 10-35. Data Group Format 158
Figure 10-36. Frame Format 158
Figure 10-37. Framer Detailed Block Diagram 159
Figure 10-38. DS3 Frame Format 161
Figure 10-39. DS3 Subframe Framer State Diagram 162
Figure 10-40. DS3 Multiframe Framer State Diagram 163
Figure 10-41. G.751 E3 Frame Format 170
Figure 10-42. G.832 E3 Frame Format 172
Figure 10-43. MA Byte Format 173
Figure 10-44. HDLC Controller Block Diagram 178
Figure 10-45. Trail Trace Controller Block Diagram 182
Figure 10-46. Trail Trace Byte (DT = Trail Trace Data) 183

Figure 10-47. FEAC Controller Block Diagram 185
Figure 10-48. FEAC Codeword Format 186
Figure 10-49. Line Encoder/Decoder Block Diagram 187
Figure 10-50. B3ZS Signatures 189
Figure 10-51. HDB3 Signatures 189
Figure 10-52. BERT Block Diagram 190
Figure 10-53. PRBS Synchronization State Diagram 192
Figure 10-54. Repetitive Pattern Synchronization State Diagram 193
Figure 13-1. JTAG Block Diagram 361
Figure 13-2. JTAG TAP Controller State Machine 362
Figure 13-3. JTAG Functional Timing 365
Figure 14-1. DS3164 Pin Assignments—400-Lead BGA 366
Figure 14-2. DS3163 Pin Assignments—400-Lead BGA 367
Figure 14-3. DS3162 Pin Assignments—400-Lead BGA 368
Figure 14-4 DS3161 Pin Assignments—400-Lead BGA 369
Figure 18-1. Clock Period and Duty Cycle Definitions 374
Figure 18-2. Rise Time, Fall Time, and Jitter Definitions 374
Figure 18-3. Hold, Setup, and Delay Definitions (Rising Clock Edge) 374
Figure 18-4. Hold, Setup, and Delay Definitions (Falling Clock Edge) 375
Figure 18-5. To/From Hi-Z Delay Definitions (Rising Clock Edge) 375
Figure 18-6. To/From Hi-Z Delay Definitions (Falling Clock Edge) 375
Figure 18-7. Micro Interface Nonmultiplexed Read/Write Cycle 381
Figure 18-8. Micro Interface Multiplexed Read Cycle 382

LIST OF TABLES

Table 4-1. Standards Compliance 22
Table 6-1. DS3/E3 ATM/Packet Mode Configuration Registers 25
Table 6-2. DS3/E3 ATM/Packet—OHM Mode Configuration Registers 26
Table 6-3. DS3/E3 Internal Fractional (IFRAC) ATM/Packet Mode Configuration Registers 27
Table 6-4. DS3/E3 External Fractional (XFRAC) ATM/Packet Mode Configuration Registers 28
Table 6-5. DS3/E3 Flexible External Fractional (Subrate) Mode Configuration Registers 29
Table 6-6. DS3/E3 G.751 PLCP ATM Mode Configuration Registers 30
Table 6-7. DS3/E3 G.751 PLCP ATM—OHM Mode Configuration Registers 31
Table 6-8. Clear-Channel ATM/Packet Mode Configuration Modes 33
Table 6-9. Clear-Channel ATM/Packet—OHM Mode Configuration Registers 34
Table 6-10. Clear-Channel Octet Aligned ATM/Packet—OHM Mode Configuration Registers 35
Table 7-1. HDB3/B3ZS/AMI Mode Configuration Registers 36
Table 7-2. UNI Line Interface Mode Configuration Registers 37
Table 7-3. UNI Line Interface—OHM Mode Configuration Registers 38
Table 8-1. DS3164 Short Pin Descriptions 39
Table 8-2. Detailed Pin Descriptions 44
Table 9-1. Configuration of Global Register Settings 92
Table 9-2. Configuration of Port Register Settings 92
Table 10-1. All Possible Clock Sources Based on Mode and Loopback 98
Table 10-2. Source Selection of TLCLK Clock Signal 98
Table 10-3. Source Selection of TCLKOn (internal TX clock) 99
Table 10-4. Source Selection of RCLKO Clock Signal (internal RX clock) 99
Table 10-5. Transmit Line Interface Signal Pin Valid Timing Source Select 100
Table 10-6. Transmit Framer Pin Signal Timing Source Select 101
Table 10-7. Receive Framer Pin Signal Timing Source Select 101
Table 10-8. Reset and Power-Down Sources 104
Table 10-9. CLAD IO Pin Decode 107
Table 10-10. Global 8kHz Reference Source Table 108
Table 10-11. Port 8kHz Reference Source Table 108
Table 10-12. GPIO Global Signals 110
Table 10-13. GPIO Pin Global Mode Select Bits 110
Table 10-14. GPIO Port Alarm Monitor Select 110
Table 10-15. Loopback Mode Selections 112
Table 10-16. Line AIS Enable Modes 116
Table 10-17. Payload (downstream) AIS Enable Modes 116
Table 10-18. TSOFIn / TOHMIn Input Pin Functions 117
Table 10-19. TSERn / TPOHn / TFOHn Input Pin Functions 118
Table 10-20. TPDENIn / TPOHENn / TFOHENIn Input Pin Functions 118
Table 10-21. TSOFOn / TDENn / TPOHSOFn / TFOHENOn Output Pin Functions 118
Table 10-22. TCLKOn / TGCLKn / TPOHCLKn Output Pin Functions 119
Table 10-23. TPDATn Input Pin Functions 119
Table 10-24. TPDENOn Output Pin Functions 119
Table 10-25. RSERn / RPOHn Output Pin Functions 120
Table 10-26. RPDENIn / RFOHENIn Input Pin Functions 120
Table 10-27. RPDATn Input Pin Functions 120
Table 10-28. RSOFOn / RDENn / RPOHSOFn / RFOHENOn Output Pin Functions 121
Table 10-29. RCLKOn / RGCLKn / RPOHCLKn Output Pin Functions 121
Table 10-30. Framing Mode Select Bits FM[5:0] 122
Table 10-31. Line Mode Select Bits - LM 127
Table 10-32. C-Bit DS3 Frame Overhead Bit Definitions 165
Table 10-33. M23 DS3 Frame Overhead Bit Definitions 168
Table 10-34. G.832 E3 Frame Overhead Bit Definitions 173
Table 10-35. Payload Label Match Status 176
Table 10-36. Pseudo-Random Pattern Generation 191
Table 10-37. Repetitive Pattern Generation 191

Table 11-1. Global and Test Register Address Map 195
Table 11-2. Per Port Register Address Map 196
Table 12-1. Global Register Bit Map 197
Table 12-2. System Interface Bit Map 198
Table 12-3. Port Register Bit Map 198
Table 12-4. BERT Register Bit Map 199
Table 12-5. Line Register Bit Map 200
Table 12-6. HDLC Register Bit Map 200
Table 12-7. FEAC Register Bit Map 201
Table 12-8. Trail Trace Register Bit Map 202
Table 12-9. T3 Register Bit Map 202
Table 12-10. E3 G.751 Register Bit Map 203
Table 12-11. E3 G.832 Register Bit Map 204
Table 12-12. Clear-Channel Register Bit Map 205
Table 12-13. Fractional Register Bit Map 205
Table 12-14. PLCP Register Bit Map 206
Table 12-15. FIFO Register Bit Map 207
Table 12-16. Transmit Cell Processor Register Bit Map 208
Table 12-17. Transmit Packet Processor Register Bit Map 208
Table 12-18. Receive Cell Processor Register Bit Map 209
Table 12-19. Receive Packet Processor Register Bit Map 210
Table 12-20. Global Register Map 211
Table 12-21. Transmit System Interface Register Map 220
Table 12-22. Receive System Interface Register Map 221
Table 12-23. Per Port Common Register Map 224
Table 12-24. BERT Register Map 236
Table 12-25. Transmit Side B3ZS/HDB3 Line Encoder/Decoder Register Map 245
Table 12-26. Receive Side B3ZS/HDB3 Line Encoder/Decoder Register Map 246
Table 12-27. Transmit Side HDLC Register Map 250
Table 12-28. Receive Side HDLC Register Map 254
Table 12-29. FEAC Transmit Side Register Map 258
Table 12-30. FEAC Receive Side Register Map 261
Table 12-31. Transmit Side Trail Trace Register Map 264
Table 12-32. Trail Trace Receive Side Register Map 266
Table 12-33. Transmit DS3 Framer Register Map 270
Table 12-34. Receive DS3 Framer Register Map 272
Table 12-35. Transmit G.751 E3 Framer Register Map 280
Table 12-36. Receive G.751 E3 Framer Register Map 282
Table 12-37. Transmit G.832 E3 Framer Register Map 287
Table 12-38. Receive G.832 E3 Framer Register Map 290
Table 12-39. Transmit Clear-Channel Register Map 298
Table 12-40. Receive Clear-Channel Register Map 299
Table 12-41. Fractional Transmit Side Register Map 301
Table 12-42. Receive Side Register Map 303
Table 12-43. Transmit Side PLCP Register Map 305
Table 12-44. Receive Side PLCP Register Map 309
Table 12-45. Transmit FIFO Register Map 318
Table 12-46. Receive FIFO Register Map 322
Table 12-47. Transmit Cell Processor Register Map 325
Table 12-48. HEC Error Mask 329
Table 12-49. Receive Cell Processor Register Map 333
Table 12-50. Transmit Packet Processor Register Map 345
Table 12-51. Receive Packet Processor Register Map 350
Table 13-1. JTAG Instruction Codes 364
Table 13-2. JTAG ID Codes 365
Table 14-1. Pin Assignment Breakdown 366
Table 17-1. Recommended DC Operating Conditions 372

Table 17-2. DC Electrical Characteristics 372
Table 17-3. Output Pin Drive 373
Table 18-1. Fractional Port Timing 376
Table 18-2. Line interface Timing 376
Table 18-3. Miscellaneous Pin Timing 377
Table 18-4. Overhead Port Timing 377
Table 18-5. System Interface Level 2 Timing 378
Table 18-6. System Interface Level 3 Timing 379
Table 18-7. Micro Interface Timing 380
Table 18-8. JTAG Interface Timing 383

2 APPLICATIONS

- Access Concentrators
- Multi-Service Access Platforms
- ATM and Frame Relay Equipment
- Routers and Switches
- SONET/SDH ADM
- SONET/SDH Muxes
- PBXs
- Digital Cross Connect
- PDH Multiplexer/Demultiplexer
- Test Equipment
- Integrated Access Device (IAD)

Figure 2-1 and Figure 2-2 show applications for the DS3164 as four-port unchannelized ATM and packet DS3/E3 line cards, respectively.

Figure 2-1. Four-Port Unchannelized ATM over DS3/E3/CC52 Line Card

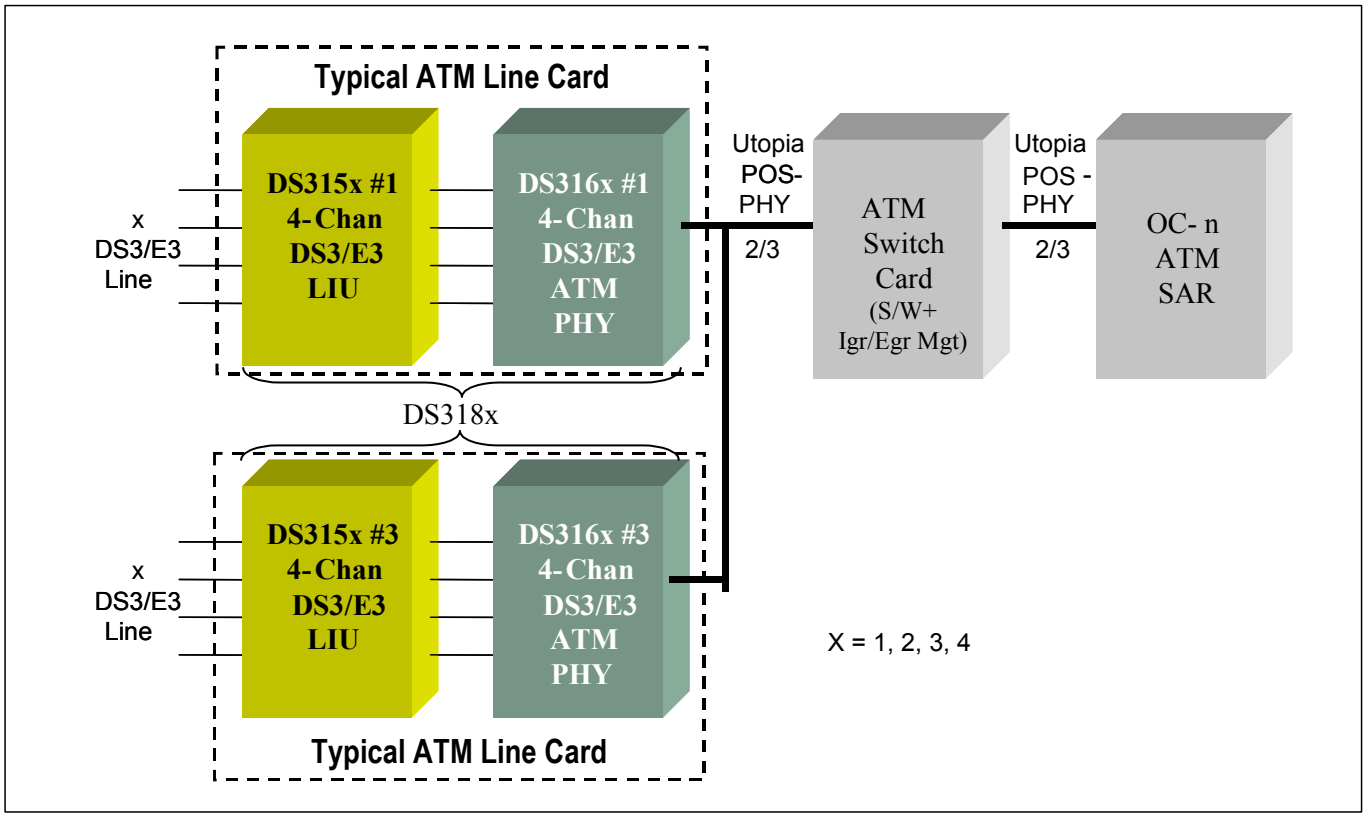
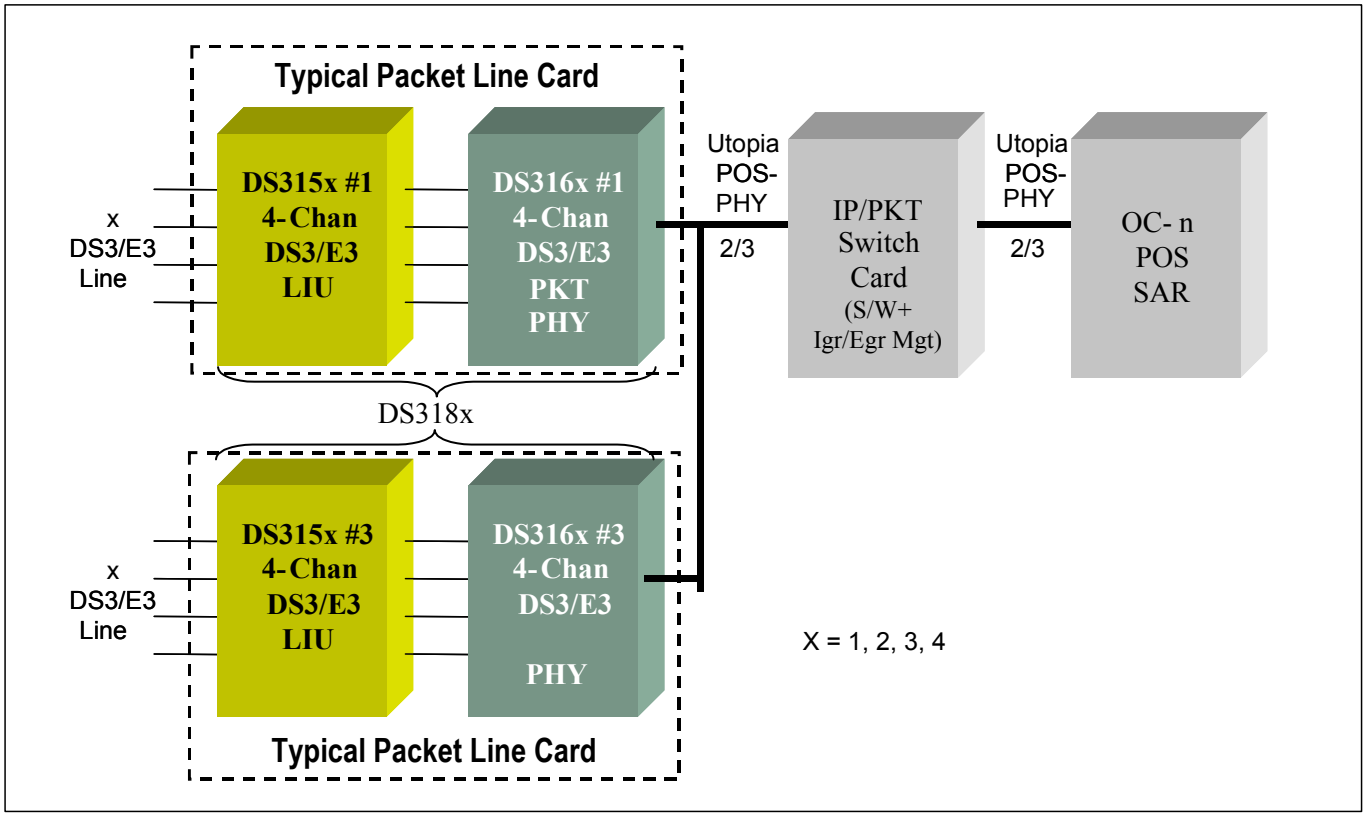


Figure 2-2. Four-Port Unchannelized HDLC over DS3/E3/CC52 Line Card



3 FEATURE DETAILS

The following sections describe the features provided by the DS3161 (single), DS3162 (dual), DS3163 (triple), and DS3164 (quad) PHYs.

- Each port independently configurable
- Universal PHYs map ATM cells and/or HDLC packets into DS3 or E3 data streams
- UTOPIA L2/L3 or POS-PHY L2/L3 OR SPI-3 interface with 8-, 16-, or 32-bit bus
- 66MHz UTOPIA L3 and POS-PHY L3 clock
- 52MHz UTOPIA L2 and POS-PHY L2 clock
- Ports independently configurable for cell or packet traffic in POS-PHY bus modes
- Direct, PLCP, DSS, and clear-channel cell mapping
- Direct and clear-channel packet mapping
- On-chip DS3 (M23 or C-bit) and E3 (G.751 or G.832) framer(s)
- Ports independently configurable for DS3, E3 (full or sub-rate) or arbitrary framing protocols up to 52 Mbps
- Programmable (externally controlled or internally finite state machine controlled) subrate DS3/E3
- Full featured DS3/E3/PLCP alarm generation and detection
- Built-in HDLC controllers with 256-byte FIFOs for the insertion/extraction of DS3 PMDL, G.751 Sn bit and G.832 NR/GC bytes, and PLCP NR/GC bytes
- On-chip BERTs for PRBS and repetitive pattern generation, detection, and analysis
- Large performance-monitoring counters for accumulation intervals of at least 1 second
- Flexible overhead insertion/extraction ports for DS3, E3, and PLCP framers
- Loopbacks include line, diagnostic, framer, payload, terminal, and system interface with capabilities to insert AIS in the directions away from loopback directions
- Ports can be disabled to reduce power
- Integrated Clock Rate Adapter to generate the remaining internally required 44.736MHz (DS3), 34.368MHz (E3), and 52MHz (arbitrary framing at up to 52 Mbps) from a single clock reference source at one of those three frequencies
- Pin and Software Compatible with DS3181–DS3184 Single–Quad ATM/Packet PHYs with Built-In LIUs and DS3171–DS3174 Single–Quad DS3/E3 Single-Chip Transceivers—Framers and LIUs
- 8/16-bit generic microprocessor interface
- Low power (1.6W typ) 3.3V operation (5V tolerant I/O)
- Small high-density thermally enhanced BGA packaging (TE-PBGA) with 1.27mm pin pitch
- Industrial temperature operation: -40°C to 85°C
- IEEE1149.1 JTAG test port

3.1 Global Features

- System interface configurable for UTOPIA L2 / UTOPIA L3 for ATM cell traffic or POS-PHY L2 / POS-PHY L3 or SPI-3 for HDLC packets or mixed packet/cell traffic
- Supports the following transmission protocols:
    - Direct-mapped ATM over DS3 or sub-rate DS3
    - PLCP-mapped ATM over DS3
    - Direct-mapped ATM over G.751 E3 or sub-rate G.751 E3
    - PLCP-mapped ATM over G.751 E3
    - Direct-mapped ATM over G.832 E3 or sub-rate G.832 E3
    - Bit or byte synchronous (octet-aligned) direct-mapped ATM over externally-defined frame formats up to 52 Mbps
    - Clear-channel ATM (cell-based physical layer) at line rates up to 52 Mbps
    - Clear-channel ATM DSS at line rates up to 52 Mbps
    - Direct-mapped HDLC over DS3 or sub-rate DS3
    - Direct-mapped HDLC over G.751 E3 or sub-rate G.751 E3
    - Direct-mapped HDLC over G.832 E3 or sub-rate G.832 E3
    - Bit or byte synchronous (octet-aligned) direct-mapped HDLC over externally-defined frame formats up to 52 Mbps

    - Clear-channel HDLC at line rates up to 52 Mbps
- In UTOPIA bus mode, ports are independently configurable for any ATM protocol
- In POS-PHY bus mode, ports are independently configurable for any ATM or HDLC protocol
- Programmable to support internally or externally controlled sub-rate DS3 or E3 on any ports
- Supports gapped 52 MHz clock rates for signals embedded in SONET/SDH
- Optional transmit loop timed clock(s) mode usingthe associated port's receive clock(s)
- Optional transmit clock mode using references generated by the internal Clock Rate Adapter (CLAD)
- Requires only a single reference clock for all three data rates using internal CLAD
- Clock, data and control signals can be inverted for a direct interface to many other devices
- Detection of loss of transmit clock and loss of receive clock
- Automatic one-second, external or manual update of performance monitoring counters
- Each port can be placed into a low-power standby mode when not being used
- Framing and line code error insertion available

3.2 Receive DS3/E3 Framer Features

- Frame synchronization for M23 or C-bit Parity DS3,or G.751 E3 or G.832 E3
- B3ZS/HDB3/AMI decoding
- Detection and accumulation of bipolar violations (BPV), code violations (CV), excessive zeroes occurrences (EXZ), F-bit errors, M-bit errors, FAS errors, LOF occurrences, P-bit parity errors, CP-bit parity errors, BIP-8 errors, and far end block errors (FEBE)
- Detection of RDI, AIS, DS3 idle signal, loss of signal (LOS), severely errored framing event (SEFE), change of frame alignment (COFA), receipt of B3ZS/HDB3 codewords, DS3 application ID bit,DS3 M23/C-bit format mismatch, G.751 national bit, and G.832 RDI (FERF), payload type, and timing marker bits
- HDLC port for DS3 path maintenance data link (PMDL), G.751 national bit or G.832 NR or GC channels
- FEAC port for DS3 FEAC channel
- 16-byte Trail Trace Buffer port for G.832 trail access point identifier
- DS3 M23 C bits, and stuff bits configurable as payload or overhead, stored in registers for software inspection
- Most framing overhead fields presented on the receive overhead port
- Support for internal and external subrate DS3/E3 control (Fractional DS3/E3)

3.3 Receive PLCP Framer Features

- PLCP frame synchronization
- C1 cycle/stuff counter interpretation
- Detection of out of frame (OOF), BIP-8 errors, FEBE and RAI (Yellow Signal)
- Frame timing can be presented on the GPIO2 output pin or used as the transmit PLCP reference
- All path overhead fields presented on the PLCP receive overhead port
- HDLC port for data link messages on F1, M1 or M2 bytes
- Trail Trace port for trace messages on F1 byte

3.4 Receive Cell Processor Features

- HEC-based cell delineation within the DS3/E3 frame, the PLCP frame, an externally defined frame, or the entire line bandwidth
- Cell de-scrambling using the self-synchronizing scrambler ($x^{43}+1$) for ATM over DS3/E3
- Distributed Sample Scrambler (DSS) for clear-channel ATM (cell-based physical layer)
- HEC error detection and correction; HEC discard
- Filtering of idle, unassigned and/or invalid cells (provisionable)
- Header pattern comparison vs. 32-bit header pattern and mask registers; counting of matching or non-matching cells; discard of matching or non-matching cells
- Four-cell Receive FIFO
- Controls include enables/disables/settings for: cell processing, coset polynomial addition, error correction, erred cell extraction, cell de-scrambling, idle/unassigned/invalid cell filtering, header pattern match counting/discarding, LCD integration time
- Status fields include: out of cell delineation (OCD), loss of cell delineation (LCD) and receipt of idle, unassigned, invalid, erred, corrected or header-pattern-match cells

- Performance monitoring counters for forwarded cells, corrected cells, uncorrectable cells, header pattern match/no-match cells, and filtered idle/unassigned/invalid cells
- Octet alignment option for externally defined frame formats

3.5 Receive Packet Processor Features

- Packet de-scrambling using the self-synchronizing scrambler ($x^{43}+1$)
- Flag detection, packet delineation, and inter-frame fill discard (flags and all-ones)
- Packet abort detection and accumulation
- Bit or octet de-stuffing
- FCS checking (16-bit or 32-bit), error accumulation, and FCS discard
- Packet size checking vs. programmable minimum and maximum size registers
- Abort declaration for packets with non-integral number of bytes
- Controls include enables/disables/settings for: packet processing, de-scrambling, 16/32-bit FCS, filtering of FCS erred packets, FCS discard, minimum/maximum packet size
- Status fields include: receipt of FCS erred packet, aborted packet, size violation packet, non-integer-length packets
- Performance monitoring counters for forwarded packets, forwarded bytes, aborted bytes, FCS erred packets, aborted packets, size violation packets (min, max, non-integer-length)
- Octet alignment with octet de-stuffing option for externally defined frame formats

3.6 Receive FIFO Features

- Storage capacity for four cells or 256 bytes of packet data per port
- Programmable port address
- Programmable fill level thresholds
- Underflow and overflow status indications

3.7 Receive System Interface Features

- UTOPIA L2 / UTOPIA L3 interface in cell mode, POS-PHY L2 / POS-PHY L3 or SPI-3 interface in packet or mixed traffic modes
- 8, 16, or 32-bit data bus at clock rates from 10 MHz to 66 MHz (52 MHz in L2 modes)
- Polled and direct cell available outputs
- Controls include enables/disables/settings for: HEC transfer, signal inversions, parity enable/polarity, cell available de-assertion time

3.8 Transmit System Interface Features

- UTOPIA L2 / UTOPIA L3 interface in cell mode, POS-PHY L2 / POS-PHY L3 or SPI-3 interface in packet or mixed traffic modes
- 8, 16, or 32-bit data bus at clock rates from 10 MHz to 66 MHz (52 MHz in L2 modes)
- Polled and direct cell available outputs
- Controls include enables/disables/settings for: HEC transfer, signal inversions, parity enable/polarity, cell available de-assertion time

3.9 Transmit FIFO Features

- Storage capacity for four cells or 256 bytes of packet data per port
- Programmable port address
- Programmable fill level thresholds
- Underflow and overflow status indications

3.10 Transmit Cell Processor Features

- Programmable fill cell type
- HEC calculation and insertion/overwrite, including coset addition
- Cell scrambling using the self-synchronizing scrambler ($x^{43}+1$) for ATM over DS3/E3
- Distributed Sample Scrambler (DSS) for clear-channel ATM (cell-based physical layer)

- Single-bit and multiple-bit header error insertion for diagnostics
- Controls include enables/disables/settings for: cell processing, HEC insertion, coset polynomial addition, cell scrambling, fill cell type, error insertion type/rate/count, HEC bit corruption
- Counter for number of cells read from the transmit FIFO
- Cell mapping into the DS3/E3 frame, the PLCP frame, an externally defined frame, or the entire line bandwidth
- Octet alignment option for externally defined frame formats

3.11 Transmit Packet Processor Features

- FCS calculation (16-bit or 32-bit) and insertion/overwrite
- Programmable FCS error insertion for diagnostics
- Bit or octet stuffing
- Programmable inter-frame fill insertion (flags or all-ones)
- Automatic packet abort insertion
- Packet scrambling using the self-synchronizing scrambler ($x^{43}+1$)
- Controls include enables/disables/settings for: packet processing, FCS insertion or overwrite, 16/32-bit FCS, inter-frame fill type/length, scrambling, FCS error insertion type/rate/count
- Counters for number of packets and bytes read from the transmit FIFO
- Octet alignment with octet stuffing option for externally defined frame formats

3.12 Transmit PLCP Formatter Features

- Insertion of FAS bytes (A1, A2), path overhead identification (POI) bytes, and path overhead bytes
- Generation of BIP-8 (B1), FEBE and RAI (G1)
- C1 cycle/stuff counter generation referenced to GPIO4 input pin, referenced to the received PLCP timing, or based on an 8 kHz division of one of the clock sources
- Automatic or manual insertion of FAS errors, BIP-8 errors
- All path overhead fields can be sourced from the PLCP transmit overhead port
- HDLC port for data link messages on F1, M1 or M2 bytes
- Trail Trace port for trace messages on F1 byte

3.13 Transmit DS3/E3 Formatter Features

- Insertion of framing overhead for M23 or C-bit parity DS3,or G.751 E3 or G.832 E3
- B3ZS/HDB3 encoding
- Generation of RDI, AIS, and DS3 idle signal
- Automatic or manual insertion of bipolar violations (BPVs), excessive zeroes (EXZ) occurrences, F-bit errors, M-bit errors, FAS errors, P-bit parity errors, CP-bit parity errors, BIP-8 errors, and far end block errors (FEBE)
- HDLC port for DS3 path maintenance data link (PMDL), G.751 national bit or G.832 NR or GC channels
- FEAC port for DS3 FEAC channel can be configured to send one codeword, one codeword continuously, or two different codewords back-to-back to send DS3 Line Loopback commands
- 16-byte Trail Trace Buffer port for the G.832 trail access point identifier
- Insertion of G.832 payload type, and timing marker bits from registers
- DS3 M23 C bits configurable as payload or overhead; as overhead they can be controlled from registers or the transmit overhead port
- Most framing overhead fields can be sourced from transmit overhead port
- Formatter bypass mode for clear channel or externally defined format applications
- Support for subrate DS3/E3, internally or externally controlled (Fractional DS3/E3)

3.14 Clock Rate Adapter Features

- Generation of the internally needed DS3 (44.736 MHz), E3 (34.368 MHz), and STS-1(51.84 MHz) clocks a from single input reference clock
- Input reference clock can be 51.84 MHz, 44.736MHz or 34.368 MHz
- Derived clocks can be transmitted off-chip for external system use
- Standards compliant jitter and wander requirements.

3.15 HDLC Overhead Controller Features

- Each port has a dedicated HDLC controller for DS3/E3 framer or PLCP link management
- 256-byte receive and transmit FIFOs
- Handles all of the normal Layer 2 tasks including zero stuffing/de-stuffing, FCS generation/checking, abort generation/checking, flag generation/detection, and byte alignment
- Programmable high and low water marks for the transmit and receive FIFOs
- Terminates the Path Maintenance Data Link in DS3 C-bit Parity mode and optionally the G.751 Sn bit or the G.832 NR or GC channels or PLCP F1, M1 or M2 bytes
- RX data is forced to all ones during LOS, LOF and AIS detection to eliminate false packets

3.16 FEAC Controller Features

- Each port has a dedicated FEAC controller for DS3/E3 link management
- Designed to handle multiple FEAC codewords without Host intervention
- Receive FEAC automatically validates incoming codewords and stores them in a 4-byte FIFO
- Transmit FEAC can be configured to send one codeword, one codeword continuously, or two different codewords back-to-back to send DS3 Line Loopback commands
- Terminates the FEAC channel in DS3 C-Bit Parity mode and optionally the Sn bit in E3 mode

3.17 Trail Trace Buffer Features

- Each port has a dedicated Trail Trace Buffer for E3-G.832 or DS3/E3 PLCP link management
- Extraction and storage of the incoming G.832 or PLCP trail access point identifier in a 16-byte receive register
- Insertion of the outgoing trail access point identifier from a 16-byte transmit register
- Receive trace identifier unstable status indication

3.18 Bit Error Rate Tester (BERT) Features

- Each port has a dedicated BERT tester
- Generation and detection of pseudo-random patterns and repetitive patterns from 1 to 32 bits in length
- Pattern insertion/extraction in PLCP payload, DS3/E3 payload, DS3/E3 fractional payload or entire data stream to and from the line interface
- Large 24-bit error counter allows testing to proceed for long periods without host intervention
- Errors can be inserted in the generated BERT patterns for diagnostic purposes (single bit errors or specific bit-error rates)

3.19 Loopback Features

- Analog interface loopback – ALB (transmit to receive)
- Line facility loopback – LLB (receive to transmit) with optional transmission of unframed all-one AIS payload toward system/trunk interface
- Framer diagnostic loopback – DLB (transmit to receive) with automatic transmission of DS3 AIS or unframed all-one AIS signal toward line/tributary interface(s)
- DS3/E3 framer payload loopback – PLB (receive to transmit) with optional transmission of unframed all-one AIS payload toward system/trunk interface
- System interface loopback – SLB (transmit to receive)
- Simultaneous line facility loopback and framer diagnostic loopback

3.20 Microprocessor Interface Features

- Multiplexed or non-multiplexed address bus modes
- 8 or 16-bit data bus modes
- Byte swapping option in 16-bit data bus mode
- Read/Write and Data Strobe modes
- Ready handshake output signal
- Global reset input pin
- Global interrupt output pin

- Two programmable I/O pins per port

3.21 Subrate Features (Fractional DS3/E3)

- Independent per port built-in support for subrate DS3 or E3
- Independent subrate operation for both RX and TX data paths
- Subrate operation for each channel is totally independent from the other channels' operation, i.e. all subrate functions within the device are mutually exclusive
- Three distinct subrate algorithms:
  - (FFRAC) Externally controlled with DS3 or E3 payload manipulating capability
  - (XFRAC) Externally controlled with flexible DS3 or E3 data rate reduction capability
  - (IFRAC) Internally controlled with simple DS3 or E3 data rate reduction capability
- Subrate algorithm selection is on per port basis
- Internal subrate mechanism allows down to bit-level granularity of the DS3 or E3 payload

3.22 Test Features

- Five pin JTAG port
- All functional pins are inout pins in JTAG mode
- Standard JTAG instructions: Sample/Preload, Bypass, Extest, Clamp, HighZ, Idcode
- RAM BIST on all internal RAM
- Hi-Z pin to force all digital output and inout pins into HIZ
- TEST pin for manufacturing scan test modes

4 STANDARDS COMPLIANCE

Table 4-1. Standards Compliance

SPECIFICATION	SPECIFICATION TITLE
ANSI	
T1.102-1993	*Digital Hierarchy – Electrical Interfaces*
T1.107-1995	*Digital Hierarchy – Formats Specification*
T1.231-1997	*Digital Hierarchy – Layer 1 In-Service Digital Transmission Performance Monitoring*
T1.404-1994	*Network-to-Customer Installation – DS3 Metallic Interface Specification*
T1.646-1995	*Broadband ISDN – Physical Layer Specification for User-Network Interfaces Including DS1/ATM*
ATM Forum	
af-phy-0034.000	*E3 Public UNI,* August, 1995
af-phy-0039.000	*UTOPIA Level 2, Version 1.0,* June, 1995
af-phy-0043.000	*A Cell-Based Transmission Convergence Sublayer for Clear-Channel Interfaces,* November, 1995
af-phy-0054.000	*DS3 Physical Layer Interface Specification,* January, 1996
af-phy-0136.000	*UTOPIA L3 Physical Layer Interface,* November, 1999
af-phy-0143.000	*Frame-based ATM Interface (Level 3),* March, 2000
af-bici-0013.003	*BISDN Inter Carrier Interface (B-ICI) Specification Version 2.0 (Integrated),* December, 1995
ETSI	
ETS 300 686	*Business TeleCommunications; 34Mbps and 140Mbits/s digital leased lines (D34U, D34S, D140U and D140S); Network interface presentation, 1996*
ETS 300 337	*Transmission and Multiplexing (TM); Generic frame structures for the transport of various signals (including Asynchronous Transfer Mode (ATM) cells and Synchronous Digital Hierarchy (SDH) elements) at the ITU-T Recommendation G.702 hierarchical rates of 2 048 kbit/s, 34 368 kbit/s and 139 264 kbit/s*, Second Edition, June, 1997
ETS EN 300 689	*Access and Terminals (AT); 34Mbps Digital Leased Lines (D34U and D34S); Terminal equipment interface,* July 2001
ETS 300 689	*Business TeleCommunications (BTC); 34 Mbps digital leased lines (D34U and D34S), Terminal equipment interface*, V 1.2.1, 2001-07
IETF	
RFC 1661	*The Point-to-Point Protocol (PPP)*, July, 1994
RFC 1662	*PPP in HDLC-like Framing*, July, 1994
RFC 2496	*Definition of Managed Objects for the DS3/E3 Interface Type*, January, 1999
ISO	
ISO 3309:1993	*Information Technology – Telecommunications & information exchange between systems – High Level Data Link Control (HDLC) procedures – Frame structure*, Fifth Edition, 1993
ITU-T	
G.703	*Physical/Electrical Characteristics of Hierarchical Digital Interfaces,* 1991
G.704	*Synchronous Frame Structures Used at 1544, 6312, 2048, 8488 and 44 736 kbit/s Hierarchical Levels,* July, 1995
G.751	*Digital Multiplex Equipment Operating at the Third Order Bit Rate of 34,368 kbit/s and the Fourth Order bit Rate of 139,264 kbit/s and Using Positive Justification,* 1993
G.775	*Loss Of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria,* November, 1994
G.804	*ATM Cell Mapping Into Plesiochronous Digital Hierarchy (PDH),* November, 1993
G.823	*The Control of Jitter and Wander Within Digital Networks Which are Based on the 2048 kbit/s Hierarchy*, 1993
G.824	*The Control of Jitter and Wander within Digital Networks that are Based on the 1544kbps Hierarchy*, 1993
G.832	*Transport of SDH Elements on PDH Networks – Frame and Multiplexing Structures,* November, 1995

SPECIFICATION	SPECIFICATION TITLE
I.432	*B-ISDN User-Network Interface – Physical Layer Specification,* March, 1993
O.151	*Error Performance Measuring Equipment Operating at the Primary Rate and Above,* October, 1992
Q.921	*ISDN User-Network Interface – Data Link Layer Specification*, March 1993
OIF	
OIF-SPI3-01.0	*System Packet Interface Level 3 (SPI-3): OC-48 System Interface for Physical and Link Layer Devices*
Saturn® Group	
POS-PHY L2	*POS-PHY™ Level 2 Packet Over SONET Interface Specification for Physical Layer Devices,* December, 1998
POS-PHY L3	*POS-PHY Level 3 Packet Over SONET Interface Specification for Physical and Link Layer Devices,* June, 2000
Telcordia	
GR-253-CORE	*SONET Transport Systems: Common Generic Criteria*, Issue 2, December 1995
GR-499-CORE	*Transport Systems Generic Requirements (TSGR): Common Requirements,* Issue 2, December 1998
GR-820-CORE	*Generic Digital Transmission Surveillance*, Issue 1, November 1994
IEEE	
IEEE Std 1149-1990	*IEEE Standard Test Access Port and Boundary-Scan Architecture, (Includes IEEE Std 1149-1993)* October 21, 1993

Saturn is a registered trademark of PMC-Sierra, Inc.

5 ACRONYMS AND GLOSSARY

Definition of the terms used in this datasheet:

Acronyms

- ATM – Asynchronous Transfer Mode
- CC52 – Clear-Channel 52 Mbps (STS-1 Clock Rate)
- CLAD – Clock Rate Adapter
- CLR – Clear-Channel Mode
- DSS – Distributed Sample Scrambler
- FFRAC – Flexible Fractional Mode
- FRM – Frame Mode
- HDLC – High Level Data Link Control
- IFRAC – Internal Fractional Mode
- OHM – Overhead Mask mode for externally defined framing
- PLCP – Physical Layer Convergence Protocol
- SPI-3 – same as POS-PHY L3
- XFRAC – External Fractional Mode

Glossary

- Cell – ATM cell
- Clear Channel – A datastream with no framing included
- Fractional – Uses only a portion of available payload for data, also known as subrate
- Octet Aligned – Byte aligned
- Packet – HDLC packet
- Subrate – See Fractional
- Un-channelized – See Clear Channel

6 MAJOR OPERATIONAL MODES

The major operational modes are determined by the FM[5:0] framer mode bitsand a few other control bits. Unused features are powered down and the data paths are held in reset. The configuration registers of the unused features can be written to and read from. The function of some IO pins change in different operational modes. The line interface operational modes are determined by the LM bit.

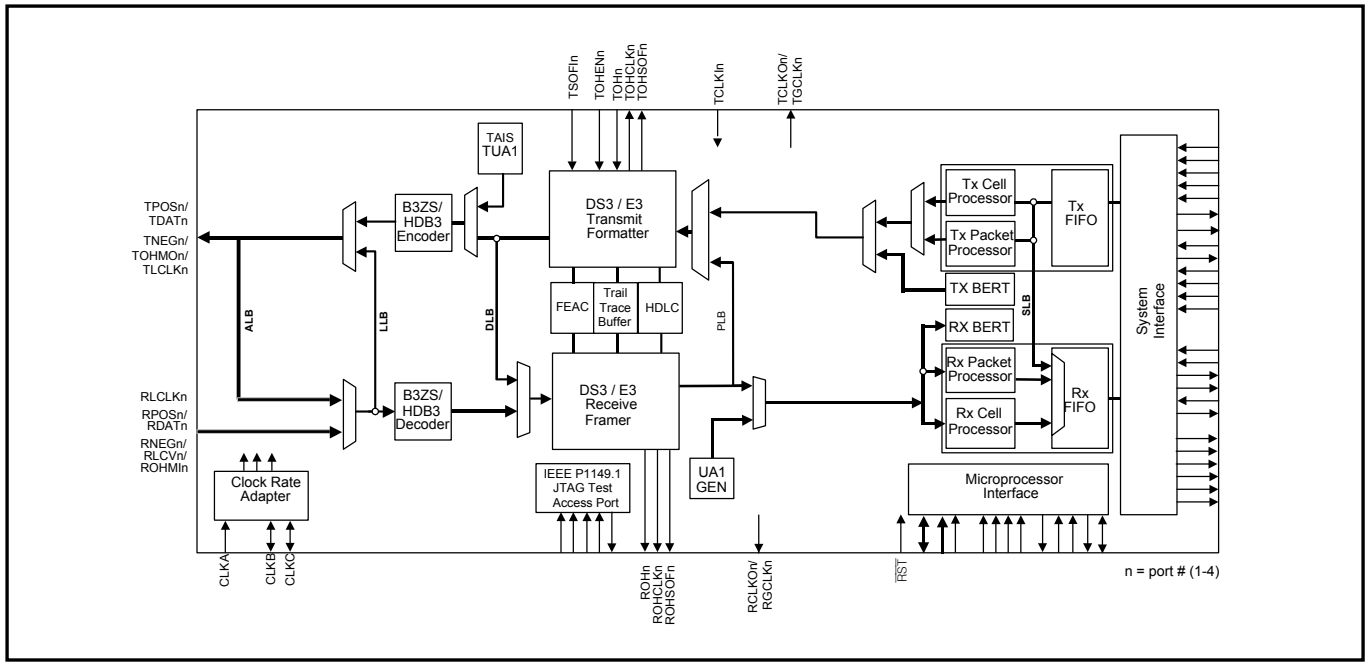
6.1 DS3/E3 ATM/Packet Mode

DS3/E3 ATM/Packet mode is a normal mode of operation for the DS316x device, which maps/de-maps ATM cells or packet data into a DS3 or E3 data stream via the selected mapping mode. Major functional blocks for the DS3/E3 ATM/Packet mode are shown in Figure 6-1. Mapping configuration is programmable on per port basis and is shown in Table 6-1.

Table 6-1. DS3/E3 ATM/Packet Mode Configuration Registers

MODE	FM[5:0]	SIM[1:0] GL.CR1	PMCPE *PORT.CR2*
UTOPIA L2 ATM	0XX000	00	X
UTOPIA L3 ATM	0XX000	01	X
POS-PHY L2 ATM	0XX000	10	1
POS-PHY L3 ATM	0XX000	11	1
POS-PHY L2 Packet	0XX000	10	0
POS-PHY L3 Packet	0XX000	11	0

Figure 6-1. DS3/E3 ATM/Packet Mode



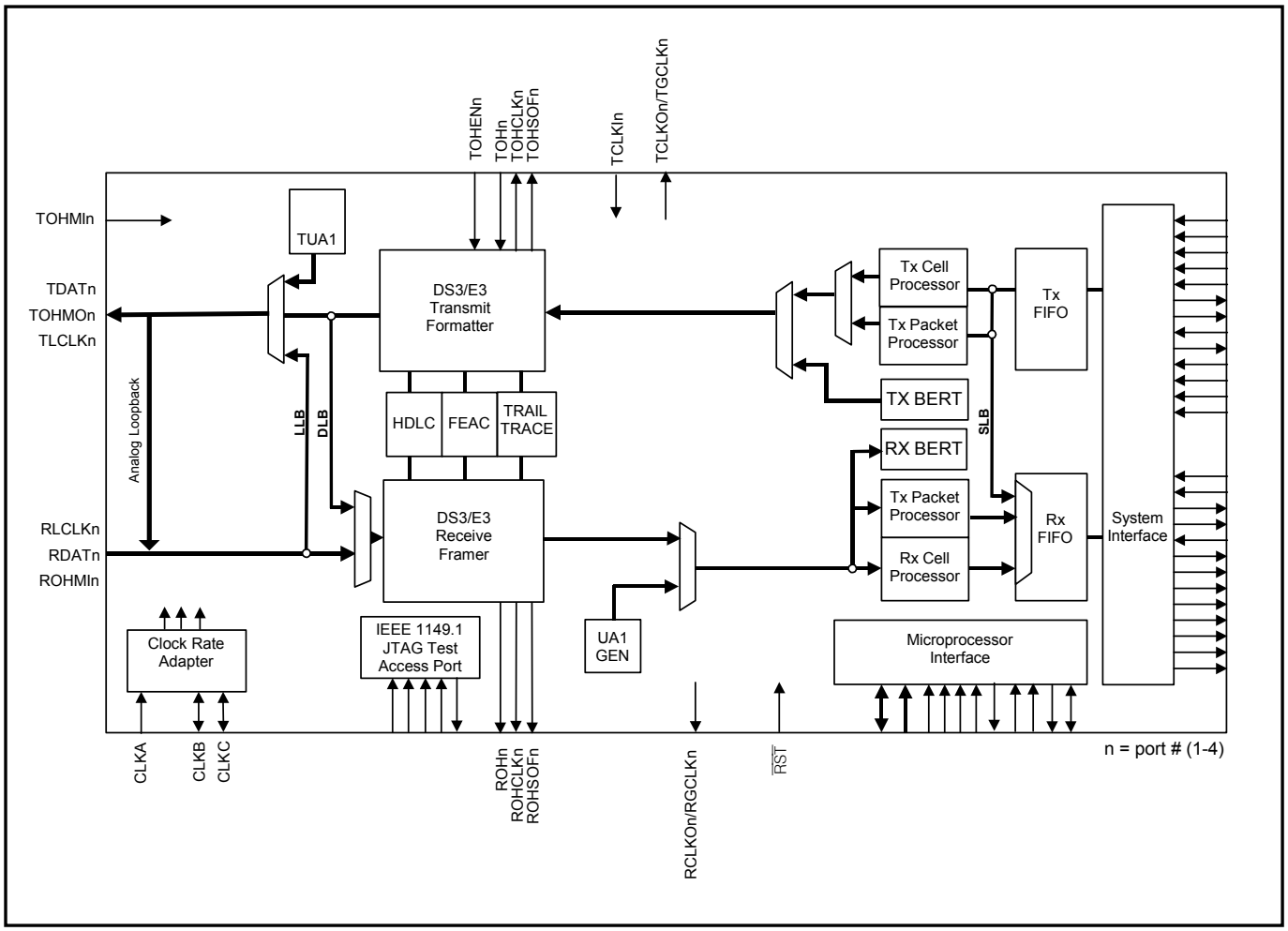
6.2 DS3/E3 ATM/Packet—OHM Mode

DS3/E3 ATM/Packet—OHM Mode is a normal mode of operation for the DS316x device, which maps/de-maps ATM cells or packet data into a DS3 or E3 data stream, supporting externally defined framing protocols. Major functional blocks for the DS3/E3 ATM/Packet—OHM Mode are shown in Figure 6-2. Mapping configuration is programmable on per port basis and is shown in Table 6-2.

Table 6-2. DS3/E3 ATM/Packet—OHM Mode Configuration Registers

MODE	FM[5:0]	SIM[1:0] GL.CR1	PMCPE *PORT.CR2*
UTOPIA L2 ATM	0XX001	00	X
UTOPIA L3 ATM	0XX001	01	X
POS-PHY L2 ATM	0XX001	10	1
POS-PHY L3 ATM	0XX001	11	1
POS-PHY L2 Packet	0XX001	10	0
POS-PHY L3 Packet	0XX001	11	0

Figure 6-2. DS3/E3 ATM/Packet—OHM Mode



6.3 DS3/E3 Internal Fractional (Subrate) ATM/Packet Mode

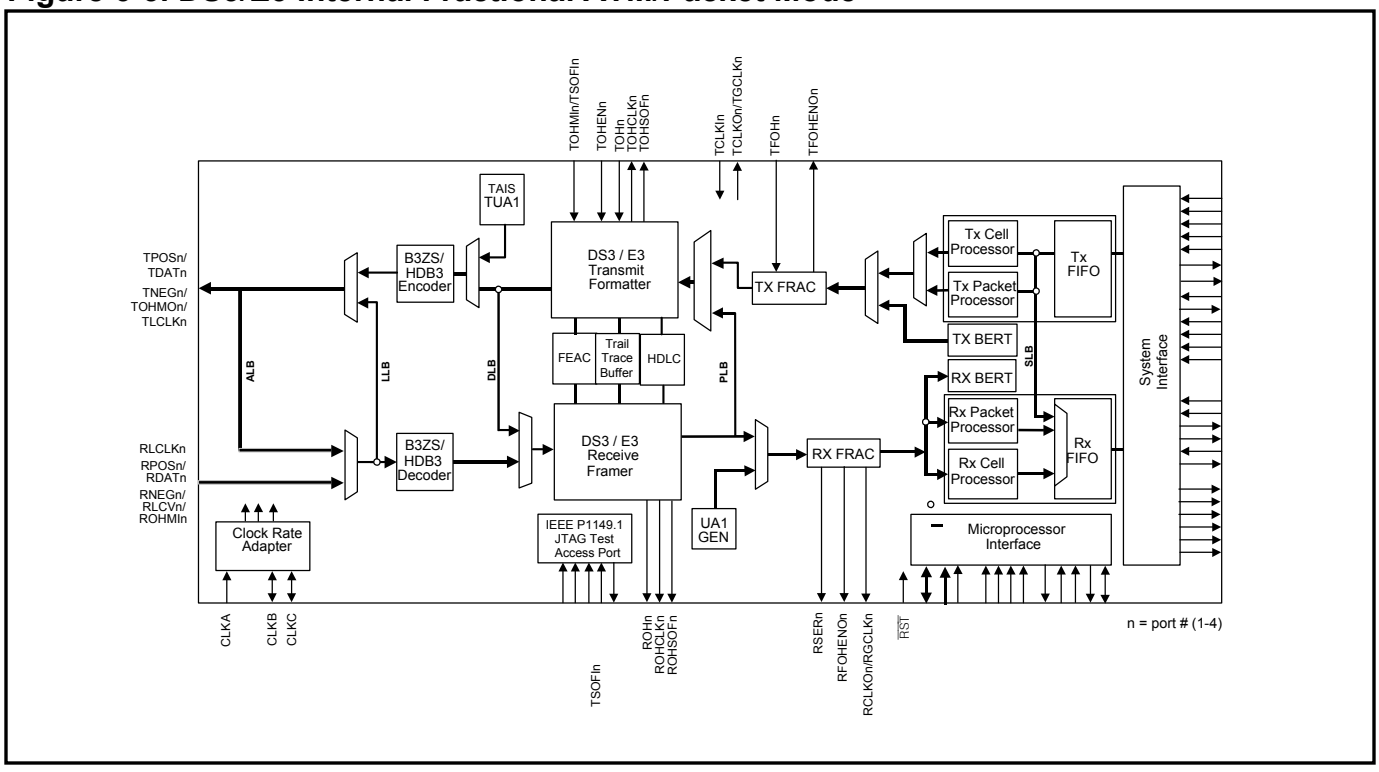
DS3/E3 Internal Fractional Mode allows subrate datastreams to be inserted into a DS3 or E3 line, with the fractional overhead internally controlled. Major functional blocks for the DS3/E3 Internal Fractional Mode are shown in Figure 6-3. Mapping configuration is programmable on per port basis and is shown in Table 6-3.

The "-OHM" modes are not allowed in fractional framing modes since the user is not able to distinguish between internal framing overhead and external framing overhead bit locations.

Table 6-3. DS3/E3 Internal Fractional (IFRAC) ATM/Packet Mode Configuration Registers

MODE	FM[5:0]	SIM[1:0] GL.CR1	PMCPE *PORT.CR2*
UTOPIA L2 ATM	0XX010	00	X
UTOPIA L3 ATM	0XX010	01	X
POS-PHY L2 ATM	0XX010	10	1
POS-PHY L3 ATM	0XX010	11	1
POS-PHY L2 Packet	0XX010	10	0
POS-PHY L3 Packet	0XX010	11	0

Figure 6-3. DS3/E3 Internal Fractional ATM/Packet Mode



6.4 DS3/E3 External Fractional (Subrate) ATM/Packet Mode

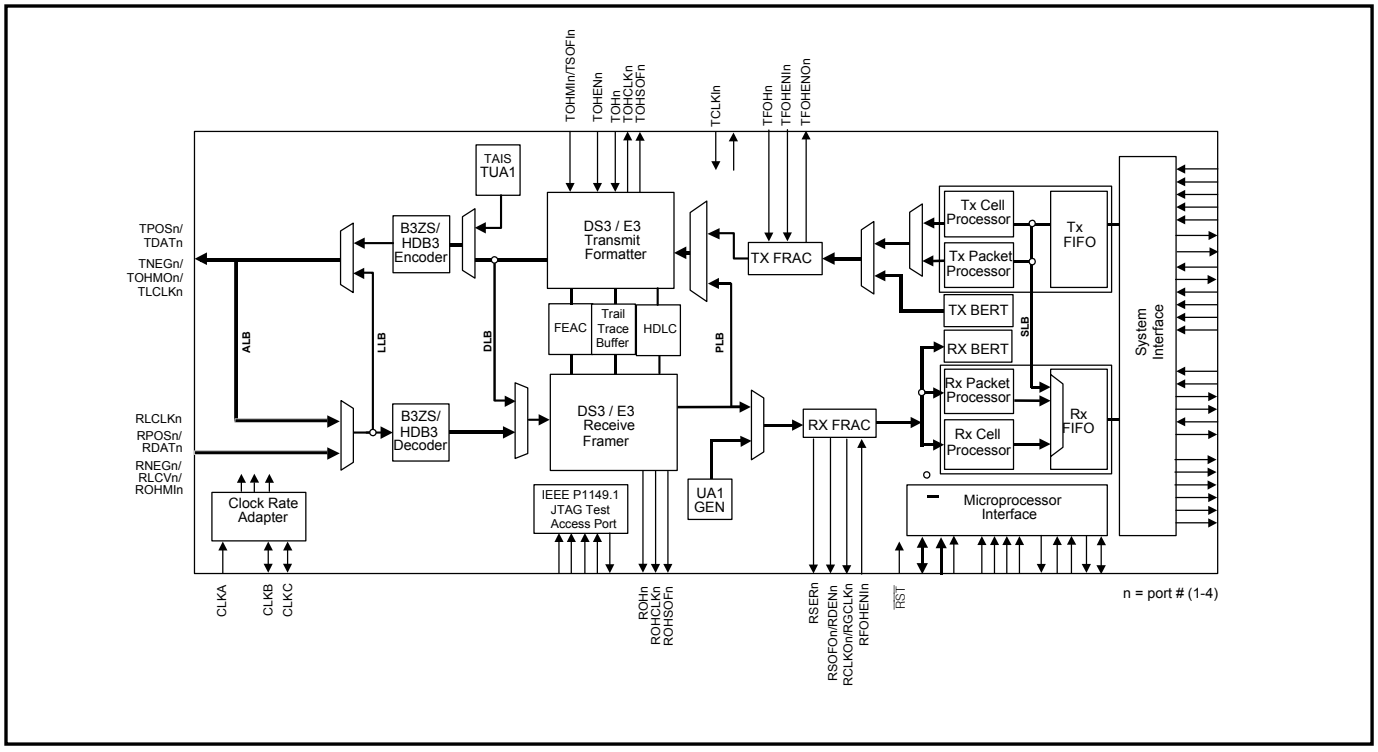
DS3/E3 External Fractional Mode allows subrate datastreams to be inserted into a DS3 or E3 line, with the fractional overhead externally controlled. Major functional blocks for the DS3/E3 Internal Fractional Mode are shown in Figure 6-4. Mapping configuration is programmable on per port basis and is shown in Table 6-4.

The "-OHM" modes are not allowed in fractional framing modes since the user cannot distinguish between internal framing overhead and external framing overhead bit locations.

Table 6-4. DS3/E3 External Fractional (XFRAC) ATM/Packet Mode Configuration Registers

MODE	FM[5:0]	SIM[1:0] GL.CR1	PMCPE *PORT.CR2*
UTOPIA L2 ATM	0XX011	00	X
UTOPIA L3 ATM	0XX011	01	X
POS-PHY L2 ATM	0XX011	10	1
POS-PHY L3 ATM	0XX011	11	1
POS-PHY L2 Packet	0XX011	10	0
POS-PHY L3 Packet	0XX011	11	0

Figure 6-4. DS3/E3 External Fractional ATM/Packet Mode



6.5 DS3/E3 Flexible External Fractional (Subrate) Mode Configuration Mode

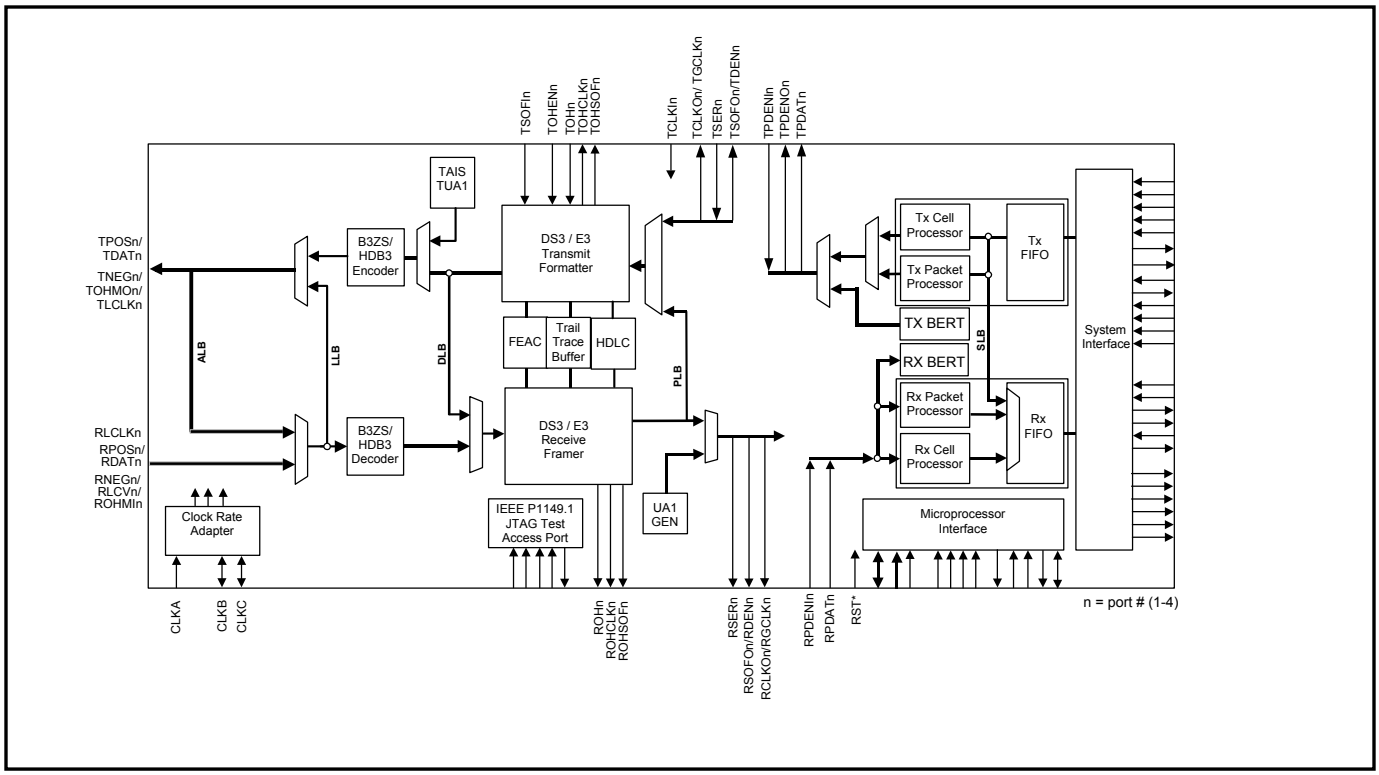
DS3/E3 Flexible External Fractional Mode allows subrate datastreams to be inserted into a DS3 or E3 line, with the fractional overhead and payload externally multiplexed. Major functional blocks for the DS3/E3 Flexible External Fractional Mode are shown in Figure 6-5. Mapping configuration is programmable on per port basis and is shown in Table 6-5.

The “-OHM” modes are not allowed in fractional framing modes since the user cannot distinguish between internal framing overhead and external framing overhead bit locations.

Table 6-5. DS3/E3 Flexible External Fractional (Subrate) Mode Configuration Registers

MODE	FM[5:0]	SIM[1:0] GL.CR1	PMCPE *PORT.CR2*
UTOPIA L2 ATM	0XX110	00	X
UTOPIA L3 ATM	0XX110	01	X
POS-PHY L2 ATM	0XX110	10	1
POS-PHY L3 ATM	0XX110	11	1
POS-PHY L2 Packet	0XX110	10	0
POS-PHY L3 Packet	0XX110	11	0

Figure 6-5. DS3/E3 Flexible External Fractional Mode



6.6 DS3/E3 G.751 PLCP ATM Mode

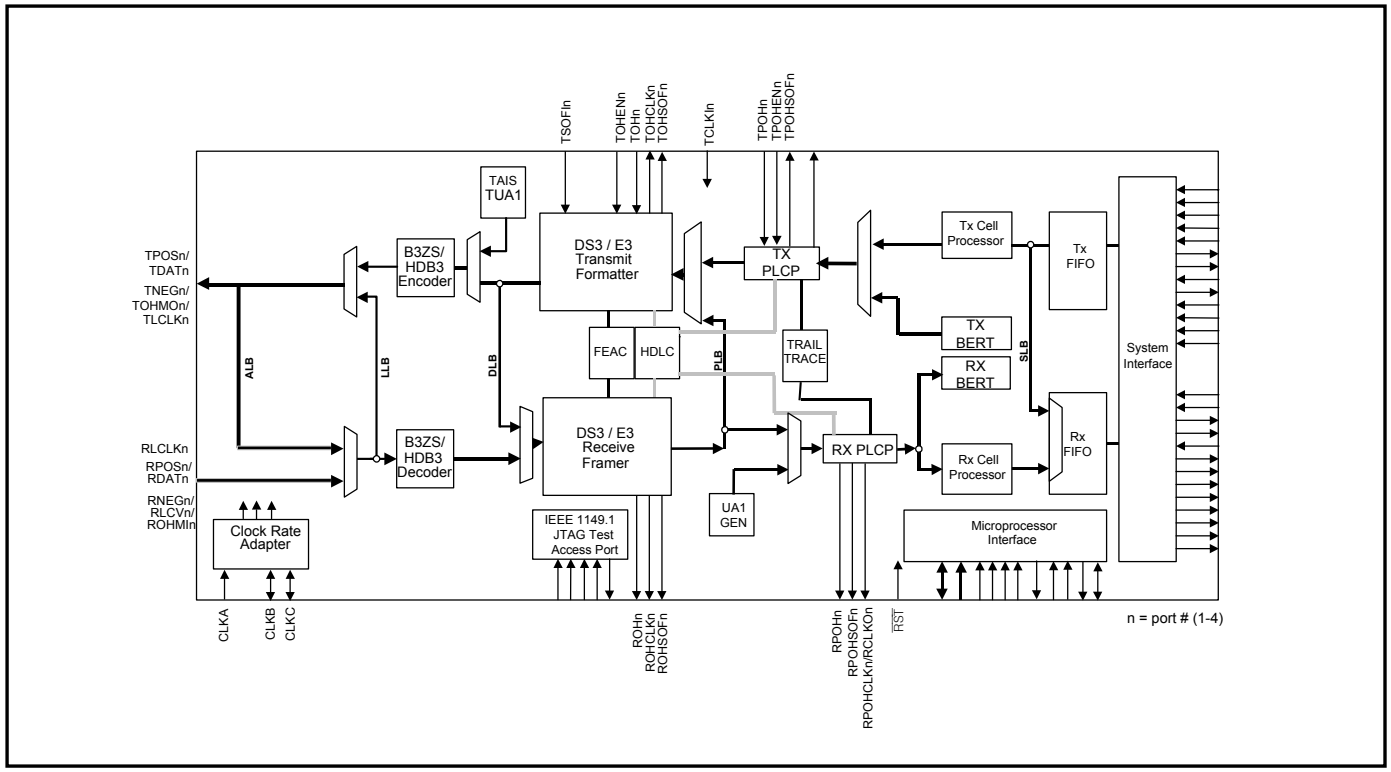
DS3/E3 G.751 PLCP ATM mode is a normal mode of operation for the DS316x device, which maps/de-maps ATM cells into/from the DS3/E3 PLCP data stream. Major functional blocks for the DS3/E3 ATM/Packet mode are shown in Figure 6-6. Mapping configuration is programmable on per port basis and is shown in Table 6-6.

The PMCPE configuration bit is ignored when in PLCP mode and ATM cell processing is forced.

Table 6-6. DS3/E3 G.751 PLCP ATM Mode Configuration Registers

MODE	FM[5:0]	SIM[1:0] GL.CR1	PMCPE *PORT.CR2*
UTOPIA L2 ATM	0XX100	00	X
UTOPIA L3 ATM	0XX100	01	X
POS-PHY L2 ATM	0XX100	10	1
POS-PHY L3 ATM	0XX100	11	1
POS-PHY L2 Packet	0XX100	10	0
POS-PHY L3 Packet	0XX100	11	0

Figure 6-6. DS3/E3 G.751 PLCP ATM Mode



6.7 DS3/E3 G.751 PLCP ATM—OHM Mode

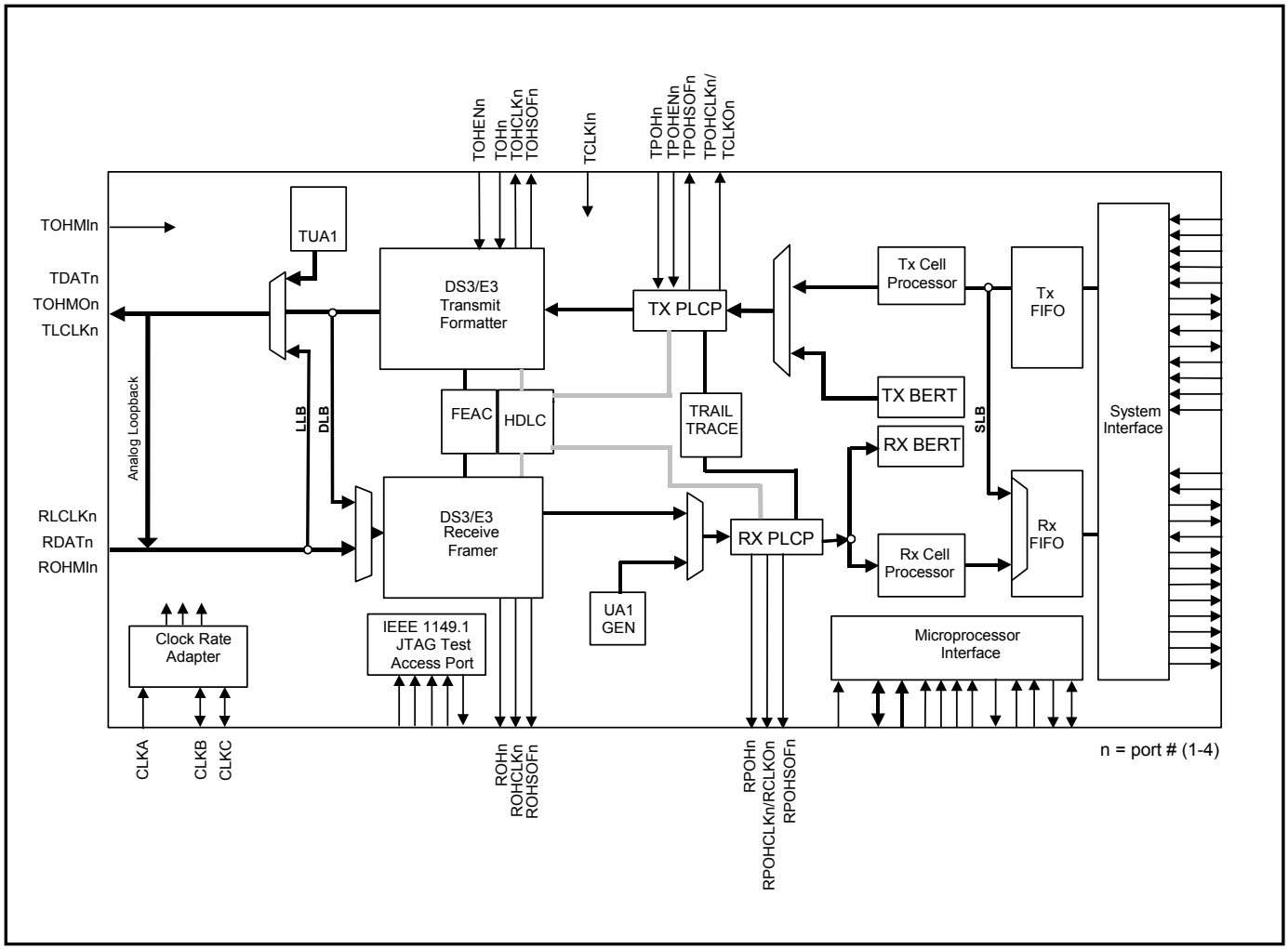
DS3/E3 G.751 PLCP ATM—OHM mode is a normal mode of operation for the DS316x device, which maps/de-maps ATM cells into/from the DS3/E3 PLCP data stream, supporting externally defined framing modes. Major functional blocks for the DS3/E3 G.751 PLCP ATM – OHM mode are shown in Figure 6-7. Mapping configuration is programmable on per port basis and is shown in Table 6-7.

The PMCPE configuration bit is ignored when in PLCP mode and ATM cell processing is forced.

Table 6-7. DS3/E3 G.751 PLCP ATM—OHM Mode Configuration Registers

MODE	FM[5:0]	SIM[1:0]	PMCPE *PORT.CR2*
DS3 UTOPIA L2 ATM	0XX101	00	X
DS3 UTOPIA L3 ATM	0XX101	01	X
DS3 POS-PHY L2 ATM	0XX101	10	X
DS3 POS-PHY L3 ATM	0XX101	11	X
E3 G.751 UTOPIA L2 ATM	010101	00	X
E3 G.751 UTOPIA L3 ATM	010101	01	X
E3 G.751 POS-PHY L2 ATM	010101	10	X
E3 G.751 POS-PHY L3 ATM	010101	11	X

Figure 6-7. DS3/E3 G.751 PLCP ATM—OHM Mode



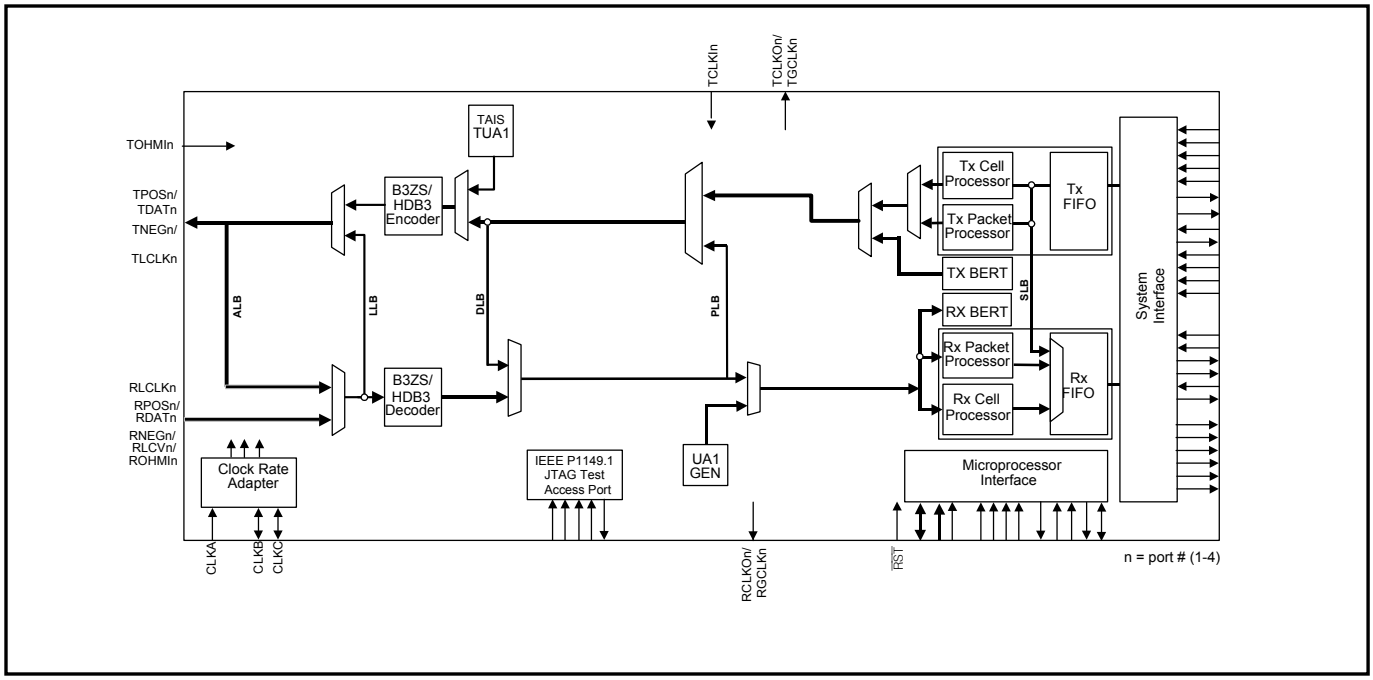
6.8 Clear-Channel ATM/Packet Mode

The Clear-Channel ATM/Packet Mode maps/de-maps ATM cells or HDLC packets into/from a serial datastream, bypassing the DS3/E3 formatter/framer. Major functional blocks for the Clear-Channel ATM/Packet Mode are shown in Figure 6-8. Mapping configuration is programmable on per port basis and is shown in Table 6-8.

Table 6-8. Clear-Channel ATM/Packet Mode Configuration Modes

MODE	FM[5:0]	SIM[1:0] GL.CR1	PMCPE *PORT.CR2*
UTOPIA L2 ATM	1XX0X0	00	X
UTOPIA L3 ATM	1XX0X0	01	X
POS-PHY L2 ATM	1XX0X0	10	1
POS-PHY L3 ATM	1XX0X0	11	1
POS-PHY L2 Packet	1XX0X0	10	0
POS-PHY L3 Packet	1XX0X0	11	0

Figure 6-8. Clear-Channel ATM/Packet Modes



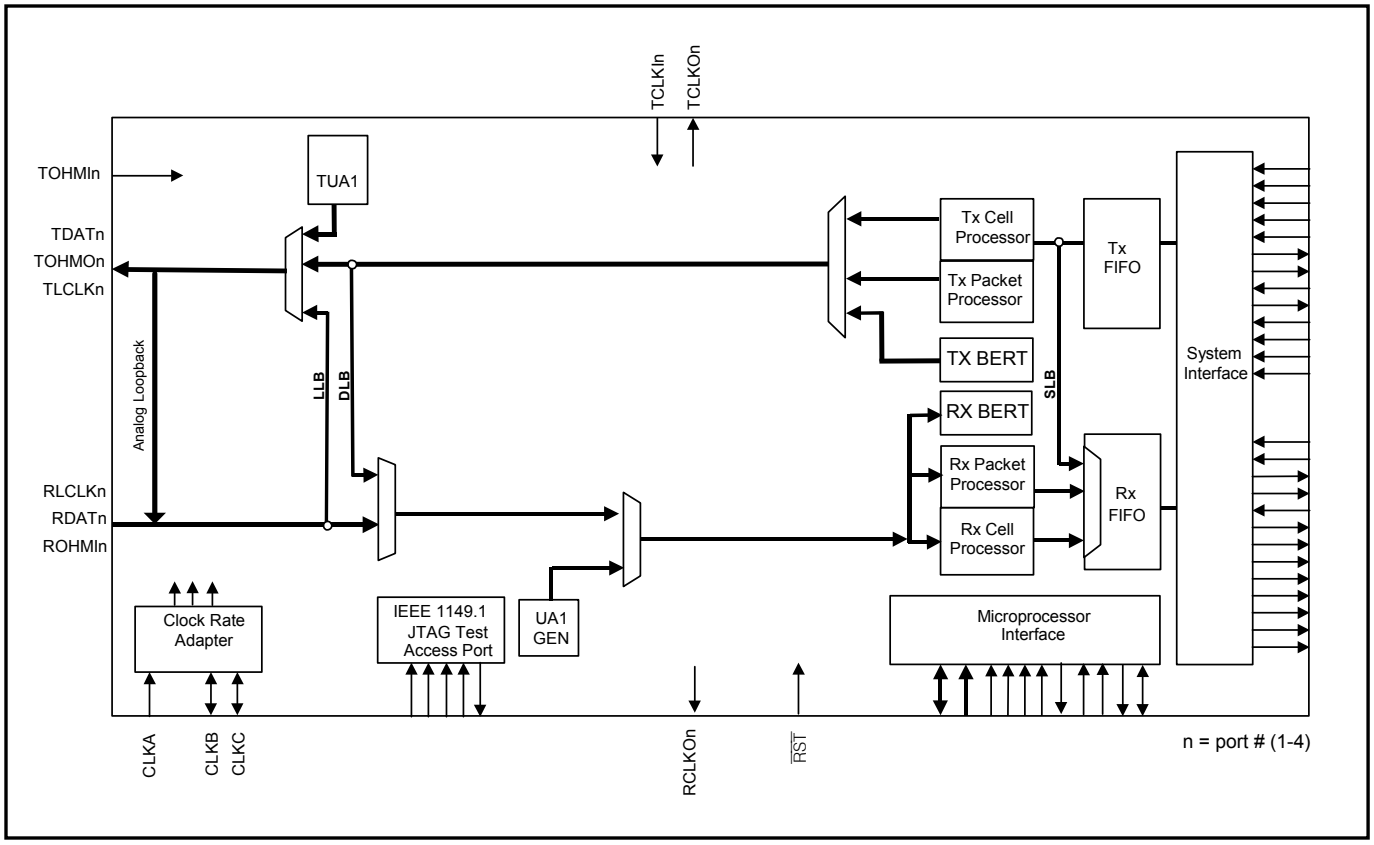
6.9 Clear-Channel ATM/Packet—OHM Mode

The Clear-Channel ATM/Packet—OHM Mode maps/de-maps ATM cells or HDLC packets into/from a serial datastream, bypassing the DS3/E3 formatter/framer, supporting externally defined framing modes. Major functional blocks for the Clear-Channel ATM/Packet—OHM Mode are shown in Figure 6-9. Mapping configuration is programmable on per port basis and is shown in Table 6-9.

Table 6-9. Clear-Channel ATM/Packet—OHM Mode Configuration Registers

MODE	FM[5:0]	SIM[1:0] GL.CR1	PMCPE *PORT.CR2*
UTOPIA L2 ATM	1XX001	00	X
UTOPIA L3 ATM	1XX001	01	X
POS-PHY L2 ATM	1XX001	10	1
POS-PHY L3 ATM	1XX001	11	1
POS-PHY L2 Packet	1XX001	10	0
POS-PHY L3 Packet	1XX001	11	0

Figure 6-9. Clear-Channel ATM/Packet—OHM Mode



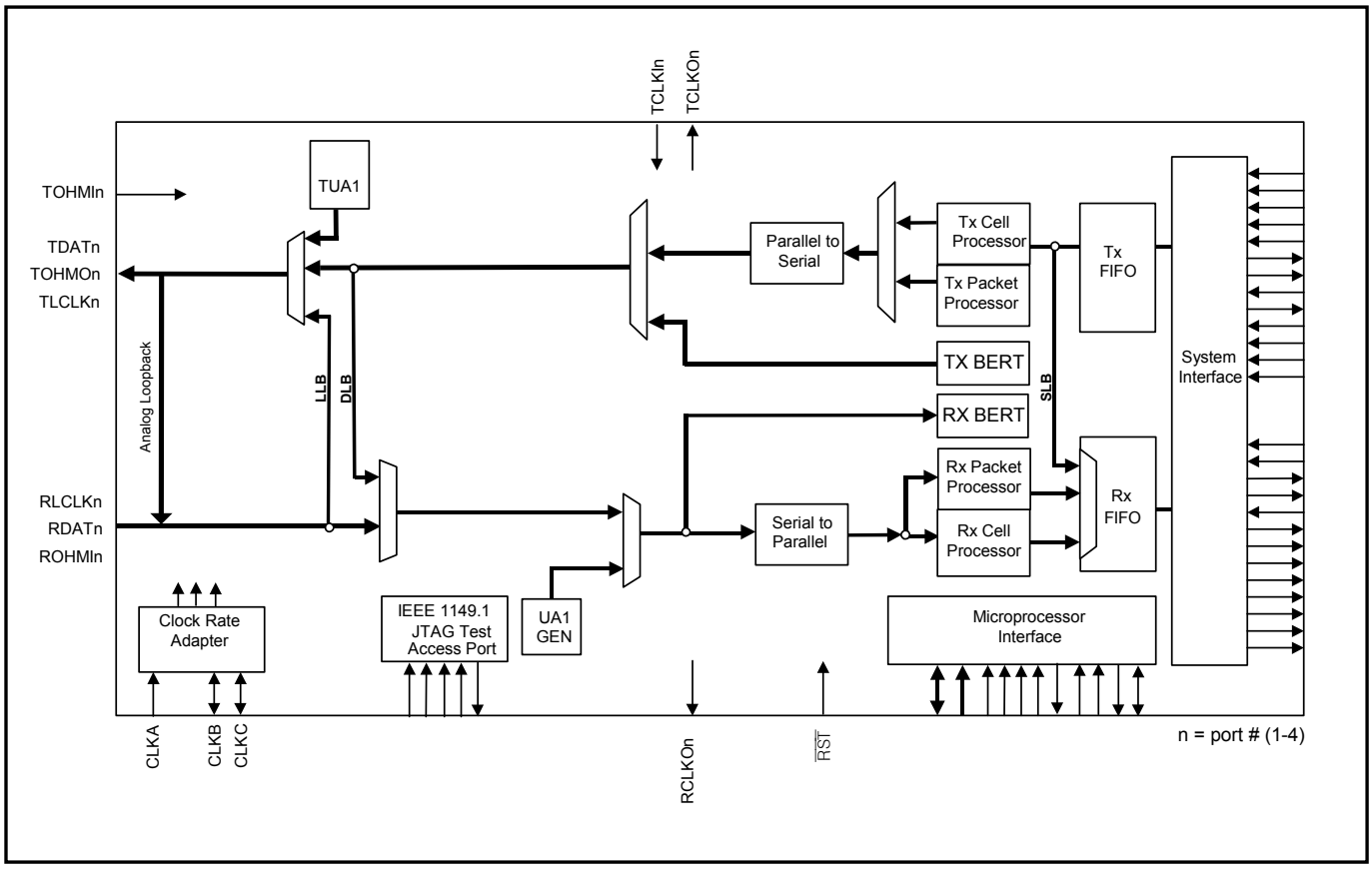
6.10 Clear-Channel Octet Aligned ATM/Packet—OHM Mode

The Clear-Channel Octet Aligned ATM/Packet—OHM Mode maps/de-maps ATM cells or HDLC packets into/from a serial datastream, bypassing the DS3/E3 formatter/framer, supporting arbitrary framing modes. Major functional blocks for the Clear-Channel Octet Aligned ATM/Packet—OHM Mode are shown in Figure 6-10. Mapping configuration is programmable on per port basis and is shown in Table 6-10.

Table 6-10. Clear-Channel Octet Aligned ATM/Packet—OHM Mode Configuration Registers

MODE	FM[5:0]	SIM[1:0] GL.CR1	PMCPE *PORT.CR2*
UTOPIA L2 ATM	1XX011	00	X
UTOPIA L3 ATM	1XX011	01	X
POS-PHY L2 ATM	1XX011	10	1
POS-PHY L3 ATM	1XX011	11	1
POS-PHY L2 Packet	1XX011	10	0
POS-PHY L3 Packet	1XX011	11	0

Figure 6-10. Clear-Channel Octet Aligned ATM/Packet—OHM Mode



7 MAJOR LINE INTERFACE OPERATING MODES

The line interface modes provide the following function:

1. Selection of the line coding type: i.e., B3ZS/HDB3/AMI or UNI.

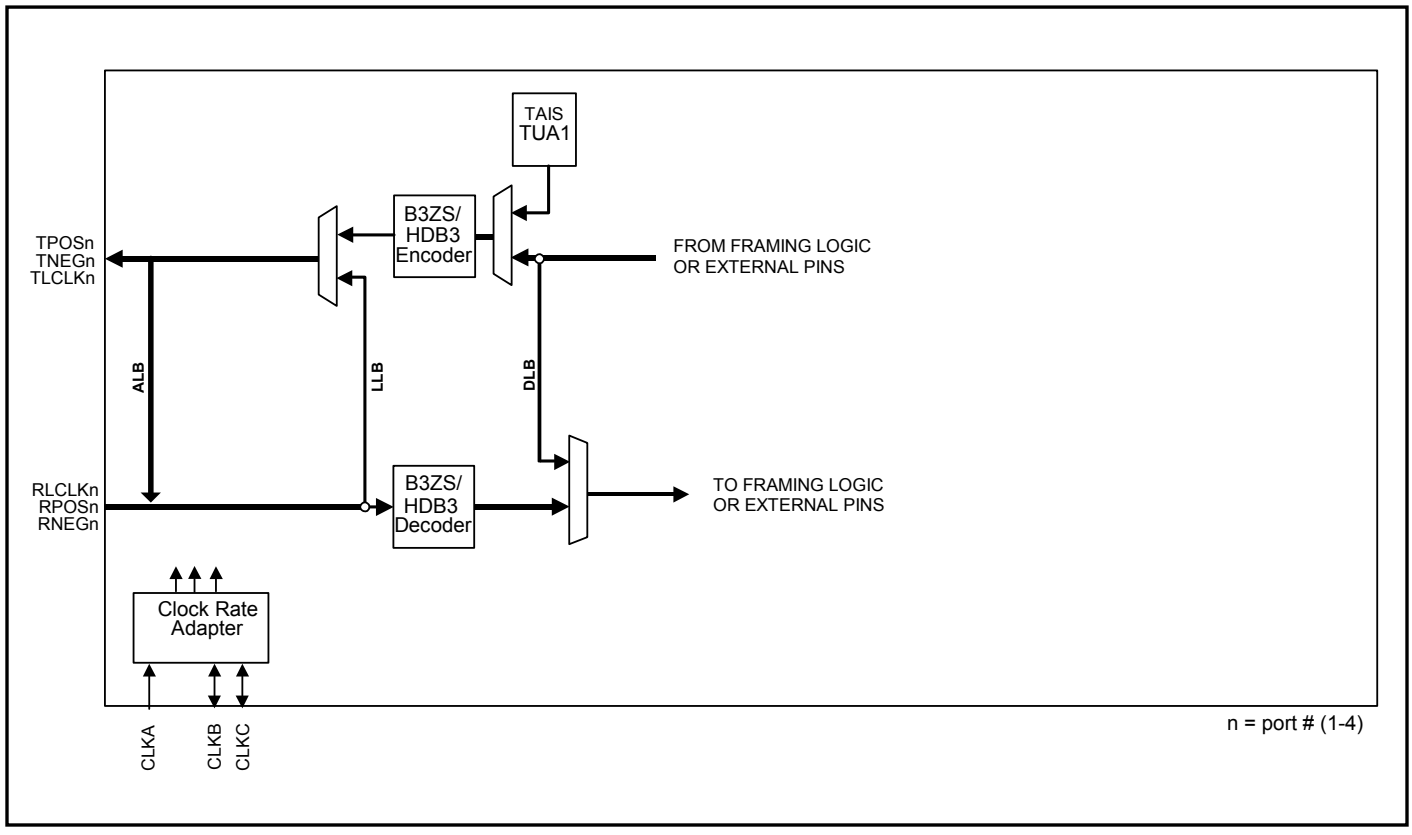
7.1 HDB3/B3ZS/AMI Line Interface Mode

The Line Interface Mode outputs/inputs a digital representation of AMI on the TPOSn/TNEGn signals and the RPOSn/RNEGn signals. Selection between AMI and HDB3/B3ZS is made via the LINE.TCR Register. HDB3 and B3ZS selection is controlled by the configuration selected by the FM bits. DS3 and CC52 frame modes select the B3ZS line code while the E3 modes select the HDB3 line code. The DS3AIS signal can only be generated in non-OHM DS3 modes.

Table 7-1. HDB3/B3ZS/AMI Mode Configuration Registers

MODE	LM	LINE.TCR.TZSD & LINE.RCR.RZSD
B3ZS or HDB3	0	0
AMI	0	1

Figure 7-1. HDB3/B3ZS/AMI Line Interface Mode



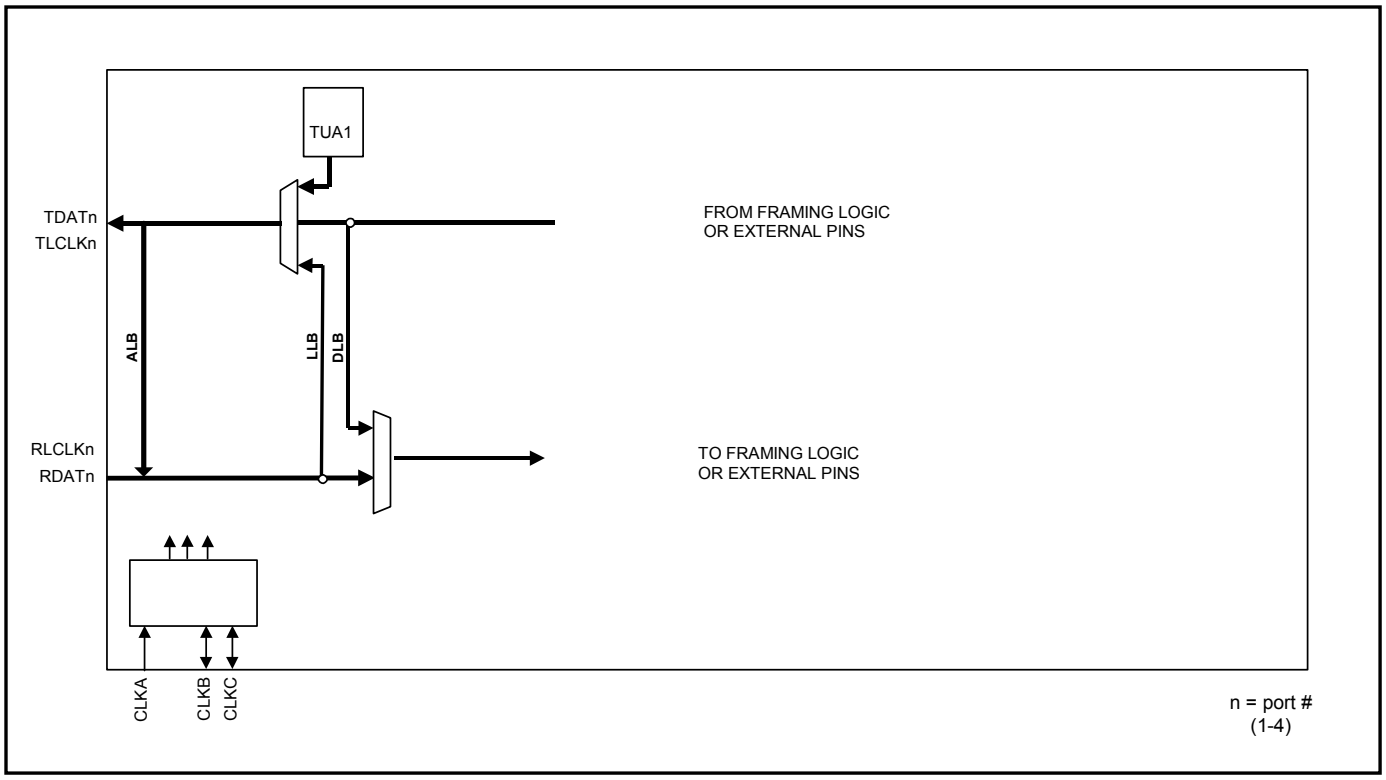
7.2 UNI Line Interface Mode

This mode is valid for all framing modes, providing a digital NRZ input/output on RDATn and TDATn and clocked by RLCLKn and TLCLKn. The B3ZS/HDB3 decoder/encoder block is disabled except for the BPV counter, which is used to count RLCV errors.

Table 7-2. UNI Line Interface Mode Configuration Registers

MODE	LM PORT.CR2	LINE.TCR.TZSD & LINE.RCR.RZSD
Unipolar Mode	1	X

Figure 7-2. UNI Line Interface Mode



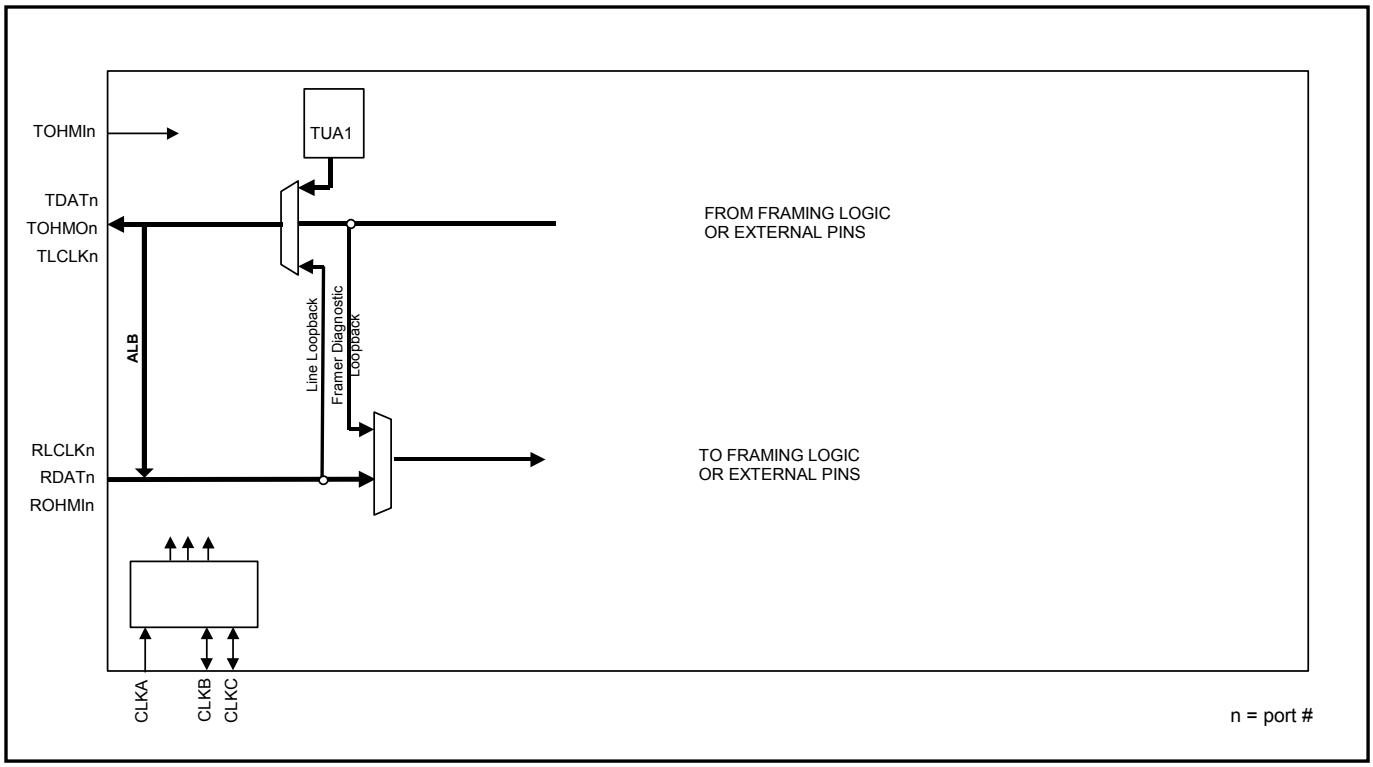
7.3 UNI Line Interface—OHM Mode

The line interface is forced into UNI mode when the framer is in any OHM mode; therefore, the LM bits are Don't Cares. This mode is the same as the UNI Line Interface Mode except that the OHM pins determine whether the data is payload or not.

Table 7-3. UNI Line Interface—OHM Mode Configuration Registers

MODE	FM[5:0] PORT.CR2	LM PORT.CR2	LINE.TCR.TZSD & LINE.RCR.RZSD
DS3/E3 Overhead Mask Mode	0XXX01	X	X
Clear-Channel Overhead Mask Mode	1XX0X1	X	X

Figure 7-3. UNI Line Interface—OHM Mode



8 PIN DESCRIPTIONS

Note: In JTAG mode, all digital pins are bidirectional to increase the effectiveness of board level ATPG patterns for isolation of interconnect failures.

8.1 Short Pin Descriptions

Table 8-1. DS3164 Short Pin Descriptions

n = 1,2,3,4 (port number); Ipu (input with pullup); Oz (output tri-stateable, needs an external pullup or pulldown resistor to keep from floating); Oa (analog output); Ia (analog input); I/O (bidirectional inout); all unused input pins without pullup should be tied low.

NAME	TYPE	FUNCTION	PIN			
			PORT 4	PORT 3	PORT 2	PORT 1
LINE IO						
TLCLKn	O	Transmit Line Clock Output	V11	C11	Y8	A8
TPOSn / TDATn	O	Transmit Positive AMI / Data	V14	C14	V4	C4
TNEGn / TOHMOn	O	Transmit Negative AMI / Line OH Mask	W14	B14	U4	D4
RLCLKn	I	Receive Clock Input	Y12	A12	W8	B8
RPOSn / RDATn	Ia	Positive AMI / Data	W15	B15	Y3	A3
RNEGn / RLCVn / ROHMIn	Ia	Negative AMI / Line Code Violation / Line OH Mask Output	Y15	A15	W3	B3
DS3/E3 OVERHEAD INTERFACE						
TOHn	I	Transmit Overhead	U11	D11	U8	D8
TOHENn	I	Transmit Overhead Enable	T14	E14	T5	E5
TOHCLKn	O	Transmit Overhead Clock	T11	E11	V8	C8
TOHSOFn	O	Transmit Overhead Start Of Frame	T12	E12	V7	C7
ROHn	O	Receive Overhead	T10	E10	U10	D10
ROHCLKn	O	Receive Overhead Clock	T13	E13	U5	D5
ROHSOFn	O	Receive Overhead Start Of Frame	U14	D14	Y2	B2
DS3/E3 SERIAL DATA, PLCP AND FRACTIONAL DS3/E3 OVERHEAD INTERFACE						
TCLKIn	I	Transmit Line Clock Input	Y14	A14	W4	B4
TSOFIn / TOHMIn	I	Transmit Start Of Frame Input / OH Mask Input	U12	D12	W7	B7
TSERn/ TPOHn / TFOHn/	I	Transmit Serial Data / PLCP Overhead / Fractional Overhead	V13	C13	T6	E6
TPDENIn / TPOHENn / TFOHENIn	I	Transmit Payload Data Enable Input / PLCP Overhead Enable / Fractional OH Enable Input	U13	D13	V5	C5
TCLKOn / TGCLKn / TPOHCLKn	O	Transmit Clock Output / Gapped Clock / PLCP Overhead Clock	Y13	A13	U7	D7
TSOFOn / TDENn / TPOHSOFn / TFOHENOn	O	Transmit Framer Start Of Frame / Data Enable / PLCP Overhead Start Of Frame / Fractional OH Enable Output	V12	C12	Y7	A7
TPDENOn	O	Transmit Payload Data Enable Output	W10	B10	Y9	A9
TPDATn	O	Transmit Payload Data	V10	C10	W9	B9
RPDENIn / RFOHENIn	I	Receive Payload Data Enable Input / Fractional Overhead Enable Input	W13	B13	U6	D6
RPDATn	I	Receive Payload Data	Y10	A10	V9	C9
RSERn / RPOHn	O	Receive Serial Data / PLCP Overhead	W11	B11	T9	E9
RCLKOn / RGCLKn RPOHCLKn	O	Receive / Clock Output / Gapped Clock / PLCP Overhead Clock	Y11	A11	U9	D9
RSOFOn / RDENn / RPOHSOFn / RFOHENOn	O	Receive Framer Start Of Frame / Data Enable / PLCP Overhead Start Of Frame / Fractional Overhead Enable Output	W12	B12	T8	E8

NAME	TYPE	FUNCTION	PIN
UTOPIA L2/3 OR POS-PHY L2/3 OR SPI-3 SYSTEM INTERFACE			
TSCLK	I	Transmit System Clock	J20
TADR[4]	I	Transmit Address [4:0]	C15
TADR[3]			D15
TADR[2]			E15
TADR[1]			A16
TADR[0]			A18
TDATA[31]	I	Transmit Data [31:0]	U15
TDATA[30]			T15
TDATA[29]			U16
TDATA[28]			U17
TDATA[27]			D18
TDATA[26]			D17
TDATA[25]			C19
TDATA[24]			F20
TDATA[23]			E16
TDATA[22]			D16
TDATA[21]			C16
TDATA[20]			C18
TDATA[19]			C17
TDATA[18]			T17
TDATA[17]			T16
TDATA[16]			R17
TDATA[15]			V16
TDATA[14]			W17
TDATA[13]			Y18
TDATA[12]			V17
TDATA[11]			W18
TDATA[10]			W19
TDATA[9]			B19
TDATA[8]			C20
TDATA[7]			W20
TDATA[6]			U18
TDATA[5]			V18
TDATA[4]			V19
TDATA[3]			U19
TDATA[2]			V20
TDATA[1]			T18
TDATA[0]			U20
$\overline{\text{TPRTY}}$	I	Transmit Parity (Active Low)	A17
$\overline{\text{TEN}}$	I	Transmit Enable (Active Low)	A19
TDXA[1] / TPXA	Oz	Transmit Direct Cell/Packet Available [1] / Polled Cell/Packet Available (Tri-State)	K17
TDXA[4]	O	Transmit Direct Cell/Packet Available [4:2]	D19
TDXA[3]			E19
TDXA[2]			D20
TSOX	I	Transmit Start Of Cell/Packet	W16
TSPA	Oz	Transmit Selected Packet Available	K16
TEOP	I	Transmit End Of Packet	V15
TSX	I	Transmit Start Of Transfer	Y16
TMOD[1]	I	Transmit Packet Data Modulus [1:0]	B18
TMOD[0]			B17
TERR	I	Transmit Packet Error	Y17
RSCLK	I	Receive System Clock	M20

NAME	TYPE	FUNCTION	PIN
RADR[4] RADR[3] RADR[2] RADR[1] RADR[0]	I	Receive Address [4:0]	T19 T20 R18 R19 R20
RDATA[31] RDATA[30] RDATA[29] RDATA[28] RDATA[27] RDATA[26] RDATA[25] RDATA[24] RDATA[23] RDATA[22] RDATA[21] RDATA[20] RDATA[19] RDATA[18] RDATA[17] RDATA[16] RDATA[15] RDATA[14] RDATA[13] RDATA[12] RDATA[11] RDATA[10] RDATA[9] RDATA[8] RDATA[7] RDATA[6] RDATA[5] RDATA[4] RDATA[3] RDATA[2] RDATA[1] RDATA[0]	Oz	Receive Data [31:0] (Tri-State)	F16 G16 H16 J16 E17 F17 G17 H17 J17 H18 J18 E18 G19 H19 G20 H20 M16 N16 P16 R16 M17 N17 P17 P18 P19 P20 N18 N19 N20 M18 M19 L20
$\overline{\text{RPRTY}}$	Oz	Receive Parity (Active Low Tri-State)	K20
$\overline{\text{REN}}$	I	Receive Enable (Active Low)	G18
RDXA[1] / RPXA / RSX	Oz	Receive Direct Cell/Packet Available [1] / Polled Cell/Packet Available / Start Of Transfer (Tri-State)	K19
RDXA[4] RDXA[3] RDXA[2]	O	Receive Direct Cell/Packet Available [4:2]	E20 F18 F19
RSOX	Oz	Receive Start Of Cell/Packet (Tri-State)	L17
REOP	Oz	Receive End Of Packet	L16
RVAL	Oz	Receive Packet Data Valid	K18
RMOD[1] RMOD[0]	Oz	Receive Packet Data Modulus [1:0]	L19 L18
RERR	Oz	Receive Packet Error	J19

NAME	TYPE	FUNCTION	PIN
MICROPROCESSOR INTERFACE			
D[15] D[14] D[13] D[12] D[11] D[10] D[9] D[8] D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O	Data [15:0]	J5 T4 R4 P4 N4 V3 U3 T3 P3 N3 W2 U2 T2 P2 U1 P1
A[10] A[9] A[8] A[7] A[6] A[5] A[4] A[3] A[2] A[1]	I	Address [10:1]	C3 D3 E3 G3 H3 D2 E2 G2 H2 E1
A[0] / BSWAP		Address [0] / Byte Swap	H1
ALE	I	Address Latch Enable	N2
$\overline{CS}$	I	Chip Select (Active Low)	L3
$\overline{RD}$ / $\overline{DS}$	I	Read Strobe (Active Low) / Data Strobe (Active Low)	K3
$\overline{WR}$ / R/$\overline{W}$	I	Write Strobe (Active Low) / R/$\overline{W}$ Select	K4
$\overline{RDY}$	Oz	Ready Handshake (Active Low)	K2
$\overline{INT}$	Oz	Interrupt (Active Low)	L4
MODE	I	Mode Select $\overline{RD}$/$\overline{WR}$ or DS Strobe Mode	B1
WIDTH	I	Width Select 8-Bit or 16-Bit Interface	L5
MISC I/O			
GPIO[8] GPIO[7] GPIO[6] GPIO[5] GPIO[4] GPIO[3] GPIO[2] GPIO[1]	I/O	General-Purpose I/O [8:1]	V2 V1 C2 C1 P5 R5 G5 F5
$\overline{TEST}$	I	Test Enable (Active Low)	M3
$\overline{HIZ}$	I	High-Impedance Test Enable (Active Low)	R3
$\overline{RST}$	I	Reset (Active Low)	B16
JTAG			
JTCLK	I	JTAG Clock	F3
JTMS	Ipu	JTAG Mode Select (with Pullup)	F4
JTDI	Ipu	JTAG Data Input (with Pullup)	J3
JTDO	Oz	JTAG Data Output	G4
$\overline{JTRST}$	Ipu	JTAG Reset (Active Low with Pullup)	E4

NAME	TYPE	FUNCTION	PIN
CLAD			
CLKA	I	Clock A	K1
CLKB	I/O	Clock B	L1
CLKC	I/O	Clock C	L2
POWER			
VSS	PWR	Ground, 0V Potential	K10, K9, K8, J10, J9, J8, H10, H9, M7, M6, L7. L6, K7. K6, J7, J6, A1, N10, N9, M10, M9, M8, L10, L9, L8, R12, R11, R10, R9, P12, P11, P10, P9, Y1, N12, N11, M13, M12, M11, L13, L12, L11, M15, M14, L15, L14, K15, K14, J15, J14, Y20, K13, K12, K11, J13, J12, J11, H12, H11, G12, G11, G10, G9, F12, F11, F10, F9, A20
VDD	PWR	Digital 3.3V	H8, H7, H6, G8, G7, G6, F8, F7, F6, A2, R8, R7, R6, P8, P7, P6, N8, N7, N6, W1, R15, R14, R13, P15, P14, P13, N15, N14, N13, Y19, H15, H14, H13, G15, G14, G13, F15, F14, F13, B20
AVDDC	PWR	Analog 3.3V for CLAD	K5
NO CONNECTS			
N.C.	N.C.	No Connection. Unused.	A4, A5, A6, B5, B6, C6, D1, E7, F1, F2, G1, H4, H5, J1, J2, J4, M1, M2, M4, M5, N1, N5, R1, R2, T1, T7, V6, W5, W6, Y4, Y5, Y6

8.2 Detailed Pin Descriptions

Table 8-2. Detailed Pin Descriptions

n = 1,2,3,4 (port number); Ipu (input with pullup); Oz (output tri-stateable, needs an external pullup or pulldown resistor to keep from floating); Oa (analog output); Ia (analog input); I/O (bidirectional inout); all unused input pins without pullup should be tied low.

PIN	TYPE	FUNCTION
LINE I/O		
TLCLKn	O	Transmit Line Clock Output **TLCLKn**: This clock is typically used as the clock reference for the TPOSn / TDATn and TNEG / TOHMOn signals, but can also be used as the reference for the TOHMIn / TSOFIn, TFOHn / TSERn, TFOHENIn and TSOFOn / TDENn / TFOHENOn signals. This output signal can be inverted. ○ DS3: 44.736 MHz ±20 ppm ○ E3: 34.368 MHz ±20 ppm ○ CC52: 52 MHz ±20 ppm
TPOSn / TDATn	O	Transmit Positive AMI / Data Output **TPOSn**: When the port line interface is configured for B3ZS, HDB3 or AMI mode and the framer is not configured for one of the "-OHM" modes (see Table 10-30), a high on this pin indicates that a positive pulse should be transmitted on the line. The signal is updated on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is updated on the falling edge of the clock. The signal is typically referenced to the TLCLKn line clock output pins, but it can be referenced to the TCLKOn, TCLKIn, RLCLKn or RCLKOn pins. This output signal can be inverted. **TDATn**: When the port line interface is configured for UNI mode or the framer is configured for one of the "-OHM" modes (see Table 10-30), the un-encoded transmit signal is output on this pin. The signal is updated on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is updated on the falling edge of the clock. The signal is typically referenced to the TLCLK line clock output pins, but it can be referenced to the TCLKOn, TCLKIn, RLCLKn or RCLKOn pins This output signal can be inverted. ○ DS3: 44.736 Mbps ±20ppm ○ E3: 34.368 Mbps ±20ppm ○ CC52: 52 Mbps ±20ppm

PIN	TYPE	FUNCTION
TNEGn / TOHMOn	O	Transmit Negative AMI / Line OH Mask **TNEGn**: When the port line is configured for B3ZS, HDB3 or AMI mode and the framer is not configured for one of the "-OHM" modes (see Table 10-30), a high on this pin indicates that a negative pulse should be transmitted on the line. The signal is updated on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is updated on the falling edge of the clock. The signal is typically referenced to the TLCLKn line clock output pins, but it can be referenced to the TCLKOn, TCLKIn, RLCLKn or RCLKOn pins. This output signal can be inverted. ○ DS3: 44.736 Mbps ±20ppm ○ E3: 34.368 Mbps ±20ppm ○ CC52: 52 Mbps ±20ppm **TOHMOn**: When the framer is configured for one of the "-OHM" modes (see Table 10-30), the transmit overhead mask signal is output on this pin. This signal is a delayed version of TOHMIn or ROHMIn when in local loopback (three clock period delay). This signal will be high to indicate that the data on TDATn is not valid data and can be overwritten by external logic to add an external frame signal. This signal will be low to indicate that the data on TDATn is valid. The signal is updated on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is updated on the falling edge of the clock. The signal is typically referenced to the TLCLKn line clock output pins, but it can be referenced to the TCLKOn, TCLKIn, RLCLKn or RCLKOn pins. This output signal can be inverted.
RLCLKn	I	Receive Line Clock Input **RLCLKn**: This clock is typically used for the reference clock for the RPOSn / RDATn, RNEGn / RLCVn / ROHMIn signals but can also be used as the reference clock for the RSERn, RSOFOn / RDENn / RFOHENOn, RFOHENIn, TOHMIn / TSOFIn, TFOHn / TSERn, TFOHENIn, TSOFOn / TDENn / TFOHENOn, TPOSn / TDATn and TNEGn / TOHMOn signals. This input signal can be inverted. ○ DS3: 44.736 MHz ±20 ppm ○ E3: 34.368 MHz ±20 ppm ○ CC52: 52 MHz ±20 ppm
RPOSn / RDATn	Iad	Receive Positive AMI / Data **RPOSn**: When the port line is configured for B3ZS, HDB3 or AMI mode and the framer is not configured for one of the "-OHM" modes, a high on this pin indicates that a positive pulse has been detected using an external LIU. The signal is sampled on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is sampled on the falling edge of the clock. The signal is typically referenced to the RLCLKn line clock input pins, but it can be referenced to the RCLKOn output pins. This input signal can be inverted. **RDATn**: When the port line interface is configured for UNI mode or the framer is configured for one of the "-OHM" modes, the un-encoded receive signal is input on this pin. The signal is sampled on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is sampled on the falling edge of the clock. The signal is typically referenced to the RLCLKn line clock input pins, but it can be referenced to the RCLKOn output pins. This input signal can be inverted. ○ DS3: 44.736 Mbps ±20ppm ○ E3: 34.368 Mbps ±20ppm ○ CC52: 52 Mbps ±20ppm
RNEGn / RLCVn / ROHMIn	Iad	Receive Negative AMI / Line Code Violation / Line OH Mask input **RNEGn**: When the port line is configured for B3ZS, HDB3 or AMI mode and the framer is not configured for one of the "-OHM" modes, a high on this pin indicates that a negative pulse has been detected using an external LIU. The signal is sampled on

PIN	TYPE	FUNCTION
		the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is sampled on the falling edge of the clock. The signal is typically referenced to the RLCLKn line clock input pins, but it can be referenced to the RCLKOn output pins. This input signal can be inverted. o DS3: 44.736 Mbps ±20ppm o E3: 34.368 Mbps ±20ppm o CC52: 52 Mbps ±20ppm **RLCVn**: When the port line interface is configured for UNI mode and the framer is not configured for one of the "-OHM" modes, the BPV counter in the encoder/decoder block is incremented each clock when this signal is high. The signal is sampled on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is sampled on the falling edge of the clock. The signal is typically referenced to the RLCLKn line clock input pins, but it can be referenced to the RCLKOn output pins. This input signal can be inverted. **ROHMIn**: When the port framer is configured for one of the "-OHM" modes, this signal is used to mark the overhead bits on the RDATn pins when it is high. The DS316x will ignore overhead bits. The signal is sampled on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is sampled on the falling edge of the clock. The signal is typically referenced to the RLCLKn line clock input pins, but it can be referenced to the RCLKOn output pins. This input signal can be inverted.
DS3/E3 OVERHEAD INTERFACE		
TOHn	I	Transmit Overhead / Line OH Mask Input **TOHn**: When the port framer is configured for one of the DS3 or E3 framing modes, this signal will be used to over-write the DS3 or E3 framing overhead bits when TOHENn is active. In T3 mode, the X-bits, P-bits, M-bits, F-bits, and C-bits are input. In G.751 E3 mode, all of the FAS, RAI, and National Use bits are input. In G.832 E3 mode, all of the FA1, FA2, EM, TR, MA, NR, and GC bytes are input. The TOHSOFn signal marks the start of the framing bit sequence. This signal is sampled at the same time as the TOHCLKn signal transitions high to low. This signal can be inverted.
TOHENn	I	Transmit Overhead Enable / Start Of Frame Input **TOHENn**: When the port framer is configured for one of the DS3 or E3 framing modes, this signal will be used the determine which DS3 or E3 framing overhead bits to over-write with the signal on the TOHn pins. The TOHSOFn signal marks the start of the framing bit sequence. This signal is sampled at the same time as the TOHCLKn signal transitions high to low. This signal can be inverted.
TOHCLKn	O	Transmit Overhead Clock **TOHCLKn**: When the port framer is configured for one of the DS3 or E3 framing modes, this clock is used for the transmit overhead port signals TOHn, TOHENn and TOHSOFn. The TOHSOFn output signal is updated and the TOHn and TOHENn input signals are sampled at the same time this clock signal transitions from high to low. The external logic is expected to sample TOHSOFn signal and update the TOHn and TOHENn signals on the rising edge of this clock signal. This clock is a low frequency clock. This signal can be inverted.
TOHSOFn	O	Transmit Overhead Start Of Frame **TOHSOFn**: When the port framer is configured for one of the DS3 or E3 framing modes, this signal is used to mark the start of a DS3 or E3 overhead sequence on the TOHn pins. In T3 mode, the first X-bit is marked. In G.751 E3 mode, the first bit of the FAS word is marked. In G.832 E3 mode, the first bit of the FA1 byte is marked. The sequence starts on the same high to low transition of the TOHCLKn clock that this signal is high. This signal is updated at the same time as the TOHCLKn signal

PIN	TYPE	FUNCTION
		transitions high to low. This signal can be inverted.
ROHn	O	Receive Overhead **ROHn**: When the port framer is configured for one of the DS3 or E3 framing modes, this signal outputs the value of the receive overhead bits. The ROHSOFn signal marks the start of the framing bit sequence. In T3 mode, the X-bits, P-bits, M-bits, F-bits, and C-bits are output (Note: In M23 mode, the C-bits are extracted even though they are marked as data at the payload interface). In G.751 E3 mode, all of the FAS, RAI, and National Use bits are output. In G.832 E3 mode, all of the FA1, FA2, EM, TR, MA, NR, and GC bytes are output. This signal is updated at the same time as the ROHCLKn signal transitions high to low. This signal can be inverted.
ROHCLKn	O	Receive Overhead Clock **ROHCLKn**: When the port framer is configured for one of the DS3 or E3 framing modes, this clock is used for the receive overhead port signals ROHn and ROHSOFn. The ROHSOFn and ROHn output signals are updated at the same time this clock signal transitions from high to low. The external logic is expected to sample ROHSOFn and ROHn signal on the rising edge of this clock signal. This clock is a low frequency clock. This signal can be inverted.
ROHSOFn	O	Receive Overhead Start Of Frame **ROHSOFn**: When the port framer is configured for one of the DS3 or E3 framing modes this signal is used to mark the start of a DS3 or E3 overhead sequence on the ROHn pins. In T3 mode, the first X-bit is marked. In G.751 E3 mode, the first bit of the FAS word is marked. In G.832 E3 mode, the first bit of the FA1 byte is marked. The sequence starts on the same high to low transition of the ROHCLKn clock that this signal is high. This signal is updated at the same time as the ROHCLKn signal transitions high to low. This signal can be inverted.
DS3/E3 SERIAL DATA, PLCP AND FRACTIONAL DS3/E3 OVERHEAD INTERFACE		
TCLKIn	I	Transmit Line Clock Input **TCLKIn**: This clock is typically used for the reference clock for the TOHMIn / TSOFIn, TFOHn / TSERn, TFOHENIn / TPDENIn, TPDATn, TPDENOn and TSOFOn / TDENn / TFOHENOn signals but can also be used as the reference for the TPOSn / TDATn and TNEGn / TOHMOn signals. This clock is not used when the part is in loop time mode or the CLAD clocks are used as the transmit clock source. (*PORT.CR3*.CLADC) This input signal can be inverted. o DS3: 44.736 MHz ±20 ppm o E3: 34.368 MHz ±20 ppm o CC52: 52 MHz ±20 ppm

PIN	TYPE	FUNCTION
TSOFIn / TOHMIn	I	Transmit Start Of Frame Input / OH Mask Input See Table 10-18. **TSOFIn**: When the port framer is configured for any of the DS3 or E3 non "-OHM" framed modes, this signal can be used to align the start of the DS3 or E3 frames on the TSER pin to an external signal. In the fractional mode, the TSOFIn signal can be used to align the start of frame signal position on the TSERn/TOHn pin to the rising edge of a signal on this pin. The signal edge does not need to occur on every frame and can be tied high or low. The signal is sampled on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is sampled on the falling edge of the clock. The signal is typically referenced to the TCLKIn transmit clock input pins, but it can be referenced to the TLCLKn, TCLKOn, RCLKOn and RLCLKn clock pins. This signal can be inverted. **TOHMIn**: When the port framer is configured for one of the "- OHM" modes, this signal is used to mark clock periods when valid data bits are available on the TDATn output pins. When this signal is low, valid data bits bits will be available on the TDATn output pins three clock periods later. This signal precedes the signal on TDATn and TOHMOn by three clock periods. The signal is sampled on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is sampled on the falling edge of the clock. The signal is typically referenced to the TCLKIn transmit clock input pins, but it can be referenced to the TLCLKn, TCLKOn, RCLKOn and RLCLKn clock pins. This signal can be inverted.
TSERn / TPOHn / TFOHn /	I	Transmit Serial Data / PLCP Overhead / Fractional Overhead See Table 10-19. **TSERn**: When the port framer is configured for Flexible Fractional mode, this pin is used as the source of the DS3/E3 payload data. The signal is sampled on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is sampled on the falling edge of the clock. The signal is typically referenced to the TCLKIn transmit clock input pins, but it can be referenced to the TLCLKn, TCLKOn / TGCLKn, RCLKOn and RLCLKn clock pins This signal can be inverted. ○ DS3: 44.736 Mbps ±20ppm ○ E3: 34.368 Mbps ±20ppm ○ CC52: 52 Mbps ±20ppm **TPOHn**: When the port framer is configured for one of the DS3 or E3 PLCP framing modes, and the port is enabled, this signal will be used to over-write the DS3 or E3 PLCP framing overhead bits when TPOHENn is active. The TPOHSOFn signal marks the start of the framing bit sequence. This signal is sampled at the same time as the TPOHCLKn signal transitions high to low. This signal can be inverted. **TFOHn**: When the port framer is configured for one of the DS3 or E3 internal or external fractional framing modes, and the port is enabled the internal fractional framing modes, this pin can be used to source the fractional overhead data. The signal is sampled on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is sampled on the falling edge of the clock. The signal is typically referenced to the TCLKIn transmit clock input pins, but it can be referenced to the TLCLKn, TCLKOn / TGCLKn, RCLKOn and RLCLKn clock pins This signal can be inverted.

PIN	TYPE	FUNCTION
TPDENIn / TPOHENn / TFOHENIn	I	Transmit Payload Data Enable Input / PLCP Overhead Enable / Fractional OH Enable Input / See Table 10-20. **TPDENIn**: When the port is configured for the Flexible fractional mode, this pin is used to enable payload data from the cell/packet processor. There is a three-clock delay between TPDENIn and TPDENOn. The signal is sampled on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is sampled on the falling edge of the clock. The signal is typically referenced to the TCLKIn transmit clock input pins, but it can be referenced to the TLCLKn, TCLKOn, RCLKOn and RLCLKn clock pins This signal can be inverted. **TPOHENn**: When the port framer is configured for one of the DS3 or E3 PLCP framing modes, and the port is enabled, this signal will be used the determine which DS3 or E3 PLCP framing overhead bits to over-write with the signal on the TPOHn pins. The TPOHSOFn signal marks the start of the framing bit sequence. This signal is sampled at the same time as the TPOHCLKn signal transitions high to low. This signal can be inverted. **TFOHENIn**: When the port framer is configured for the DS3 or E3 External Fractional framing, this pin is used to mark the fractional overhead data on the TFOHn pin. The TSOFOn or TSOFIn pins can be used to select which DS3/E3 payload bits relative to the start of the DS3/E3 frame to mark. The signal is sampled on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is sampled on the falling edge of the clock. The signal is typically referenced to the TCLKIn transmit clock input pins, but it can be referenced to the TLCLKn, TCLKOn, RCLKOn and RLCLKn clock pins This signal can be inverted.
TCLKOn / TGCLKn / TPOHCLKn	O	Transmit Clock Output / Gapped Clock / PLCP Overhead Clock See Table 10-22. **TCLKOn**: When the port is configured external fractional modes and TCLKOn is selected, or any other mode and the port pins are enabled and TCLKOn is selected, this clock output is enabled. This clock is the same clock as the internal framer transmit clock. This clock is typically used for the reference clock for the TOHMIn / TSOFIn, TFOHn / TSERn, TFOHENIn and TSOFOn / TDENn / TFOHENOn signals but can also be used as the reference for the TPOSn / TDATn and TNEGn / TOHMOn signals. This signal can be inverted. ○ DS3: 44.736 MHz ±20 ppm ○ E3: 34.368 MHz ±20 ppm ○ CC52: 52 MHz ±20 ppm **TGCLKn**: When the port is configured internal fractional mode or any simple DS3/E3 framed mode and the port pins are enabled and TGCLKn is selected, this gated output clock is enabled. This gapped clock is the same clock as the internal framer transmit clock and is gated by either TDENn or TFOHENOn depending on which signal is active. This clock is typically used for the reference clock for the TFOHn / TSERn signals. This signal can be inverted. **TPOHCLKn**: When the port framer is configured for one of the DS3 or E3 PLCP framing modes, the port pins are enabled and the TCLKOn pin function is not selected, this clock is used for the transmit overhead port signals TPOHn, TPOHENn and TPOHSOFn. The TPOHSOFn output signal is updated and the TPOHn and TPOHENn input signals are sampled at the same time this clock signal transitions from high to low. The external logic is expected to sample TPOHSOFn signal and update the TPOHn and TPOHENn signals on the rising edge of this clock signal. This clock is a low frequency clock. This signal can be inverted.
TSOFOn /	O	Transmit PLCP Overhead Start Of Frame / Framer Start Of Frame /Data Enable

PIN	TYPE	FUNCTION
TDENn / TPOHSOFn / TFOHENOn		See Table 10-21. **TSOFOn**: When the port framer is configured for the External Fractional or Flexible Fractional modes and the port pins are enabled and the TSOFOn pin function is selected, this signal is used to indicate the start of the DS3/E3 frame on the TPOHn / TFOHn / TSERn pin. The signal is also active in the non-PLCP non-fractional DS3 or E3 framing modes when the port pins are enabled and the TSOFOn pin function is selected. This signal pulses high three clocks before the first overhead bit in a DS3 or E3 frame that will be input on TSERn or TFOHn. The signal is updated on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is updated on the falling edge of the clock. The signal is typically referenced to the TCLKIn transmit clock input pins, but it can be referenced to the TLCLKn, TCLKOn, RCLKOn and RLCLKn clock pins. This signal can be inverted. **TDENn**: When the port framer is configured for the External Fractional or Flexible Fractional modes and the port pins are enabled and the TDENn pin function is selected, this signal is used to mark the DS3/E3 frame bits on the TPOHn / TFOHn / TSERn pin. The signal is also active in the non-PLCP non-fractional DS3 or E3 framing modes when the port pins are enabled and the TDENn pin function is selected. The signal goes high three clocks before the start of DS3/E3 payload bits and goes low three clocks before the end of the DS3/E3 payload bits. The signal is updated on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is updated on the falling edge of the clock. The signal is typically referenced to the TCLKIn transmit clock input pins, but it can be referenced to the TLCLKn, TCLKOn, RCLKOn and RLCLKn clock pins. This signal can be inverted. **TPOHSOFn**: When the port framer is configured for one of the PLCP framing modes and the port pins are enabled, this signal is used to mark the start of a DS3 or E3 PLCP overhead sequence on the TPOHn pins. The sequence starts on the same high to low transition of the TPOHCLKn clock that this signal is high. This signal is updated at the same time as the TPOHCLKn signal transitions high to low. This signal can be inverted. **TFOHENOn**: When the port framer is configured for one of the internal fractional modes and the port pins are enabled, this signal is used to indicate the fractional overhead bit positions of the data on the TOHn pin. The signal goes high one clock before the start of DS3/E3 fractional overhead bits and goes low one clock before the end of the DS3/E3 fractional payload bits. The signal is updated on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is updated on the falling edge of the clock. The signal is typically referenced to the TCLKIn transmit clock input pin, but it can be referenced to the TLCLKn, TCLKOn, RCLKOn or RLCLKn clock pin. This signal can be inverted.
TPDENOn	O	Transmit Payload Data Enable Output See Table 10-24. **TPDENOn**: When the port framer is enabled for the Flexible fractional mode and the port pins are enabled, this signal marks which bits on the TPDATn pin are valid payload data bits. It is high during the same clock cycle the TPDATn payload data bit is valid. The signal is updated on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is updated on the falling edge of the clock. The signal is typically referenced to the TCLKIn transmit clock input pin, but it can be referenced to the TLCLKn, TCLKOn, RCLKOn or RLCLKn clock pin. This signal can be inverted.

PIN	TYPE	FUNCTION
TPDATn	O	Transmit Payload Data See Table 10-24. **TPDATn**: When the port framer is enabled for the Flexible fractional mode and the port pins are enabled, this signal is the payload bits from the cell/packet processor. The data is valid if the TPDENOn signal is high during the same clock cycle. The signal is updated on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is updated on the falling edge of the clock. The signal is typically referenced to the TCLKIn transmit clock input pin, but it can be referenced to the TLCLKn, TCLKOn, RCLKOn or RLCLKn clock pin. This signal can be inverted.
RPDENIn / RFOHENIn	I	Receive Payload Data Enable Input / Fractional Overhead Enable Input See Table 10-26. **RPDENIn**: When the port is configured for the flexible fractional mode, this pin is used to enable payload data for the cell/packet processor. The data on RPDATn is used when this signal is high. The signal is sampled on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is sampled on the falling edge of the clock. The signal is typically referenced to the RCLKOn receive clock output pins, but it can be referenced to the RLCLKn clock input pin. This signal can be inverted. **RFOHENIn**: When the port framer is configured for the external fractional framing mode, this pin is used to mark the receive bits to use for fractional overhead data. The signal on the RSOFOn pin can be used to select which DS3/E3 payload bits relative to the start of the DS3/E3 frame to mark. The signal needs to go high for each bit on the RSERn pin that should be treated as fractional overhead in the DS3/E3 payload. RFOHENIn needs to go high or low three clock periods after the data bit on RSERn is present to mark that bit as payload or fractional overhead. The signal is sampled on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is sampled on the falling edge of the clock. The signal is typically referenced to the RCLKOn receive clock output pins, but it can be referenced to the RLCLKn clock input pin. This signal can be inverted.
RPDATn	I	Receive Payload Data See Table 10-27 **RPDATn**: When the port framer is enabled for the Flexible fractional mode and the port pins are enabled, this signal is the payload bits for the cell/packet processor. The data is used if the RPDENOn signal is high during the same clock cycle. The signal is sampled on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is sampled on the falling edge of the clock. The signal is typically referenced to the RCLKOn receive clock output pins, but it can be referenced to the RLCLKn clock input pin. This signal can be inverted.
RSERn / RPOHn	O	Receive Serial Data / PLCP Overhead See Table 10-25. **RSERn**: When the port framer is configured for the external fractional mode, internal fractional mode, or flexible fractional mode, and the port pins are enabled, this pin outputs the receive data signal from receive line pins. The signal is updated on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is updated on the falling edge of the clock. The signal is typically referenced to the RCLKOn receive clock output pin, but it can be referenced to the RGCLKn and RLCLKn clock pins. This signal can be inverted ○ DS3: 44.736 Mbps ±20ppm ○ E3: 34.368 Mbps ±20ppm ○ CC52: 52 Mbps ±20ppm **RPOHn**: When the port framer is configured for one of the PLCP framing modes and the port pins are enabled, this signal outputs the value of the receive PLCP overhead

PIN	TYPE	FUNCTION
		bits. The RPOHSOFn signal marks the start of the framing bit sequence. This signal is updated at the same time as the RPOHCLKn signal transitions high to low. This signal can be inverted..
RCLKOn / RGCLKn / RPOHCLKn	O	Receive Clock Output / Gapped Clock / PLCP Overhead Clock See Table 10-29. **RCLKOn**: When the port is configured for external fractional mode or flexible fractional mode and RCLKOn is selected, or any other mode and the port pins are enabled and RCLKOn is selected, this clock output signal is active. It is the same as the internal receive framer clock. This clock is typically used for the reference clock for the RSERn, RSOFOn / RDENn / RFOHENOn, RPDATn, and RFOHENIn / RPDENIn signals but can also be used as the reference for the RPOSn / RDATn, RNEGn / RLCVn / ROHMIn TOHMIn / TSOFIn, TFOHn / TSERn, TFOHENIn, TSOFOn / TDENn / TFOHENOn, TPOSn / TDATn and TNEGn / TOHMOn signals. This signal can be inverted. ○ DS3: 44.736 MHz ±20 ppm ○ E3: 34.368 MHz ±20 ppm ○ CC52: 52 MHz ±20 ppm **RGCLKn**: When the port is configured for internal fractional or any simple DS3/E3 framed mode and the port pins are enabled and RGCLKn is selected, this gated clock output signal is active. It is the internal receive framer clock gated by either RDENn or RFOHENOn, depending on which signal is active. This clock is typically used as the reference clock for the RSERn pin. This signal can be inverted **RPOHCLKn**: When the port framer is configured for one of the PLCP framing modes and the port pins are enabled, this clock is used for the receive PLCP overhead port signals RPOHn and RPOHSOFn. The RPOHSOFn and RPOHn output signals are updated at the same time this clock signal transitions from high to low. The external logic is expected to sample RPOHSOFn and RPOHn signal on the rising edge of this clock signal. This clock is a low frequency clock. This signal can be inverted.

PIN	TYPE	FUNCTION
RSOFOn / RDENn / RPOHSOFn / RFOHENOn	O	Receive Framer Start Of Frame /Data Enable / PLCP Overhead Start Of Frame See Table 10-28. **RSOFOn**: When the port framer is configured for External Fractional or Flexible Fractional mode and the RSOFOn pin function is enabled, or when it is configured for one of the DS3 or E3 framed only modes and the port pins are enabled and the RSOFOn pin function is enabled, this signal is used to indicate the start of the DS3/E3 frame. This signal indicates the first DS3/E3 overhead bit on the RSERn pin when high. The signal is updated on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is updated on the falling edge of the clock. The signal is typically referenced to the RCLKOn receive clock output pin, but it can be referenced to the RLCLKn clock input pin. This signal can be inverted. **RDENn**: When the port framer is configured for External Fractional or Flexible Fractional mode and the RDENn pin function is enabled and the port pins are enabled and the RDENn pin function is enabled, this signal is used to indicate the DS3/E3 payload bit positions of the data on the RSERn pin. The signal goes high during each DS3/E3 payload bit and goes low during each DS3/E3 overhead bit. The signal is updated on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is updated on the falling edge of the clock. The signal is typically referenced to the RCLKOn receive clock output pin, but it can be referenced to the RLCLKn clock input pin. This signal can be inverted. **RPOHSOFn**: When the port framer is configured for one of the PLCP framing modes and the port pins are enabled, this signal is used to mark the start of a DS3 or E3 PLCP overhead sequence on the RPOHn pins. The sequence starts on the same high to low transition of the RPOHCLKn clock that this signal is high. This signal is updated at the same time as the RPOHCLKn signal transitions high to low. This signal can be inverted. **RFOHENOn**: When the port framer is configured for internal fractional mode and the port pins are enabled, this signal is used to indicate the fractional overhead bit positions of the data on the RSERn pin. The signal goes high during each DS3/E3 fractional overhead bit and goes low during each DS3/E3 fractional payload bit. The signal is updated on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is updated on the falling edge of the clock. The signal is typically referenced to the RCLKOn receive clock output pin, but it can be referenced to the RLCLKn clock input pin. This signal can be inverted.
UTOPIA/POS-PHY/SPI-3 SYSTEM INTERFACE		
TSCLK	I	Transmit System Clock **TSCLK**: This signal is used to sample or update the other transmit system interface signals. TSCLK has a maximum frequency of 66 MHz in L3 modes and 52 MHz in L2 modes.
TADR[4:0]	I	Transmit Address [4:0] **TADR[4:0]**: In UTOPIA L2, UTOPIA L3 or POS-PHY L2 modes, this 5-bit address bus is used by the ATM/Link layer device to select a specific port for data transfer or to poll for FIFO status.. In POS-PHY L3 modes, this 5-bit address is used by the Link layer device to poll for FIFO status. TADR[4] is the MSB and TADR[0] is the LSB. This bus is sampled on the rising edge of TSCLK.
TDATA[31:0]	I	Transmit Data [31:0] **TDATA[31:0]**: This 32-bit data bus is used to transfer cell/packet data from the ATM/Link layer device. This bus is sampled on the rising edge of TSCLK. In 32-bit mode, TDATA[31] is the MSB and TDATA[0] is the LSB. In 16-bit mode, TDATA[15] is the MSB, TDATA[0] is the LSB, and TDATA[31:16] are not used and ignored.

PIN	TYPE	FUNCTION
		In 8-bit mode, TDATA[7] is the MSB, TDATA[0] is the LSB, and TDATA[31:8] are not used and ignored.
TPRTY	I	Transmit Parity **TPRTY**: This signal indicates the parity on the data bus when parity checking is enabled. This option is programmable. TPRTY is ignored if parity checking is disabled. This signal is sampled on the rising edge of TSCLK.
$\overline{\text{TEN}}$	I	Transmit Enable (active low) $\overline{\text{TEN}}$: This signal is used by the ATM/Link device to control the transfer of cell/packet data on the TDATA bus. If $\overline{\text{TEN}}$ is high, no transfer occurs. If $\overline{\text{TEN}}$ is low, a transfer occurs. This signal can be sampled on the rising edge of TSCLK.
TDXA[1] / TPXA	Oz	Transmit Direct cell/packet Available [1] / Polled cell/packet Available (tri-state) This signal is tri-state when global reset is applied. **TDXA[1]**: When direct status mode is selected, this signal is used to indicate when port 1 can accept data from the ATM/Link layer device. This signal is updated on the rising edge of TSCLK. In UTOPIA L2 or Utopia L3 modes, TDXA goes high when port 1 can accept the transfer of more than a programmable number of ATM cells. TDXA goes low when port 1 cannot accept the transfer of a complete ATM cell. In POS-PHY L2 or POS-PHY L3 modes, TDXA goes high when port 1 can store more data than the "almost full" level. TDXA goes low when port 1 is full. **TPXA**: (reset default) When polled status mode is selected, this signal is used to indicate when the polled port, as selected by TADR[4:0], can accept data from the ATM/Link layer device. This signal is updated on the rising edge of TSCLK. In UTOPIA L2 or UTOPIA L3 modes, TPXA goes high when the polled port can accept the transfer of more than a programmable number of ATM cells. TPXA goes low when the polled port cannot accept the transfer of a complete ATM cell. In POS-PHY L2 or POS-PHY L3 modes, TPXA goes high when the polled port can store more data than the "almost full" level. TPXA goes low when the polled port is full. In UTOPIA L2 (reset default) or POS-PHY L2 modes, this signal is driven when one of the ports is being polled, and is tri-stated when none of the ports is being polled or when data path reset is active. In UTOPIA L3 or POS-PHY L3 modes, this signal is driven. Note: Polled status mode and direct status mode is selected by the GL.CR1.DIREN bit.
TDXA[4:2]	O	Transmit Direct cell/packet Available [4:2] **TDXA[4:2]**: This signal is used to indicate when the associated port can accept data from the ATM/Link layer device. This signal can be updated on the rising edge of TSCLK. In UTOPIA L2 or L3 modes, TDXA goes high when the associated port can accept the transfer of more than a programmable number of ATM cells. TDXA goes low when the associated port cannot accept the transfer of a complete ATM cell. In POS-PHY L2 or L3 modes, TDXA goes high when the associated port can store more data than the "almost full" level. TDXA goes low when the associated port is full.
TSOX	I	Transmit Start Of Cell/Packet **TSOX**: This signal is used to indicate the first transfer of a cell/packet. This signal can be sampled on the rising edge of TSCLK. In UTOPIA L2 or L3 modes, TSOX indicates the first transfer of a cell. In POS-PHY L2 or L3 modes, TSOX indicates the first transfer of a packet.
TSPA	Oz	Transmit Selected Packet Available This signal is tri-state when global reset is applied. **TSPA**: In POS-PHY L2 or POS-PHY L3 modes, this signal is used to indicate the selected port can accept data from the Link layer device. TSPA goes high when a port is selected for transfer and it can accept more data than the "almost full" level. TSPA goes low when the selected port is "full" or no port is selected. This signal is

PIN	TYPE	FUNCTION
		updated on the rising edge of TSCLK. In UTOPIA L3 mode this signal is low. In POS-PHY L2 mode, this signal is driven when one of the ports is selected for data transfer, and tri-state when $\overline{TEN}$ is deasserted, none of the ports is selected or when data path reset is active. POS-PHY L3 or UTOPIA L3 modes this signal is driven. In UTOPIA L2 (reset default) mode this signal is tri-stated.
TEOP	I	Transmit End Of Packet **TEOP**: In POS-PHY L2 or L3 modes, this signal is used to indicate the last transfer of a packet. This signal is sampled on the rising edge of TSCLK. In UTOPIA L2 or L3 modes, this signal is ignored.
TSX	I	Transmit Start of Transfer **TSX**: In POS-PHY L3 mode, this signal indicates the start of a data transfer. TSX goes high goes high immediately before the start of data transfer to indicate that the in-band port address is present on TDATA. TSX goes high when the value of TDATA is the address of the transmit port to which data is to be transferred. When TSX goes low, all subsequent transfers will be to the port specified by the in-band address. This signal is sampled on the rising edge of TSCLK. TSX is only valid when $\overline{TEN}$ is high. In UTOPIA L2, UTOPIA L3 or POS-PHY L2 modes, this signal is ignored.
TMOD[1:0]	I	Transmit packet data Modulus [1:0] **TMOD[1:0]**: In POS-PHY L2 or L3 modes, this signal indicates the number of valid bytes on the TDATA bus. TMOD[1:0]=00 TDAT[31:0] valid TMOD[1:0]=01 TDAT[31:8] valid TMOD[1:0]=10 TDAT[31:16] valid TMOD[1:0]=11 TDAT[31:24] valid This signal is sampled on the rising edge of TSCLK. TMOD is only valid when TEOP is high. In 16-bit POS-PHY L2 or 16 bit POS-PHY L3 mode, TMOD[1] is ignored. In 8-bit POS-PHY L2 or 8-bit POS-PHY L3 modes, TMOD[1:0] are ignored. In UTOPIA L2 or UTOPIA L3 modes, TMOD[1:0] are ignored.
TERR	I	Transmit packet Error **TERR**: In POS-PHY L2 or POS-PHY L3 modes, this signal indicates that the current packet is erred. When TERR is high, the current packet should be aborted. This signal is sampled on the rising edge of TSCLK. TERR is only valid when TEOP is high. In UTOPIA L2 or UTOPIA L3 modes, this signal is ignored.
RSCLK	I	Receive System Clock **RSCLK**: This signal is used to sample or update the other receive system interface signals. RSCLK has a maximum frequency of 66 MHz in UTOPIA L3 or POS-PHY L3 modes and 52 MHZ in UTOPIA L2 or POS-PHY L2 modes.
RADR[4:0]	I	Receive Address [4:0] **RADR[4:0]**: In UTOPIA L2, UTOPIA L3 or POS-PHY L2 modes, this 5-bit address bus is used by the ATM/Link layer device to select a specific port for data transfer and polling FIFO status. RADR[4] is the MSB and RADR[0] is the LSB. This bus is sampled on the rising edge of RSCLK. In POS-PHY Level 3 (or SPI-3) mode, this bus is ignored.

PIN	TYPE	FUNCTION
RDATA[31:0]	Oz	Receive Data [31:0] (tri-state) This signal is tri-state when global reset is applied. **RDATA[31:0]**: This 32-bit data bus is used to transfer cell/packet data to the ATM/Link layer device. This bus is updated on the rising edge of RSCLK. In 32-bit mode- RDATA[31] is the MSB and RDATA[0] is the LSB. In UTOPIA L2 or POS-PHY L2 modes, RDATA[31:0] are driven when one of the ports is selected for data transfer, and tri-stated when $\overline{REN}$ is deasserted, none of the ports is selected or data path reset is active. In UTOPIA L3 or POS-PHY L3 modes RDATA[31:0] are driven. In 16-bit mode- RDATA[15] is the MSB, RDATA[0] is the LSB, and RDATA[31:16] are not used. In UTOPIA L2 or POS-PHY L2 modes, RDATA[15:0] are driven when one of the ports is selected for data transfer, and tri-stated when $\overline{REN}$ is deasserted, none of the ports is selected or data path reset is active. RDATA[31:16] are tri-stated. In UTOPIA L3 or POS-PHY L3 modes, RDATA[31:0] are driven. In 8-bit mode (reset default)- RDATA[7] is the MSB, RDATA[0] is the LSB, and RDATA[31:8] are not used. In UTOPIA L2 (reset default) or POS-PHY L2 modes, RDATA[7:0] are driven when one of the ports is selected for data transfer, and tri-stated when $\overline{REN}$ is deasserted, none of the ports is selected or data path reset is applied. RDATA[31:8] are tri-stated. In UTOPIA L3 or POS-PHY L3 modes, RDATA[31:0] are driven.
RPRTY	Oz	Receive Parity (tri-state) **RPRTY**: This signal indicates the parity on the data bus when parity generation is enabled. This option programmable. RPRTY is held low if parity generation is disabled. This signal is updated on the rising edge of RSCLK. In UTOPIA L2 (reset default) or POS-PHY L2 modes, this signal is driven when one of the ports is selected for data transfer, and tri-stated when $\overline{REN}$ is deasserted, none of the ports is selected or data path reset is active. In UTOPIA L3 or POS-PHY L3 modes this signal is driven.
$\overline{REN}$	I	Receive Enable (active low) $\overline{REN}$: This signal is used by the ATM/Link device to control the transfer of cell/packet data on the RDATA bus. If $\overline{REN}$ is high, no transfer occurs. If $\overline{REN}$ is low, a transfer occurs. This signal can be sampled on the rising edge of RSCLK.
RDXA[1] / RPXA / RSX	Oz	Receive Direct cell/packet Available [1] / Polled cell/packet Available / Start of Transfer (tri-state) This signal is tri-state when global reset is applied. **RDXA[1]**: This signal is active in UTOPIA L2, UTOPIA L3 or POS-PHY L2 modes when direct status mode is selected. It is used to indicate when port 1 can send data to the ATM/Link layer device. This signal is updated on the rising edge of RSCLK. In UTOPIA L2 or UTOPIA L3 modes, RDXA goes high when port 1 has more than a programmable number of ATM cells ready for transfer ("almost empty" level). RDXA goes low when the associated port does not have a complete ATM cell ready for transfer. In POS-PHY L2 mode, RDXA goes high when port 1 contains more data than the "almost empty" level or has an end of packet ready for transfer. RDXA goes low when the associated port does not have an end of packet ready for transfer and is "almost empty". **RPXA**: (Reset default) This signal is active in UTOPIA L2, UTOPIA L3 or POS-PHY L2 modes when polled status mode is selected. It is used to indicate when the polled port, as selected by RADR[4:0], can send data to the ATM/Link layer device. This signal is updated on the rising edge of RSCLK.

PIN	TYPE	FUNCTION
		In UTOPIA L2 or UTOPIA L3 modes, RPXA goes high when the polled port has more than a programmable number of ATM cells ready for transfer ("almost empty" level). RPXA goes low when the polled port does not have a complete ATM cell ready for transfer. In POS-PHY L2 mode, RPXA goes high when the polled port contains more data than the "almost empty" level or has an end of packet ready for transfer. RPXA goes low when the port does not have an end of packet ready for transfer and is "almost empty". In UTOPIA L2 (reset default) or POS-PHY L2 modes, this signal is driven when one of the ports is being polled, and is tri-stated when none of the ports is being polled or when data path reset is active. In UTOPIA L3 mode this signal is driven. **RSX**: This signal is active in POS-PHY L3 modes and indicates the start of a data transfer. This signal is updated on the rising edge of RSCLK. RSX goes high immediately before the start of data transfer to indicate that the in-band port address is present on RDATA. RSX goes high when the value of RDATA is the address of the receive port from which data is to be transferred. When RSX goes low, all subsequent transfers will be from the port specified by the in-band address. When RSX is high, RVAL must be low. This signal is always driven in POS-PHY L3 mode.
RDXA[4:2]	O	Receive Direct cell/packet Available [4:2] **RDXA[4:2]**: This signal is used to indicate when the associated port can send data to the ATM/Link layer device. This signal is updated on the rising edge of RSCLK. In UTOPIA L2 or UTOPIA L3 modes, RDXA goes high when the associated port has more than a programmable number of ATM cells ready for transfer ("almost empty" level). RDXA goes low when the associated port does not have a complete ATM cell ready for transfer. In POS-PHY L2 mode, RDXA goes high when the associated port contains more data than the "almost empty" level or has an end of packet ready for transfer. RDXA goes low when the associated port does not have an end of packet ready for transfer and is "almost empty". In POS-PHY Level 3 (or SPI-3) mode or when polled status mode is selected, these signals are held low.
RSOX	Oz	Receive Start Of cell/packet (tri-state) This signal is tri-state when global reset is applied. **RSOX**: This signal is used to indicate the first transfer of a cell/packet. This signal is updated on the rising edge of RSCLK. In UTOPIA L2 or UTOPIA L3 modes, RSOX is used to indicate the first transfer of a cell. In POS-PHY L2 or POS-PHY L3 modes, RSOX is used to indicate the first transfer of a packet. In UTOPIA L2 (reset default) or POS-PHY L2 modes, this signal is driven when one of the ports is selected for data transfer, and tri-stated when $\overline{REN}$ is deasserted, none of the ports is selected or data path reset is active. In UTOPIA L3 or POS-PHY L3 modes this signal is driven.
REOP	Oz	Receive End Of Packet (tri-state) This signal is tri-state when global reset is applied. **REOP**: In POS-PHY L2 or POS-PHY L3 modes, this signal is used to indicate the last transfer of a packet. This signal is updated on the rising edge of RSCLK. In UTOPIA L3 mode, this signal is held low. In POS-PHY L2 mode, this signal is driven when one of the ports is selected for data transfer, and tri-stated when $\overline{REN}$ is deasserted, none of the ports is selected or data path reset is active. In UTOPIA L2 (reset default) mode this signal is tri-stated. In all UTOPIA L3 or POS-PHY L3 modes this signal is driven.

PIN	TYPE	FUNCTION
RVAL	Oz	Receive packet data Valid(tri-state) This signal is tri-state when global reset is applied. **RVAL**: In POS-PHY L2 or POS-PHY L3 modes, this signal is used to indicate the validity of a receive data transfer. When RVAL is high, the receive data bus (RDATA, RPRTY, RSOX, REOP, RMOD, and RERR) is valid and a packet data transfer occurs. When RVAL is low, the receive data bus is invalid and a data transfer does not occurs. This signal is updated on the rising edge of RSCLK. RVAL goes high when a port is selected for packet data transfer and the port has a programmable size block of data or an end of packet ready for transfer. In POS-PHY L2 mode, RVAL goes low if the selected port is empty, at the end of a packet, or when $\overline{REN}$ is de-asserted. Once RVAL goes low, it will remain low until $\overline{REN}$ is de-asserted. In POS-PHY L3 mode, RVAL goes low if the selected port is empty or at the end of a packet if the minimum de-assertion time is greater than zero. RVAL will remain de-asserted for the programmable minimum de-assertion time. In UTOPIA L3 mode, this signal is held low. In POS-PHY L2 mode, this signal is driven when one of the ports is selected for data transfer, and tri-stated when $\overline{REN}$ is deasserted, none of the ports is selected or data path reset is active. In UTOPIA L2 (reset default) mode this signal is tri-stated. In all UTOPIA L3 or POS-PHY L3 modes this signal is driven.
RMOD[1:0]	Oz	Receive packet data Modulus [1:0] (tri-state) This signal is tri-state when global reset is applied. **RMOD[1:0]**: In POS-PHY L2 or POS-PHY L3 modes, this signal is used to indicate the number of valid bytes on the RDATA bus. RMOD[1:0]=00 RDATA[31:0] valid RMOD[1:0]=01 RDATA[31:8] valid RMOD[1:0]=10 RDATA[31:16] valid RMOD[1:0]=11 RDATA[31:24] valid This signal is updated on the rising edge of RSCLK. RMOD is only valid when REOP is high. In UTOPIA L3, 8-bit POS-PHY L2 or 8-bit POS-PHY L3 modes, RMOD[1:0] signals are held low. In 16-bit POS-PHY L2 or 16 bit POS-PHY L3 modes, RMOD[1] is held low. In POS-PHY L2 mode, these signals are driven when one of the ports is selected for data transfer, and tri-stated when $\overline{REN}$ is deasserted, none of the ports is selected or data path reset is active. In UTOPIA L2 (reset default) mode these signals are tri-stated. In UTOPIA L3 or POS-PHY L3 modes these signals are driven.
RERR	Oz	Receive packet Error (tri-state) This signal is tri-state when global reset is applied. **RERR**: In POS-PHY L2 or POS-PHY L3 modes, this signal is used to indicate that the current packet is erred. When RERR is high, the current packet should be aborted. This signal is updated on the rising edge of RSCLK. RERR is only valid when REOP is high. In UTOPIA L3 mode this signal is held low. In POS-PHY L2 mode, this signal is driven when one of the ports is selected for data transfer, and tri-stated when $\overline{REN}$ is deasserted, none of the ports is selected or data path reset is active. In UTOPIA L2 (reset default) mode this signal is tri-stated. In UTOPIA L3 or POS-PHY L3 modes, this signal is driven.
MICROPROCESSOR INTERFACE		
D[15:0]	I/O	Bidirectional 16 or 8-bit data bus This bus is tri-state when $\overline{RST}$ pin is low or $\overline{CS}$ pin is high. **D[15:0]**: A 16-bit or 8-bit data bus used to input data during register writes, and data

PIN	TYPE	FUNCTION
		outputs during register reads. The upper 8 bits are not used and never driven in 8-bit bus mode. Weak pullup resistors or bus holders should be used for each pin.
A[10:1]	I	Address bus (minus LSB) **A[10:1]**: identifies the specific 16 bit registers, or group of 8 bit registers, being accessed. A[10] must be tied to ground for the DS3161 and DS3162 versions.
A[0] / BSWAP		Address bus LSB / Byte Swap **A[0]**: This signal is connected to the lower address bit in 8-bit systems. (WIDTH=0) 1 = Output register bits 15:8 on D[7:0], D[15:8] not driven 0 = Output register bits 7:0 on D[7:0], D[15:8] not driven **BSWAP**: This signal is tied high or low in 16-bit systems. (WIDTH=1) 1 = Output register bits 15:8 on D[7:0], 7:0 on D[15:8] 0 = Output register bits 7:0 on D[7:0], 15:8 on D[15:8]
ALE	I	Address Latch Enable **ALE**: This signal is used to latch the address on the A[10:0] pins in multiplexed address systems. When it is high the address is fed through the address latch to the internal logic. When it transitions to low, the address is latched and held internally until the signal goes back high. ALE should be tied high for non-multiplexed address systems.
$\overline{CS}$	I	Chip Select (active low) $\overline{CS}$: This signal must be low during all accesses to the registers
$\overline{RD}$ / $\overline{DS}$	I	Read Strobe (active low) / Data Strobe (active low) $\overline{RD}$: Read Strobe mode (MODE=0): $\overline{RD}$ is low during a register read. $\overline{DS}$: Data Strobe mode (MODE=1): $\overline{DS}$ is low during either a register read or a write.
$\overline{WR}$ / R/$\overline{W}$	I	Write Strobe (active low) / R/W Select $\overline{WR}$: Write Strobe mode (MODE=0): $\overline{WR}$ is low during a register write. **R/$\overline{W}$**: Data Strobe mode (MODE=1): R/$\overline{W}$ is high during a register read cycle, and low during a register write cycle.
$\overline{RDY}$	Oz	Ready handshake (active low) $\overline{RDY}$: This ready signal is driven low when the current read or write cycle is in progress. When the current read or write cycle is not ready it is driven high. When device is not selected, it is not driven.
$\overline{INT}$	Oz	Interrupt (active low) This signal is tri-state when $\overline{RST}$ pin is low. $\overline{INT}$: This interrupt signal is driven low when an event is detected on any of the enabled interrupt sources in any of the register banks. When there are no active and enabled interrupt sources, the pin can be programmed to either drive high or not drive high. The reset default is to not drive high when there are no active and enabled interrupt source. All interrupt sources are disabled when $\overline{RST}$=0 and they must be programmed to be enabled.
MODE	I	Mode select $\overline{RD}$/$\overline{WR}$ or $\overline{DS}$ strobe mode **MODE**: 1 = Data Strobe Mode, 0 = Read/Write Strobe Mode
WIDTH	I	Data bus width select 8 or 16-bit interface **WIDTH**: 1 = 16-bits, 0 = 8 bits
MISC I/O		
GPIO1	I/O	General-Purpose I/O 1 **GPIO1**: This signal is configured to be a general-purpose I/O pin, or an alarm output signal for port 1.

PIN	TYPE	FUNCTION
GPIO2	I/O	General-Purpose I/O 2 **GPIO2**: This signal is configured to be a general-purpose I/O pin, or the 8KREFO output signal, or an alarm output signal for port 1.
GPIO3	I/O	General-Purpose I/O 3 **GPIO3**: This signal is configured to be a general-purpose I/O pin, or an alarm output signal for port 2.
GPIO4	I/O	General-Purpose I/O 4 **GPIO4**: This signal is configured to be a general-purpose I/O pin, or the 8KREFI input signal, or an alarm output signal for port 2. When configured for 8KREFI mode the signal frequency should be 8,000 Hz ±500ppm and about 50% duty cycle.
GPIO5	I/O	General-Purpose I/O 5 **GPIO5**: This signal is configured to be a general-purpose I/O pin, or an alarm output signal for port 3.
GPIO6	I/O	General-Purpose I/O 6 **GPIO6**: This signal is configured to be a general-purpose I/O pin, or the TMEI input signal, or an alarm output signal for port 3. When configured for TMEI input, the signal low time and high time must be greater than 500ns.
GPIO7	I/O	General-Purpose I/O 7 **GPIO7**: This signal is configured to be a general-purpose I/O pin, or an alarm output signal for port 4.
GPIO8	I/O	General-Purpose I/O 8 **GPIO8**: This signal is configured to be a general-purpose I/O pin, or the PMU input signal, or an alarm output signal for port 4. When configured for PMU input, the signal low time and high time must be greater than 500 ns.
$\overline{\text{TEST}}$	I	Test enable (active low) $\overline{\text{TEST}}$: This signal enables the internal scan test mode when low. For normal operation tie high. This is an asynchronous input.
$\overline{\text{HIZ}}$	I	High-impedance test enable (active low) $\overline{\text{HIZ}}$: This signal puts all digital output and bi-directional pins in the high-impedance state when it low and $\overline{\text{JTRST}}$ is low. For normal operation tie high. This is an asynchronous input.
$\overline{\text{RST}}$	I	Reset (active low) $\overline{\text{RST}}$: This signal resets all the internal processor registers and logic when low. This pin should be low while power is applied and set high after the power is stable. This is an asynchronous input.
JTAG		
JTCLK	I	JTAG Clock **JTCLK**: This clock input is typically a low frequency (less than 10MHz) 50% duty cycle clock signal.
JTMS	Ipu	JTAG Mode Select (with pullup) **JTMS**: This input signal is used to control the JTAG controller state machine and is sampled on the rising edge of JTCLK.
JTDI	Ipu	JTAG Data Input (with pullup) **JTDI**: This input signal is used to input data into the register that is enabled by the JTAG controller state machine and is sampled on the rising edge of JTCLK.
JTDO	Oz	JTAG Data Output **JTDO**: This output signal is the output of an internal scan shift register enabled by the JTAG controller state machine and is updated on the falling edge of JTCLK. The pin is in the high-impedance mode when a register is not selected or when the $\overline{\text{JTRST}}$ signal is high. The pin goes into and exits the high-impedance mode after the falling edge of JTCLK

PIN	TYPE	FUNCTION
$\overline{\text{JTRST}}$	Ipu	JTAG Reset (active low with pullup) $\overline{\text{JTRST}}$: This input forces the JTAG controller logic into the reset state and forces the JTDO pin into high impedance when low. This pin should be low while power is applied and set high after the power is stable. The pin can be driven high or low for normal operation, but must be high for JTAG operation.
CLAD		
CLKA	I	Clock A **CLKA**: This clock input is a DS3 signal (44.736MHz ±20ppm) when the CLAD is disabled or it is one of the CLAD reference clock signals when the CLAD is enabled.
CLKB	IO	Clock B **CLKB**: This pin is a E3 (34.368 MHz ±20ppm) input signal when the CLAD is disabled or it can be enabled to output a generated clock when the CLAD is enabled. The pin is driven low when it is not selected to output a clock signal and the CLAD is enabled. Refer to Table 10-9.
CLKC	IO	Clock C **CLKC**: This pin is a STS-1 (51.84 MHz ±20ppm) input signal when the CLAD is disabled or it can be enabled to output a generated clock when the CLAD is enabled. The pin is driven low when it is not selected to output a clock signal and the CLAD is enabled. Refer to Table 10-9.
POWER		
VSS	PWR	Ground, 0V potential Common to digital core, digital IO and all analog circuits.
VDD	PWR	Digital 3.3V Common to digital core and digital IO.
AVDDC	PWR	Analog 3.3V for CLAD Powers clock rate adapter common to all ports.

8.3 Pin Functional Timing

8.3.1 Line I/O

8.3.1.1 B3ZS/HDB3/AMI Mode Transmit Pin Functional Timing

There is no suggested time alignment between the TX LINE signals and the TLCLKn clock signal. The TX DATA signal is not a readily available signal, it is meant to represent the data value of the other signals.

The TPOSn, TNEGn and TLCLKn signals are available when the line is in B3ZS/HDB3 or AMI mode and the transmit line pins are enabled.

The TPOSn and TNEGn signals change a small delay after the positive edge of the reference clock if the clock pin is not inverted; otherwise they change after the negative edge. The TLCLKn clock pin is the clock reference typically used for the TPOSn and TNEGn signals, but they can be time referenced to the TCLKIn, TCLKOn, RLCLKn or RCLKOn clock pins. The TPOSn and TNEGn pins can be inverted.

Figure 8-1 and Figure 8-2 show the relationship between the digital outputs.

Figure 8-1. TX Line I/O B3ZS Functional Timing Diagram

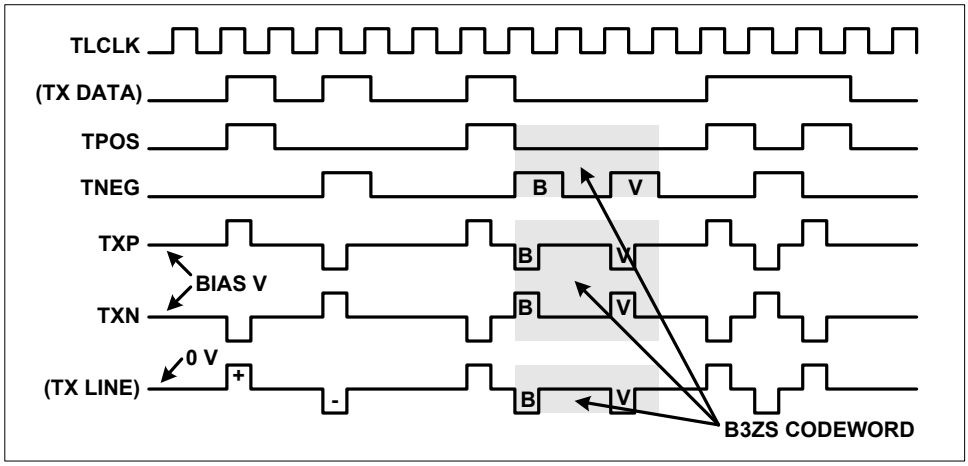
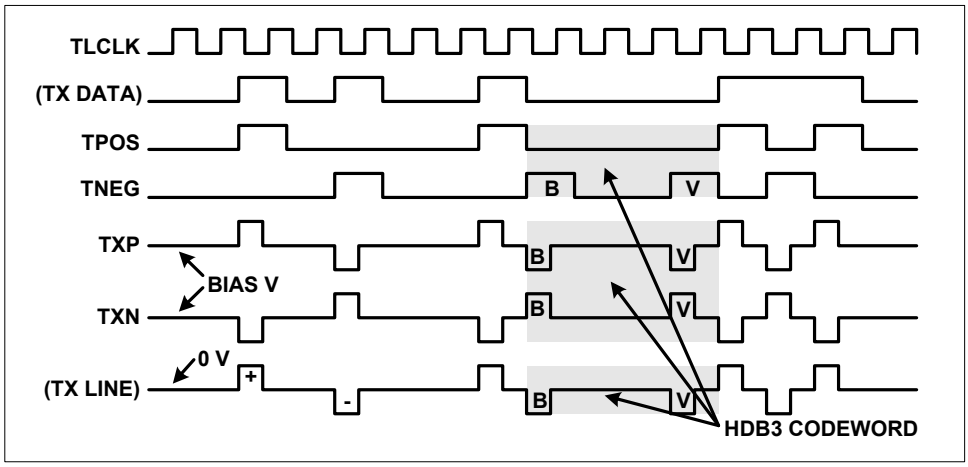


Figure 8-2. TX Line I/O HDB3 Functional Timing Diagram



8.3.1.2 B3ZS/HDB3/AMI Mode Receive Pin Functional Timing

There is no suggested time alignment between the RX LINE signals and the RLCLKn clock signal. The RX DATA signal is not an always readily available signal, it is meant to represent the data value of the other signals.

The RPOSn, RNEGn and RLCLKn pins are available when the line is in B3ZS/HDB3 or AMI mode

The RPOSn and RNEGn signals are sampled at the rising edge of the reference clock signal if the clock pin is not inverted, otherwise they are sampled at the negative edge. The RLCLKn clock pin is the clock reference used for the RPOSn and RNEGn signals. The RPOSn and RNEGn pins can be inverted.

Figure 8-3 and Figure 8-4 show the relationship between the digital outputs.

Figure 8-3. RX Line I/O B3ZS Functional Timing Diagram

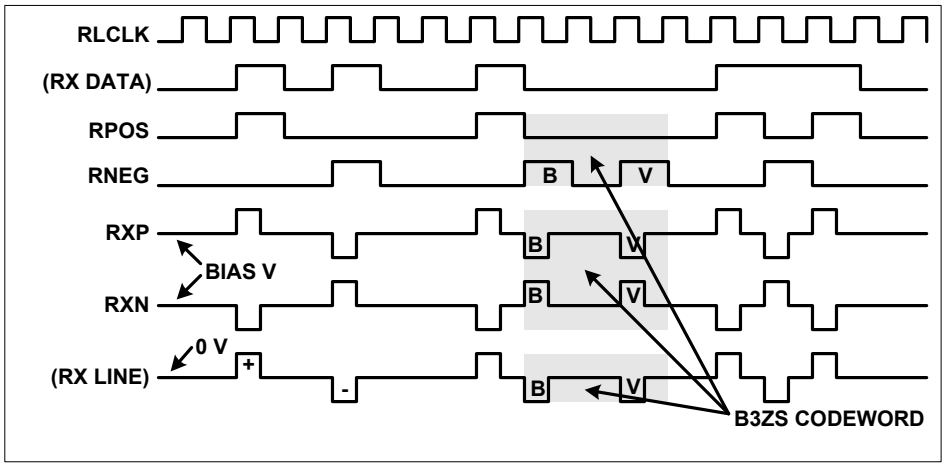
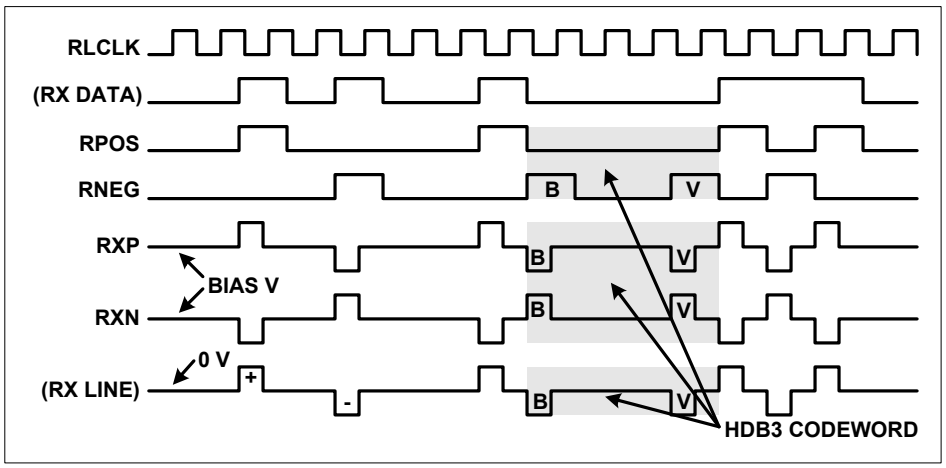


Figure 8-4. RX Line I/O HDB3 Functional Timing Diagram



8.3.1.3 UNI Mode Transmit Pin Functional Timing

The TDATn pin is available when the line interface is in the UNI mode and the transmit line pins are enabled. The TOHMOn and TOHMIn pins are available when the framer is in one of the “- OHM” modes and the transmit line pins are enabled. The line interface is forced into the UNI mode when the framer is in one of the “- OHM” modes.

The TOHMIn pin is used to control the insertion of gaps in the data by stopping the internal formatters and data sources. These gaps are inserted where external logic will add more overhead bits to the signal. The TOHMOn signal is delayed from the TOHMIn signal by three clock periods. The TOHMOn signal aligns to the TDATn signal and is high when internal framing and signal source has stopped inserting data. The TDATn signal should be

ignored when TOHMOn is high. In the “- OHM Octet” framing modes, the first payload bit after the TOHMOn signal goes low is the MSB (Bit 1) of a payload Octet.

The TDATn and TOHMOn signals change a small delay after the positive edge of the reference clock signal if the clock pin is not inverted; other wise they change after the negative edge. The TOHMIn signal is sampled at the rising edge of the reference clock signal if the clock pin is not inverted; otherwise it is sampled at the negative edge. The TLCLKn clock pin is the clock reference typically used for the TDATn, TOHMOn and TOHMIn signals, but they can be time referenced to the TCLKIn, TCLKOn, RLCLKn or RCLKOn clock pins. The TDATn, TOHMOn, and TOHMIn pins can be inverted. See Figure 8-5 and Figure 8-6.

Figure 8-5. TX Line I/O UNI OHM Functional Timing Diagram

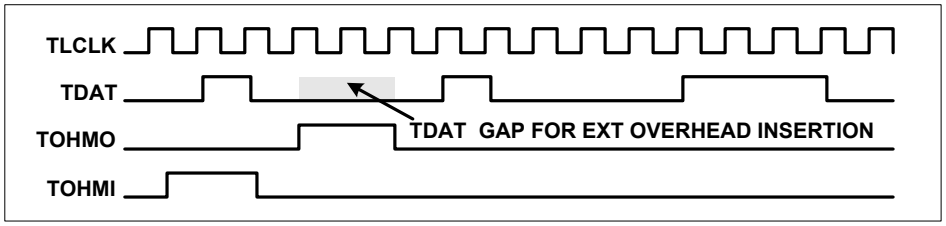
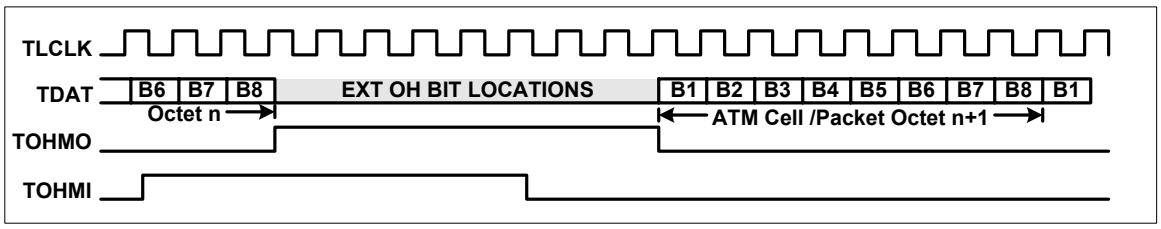


Figure 8-6. TX Line I/O UNI Octet Aligned OHM Functional Timing Diagram



8.3.1.4 UNI Mode Receive Pin Functional Timing

The RDATn pin is available when the line interface is in the UNI mode. The ROHMIn pin is available when the framer is in one of the “-OHM” modes. The RLCVn pin is available when the line interface is in the UNI mode and the framer is not in one of the “-OHM” modes. The line interface is forced into the UNI mode when the framer is in one of the “-OHM” modes.

The ROHMIn pin is used to mark the RDATn bits that will be ignored by the internal receive logic. When the ROHMIn pin is high, the internal framers and data sinks will ignore the corresponding RDATn bits. In the “- OHM Octet” framing modes, the data on RDATn is octet-aligned with the ROHMIn signal, the first bit of the serial data on RDATn is the MSB (Bit 1) of a payload Octet.

All bits on the RDATn pin, even the bits that are marked by ROHMIn, will come out the RSERn pin, if the RSERn pin is enabled.

The signal on the RLCVn pin enables the BPV counter, which is in the line interface, to increment each clock it is high.

The RDATn, ROHMIn and RLCVn signals are sampled at the rising edge of the reference clock signal if the clock pin is not inverted; otherwise they are sampled at the negative edge. The RLCLKn clock pin is the clock reference used for the RDATn, ROHMIn and RLCVn signals. The RDATn, ROHMIn and RLCVn pins can be inverted. Please refer to Figure 8-7 and Figure 8-8.

Figure 8-7. RX Line I/O OHM UNI Functional Timing Diagram

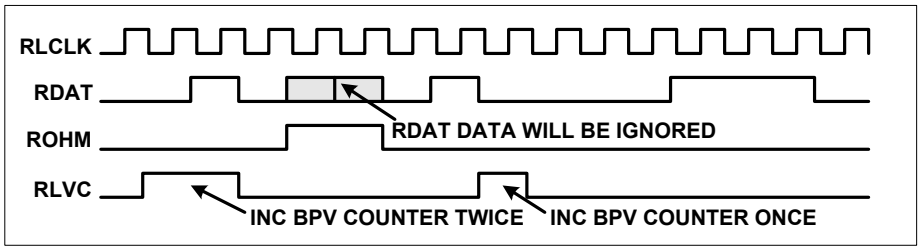
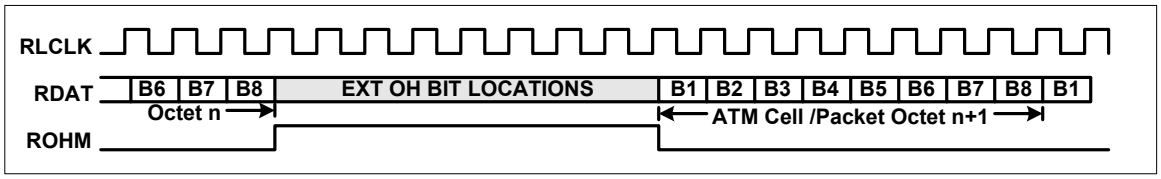


Figure 8-8. RX Line I/O UNI Octet Aligned OHM Functional Timing Diagram



8.3.2 DS3/E3 Framing and PLCP Overhead Functional Timing

Figure 8-9 shows the relationship between the DS3 receive overhead port pins.

Figure 8-9. DS3 Framing Receive Overhead Port Timing

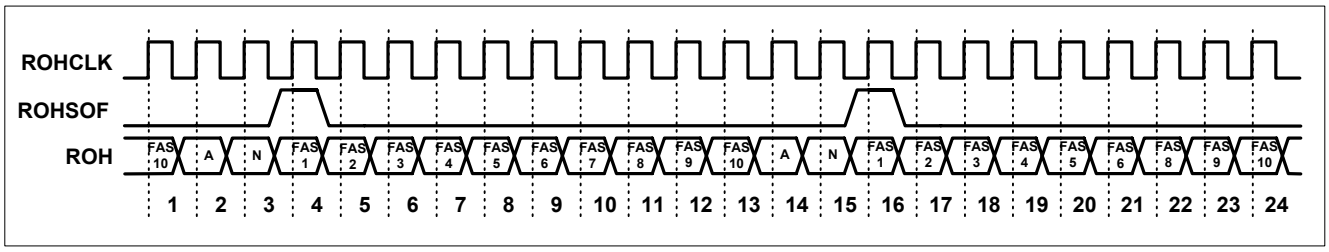


Figure 8-10 shows the relationship between the E3 G.751 receive overhead port pins.

Figure 8-10. E3 G.751 Framing Receive Overhead Port Timing

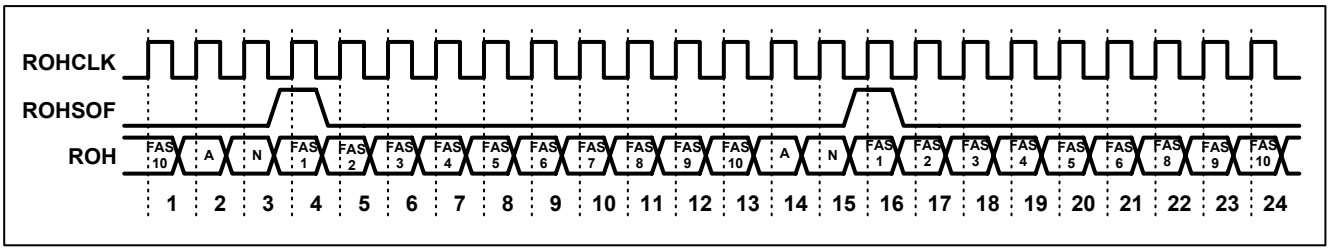


Figure 8-11 shows the relationship between the E3 G.832 receive overhead port pins.

Figure 8-11. E3 G.832 Framing Receive Overhead Port Timing

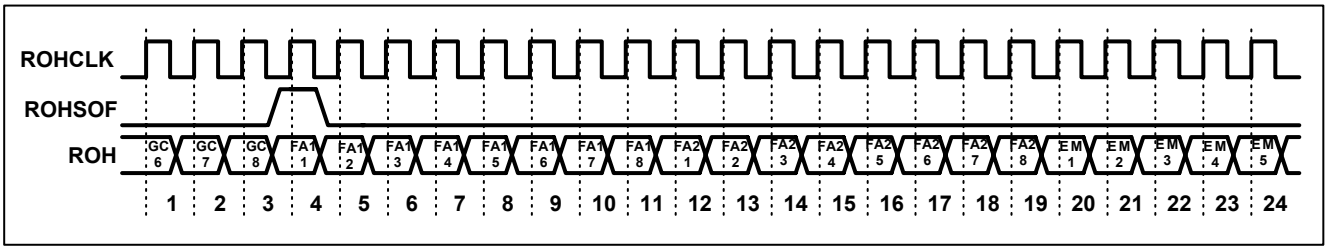


Figure 8-12 shows the relationship between the DS3 transmit overhead port pins.

Figure 8-12. DS3 Framing Transmit Overhead Port Timing

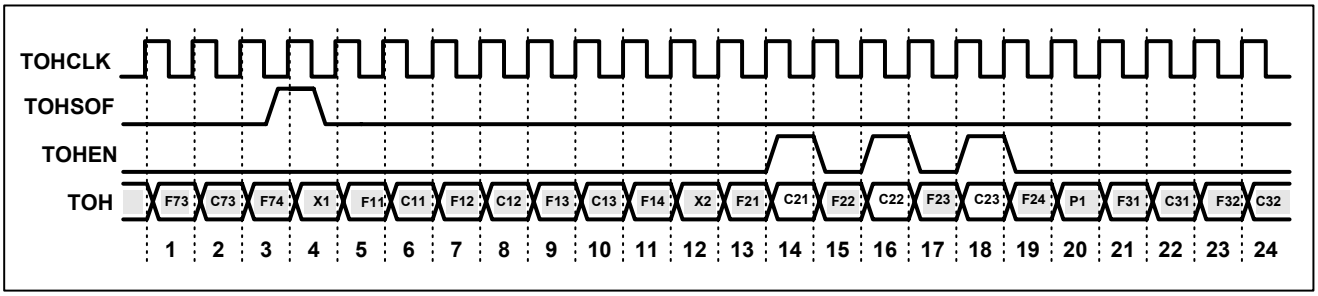


Figure 8-13 shows the relationship between the E3 G.751 transmit overhead port pins.

Figure 8-13. E3 G.751 Framing Transmit Overhead Port Timing

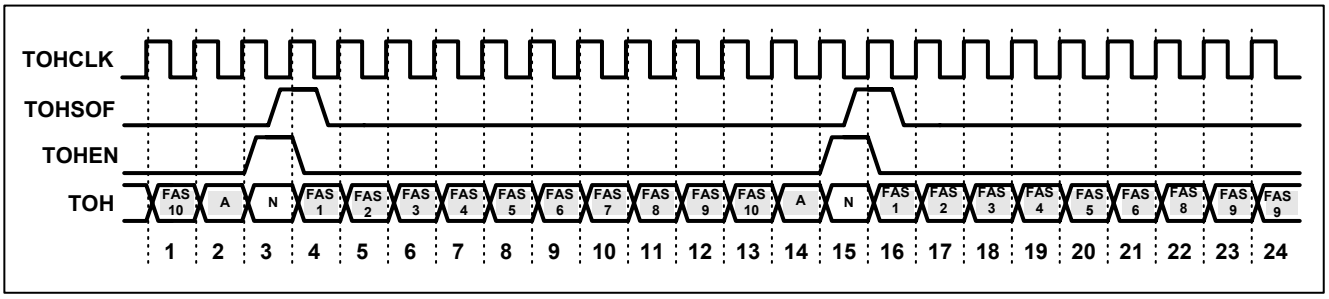


Figure 8-14 shows the relationship between the E3 G.832 transmit overhead port pins.

Figure 8-14. E3 G.832 Framing Transmit Overhead Port Timing

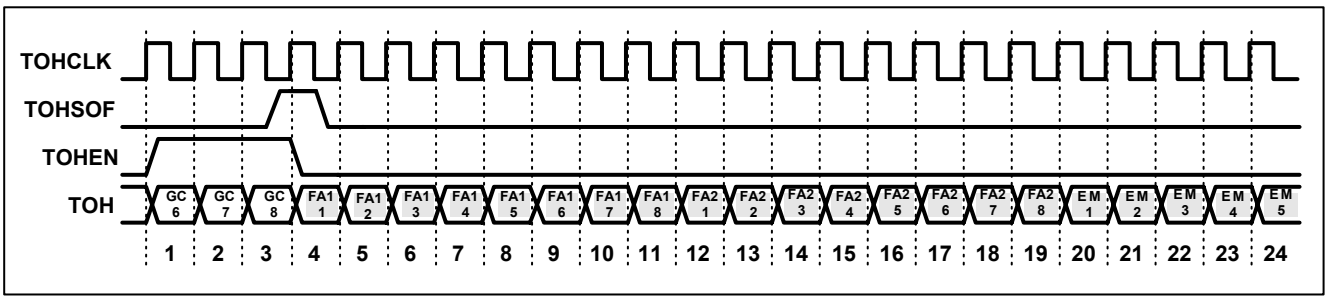


Figure 8-15 shows the relationship between the DS3 PLCP receive overhead port pins.

Figure 8-15. DS3 PLCP Receive Overhead Port Timing

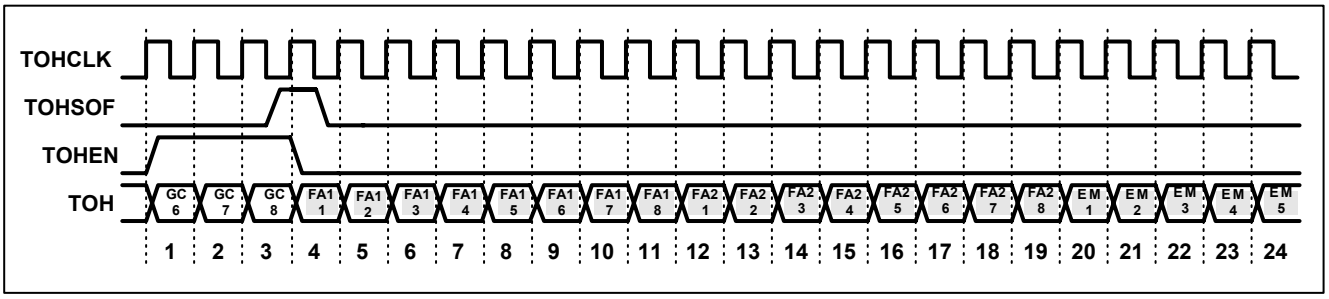


Figure 8-16 shows the relationship between the E3 G.751 PLCP receiver overhead port pins.

Figure 8-16. E3 G.751 PLCP Receive Overhead Port Timing

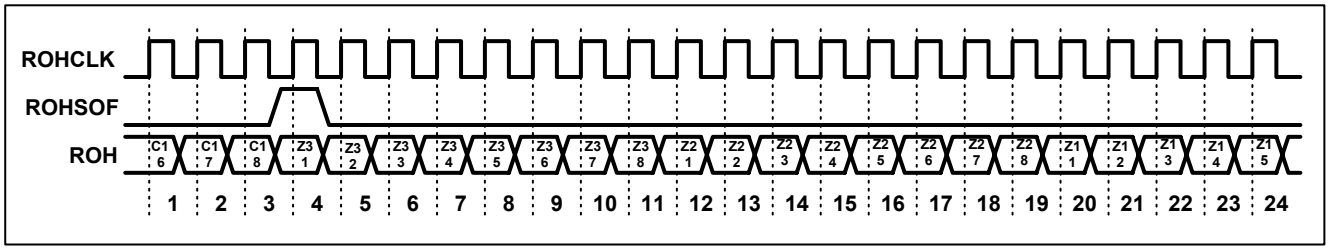


Figure 8-17 shows the relationship between the DS3 PLCP transmit overhead port pins.

Figure 8-17. DS3 PLCP Transmit Overhead Port Timing

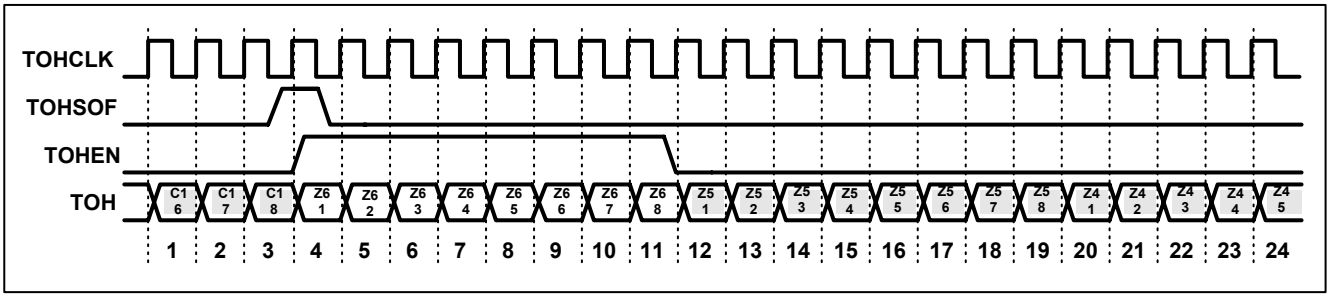
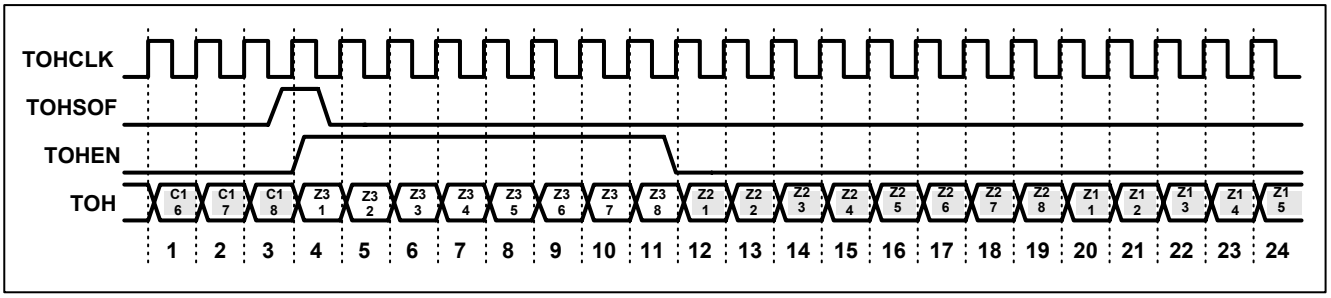


Figure 8-18 shows the relationship between the E3 G.751 PLCP transmit overhead port pins.

Figure 8-18. E3 G.751 PLCP Transmit Overhead Port Timing



8.3.3 Internal (IFRAC) and External (XFRAC) Fractional DS3/E3 Overhead Functional Timing

The fractional overhead pins provide the ability to insert bits in the DS3/E3 payload that are not used for cells or packets. The source of fractional overhead bits is controlled by an internal register (see FRAC.TCR), specifying internal generation or external sourcing via the TFOHENIn pin. The allocation of DS3/E3 payload used for cell and packet data is also programmable or controlled by the TFOHENIn pin. The TSOFIn, TSOFOn, TDENn, RSOFOn and RDENn pins are used to determine which bit positions are DS3/E3 overhead so that fractional overhead bits will be inserted only in DS3/E3 payload. The TCLKOn and RCLKOn clocks can be configured for gapped modes that will toggle for each fractional overhead bit, allowing a simple way of using the overhead bits for messaging.

Figure 8-19 shows the timing with the external fractional transmit port pins

P designates payload bits, F designates fractional overhead, and L designates DS3/E3 overhead, based on TDEN.

Figure 8-19. External (XFRAC) Transmit Fractional Timing

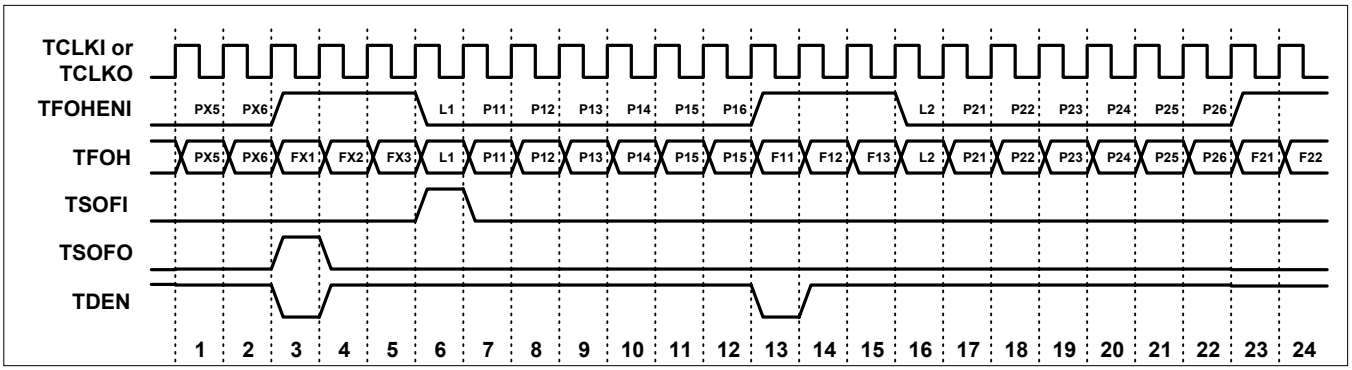


Figure 8-20 shows the timing with the external fractional receive port pins

Figure 8-20. External (XFRAC) Receive Fractional Timing

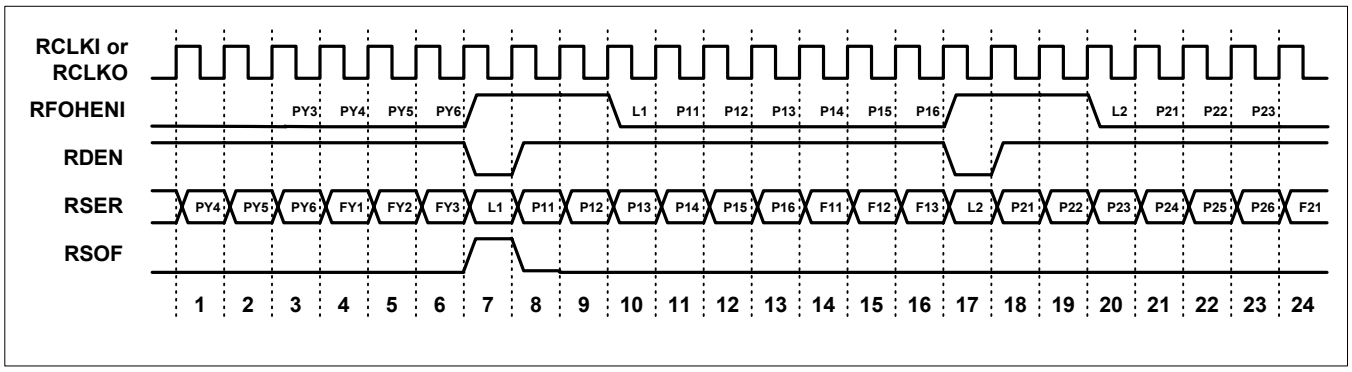


Figure 8-21 shows the timing with the internal fractional transmit port pins

Figure 8-21. Internal (IFRAC) Transmit Fractional Timing

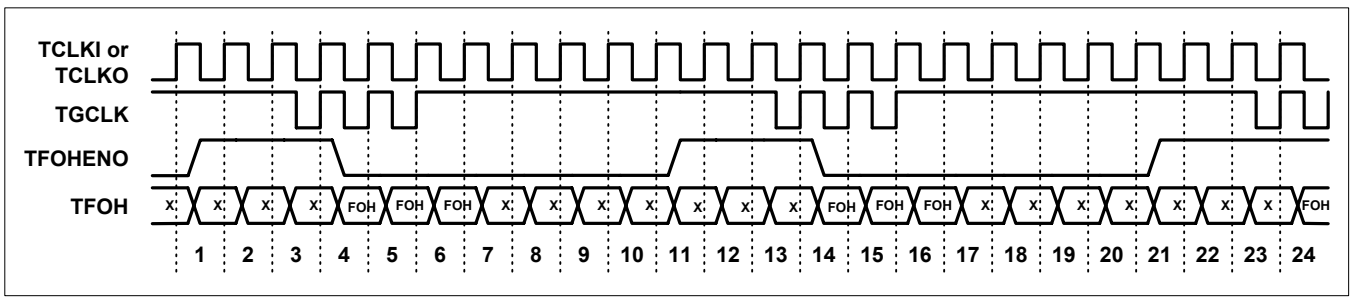
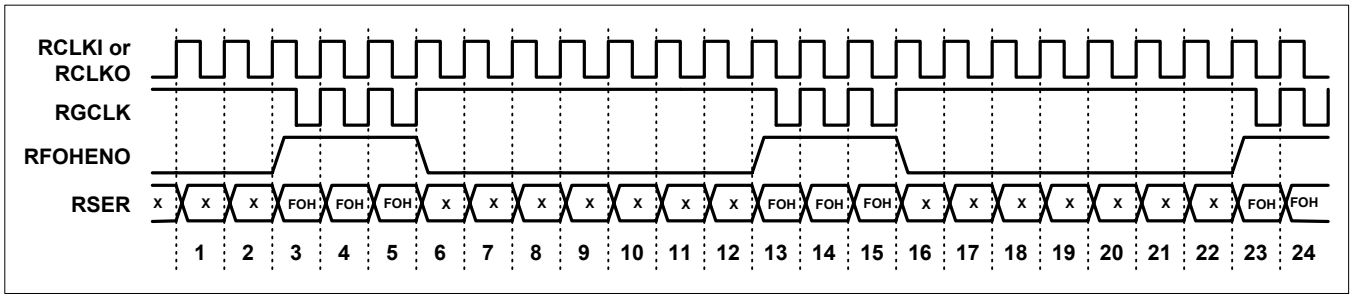


Figure 8-22 shows the timing with the internal fractional transmit port pins

Figure 8-22. Internal (IFRAC) Receive Fractional Timing



8.3.4 Flexible Fractional (FFRAC) DS3/E3 Overhead Interface Functinal Timing

The Flexible fractional mode provides the capability to modify the payload data from the cell/packet processor before inserting it into the DS3 or E3 payload. The bit rate of the payload from the cell/packet processor can be less than the DS3 or E3 payload bit rate. The interface to the DS3 or E3 payload uses the TSOFIn, TSOFOn, TDENn, TSERn, RSOFOn, RDENn and RSERn pins. The interface to the cell/packet processor uses the TPDENIn, TPDENOn, TPDATn, RPDENIn and RPDATn pins. The TPDENIn pin is used to determine the bit rate of the transmit cell/packet payload data. The TPDENOn pin is high when the data on TPDATn is valid. The delay between TPDENIn and TPDENOn is three clocks. The RPDENIn pin is used to determine the bit rate of the receive cell/packet processor data. The cell/packet processor uses the cell/packet data on the RPDATn pin when the RPDENIn pin is high.

Figure 8-23 shows the timing with the flexible fractional transmit port pins

Figure 8-23. Transmit Flexible Fractional (FFRAC) Timing

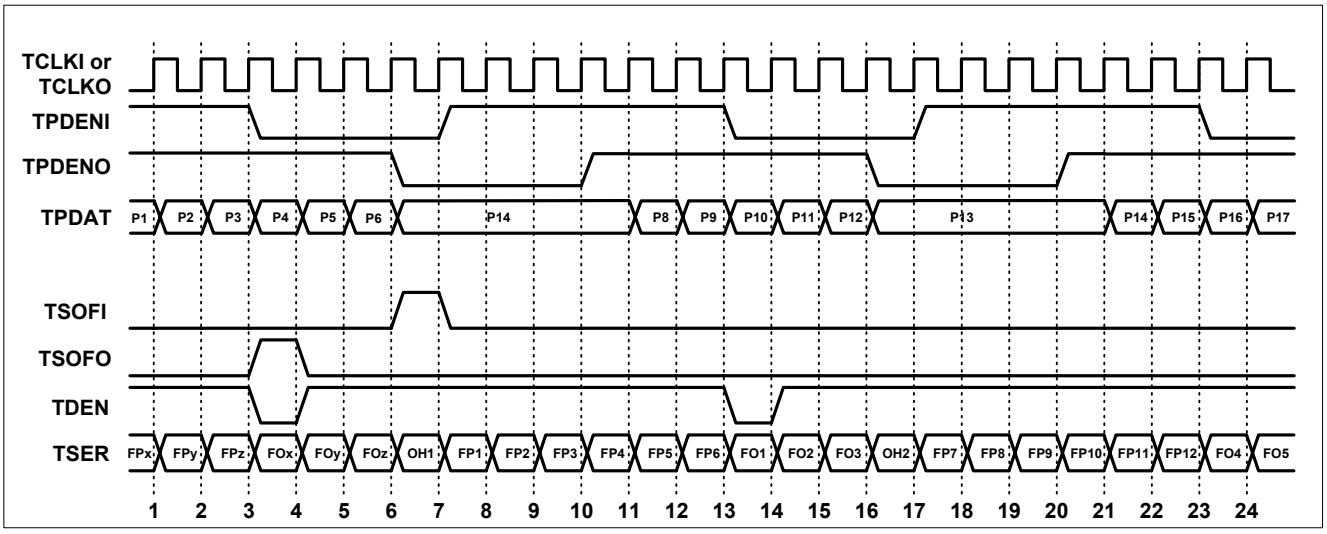
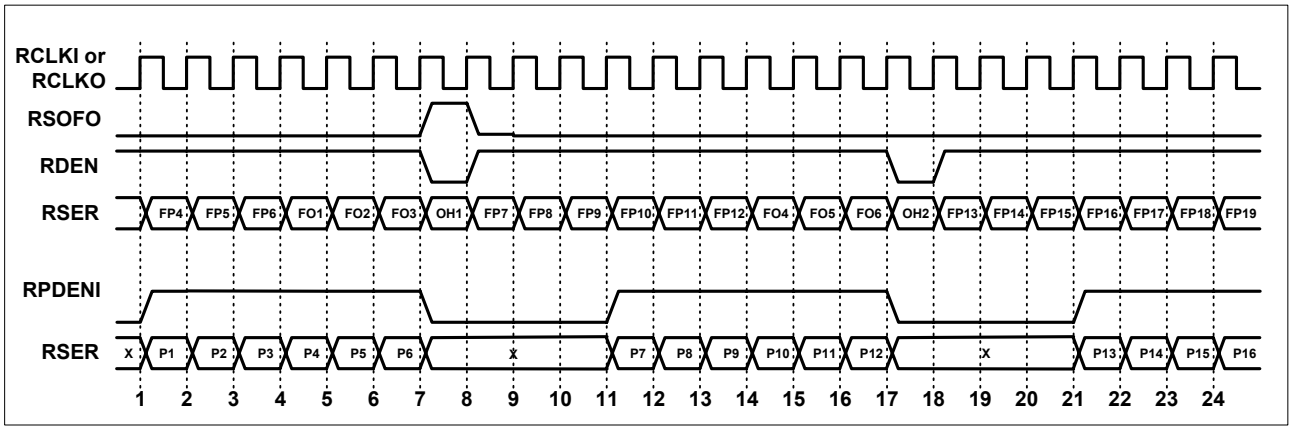


Figure 8-24 shows the timing with the flexible fractional receive port pins

Figure 8-24. Receive Flexible Fractional (FFRAC) Timing



8.3.5 UTOPIA/POS-PHY/SPI-3 System Interface Functional Timing

8.3.5.1 UTOPIA Level 2 Functional Timing

Figure 8-25 shows a multi-device transmit interface multiple cell transfer to different PHY devices. On clock edge 2, the ATM device places address ‘00h’ on the address bus (which is mapped to Port 1). PHY device '1' (Port 1) indicates to the ATM device that it can accept cell data by asserting TDXA[1]. On clock edge 4, the ATM device selects PHY device '1'. On clock edge 5, the ATM device starts a cell transfer to PHY device '1' by asserting $\overline{\text{TEN}}$, placing the first byte of cell data on TDATA, and asserting TSOX to indicate the transfer of the first byte of the cell. On clock edge 6, the ATM device de-asserts TSOX as it continues to place additional bytes of the cell on TDATA.. On clock edge 13, PHY device ‘2’ asserts TDXA[2] to indicate to the ATM device that it is ready to accept cell data. On clock edge 15, PHY device '1’ indicates that it cannot accept the transfer of a complete cell by de-asserting TDXA[1]. On clock edge 16, the ATM device deselects PHY device '1' and selects PHY device '2' by de-asserting $\overline{\text{TEN}}$ and placing PHY device '2's address on TADR. On clock edge 17, the ATM device starts the transfer of a cell to PHY device '2' by asserting $\overline{\text{TEN}}$, placing the first byte of cell data on TDATA, and asserting TSOX to indicate the transfer of the first byte of the cell. On clock edge 18, the ATM device de-asserts TSOX as it continues to place additional bytes of the cell on TDATA.

Figure 8-25. UTOPIA Level 2 Transmit Cell Transfer Direct Mode

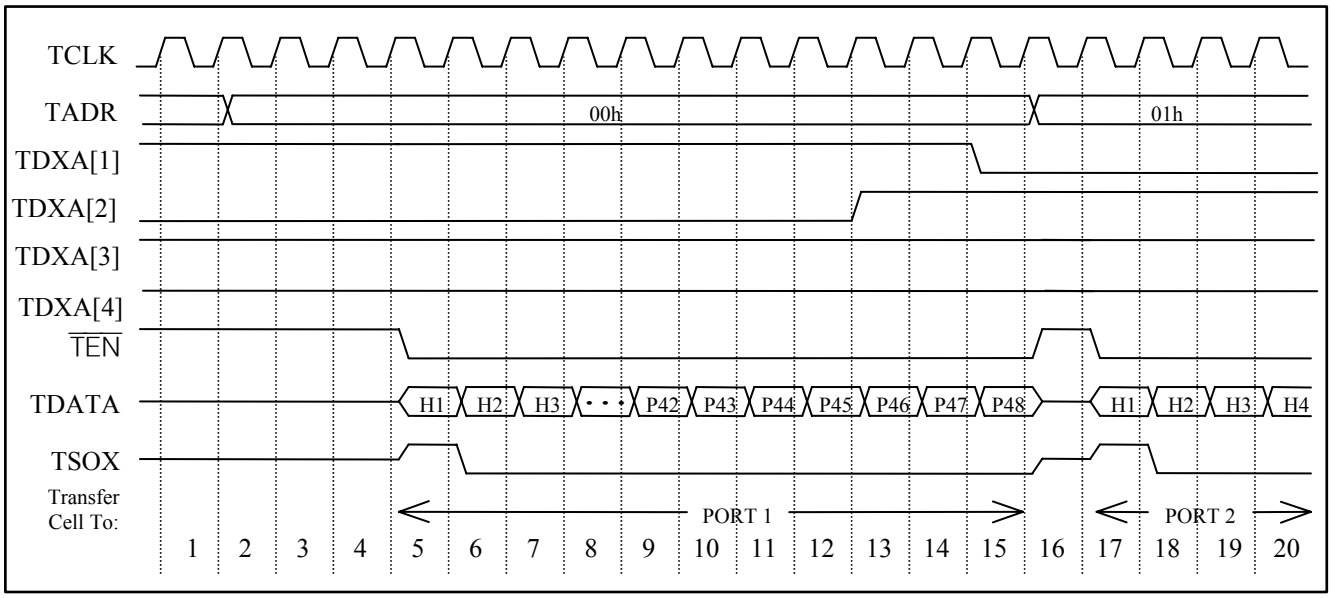


Figure 8-26 shows a multi-device transmit interface multiple cell transfer to different PHY devices. On clock edge 2, the ATM device places address ‘00h’ on the address bus (which is mapped to Port 1). PHY device '1' (Port 1) indicates to the ATM device that it has a complete cell to send by asserting RDXA[1]. On clock edge 4, the ATM device selects PHY device '1'. On clock edge 5, the ATM device asserts $\overline{REN}$. On clock edge 6, the PHY device ‘1’ starts a cell transfer to the ATM device by placing the first byte of cell data on RDATA, and asserting RSOX to indicate the transfer of the first byte of the cell. On clock edge 7, the PHY device de-asserts RSOX as it continues to place additional bytes of the cell on RDATA. On clock edge 13, PHY device ‘2’ asserts RDXA[2] to indicate to the ATM device that it is ready to send a cell. On clock edge 15, PHY device '1’ indicates that it cannot transfer a complete cell by de-asserting RDXA[1]. On clock edge 16, the ATM device deselects PHY device '1' and selects PHY device '2' by de-asserting $\overline{REN}$ and placing PHY device '2's address on RADR. On clock edge 17, the ATM device asserts REN. On clock edge 18, PHY device ‘2’ (Port 2) starts the transfer of a cell to the ATM device by placing the first byte of cell data on RDATA, and asserting RSOX to indicate the transfer of the first byte of the cell. On clock edge 18, the PHY device de-asserts RSOX as it continues to place additional bytes of the cell on RDATA.

Figure 8-26. UTOPIA Level 2 Receive Cell Transfer Direct Mode

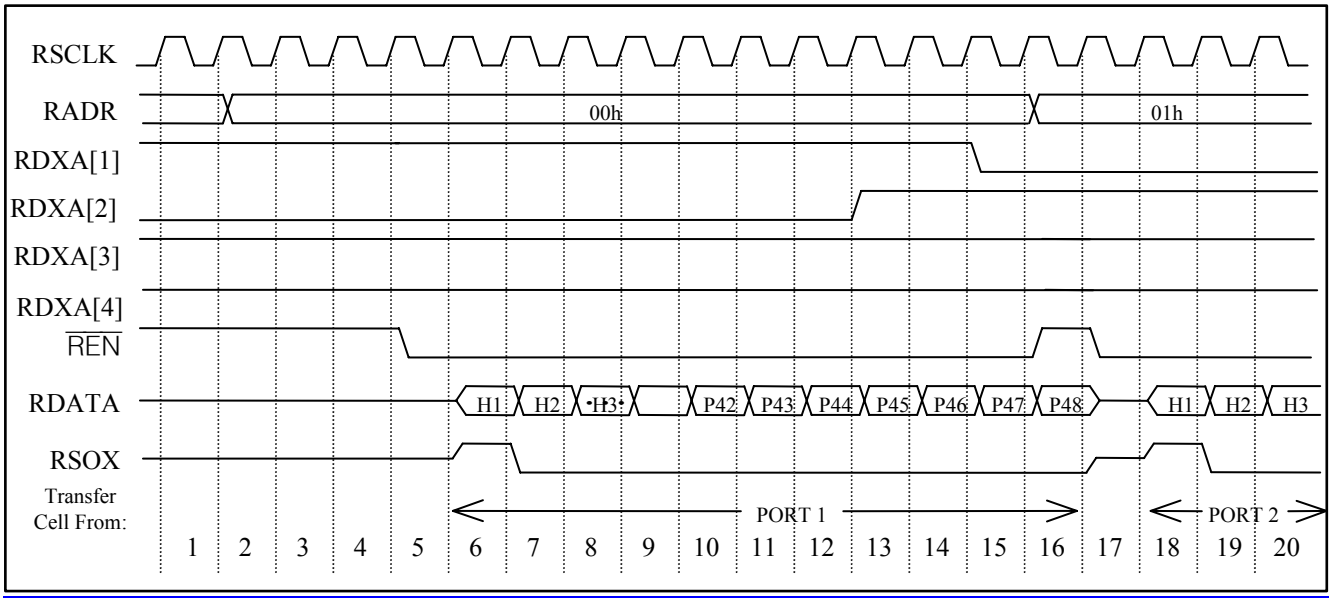


Figure 8-27 shows a multi-device transmit interface multiple cell transfer to different PHY devices. On clock edge 2, the ATM device polls PHY device 'N'. On clock edge 3, PHY device 'N' indicates to the ATM device that it can accept cell data by asserting TPXA. On clock edge 4, the ATM device selects PHY device 'N'. On clock edge 5, the ATM device starts a cell transfer to PHY device 'N' by asserting $\overline{TEN}$, placing the first byte of cell data on TDATA, and asserting TSOX to indicate the transfer of the first byte of the cell. On clock edge 6, the ATM device de-asserts TSOX as it continues to place additional bytes of the cell on TDATA. On clock edge 6, the ATM device also polls PHY device 'O'. On clock edge 7, PHY device 'O' indicates that it can accept the transfer of a complete cell. On clock edge 14, the ATM device polls PHY device 'N'. On clock edge 15, PHY device 'N' indicates that it cannot accept the transfer of a complete cell. On clock edge 16, the ATM device deselects PHY device 'N' and selects PHY device 'O' by de-asserting $\overline{TEN}$ and placing PHY device 'O's address on TADR. On clock edge 17, the ATM device starts the transfer of a cell to PHY device 'O' by asserting $\overline{TEN}$, placing the first byte of cell data on TDATA, and asserting TSOX to indicate the transfer of the first byte of the cell. On clock edge 18, the ATM device de-asserts TSOX as it continues to place additional bytes of the cell on TDATA.

Figure 8-27. UTOPIA Level 2 Transmit Multiple Cell Transfer Polled Mode

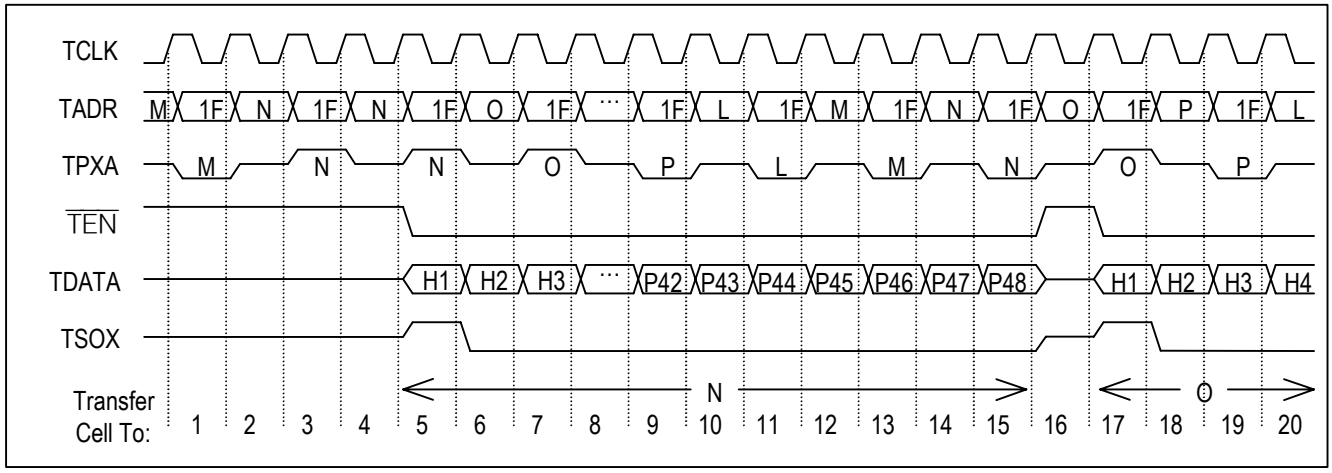


Figure 8-28 shows a multi-device receive interface multiple cell transfer from different PHY devices. On clock edge 2, the ATM device polls PHY device 'N'. On clock edge 3, PHY device 'N' indicates to the ATM device that it has a complete cell ready for transfer by asserting RPXA. On clock edge 4, the ATM device selects PHY device 'N'. On clock edge 5, the ATM device asserts $\overline{REN}$. On clock edge 6, PHY device 'N' starts a cell transfer by placing the first byte of cell data on RDATA, and asserting RSOX to indicate the transfer of the first byte of the cell. On clock edge 7, PHY device 'N' de-asserts RSOX as it continues to place additional bytes of the cell on RDATA. On clock edge 12, the ATM device polls PHY device 'O'. On clock edge 13, PHY device 'O' indicates to the ATM device that it has a complete cell ready for transfer by asserting RPXA. On clock edge 16, the ATM device deselects PHY device 'N' and selects PHY device 'O' by de-asserting $\overline{REN}$ and placing PHY device 'O's address on RADR. On clock edge 17, the ATM device asserts $\overline{REN}$ and PHY device 'N' stops transferring cell data and tri-states its RDATA and RSOX outputs. On clock edge 18, PHY device 'O' starts a cell transfer by placing the first byte of cell data on RDATA, and asserting RSOX to indicate the transfer of the first byte of the cell. On clock edge 19, PHY device 'O' de-asserts RSOX as it continues to place additional bytes of the cell on RDATA.

Figure 8-28. UTOPIA Level 2 Receive Multiple Cell Transfer Polled Mode

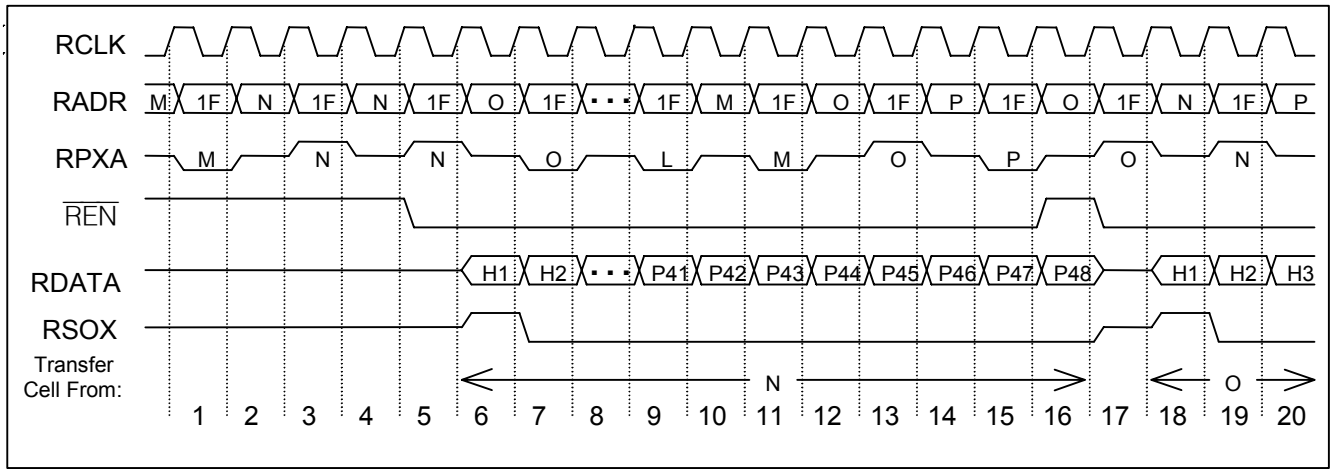
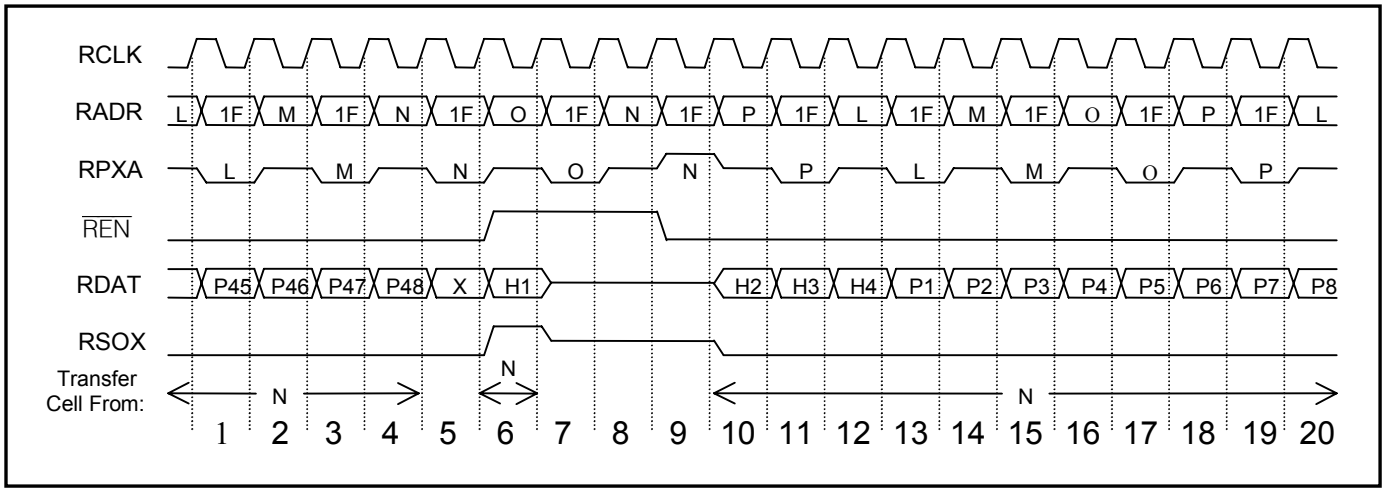


Figure 8-29 shows a multi-device receive interface unexpected multiple cell transfer. Prior to clock edge 1, the cell transfer was started. On clock edge 4, since no other PHY device has a cell ready for transfer, the ATM device assumes another cell transfer from PHY device 'N' and leaves $\overline{REN}$ asserted. On clock edge 5, PHY device 'N' stops transferring cell data and indicates that it does not have another cell ready for transfer by not asserting RSOX. On clock edge 6, the ATM device deasserts $\overline{REN}$ to end the cell transfer process. At the same time, PHY device 'N' indicates to the ATM device that it now has a complete cell ready for transfer by placing the first byte of cell data on RDAT, and asserting RSOX to indicate the transfer of the first byte of the cell. On clock edge 7, PHY device 'N' tri-states its RDAT and RSOX outputs because $\overline{REN}$ is deasserted. On clock edge 8, the ATM device selects PHY device 'N'. On clock edge 9, the ATM device asserts $\overline{REN}$. On clock edge 10, PHY device 'N' continues the cell transfer by placing the second byte of cell data on RDAT, and deasserting RSOX.

Figure 8-29. UTOPIA Level 2 Receive Unexpected Multiple Cell Transfer



8.3.5.2 UTOPIA Level 3 Functional Timing

Figure 8-30 shows a multi-port transmit interface multiple cell transfer to different PHY devices. PHY port '1', '3', '4' indicate to the ATM device that they can accept cell data by asserting the TDXA[n]. On clock edge 2, the ATM device selects PHY port '1' by putting address '00h' on the address bus. On clock edge 5, the ATM device starts a cell transfer to PHY port '1' by asserting $\overline{TEN}$, placing the first byte of cell data on TDATA, and asserting TSOX to indicate the transfer of the first byte of the cell. On clock edge 6, the ATM device de-asserts TSOX as it continues to place additional bytes of the cell on TDATA. On clock edge 13, PHY port '2' asserts TDXA[2] to indicate it is ready to accept a cell. On clock edge 15, PHY port '1' deasserts TDXA[1] to indicate to the ATM device that it does not have the availability to receive another complete cell. On clock edge 16, the ATM device selects PHY port '2' by de-asserting $\overline{TEN}$ and placing PHY port '2's address on TADR. On clock edge 17, the ATM device starts the transfer of a cell to PHY port '2' by asserting $\overline{TEN}$, placing the first byte of cell data on TDATA, and asserting TSOX to indicate the transfer of the first byte of the cell. On clock edge 18, the ATM device de-asserts TSOX as it continues to place additional bytes of the cell on TDATA.

Figure 8-30. UTOPIA Level 3 Transmit Multiple Cell Transfer Direct Mode

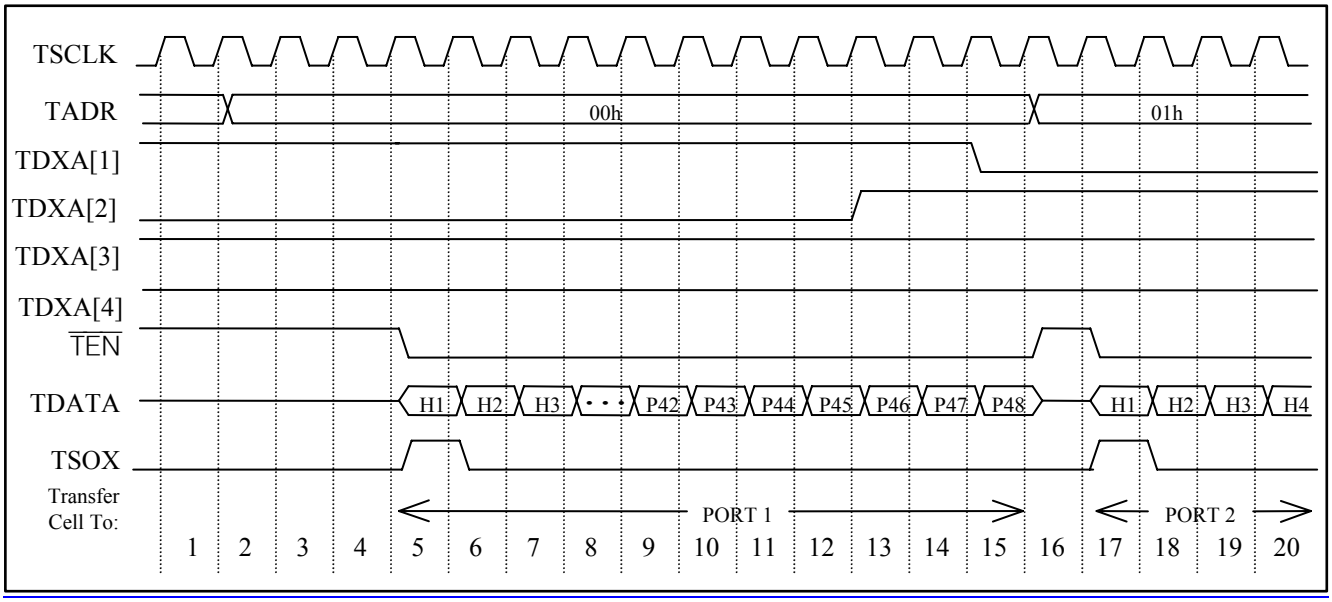


Figure 8-31 shows a multi-port transmit interface multiple cell transfer to different PHY devices. On clock edge 1, the ATM device polls PHY port 'N'. On clock edge 3, PHY port 'N' indicates to the ATM device that it can accept cell data by asserting TPXA. On clock edge 5, the ATM device selects PHY port 'N'. On clock edge 6, the ATM device starts a cell transfer to PHY port 'N' by asserting $\overline{TEN}$, placing the first byte of cell data on TDATA, and asserting TSOX to indicate the transfer of the first byte of the cell. On clock edge 7, the ATM device de-asserts TSOX as it continues to place additional bytes of the cell on TDATA. On clock edge 11, the ATM device polls PHY port 'M'. On clock edge 12, the ATM device polls PHY port 'N'. On clock edge 13, PHY port 'M' indicates that it can accept the transfer of a complete cell. On clock edge 14, PHY port 'N' indicates that it cannot accept the transfer of a complete cell. On clock edge 16, the ATM device deselects PHY port 'N' and selects PHY port 'M' by de-asserting $\overline{TEN}$ and placing PHY port 'M's address on TADR. On clock edge 17, the ATM device starts the transfer of a cell to PHY port 'M' by asserting $\overline{TEN}$, placing the first byte of cell data on TDATA, and asserting TSOX to indicate the transfer of the first byte of the cell. On clock edge 18, the ATM device de-asserts TSOX as it continues to place additional bytes of the cell on TDATA.

Figure 8-31. UTOPIA Level 3 Transmit Multiple Cell Transfer Polled Mode

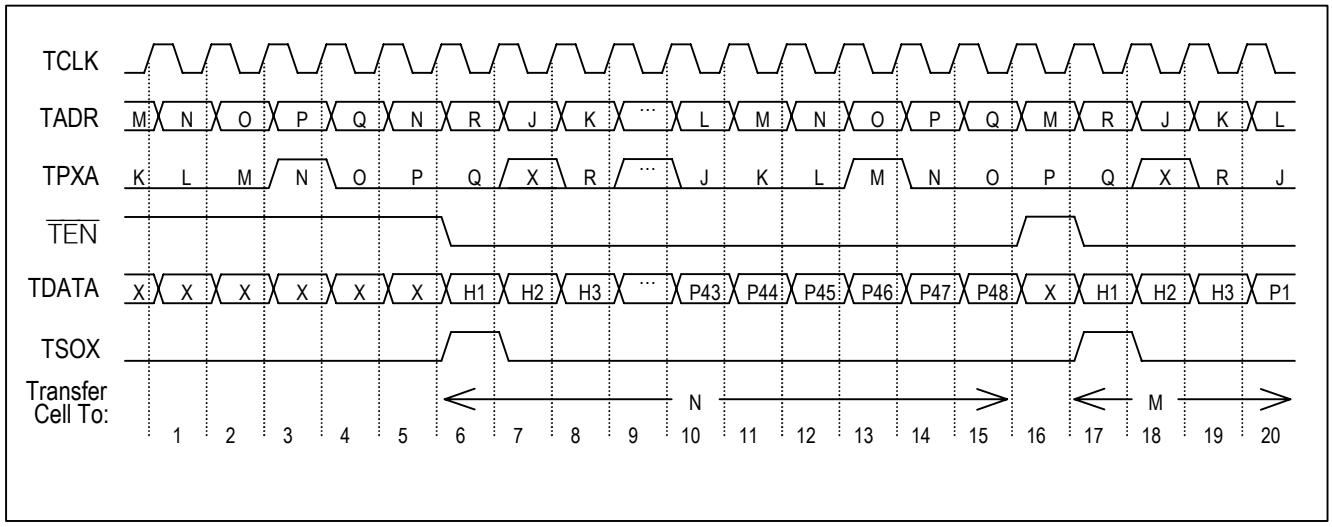


Figure 8-32 shows a multi-port receive interface multiple cell transfer from different PHY ports. On clock edge 3, PHY port 'N' indicates to the ATM device that it has a complete cell ready for transfer by asserting RPXA. On clock edge 5, the ATM device selects PHY port 'N'. On clock edge 6, the ATM device indicates to PHY port 'N' that it is ready to accept a complete cell transfer by asserting $\overline{REN}$. On clock edge 8, PHY port 'N' starts a cell transfer by placing the first byte of cell data on RDATA, and asserting RSOX to indicate the transfer of the first byte of the cell. On clock edge 9, PHY port 'N' de-asserts RSOX as it continues to place additional bytes of the cell on RDAT. On clock edge 11, the ATM device polls PHY device 'N'. On clock edge 12, PHY port 'M' indicates to the ATM device that it has a complete cell ready for transfer by asserting RPXA. On clock edge 12, PHY port 'N' indicates to the ATM device that it does not have a complete cell ready for transfer by de-asserting RPXA. On clock edge 15, the ATM device deselects PHY port 'N' and selects PHY port 'M' by de-asserting $\overline{REN}$ and placing PHY port 'M's address on RADR. On clock edge 16, the ATM device asserts $\overline{REN}$. On clock edge 17, PHY port 'N' stops transferring cell data. On clock edge 18, PHY port 'M' starts a cell transfer by placing the first byte of cell data on RDATA, and asserting RSOX to indicate the transfer of the first byte of the cell. On clock edge 19, PHY port 'M' de-asserts RSOX as it continues to place additional bytes of the cell on RDATA.

Figure 8-32: UTOPIA Level 3 Receive Multiple Cell Transfer Direct Mode

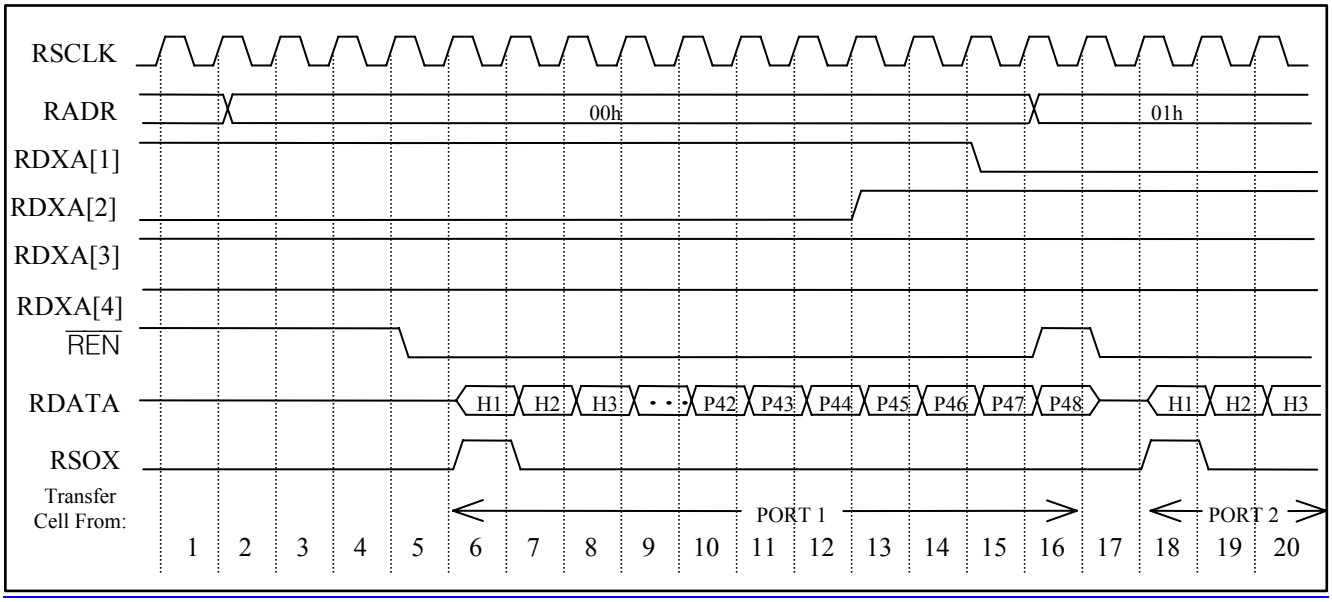
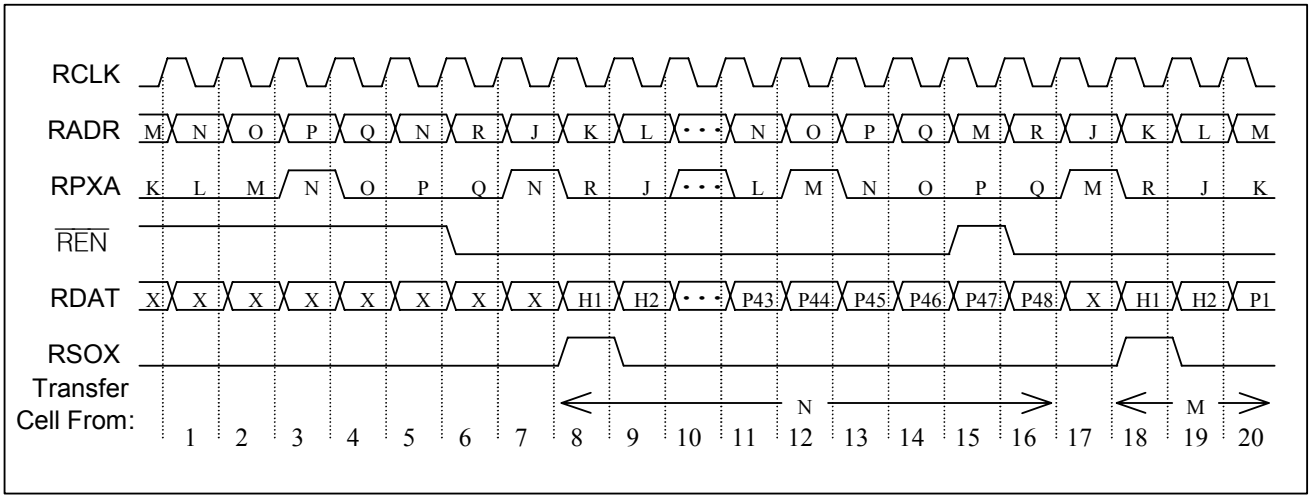


Figure 8-33 shows a multi-port receive interface multiple cell transfer from different PHY ports. On clock edge 1, the ATM device polls PHY port 'N'. On clock edge 3, PHY port 'N' indicates to the ATM device that it has a complete cell ready for transfer by asserting RPXA. On clock edge 5, the ATM device selects PHY port 'N'. On clock edge 6, the ATM device indicates to PHY port 'N' that it is ready to accept a complete cell transfer by asserting $\overline{REN}$. On clock edge 8, PHY port 'N' starts a cell transfer by placing the first byte of cell data on RDATA, and asserting RSOX to indicate the transfer of the first byte of the cell. On clock edge 9, PHY port 'N' de-asserts RSOX as it continues to place additional bytes of the cell on RDAT. On clock edge 11, the ATM device polls PHY device 'N'. On clock edge 12, PHY port 'M' indicates to the ATM device that it has a complete cell ready for transfer by asserting RPXA. On clock edge 12, PHY port 'N' indicates to the ATM device that it does not have a complete cell ready for transfer by de-asserting RPXA. On clock edge 15, the ATM device deselects PHY port 'N' and selects PHY port 'M' by de-asserting $\overline{REN}$ and placing PHY port 'M's address on RADR. On clock edge 16, the ATM device asserts $\overline{REN}$. On clock edge 17, PHY port 'N' stops transferring cell data. On clock edge 18, PHY port 'M' starts a cell transfer by placing the first byte of cell data on RDATA, and asserting RSOX to indicate the transfer of the first byte of the cell. On clock edge 19, PHY port 'M' de-asserts RSOX as it continues to place additional bytes of the cell on RDATA.

Figure 8-33. UTOPIA Level 3 Receive Multiple Cell Transfer Polled Mode



8.3.5.3 POS-PHY Level 2 Functional Timing

Figure 8-34 shows a multi-device transmit interface in byte transfer mode multiple packet transfer to different PHY ports. Prior to clock edge 1, the POS device started a packet transfer to PHY port '1'. On clock edge 2, PHY port '1' de-asserts its TDXA to indicate to the POS device that it cannot accept any more data transfers. On clock edge 3, the POS device stops the packet transfer to PHY port '1', and starts a packet transfer to PHY port '2' by leaving $\overline{TEN}$ asserted, placing PHY port '2's address on TADR, placing the first byte of packet data on TDATA, and asserting TSOX to indicate the transfer of the first byte of the packet. On clock edge 7, PHY port '2' de-asserts its TDXA to indicate to the POS device that it cannot accept any more data transfers. On clock edge 8, the POS device stops the packet transfer to PHY port '2', and resumes a packet transfer to PHY port '3'. On clock edge 12, PHY port '2' indicates to the POS device that it can accept a block of packet data by asserting its TDXA. Also, the POS device indicates it is transferring the last byte of packet data by asserting TEOP. On clock edge 13, the POS device ends the packet transfer to PHY port '3', and starts a packet transfer to PHY port '4'. On clock edge 15, PHY port '1' indicates to the POS device that it can accept a block of packet data. On clock edge 17, PHY port '4' de-asserts its TDXA to indicate to the POS device that it cannot accept any more data transfers. On clock edge 18, the POS device stops the packet transfer to PHY port '4', and resumes a packet transfer to PHY port '1'.

Figure 8-34. Transmit Multiple Packet Transfer to Different PHY ports (Direct Status Mode)

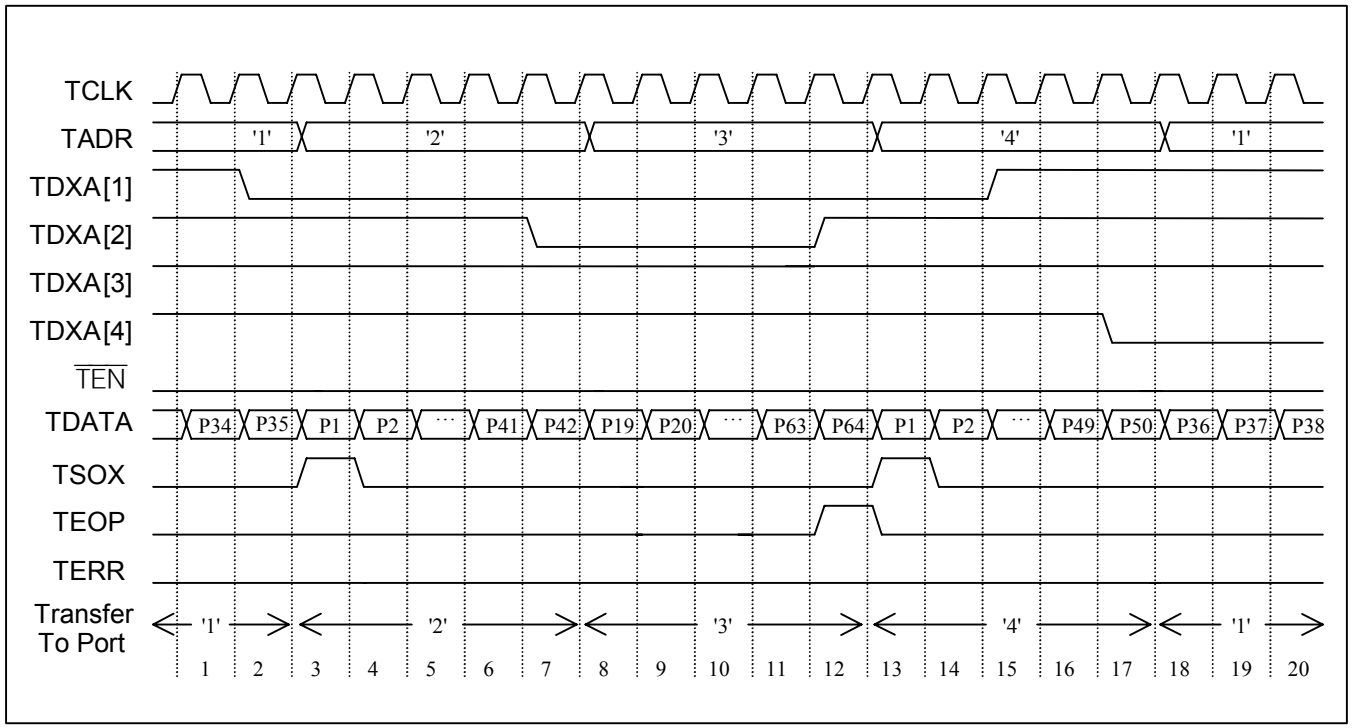


Figure 8-35 shows a multi-device receive interface in byte transfer mode multiple packet transfer from different PHY ports/devices. Prior to clock edge 1, a packet data transfer was initiated from PHY port '1', and PHY ports '2', '3', and '4' indicated to the POS device that they have a block of packet data or an end of packet ready for transfer by asserting their RDXA. On clock edge 2, the POS device indicates to PHY port '1' that it cannot accept any more data transfers by removing its address from RADR, and indicates to PHY port '2' that it is ready to accept a block of packet data by placing its address on RADR and leaving $\overline{REN}$ asserted. On clock edge 3, PHY port '1' stops transferring packet data, and PHY port '2' starts a packet transfer by leaving RVAL asserted, placing the first byte of the packet on RDATA, and asserting RSOX to indicate that this is the first transfer of the packet. On clock edge 4, PHY port '2' de-asserts RSOX as it leaves RVAL asserted and continues to place additional bytes of the packet on RDATA. On clock edge 8, the POS device de-asserts $\overline{REN}$ to indicate to PHY port '2' that it cannot accept any more data transfers. On clock edge 9, PHY port '2' ends the packet transfer process by de-asserting RVAL and tri-stating its RVAL, RDATA, RSOX, REOP, and RERR outputs. And, the POS device indicates to PHY port '3' that it is ready to accept a block of packet data by placing its address on RADR and reasserting $\overline{REN}$. On clock edge 10, PHY port '3' continues a packet transfer by asserting RVAL and placing the next byte of packet data on RDATA. On clock edge 14, PHY port '3' places the last byte of the packet on RDATA, and asserts REOP to indicate that this is the last transfer of the packet. On clock edge 15, PHY port '3' de-asserts RVAL and REOP ending the packet transfer process, as well as, de-asserting RDXA to indicate that it does not have another block of packet data or an end of packet ready for transfer. On clock edge 16, the POS device indicates to PHY port '4' that it is ready to accept a block of packet data by placing its address on RADR and leaving $\overline{REN}$ asserted. On clock edge 17, PHY port '4' starts a packet transfer by leaving RVAL asserted, placing the first byte of the packet on RDATA, and asserting RSOX to indicate that this is the first transfer of the packet. On clock edge 18, PHY port '4' de-asserts RSOX as it leaves RVAL asserted and continues to place additional bytes of the packet on RDATA.

Figure 8-35. POS-PHY Level 2 Receive Multiple Packet Transfer from Different PHY Ports/Devices (Direct Status Mode)

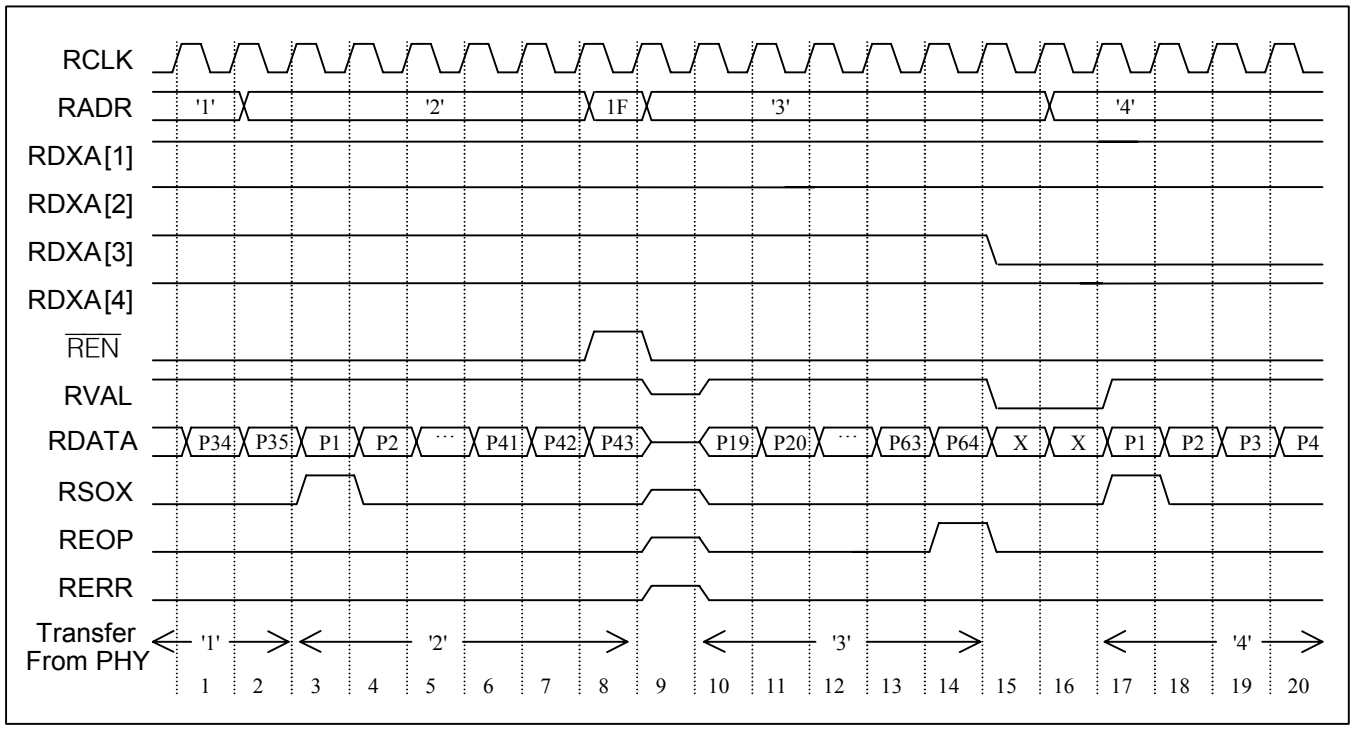


Figure 8-36 shows a multi-device transmit interface in packet transfer mode multiple packet transfer to different PHY ports. On clock edge 2, the POS device polls PHY port 'N'. On clock edge 3, PHY port 'N' indicates to the POS device that it can accept a block of packet data by asserting TPXA. On clock edge 4, the POS device selects PHY port 'N'. On clock edge 5, the POS device starts a packet transfer to PHY port 'N' by asserting $\overline{TEN}$, placing the first byte of packet data on TDATA, and asserting TSOX to indicate the transfer of the first byte of the packet. On clock edge 6, the POS device de-asserts TSOX as it continues to place additional bytes of the packet on TDATA. And, PHY port 'N' drives its TSPA output high. On clock edge 10, the POS device polls PHY port 'M'. On clock edge 11, the POS device asserts TEOP to indicate the transfer of the last byte of the packet to PHY port 'N' and PHY port 'M' indicates to the POS device that it can accept a block of packet data by asserting TPXA. On clock edge 12, the POS device de-asserts $\overline{TEN}$ to end the packet transfer process to PHY port 'N' and selects PHY port 'M'. On clock edge 13, the POS device starts a packet transfer to PHY port 'M' by asserting $\overline{TEN}$, placing the first byte of packet data on TDATA, and asserting TSOX to indicate the transfer of the first byte of the packet. And, PHY port 'N' tri-states its TSPA output. On clock edge 14, the POS device de-asserts TSOX as it continues to place additional bytes of the packet on TDATA. And, PHY port 'M' drives its TSPA output high.

Figure 8-36. POS-PHY Level 2 Transmit Multiple Packet Transfer to Different PHY Ports (Polled Status Mode)

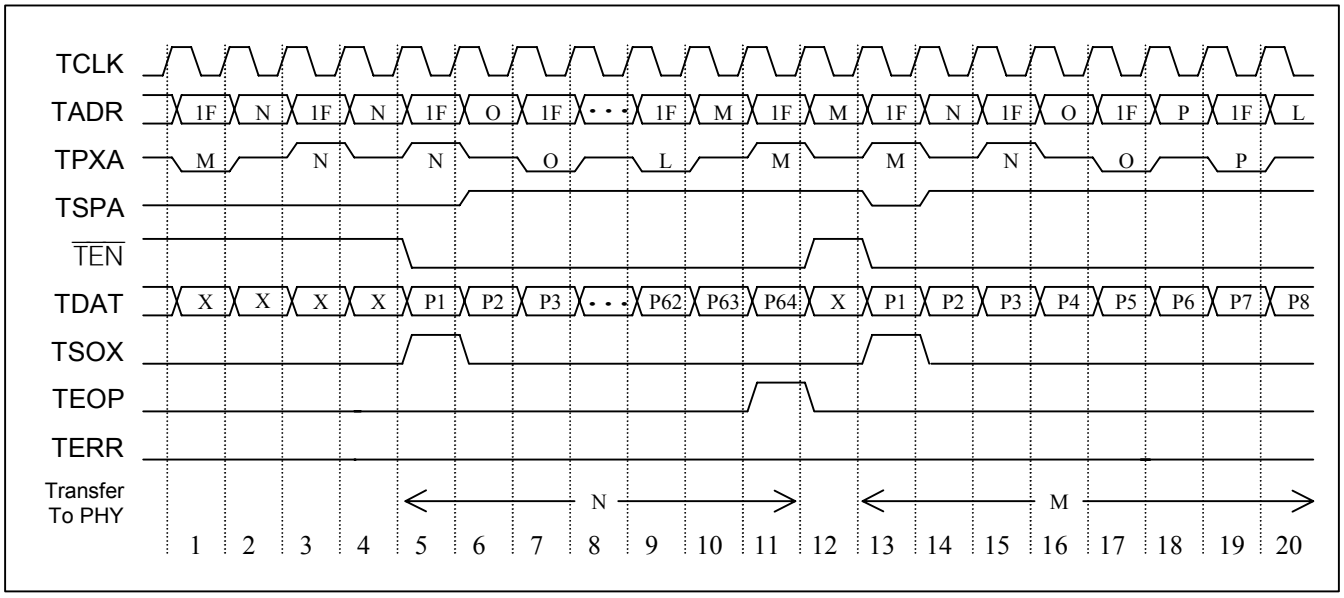
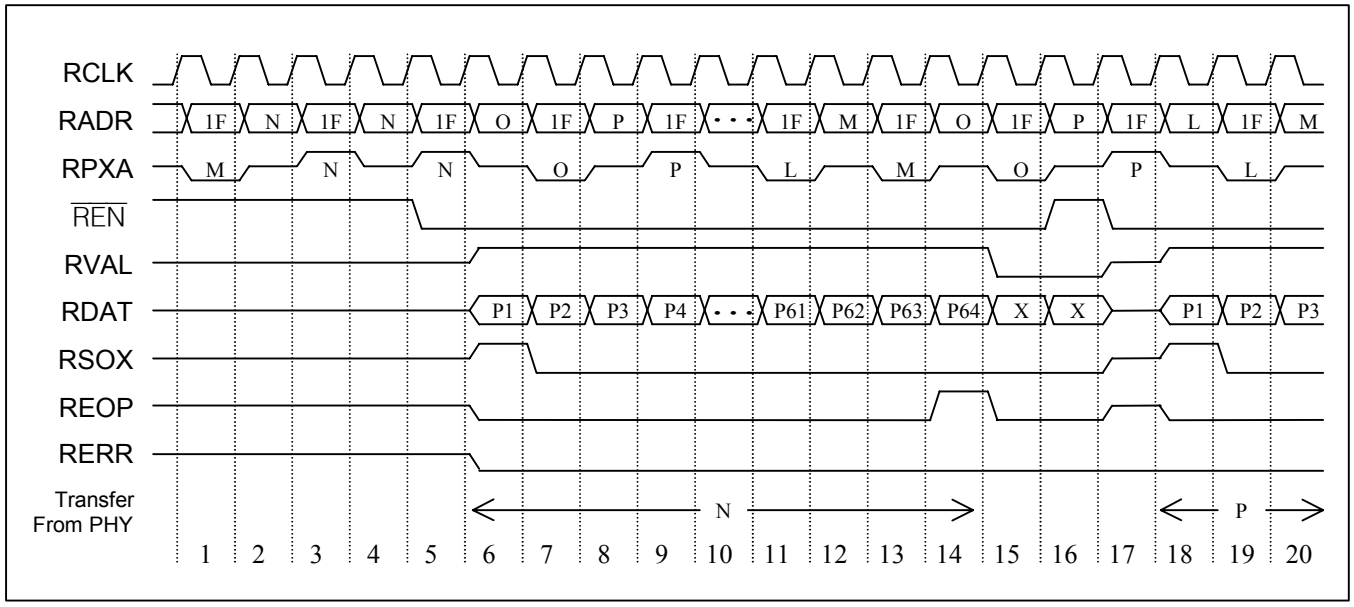


Figure 8-37 shows a multi-device receive interface in packet transfer mode multiple packet transfer. On clock edge 2, the POS device polls PHY port 'N'. On clock edge 3, PHY port 'N' indicates to the POS device that it has a block of packet data or an end of packet ready for transfer by asserting RPXA. On clock edge 4, the POS device selects PHY port 'N'. On clock edge 5, the POS device indicates to PHY port 'N' that it is ready to accept a block of packet data by placing its address on RADR and asserting $\overline{REN}$. On clock edge 6, PHY port 'N' starts packet transfer by asserting RVAL, placing the first byte of the packet on RDATA, and asserting RSOX to indicate that this is the first transfer of the packet. On clock edge 7, PHY port 'N' de-asserts RSOX as it leaves RVAL asserted and continues to place additional bytes of the packet on RDATA. On clock edge 14, PHY port 'N' places the last byte of the packet on RDATA, and asserts REOP to indicate that this is the last transfer of the packet. On clock edge 15, PHY port 'N' de-asserts RVAL and REOP ending the packet transfer process. On clock edge 16, the POS device de-asserts $\overline{REN}$ and selects PHY port 'P'. On clock edge 17, PHY port 'N' tri-states its RVAL, RDATA, RSOX, REOP, and RERR outputs and the POS device indicates to PHY port 'P' that it is ready to accept a block of packet data by placing its address on RADR and asserting $\overline{REN}$. On clock edge 18, PHY port 'P' starts packet transfer by asserting RVAL, placing the first byte of the packet on RDATA, and asserting RSOX to indicate that this is the first transfer of the packet. On clock edge 19, PHY port 'P' de-asserts RSOX as it leaves RVAL asserted and continues to place additional bytes of the packet on RDATA. While this example shows a different PHY port ('P') being selected for the next packet transfer, the timing is identical if the same PHY port ('N') is chosen for the next packet transfer.

Figure 8-37. POS-PHY Level 2 Receive Multiple Packet Transfer (Polled Status Mode)



8.3.5.4 POS-PHY Level 3 Functional Timing

Figure 8-38 shows a multi-port transmit interface multiple packet transfer to different PHY ports. On clock edge 1, PHY port 'N' indicates to the POS device that it can accept a block of packet data by asserting TPXA. On clock edge 3, the POS device selects PHY port 'N' by placing its address on TDATA and asserting TSX while $\overline{TEN}$ is de-asserted. On clock edge 4, the POS device starts a packet transfer to PHY port 'N' by de-asserting TSX, asserting $\overline{TEN}$, placing the first byte of packet data on TDATA, and asserting TSOX to indicate the transfer of the first byte of the packet. On clock edge 5, the POS device de-asserts TSOX as it continues to place additional bytes of the packet on TDATA and PHY port 'N' asserts TSPA. On clock edge 11, the POS device polls PHY port 'L'. On clock edge 12, PHY port 'N' indicates that it cannot accept any more data transfers by de-asserting TSPA. On clock edge 13, PHY port 'L' indicates to the POS device that it can accept a block of packet data by asserting TPXA. On clock edge 14, the POS device de-asserts $\overline{TEN}$ to end the packet transfer process to PHY port 'N' and selects PHY port 'L' by placing its address on TDATA and asserting TSX while $\overline{TEN}$ is de-asserted. On clock edge 15, the POS device starts a packet transfer to PHY port 'L' by asserting $\overline{TEN}$, de-asserting TSX, placing the first byte of packet data on TDATA, and asserting TSOX to indicate the transfer of the first byte of the packet. On clock edge 16, the POS device de-asserts TSOX as it continues to place additional bytes of the packet on TDATA and PHY port 'L' asserts TSPA.

Figure 8-38. POS-PHY Level 3 Transmit Multiple Packet Transfer In-Band Addressing

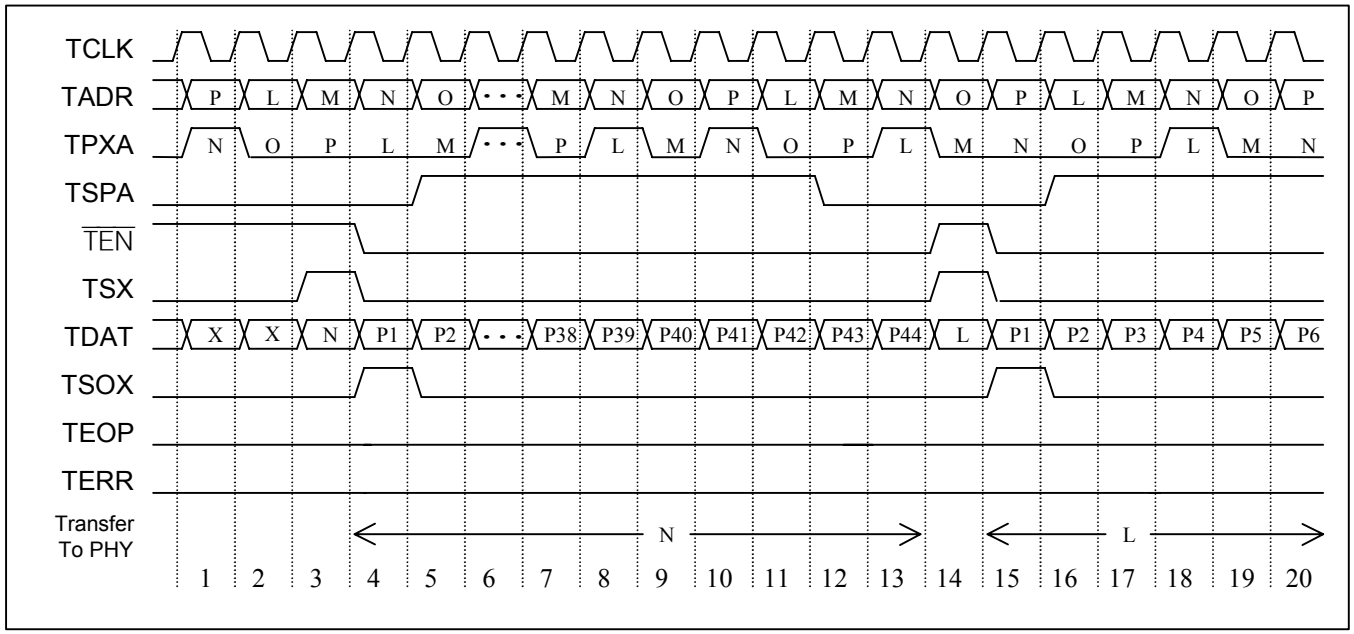
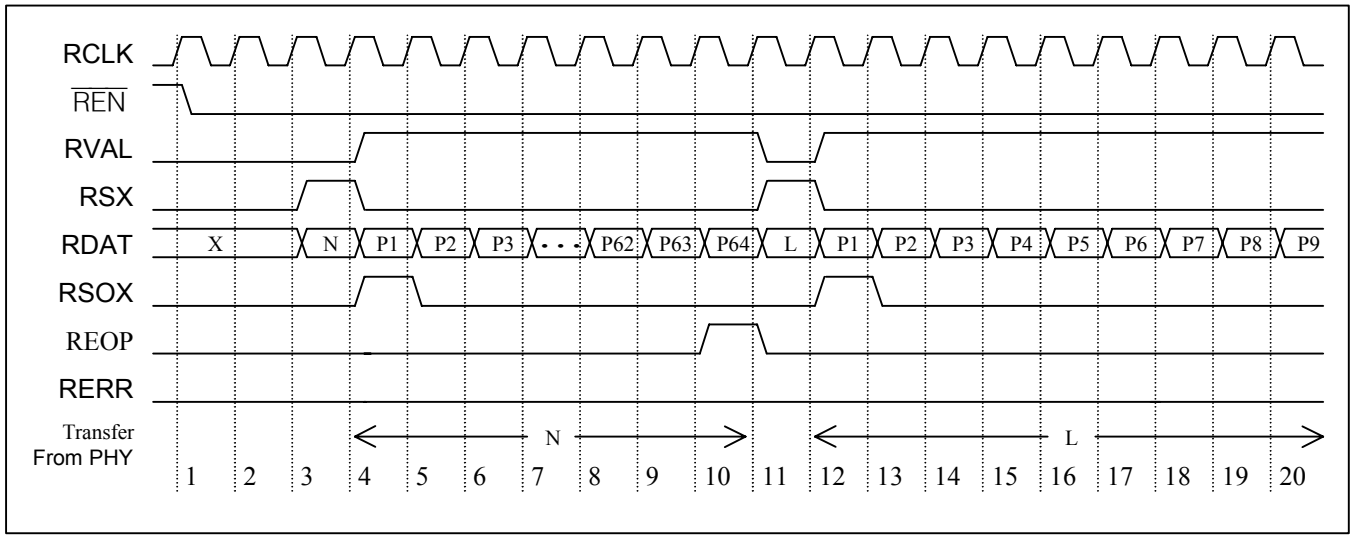


Figure 8-39 shows a multi-port receive interface multiple packet transfer from different ports. On clock edge 1, the POS device indicates to PHY port 'N' that it is ready to accept a block of packet data by asserting $\overline{REN}$. On clock edge 3, the PHY device selects port 'N' for transfer by asserting RSX and placing its address on RDATA. On clock edge 4, PHY port 'N' starts packet transfer by de-asserting RSX, asserting RVAL, placing the first byte of the packet on RDATA, and asserting RSOX to indicate that this is the first transfer of the packet. On clock edge 5, PHY port 'N' de-asserts RSOX as it leaves RVAL asserted and continues to place additional bytes of the packet on RDATA. On clock edge 10, PHY port 'N' places the last byte of the packet on RDATA, and asserts REOP to indicate that this is the last transfer of the packet. On clock edge 11, the PHY device de-asserts RVAL and REOP ending the packet transfer process from port 'N' and selects PHY port 'L' for transfer by asserting RSX and placing its address on RDATA. On clock edge 12, PHY port 'L' starts packet transfer by de-asserting RSX, asserting RVAL, placing the first byte of the packet on RDATA, and asserting RSOX to indicate that this is the first transfer of the packet. On clock edge 13, PHY port 'L' de-asserts RSOX as it leaves RVAL asserted and continues to place additional bytes of the packet on RDATA.

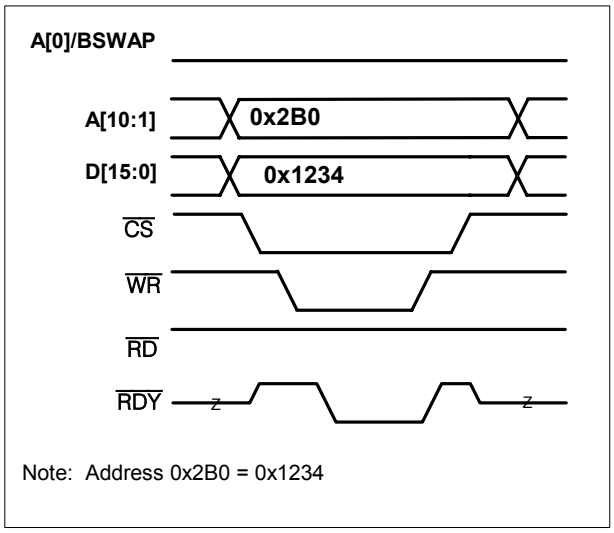
Figure 8-39. POS-PHY Level 3 Receive Multiple Packet Transfer In-Band Addressing



8.3.6 Microprocessor Interface Functional Timing

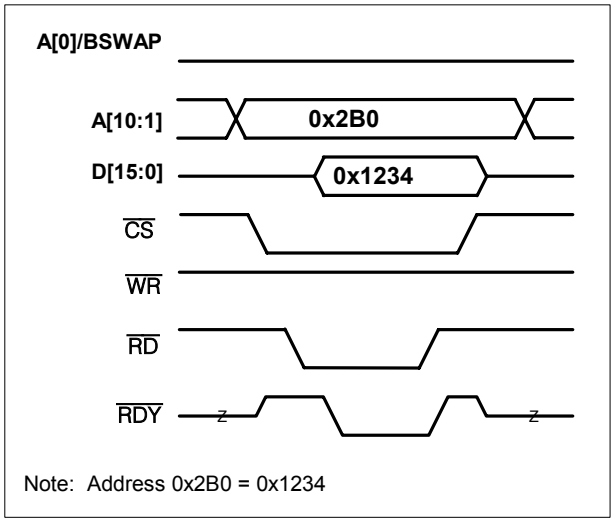
Figure 8-40 and Figure 8-42 show examples of a 16-bit databus and an 8-bit databus, respectively. In 16-bit mode, the A[0]/BSWAP signal controls whether or not to byte swap. In 8-bit mode, the A[0]/BSWAP signal is used as the LSB of the address bus (A[0]). The selection of databus size is determined by the WIDTH input signal. See also Section 10.1.1.

Figure 8-40. 16-Bit Mode Write



Note: Address 0x2B0 = 0x1234

Figure 8-41. 16-Bit Mode Read



Note: Address 0x2B0 = 0x1234

Figure 8-42. 8-Bit Mode Write

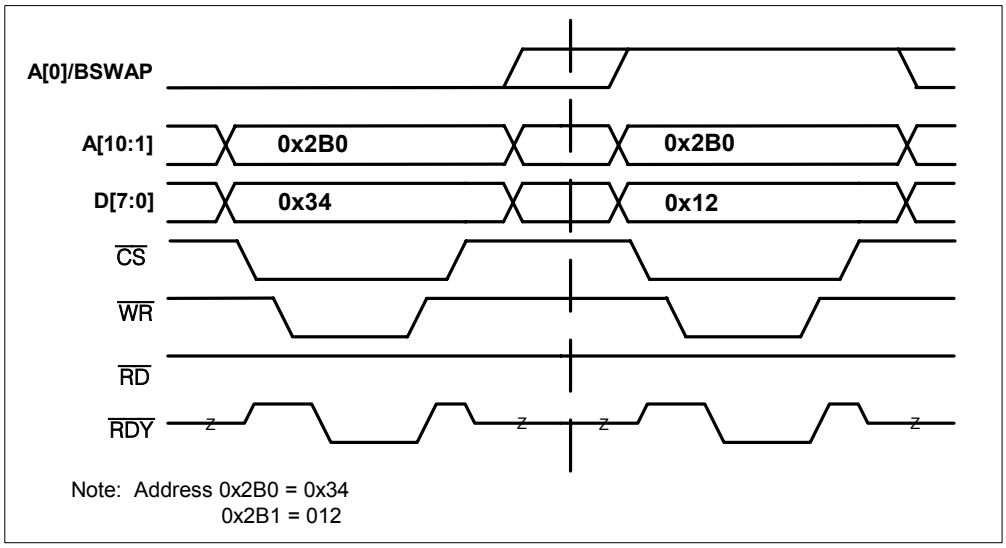


Figure 8-43. 8-Bit Mode Read

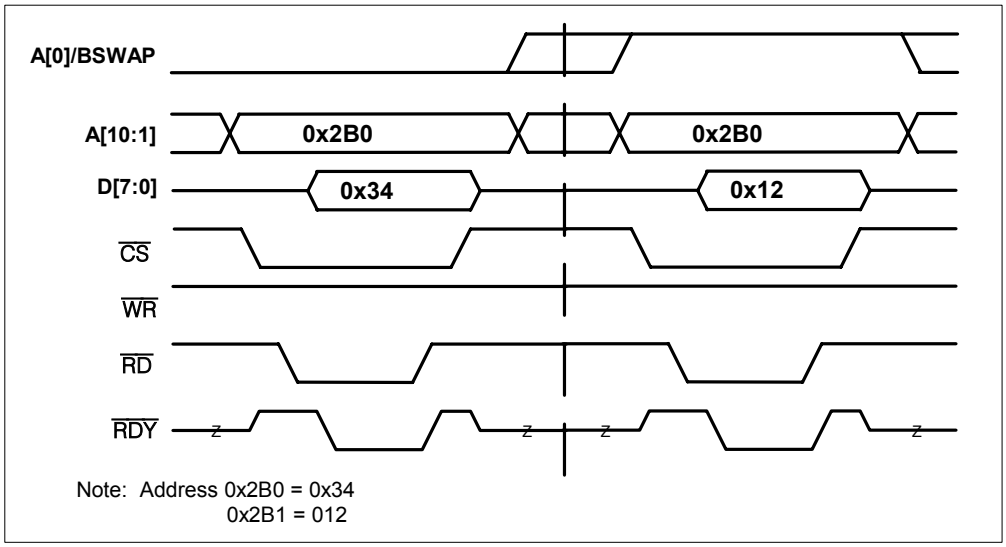


Figure 8-44 and Figure 8-45 are examples of databuses without and with byte swapping enabled, respectively. When the A[0]/BSWAP pin is set to 0, byte swapping is disabled, and when one, byte swapping is enabled. This pin should be static and not change while operating. Note: Address bit A[0] is not used in 16-bit mode. See also Section 10.1.2.

Figure 8-44. 16-Bit Mode without Byte Swap

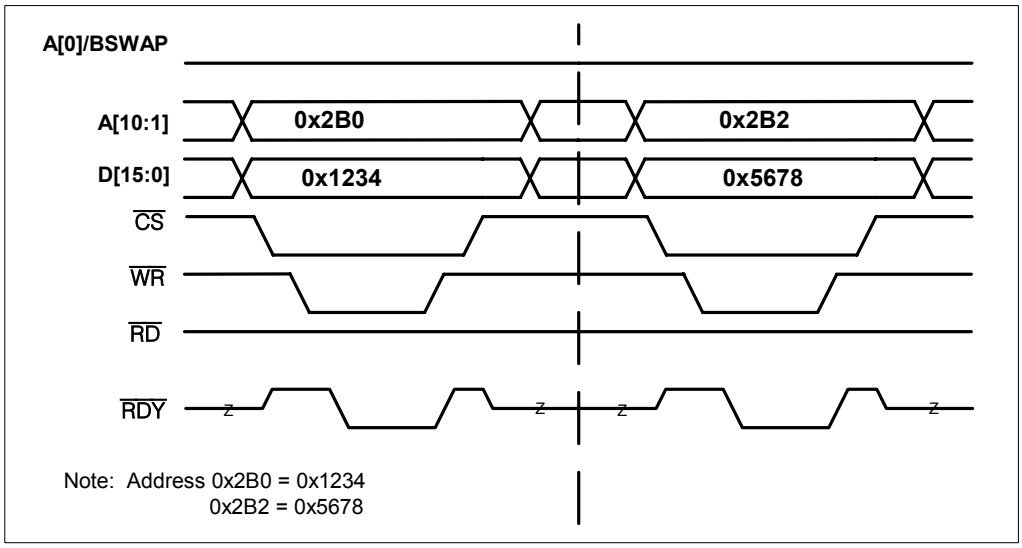
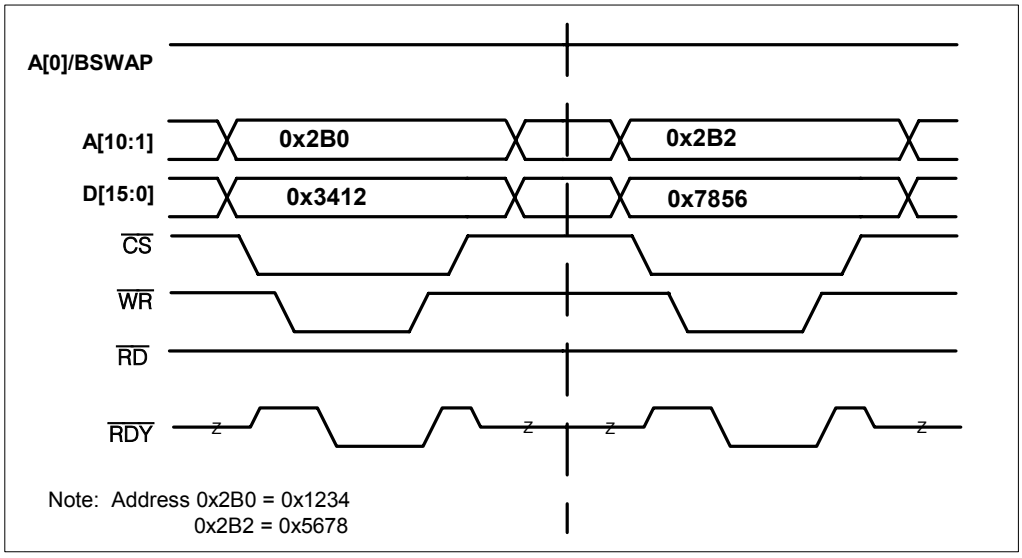


Figure 8-45. 16-Bit Mode with Byte Swap



Clearing status latched registers on a read or write access is selectable via the GL.CR1.LSBCRE register bit. Clearing on read clears all bits in the register, while the clear on write clears only those bits which are written with a '1' when the user writes to the status latched register.

To use the Clear on Read method, the user must only read the status latched register. All bits are set to zero after the read. Figure 8-46 shows a read of a status latched register and another read of the same register verifying the register has cleared.

To use the Clear on Write method, the user must write the register with ones in the bit locations that he desires to clear. Figure 8-47 shows a read, a write, and then a subsequent read revealing the results of clearing of the bits which he wrote a '1'. See also Section 10.1.5.

Figure 8-46. Clear Status Latched Register on Read

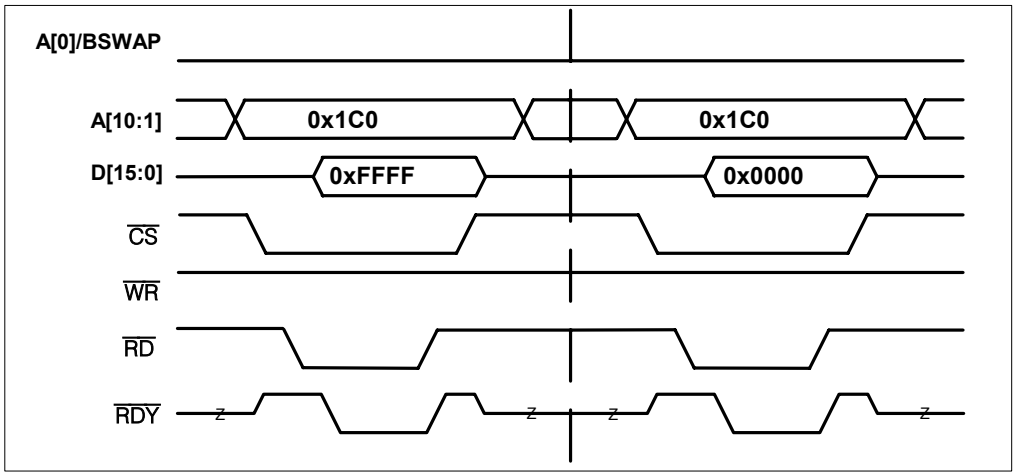


Figure 8-47. Clear Status Latched Register on Write

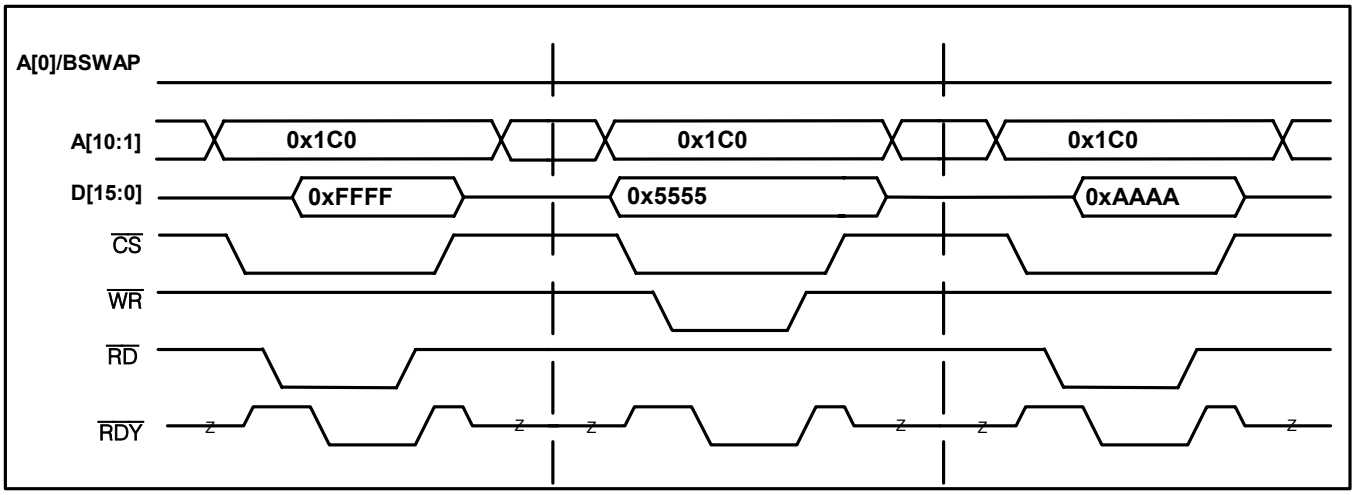


Figure 8-48 and Figure 8-49 show exaggerated views of the Ready Signal to describe the difference in access times to write or read to or from various memory locations on the DS316x device. Some registers will have a faster access time than others will and if needed, the user can implement the RDY signal to maximize efficiency of read and write accesses.

Figure 8-48. RDY Signal Functional Timing Writes

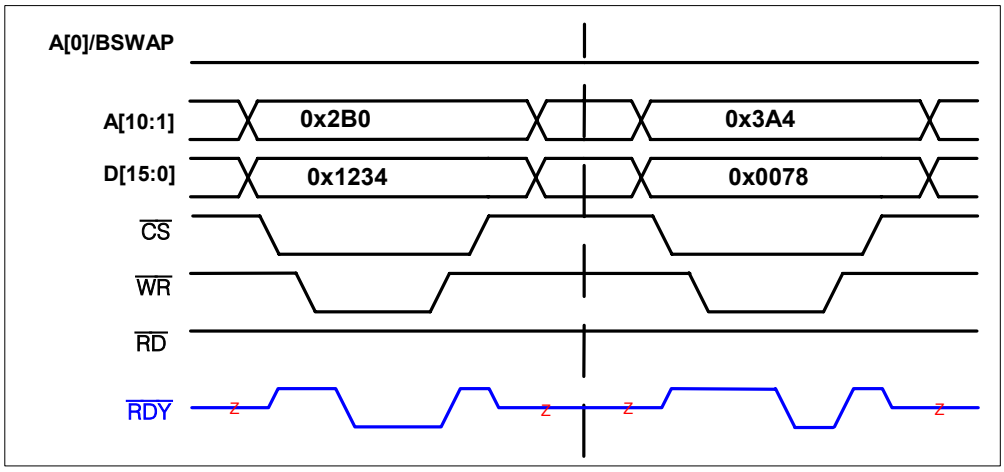
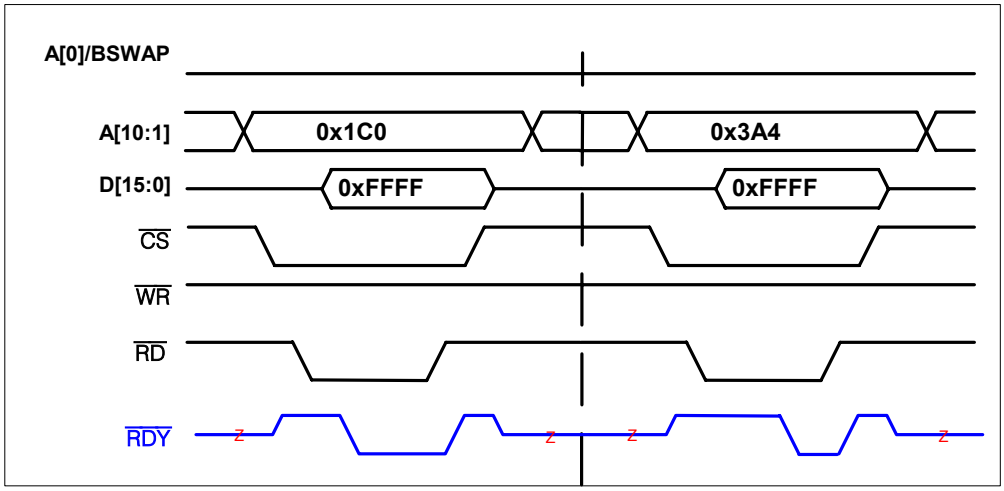


Figure 8-49. RDY Signal Functional Timing Read



See also Figure 18-7 and Figure 18-8.

8.3.7 JTAG Functional Timing

See Section 13.5.

9 INITIALIZATION AND CONFIGURATION

STEP 1: Check Device ID Code:

Before any testing can be done, device ID code, which is stored in GL.IDR, shoud be checked against device ID codes shown below to ensure correct device is being used.

Current device ID codes are:

- **DS3161 rev 1.0: 0x40h**
- **DS3162 rev 1.0: 0x41h**
- **DS3163 rev 1.0: 0x42h**
- **DS3164 rev 1.0: 0x43h**

STEP 2: Initialize the Device.

Before configuring for operation, make sure the device is in a known condition with all registers set to their default value by initiating a Global Reset. (See Section 10.3) A Global Reset can be initiated via the RST pin or by the Global Reset bit (*GL.CR1*.RST). A Port Reset is not necessary since the global reset includes a reset of all ports to their default values.

STEP 3: Clear the Reset.

It is necessary to clear the RST bit to begin normal operation.

After clearing the RST bit, the device is configured for default mode.

Default mode:

System Interface: UTOPIA Level 2, 8-bit databus
Framer: C-bit DS3

STEP 4: Clear the Data Path Resets and the Port Power-Down bit.

The default value of the Data Path Resets is one, which keeps the internal logic in the reset status. The user needs to clear the following bits:

GL.CR1.RSTDP = 0
PORT.CR1.RSTDP = 0
PORT.CR1.PD = 0

STEP 5: Select the clock source.

Loop Time (use the receive clock (RLCLKn)): Set PORT.CR3.LOOPT = 1
CLAD Source: Set PORT.CR3.CLADC = 0
TCLKI Source: Set PORT.CR3.CLADC = 1
If using the CLAD, properly configure the CLAD by setting the CLAD bits in GL.CR2.

STEP 6: Configure the Framing Mode and the Line Mode.

PORT.CR2.LM = 0 (AMI/B3ZS/HDB3 Interface) or another setting. See Table 10-31
PORT.CR2.FM[5:0] set to the correct framing mode. See Table 10-30.

STEP 7: Disable Payload AIS (downstream AIS) and Line AIS

PORT.CR1.PAIS[2:0] = 111
PORT.CR1.LAIS[1:0] = 11

STEP 8: Initialize and configure the FIFOs.

Reset the Transmit and Receive FIFO. *FF.TCR*.TFRST = 1. *FF.RCR*.RFRST = 1.
Clear the FIFO Reset bits. *FF.TCR*.TFRST = 0. *FF.RCR*.RFRST = 0.
Set the FIFO Transmit Level Control Register and the FIFO Transmit Port Address Control Register.
Set the FIFO Receive Level Control Register and the FIFO Receive Port Address Control Register.
The Port Address needs to be configured to match the master controller address for each port.

STEP 9: Configure the System Bus

Configure for bus size and for interface type. See Table 9-1.
Optionally, set the System Interface Transmit Control Register, System Interface Receive Control Register #1 and #2 to fine tune for the specific application.
(User may leave registers at default value.)

STEP 11: Configure the Cell or Packet Processor

For cell mode, the default is to send the cell across the system interface without the HEC. Also, default mode scrambles the cell data to the line.
To attach the HEC to the cell, set *SI.TCR*.THECT = 1 and *SI.RCR*.RHECT = 1.

STEP 12: Enable each port

PORT.CR2.TLEN = 1

Table 9-1. Configuration of Global Register Settings

Note: This table assumes a DS3 clock input on the CLKA pin.

MODE	GL.CR1 0x002	GL.CR2 0x004	GL.GIOCR 0x00A
UTOPIA L2	0000 XX00 0000 0000	0x0204	0x0000
UTOPIA L3	0000 XX01 0000 0000	0x0204	0x0000
POS-PHY L2	0000 XX10 0000 0000	0x0204	0x0000
POS-PHY L3 or SPI-3	0000 XX11 0000 0000	0x0204	0x0000
8-bit System Bus	0000 00XX 0000 0000	0x0204	0x0000
16-bit System Bus	0000 01XX 0000 0000	0x0204	0x0000
32-bit System Bus	0000 10XX 0000 0000	0x0204	0x0000

Table 9-2. Configuration of Port Register Settings

Note: The Line Mode has been configured for B3ZS/HDB3 for all modes except OHM mode. Only Port 1 registers have been displayed.

MODE	PORT.CR1 0x040	PORT.CR2 0x042	PORT.CR3 0x044	PORT.CR4 0x046
DS3 C-Bit	0x7C00	0000 0011 0000 000X	0x0000	0x0000
DS3 C-Bit PLCP	0x7C00	0000 0011 0000 010X	0x0000	0x0000
DS3 M23	0x7C00	0000 0011 0000 100X	0x0000	0x0000
DS3 M23 PLCP	0x7C00	0000 0011 0000 110X	0x0000	0x0000
E3.751	0x7C00	0000 0011 0001 000X	0x0000	0x0000
E3.751 PLCP	0x7C00	0000 0011 0001 010X	0x0000	0x0000
E3.823	0x7C00	0000 0011 0001 100X	0x0000	0x0000
OHM Mode (DS3/E3/Clear Channel)	0x7C00	1100 0XXX 00XX XXXX	0x0000	0x0000

Considerations

Select the HDLC Controller connection. The default setting connects it to the DS3/E3 Framers. Setting PORT.CR1.HDSEL = 1 connects the HDLC Controller to the PLCP framers.

In POS-PHY mode, to select cell processing rather than packet processing, set PORT.CR2.PMCPE = 1.

9.1 Monitoring and Debugging

To determine if the device is receiving a good signal and that the chip is correctly configured for its environment, check the following status registers.

Loss of Signal – LINE.RSR.LOS – This indicates that the receiver is receiving all zeros.

Loss of Frame – T3.RSR1.LOF (or E3751.RSR1 or E3832.RSR1) – This indicates that the framer was unable to synchronize to the incoming data. Verify that the FM bits have been correctly configured for the correct mode of traffic (DS3, E3 G.751, E3 G.832)

Other helpful techniques to utilize in diagnosing a problem include using Line Loopback and Diagnostic Loopback. These features help to isolate and identify the source of the problem. Line Loopback will loop the receive input to the transmit output, eliminating the transmit side input from the equation. Diagnostic Loopback will loop the transmit output before the line interface to the receive framer.

One other potential problem is the Line Encoding/Decoding. The device needs to be configured in the same mode as the far end piece of equipment. If the far end piece of equipment is transmitting and receiving HDB3/B3ZS encoded data, the DS316x also must be configured to do the same. This is controlled by the *LINE.TCR*.TZSD and the *LINE.RCR*.RZSD bits.

9.1.1 Cell/Packet FIFO

Check the status registers of the FIFO block. Common indicators to check would be the Transmit Underflow, Transmit Overflow, and Receive Overflow status bits. These status bits are located in the FIFO.TSRL Register and the FIFO.RSRL Register.

A Transmit Underflow indicates that the transmit cell processor or packet processor has attempted a read while the FIFO was empty.

A Transmit Overflow indicates that either a start of cell or a start of packet or a short packet was received when the FIFO was full. Additionally, if additional packet data is received when the FIFO is already full, it will result in an abort status for the current packet and the Transmit Overflow being declared.

A Receive Overflow occurs when cell data is received while the FIFO is full. In a packet system, the overflow will be declared when a start of packet or a short packet is received or packet data is received when the FIFO is full resulting in an abort status for the current packet and the Receive Overflow being declared.

9.1.2 Cell Processor

Monitoring the Loss of Cell Delineation in the Cell Processor is recommended to insure proper operation. The LCD status bit is located in the CP.RSR Register and indicates when an Out of Cell Delineation persists for a programmed number of cells (set in the CP.RLTC Register).

9.1.3 Packet Processor

Monitoring the number of errored packets in the Packet Processor is recommended for proper operation. The REPC status bit is located in the PP.RSR Register and indicates when the errored packet count is not zero. An errored packet is detected when an errored FCS is detected. To determine how many errored packets have been received, the FCS Errored Packet Count Registers must first be updated via the PMU signal.

10 FUNCTIONAL DESCRIPTION

10.1 Processor Bus Interface

10.1.1 8/16-Bit Bus Widths

The external processor bus can be sized for 8 or 16 bits using the WIDTH pin. When in 8-bit mode (WIDTH=0), the address is composed of all the address bits including A[0], the lower 8 data lines D[7:0] are used and the upper 8 data lines D[15:8] are not used and never driven during a read cycle. When in 16-bit mode (WIDTH=1), the address bus does not include A[0] (the LSB of the address bus is not routed to the chip) and all 16 data lines D[15:0] are used. See Figure 8-40 and Figure 8-42 for functional timing diagrams.

10.1.2 Ready Signal ($\overline{RDY}$)

The $\overline{RDY}$ signal allows the microprocessor to use the minimum bus cycle period for maximum efficiency. When this signal goes low, the $\overline{RD}$ or $\overline{WR}$ cycle can be terminated. See Figure 8-48 for functional timing diagrams.

Note: The $\overline{RDY}$ signal will not go active if the user attempts to read or write unused ports or unused registers not assigned to any design blocks. The $\overline{RDY}$ signal will go active if the user writes or reads reserved registers or unused registers within design blocks.

10.1.3 Byte Swap Modes

The processor interface can operate in byte swap mode when the data bus is configured for 16-bit operation. The A[0]/BSWAP pin is used to determine whether byte swapping is enabled. This pin should be static and not change while operating. When the A[0]/BSWAP pin is low the upper register bits REG[15:8] are mapped to the upper external data bus lines D[15:8], and the lower register bits REG[7:0] are mapped to the lower external data bus lines D[7:0]. When the A[0]/BSWAP pin is high the upper register bits REG[15:8] are mapped to the lower external data bus lines D[7:0], and the lower register bits REG[7:0] are mapped to the upper external data bus lines D[15:8]. See Figure 8-44 and Figure 8-45 for functional timing diagrams.

10.1.4 Read-Write/Data Strobe Modes

The processor interface can operate in either read-write strobe mode or data strobe mode. When MODE=0 the read-write strobe mode is enabled and a negative pulse on $\overline{RD}$ performs a read cycle, and a negative pulse on $\overline{WR}$ performs a write cycle. When MODE=1 the data strobe mode is enabled and a negative pulse on $\overline{DS}$ when R/$\overline{W}$ is high performs a read cycle, and a negative pulse on $\overline{DS}$ when R/$\overline{W}$ is low performs a write cycle. The read-write strobe mode is commonly called the “Intel” mode, and the data strobe mode is commonly called the “Motorola” mode.

10.1.5 Clear on Read/Clear on Write Modes

The latched status register bits can be programmed to clear on a read access or clear on a write access. The global control register bit *GL.CR1*.LSBCRE controls the mode that all of the latched registers are cleared. When LSBCRE=0, the latched register bits will be cleared when the register is written to and the write data has the register bits to clear set. When LSBCRE=1, the latched register bits that are set will be cleared when the register is read.

The clear on write mode expects the user to use the following protocol:

1. Read the latched status register
2. Write to the registers with the bits set that need to be cleared.

This protocol is useful when multiple uncoordinated software tasks access the same latched register. Each task should only clear the bits with which it is concerned; the other tasks will clear the bits with which they are concerned.

The clear on read mode is simpler since the bits that were read as being set will be cleared automatically. This method will work well in a software system where multiple tasks do not read the same latched status register. The latched status register bits in clear on read mode are carefully designed not to miss events that occur while a register is being read when the latched bit has not already been set. Refer to Figure 8-46 and Figure 8-47.

10.1.6 Global Write Method

All of the ports can be written to simultaneously using the global write method. This method is enabled by setting the GL.CR1.GWM bit. When the global write method is enabled, a write to a register on any valid port will write to the same register on all valid ports. A valid port is a port that is available in a particular packaged part. For example, port four would not be valid in a DS3163 device. After reset, the global write method is not enabled.

When the GWM bit is set, read data from the port registers is not valid and read data from the global and test registers is valid. The data value read back from a port register should be ignored.

10.1.7 Interrupt and Pin Modes

The interrupt ($\overline{INT}$) pin is configurable to drive high or float when not active. The GL.CR1.INTM bit controls the pin configuration, when it is set the $\overline{INT}$ pin will drive high when not active. After reset, the $\overline{INT}$ pin will be in high-impedance mode until an interrupt source is active and enabled to drive the interrupt pin.

10.1.8 Interrupt Structure

The interrupt structure is designed to efficiently guide the user to the source of an enabled interrupt source. The status bits in the global status (*GL.SR*) and global status latched register (*GL.SRL*) are read to determine if the interrupt source is a global event like the UTOPIA/POS-PHY interface, global performance monitor update or whether it came from one of the ports. If the interrupt event came from one of the ports then the port status register (*PORT.SR*) and port status register latched (*PORT.SRL*) can be read to determine if the interrupt source is a common port event like the performance monitor update or whether it came from one of the DS3/E3 Framers, PLCP Framer, ATM/PKT, BERT, HDLC, FEAC or Trail Trace status registers. If the interrupt came from one of the DS3/E3 Framers, PLCP Framer, ATM/PKT, BERT, HDLC, FEAC or Trail Trace status registers, then one of those registers will need to be read to determine the event that caused the interrupt.

The source of an interrupt can be determined by reading three status registers: global, port and block status registers.

When a mode is not enabled, then interrupts from that source will not occur. For example, if PLCP framing is not enabled then the potential interrupts from the latched status register in the PLCP block cannot occur. Similarly, if E3 framing mode is enabled, an interrupt source that is defined in DS3 framing, but not in E3 framing, cannot create a new interrupt. Note that when modes are changed, the latched status bits of the new mode, as well as any other mode, may get set. If the data path reset is set during or after the mode change, the latched status bits will be automatically cleared. If the data path reset is not used to clear the latched status bits, then the registers must be cleared by reading or writing to them based on the register clear method selected.

Figure 10-1. Interrupt Structure

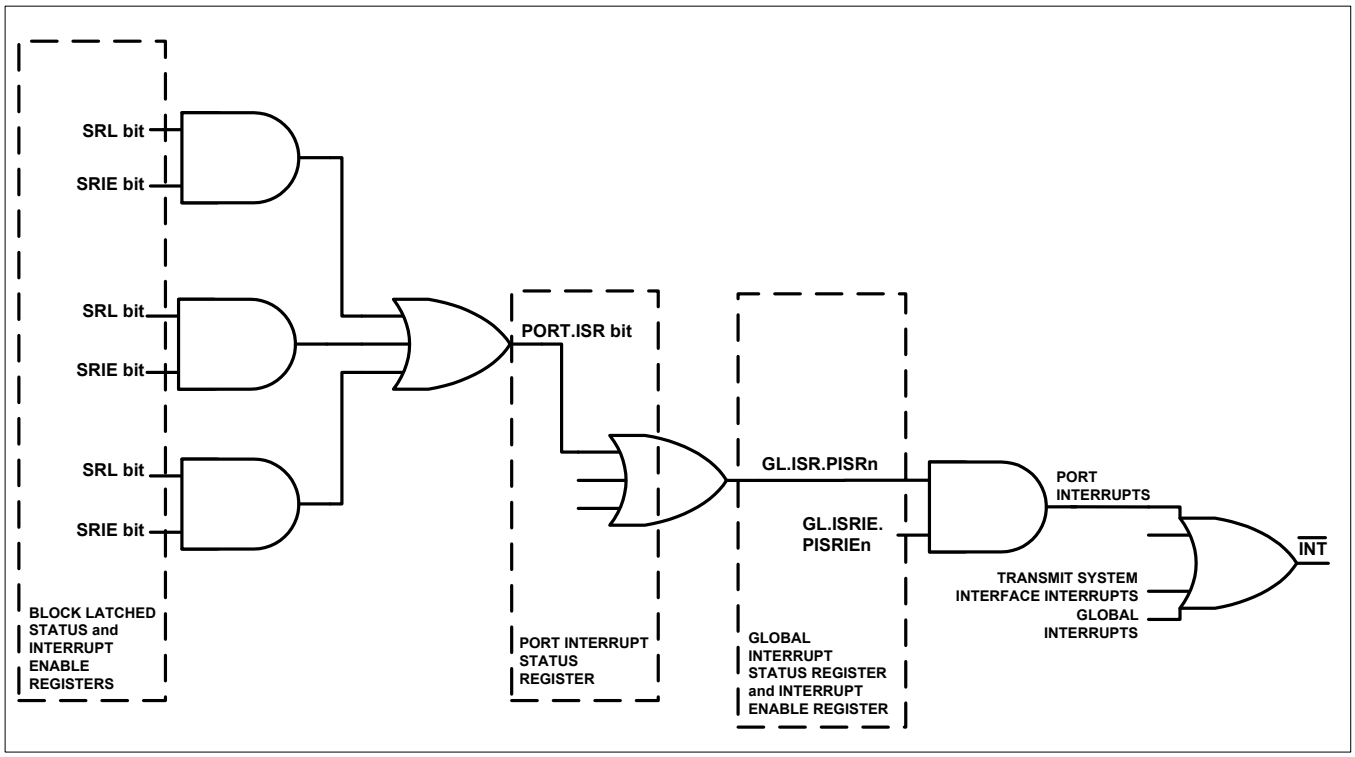


Figure 10-1 not only tells the user how to determine which event caused the interrupt, it also tells the user how to enable a particular interrupt. Each block has a Status Register Interrupt Enable register that must be set in order to enable an interrupt. The next step is to unmask the interrupt at the port level, on a per port basis. This is controlled in the Global Interrupt Status Register Interrupt Enable register (GL.ISRIE). Now the device is ready to drive the INT pin low when a particular status bit gets set.

For example, in order to enable DS3 Out of Frame interrupts on Port 2, the following registers would need to be written:

Register Bit	Address	Value Written	Note
T3.RSRIE1.OOFIE	0x32C	0x0002	Unmask OOF interrupt on Port 2
GL.ISRIE.PISRIE2	0x012	0x0020	Unmask Port 2 interrupts

The following status registers bits will be set upon reception of OOF on Port 2:

Register Bit	Address	Value Read	Note
T3.RSRL1.OOFL	0x328	0x0002	DS3 Out of Frame on Port 2
PORT.ISR.FMSR	0x250	0x0001	Framer Block Interrupt Active, Port 2
GL.ISR.PISR2	0x010	0x0020	Port 2 Interrupt Active

10.2 Clocks

10.2.1 Line Clock Modes

The system loopback (SLB) function does not affect the line clocks in any way.

10.2.1.1 Loop Timing

When loop timing is enabled (PORT.CR3.LOOPT), the transmit clock source is the same as the receive clock source. The TCLKIn pins are not used as a clock source. Because loop timing is enabled, the loopback functions (LLB, PLB, and DLB) do not cause the clock sources to switch when they are activated. The transmit and receive signal pins can be timed to a single clock reference without concern about having the clock source change during loopbacks.

10.2.1.1.1 Loop Timing Enabled

In this mode, the RLCLKn pins are the source of the clock for both the receive and transmit logic. The RCLKOn, TCLKOn and TLCLKn clock output pins will both be the same as the RLCLKn clock. The transmit or receive line, payload and fractional signals can be timed to any of these clock pins. The use of the RLCLKn pin as the timing source is suggested. If RLCLKn is used as the timing source, be sure to set PORT.CR3.RFTS = 1 for input timing.

10.2.1.1.2 Loop Timing Disabled

When loop timing is disabled, the transmit clock source can be different than the receive clock source. The loopback functions, LLB, PLB and DLB, will cause the clock sources to switch when they are activated. Care must be taken when selecting the clock reference for the transmit and receive signals.

The most versatile clocking option has the receive line interface signals timed to RLCLKn, the transmit line interface signals timed to TLCLKn, the receive framer and fractional signals timed to RCLKOn, and the transmit framer and fractional signals timed to TCLKOn. This clocking arrangement works in all modes.

When LLB is enabled, the clock on the TLCLKn pins will switch to the clock from the RLCLKn pins. It is recommended that the transmit line interface signals be timed to the TLCLKn pins. If TLCLKn is used as the timing source, be sure to set PORT.CR3.TLTS = 0 for output timing.

When PLB is enabled, the TCLKIn pin will not be used and the internal transmit clock is switched to the internal receive clock. The clock on the TCLKOn pins will switch to the clock from the RLCLKn pins. The framer or fractional input signals will be ignored while PLB is enabled. It is recommended that the transmit line interface signals be timed to the TCLKOn pins.

When DLB is enabled, the internal receive clock is switched to the internal transmit clock which is sourced from the TCLKIn pins or one of the CLAD clocks, and the clock on the RLCLKn pins will not be used. The clock on the RCLKOn pins will switch to the clock on the TCLKIn pins or one of the CLAD clocks. The receive line signals from the line interface pins will be ignored. It is recommended that the receive framer and fractional pins be timed to the RCLKOn pins. If TCLKOn is used as the timing source, be sure to set PORT.CR3.TFTS = 0 for output timing.

When both DLB and LLB are enabled, the TLCLKn clock pins are connected to the RLCLKn clock pins, and the RCLKOn clock pins will be connected to the TCLKIn clock pins or one of the CLAD clocks. It is recommended that the transmit line signals be timed to the TLCLKn pins, the receive line interface signals be timed to the RLCLKn pins, the receive framer and fractional signals be timed to the RCLKOn pins, and the transmit framer and fractional signals be timed to the TCLKOn pins.

10.2.1.2 CLAD Timing Disabled – no LB

In this mode, the RLCLKn pins source the clock for the receive logic and the TCLKIn pins source the clock for the transmit logic.

10.2.1.3 CLAD Timing Enabled – no LB

In this mode, the RLCLKn pins source the clock for the receive logic and one of the CLAD clocks sources the clock for the transmit logic.

10.2.2 Sources of Clock Output Pin Signals

The clock output pins can be sourced from many clock sources. The clock sources are the transmit input clocks pins (TCLKIn), the receive clock input pins (RLCLKn), and the clock signals in the clock rate adapter circuit (CLAD). The default clock source for the receive logic is the RLCLKn pin. The default clock source for the transmit logic is the CLAD clocks.

The bits LM, LBM[2:0], LOOPT and CLADC are located in the port configuration registers.

Table 10-1 identifies the framer clock source and the line clock source depending on the mode that the device is configured. Putting the device in loopback will typically mux in a different clock than the normal clock source.

Table 10-1. All Possible Clock Sources Based on Mode and Loopback

Mode	Loopback	RX framer clock source	TX framer clock source	TX line clock source
Loop Timed	Any	RLCLKn	Same as RX	Same as RX
Normal	None	RLCLKn	TCLKIn or CLAD	Same as TX
Normal	LLB	RLCLKn	TCLKIn or CLAD	Same as RX
Normal	PLB	RLCLKn	Same as RX	Same as RX
Normal	DLB	Same as TX	TCLKIn or CLAD	Same as TX
Normal	LLB and DLB	Same as TX	TCLKIn or CLAD	RLCLKn

Table 10-2 identifies the source of the output signal TLCLKn based on certain variables and register bits.

Table 10-2. Source Selection of TLCLK Clock Signal

Signal	LOOPT PORT.CR3	LBM[2:0] (PORT.CR4)	LLB or PLB?	CLADC (PORT.CR3)	Source
TLCLKn	1	XXX	NA	X	RLCLKn
	0	010	LLB	X	RLCLKn
	0	110	LLB	X	RLCLKn
	0	000	NO	0	CLAD
	0	001	NO	0	CLAD
	0	100	NO	0	CLAD
	0	10X	NO	0	CLAD
	0	111	NO	0	CLAD
	0	000	NO	1	TCLKIn
	0	001	NO	1	TCLKIn
	0	100	NO	1	TCLKIn
	0	10X	NO	1	TCLKIn
	0	111	NO	1	TCLKIn

Figure 10-2 shows the source of the TCLKOn signals.

Figure 10-2. Internal TX Clock

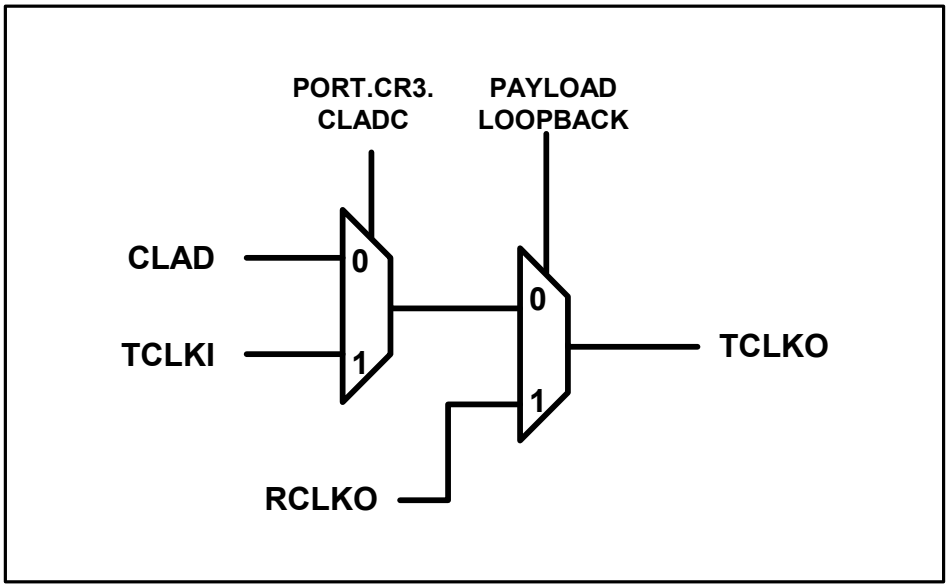


Table 10-3 identifies the source of the output signal TCLKOn based on certain variables and register bits.

Table 10-3. Source Selection of TCLKOn (internal TX clock)

Signal	LOOPT PORT.CR3	LBM[2:0] (PORT.CR4)	CLADC (PORT.CR3)	Source
	1	XXX	X	RLCLKn
	0	PLB (011)	X	RLCLKn
	0	PLB disabled	0	CLAD
	0	PLB disabled	1	TCLKIn

Table 10-4 identifies the source of the output signal RCLKOn based on certain variables and register bits.

Table 10-4. Source Selection of RCLKO Clock Signal (internal RX clock)

Signal	LOOPT PORT.CR3	LBM[2:0] (PORT.CR4)	CLADC (PORT.CR3)	Source
	1	XXX	X	RLCLKn
	0	DLB disabled & ALB disabled	X	RLCLKn
	0	DLB (1XX)	0	CLAD
	0	DLB (1XX) or ALB (001)	1	TCLKIn
	0	DLB (1XX)	1	TCLKIn

10.2.3 Line I/O Pin Timing Source Selection

The line I/O pins can use any input clock pin (RLCLKn or TCLKIn) or output clock pin (TLCLKn, RCLKOn, or TCLKOn) for its clock pin and meet the AC timing specifications as long as the clock signal is valid for the mode the part is in. The clock select bit for the transmit line IO signal group PORT.CR3.TLTS selects the correct input or output clock timing.

10.2.3.1 Transmit Line Interface Pins Timing Source Selection

(TPOSn/TDATn, TNEGn/TOHMOn)

The transmit line interface signal pin group has the same functional timing clock source as the TLCLKn pin described in Table 10-2. Other clock pins can be used for the external timing. The TLCLKn transmit line clock output pin is always a valid output clock for external logic to use for these signals when PORT.CR3.TLTS=0.

The transmit line timing select bit (TLTS) is used to select input or output clock pin timing. When TLTS=0, output clock timing is selected. When TLTS=1, input clock timing is selected. If TLTS is set for input clock timing and an output clock pin is used, or if TLTS is set for output clock timing and an input clock pin is used, then the setup, hold and delay timings, as specified in Table 18-1, will not be valid. There are some combinations of TLTS=1 and other modes in which there is no input clock pin available for external timing since the clock source is derived internally from the CLAD.

Table 10-5. Transmit Line Interface Signal Pin Valid Timing Source Select

LOOPT	LBM[2:0]	CLADC	TLTS	Valid Timing to These Clock Pins
1	XXX	X	0	TLCLKn, TCLKOn, RCLKOn
1	XXX	X	1	RLCLKn
0	DLB (100)	X	0	TLCLKn, TCLKOn, RCLKOn
0	LLB (010) or PLB (011)	X	0	TLCLKn, RCLKOn
0	DLB&LLB (110)	X	0	TLCLKn
0	not DLB (100), not LLB (010), not PLB (011) and not LLB&DLB (110)	X	0	TLCLKn, TCLKOn (default)
0	not LLB (010) and not PLB (011) and not LLB&DLB (110)	0	1	No valid timing to any input clock pin
0	not LLB (010) and not PLB (011) and not LLB&DLB (110)	1	1	TCLKIn
0	LLB (010) or PLB (011) or DLB&LLB (110)	X	1	RLCLKn

10.2.3.2 Transmit Framer and Fractional Pin Timing Source Selection

(TFOHn/TSERn, TFOHENIn/TPDENIn, TOHMIn/TSOFIn, TSOFOn/TDENn/TFOHENOn, TPDATn, TPDENOn)

The transmit framer and fractional signal pin group has the same functional timing clock source as the TCLKO pin described in Table 10-3. Other clock pins can be used for the external timing. The TCLKO transmit clock output pin is always a valid output clock for external logic to use for these signals when TFTS=0.

The transmit framer and fractional timing select bit (TFTS) is used to select input or output clock pin timing. When TFTS=0, output clock timing is selected. When TFTS=1, input clock timing is selected. If TFTS is set for input clock timing and an output clock pin is used, or If TFTS is set for output clock timing and an input clock pin is used, then the setup, hold and delay timings, as specified in Table 18-1, will not be valid. There are some combinations of TFTS=1 and other modes in which there is no input clock pin available for external timing since the clock source is derived internally from the CLAD.

Table 10-6. Transmit Framer Pin Signal Timing Source Select

LOOPT	LBM[2:0]	CLADC	TFTS	Valid Timing to These Clock Pins
1	XXX	X	0	TCLKOn, TLCLKn, RCLKOn
1	XXX	X	1	RLCLKn
0	PLB (011) or DLB (100) or ALB(001)	X	0	TCLKOn, TLCLKn, RCLKOn
0	DLB&LLB (110)	X	0	TCLKOn, RCLKOn
0	LLB (010)	X	0	TCLKOn
0	not LLB, DLB or PLB (00X)	X	0	TCLKOn, TLCLKn
0	not PLB (011)	0	1	No valid timing to any input clock pin
0	not PLB (011)	1	1	TCLKIn
0	PLB (011)	X	1	RLCLKn

10.2.3.3 Receive Line Interface Pin Timing Source Selection

(RPOSn/RDATn, RNEGn/RLCVn/ROHMIn)

The receive line interface signal pin group must be clocked in with the RLCLK clock input pin.

10.2.3.4 Receiver Framer and Fractional Pin Timing Source Selection

(RSERn, RSOFOn/RDENn/RFOHENOn, RFOHENIn/RPDENIn, RPDATn)

The receive framer and fractional signal pin group has the same functional timing clock source as the RCLKOn pin described in Table 10-4.

Other clock pins can be used for the external timing. The RCLKOn receive clock output pin is always a valid output clock for external logic to use for these signals when PORT.CR3.RFTS=0.

The receive framer and fractional timing select bit (RFTS) is used to select input or output clock pin timing. When RFTS=0, output clock timing is selected. When RFTS=1, input clock timing is selected. If RFTS is set for input clock timing and an output clock pin is used, or if RFTS is set for output clock timing and an input clock pin is used, then the setup, hold and delay timings, as specified in Table 18-1, will not be valid. There are some combinations of RFTS=1 and other modes in which there is no input clock pin available for external timing since the clock source is derived internally from the CLAD.

Table 10-7. Receive Framer Pin Signal Timing Source Select

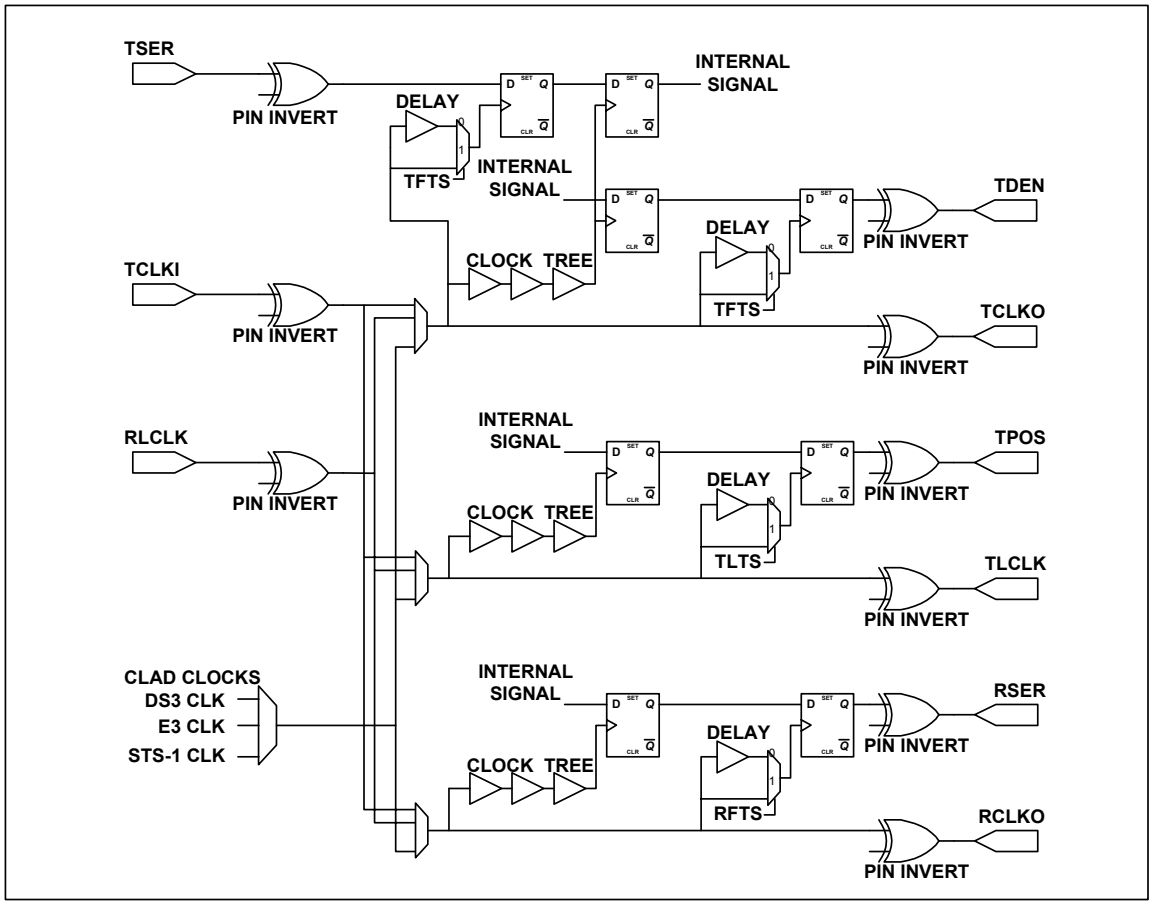
LOOPT	LBM[2:0]	CLADC	RFTS	Valid Timing to These Clock Pins
1	XXX	X	0	RCLKOn, TLCLKn, TCLKOn
1	XXX	X	1	RLCLKn
0	PLB (011) or DLB (100) or ALB(001)	X	0	RCLKOn, TLCLKn, TCLKOn
0	DLB&LLB (110)	X	0	RCLKOn, TCLKOn
0	LLB (010)	X	0	RCLKOn, TLCLKn
0	not LLB, DLB or PLB (00X)	X	0	RCLKOn
0	DLB (100) or LLB&DLB(110)	0	1	No valid timing to any input clock pin
0	DLB (100) or LLB&DLB(110)	1	1	TCLKIn
0	not DLB (100) and not LLB&DLB(110)	X	1	RLCLKn

10.2.4 Clock Structures On Signal IO Pins

The signals on the input pins (RFOHENIn, TOHMIn/TSOFIn, TFOHn/TSERn, TFOHENIn) can be used with any of the clock pins for setup/hold timing on clock input and output pins. There will be a flop at each input whose clock is connected to the signal from the input or output clock source pins with as little delay as possible from the signal on the clock IO pins. This means using the input clock signal before the delays of the internal clock tree to clock the input signals, and using the output clock signals used to drive the output clock pins to clock the input signals.

The signals on the output pins (TPOSn/TDATn, TNEGn/TOHMOn, TSOFOn/TDENn/TFOHENOn, RSERn, RSOFOn/RDENn/RFOHENOn) can be used with any of the clock sources for delay timing. There will be a flop at each output whose clock is connected to the signal from the input or output clock source pins with as little delay as possible from the signal on the clock I/O pins. This means using the input clock signal before the delays of the internal clock tree to clock the input signals, and using the output clock signals to drive the output clock pins to clock the input signals.

Figure 10-3. Example I/O Pin Clock Muxing



10.2.5 Gapped Clocks

The transmit and receive output clocks can be gapped in certain configurations. See Table 10-22 and Table 10-29 for the configuration settings. The gapped clocks are active during DS3 or E3 framed payload bits or DS3 or E3 fractional overhead bits depending on which mode the device is configured for.

In the internal DS3 or E3 fractional modes, the transmit gapped clock is created by the logical OR of the TCLKOn and TFOHENOn signals creating a positive or negative clock edge for each fractional overhead bit, the receive gapped clock is created by the logical OR of the RCLKOn and RFOHENOn signals. In the internal DS3 or E3 non-fractional modes, the transmit gapped clock is created by the logical OR of the TCLKOn and TDENn signals

creating a positive or negative clock edge for each payload bit, the receive gapped clock is created by the logical OR of the RCLKOn and RDENn signals.

When the output clock is disabled, the gapped output signal is high during clock periods if the pin is not inverted; otherwise it will be low.

The gapped clocks are very useful when the data being clocked does not need to be aligned with any frame structure. The data is simply clocked one bit at a time as a continuous data stream.

10.3 Reset and Power-Down

The device can be reset at a global level via the GL.CR1.RST bit or the $\overline{\text{RST}}$ pin and at the port level via the PORT.CR1.RST bit and each port can be explicitly powered down via the PORT.CR1.PD bit. The JTAG logic is reset using the $\overline{\text{JTRST}}$ pin.

The external $\overline{\text{RST}}$ pin and the global reset bit in the global configuration register (GL.CR1.RST) are combined to create an internal global reset signal. The global reset signal resets all the status and control registers on the chip, except the GL.CR1.RST bit, to their default values and resets all the other flops in the system bus interface, global logic and ports to their reset values. The processor bus output signals are also forced to be HIZ when the $\overline{\text{RST}}$ pin is active (low). The global reset bit (GL.CR1.RST) stays set after a one is written to it, but is reset to zero when the external $\overline{\text{RST}}$ pin is active or when a zero is written to it.

At the port level, the global reset signal combines with the port reset bit in the port control register (PORT.CR1.RST) to create a port reset signal. The port reset signal resets all the status and control registers on the port to their default values and resets all the other flops, except PORT.CR1.RST, to their reset values. The port reset bit (PORT.CR1.RST) stays set after a one is written to it, but is reset to zero when the global reset signal is active or when a zero is written to it.

The data path reset function is a little different from the “general” reset function. The data path reset signal does not reset the control register bits, but it does reset all of the status registers, counters and flops, the “general” reset signal resets everything including the control register bits, excluding the reset bit. All clocks are functional, being controlled by configuration bits, while data path reset is active. The CLAD circuit will be operating normally during data path reset which allows the internal phase locked loops to settle as quickly as possible. The line interface will be sending all zeroes (LOS) since data path reset will be forcing the transmit TPOSn and TNEGn to logic zero. (NOTE: The BERT data path and control registers are reset when the global data path reset or the port data path reset or the port power-down signal is active.)

The global data path reset bit (GL.CR1.RSTDP) gets set to one when the global reset signal is active. The port data path reset bit (PORT.CR1.RSTDP) and the port power-down bit (PORT.CR1.PD) bit get set to one when the global reset signal is active or the port reset signal is active. These control bits will be cleared when a zero is written to them if the global reset or the port reset signal is not active. The global data path reset signal is active when the global data path reset bit is set. The port data path reset signal is active when either the global data path reset bit or the port data path reset bit is set. The port power-down signal is active when the port power-down bit is set.

Figure 10-4. Reset Sources

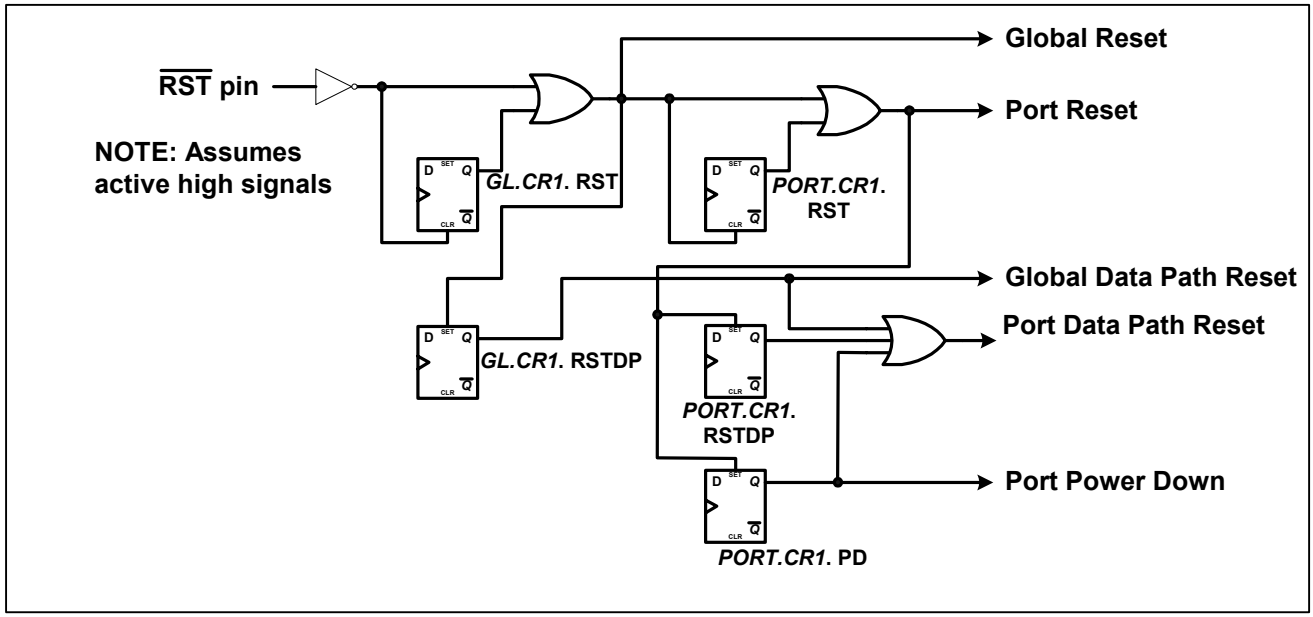


Table 10-8. Reset and Power-Down Sources

Register bit states - F0: Forced to 0, F1: Forced to 1, 0: Set to 0, 1: Set to 1, X: Don't care
Forced: Internally controlled
Set: User controlled

PIN	REGISTER BITS					INTERNAL SIGNALS				
$\overline{RST}$	G:RST	G:RSTDP	P:RST	P:RSTDP	P:PD	Global Reset	Global DP Reset	Port Reset	Port DP Reset	Port Power Down
0	F0	F1	F0	F1	F1	1	1	1	1	1
1	1	F1	F0	F1	F1	1	1	1	1	1
1	0	1	1	F1	F1	0	1	1	1	1
1	0	1	0	X	1	0	1	0	1	1
1	0	1	0	X	0	0	1	0	1	0
1	0	0	1	F1	F1	0	0	1	1	1
1	0	0	0	1	1	0	0	0	1	1
1	0	0	0	1	0	0	0	0	1	0
1	0	0	0	0	1	0	0	0	1	1
1	0	0	0	0	0	0	0	0	0	0

The reset signals in the device are asynchronous so they no not require a clock to put the logic into the reset state. Clock signals may be needed to make the logic come out of the reset state.

The power-down function disables the appropriate clocks to cause the logic to generate a minimum of power. Note that the UTOPIA/POS-PHY system interface logic cannot be powered down, the clocks can not be stopped. The 8KREF and ONESEC circuits can be powered down by disabling the 8KREF source. The CLAD can also be powered down by disabling it.

After a global reset, all of the control and status registers in all ports are set to their default values and all the other flops are reset to their reset values. The global register GL.CR1.RSTDP, and the port register PORT.CR1.RSTDP and PORT.CR1.PD bits in all ports, are set after the global reset. A valid initialization sequence would be to clear the PORT.CR1.PD bits in the ports that are to be active, write to all of the configuration registers to set them in the desired modes, then clear the GL.CR1.RSTDP and PORT.CR1.RSTDP bits. This would cause the logic in the ports to start up in a repeatable sequence. The device can also be initialized by clearing the GL.CR1.RSTDP, PORT.CR1.RSTDP and PORT.CR1.PD them writing to all of the configuration registers to set them in the desired modes, and clearing all of the latched status bits. The second initialization scheme could cause the device to temporarily go into modes of operation that were not requested, but will quickly go into the requested modes of operation.

Some of the IO pins are put in a known state at reset. The global IO pins (GPIO[7:0]) are set as inputs at global reset. The port output pins (TLCLKn, TPOSn/TDATn, TNEGn/TOHMOn, TOHCLKn, TOHSOFn, TPOHSOFn/TSOFOn/TDENn/ TFOHENOn, TPOHCLKn/TCLKOn/TGCLKn, ROHn, ROHCLKn, ROHSOFn, RPOHn/RSERn, RPOHSOFn/RSOFOn/RDENn/RFOHENOn, RPOHCLKn/RCLKOn/RGCLKn) are driven low at global or port reset and should stay low until after the port power-down PORT.CR1.PD and port data path reset PORT.CR1.RSTDP bits are cleared. The system interface tri-state output pins (TDXA[1]/TPXA, TSPA, RDATA[31:0], RPRTY, RDXA[1]/RPXA/RSX, RSOX, REOP, RVAL, RMOD[1:0], RERR) are high impedance and the system interface output pins (TDXA[4:2],RDXA[4:2]) are driven low at global reset. The processor port tr8-state output pins (D[15:0], $\overline{\text{RDY}}$, $\overline{\text{INT}}$) are forced into the high-impedance state when the $\overline{\text{RST}}$ pin is active, but not when the GL.CR1.RST bit is active.

After reset, the device will be in the default configuration: The latched status bits are enabled to be cleared on write. The CLAD is disabled. The global 8KREF and one-second timers are disabled. The line interface is in B3ZS mode and the transmit line pins are also disabled. The frame mode is DS3 C-bit with automatic downstream AIS on LOS or OOF is enabled and automatic RDI on LOF, LOS, SEF or AIS is enabled and automatic FEBE is enabled. Transmit clock comes from the CLAD CLKA pin. Cell processing is enabled with payload scrambling and HEC recalculation and Coset addition enabled. The transmit and receive FIFOs are held in reset so no cell traffic will occur until the FIFOs are configured. The system interface is in 8-bit UTOPIA level 2 with odd parity enabled and HEC transfer disabled. The pin inversion on all pins is disabled.

Individual blocks are reset and powered down when not used determined by the settings in the line mode bits PORT.CR2.LM and framer mode bits PORT.CR2.FM[5:0].

10.4 Global Resources

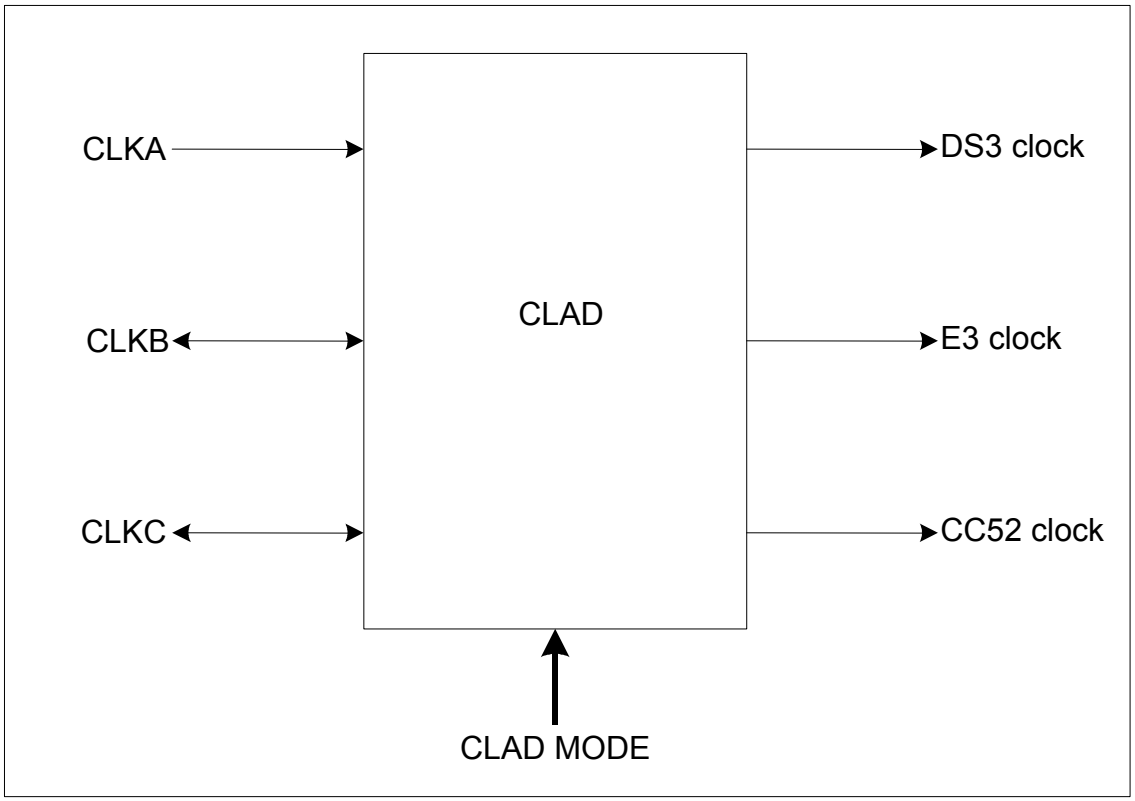
10.4.1 Clock Rate Adapter (CLAD)

The clock rate adapter is used to create multiple clocks for transmit clocks from a single clock reference input on the CLKA pin. The clock frequency applied to this pin must be at the DS3 (44.736 MHz), E3 (34.368 MHz) and STS-1 (51.84 MHz) clock rates. Given one of these clocks the other two clocks will be generated. The internally generated signals can be driven on output pins (CLKB and CLKC) for external use.

The CLAD output is also available as a transmit clock source if selected via the PORT.CR2.CLADC register bit.

The user must supply at least one of the three rates (DS3, E3, STS-1) to the CLKA pin. The CLAD[3:0] bits informs the PLL of the frequency applied to the pins. Selection of the output clock of the CLAD applied to the transmitter is controlled by the FM bits (located in PORT.CR2). The CLAD allows maximum flexibility to the user. The user may supply any of the three clock rates and use the CLAD to convert the rate to the particular clock rate needed for his application.

Figure 10-5. CLAD Block



The clock rate adapter can also be disabled and all three clocks supplied externally using the CLKA, CLKB and CLKC pins as clock inputs. When the CLAD is disabled, the three reference clocks DS3, E3 and STS-1 will need to be applied to the CLKA, CLKB and CLKC pins, respectively. If any of the three frequencies is not required, it does not need to be applied to the CLAD CLK pins.

The CLAD MODE inputs to the clock rate adapter are composed of CLAD[3:0] control bits (located in the GL.CR2 Register) which determines which pins are input and output and which clock rate is on which pin. When CLAD[3:0]=00XX, the PLL circuits are disabled and the signals on the input clock pins are used. When CLAD[3:0]=(01XX or 10XX or 11XX), none, one or two PLL circuits are enabled to generate the required clocks as determined by the CLAD[3:0] bits and the framing mode (FM[5:0]) and the line mode (LM) control bits. If a clock rate is not required on the CLAD output clock pins, then the PLL used to generate that clock is disabled and powered down.

For example, in a design that only has the ports running at DS3 rates, then CLAD[3:0] can be set = 0100 and no PLL circuit will be enabled.

Table 10-9. CLAD IO Pin Decode

GL.CR2. CLAD[3:0]	CLKA PIN	CLKB PIN	CLKC PIN
00 XX	DS3 clock input	E3 clock input	STS-1 clock input
01 00	DS3 clock input	Low output	Low output
01 01	DS3 clock input	E3 clock output	Low output
01 10	DS3 clock input	Low output	STS-1 clock output
01 11	DS3 clock input	STS-1 clock output	E3 clock output
10 00	E3 clock input	Low output	Low output
10 01	E3 clock input	DS3 clock output	Low output
10 10	E3 clock input	Low output	STS-1 clock output
10 11	E3 clock input	STS-1 clock output	DS3 clock output
11 00	STS-1 clock input	Low output	Low output
11 01	STS-1 clock input	E3 output	Low output
11 10	STS-1 clock input	Low output	DS3 clock output
11 11	STS-1 clock input	DS3 clock output	E3 clock output

10.4.2 8 kHz Reference Generation

The 8KREF signal is used to control the rate of PLCP frames to precisely 8000 per second. The global 8KREF signal is also used to generate the one-second reference signal by dividing it by 8000. This signal can be derived from almost any clock source on the chip as well as the general-purpose I/O pin GPIO4. The port 8KREF signal can be sourced from either the global 8KREF signal or from the transmit or receive port clock or from the receive 8KREF signal. The minimum input frequency stability of the 8KREF input pin is ±500 ppm.

The global 8KREF signal can come from an external 8000 Hz reference connected to the GPIO4 general-purpose I/O pin by setting the GL.CR2.G8KIS bit. The global 8KREF signal can be output on the GPIO2 general-purpose I.O pin when the GL.CR2.G8KOS bit is set.

The global 8KREF signal can be derived from the CLAD PLL or pins or come from any of the port 8KREF signals by clearing GL.CR2.G8KIS bit and selecting the source using the GL.CR2.G8KRS[2:0] bits.

The port 8KREF signal can be derived from either the receive PLCP 8KREF signal or from the transmit clock input pin or input clock pin. The PORT.CR3.P8KRS[1:0] bits are used to select which source.

The transmit PLCP 8KREF signal can be selected to be either the global 8KREF signal or the port 8KREF signal using the PORT.CR3.P8KREF bit.

The 8KREF 8.000 kHz signal is a simple divisor of 51840 kHz (CC52 divided by 6480), 44736 kHz (DS3 divided by 5592) or 33368 kHz (E3 divided by 4296). The correct divisor for the port 8KREF source is selected by the mode the port is configured for. The CLAD clock chosen for the clock source selects the correct divisor for the global 8KREF. The 8KREF signal is only as accurate as the clock source chosen to generate it.

Table 10-10 lists the selectable sources for global 8 kHz reference sources.

Table 10-10. Global 8kHz Reference Source Table

GL.CR2. G8KIS	GL.CR2. G8KRS[2:0]	Source
0	**000**	None, the 8KHZ divider is disabled.
0	001	Derived from CLAD DS3 clock output or CLKA pin if CLAD is disabled. (Note: CLAD is disabled after reset)
0	010	Derived from CLAD E3 clock output or CLKB pin if CLAD is disabled
0	011	Derived from CLAD STS-1 clock output or CLKC pin if CLAD is disabled
0	100	Port 1 8KREF source selected by P8KRS[1:0]
0	101	Port 2 8KREF source selected by P8KRS[1:0]
0	110	Port 3 8KREF source selected by P8KRS[1:0]
0	111	Port 4 8KREF source selected by P8KRS[1:0]
1	XXX	GPIO4 pin

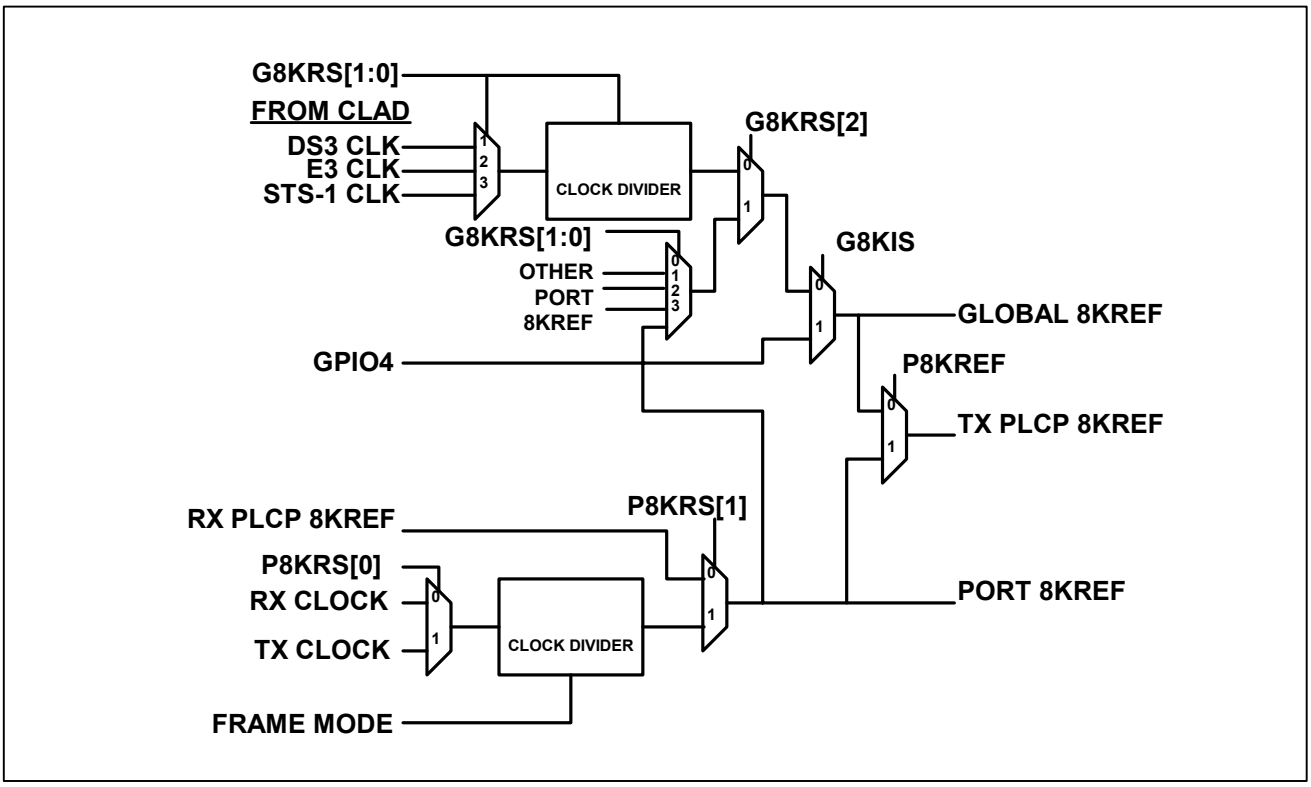
Table 10-11 lists the selectable sources for port 8 kHz reference sources.

Table 10-11. Port 8kHz Reference Source Table

PORT.CR3.P8KRS[1:0]	Source
0X	Receive PLCP 8kHZ output
10	Receive RLCLKn pin
11	Transmit internal framer clock (based on TCLKIn pin or CLAD clock)

The 8 kHz reference logic tree is shown below.

Figure 10-6. 8KREF Logic



10.4.3 One-Second Reference Generation

The one-second reference signal is used as an option to update the performance registers on a precise one second interval. The generated internal signal should be about 50% duty cycle and it is derived from the Global 8 kHz reference signal by dividing it by 8000. The low to high edge on this signal will set the GL.SRL.ONESL latched one second detect bit which can generate an interrupt when the GL.SRIE.ONESIE interrupt enable bit is set. The low to high edge can also be used to generate performance monitor updates when GL.CR1.GPM[1:0]=1X.

10.4.4 General-Purpose I/O Pins

There are eight general-purpose I/O pins that can be used for general I/O, global signals and per port alarm signals. Each pin is independently configurable to be a general-purpose input, general-purpose output, global signal or port alarm. Two of the GPIO pins are assigned to each port and can be programmed to output one or two alarm statuses using one or two GPIO pins. One of the two pins assigned to each port can be programmed as global input or output signals. When the device is bonded out (or has ports powered down) to have 1, 2 or 3 ports active, the GPIO pins associated with the disabled ports will still operate as either general-purpose inputs, general-purpose outputs or global signals. When the ports are disabled and GL.GIOCR.GPIOx[1:0] = 01, the GPIO pin will be an output driving low. The 8KREFI, TMEI, and PMU signals that can be sourced by the GPIO pin will be driven low into the core logic when the GPIO pin is not selected for the source of the signal.

Table 10-12 lists the purpose and control thereof of the general-purpose I/O Pins.

Table 10-12. GPIO Global Signals

Pin	Global signal	Control bit
GPIO2	8KREFO output	GL.CR2.G8KOS
GPIO4	8KREFI input	GL.CR2.G8KIS
GPIO6	TMEI input	GL.CR1.MEIMS
GPIO8	PMU input	GL.CR1.GPM[1:0]

Table 10-13 describes the selection of mode for the GPIO Pins.

Table 10-13. GPIO Pin Global Mode Select Bits

n = port 1 to 4, x = A or B, valid when a GPIO pin is not selected for a global signal

GL.GIOCR.**GPIOnSx**	**GPIO pin mode**
00	Input
01	Port alarm status selected by port GPIO
10	Output logic 0
11	Output logic 1

Table 10-14 lists the various port alarm monitors that can be output on the GPIO pins.The GPIO(A/B)[3:0] bits are located in the PORT.CR4 Register.

Table 10-14. GPIO Port Alarm Monitor Select

PORT.CR4 **GPIO(A/B)[3:0]**	**LINE LOS**	**DS3/E3 OOF**	**DS3/E3 LOF**	**DS3/E3 AIS**	**DS3/E3 RAI**	**DS3 IDLE**	**PLCP OOF**	**PLCP LOF**	**PLCP RAI**	**ATM OCD**	**ATM LCD**
0000	X										
0001		X									
0010			X								
0011				X							
0100					X						
0101						X					
0110							X				
0111								X			
1000									X		
1001										X	
1010											X
1011	X		X	X							
1100								X			X
1101	X		X	X				X			X
1110					X	X			X		
1111	X	X	X	X	X	X	X	X	X	X	X

10.4.5 Performance Monitor Counter Update Details

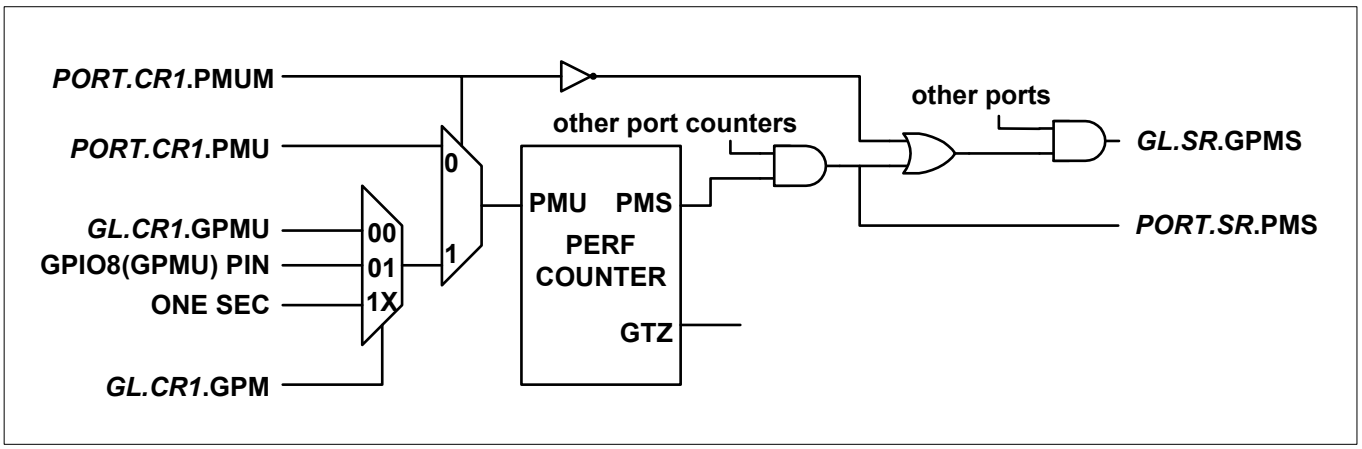
The performance monitor counters are designed to count at least one second of events before saturating to the maximum count. There is a status bit associated with some of the performance monitor counters that is set when the its counter is greater than zero, and a latched status bit that gets set when the counter changes from zero to one. There is also a latched status bit that gets set on every event that causes the error counter to increment.

There is a read register for each performance monitor counter. The count value of the counter gets loaded into this register and the counter is cleared when the update-clear operation is performed. If there is an event to be counted at the exact moment (clock cycle) that the counter is to be cleared then the counter will be set to a value of one so that that event will be counted.

The Performance Monitor Update signal affects the counter registers of the following blocks: the BERT, the DS3/E3 framer, the Line Encoder/Decoder, the DS3/E3 PLCP framer, the Cell Processor, and the Packet Processor.

The update-clear operation is controlled by the Performance Monitor Update signal (PMU). The update-clear operation will update the error counter registers with the value of the error counter and also reset each counter. The PMU signal can be created in hardware or software. The hardware sources can come from the one second counter or one of the general-purpose I/O pins, which can be programmed to source this signal. The software sources can come from one of the per-port control register bits or one of the global control register bits. When using the software update method, the PMU control bit should be set to initiate the process and when the PMS status bit gets set, the PMU control bit should be cleared making it ready for the next update. When using the hardware update method, the PMS bit will be set shortly after the hardware signal goes high, and cleared shortly after the hardware signal goes low. The latched PMS signal can be used to generate an interrupt for reading the count registers. If the port is not configured for global PMU signals, the PMS signal from that port should be blocked from affecting the global PMS status.

Figure 10-7. Performance Monitor Update Logic

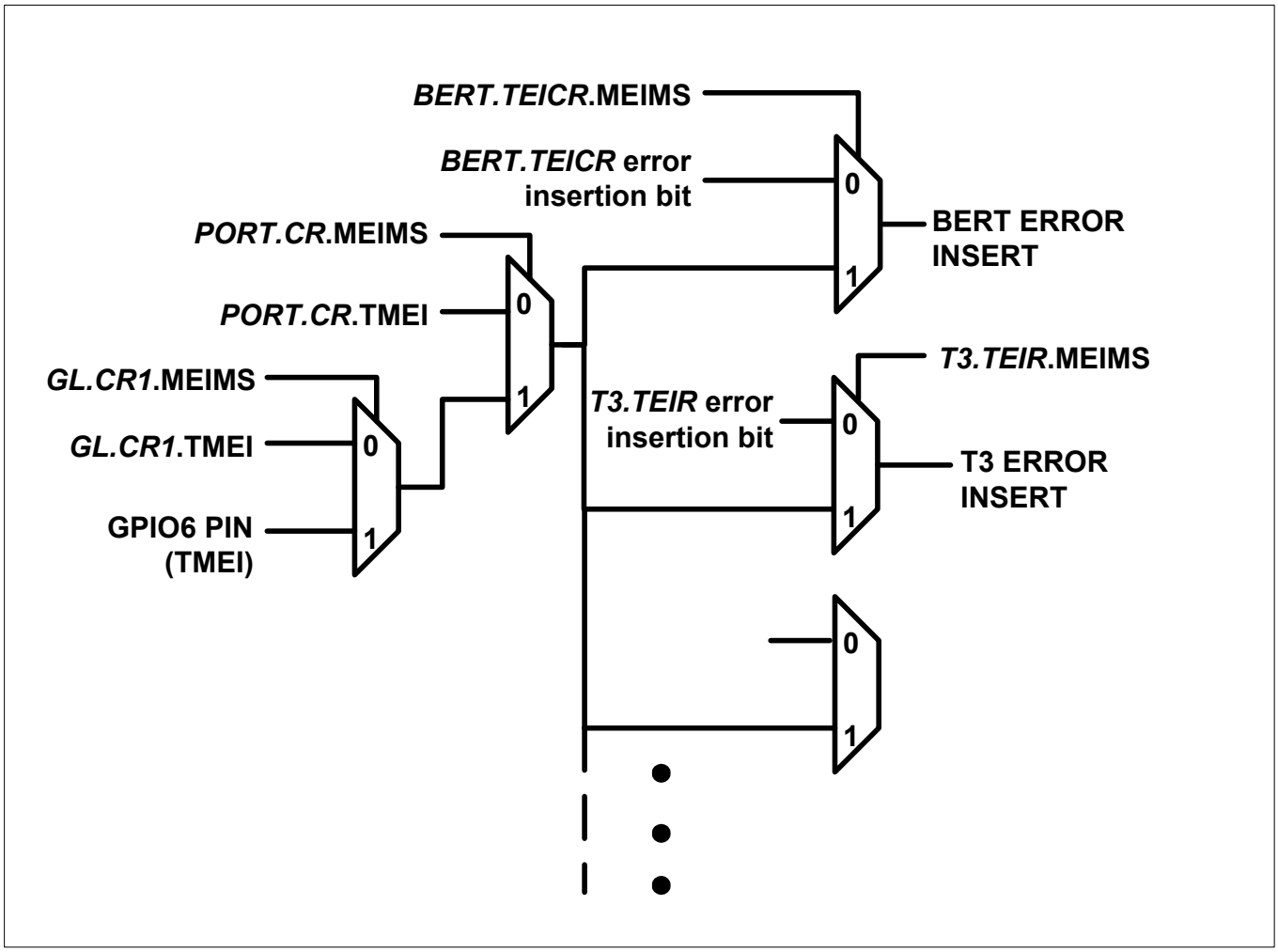


10.4.6 Transmit Manual Error Insertion

Transmit errors can be inserted in some of the functional blocks. These errors can be inserted using register bits in the functional blocks, using the global GL.CR1.TMEI bit, using the port PORT.CR1.TMEI bit, or by using the GPIO6 pin configured for TMEI mode.

There is a transmit error insertion register in the functional blocks that allow error insertion. The MEIMS bit controls whether the error is inserted using the bits in the error insertion register or using error insertion signals external to that block. When bit MEIMS=0, errors are inserted using other bits in the transmit error insertion register. When bit MEIMS=1, errors are inserted using a signal generated in the port or global control registers or using the external GPIO6 pin configured for TMEI operation.

Figure 10-8. Transmit Error Insert Logic



10.5 Per Port Resources

10.5.1 Loopbacks

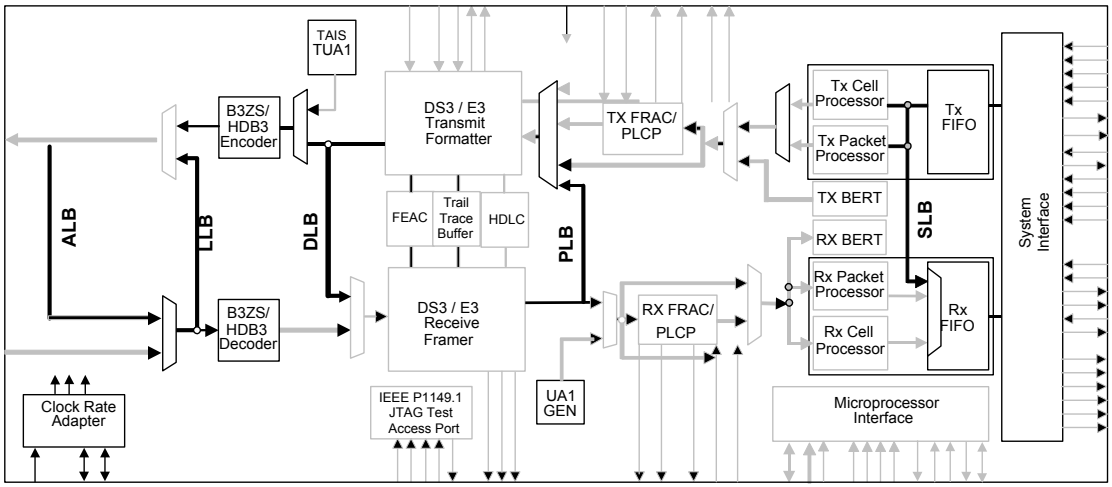
There are several loop back paths available. The following table lists the loopback modes available for analog loopback (ALB), line loopback (LLB), payload loopback (PLB) and diagnostic loopback (DLB). System loopback (SLB) does not interact with these loopbacks and is given its own control bit. The LBM bits are located in PORT.CR4.

Table 10-15. Loopback Mode Selections

LBM[2:0]	ALB	LLB	PLB	DLB
000	0	0	0	0
001	1	0	0	0
010	0	1	0	0
011	0	0	1	0
10X	0	0	0	1
110	0	1	0	1
111	0	0	0	1

Figure 10-9 highlights where each loopback mode is located and gives an overall view of the various loopback paths available.

Figure 10-9. Loopback Modes



10.5.1.1 Terminal Loopback (TLB)

Terminal loopback is enabled by setting PORT.CR4.LBM[2:0] = 001. Terminal loopback mode will not be enabled when the port is configured for loop timed mode (set via the PORT.CR3.LOOPT bit).

The terminal loopback is a loopback as close to the pins as possible. It will loop back TLCLKn,TPOSn / TDATn,TNEGn / TOHMOn to RLCLKn ,RPOSn / RDATn , RNEGn / ROHMIn.

10.5.1.2 Line Loopback (LLB)

Line loopback is enabled by setting PORT.CR4.LBM[2:0] = X10. DLB and LLB are enabled at the same time when LBM[2:0] = 110, and only LLB is enabled when LBM[2:0] = 010.

The clock from the RLCLK pin will be output to the TCLKOn pin. The POS and NEG data from the RPOSn and RNEGn pin will be sampled with the receive clock to time it to the pin interface.

When LLB is enabled, unframed all ones AIS can optionally be automatically enabled on the receive data path. This AIS signal will be output on the RSERn pin in flexible fractional mode, and sent to the receive cell or packet processor in framer modes, effectively stopping cell or packet data flow. When DLB and LLB is enabled, the AIS signal will not be transmitted.

Refer to Figure 10-9.

10.5.1.3 Payload Loopback (PLB)

Payload loopback is enabled by setting PORT.CR4.LBM[2:0] = 011.

The payload loopback copies the payload data from the receive framer to the transmit framer (before the fractional logic) which then re-frames the payload before transmission. Payload loopback is operational in all framing modes except “- OHM” modes.

When PLB is enabled, unframed all ones AIS transmission can optionally be automatically enabled on the receive data path. This AIS signal will be output on the RSER pin in flexible fractional mode, and sent to the receive cell or packet processor in framer modes, effectively stopping cell or packet data flow.

In all modes, the TSOFIn input pin is ignored. The external transmit output pins TDENn and TSOFOn/TDENn can optionally be disabled by forcing a zero when PLB is enabled.

In the framed modes, the data flow from the transmit cell or packet processor can be optionally disabled when PLB is enabled. If the data flow is not disabled, the cells or packets from the system interface will be discarded. See Figure 10-9.

10.5.1.4 Diagnostic Loopback (DLB)

Diagnostic loopback is enabled by setting PORT.CR4.LBM[2:0] = 1XX. DLB and LLB are enabled at the same time when LBM[2:0] = 110, only DLB is enabled when LBM[2:0] = 10X or 111.

The Diagnostic loopback sends the transmit data, before line encoding, back to the receive side.

Transmit AIS can still be enabled using PORT.CR1.LAIS[2:0] even when DLB is enabled.

Refer to Figure 10-9.

10.5.1.5 System Loopback (SLB)

System loopback is enabled by setting the PORT.CR4.SLB bit. The system loopback sends the packets or cells from the transmit UTOPIA or POS-PHY interface back to the receive UTOPIA or POS-PHY interface. Cells and packets from the line interface will be discarded.

Refer to Figure 10-9.

10.5.2 Loss Of Signal Propagation

The Loss Of Signal (LOS) is detected in the line decoder logic if the device is set for HDB3 or B3ZS line encoding. In unipolar (UNI) line interface modes and AMI modes LOS detection is disabled. The LOS signal from the line decoder is sent to the DS3/E3 framer and the top level payload AIS logic except when DLB is activated. When DLB is activated the LOS signal to the framer and AIS logic is never active. The LOS status in the line decoder status register is valid in all frame and loop back modes, though it is always off in the line interface is in the UNI mode.

10.5.3 AIS Logic

There is AIS logic in both the framers and at the top level logic of the ports. The framer AIS is enabled by setting the TAIS bit in the appropriate framer transmit control register (T3, E3-G.751, E3-G.832, or Clear Channel). The top level AIS is enabled by setting the PORT.CR1.LAIS[2:0] bits (see Table 10-16). The AIS signal is an unframed all ones pattern or a DS3 framed 101010… pattern depending on the FM[5:0] mode bits. The DS3 Framed Alarm Indication Signal (AIS) is a DS3 signal with valid F-bits, M-bits, and P-bits (P_1 and P_2). The X-bits (X_1 and X_2) are set to one, all C-bits (C_{XY}) are set to zero, and the payload bits are set to a 1010 pattern starting with a one immediately after each overhead bit. The DS3 framed AIS pattern is only available in DS3 modes. The unframed all ones pattern is available in all framing and clear-channel modes including the DS3 modes. The transmit line interface can send both unframed all ones AIS and DS3 framed AIS patterns from either the AIS generator in the framer or the AIS generator at the top level.

The AIS signal generated in the framer can be initiated and terminated without introducing any errors in the signal. When the unframed AIS signal is initiated or terminated, there will be no BPV or CV errors introduced, there will be framing errors if a framed mode is enabled. When the DS3 framed AIS signal is initiated or terminated, in addition to no BPV or CV errors, there should be no framing or P-bit (parity) or CP-bit errors introduced.

The AIS signal generated at the top level will not generate BPV errors but may generate P-bit and CP-bit errors when the signal is initiated and terminated. The framed DS3 AIS signal will not cause the far end receiver to re-sync when the signal is initiated, but it may cause a re-sync when terminated if the DS3 frame position in the framer is changed while the DS3 AIS signal is being generated. A sequence of events can be executed which will enable the initiation and termination of DS3 AIS or unframed all ones at the top level without any errors introduced. The sequence will only work when the automatic AIS generation is not enabled. CV and P-bit errors can occur when AIS is automatically generated and cannot be avoided. This sequence to generate an error free DS# AIS at the top level is to have the DS3 AIS or unframed all ones signal initiate in the DS3 framer, and a few frames sent before initiating or terminating the DS3 AIS or unframed all ones at the top level. After the top level AIS signal is activated, the AIS signal in the framer can be terminated, DLB activated and diagnostic patterns generated. The DS3 AIS signal generated at the top level will not change frame alignment after starting even if the DS3 frame position in the framer is changed.

The transmit line AIS generator at the top level can generate AIS signals even when the framer is looped back using DLB, but not when the line is looped back using LLB. The AIS signal generated in the framer will be looped back to the receive side when DLB is activated.

The receive framer can detect both unframed all ones AIS and DS3 framed AIS patterns. When in DS3 framing modes, both framed DS3 AIS and unframed all ones can be detected. In E3 framing modes E3 AIS, which is unframed all ones, is detected. In clear-channel modes, unframed all ones is detected.

The receive payload interface going to the RSERn pin or the PLCP, FRAC, BERT or ATM/PKT logic can have an unframed all ones AIS signal replacing the receive signal, this is called Payload AIS. The all ones AIS signal is generated from either the DS3/E3 framer or the downstream top level unframed all ones AIS generator. The unframed all ones AIS signal generated in the framer will be looped back to the transmit side when PLB is activated. The unframed all ones AIS signal generated at the top level will be sent to the RSERn pin and other receive logic, but not to the transmit side while PLB is activated. The top level AIS generator is used when a downstream AIS signal is desired while payload loop back is activated and is enabled by default after rest and must be cleared during configuration. Note that the downstream AIS circuit in the framer, when a DS3 mode is selected, enforces the OOF to be active for 2.5 msec before activating when automatic AIS in the framer is enabled. The top level downstream AIS will be generated with no delay when OOF is detected when automatic AIS at the top level is enabled.

There is no detection of any AIS signal on the transmit payload signal from the TSERn pin or anywhere on the transmit data path.

The transmit AIS generator at the top level can also be activated with a software bit or automatically when DLB is activated. The receive AIS generator in the framer can be activated with a software bit, and automatically when AIS, LOS or OOF are detected. The receive payload AIS generator at the top level can be activated with a software bit or automatically when LOS, DS3/E3 OOF, LLB, or PLB is activated.

When the port is configured for "- OHM" modes, the transmit DS3 AIS signal pattern generation is paused when the TOHMI signal is active. Also the receive DS3 AIS and unframed all ones detectors do not use the bits marked for overhead from the ROHMIn signal when DLB is not activated or the TOHMIn signal when DLB is activated. The payload unframed all ones overwrites the receive signal with all ones even in overhead bit positions.

Figure 10-10 shows the AIS signal flow through the device.

Figure 10-10. AIS Signal Flow

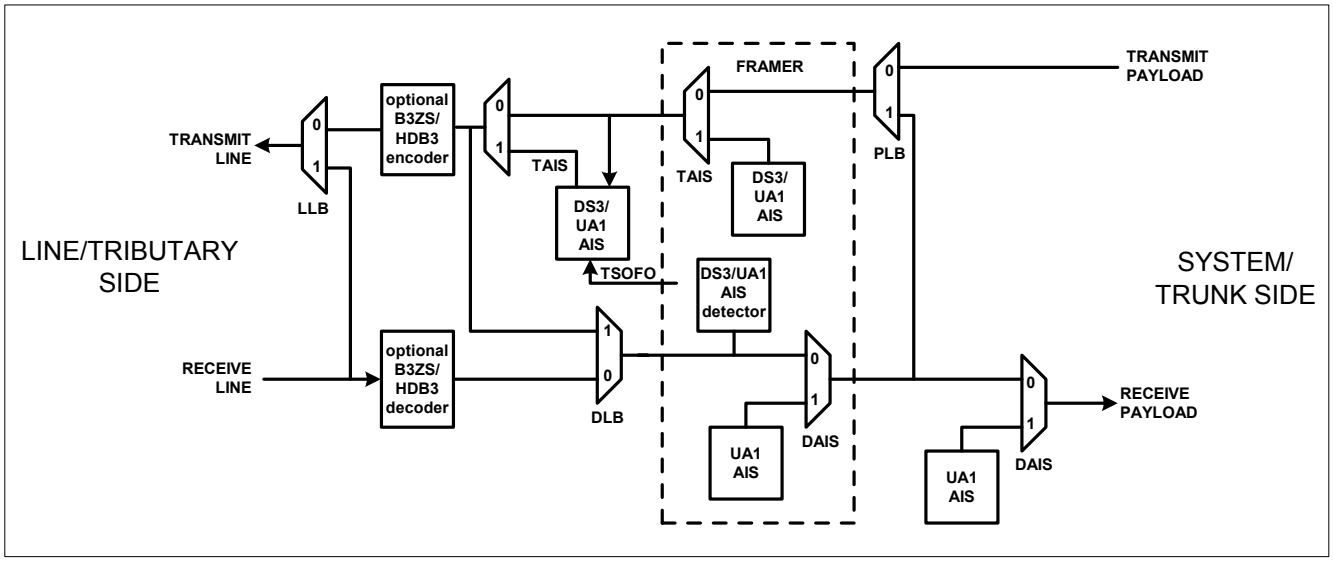


Table 10-16 lists the LAIS decodes for various line AIS enable modes.

Table 10-16. Line AIS Enable Modes

LAIS[1:0] PORT.CR1	Frame Mode	Description	AIS Code
00	DS3	Automatic AIS when DLB is enabled (PORT.CR4.LBM = 1XX)	DS3AIS
00	E3	Automatic AIS when DLB is enabled	UA1
00	Clear Channel	Automatic AIS when DLB is enabled	UA1
01	Any	Send UA1	UA1
10	DS3	Send AIS	DS3AIS
10	E3 or Clear Channel	Send AIS	UA1
11	Any	Disable	none

Table 10-17 lists the PAIS decodes for various payload AIS enable modes.

Table 10-17. Payload (downstream) AIS Enable Modes

PAIS[2:0] PORT.CR1	When AIS is sent	AIS Code
000	Always	UA1
001	When LLB (no DLB) active	UA1
010	When PLB active	UA1
011	When LLB(no DLB) or PLB active	UA1
100	When LOS (no DLB) active	UA1
101	When OOF active	UA1
110	When OOF, LOS. LLB (no DLB), or PLB active	UA1
111	Never	none

10.5.4 Loop Timing Mode

Loop timing mode is enabled by setting the *PORT.CR3*.LOOPT bit. This mode replaces the clock from the TCLKIn pin with the internal receive clock from the RLCLKn pin. The loop timing mode can be activated in any framing or line interface mode.

10.5.5 HDLC Overhead Controller

There is a single HDLC controller for use in line maintenance protocols. The DS3, E3 and PLCP framers share the same HDLC controller. Since the PLCP and DS3 or E3 framers can potentially use the HDLC controller at the same time, there is a select bit in the port control register to chose which one uses the HDLC controller (PORT.CR1.HDSEL). The port that does not get access to the HDLC controller will transmit all ones in the overhead bits that the HDLC controller would connect to. The external overhead ports can be used to connect to an external HDLC controller if both framers need the function.

The data signal to the receive HDLC controller will be forced to a one while still being clocked when the framer (DS3, E3, or PLCP), to which the HDLC is connected, detects LOF or AIS. Forcing the data signal to all ones will cause an HDLC packet abort if the data started to look like a packet instead of allowing a bad, and possibly very long, HDLC packet.

10.5.6 Trail Trace

There is a single Trail Trace controller for use in line maintenance protocols. The E3-G.832 and PLCP framers can use the trail trace controller and it is shared automatically since the E3-G.832 and PLCP framing can not be enabled at the same time.

10.5.7 BERT

There is a Bit Error Rate Test (BERT) circuit for each port for use in generating and detecting test signals in the payload bits. The BERT can generate and detect PRBS patterns up to 2^32-1 bits as well as repeating patterns up to 32 bits long. The generated BERT signal replaces the cells or packets from the system interface when the BERT is enabled by setting the PORT.CR1.BENA.

The cells or packets from the system interface will still be processed using the same bit rate as when the BERT was not enabled. Any transmit cells will be simply discarded when the BERT is enabled, and any cells or packets on the line interface will be processed and sent to the system bus when the BERT is enabled. The TDENn and RDENn pins will still be active but the data on the TSERn pin will be discarded when the BERT is enabled.

10.5.8 Fractional Payload Controller

The Fractional Payload Controller allows the user flexibility to control sub-rate datastreams. The Fractional Payload Controller performs fractional overhead/payload data multiplexing. Fractional overhead is sourced from either an internal register or the external interface. The allocation of the DS3/E3 payload is also controlled either internally (internally controlled mode) or through the external interface (externally controlled mode).

The third option is Flexible Mode, which allows the user to externally multiplex payload and overhead, bypassing the Fractional Payload Controller.

10.5.9 PLCP/Fractional port pins

The PLCP/Fractional port pins have multiple functions based on the framing mode the device is in as well as other pin mode select bits.

10.5.9.1 Transmit PLCP/Fractional port pins

The transmit PLCP/Fractional pins are TSOFIn / TOHMIn, TPOHn / TFOHn / TSERn, TPOHENn / TFOHENIn / TPDENIn, TPOHSOFn / TSOFOn / TDENn / TFOHENOn, TPDENOn, TPDATn, and TPOHCLKn / TCLKOn / TGCLKn. They have different functions based on the framing mode and other pin mode bits. Unused input pin functions should drive a logic zero into the device circuits expecting a signal from that pin. The control bits that configure the pins' modes are PORT.CR2.FM[5:0], PORT.CR3.TPFPE, PORT.CR3.TSOFOS and PORT.CR3.TCLKS.

Table 10-18 to Table 10-24 describe the function selected by the FM bits and other pin mode bits for the multiplexed pins.

Table 10-18. TSOFIn / TOHMIn Input Pin Functions

FM[5:0] PORT.CR2	Pin function
0XXX00 (FRM)	TSOFIn
0XXX1X (FRM)	TSOFIn
0XXX01 (OHM)	TOHMIn
1XX0X1 (OHM)	TOHMIn
1XX0X0 (UFRM)	Not used
1XX1XX (UFRM)	Not used

Table 10-19. TSERn / TPOHn / TFOHn Input Pin Functions

FM[5:0] PORT.CR2	TPFPE PORT.CR3	Pin function
0XX00X (FRM)	X	Not used
0XX010 (IFRAC)	0	Not used
0XX010 (IFRAC)	1	TFOHn
0XX011 (XFRAC)	X	TFOHn
0XX10X (PLCP)	0	Not used
0XX10X (PLCP)	1	TPOHn
0XX110 (FFRAC)	X	TSERn
1XX0XX (CLR)	X	Not used

Table 10-20. TPDENIn / TPOHENn / TFOHENIn Input Pin Functions

FM[5:0] PORT.CR2	TPFPE PORT.CR3	Pin function
0XX00X (FRM)	X	Not used
0XX010 (IFRAC)	X	Not used
0XX011 (XFRAC)	X	TFOHENIn
0XX10X (PLCP)	0	Not used
0XX10X (PLCP)	1	TPOHENn
0XX110 (FFRAC)	X	TPDENIn
1XXXXX (CLR)	X	Not used

Table 10-21. TSOFOn / TDENn / TPOHSOFn / TFOHENOn Output Pin Functions

FM[5:0] PORT.CR2	TPFPE PORT.CR3	TSOFOS PORT.CR3	Pin function
0XX00X (FRM)	0	X	Low
0XX00X (FRM)	1	0	TDENn
0XX00X (FRM)	1	1	TSOFOn
0XX010 (IFRAC)	0	X	Low
0XX010 (IFRAC)	1	X	TFOHENOn
0XX011 (XFRAC)	X	0	TDENn
0XX011 (XFRAC)	X	1	TSOFOn
0XX10X (PLCP)	0	X	Low
0XX10X (PLCP)	1	X	TPOHSOFn
0XX110 (FFRAC)	X	0	TDENn
0XX110 (FFRAC)	X	1	TSOFOn
1XX0XX (CLR)	X	X	Low

Table 10-22. TCLKOn / TGCLKn / TPOHCLKn Output Pin Functions

FM[5:0] PORT.CR2	TPFPE PORT.CR3	TCLKS PORT.CR3	Pin function	Gap source
0XX00X (FRM)	0	X	Low	none
0XX00X (FRM)	1	0	TGCLKn	TDENn
0XX00X (FRM)	1	1	TCLKOn	none
0XX010 (IFRAC)	0	X	Low	none
0XX010 (IFRAC)	1	0	TGCLKn	TFOHENOn
0XX010 (IFRAC)	1	1	TCLKOn	none
0XX011 (XFRAC)	X	X	TCLKOn	none
0XX10X (PLCP)	0	X	Low	none
0XX10X (PLCP)	1	0	TPOHCLKn	none
0XX10X (PLCP)	1	1	TCLKOn	none
0XX110 (FFRAC)	X	0	Low	none
0XX110 (FFRAC)	X	1	TCLKOn	none
1XX0XX (CLR)	0	X	Low	none
1XX0XX (CLR)	1	X	TCLKOn	none

Table 10-23. TPDATn Input Pin Functions

FM[5:0] PORT.CR2	TPFPE PORT.CR3	Pin function
0XX0XX (FRM)	X	Low
0XXX0X (FRM)	X	Low
0XX110 (FFRAC)	X	TPDATn
1XXXXX (CLR)	X	Low

Table 10-24. TPDENOn Output Pin Functions

FM[5:0] PORT.CR2	TPFPE PORT.CR3	Pin function
0XX0XX (FRM)	X	Low
0XXX0X (FRM)	X	Low
0XX110 (FFRAC)	X	TPDENOn
1XXXXX (CLR)	X	Low

10.5.9.2 Receive PLCP/Fractional port pins

The receive PLCP/Fractional pins are RPOHn / RSERn, RFOHENIn / RPDENIn, RPDATn, RPOHSOFn / RSOFOn / RDENn / RFOHENOn and RPOHCLKn / RCLKOn / RGCLKn. They have different functions based on the framing mode and other pin mode bits. Unused input pin functions should drive a logic zero into the device circuits expecting a signal from that pin. The control bits that configure these pins are PORT.CR2.FM[5:0], PORT.CR3.RPFPE, PORT.CR3.RSOFOS and PORT.CR3.RCLKS.

Table 10-25 to Table 10-29 describe the function selected by the FM bits and other pin mode bits for the multiplexed pins.

Table 10-25. RSERn / RPOHn Output Pin Functions

FM[5:0] PORT.CR2	RPFPE PORT.CR3	Pin function
0XX00X (FRM)	0	Low
0XX00X (FRM)	1	RSERn
0XX010 (IFRAC)	0	Low
0XX010 (IFRAC)	1	RSERn
0XX011 (XFRAC)	X	RSERn
0XX10X (PLCP)	0	Low
0XX10X (PLCP)	1	RPOHn
0XX110 (FFRAC)	X	RSERn
1XX0XX (CLR)	0	Low
1XX0XX (CLR)	1	RSERn

Table 10-26. RPDENIn / RFOHENIn Input Pin Functions

FM[5:0] PORT.CR2	RPFPE PORT.CR3	Pin function
0XX00X (FRM)	X	Not used
0XX010 (IFRAC)	X	Not used
0XX011 (XFRAC)	X	RFOHENIn
0XX10X (PLCP)	X	Not used
0XX110 (FFRAC)	X	RPDENIn
1XXXXX (CLR)	X	Not used

Table 10-27. RPDATn Input Pin Functions

FM[5:0] PORT.CR2	RPFPE PORT.CR3	Pin function
0XX0XX (FRM)	X	Not used
0XXX0X (FRM)	X	Not used
0XX110 (FFRAC)	X	RPDATn
1XXXXX (CLR)	X	Not used

Table 10-28. RSOFOn / RDENn / RPOHSOFn / RFOHENOn Output Pin Functions

FM[5:0] PORT.CR2	RPFPE PORT.CR3	RSOFOS PORT.CR3	Pin function
0XX00X (FRM)	0	X	Low
0XX00X (FRM)	1	0	RDENn
0XX00X (FRM)	1	1	RSOFOn
0XX010 (IFRAC)	0	X	Low
0XX010 (IFRAC)	1	X	RFOHENOn
0XX011 (XFRAC)	X	0	RDENn
0XX011 (XFRAC)	X	1	RSOFOn
0XX10X (PLCP)	0	X	Low
0XX10X (PLCP)	1	X	RPOHSOFn
0XX110 (FFRAC)	X	0	RDENn
0XX110 (FFRAC)	X	1	RSOFOn
1XX0XX (CLR)	X	X	Low

Table 10-29. RCLKOn / RGCLKn / RPOHCLKn Output Pin Functions

FM[5:0] PORT.CR2	RPFPE PORT.CR3	RCLKS PORT.CR3	Pin function	Gap source
0XX00X (FRM)	0	X	Low	none
0XX00X (FRM)	1	0	RGCLKn	RDEN
0XX00X (FRM)	1	1	RCLKOn	none
0XX010 (IFRAC)	0	X	Low	none
0XX010 (IFRAC)	1	0	RGCLKn	RFOHENOn
0XX010 (IFRAC)	1	1	RCLKOn	none
0XX011 (XFRAC)	X	X	RCLKOn	none
0XX10X (PLCP)	0	X	Low	none
0XX10X (PLCP)	1	0	RPOHCLKn	none
0XX10X (PLCP)	1	1	RCLKOn	none
0XX110 (FFRAC)	X	0	Low	none
0XX110 (FFRAC)	X	1	RCLKOn	none
1XX0XX (CLR)	0	X	Low	none
1XX0XX (CLR)	1	X	RCLKOn	none

10.5.10 Framing Modes

The framing modes are selected independently of the line interface modes using the *PORT.CR2*.FM[5:0] control bits. Different blocks are used in different framing modes. The bit error test (BERT) function can be enabled in any mode. The line encoder/decoder blocks are selected by the line mode (LM) code.

The “- OHM” mode, also known as “externally defined frame mode”, is a mode that allow the use of the external frame overhead bit mask pins TOHMIn, TOHMOn and ROHMIn. This mode allows external logic to select bit locations where another level of framing can add overhead bits such as SONET/SDH overhead bits. Payload loopback (PLB) is disabled in this mode. The “Clear-Channel—OHM Octet aligned” modes perform octet alignment

to the overhead mask for ATM and packets and the packets become octet stuffed instead of bit stuffed. Refer to Table 10-30.

Table 10-30. Framing Mode Select Bits FM[5:0]

FM[5:0]	DESCRIPTION	LINE CODE	SYSTEM	FIGURE
0 00 000	DS3 C-bit	B3ZS/AMI/UNI	ATM/PKT	Figure 6-1
0 00 001	DS3 C-bit - OHM	UNI	ATM/PKT	Figure 6-2
0 00 010	DS3 C-bit Internal Fractional	B3ZS/AMI/UNI	ATM/PKT	Figure 6-3
0 00 011	DS3 C-bit External Fractional	B3ZS/AMI/UNI	ATM/PKT	Figure 6-4
0 00 100	DS3 C-bit PLCP	B3ZS/AMI/UNI	ATM	Figure 6-6
0 00 101	DS3 C-bit PLCP - OHM	UNI	ATM	Figure 6-7
0 00 110	DS3 C-bit Flexible Fractional	B3ZS/AMI/UNI	ATM/PKT	Figure 6-5
0 01 000	DS3 M23	B3ZS/AMI/UNI	ATM/PKT	Figure 6-1
0 01 001	DS3 M23 - OHM	UNI	ATM/PKT	Figure 6-2
0 01 010	DS3 M23 Internal Fractional	B3ZS/AMI/UNI	ATM/PKT	Figure 6-3
0 01 011	DS3 M23 External Fractional	B3ZS/AMI/UNI	ATM/PKT	Figure 6-4
0 01 100	DS3 M23 PLCP	B3ZS/AMI/UNI	ATM	Figure 6-6
0 01 101	DS3 M23 PLCP - OHM	UNI	ATM	Figure 6-7
0 01 110	DS3 M23 Flexible Fractional	B3ZS/AMI/UNI	ATM/PKT	Figure 6-5
0 10 000	E3 G.751	HDB3/AMI/UNI	ATM/PKT	Figure 6-1
0 10 001	E3 G.751 – OHM	UNI	ATM/PKT	Figure 6-2
0 10 010	E3 G.751 Internal Fractional	HDB3/AMI/UNI	ATM/PKT	Figure 6-3
0 10 011	E3 G.751 External Fractional	HDB3/AMI/UNI	ATM/PKT	Figure 6-4
0 10 100	E3 G.751 PLCP	HDB3/AMI/UNI	ATM	Figure 6-6
0 10 101	E3 G.751 PLCP – OHM	UNI	ATM	Figure 6-7
0 10 110	E3 G.751 Flexible Fractional	HDB3/AMI/UNI	ATM/PKT	Figure 6-5
0 11 000	E3 G.832	HDB3/AMI/UNI	ATM/PKT	Figure 6-1
0 11 001	E3 G.832- OHM	UNI	ATM/PKT	Figure 6-2
0 11 010	E3 G.832 Internal Fractional	HDB3/AMI/UNI	ATM/PKT	Figure 6-3
0 11 011	E3 G.832 External Fractional	HDB3/AMI/UNI	ATM/PKT	Figure 6-4
0 11 100	Reserved			
0 11 101	Reserved			
0 11 110	E3 G.832 Flexible Fractional	HDB3/AMI/UNI	ATM/PKT	Figure 6-5
1 00 0X0	DS3 Clear Channel	B3ZS/AMI/UNI	ATM/PKT	Figure 6-8
1 00 001	DS3 Clear Channel—OHM	UNI	ATM/PKT	Figure 6-9
1 00 011	DS3 Clear Channel—OHM Octet Aligned	UNI	ATM/PKT	Figure 6-10
1 01 0X0	STS-1 Clear Channel	B3ZS/AMI/UNI	ATM/PKT	Figure 6-8
1 01 001	STS-1 Clear Channel—OHM	UNI	ATM/PKT	Figure 6-9
1 01 011	STS-1 Clear Channel—OHM Octet Aligned	UNI	ATM/PKT	Figure 6-10
1 1X 0X0	E3 Clear Channel	HDB3/AMI/UNI	ATM/PKT	Figure 6-8
1 1X 001	E3 Clear Channel —OHM	UNI	ATM/PKT	Figure 6-9
1 1X 011	E3 Clear Channel—OHM Octet Aligned	UNI	ATM/PKT	Figure 6-10

10.5.11 Mapping Modes

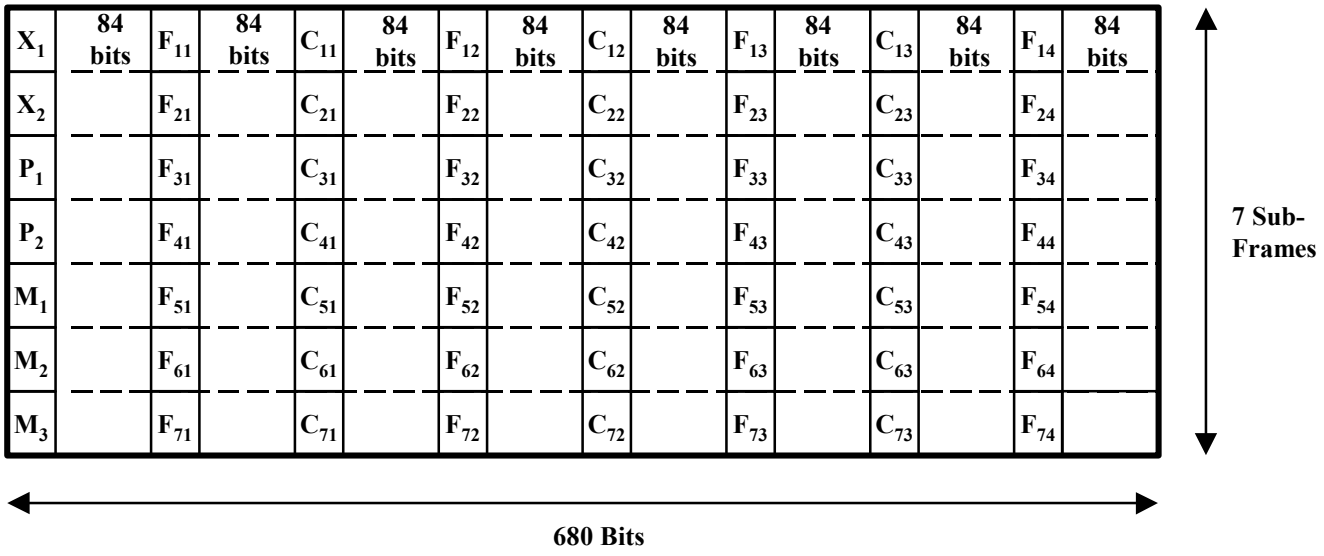
Cells and packets are mapped into various internally generated frame structures or mapped with no framing or mapped into an externally generated frame structure. When ATM cells are mapped into an internally generated frame structure they are either directly mapped into a DS3 or E3 frame or they are mapped into a PLCP frame and then the PLCP frame is mapped into a DS3 or E3 frame. ATM cells are always delineated using bit-by-bit HEC searching except when byte aligned OHM modes are used, then HEC is searched for byte-by-byte. HDLC packets are always use the bit stuffing protocol searching bit-by-bit except when byte aligned OHM modes are used, then they use the byte stuffing protocol. PLCP framing is always searched for bit-by-bit.

The following sections give examples of the major framed mapping configurations:

10.5.11.1 DS3 C-bit or DS3 M23 (with C-bit generation) Direct and PLCP Mapping

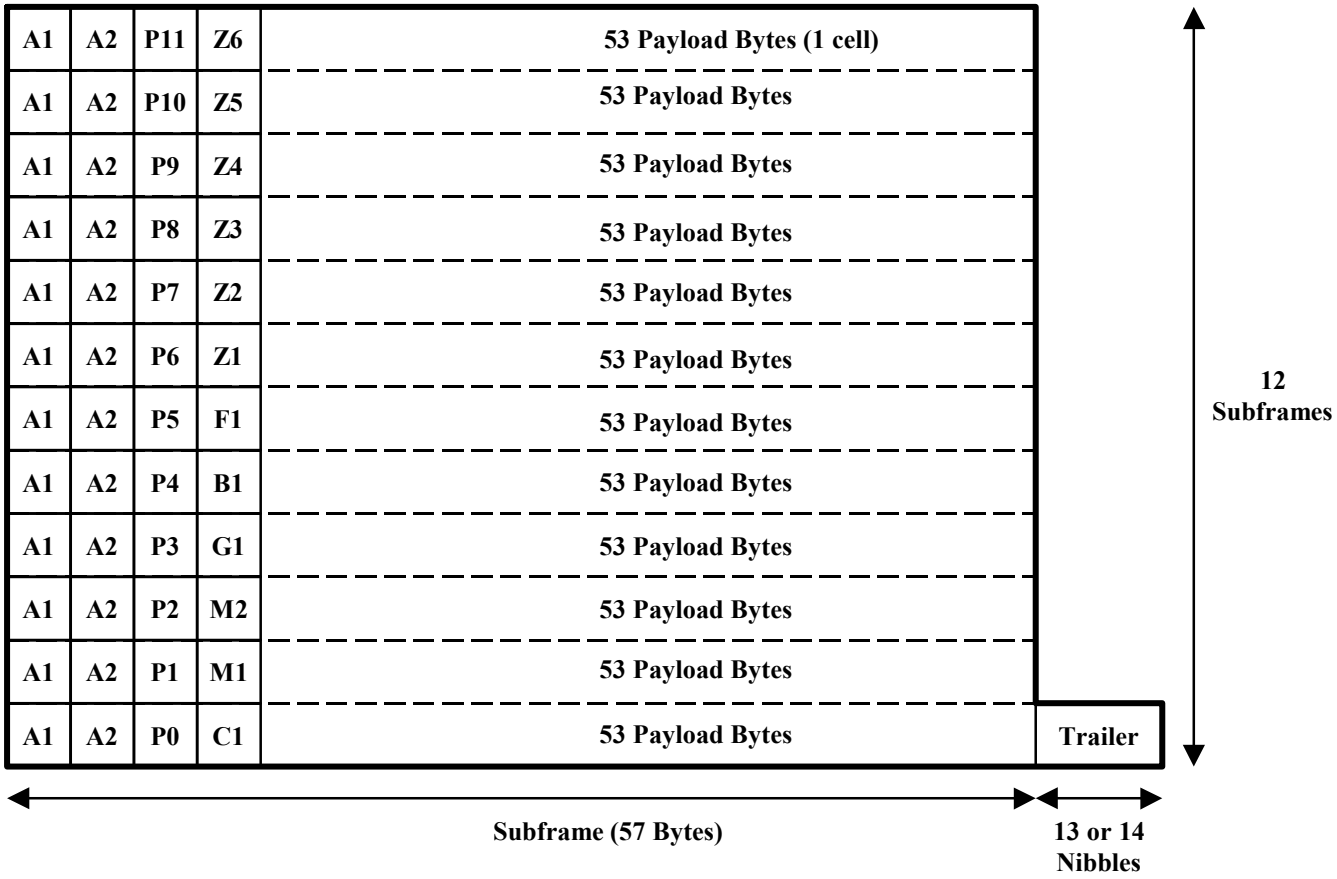
For direct mapping into DS3 C-bit and DS3 M23 (with C-bit generation) frames, ATM cells are nibble aligned or bit aligned, HDLC packets are always bit aligned. For PLCP mapping into DS3 C-bit and DS3 M23 (with C-bit generation) frames, the PLCP frame is always nibble aligned. The ATM cell nibble/bit alignment is controlled with the NAD bit in the PORT.CR1 register.

Figure 10-11. DS3 C-bit or DS3 M23 (with C-bit generation) Frame



In DS3 PLCP framing, the ATM cell is always cell aligned into the PLCP frame, HDLC packets can not be mapped into PLCP frames. The DS3 PLCP frame can only be mapped into a DS3 C-bit frame or DS3 M23 (with generated C-bits) frame. The NAD control bit is ignored.

Figure 10-12. DS3 PLCP Frame

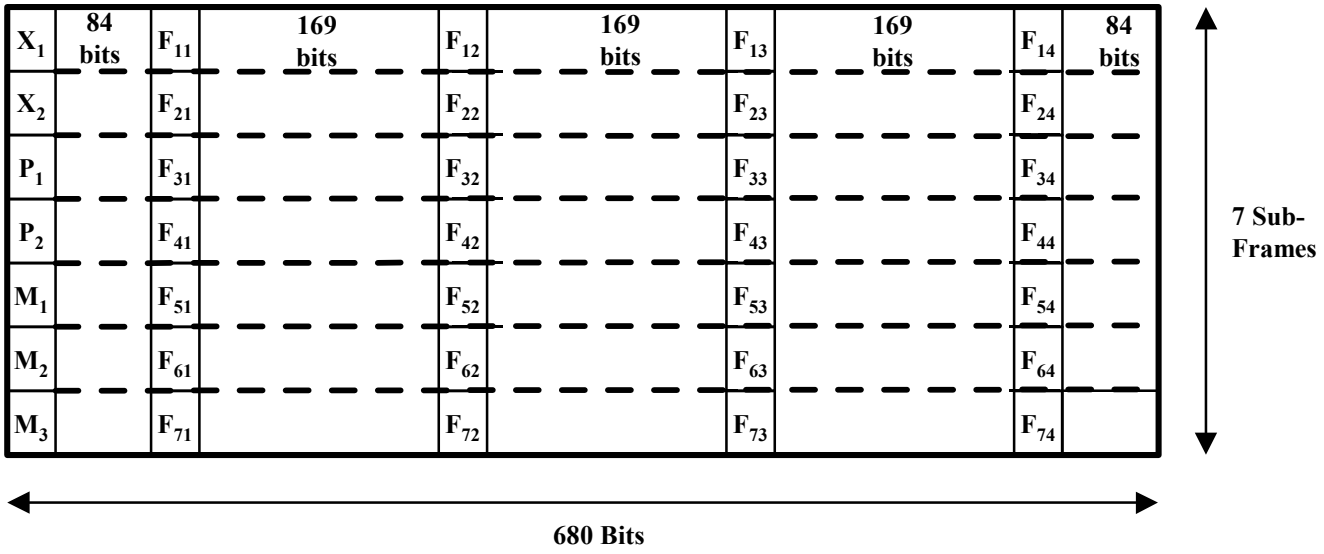


10.5.11.2 DS3 M23 (with C-bits used as payload) Direct Mapping

For direct mapping into DS3 M23 (with the C-bits used as payload) frames, ATM cells must be bit aligned, HDLC packets are always bit aligned. The NAD bit must be set to one in this mode when direct mapping ATM cells into DS3 M23 (with the C-bits used as payload) frames.

NOTE: PLCP mapping into DS3 M23 (with the C-bits used as payload) frames will not operate correctly.

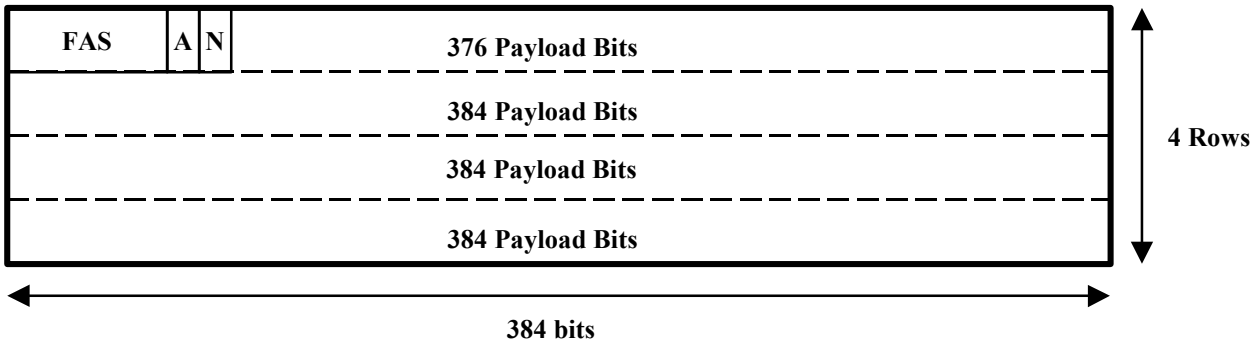
Figure 10-13. DS3 M23 (with C-bits used as payload) Frame



10.5.11.3 E3 G.751 Direct and PLCP Mapping

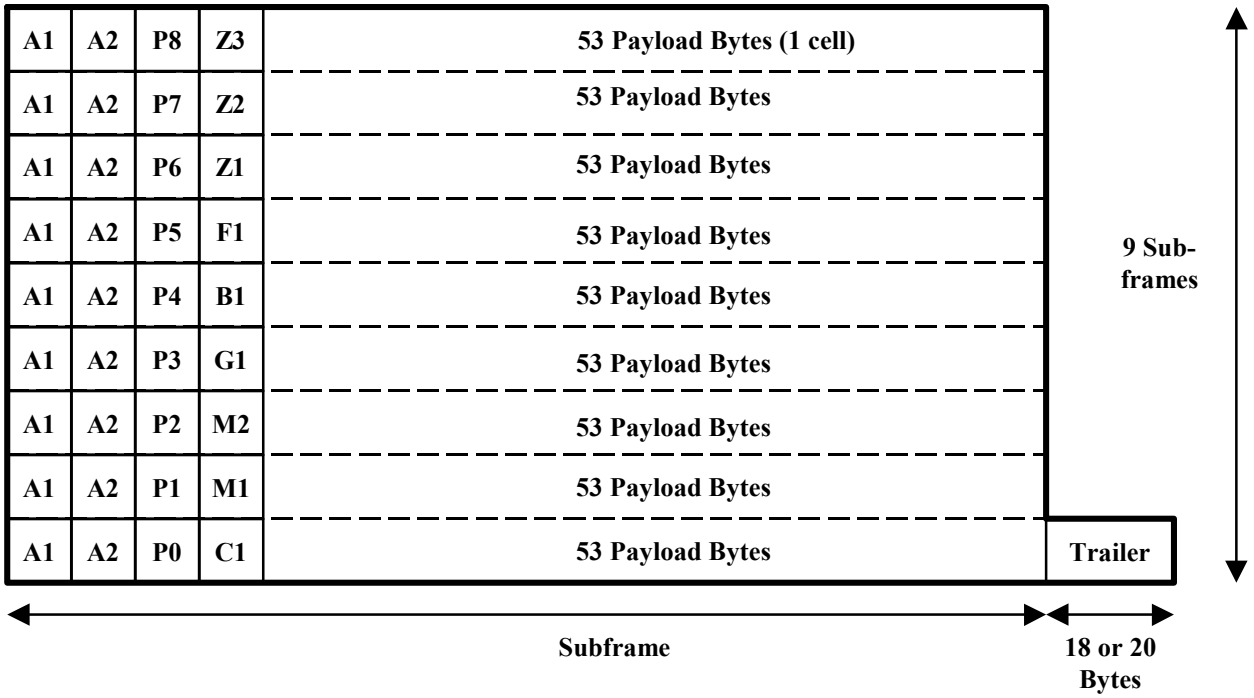
For direct mapping into E3 G.751 frames, ATM cells and HDLC packets are bit aligned. ATM cells can also be PLCP mapped to the E3 G.751 frame. When E3 PLCP mapping is used, the first four bits of the payload (E3 frame bits 13,14,15 and 16) are forced to be 1100 and the rest of the payload is used for the PLCP frame which is transmitted byte aligned and the NAD bit is ignored.

Figure 10-14. E3 G.751 Frame



In E3 PLCP framing, the ATM cell is always cell aligned into the PLCP frame, HDLC packets can not be mapped into PLCP frames. The E3 PLCP frame can only be mapped into a E3 G.751 frame. The NAD control bit is ignored.

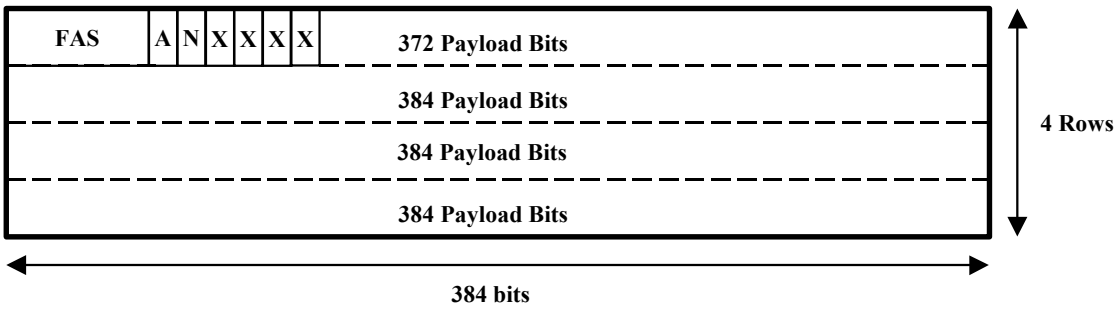
Figure 10-15. E3 PLCP Frame



10.5.11.4 Example E3 G.751 Internal Fractional Mapping

The example E3 G.751 internal fractional mapping shown in Figure 10-16 is accomplished using the internal fractional block. The first four bits of the E3. G.751 payload is designated fractional overhead This is done by setting Section A (FRAC.TDASR) register of the fractional block to be overhead and setting its size to be four bits. The data group size (FRAC.TDGSR) register should be set to the length of the normal payload (1524) or any number greater than that. The four bits of fractional overhead (E3 frame bits 13,14,15 and 16) can be set to all ones, all zeros, or a 1010 pattern. Both ATM cell and HDLC packet mapping in this mode is bit aligned. The NAD bit is ignored.

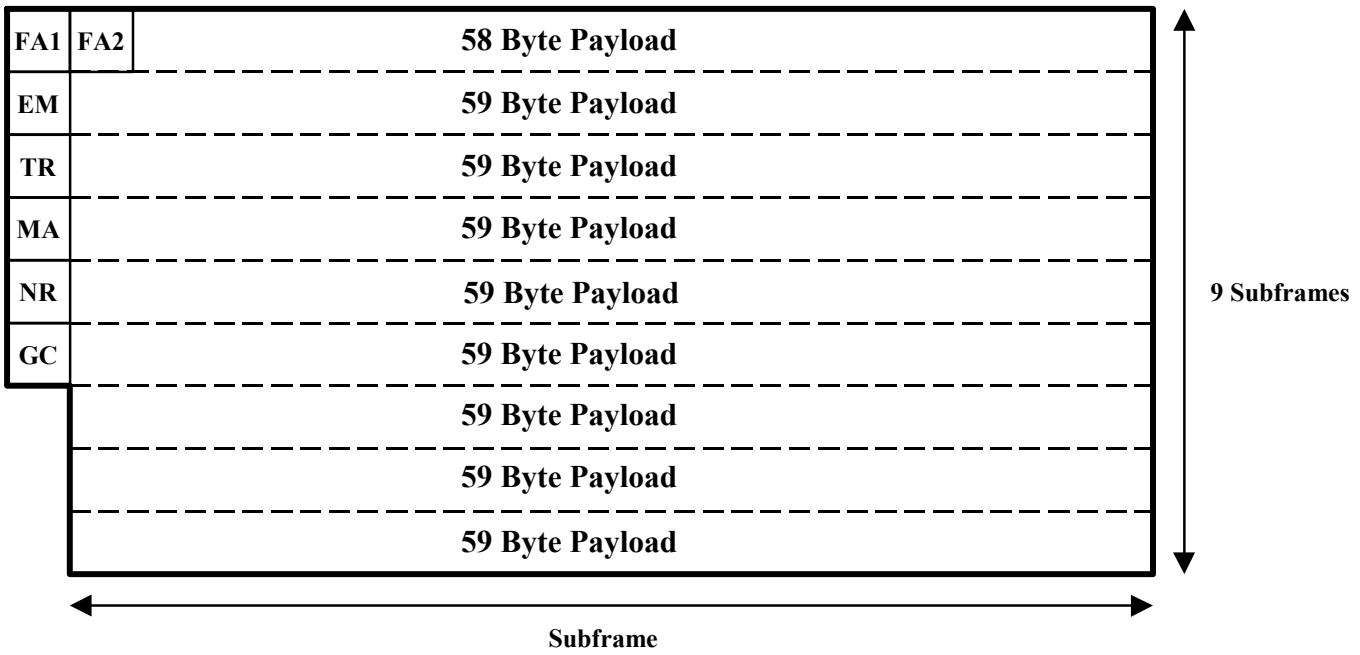
Figure 10-16. Example E3 G.751 Internal Fractional Frame



10.5.11.5 E3 G.832 Direct Mapping

For mapping into E3 G.832 frames ATM cells are byte aligned or bit aligned, HDLC packets are always bit aligned. The ATM cell byte/bit alignment is controlled with the NAD bit in the PORT.CR1 register. The NAD bit is ignored when HDLC packets are mapped into the E3 G.832 frame.

Figure 10-17. E3 G.832 Frame



10.5.12 Line Interface Modes

The line interface modes can be selected semi-independently of the framing modes using the *PORT.CR2*.LM control bit. The major block enabled is the line encoder/decoder block. The line encoder/decoder is used for B3ZS, HDB3 and AMI line interface encoding modes. The line encoder/decoder block is not used for line encoding or decoding in the UNI mode but the BPV counter in it can be used to count external pulses on the RNEGn / RCLVn / ROHMn pin. In “OHM” modes, the line encoder-decoder does not count pulses on the RNEGn / RLCVn / ROHMn pin.

The line codes are determined by the framing mode and the TZCDS and RZCDS bits, which control the AMI line mode selection bits in the line encoder/decoder blocks. The DS3 and CC52 framing modes select the B3ZS line coding, the E3 framing modes select the HDB3 line codes. Refer to Table 10-31 for configuration.

Table 10-31. Line Mode Select Bits - LM

LINE.TCR.**TZSD** & LINE.RCR.**RZSD**	**LM** (PORT.CR2)	**Line Code**
0	0	B3ZS/HDB3
1	0	AMI
X	1	UNI

10.6 UTOPIA/POS-PHY/SPI-3 System Interface

10.6.1 General Description

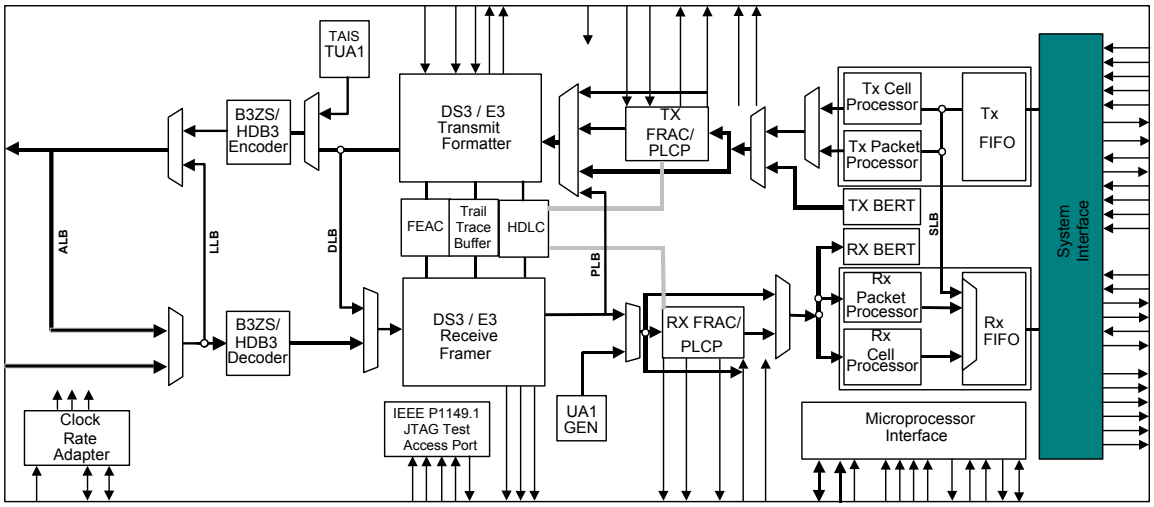
The UTOPIA/POS-PHY system interface transports ATM cells or HDLC packets between the DS316x and an ATM or Link Layer device. In UTOPIA mode, the DS316x is connected to an ATM layer device and cells are transported via a UTOPIA L2 or UTOPIA L3 Bus. In POS-PHY packet mode, the DS316x is connected to a Link Layer device and the packets are transported via a POS-PHY L2 or a POS-PHY L3 (or SPI-3) Bus. In POS-PHY cell mode, the DS316x is connected to an ATM layer device and cells are transported via a POS-PHY L2 or a POS-PHY L3 (or SPI-3) Bus. The system interface supports 8-bit, 16-bit, or 32-bit transfers at a rate of 66 MHz or less.

The receive direction removes cell/packet data for each port from the FIFO, and outputs the cell/packet data to the ATM/Link Layer device via the system interface.

The transmit direction inputs the cell/packet data from the ATM/Link Layer device via the system interface, and stores the cell/packet data for each port in the FIFO.

See Figure 10-18 for the location of the system interface block in the DS316x devices.

Figure 10-18. System Interface Functional Diagram



10.6.2 Features

- **Programmable system interface type** – When performing cell mapping/demapping, the system interface can be programmed as a UTOPIA Level 2 Bus, a UTOPIA Level 3 Bus, a POS-PHY Level 2 Bus, or a POS-PHY Level 3 (or SPI-3) Bus. When performing packet mapping/demapping, the system interface can be programmed as a POS-PHY Level 2 Bus or a POS-PHY Level 3 (or SPI-3) Bus.
- **Selectable system interface bus width** – The data bus can be a 32-bit, 16-bit, or 8-bit bus at operations speeds up to 66 MHz.
- **Supports multiple ports on the system interface** – Each line has its own port address for access via the system interface.
- **Supports per port system loopback** – Each port can be placed in system loopback which causes cells/packets from the transmit FIFO to be looped back to the receive FIFO.
- **System interface byte reordering** – In 16-bit and 32-bit modes, the received/transmitted order of the bytes transferred across the system interface is programmable, i.e., the first byte received/transmitted by ATM cell / packet processing can be transferred in [31:24] ([15:8]) or [7:0].

10.6.6 System Interface Bus Controller

The Transmit and Receive System Interface Bus Controller can be programmed to operate as a UTOPIA Level 2, UTOPIA Level 3, POS-PHY Level 2, or POS-PHY Level 3 (or SPI-3) bus controller. It controls the system interface bus timing and provides a common interface to the Transmit and Receive FIFO for FIFO status polling and cell/packet data transfer. Normally, the first byte transmitted is transferred across the system interface as the most significant byte (TDATA[31:24] in 32-bit mode or TDATA[15:8] in 16-bit mode). If byte reordering is enabled, the first byte transmitted is transferred across the system interface as the least significant byte (TDATA[7:0]).On the receive side, the first byte received is transferred across the system interface as the most significant byte (RDATA[31:24] in 32-bit mode or RDATA[15:8] in 16-bit mode). If byte reordering is enabled, the first byte received is transferred across the system interface as the least significant byte (RDATA[7:0]).

See Figure 10-19, Figure 10-20, Figure 10-21, and Figure 10-22. Byte reordering is ignored in 8-bit mode.

Figure 10-19. Normal Packet Format in 32-Bit Mode

Bit 31			Bit 0	
Byte 1	Byte 2	Byte 3	Byte 4	1st Transfer
Byte 5	Byte 6	Byte 7	Byte 8	2nd Transfer
• • •	• • •	• • •	• • •	
Byte 4n-7	Byte 4n-6	Byte 4n-5	Byte 4n-4	(n-1)th Transfer
Byte 4n-3	Byte 4n-2	Byte 4n-1	Byte 4n	nth Transfer

Figure 10-20. Normal Packet Format in 16-Bit Mode

Bit 15	Bit 0	
Byte 1	Byte 2	1st Transfer
Byte 3	Byte 4	2nd Transfer
• • •	• • •	
Byte 2n-3	Byte 2n-2	(n-1)th Transfer
Byte 2n-1	Byte 2n	nth Transfer

Figure 10-21. Byte Reordered Packet Format in 32-Bit Mode

Bit 31			Bit 0	
Byte 4	Byte 3	Byte 2	Byte 1	1st Transfer
Byte 8	Byte 7	Byte 6	Byte 5	2nd Transfer
• • •	• • •	• • •	• • •	
Byte 4n-4	Byte 4n-5	Byte 4n-6	Byte 4n-7	(n-1)th Transfer
Byte 4n	Byte 4n-1	Byte 4n-2	Byte 4n-3	nth Transfer

Figure 10-22. Byte Reordered Packet Format in 16-Bit Mode

Bit 15	Bit 0	
Byte 2	Byte 1	1st Transfer
Byte 4	Byte 3	2nd Transfer
•	•	
•	•	
•	•	
Byte 2n-2	Byte 2n-3	(n-1)th Transfer
Byte 2n	Byte 2n-1	nth Transfer

10.6.6.4 UTOPIA Level 2, Transmit Side

In UTOPIA Level 2, an ATM layer device pushes cells across the system interface. The ATM layer device polls the individual ports of the DS316x to determine which ports have space available for a cell, and selects a port for cell transfer. More than one PHY layer device can be present on a UTOPIA Level 2 bus. Whether or not the HEC byte is transferred with the cells is programmable.

The Transmit System Interface Bus Controller accepts a transmit clock (TSCLK), transmit address (TADR[4:0]), transmit enable ($\overline{\text{TEN}}$), and a transmit data bus consisting of transmit data (TDATA[31:0]), transmit parity (TPRTY), and transmit start of cell (TSOX). It outputs transmit direct cell available (TDXA) and transmit polled cell available (TPXA) signals. The transmit data bus is used to transfer cell data whenever one of the ports is selected for cell data transfer. TSOX is asserted during the first transfer of a cell, cell data is transferred on TDATA, and the data bus parity is indicated on TPRTY. All signals are sampled or updated using TSCLK. The TDXA and TPXA signals are used to indicate when the Transmit FIFO has space available for a programmable number of cells. There is a TDXA for each port in the device. TDXA goes high when the associated port's Transmit FIFO has more space available than a programmable number of cells. TDXA goes low when the associated port's Transmit FIFO is full (does not have space for another cell). TPXA reflects the current status of a port's TDXA signal when the port is polled. The TPXA signal is tri-stated unless one of the ports is being polled for FIFO fill status.

10.6.6.5 UTOPIA Level 3, Transmit Side

In UTOPIA Level 3, the ATM layer device pushes cells across the system interface. The ATM layer device polls the individual ports of the DS316x to determine which ports have space available for a cell, and selects a port for cell transfer. Only one PHY layer device can be present on a UTOPIA Level 3 bus. Whether or not the HEC byte is transferred with the cells is programmable.

The Transmit System Interface Bus Controller accepts a transmit clock (TSCLK), transmit address (TADR[7:0]), transmit enable ($\overline{\text{TEN}}$), and a transmit data bus consisting of transmit data (TDATA[31:0]), transmit parity (TPRTY), and transmit start of cell (TSOX). It outputs transmit direct cell available (TDXA) and transmit polled cell available (TPXA) signals. The transmit data bus is used to transfer cell data whenever one of the ports is selected for cell data transfer. TSOX is asserted during the first transfer of a cell, cell data is transferred on TDATA, and the data bus parity is indicated on TPRTY. All signals are sampled or updated using TSCLK. The TDXA and TPXA signals are used to indicate when the Transmit FIFO has space available for a programmable number of cells.

There is a TDXA for each port in the device. TDXA goes high when the associated port's Transmit FIFO has more space available than a programmable number of cells. TDXA goes low when the associated port's Transmit FIFO is full (does not have space for another cell). TPXA reflects the current status of a port's TDXA signal when the port is polled. The TPXA signal is always driven.

10.6.6.6 UTOPIA Level 2, Receive Side

In UTOPIA Level 2, the ATM layer device pulls cells across the system interface. The ATM layer device polls the individual ports to determine which ports have cells available, and selects a port for cell transfer. More than one PHY layer device can be present on a UTOPIA Level 2 bus. Whether or not the HEC byte is transferred with the cells is programmable.

The Receive System Interface Bus Controller accepts a receive clock (RSCLK), receive address (RADR[4:0]), and receive enable ($\overline{REN}$). It outputs a receive data bus consisting of receive data (RDATA[31:0]), receive parity (RPRTY), and receive start of cell (RSOX), as well as, receive direct cell available (RDXA) and receive polled cell available (RPXA) signals. The receive bus is used to transfer cell data whenever one of the ports is selected for cell data transfer. RSOX is asserted during the first transfer of a cell, cell data is transferred on RDATA, and the data bus parity is indicated on RPRTY. All signals are sampled or updated using RSCLK. The data bus is tri-stated unless $\overline{REN}$ is asserted (low) and one of the ports is selected for data transfer. The RDXA and RPXA signals are used to indicate when the Receive FIFO has a programmable number of cells available for transfer. There is an RDXA for each port in the device. RDXA goes high when the associated port's Receive FIFO contains more than a programmable number of cells. RDXA goes low when the associated port's Receive FIFO is empty (does not contain any cells). RPXA reflects the current status of a port's RDXA signal when the port is polled. The RPXA signal is tri-stated unless one of the ports is being polled for FIFO fill status.

10.6.6.2 UTOPIA Level 3, Receive Side

In UTOPIA Level 3, the ATM layer device pulls cells across the system interface. The ATM layer device polls the individual ports to determine which ports have cells available, and selects a port for cell transfer. Only one PHY layer device can be present on a UTOPIA Level 3 bus. Whether or not the HEC byte is transferred with the cells is programmable.

The Receive System Interface Bus Controller accepts a receive clock (RSCLK), receive address (RADR[7:0]), and receive enable ($\overline{REN}$). It outputs a receive data bus consisting of receive data (RDATA[31:0]), receive parity (RPRTY), and receive start of cell (RSOX), as well as, receive direct cell available (RDXA) and receive polled cell available (RPXA) signals. The receive data bus is used to transfer cell data whenever one of the ports is selected for cell data transfer. RSOX is asserted during the first transfer of a cell, cell data is transferred on RDATA, and the data bus parity is indicated on RPRTY. All signals are sampled or updated using RSCLK. The data bus is always driven. The RDXA and RPXA signals are used to indicate when the Receive FIFO has a programmable number of cells available for transfer. There is an RDXA for each port in the device. RDXA goes high when the associated port's Receive FIFO contains more than a programmable number of cells. RDXA goes low when the associated port's Receive FIFO is empty (does not contain any cell ends). RPXA reflects the current status of a port's RDXA signal when the port is polled. The RPXA signal is always driven.

10.6.6.3 POS-PHY Level 2, Transmit Side

In POS-PHY Level 2, the Link layer device pushes packets across the system interface. The Link layer device polls the individual ports of the DS316x to determine which ports have space available for packet data, and selects a port for packet data transfer. More than one PHY layer device can be present on a POS-PHY Level 2 bus.

The Transmit System Interface Bus Controller accepts a transmit clock (TSCLK), transmit address (TADR[4:0]), transmit enable ($\overline{TEN}$), and a transmit data bus consisting of transmit data (TDATA[31:0]), transmit parity (TPRTY), transmit start of packet (TSOX), transmit end of packet (TEOP), transmit error (TERR), and transmit modulus (TMOD[1:0]). It outputs transmit direct packet available (TDXA), transmit polled packet available (TPXA), and transmit selected packet available (TSPA) signals. The transmit data bus is used to transfer packet data whenever one of the ports is selected for packet data transfer. TSOX is asserted during the first transfer of a packet, TEOP is asserted during the last transfer of a packet, TERR is asserted when a packet has an error, TMOD indicates the number of bytes transferred on TDATA during the last transfer of a packet, packet data is transferred on TDATA, and the data bus parity is indicated on TPRTY. All signals are sampled and updated using TSCLK. The TDXA, TPXA, and TSPA signals are used to indicate when the Transmit FIFO has space available for a programmable number of bytes. There is a TDXA for each port in the device. TDXA goes high when the associated port's Transmit FIFO has space available for more than a programmable number of bytes. TDXA goes low when the associated port's Transmit FIFO is full. TPXA reflects the current status of a port's TDXA signal when the system interface is in polled mode. TSPA reflects the current status of a port's TDXA signal when the port is selected. The TSPA signal is tri-stated unless $\overline{TEN}$ is asserted (low) and one of the ports is selected for packet data transfer. The TPXA signal is tri-stated unless one of the ports is being polled for FIFO fill status.

10.6.6.4 POS-PHY Level 3 (or SPI-3), Transmit Side

In POS-PHY Level 3 (or SPI-3), the Link layer device pushes packets across the system interface. The Link layer device polls the individual ports of the DS316x to determine which ports have space available for packet data, and selects a port for packet data transfer. Only one PHY layer device can be present on a POS-PHY Level 3 (or SPI-3) bus.

The Transmit System Interface Bus Controller accepts a transmit clock (TSCLK), transmit enable ($\overline{\text{TEN}}$), and a transmit data bus consisting of transmit data (TDATA[31:0]), transmit parity (TPRTY), transmit start of packet (TSOX), transmit end of packet (TEOP), transmit error (TERR), transmit start of transfer (TSX), and transmit modulus (TMOD[1:0]). It outputs transmit direct packet available (TDXA), transmit polled packet available (TPXA), and transmit selected packet available (TSPA) signals. The transmit bus is used to transfer packet data whenever one of the ports is selected for packet data transfer. TSOX is asserted during the first transfer of a packet, TEOP is asserted during the last transfer of a packet, TERR is asserted when a packet has an error, TMOD indicates the number of bytes transferred on TDATA during the last transfer of a packet, TSX is asserted when the selected FIFO's port address has been placed on TDATA, packet data is transferred on TDATA, and the data bus parity is indicated on TPRTY. All signals are sampled and updated using TSCLK. The TDXA, TPXA, and TSPA signals are used to indicate when the Transmit FIFO has space available for a programmable number of bytes. There is a TDXA for each port in the device. TDXA goes high when the associated port's Transmit FIFO has space available for more than a programmable number of bytes. TDXA goes low when the associated port's Transmit FIFO is full. TPXA reflects the current status of a port's TDXA signal when the port is polled. TSPA reflects the current status of a port's TDXA signal when the port is selected. The TPXA and TSPA signals are always driven.

10.6.6.5 POS-PHY Level 2, Receive Side

In POS-PHY Level 2, the Link layer device pulls packets across the system interface. The Link layer device polls the individual ports to determine which ports have packet data available, and selects a port for packet data transfer. More than one PHY layer device can be present on a POS-PHY Level 2 bus.

The Receive System Interface Bus Controller accepts a receive clock (RSCLK), receive address (RADR[4:0]), and receive enable ($\overline{\text{REN}}$). It outputs a receive data bus consisting of receive data (RDATA[31:0]), receive parity (RPRTY), receive start of packet (RSOX), receive end of packet (REOP), receive error (RERR), receive data valid (RVAL), and receive modulus (RMOD[1:0]), as well as, a receive direct packet available (RDXA) signal and a receive polled packet available (RPXA) signal. The receive data bus is used to transfer packet data whenever one of the ports is selected for packet data transfer. RSOX is asserted during the first transfer of a packet, REOP is asserted during the last transfer of a packet, RERR is asserted when a packet has an error, RMOD indicates the number of bytes transferred on RDATA during the last transfer of a packet, RVAL is asserted when the receive data bus is valid, RDATA transfers packet data, and RPRTY indicates the data bus parity. All signals are sampled and updated using RSCLK. The RDXA and RPXA signals are used to indicate when the Receive FIFO has a programmable number of bytes or an end of packet available for transfer. There is an RDXA for each port in the device. RDXA goes high when the associated port's Receive FIFO contains more than a programmable number of bytes or an end of packet. RDXA goes low when the associated port's Receive FIFO is empty. RPXA reflects the current status of a port's RDXA signal when the port is polled. The data bus is tri-stated unless $\overline{\text{REN}}$ is asserted (low) and one of the ports is selected for packet data transfer. The RPXA signal is tri-stated unless one of the ports is being polled for FIFO fill status.

10.6.6.6 POS-PHY Level 3 (or SPI-3), Receive Side

In POS-PHY Level 3, the DS316x pushes packets across the system interface. The DS316x selects a port for packet data transfer when it has packet data available. Only one PHY layer device can be present on a POS-PHY Level 3 (or SPI-3) bus.

The Receive System Interface Bus Controller accepts a receive clock (RSCLK) and receive enable ($\overline{\text{REN}}$). It outputs a receive data bus consisting of receive data (RDATA[31:0]), receive parity (RPRTY), receive start of packet (RSOX), receive end of packet (REOP), receive error (RERR), receive data valid (RVAL), receive start of transfer (RSX), and receive modulus (RMOD[1:0]). The receive data bus is used to transfer packet data whenever one of the ports has packet data available for transfer. RSOX is asserted during the first transfer of a packet, REOP is asserted during the last transfer of a packet, RERR is asserted when a packet has an error, RMOD indicates the number of bytes transferred on RDATA during the last transfer of a packet, RSX is asserted when the Link layer port address has been placed on RDATA, RVAL is asserted when the receive data bus is valid, RDATA transfers

packet data, and RPRTY indicates the data bus parity. All signals are sampled and updated using RSCLK. The data bus is always driven.

In POS-PHY Level 3 (or SPI-3) the Receive System Interface Bus Controller determines which port to transfer data from using a round-robin arbitration scheme (the ports are checked one after another in numerical order according to their line number x. A transfer is initiated from a port when it is not almost empty (contains more data than the almost empty level or contains an end of packet). Transfer from a port is terminated when the maximum burst length has been transferred, the FIFO is emptied, or an end of packet is transferred while the Receive FIFO is almost empty (contains the same or less data than the almost empty level and does not contain an end of packet). When a transfer is terminated, a transfer is initiated from the next available port that is not almost empty. At the end of a packet or between a transfer from one port and the transfer from the next port, RVAL will go low for a programmable number of clock cycles (0-7) to allow the POS-PHY master to halt data transfer. At the end of a packet, data transfer will continue from the same port if the port is not almost empty. When the maximum burst length has been transferred, data transfer will continue from the same port if no other port has data available, and the port is not almost empty. The maximum burst length is programmable (8 – 256 bytes in four byte increments), or can be disabled.

10.7 ATM Cell / HDLC Packet Processing

10.7.1 General Description

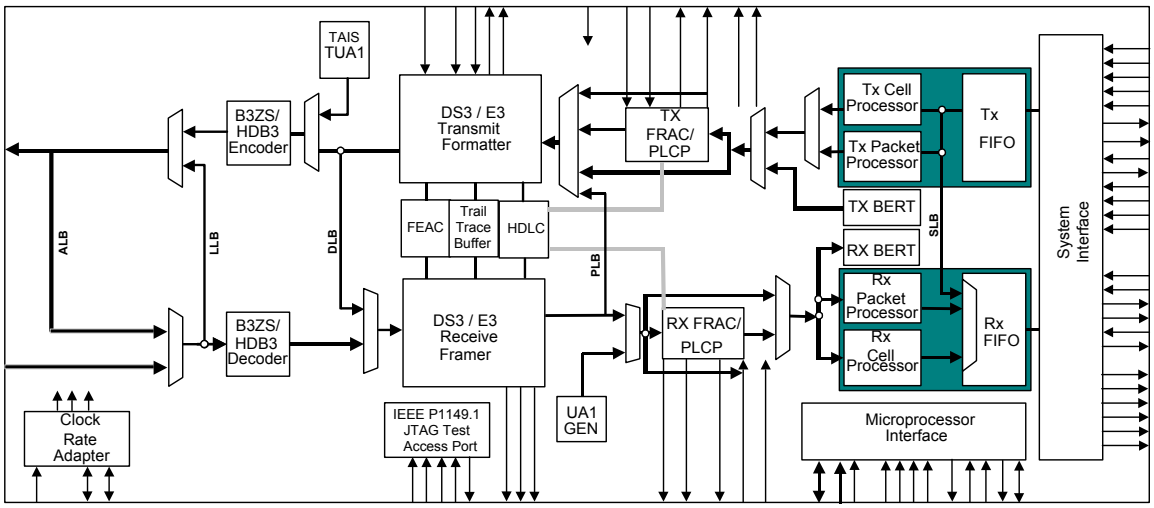
The ATM cell / packet processing de-maps the ATM cells or HDLC packets from the receive data stream and maps ATM cells or HDLC packets into the transmit data stream. ATM cell / packet processing supports any framed or unframed bit synchronous or byte synchronous (octet-aligned) data stream with a bit or byte rate of 52 MHz or less.

The receive direction extracts the payload from physical data stream, performs cell/packet processing on the individual lines, and stores the cell/packet data from each line in the FIFO.

The transmit direction removes the cell/packet data for each line from the FIFO, performs cell/packet processing for each individual line and inserts the payload into the physical data stream.

See Figure 10-23 for the location of the Cell/Packet processing block in the DS316x devices.

Figure 10-23. ATM Cell / HDLC Packet Functional Diagram



10.7.2 Features

General

- **Up to 4 data lines (ports) each with a bit or byte rate of 0–52 MHz**
- **Supports bit or byte wide, framed or unframed data lines** – Each port is programmable as bit synchronous or octet-aligned, the data stream can be framed or unframed, and the clock can be continuous or gapped.
- **Bit reordering** – The received/transmitted order of the bits as transferred across the system interface is programmable on a per port basis. i.e., In bit synchronous mode, the first bit received/transmitted by ATM cell / packet processing can be transferred in bit position 7 (31, 23, 15, or 7) or bit position 0 (24, 16, 8, or 0). In octet-aligned mode, the bit received/transmitted by ATM cell / packet processing in bit position 7 can be transferred in bit position 7 (31, 23, 15, or 7) or bit position 0 (24, 16, 8, or 0).

ATM Cell Processor

- **Programmable HEC insertion and extraction** – The transmit side can be programmed to accept cells from the system interface that do or do not contain a HEC byte. If cells are transferred without a HEC byte, the HEC byte will be computed and inserted. If cells are transferred with a HEC byte, then the transferred HEC byte can be programmed to be passed through or overwritten with a newly calculated HEC. The receive side can be programmed to send cells to the system interface that do or don't contain the HEC byte.
- **Programmable erred cell insertion** – An HEC error mask can be programmed for insertion of single or multiple errors individually or continuously at a programmable rate.

- **Programmable transmit cell synchronization** – The transmit data line can be provisioned to be bit synchronous or octet-aligned.
- **PLCP or HEC based cell delineation** – Cell delineation is determined from the PLCP frame during PLCP framing modes, and from the HEC during all other ATM modes.
- **Programmable header cell pass-through** – Receive cell filtering can pass-through only those cells that matching a programmable header value.
- **Selectable idle/unassigned/invalid/programmable header cell padding and filtering** – Transmit cell padding can be programmed for idle cell or programmable header cell padding. The padded cell payload byte contents are also programmable. Receive cell filtering can be programmed for any combination of idle cell, unassigned cell, invalid cell, or programmable header cell filtering. Or, all cell filtering can be disabled.
- **Optional header error correction** – Receive side single bit header error correction can enabled.
- **Separate corrected and uncorrected erred cell counts** – Separate counts of erred cells containing a corrected HEC error, and cells containing non-corrected HEC errors are kept.
- **Optional HEC uncorrected erred cell filtering** – Uncorrected erred cell extraction can be disabled.
- **Selectable cell scrambling/de-scrambling** – Cell scrambling and/or de-scrambling can be disabled. The scrambling can be a self-synchronous scrambler ($x^{43} + 1$) over the payload only, a self-synchronous scrambler over the entire cell, or a Distributed Sample Scrambler ($x^{31} + x^{28} + 1$).
- **Optional HEC calculation coset polynomial addition** – The performance of coset polynomial addition during HEC calculation can be disabled.

HDLC Packet Processor

- **Programmable FCS insertion and extraction** – The transmit side can be programmed to accept packets from the system interface that do or don't contain FCS bytes. If packets are transferred without FCS bytes, the FCS will be computed and appended to the packet. If packets are transferred with FCS bytes, then the FCS can be programmed to be passed through or overwritten with a newly calculated FCS. The receive side can be programmed to send packets to the system interface that do or don't contain FCS bytes.
- **Programmable transmit packet synchronization** – The transmit data line can be provisioned to be bit synchronous or octet-aligned.
- **Programmable FCS type** – The FCS can be programmed to be a 16-bit FCS or a 32-bit FCS.
- **Supports FCS error insertion** – FCS error insertion can be programmed for insertion of errors individually or continuously at a programmable rate.
- **Supports bit or byte stuffing/destuffing** – The bit or byte synchronous(octet-aligned) mode determines the bit or byte stuffing/destuffing.
- **Programmable packet size limits** – The receive side can be programmed to abort packets over a programmable maximum size or under a programmable minimum size. The maximum packet size allowed is 65,535 bytes.
- **Selectable packet scrambling/de-scrambling** – Packet scrambling and/or de-scrambling can be disabled.
- **Separate FCS erred packet and aborted packet counts** – Separate counts of aborted packets, size violation packets, and FCS erred packets are kept.
- **Optional erred packet filtering** – Erred packet extraction can be disabled
- **Programmable inter-frame fill** – The transmit inter-frame fill value is programmable.

10.7.3 Transmit Cell/Packet Processor

The Transmit Cell Processor and Transmit Packet Processor both receive the 32-bit parallel data stream from the Transmit FIFO, however, only one of the processors will be enabled. Which processor is enabled is determined by the system interface mode. In UTOPIA mode, the Transmit Cell Processor is enabled. In POS-PHY mode, if the *PORT.CR2*.PMCPE bit is low, the Transmit Packet Processor is enabled. If the *PORT.CR2*.PMCPE bit (PORT.CR2) is high, the Transmit Cell Processor is enabled.

10.7.4 Receive Cell/Packet Processor

The Receive Cell Processor and Receive Packet Processor both receive the incoming data stream from the Receive Framer (minus all overhead and stuff data), however, only one of the processors will be enabled. The other will be disabled. Which processor is enabled is determined by the system interface mode. In UTOPIA mode,

the Receive Cell Processor is enabled. In POS-PHY mode, if the *PORT.CR2*.PMCPE bit is low, the Receive Packet Processor is enabled. If the PORT.CR2.PMCPE bit is high, the Receive Cell Processor is enabled.

The bits in a byte are received MSB first, LSB last. When they are output serially, they are output MSB first, LSB last. The bits in a byte in an incoming signal are numbered in the order they are received, 1 (MSB) to 8 (LSB). However, when a byte is stored in a register, the MSB is stored in the highest numbered bit (7], and the LSB is stored in the lowest numbered bit (0). This is to differentiate between a byte in a register and the corresponding byte in a signal.

10.7.5 Cell Processor

10.7.5.1 Transmit Cell Processor

The Transmit Cell Processor accepts data from the Transmit FIFO and performs bit reordering, cell padding, HEC processing, cell error insertion, and cell scrambling. The data output from the Transmit Cell Processor can be either a serial data stream (bit synchronous mode) or an 8-bit parallel data stream (octet-aligned mode). Cell processing can be disabled (clear-channel enable). Disabling cell processing disables cell padding, HEC processing, and cell error insertion. Only bit reordering and cell scrambling are not disabled.

When cell processing is disabled, data is continually read out of the Transmit FIFO. When the Transmit FIFO is empty, the output data stream is padded with FFh until the Transmit FIFO contains more data than the "almost empty" level.

The 32-bit data words read from the Transmit FIFO are multiplexed into an 8-bit parallel data stream and passed on to bit reordering.

Bit reordering changes the bit order of each byte. If bit reordering is enabled, the incoming 8-bit data stream DT[7:0] with DT[7] being the MSB and DT[0] being the LSB is rearranged so that the MSB is in DT[0] and the LSB is in DT[7] of the outgoing data stream DT[7:0]. In bit synchronous mode, DT[7] is the first bit transmitted. If cell processing is disabled the data stream is passed on to cell scrambling, bypassing cell padding, HEC processing, and cell error insertion.

Cell padding inserts fill cells. After a cell end, fill cells are inserted into the data stream if the Transmit FIFO does not contain a complete cell. The fill cell type and fill cell payload value are programmable. The resulting data stream is passed on to HEC processing. If cell processing is disabled, cell padding will not be performed.

HEC processing calculates a HEC and inserts it into the cell. HEC calculation is a CRC-8 calculation over the four header bytes. The polynomial used is $x^8 + x^2 + x + 1$. The coset polynomial, $x^6 + x^4 + x^2 + 1$, is added (modulo 2) to the residue. The calculated HEC is then inserted into the byte immediately following the header. HEC coset polynomial addition is programmable. If the cell received from the Transmit FIFO contains a HEC byte, the received HEC byte can be passed through or overwritten with the calculated HEC byte. HEC byte pass through is programmable. If the cell received from the Transmit FIFO does not contain a HEC byte, the calculated HEC byte is inserted into the cell. If cell processing is disabled, HEC processing will not be performed.

Cell error insertion inserts errors into the HEC byte. The HEC bits to be errored are programmable. Error insertion can be controlled by a register or by the manual error insertion input (TMEI). The error insertion initiation type (register or input) is programmable. If a register controls error insertion, the number and frequency of the errors are programmable. If cell processing is disabled, cell error insertion will not be performed.

Cell scrambling can scramble the 48-byte cell payload, scramble the entire cell data stream, or scramble the data stream with a Distributed Sample Scrambler (DSS). If the payload or the entire data stream is scrambled, a self-synchronous scrambler with a generation polynomial of $x^{43} + 1$ is used. For payload scrambling, the scrambler scrambles the 48-byte payload, and does not scramble the four header or the HEC bytes. For a DSS scrambled data stream, a distributed sample scrambler with a generation polynomial of $x^{31} + x^{28} + 1$ is used for scrambling. The transmit DSS scrambler scrambles the 48-byte payload and the four byte header. It scrambles the first HEC bit (HEC[1]) with the first transmit DSS scrambler sample (the transmit DSS scrambler bit from 211 bits earlier), scrambles the second HEC bit (HEC[2]) with the second transmit DSS scrambler sample (the current transmit DSS scrambler bit), and does not scramble the remaining HEC bits (HEC[3:8]). DSS scrambling can only be performed in bit synchronous mode. Cell scrambling is programmable (payload, entire data stream, or DSS). If cell processing is disabled, the entire data stream will be scrambled whenever scrambling is enabled

Once all cell processing has been completed, in bit synchronous mode, the 8-bit parallel data stream is multiplexed into a serial data stream and passed on. In octet-aligned mode, the 8-bit parallel data stream is passed on.

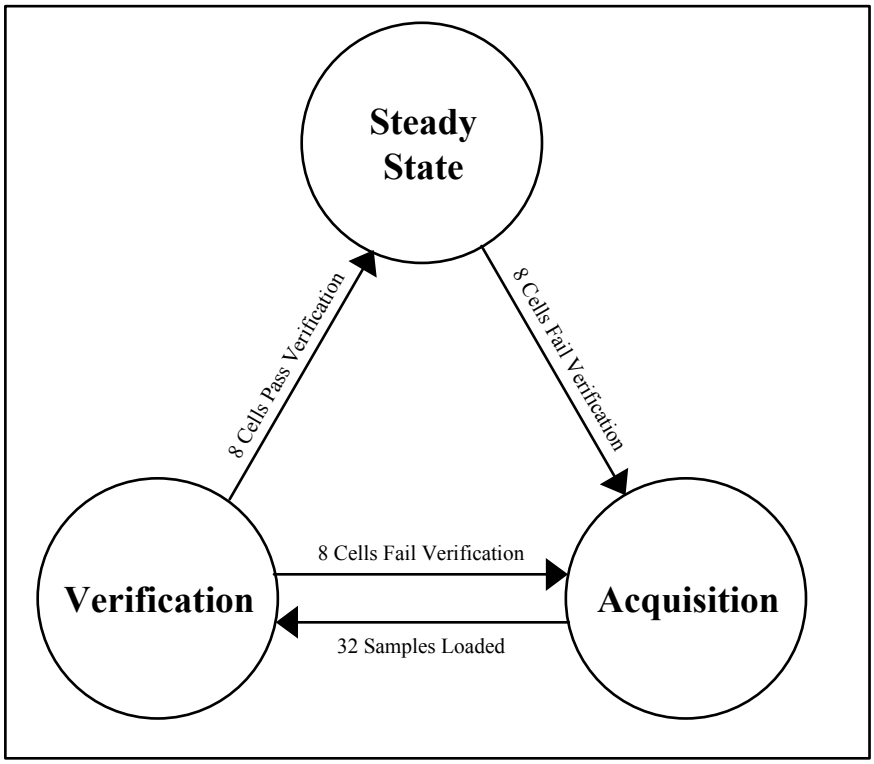
10.7.5.2 Receive Cell Processor

The Receive Cell Processor performs cell de-scrambling, cell delineation, cell filtering, header pattern comparison, OCD detection, HEC error monitoring, HEC byte filtering, and bit reordering. The data coming in can be either a serial data stream (bit synchronous mode) or an 8-bit parallel data stream (octet-aligned mode). The type of data stream received affects cell de-scrambling and cell delineation, however, it does not affect OCD detection, HEC error monitoring, cell filtering, header pattern comparison, HEC byte filtering, or bit reordering. Cell processing can be disabled (clear-channel enable). Disabling cell processing disables cell delineation, OCD detection, cell filtering, header pattern comparison, HEC error monitoring, and HEC byte filtering. Only cell de-scrambling and bit reordering are not disabled.

Cell de-scrambling can descramble the 48-byte cell payload, descramble the entire cell data stream, or descramble a data stream scrambled by a Distributed Sample Scrambler (DSS). If the payload or the entire data stream is descrambled, a self-synchronous scrambler with a generation polynomial of $x^{43} + 1$ is used for de-scrambling. Payload de-scrambling, descrambles the 48-byte payload, and does not descramble the four header bytes or the HEC byte. For a DSS scrambled data stream, a distributed sample scrambler with a generation polynomial of $x^{31} + x^{28} + 1$ is used for de-scrambling. The receive DSS scrambler is synchronized to the transmit DSS scrambler by DSS scrambler synchronization. DSS de-scrambling can only be performed in bit synchronous mode. Cell de-scrambling is programmable (payload, entire data stream, or DSS). In bit synchronous mode, de-scrambling is performed one bit at a time, and the serial data stream is demultiplexed in to an 8-bit data stream before being passed on. In octet-aligned mode, de-scrambling is performed 8-bits at a time, and only payload or entire data stream de-scrambling can be performed. When cell processing is disabled, the entire data stream will be descrambled if de-scrambling is enabled.

DSS Scrambler Synchronization synchronizes the receive DSS scrambler with the transmit DSS scrambler used to scramble the incoming data stream. The DSS Scrambler Synchronization state machine has three states: "Acquisition", "Verification", and "Steady State". The "Acquisition" state adds the transmit DSS scrambler samples from 16 incoming cells into the receive DSS scrambler (32 samples total). The samples are derived from the two MSBs (HEC[1:2]) of the incoming HEC byte. Each time the samples in a cell are loaded into the receive DSS scrambler, the confidence counter is incremented. When the confidence counter reaches 16, DSS scrambler synchronization transitions to the “Verification” state. The "Verification" state verifies the samples in the incoming cells by comparing the samples from the cell with the corresponding receive DSS scrambler bits. Each time both samples from a cell match the corresponding receive DSS scrambler bits, the confidence counter is incremented. Each time one of the samples from a cell does not match the corresponding receive DSS scrambler bit, the confidence counter is decremented if the confidence counter reaches 24, DSS scrambler synchronization transitions to the “Steady State” state. If the confidence counter reaches 8, DSS scrambler synchronization transitions to the “Acquisition” state. The "Steady State" state continues to verify the samples in the incoming cells. Each time both samples from a cell match the corresponding receive DSS scrambler bits, the confidence counter is incremented (maximum count = 24). Each time one of the samples from a cell does not match the corresponding receive DSS scrambler bit, the confidence counter is decremented. If the confidence counter reaches 16, DSS scrambler synchronization transitions to the “Acquisition” state. The DSS scrambler synchronization state diagram is shown in Figure 10-24. DSS scrambler synchronization starts in the “Acquisition” state. Note: All ATM cells are discarded during the “Acquisition” and “Verification” states.

Figure 10-24. Receive DSS Scrambler Synchronization State Diagram



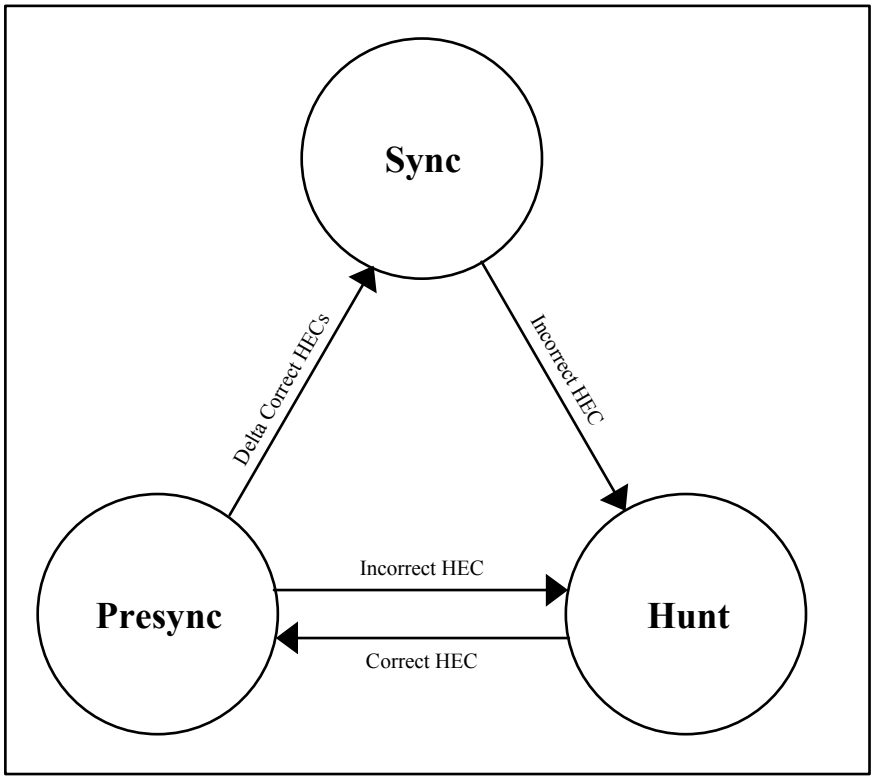
If cell processing is disabled, a cell boundary is arbitrarily chosen, and the data is divided into "cells" whose size is programmable. If HEC transfer is enabled in the receive system interface, the incoming data stream will be divided into 53-byte "cells". If HEC transfer is disabled in the receive system interface, the data is divided into 52-byte "cells". These cells are then passed on to bit reordering bypassing cell delineation, OCD detection, cell filtering, header pattern comparison, HEC error monitoring, and HEC byte filtering.

Cell delineation determines the cell boundary by identifying the header bytes and the HEC byte of a cell, and detects an out of cell delineation (OCD) condition or a change of cell delineation (COCD). Cell delineation is performed off-line, and the data path cell boundary is only updated by cell delineation if an OCD condition is present. Performing cell delineation off-line results in fewer cells being discarded when the cell boundary changes. If DSS scrambling is enabled (bit synchronous mode only), only the six least significant bits (LSBs) of the HEC (HEC[3:8]) are used for cell delineation, as the two most significant bits (MSBs) are scrambled. An OCD condition is declared if seven consecutive cells are received with incorrect HEC bytes. An OCD condition is terminated if “Delta” consecutive cells are received with correct HEC bytes, if cell delineation updates the data path cell boundary, or if the PLCP framer updates the data path cell boundary (PLCP modes only). All ATM cells are discarded during an OCD condition. A COCD is declared when Cell Delineation or the PLCP framer updates the data path cell boundary with a cell boundary that is different from the current data path cell boundary .

Cell delineation has three states: "Hunt", "Presync", and "Sync". The "Hunt" state searches for the cell boundary. Each time slot is checked for an HEC byte (six LSBs of the HEC byte if DSS is enabled). The cell boundary is set once the header and HEC bytes are identified, and cell delineation transitions to the “Presync” state. The "Presync" state verifies the cell boundary identified in the “Hunt” state. The HEC is checked in each incoming cell. If “Delta” cells (including the "Hunt" to "Presync" transition cell) with a correct HEC are received, cell delineation transitions to the “Sync” state. If a cell with an incorrect HEC is received, cell delineation transitions to the “Hunt” state. The "Sync" state checks the HEC in each cell. If a cell with a correct HEC is received, cell delineation updates the data path cell boundary if an OCD condition is present. If a cell with an incorrect HEC is received, cell delineation transitions to the “Hunt” state. The cell delineation state diagram is shown in Figure 10-25. The cell delineation process starts in the "Hunt" state. In octet-aligned mode, the HEC check is performed one byte at a time, so up to 53 checks may be needed to find the cell boundary. In bit synchronous mode, the HEC check is performed one bit at a time, so up to 424 checks may be needed to find the cell boundary. HEC calculation coset polynomial addition can be disabled. The cell delineation process can be programmed to ignore the first header byte (for DQDB applications) when calculating the HEC. If cell processing is disabled, cell delineation will not be performed. A

“Delta” of eight is used during the DS3 clear-channel, STS-1 clear-channel, and E3 clear-channel modes. A “Delta” of six is used during all other modes including the DS3 clear-channel—OHM, STS-1 clear-channel—OHM, and E3 clear-channel—OHM modes. In bit synchronous mode, the serial data stream is demultiplexed into an 8-bit parallel data stream (as determined by the data path cell boundary updated) before being passed on to cell filtering.

Figure 10-25. Cell Delineation State Diagram



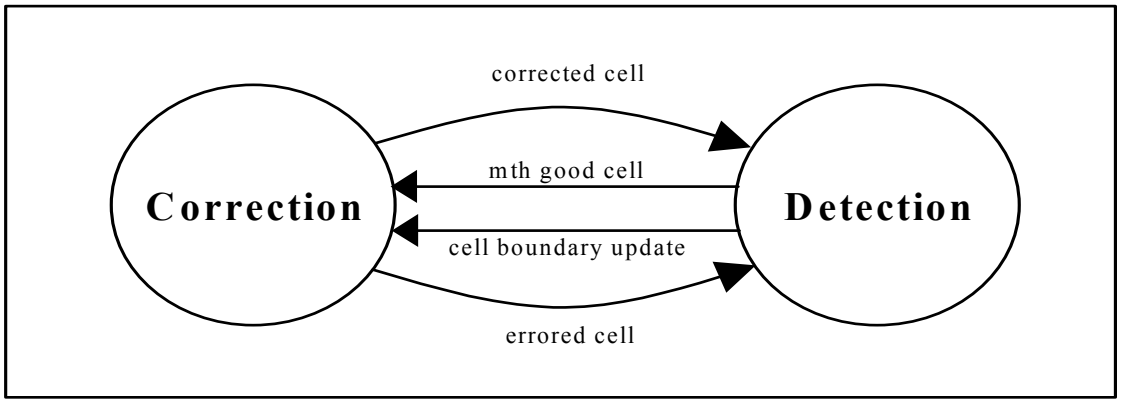
Cell filtering discards specific cell types. The 8-bit parallel data stream is monitored for idle, unassigned, and invalid cells. (Cells discarded during cell delineation or DSS de-scrambling are not monitored for cell filtering.) If cell filtering is enabled and the indicated cell type is found, the cell is discarded. Idle cell, unassigned cell, and invalid cell filtering are programmable. Idle cells have a header value of 00000000 00000000 00000000 00000001. Unassigned cells have a header value of xxxx0000 00000000 00000000 0000xxx0. Where x can be any value. Invalid cells have a header value of xxxxyyyy yyyy0000 00000000 0000xxxx. Where x can be any value, and yyyyyyyy can be any value other than 00000000. All cells discarded are counted. If cell processing is disabled, cell filtering will not be performed.

Header pattern comparison checks for a specific pattern in the header, and either discards and counts cells with a matching header (discard match), discards and counts cells without a matching header (discard no match), counts cells with a matching header (count match), or counts cells without a matching header (count no match). (Cells discarded during OCD detection, DSS de-scrambling, or cell filtering processes are not monitored for header pattern comparison.) The 8-bit parallel data stream is monitored for cells that have a header that matches the comparison header. In discard match mode, cells with a matching header are counted and discarded. In discard no match mode, cells without a matching header are counted and discarded. In count match mode, cells with a matching header are counted and passed on. In count no match mode, cells without a matching header are counted and passed on. The comparison header and comparison header pattern mode are programmable. If cell processing is disabled, header pattern comparison will not be performed.

HEC error monitoring checks the HEC and detects errored and correctable cell headers. (Cells discarded during OCD detection, DSS de-scrambling, cell filtering, or header pattern comparison are not monitored for HEC errors.). HEC Error Monitoring has two states, the "Correction" and "Detection" states. . In the “Correction” state, cells received without any header errors (good cells) are passed on. Cells received with a single header error (correctable cells) are corrected and passed on. The corrected cell count is incremented. Cells received with

multiple errors are considered errored cells. If errored cell extraction is enabled, errored cells are discarded, and the errored cell count is incremented. If errored cell extraction is disabled, errored cells are passed on. If a cell is received with an incorrect HEC, HEC error monitoring transitions to the “Detection” state. In the “Detection” state, good cells are passed on. Cells received with one or more errors are considered errored cells. If m cells are received with a correct HEC or the data path cell boundary is updated, HEC error monitoring will transition to the “Correction” state. The value of m is programmable (1, 2, 4, or 8). The HEC Error Monitoring state diagram is shown in Figure 10-26. HEC Error Monitoring starts in the “Correction” state. If header error correction is disabled, HEC error monitoring will remain in the “Detection” state. If cell processing is disabled, HEC error monitoring will not be performed.

Figure 10-26. HEC Error Monitoring State Diagram



HEC byte filtering discards the HEC byte. If HEC transfer is disabled in the receive system interface, the HEC byte is extracted from the cell and discarded. The resulting 52-byte cell is then passed on for storage in the Receive FIFO. If HEC transfer is enabled, the 53-byte cell is passed on for storage in the Receive FIFO. If cell processing is disabled, HEC byte filtering will not be performed.

Bit reordering changes the bit order of each byte. If bit reordering is enabled, the incoming 8-bit data stream DT[7:0] with DT[7] being the MSB and DT[0] being the LSB is rearranged so that the MSB is in DT[0] and the LSB is in DT[7] of the outgoing FIFO data stream DT[7:0]. In bit synchronous mode, DT[7] is the first bit received.

Once all cell processing has been completed, the 8-bit parallel data stream is demultiplexed into a 32-bit parallel data stream and passed on to the Receive FIFO. Cells are stored in the Receive FIFO in a cell format, regardless of whether or not they are transferred across a UTOPIA or POS-PHY interface. The cell format for a 53-byte cell with a 32-bit bus is shown in Figure 10-27. The cell format for a 52-byte cell with a 32-bit bus is shown in Figure 10-28.

Figure 10-27. Cell Format for 53-Byte Cell With 32-Bit Data Bus

Bit 31			Bit 0	
Header 1	Header 2	Header 3	Header 4	1st Transfer
HEC	00h	00h	00h	2nd Transfer
Payload 1	Payload 2	Payload 3	Payload 4	3rd Transfer
Payload 5	Payload 6	Payload 7	Payload 8	4th Transfer
• • •	• • •	• • •	• • •	
Payload 41	Payload 42	Payload 43	Payload 44	13th Transfer
Payload 45	Payload 46	Payload 47	Payload 48	14th Transfer

Figure 10-28. Cell Format for 52-Byte Cell With 32-Bit Data Bus

Bit 31			Bit 0	
Header 1	Header 2	Header 3	Header 4	1st Transfer
Payload 1	Payload 2	Payload 3	Payload 4	2nd Transfer
Payload 5	Payload 6	Payload 7	Payload 8	3rd Transfer
• • •	• • •	• • •	• • •	
Payload 41	Payload 42	Payload 43	Payload 44	12th Transfer
Payload 45	Payload 46	Payload 47	Payload 48	13th Transfer

10.7.6 Packet Processor

10.7.6.1 Transmit Packet Processor

The Transmit Packet Processor accepts data from the Transmit FIFO performs bit reordering, FCS processing, packet error insertion, stuffing, packet abort sequence insertion, inter-frame padding, and packet scrambling. The data output from the Transmit Packet Processor can be either a serial data stream (bit synchronous mode) or an 8-bit parallel data stream (octet-aligned mode). The type of data stream output from the Transmit Packet Processor affects stuffing, abort insertion, inter-octet padding, inter-frame padding, and packet scrambling, however, it does not affect bit reordering, FCS processing, or packet error insertion. Packet processing can be disabled (clear-channel enable). Disabling packet processing disables FCS processing, packet error insertion, stuffing, packet abort sequence insertion, and inter-frame padding. Only bit reordering and packet scrambling are not disabled.

When packet processing is disabled, data is continually read out of the Transmit FIFO. When the Transmit FIFO is read empty, the output data stream will be padded with FFh until the Transmit FIFO contains more data than the "almost empty" level. The 32-bit data words read from the Transmit FIFO are multiplexed into an 8-bit parallel data stream and passed on to bit reordering.

Bit reordering changes the bit order of each byte. If bit reordering is enabled, the incoming 8-bit data stream DT[7:0] with DT[7] being the MSB and DT[0] being the LSB is rearranged so that the MSB is in DT[0] and the LSB is in DT[7] of the outgoing data stream DT[7:0]. In bit synchronous mode, DT[7] is the first bit transmitted. If packet processing is disabled the data stream is passed on to packet scrambling, bypassing FCS processing, packet error insertion, stuffing, packet abort sequence insertion, and inter-frame padding. If packet processing is disabled in bit synchronous mode, the serial data stream is demultiplexed in to an 8-bit data stream before being passed on.

FCS processing calculates an FCS and appends it to the packet. FCS calculation is a CRC-16 or CRC-32 calculation over the entire packet. The polynomial used for FCS-16 is $x^{16} + x^{12} + x^5 + 1$. The polynomial used for FCS-32 is $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$. The FCS is inverted after calculation. The FCS type is programmable. If FCS append is enabled, the calculated FCS is appended to the packet. If FCS append is disabled, the packet is transmitted without an FCS. The FCS append mode is programmable. If packet processing is disabled, FCS processing is not performed.

Packet error insertion inserts errors into the FCS bytes. A single FCS bit is corrupted in each errored packet. The FCS bit corrupted is changed from errored packet to errored packet. Error insertion can be controlled by a register or by the manual error insertion input (TMEI). The error insertion initiation type (register or input) is programmable. If a register controls error insertion, the number and frequency of the errors are programmable. If FCS append is disabled, packet error insertion will not be performed. If packet processing is disabled, packet error insertion is not performed.

Stuffing inserts control data into the packet to prevent packet data from mimicking flags. Stuffing is performed from the beginning of a packet until the end of a packet. In bit synchronous mode, the 8-bit parallel data stream is multiplexed into a serial data stream, and bit stuffing is performed. Bit stuffing consists of inserting a '0' directly following any five contiguous '1's. In octet-aligned mode, byte stuffing is performed. Byte stuffing consists of

detecting bytes that mimic flag and escape sequence bytes (7Eh and 7Dh), and replacing the mimic bytes with an escape sequence (7Dh) followed by the mimic byte exclusive 'OR'ed with 20h. If packet processing is disabled, stuffing is not performed.

Inter-frame padding inserts start flags, end flags and inter-frame fill between packets. There will be at least one flag plus a programmable number of additional flags between packets. In octet-aligned mode, the inter-frame fill is flags. In bit synchronous mode, the inter-frame fill can be flags or all '1's followed by a start flag. If the inter-frame fill is all '1's, the number of '1's between the end and start flags may not be an integer number of bytes, however, there will be at least 15 consecutive '1's between the end and start flags. The bit synchronous mode inter-frame padding type is programmable. If packet processing is disabled, inter-frame padding is not performed.

Packet abort insertion inserts a packet abort sequences as necessary. If a packet abort indication is detected, a packet abort sequence is inserted and inter-frame padding is done until a packet start flag is detected. In bit synchronous mode, the abort sequence is FFh. In octet-aligned mode, the abort sequence is 7D7Eh. If packet processing is disabled, packet abort insertion is not performed.

The packet scrambler is a $x^{43} + 1$ selfsynchronous scrambler that scrambles the entire packet data stream. Packet scrambling is programmable.

Once all packet processing has been completed, in bit synchronous mode, the 8-bit parallel data stream is multiplexed into a serial data stream and passed on. In octet-aligned mode, the 8-bit parallel data stream is passed on.

10.7.6.2 Receive Packet Processor

The Receive Packet Processor performs packet de-scrambling, packet delineation, inter-frame fill filtering, packet abort detection, destuffing, packet size checking, FCS error monitoring, FCS byte extraction, and bit reordering. The data coming in can be either a serial data stream or an 8-bit parallel data stream, depending on the framing mode (see Table 10-30 for configuration information). The type of data stream received affects packet de-scrambling, packet delineation, inter-frame fill filtering, packet abort detection, and destuffing, however, it does not affect packet size checking, FCS error monitoring, FCS byte extraction, or bit reordering. Packet processing can be disabled (clear-channel enable). Disabling packet processing disables packet delineation, inter-frame fill filtering, packet abort detection, destuffing, packet size checking, FCS error monitoring, and FCS byte extraction. Only packet de-scrambling and bit reordering are not disabled.

The packet descrambler is a self-synchronous $x^{43} + 1$ descrambler that descrambles the entire packet data stream. Packet de-scrambling is programmable. If packet processing is disabled in bit synchronous mode, the serial data stream is demultiplexed in to an 8-bit data stream before being passed on.

If packet processing is disabled, a packet boundary is arbitrarily chosen, and the data is divided into "packets" whose size is programmable (maximum packet size setting). These packets are then passed on to bit reordering bypassing packet delineation, inter-frame fill filtering, packet abort detection, destuffing, packet size checking, FCS error monitoring, and FCS byte extraction.

Packet delineation determines the packet boundary by identifying a packet start or end flag. Each time slot is checked for a flag sequence (7Eh). Once a flag is found, it is identified as a start or end flag, and the packet boundary is set. If packet processing is disabled, packet delineation is not performed.

Inter-frame fill filtering removes the inter-frame fill between packets. When a packet end flag is detected, all data is discarded until a packet start flag is detected. In bit synchronous mode, the inter-frame fill can be flags or all '1's. When the interframe fill is all ‘1’s, the number of '1's between the start and end flags does not need to be an integer number of bytes. In bit synchronous mode when inter-frame fill is flags, there may be only one flag between packets, or the flags may have a shared zero (011111101111110). In octet-aligned mode, the inter-frame fill can only be flags, and there may be only one flag between packets. If packet processing is disabled, inter-frame fill filtering is not performed.

Packet abort detection searches for a packet abort sequence. Between a packet start flag and a packet end flag, if an abort sequence is detected, the packet is marked with an abort indication, the aborted packet count is incremented, and all subsequent data is discarded until a packet start flag is detected. In bit synchronous mode, the abort sequence is seven consecutive ones. In octet-aligned mode, the abort sequence is 7D7Eh. If packet processing is disabled, packet abort detection is not performed.

Destuffing removes the extra data inserted to prevent data from mimicking a flag or an abort sequence. In bit synchronous mode, bit destuffing is performed. Bit destuffing consists of discarding any '0' that directly follows five contiguous '1's. In octet-aligned mode, byte destuffing is performed. Byte destuffing consists of detecting an escape sequence (7Dh), discarding it, and exclusive 'OR'ing the next byte with 20h. In bit synchronous mode, after destuffing is completed, the serial bit stream is demultiplexed into an 8-bit parallel data stream and passed on to packet size checking. If there is less than eight bits in the last byte, an invalid packet flag is raised, the packet is tagged with an abort indication, and the packet size violation count is incremented. In octet-aligned mode, after destuffing is completed, the 8-bit parallel data stream is passed on to packet size checking. If packet processing is disabled, destuffing is not performed.

Packet size checking checks each packet for a programmable maximum and programmable minimum size. As the packet data comes in, the total number of bytes is counted. If the packet length is below the minimum size limit, the packet is marked with an aborted indication, and the packet size violation count is incremented. If the packet length is above the maximum size limit, the packet is marked with an aborted indication, the packet size violation count is incremented, and all packet data is discarded until a packet start is received. The minimum and maximum lengths include the FCS bytes, and are determined after destuffing has occurred. If packet processing is disabled, packet size checking is not performed.

FCS error monitoring checks the FCS and aborts errored packets. If an FCS error is detected, the FCS errored packet count is incremented and the packet is marked with an aborted indication. The FCS type (16-bit or 32-bit) is programmable. If FCS processing or packet processing is disabled, FCS byte extraction is not performed.

FCS byte extraction discards the FCS bytes. If FCS extraction is enabled, the FCS bytes are extracted from the packet and discarded. If FCS extraction is disabled, the FCS bytes are stored in the receive FIFO with the packet. If FCS processing or packet processing is disabled, FCS byte extraction is not performed.

Bit reordering changes the bit order of each byte. If bit reordering is enabled, the incoming 8-bit data stream DT[7:0] with DT[7] being the MSB and DT[0] being the LSB is rearranged so that the MSB is in DT[0] and the LSB is in DT[7] of the outgoing FIFO data stream DT[7:0]. In bit synchronous mode, DT[7] is the first bit received.

Once all packet processing has been completed, the 8-bit parallel data stream is demultiplexed into a 32-bit parallel data stream and passed on to the Receive FIFO

10.7.7 FIFO

10.7.7.1 Transmit FIFO

The Transmit FIFO block contains memory for 64 32-bit data words. The Transmit FIFO separates the transmit system interface timing from the transmit physical interface timing. The Transmit FIFO functions include filling the memory, tracking the memory fill level, maintaining the memory read and write pointers, and detecting memory overflow and underflow conditions. The number of data transfers that can occur after the Transmit FIFO "full" indication is deasserted, is programmable. The Transmit FIFO port address used for selection and polling by the Transmit System Interface Bus Controller is programmable. In system loopback, the data from the Transmit FIFO is looped back to the Receive FIFO, and a FIFO empty indication is passed on to the Transmit Cell/Packet Processor.

In cell processing mode, all operations are cell based. The Transmit FIFO is considered empty when it does not contain any data. The Transmit FIFO is considered "almost empty" when it does not contain a cell. The Transmit FIFO is considered "almost full" when it does not have space available to store a programmable number of cells. The Transmit FIFO is considered full when it does not have space available for a complete cell. When the Transmit FIFO level drops below the “almost full” indication, the TDXA[n] is asserted. The Transmit FIFO accepts cell transfers from the Transmit System Interface Bus Controller until it is full. If a start of cell is received while full, the cell is discarded and a FIFO overflow condition is declared. Once a FIFO overflow condition is declared, the Transmit FIFO will discard cell data until a start of cell is received while the FIFO has more space available than the "almost full" level. If the Transmit FIFO receives cell data other than a start of cell after a complete cell has been received, an invalid transfer is declared and all cell data is discarded until a start of cell is received. If a start of cell is received before a previous cell transfer has been completed, the current cell is discarded and a short transfer is declared. The new cell is processed normally. If the Transmit Cell Processor attempts a read while the Transmit FIFO is empty, a FIFO underflow condition is declared. Once a FIFO underflow condition is declared, the Transmit FIFO data will be discarded until a start of cell is received.

In packet processing mode, all operations are byte based. The Transmit FIFO is considered empty when its memory does not contain any data. The Transmit FIFO is considered "almost empty" when its memory does not contain a packet end and there is a programmable number of bytes or less stored in the memory. The Transmit FIFO is considered "almost full" when its memory has a programmable number of bytes or less available for storage. When the Transmit FIFO has more bytes available for storage than the “almost full” level the TDXA[n] or TPXA pin will be asserted to signal to the POS device that it is ready to receive more packet data. The Transmit FIFO is considered full when it does not have any space available for storage. When the Transmit FIFO is full, the TDXA[n] pin will be de-asserted. The Transmit FIFO accepts data from the Transmit System Interface Bus Controller until full. If a start of packet or short packet (32-bit data word with a start of packet and end of packet) is received while full, the data is discarded and a FIFO overflow condition is declared. If any other packet data is received while full, the current packet being transferred is marked with an abort indication, and a FIFO overflow condition is declared. Once a FIFO overflow condition is declared, the Transmit FIFO will discard data until a start of packet is received while the FIFO has more space available than the "almost full" level. If a packet error (a transfer with TERR and TEOP asserted) is received from the Transmit System Interface Bus Controller, an aborted transfer is declared, the data is stored in memory with a packet abort indication, and the Transmit FIFO will discard data until a start of packet is received. If an end of a packet has been received and the Transmit FIFO receives packet data other than a start of packet, an invalid transfer is declared, and all packet data is discarded until a start of packet is received. If a start of packet is received before a previous packet transfer has been completed (an end of packet was never received), the current packet being transferred is marked with an abort indication and a short transfer is declared. The new packet is processed normally. If the Transmit Packet Processor attempts a read while the Transmit FIFO is empty, a FIFO underflow condition is declared. Once a FIFO underflow condition is declared, the Transmit FIFO data will be discarded until a start of cell is received.

10.7.7.2 Receive FIFO

The Receive FIFO block contains memory for 64 32-bit data words. The Receive FIFO separates the receive system interface timing from the receive physical interface timing. The Receive FIFO functions include filling the memory, tracking the memory fill level, maintaining the memory read and write pointers, and detecting memory overflow and underflow conditions. The Receive FIFO port address used for selection and polling by the Receive System Interface Bus Controller is programmable. In system loopback, data is looped back from the Transmit FIFO to the Receive FIFO.

In cell processing mode, all operations are cell based. The Receive FIFO is considered empty unless it contains a cell. The Receive FIFO is considered "almost empty" when it contains a programmable number of cells or less. When the Receive FIFO level has more data available for transfer than the “almost empty” level, the RDXA[n] pin is asserted. The Receive FIFO is considered "almost full" when it does not have space available to store a complete cell. The Receive FIFO is considered full when it does not have any space available. The Receive FIFO accepts cell data from the Receive Cell Processor until full. If cell data is received while the FIFO is full, the cell is discarded and a FIFO overflow condition is declared. Once a FIFO overflow condition is declared, the Receive FIFO will discard cell data until a cell start is received while the FIFO has space available to store a complete cell. If the Receive System Interface Bus Controller attempts a read while the FIFO is empty, the read is ignored.

In packet processing mode, all operations are 32-bit word based. The Receive FIFO is considered empty when it does not contain any data. The Receive FIFO is considered "almost empty" when its memory does not contains a packet end and there is a programmable number of words or less stored in the memory. When the Receive FIFO has more bytes available for transfer than the “almost empty” level or has an end of packet, the RDXA[n] pin is asserted (POS-PHY Level 2). The Receive FIFO is considered "almost full" when its memory has a programmable number of words or less available for storage. The Receive FIFO is considered full when it does not have any space available for storage. The Receive FIFO accepts data from the Receive Packet Processor until full. If a packet start or short packet is received while full, the data is discarded and a FIFO overflow condition is declared. If any other packet data (packet end or middle) is received while full, the current packet being transferred is marked with an abort indication, and a memory overflow condition is declared. Once a memory overflow condition is declared, the Receive FIFO will discard data until a packet start is received while the FIFO has more space available than the "almost full" level. If the Receive System Interface Bus Controller attempts a read while the FIFO is empty, the read is ignored.

10.7.8 System Loopback

There is a system loopback available in the ATM/HDLC Mapper. The loopback can be performed on a per port basis. When a port is placed in system loopback, the data coming in from the System Interface is looped back from the Transmit FIFO to the Receive FIFO, a FIFO empty indication is passed on to the Transmit Cell/Packet Processor, and all data coming from the Receive Cell/Packet Processor is discarded. The maximum throughput of a single port is limited to half of the Receive System Interface bandwidth in 32-bit mode. A loss of data may occur if the Receive System Interface clock (RSCLK) has a frequency that is greater than one and one-half times the Transmit System Interface clock (TSCLK).

10.8 DS3/E3 PLCP Framer

10.8.1 General Description

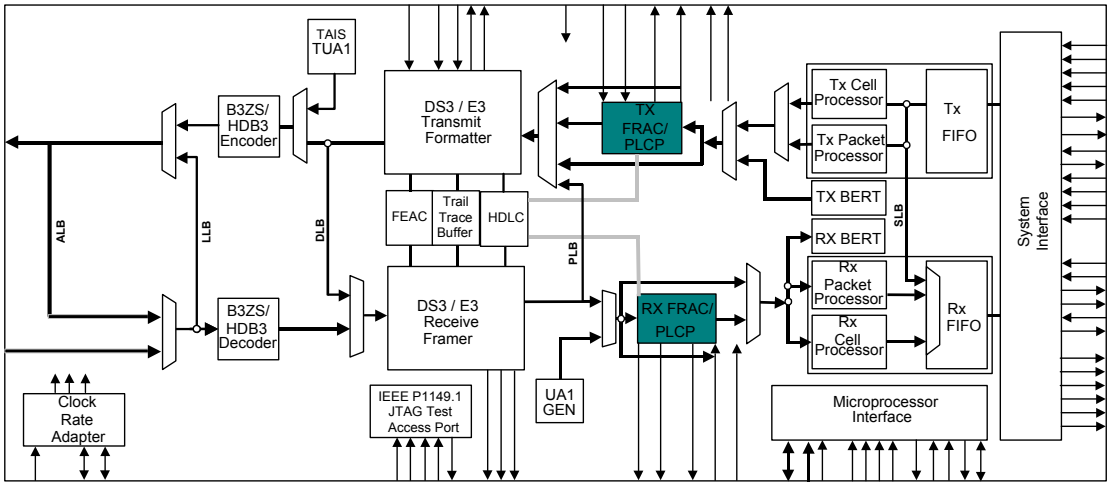
The PLCP Framer de-maps the ATM cells from the DS3/E3 PLCP data stream in the receive direction and maps ATM cells into the DS3/E3 PLCP data stream in the transmit direction.

The receive direction extracts the PLCP frame from the DS3/E3 data stream, performs frame processing, and outputs the cells with a beginning of cell indication via the payload interface.

The transmit direction inputs the cells via the payload interface, generates the frame, and inserts the PLCP frame into the DS3/E3 data stream.

See Figure 10-29 for the location of the PLCP framer in the DS316x devices.

Figure 10-29. PLCP Framer Functional Diagram



10.8.2 Features

- **DS3 PLCP frame ATM cell extraction and insertion** – Accepts a DS3 payload and performs DS3 PLCP overhead termination and generation.
- **E3 PLCP frame ATM cell extraction and insertion** – Accepts a G.751 E3 payload and performs E3 PLCP overhead termination and generation.
- **Generates and detects alarms and errors** – In the receive direction, PLCP alarm conditions (OOF, LOF, COFA, and RAI) and errors (framing, parity, and REI) are detected on the receive signal. In the transmit direction, alarm conditions and errors can be inserted into the transmit data stream.
- **Receive overhead extraction port** – Extracts all PLCP overhead from the receive signal and outputs it on a serial interface (RPOH pin).
- **Externally controlled transmit overhead insertion port** – Can insert all PLCP overhead into the transmit signal from a serial interface. Overhead insertion is fully controlled via the serial overhead interface (TPOH, TPOHEN, TPOHSOF, TPOHCLK).
- **Full Duplex serial HDLC channel extraction/insertion** – An HDLC channel can be extracted from and/or inserted into the F1, M1, M2, or M1 and M2 bytes in the PLCP data stream.
- **Full Duplex serial Trail Trace extraction/insertion** – A trail trace can be extracted from and/or inserted into the F1 byte in the PLCP data stream.

10.8.3 Transmit PLCP Frame Processor

The Transmit PLCP Frame Processor receives the ATM cells from the ATM/Packet Processor performs trailer generation, framing generation, error insertion, and overhead insertion.

The bits in a byte are transmitted MSB first, LSB last. When they are input serially, they are input in the order they are to be transmitted. The bits in a byte in an outgoing signal are numbered in the order they are transmitted, 1 (MSB) to 8 (LSB). However, when a byte is stored in a register, the MSB is stored in the highest numbered bit (7), and the LSB is stored in the lowest numbered bit (0). This is to differentiate between a byte in a register and the corresponding byte in a signal.

10.8.4 Receive PLCP Frame Processor

The Receive PLCP Frame Processor accepts the data stream from the DS3/E3 Framer and extracts the entire DS3/E3 overhead and processes only the PLCP frame data.

The bits in a byte are received MSB first, LSB last. When they are output serially, they are output in the order they are received. The bits in a byte in an incoming signal are numbered in the order they are received, 1 (MSB) to 8 (LSB). However, when a byte is stored in a register, the MSB is stored in the highest numbered bit (7), and the LSB is stored in the lowest numbered bit (0). This is to differentiate between a byte in a register and the corresponding byte in a signal.

Some bits, bit groups, or bytes (data) are integrated. Integration requires the data to have a new value for five consecutive occurrences before the new data value will be stored in the data register. Integrated data may have an associated unstable indication. Integrated data is considered unstable if for eight consecutive occurrences the received data value does not match the currently stored (integrated) data value or the previously received data value.

10.8.5 Transmit DS3 PLCP Frame Processor

The DS3 PLCP frame format is shown in Figure 10-30. A1 and A2 are the subframe alignment bytes that have a value of F6h and 28h respectively. P11 – P0 are the Path Overhead Identifier (POI) bytes that indicate the path overhead byte contained in the current subframe. Z6 – Z1 are growth bytes reserved for future use. F1 is the Path User Channel byte allocated for user communications purposes (This byte is undefined in ATM). B1 is the Bit Interleaved Parity-8 (BIP-8) byte used for PLCP path error monitoring. G1 is the PLCP Path Status Byte (See Figure 10-31) used for far-end path status and performance monitoring (bits 6 – 8 are undefined in ATM). M2 and M1 are the DQDB Layer Management Information bytes used for DQDB layer management communications (These bytes are undefined in ATM). C1 is the Cycle/Stuff Counter byte used as for PLCP superframe alignment and stuff indication.

Figure 10-30. DS3 PLCP Frame Format

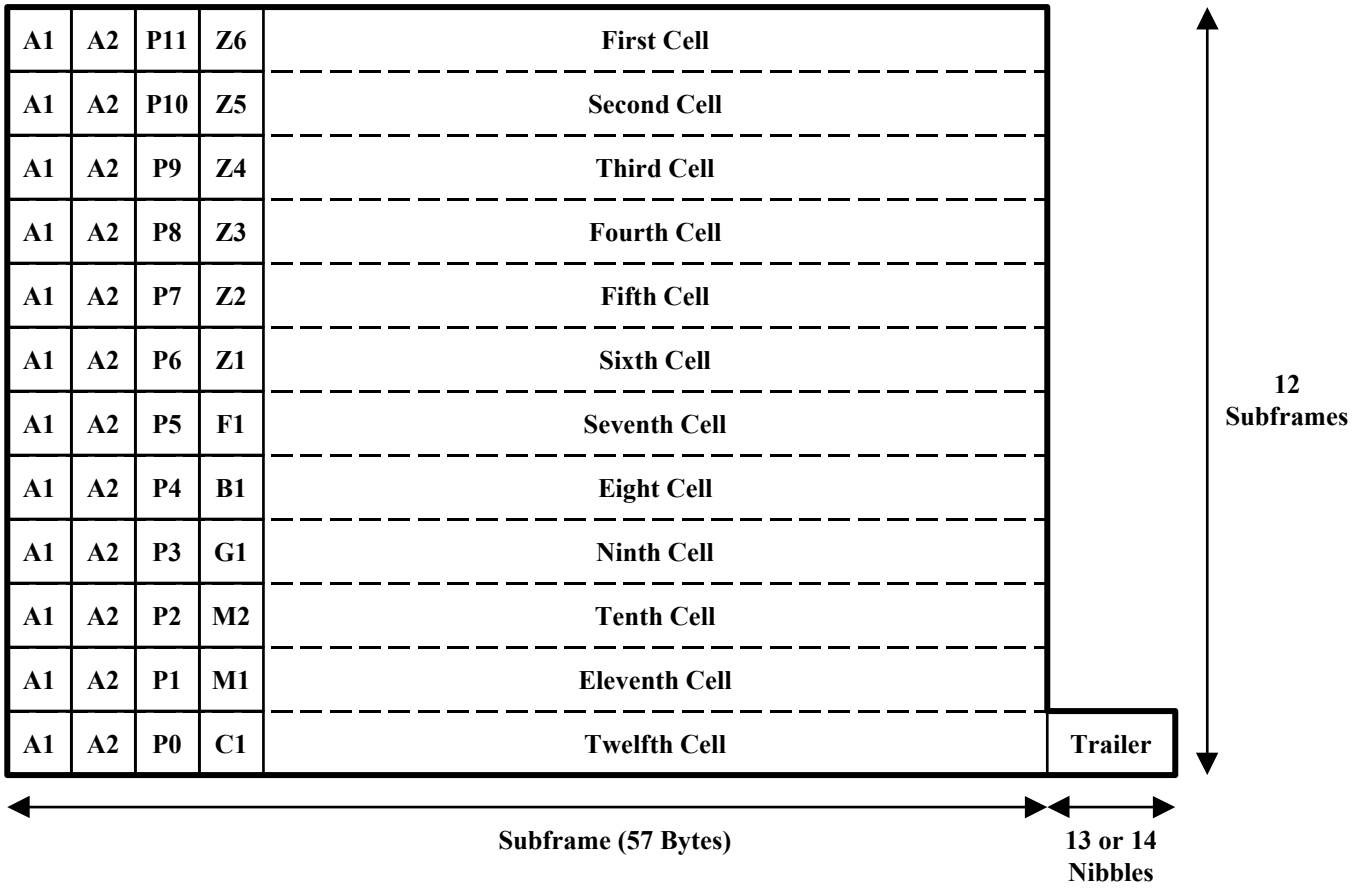
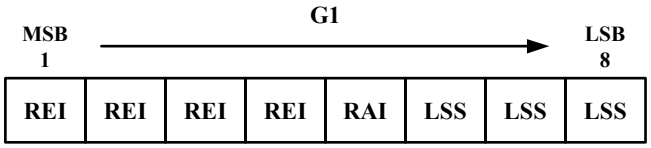


Figure 10-31. DS3 PLCP G1 Byte Format



REI - Remote Error Indicator
RAI - Remote Alarm Indicator
LSS - Link Status Signal

10.8.5.1 Transmit DS3 PLCP Trailer Generation

DS3 PLCP trailer generation inserts the DS3 PLCP frame trailer immediately following subframe 0 (POI equals 01h), and generates the C1 byte. The trailer size is determined by the DS3 PLCP superframe counter, and the 8 kHz reference clock. The DS3 PLCP superframe counter is a free running counter that indicates the current frame of the three-frame superframe. In the first frame of the superframe, the trailer size is set to thirteen, and C1 is set to FFh. In the second frame of the superframe, the trailer size is set to fourteen, and C1 is set to 00h. In the third frame of the superframe, the trailer size is variable. The trailer size is controlled by the 8 kHz reference clock. If the indicated trailer size is thirteen, C1 is set to 66h. If the indicated trailer size is fourteen, C1 is set to 99h, and the indicated number of nibbles (13 or 14) are added after subframe 0. The trailer nibbles are all set to 1100.

10.8.5.2 Transmit DS3 PLCP Frame Generation

DS3 PLCP frame generator receives the incoming PLCP payload data stream, and overwrites all of the overhead byte locations.

The first two bytes of each subframe are overwritten with the frame alignment bytes A1 and A2, which have a value of F6h and 28h respectively.

The third byte of subframe # is overwritten with POI byte # (P#). The value of P# is 00####0Pb (0 = a logic zero, #### = the hexadecimal value of #, and P = the odd parity bit).

The fourth byte of subframes #11 – 6 are overwritten with the Z6 – Z1 bytes from the corresponding registers.

The fourth byte of subframe 5 is overwritten with the F1 byte from the corresponding register, the trail trace byte input from the transmit trail trace controller, or the HDLC Overhead Processor. The F1 byte source is programmable PLCP.TCR.TF1C[1:0] (trail trace controller, HDLC, or register).

The fourth byte of subframe 4 is overwritten with the calculated BIP-8. The BIP-8 is calculated over all of the path overhead bytes and cell bytes of the previous frame after all PLCP processing (frame generation, error insertion, and overhead insertion) has been completed.

The first four bits of the fourth byte of subframe 3 are overwritten with the G1 byte REI bits (G1[1:4]). The Remote Error Indication (REI) bits can be generated automatically or inserted from the G1 register bits. The REI source is programmable (auto or register). If the REI bits are generated automatically, they are set to zero when the receive side B1 byte exactly matches the BIP-8 calculated for the previous receives side frame. Otherwise, the REI is set to a value of one to eight to indicate the number of parity errors (BIP-8 errors) detected in the receive PLCP frame (B1 byte).

The fifth bit of the fourth byte of subframe 3 is overwritten with the G1 byte RAI bit (G1[5]). The Remote Alarm Indication (RAI) bit is sourced from a register.

The last three bits of the fourth byte of subframe 3 are overwritten with the G1 byte LSS bits (G1[6:8]). The Link Status Signal (LSS) bits are sourced from a register. The three register bits are inserted in the sixth, seventh, and eighth bits of the G1 byte in each frame.

The fourth byte of subframes 2 and 1 are overwritten with the M2 and M1 bytes respectively. Each byte can be individually sourced from a register, or from the transmit HDLC controller. The M2 byte and M1 byte sources are each programmable (register or HDLC). If both bytes are programmed to be sourced from the transmit HDLC controller, they are concatenated as a single data link as opposed to two separate data links.

The fourth byte of subframe 0 is overwritten with the C1 byte created during trailer generation.

Once all of the overhead bytes have been overwritten, the data stream is passed on to error insertion.

10.8.5.3 Transmit DS3 PLCP Error Insertion

Error insertion inserts various types of errors into the different overhead bytes. The types of errors that can be inserted are framing errors, BIP-8 parity errors, and Remote Error Indication (REI) errors.

The type of framing error(s) inserted is programmable (frame bit error or framing byte error). A framing bit error is a single bit error in a frame alignment byte (A1 or A2) or POI byte (P#). A framing byte error is an error in all eight bits of a frame alignment byte (A1 or A2) or path overhead indicator (POI) byte (P#). Framing error(s) can be inserted one error at a time, or in two consecutive bytes (A1 & A2 or P# & P#+1). The framing error insertion rate (single A1 or A2, single P#, A1 & A2, or P# & P#+1) is programmable.

The type of BIP-8 error(s) inserted is programmable (errored BIP-8 bit, or errored BIP-8 byte). An errored BIP-8 bit is inverting a single bit error in the B1 byte. An errored BIP-8 byte is inverting all eight bits in the B1 byte. BIP-8 error(s) can be inserted one error at a time, or continuously. The BIP-8 error insertion rate (single or continuous) is programmable.

The type of REI error(s) inserted is programmable (single REI error or eight REI errors). A single REI error is generated by setting the first four bits of the G1 byte to a value of 1h. Eight REI errors are generated by setting the first four bits of the G1 byte to a value of 8h. REI error(s) can be inserted one error at a time, or continuously. The REI error insertion rate (single or continuous) is programmable.

Error insertion can be initiated by a register bit (*PLCP.TEIR*.TSEI) or initiated by the manual error insertion input (TMEI). Each error type is individually enabled by a register bit. The error insertion initiation type (register or input) is programmable. Once all error insertion has been performed, the data stream is passed on to overhead insertion.

10.8.5.4 Transmit DS3 PLCP Overhead Insertion

Overhead insertion can insert any (or all) of the path overhead bytes into the DS3 PLCP frame. The overhead bytes Z6 – Z1, F1, B1, G1, M1, M2, and C1 can be sourced from the transmit overhead interface (TPOHCLK, TPOH, TPOHEN, and TPOHSOF). The B1 and C1 bytes are sourced as error masks (modulo 2 addition of the input B1/C1 byte and the generated B1/C1 byte). The overhead insertion is fully controlled by the transmit overhead interface. If the transmit PLCP overhead data enable signal (TPOHEN) is driven high, then the bit on the transmit PLCP overhead signal (TPOH) is inserted into the output data stream. Insertion of bits using the TPOH signal overwrites internal overhead insertion.

10.8.6 Receive DS3 PLCP Frame Processor

The DS3 PLCP frame format is shown in Figure 10-30. A1 and A2 are the subframe Alignment bytes that have a value of F6h and 28h respectively. P11 – P0 are the Path Overhead Identifier (POI) bytes that indicate the path overhead byte contained in the current subframe. Z6 – Z1 are growth bytes reserved for future use. F1 is the Path User Channel byte allocated for user communications purposes (This byte is undefined in ATM). B1 is the Bit Interleaved Parity-8 (BIP-8) byte used for PLCP path error monitoring. G1 is the PLCP Path Status Byte (See Figure 10-31) used for far-end path status and performance monitoring (bits 6 – 8 are undefined in ATM). M1 and M2 are the DQDB Layer Management Information bytes used for DQDB layer management communications (These bytes are undefined in ATM). C1 is the Cycle/Stuff Counter byte used as for PLCP superframe alignment and stuff indication.

10.8.6.1 Receive DS3 PLCP Framing

DS3 PLCP framing determines the DS3 PLCP frame boundary. The frame boundary is found by identifying the frame alignment bytes (A1 & A2), and the path overhead indicator (POI) byte (P#). The framer is an off-line framer that updates the data path frame counters when an out of frame (OOF) condition is present. The use of an off-line framer reduces the number of ATM cells discarded during the framing process. The framer continually searches for two consecutive sets of alignment bytes (A1 and A2), and two sequential POI bytes (P#) are identified. The data path frame counters are updated if an OOF condition is present. The maximum average reframe time is 17 μs.

10.8.6.2 Receive DS3 PLCP Nibble Destuffing

Nibble destuffing discards the DS3 PLCP frame trailer immediately following subframe 0 (POI equals 01h). The trailer size is determined by the DS3 PLCP superframe counter, and the cycle counter byte (C1). The trailer is thirteen nibbles in the first frame of the superframe (C1 equals FFh). The trailer is fourteen nibbles in the second frame of the superframe (C1 equals 00h). The trailer length is variable in the third frame of the superframe. It is thirteen nibbles if C1 equals 66h, and fourteen nibbles if C1 equals 99h. The superframe counter is updated immediately upon receiving an error free C1. In the third superframe, majority voting (5 of 8) is used to determine the trailer size. Once the trailer size has been determined, the trailer nibbles are discarded.

10.8.6.3 Receive DS3 PLCP Performance Monitoring

Performance monitoring checks the DS3 PLCP frame for errors and alarm conditions. The alarm conditions detected are OOF, LOF, COFA, and RAI. All alarm conditions are defect conditions. The PLCP Framer does not integrate alarms for failure conditions.

An Out Of Frame (OOF) condition is declared when two consecutive framing bytes (A1 and A2) or two consecutive POI bytes (P0 - P11) are erred. An OOF condition is terminated when two sequential POI bytes and two consecutive framing words (A1 and A2) are error free or the DS3 PLCP framer updates the data path frame counters.

If the Loss Of Frame (LOF) integration counter is disabled, an LOF condition is declared when an OOF condition has been continuously present for 1 ms. If the LOF integration counter is enabled, an LOF condition is declared by the LOF integration counter when the counter has been active for a total of 1 ms. The LOF integration counter is active (increments count) when an OOF condition is present, it is inactive (holds count) when an OOF condition is

absent, and it is reset when an OOF condition is continuously absent for 1 ms. An LOF condition is terminated when an OOF condition is continuously absent for 1 ms.

A Change Of Frame Alignment (COFA) is declared when the DS3 PLCP framer updates the data path frame counters with a frame alignment that is different from the current data path frame alignment.

A Remote Alarm Indication (RAI) condition is declared when ten consecutive frames are received with the RAI bit (fifth bit of G1) set to one. An RAI condition is terminated when ten consecutive frames are received with the RAI bit set to zero.

Three types of errors are accumulated, framing errors, BIP-8 errors and Remote Error Indication (REI) errors. Framing errors are determined by comparing A1, A2, and P# to their expected values. The type of framing errors accumulated is programmable (OOFs, bit, byte, or word). An OOF error increments the count whenever an OOF condition is first detected (up to 1 per 3 subframes). A bit error increments the count once for each bit in A1, each bit in A2, and each bit in P# that does not match its expected value (up to 24 per subframe). A byte error increments the count once for each A1 byte, A2 byte, and P# byte that does not match its expected value (up to 3 per subframe). A word error increments the count once for each frame alignment word (A1, A2, and P#) that does not match its expected value (up to 1 per subframe). The detection of POI byte (P#) framing errors is programmable (on or off).

BIP-8 errors are determined by calculating the BIP-8 of the current frame (path overhead and cell bytes), and comparing the calculated BIP-8 to the B1 byte in the next frame. The type of BIP-8 errors accumulated is programmable (bit or block). A bit error increments the count once for each bit in the B1 byte that does not match the corresponding bit in the calculated BIP-8 (up to 8 per frame). A block error increments the count if any bit in the B1 byte does not match the corresponding bit in the calculated BIP-8 (up to 1 per frame).

REI errors are determined by the four REI bits (first four bits of G1). The REI error count is incremented by the value of the four REI bits (up to 8 per frame). Values of 9h - Fh are treated as zero errors.

10.8.6.4 Receive DS3 PLCP Overhead Extraction

Overhead extraction extracts all of the DS3 PLCP path overhead bytes from the DS3 PLCP frame. All of the PLCP path overhead (POH) bytes (Z6 – Z1, F1, B1, G1, M2, M1, and C1) are output on the receive overhead bus (RPOHCLK, RPOH, and RPOHSOF). The B1 byte is output as an error indication (modulo 2 addition of the calculated BIP-8 and the B1 byte). In addition, the Z6 – Z1, F1, G1 (6:8), M2, and M1 bytes are integrated and stored in registers along with change indications. G1 (6:8) has an unstable indication as well. The F1 byte is sent to the receive trail trace buffer, and can also be sent to the receive HDLC controller. The M2 byte and/or M1 byte can be sent to the receive HDLC controller. The source of the data transferred to the receive HDLC controller is programmable (F1, M2, M1, or M2 & M1). If both the M2 and M1 byte are programmed to be the source for the receive HDLC controller, they are concatenated as a single data link as opposed to two separate data links.

Once all frame processing has been completed, the ATM cells are passed on to the ATM/Packet Processor with a start of cell indication.

10.8.7 Transmit E3 PLCP Frame Processor

The E3 PLCP frame format is shown in Figure 10-32. A1 and A2 are the subframe Alignment bytes that have a value of F6h and 28h respectively. P8 – P0 are the Path Overhead Identifier (POI) bytes that indicate the path overhead byte contained in the current subframe. Z3 – Z1 are growth bytes reserved for future use. F1 is the Path User Channel byte allocated for user communications purposes (This byte is undefined in ATM). B1 is the Bit Interleaved Parity-8 (BIP-8) byte used for PLCP path error monitoring. G1 is the PLCP Path Status Byte (See Figure 10-33) used for far-end path status and performance monitoring (bits 6 – 8 are undefined in ATM). M2 and M1 are the DQDB Layer Management Information bytes used for DQDB layer management communications (These bytes are undefined in ATM). C1 is the Cycle/Stuff Counter byte used as for stuff indication.

Figure 10-32. E3 PLCP Frame Format

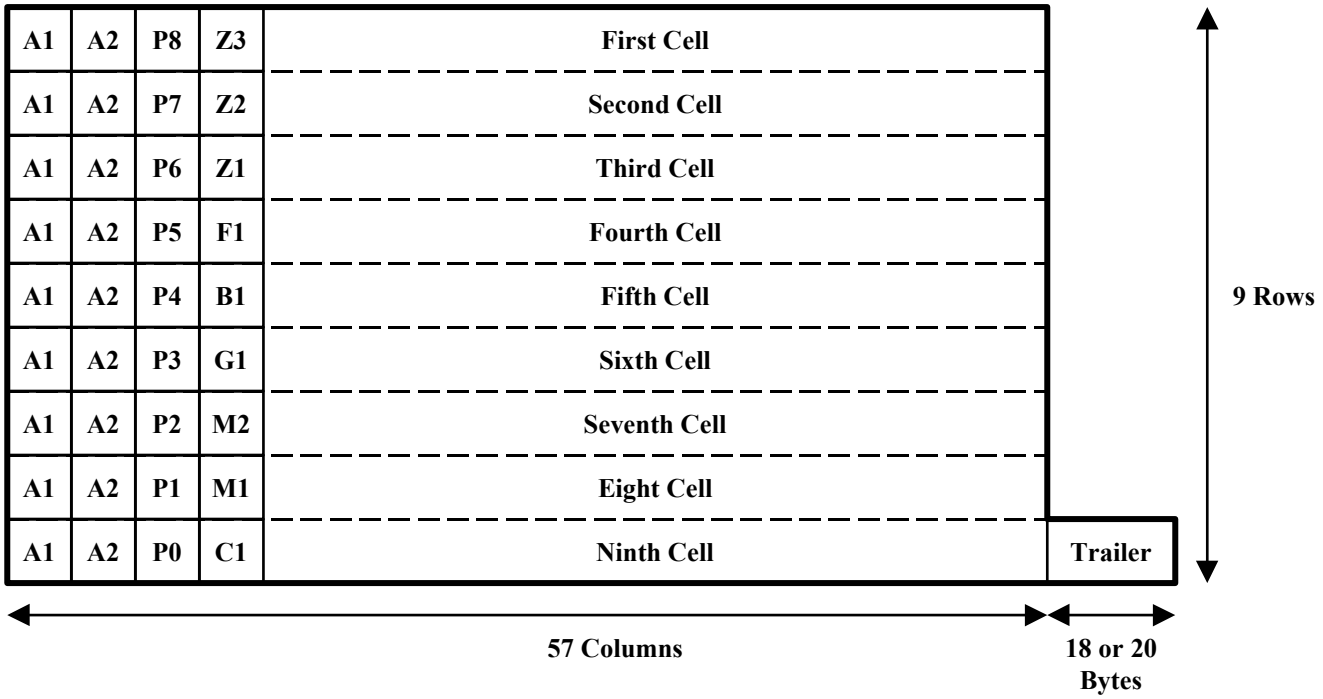
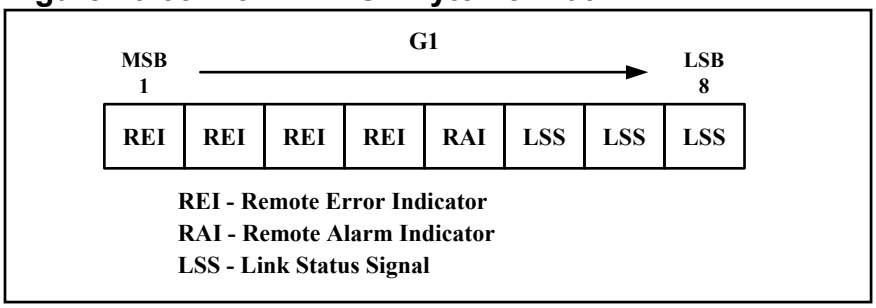


Figure 10-33. E3 PLCP G1 Byte Format



10.8.7.1 Transmit E3 PLCP Trailer Generation

E3 PLCP trailer generation inserts the E3 PLCP frame trailer immediately following subframe 0 (POI equals 01h), and generates the C1 byte. The trailer size is determined by the phase relationship of the G.751 E3 frame and PLCP frame and by the transmit 8 kHz reference clock. The trailer size is variable in all frames. The trailer size can be 17, 18, 19, 20, or 21 bytes. C1 is set to 3Bh, 4Fh, 75h, 9Dh, or A7h respectively, and the indicated number of bytes (17 – 21) are added after subframe 0. The trailer bytes are all set to 11001100.

10.8.7.2 Transmit E3 PLCP Frame Generation

E3 PLCP frame generation receives the incoming PLCP payload data stream, and overwrites all of the overhead byte locations.

The first two bytes of each subframe are overwritten with the frame alignment bytes A1 and A2, which have a value of F6h and 28h respectively.

The third byte of subframe # is overwritten with POI byte # (P#). The value of P# is 00####0Pb (0 = a logic zero, #### = the hexadecimal value of #, and P = the odd parity bit).

The fourth byte of subframes #8 – 6 are overwritten with the Z3 – Z1 bytes from the corresponding registers.

The fourth byte of subframe 5 is overwritten with the F1 byte from the corresponding register or the trail trace byte input from the transmit trail trace controller. The F1 byte from the corresponding register, the trail trace byte input

from the transmit trail trace controller, or the HDLC Overhead Processor interface). The F1 byte source is programmable (*PLCP.TCR*.TF1C[1:0]) (trail trace data link, HDLC, or register).

The fourth byte of subframe 4 is overwritten with the B1 byte which is a BIP-8 calculated over all of the path overhead bytes and cell bytes of the previous frame after all PLCP processing (frame generation, error insertion, and overhead insertion) has been completed.

The first four bits of the fourth byte of subframe 3 are overwritten with the G1 byte REI bits (G1[1:4]). The Remote Error Indication (REI) bits can be generated automatically or inserted from the G1 register bits. The REI source is programmable (auto or register). If the REI bits are generated automatically, they are set to zero when the receive side B1 byte exactly matches the BIP-8 calculated for the previous receives side frame. Otherwise, the REI is set to a value of one to eight to indicate the number of parity errors (BIP-8 errors) detected in the receive PLCP frame (B1 byte).

The fifth bits of the fourth byte of subframe 3 is overwritten with the G1 byte RAI bit (G1[5]). The Remote Alarm Indication (RAI) bit is sourced from a register.

The last three bits of the fourth byte of subframe 3 are overwritten with the G1 byte LSS bits (G1[6:8]). The Link Status Signal (LSS) bits are sourced from a register. The three register bits are inserted in the sixth, seventh, and eighth bits of the G1 byte in each frame.

The fourth byte of subframes 2 and 1 are overwritten with the M2 and M1 bytes respectively. Each byte can be individually sourced from a register, or from the transmit HDLC Overhead Processor. The M2 byte and M1 byte sources are each programmable (register or HDLC). If both bytes are programmed to be sourced from the transmit HDLC controller, they are concatenated as a single data link as opposed to two separate data links.

The fourth byte of subframe 0 is overwritten with the C1 byte created during trailer generation.

Once all of the overhead bytes have been overwritten, the data stream is passed on to error insertion.

10.8.7.3 Transmit E3 PLCP Error Insertion

Error insertion inserts various types of errors into the different overhead bytes. The types of errors that can be inserted are framing errors, BIP-8 parity errors, and Remote Error Indication (REI) errors.

The type of framing error(s) inserted is programmable (frame bit error or framing byte error). A framing bit error is a single bit error in a frame alignment byte (A1 or A2) or POI byte (P#). A framing byte error is an error in all eight bits of a frame alignment byte (A1 or A2) or path overhead indicator (POI) byte (P#). Framing error(s) can be inserted one error at a time, or in two consecutive bytes (A1 & A2 or P# & P#+1). The framing error insertion rate (single A1 or A2, single P#, A1 & A2, or P# & P#+1) is programmable.

The type of BIP-8 error(s) inserted is programmable (errored BIP-8 bit, or errored BIP-8 byte). An errored BIP-8 bit is inverting a single bit error in the B1 byte. An errored BIP-8 byte is inverting all eight bits in the B1 byte. BIP-8 error(s) can be inserted one error at a time, or continuously. The BIP-8 error insertion rate (single or continuous) is programmable.

The type of REI error(s) inserted is programmable (single REI error or eight REI errors). A single REI error is generated by setting the first four bits of the G1 byte to a value of 1h. Eight REI errors are generated by setting the first four bits of the G1 byte to a value of 8h. REI error(s) can be inserted one error at a time, or continuously. The REI error insertion rate (single or continuous) is programmable.

Error insertion can be initiated by a register bit (*PLCP.TEIR*.TSEI) or initiated by the manual error insertion input (TMEI). Each error type is individually enabled by a register bit. The error insertion initiation type (register or input) is programmable. Once all error insertion has been performed, the data stream is passed on to overhead insertion.

10.8.7.4 Transmit E3 PLCP Overhead Insertion

Overhead insertion can insert any (or all) of the path overhead bytes into the E3 PLCP frame. The overhead bytes Z3 – Z1, F1, B1, G1, M1, M2, and C1 can be sourced from the transmit overhead interface (TPOHCLK, TPOH, TPOHEN, and TPOHSOF). The B1 and C1 bytes are sourced as error masks (modulo 2 addition of the input B1/C1 byte and the generated B1/C1 byte). The overhead insertion is fully controlled by the transmit overhead interface. If the transmit PLCP overhead data enable signal (TPOHEN) is driven high, then the bit on the transmit PLCP overhead signal (TPOH) is inserted into the output data stream. Insertion of bits using the TPOH signal overwrites internal overhead insertion.

10.8.8 Receive E3 PLCP Frame Processor

The Receive E3 PLCP Frame Processor performs E3 PLCP framing, byte destuffing, performance monitoring, and overhead extraction.

The E3 PLCP frame format is shown in Figure 10-32. A1 and A2 are the subframe Alignment bytes that have a value of F6h and 28h respectively. P8 – P0 are the Path Overhead Identifier (POI) bytes that indicate the path overhead byte contained in the current subframe. Z3 – Z1 are growth bytes reserved for future use. F1 is the Path User Channel byte allocated for user communications purposes (This byte is undefined in ATM). B1 is the Bit Interleaved Parity-8 (BIP-8) byte used for PLCP path error monitoring. G1 is the PLCP Path Status Byte (See Figure 10-33) used for far-end path status and performance monitoring (bits 6 – 8 are undefined in ATM). M1 and M2 are the DQDB Layer Management Information bytes used for DQDB layer management communications (These bytes are undefined in ATM). C1 is the Cycle/Stuff Counter byte used as for PLCP stuff indication.

10.8.8.1 Receive E3 PLCP Framing

E3 PLCP framing determines the E3 PLCP frame boundary. The frame boundary is found by identifying the frame alignment bytes (A1 & A2), and the path overhead indicator (POI) byte (P#). The framer is an off-line framer that updates the data path frame counters when an out of frame (OOF) condition is present. The use of an off-line framer reduces the number of ATM cells discarded during the framing process. The continually searches for two consecutive sets of alignment bytes (A1 and A2), and two sequential POI bytes (P#) are identified. The data path frame counters are updated if an OOF condition is present). The maximum average reframe time is 23 μs.

10.8.8.2 Receive E3 PLCP Byte Destuffing

Byte destuffing discards the E3 PLCP frame trailer immediately following subframe 0 (POI equals 01h). The trailer size is determined by the cycle counter byte (C1). The trailer is seventeen to twenty-one bytes. It is seventeen bytes if C1 equals 3Bh, eighteen bytes if C1 equals 4Fh, nineteen bytes if C1 equals 75h, twenty bytes if C1 equals 9Dh, and twenty-one bytes if C1 equals A7h. The C1 codes provide error correction capability, and the C1 byte is corrected if required, and then used to determine the trailer size. Once the trailer size has been determined, the trailer bytes are discarded.

10.8.8.3 Receive E3 PLCP Performance Monitoring

Performance monitoring checks the E3 PLCP frame for errors and alarm conditions. The alarm conditions detected are OOF, LOF, COFA, and RAI. All alarm conditions are defect conditions. The FEAC Controller does not integrate alarms for failure conditions.

An Out Of Frame (OOF) condition is declared when an error is detected in both bytes in a framing word (A1 and A2) or two consecutive POI bytes (P0 - P11) are erred. An OOF condition is terminated when two sequential POI bytes and two consecutive framing words (A1 and A2) are error free or the E3 PLCP framer updates the data path frame counters.

If the Loss Of Frame (LOF) integration counter is disabled, an LOF condition is declared when an OOF condition has been continuously present for 1 ms. If the LOF integration counter is enabled, an LOF condition is declared by the LOF integration counter when the counter has been active for a total of 1 ms. The LOF integration counter is active (increments count) when an OOF condition is present, it is inactive (holds count) when an OOF condition is absent, and it is reset when an OOF condition is continuously absent for 1 ms. An LOF condition is terminated when an OOF condition is continuously absent for 1 ms.

A Change Of Frame Alignment (COFA) is declared when the E3 PLCP framer updates the data path frame counters with a frame alignment that is different from the current data path frame alignment.

A Remote Alarm Indication (RAI) condition is declared when ten consecutive frames are received with the RAI bit (fifth bit of G1) set to one. An RAI condition is terminated when ten consecutive frames are received with the RAI bit set to zero.

Three types of errors are accumulated: framing errors, BIP-8 errors and Remote Error Indication (REI) errors. Framing errors are determined by comparing A1, A2, and P# to their expected values. The type of framing errors accumulated is programmable (OOFs, bit, byte, or word). An OOF error increments the count whenever an OOF condition is first detected (up to 1 per 3 subframes). A bit error increments the count once for each bit in A1, each bit in A2, and each bit in P# that does not match its expected value (up to 24 per subframe). A byte error increments the count once for each A1 byte, A2 byte, and P# byte that does not match its expected value (up to 3

per subframe). A word error increments the count once for each frame alignment word (A1, A2, and P#) that does not match its expected value (up to 1 per subframe). The detection of POI byte (P#) framing errors is programmable (on or off).

BIP-8 errors are determined by calculating the BIP-8 of the current frame (path overhead and cell bytes), and comparing the calculated BIP-8 to the B1 byte in the next frame. The type of BIP-8 errors accumulated is programmable (bit or block). A bit error increments the count once for each bit in the B1 byte that does not match the corresponding bit in the calculated BIP-8 (up to 8 per frame). A block error increments the count if any bit in the B1 byte does not match the corresponding bit in the calculated BIP-8 (up to 1 per frame).

REI errors are determined by the four REI bits (first four bits of G1). The count is incremented by the value of the four REI bits (up to 8 per frame). Values of 9h - Fh are treated as zero errors.

10.8.8.4 Receive E3 PLCP Overhead Extraction

Overhead extraction extracts all of the E3 PLCP path overhead bytes from the E3 PLCP frame. All of the PLCP path overhead (POH) bytes (Z3 – Z1, F1, B1, G1, M1, M2, and C1) are output on the receive overhead bus (RPOHCLK, RPOH, and RPOHSOF). The B1 byte is output as an error indication (modulo 2 addition of the calculated BIP-8 and the B1 byte). In addition, the Z3 – Z1, F1, G1 (6:8), M1, and M2 bytes are integrated and stored in registers along with change indications. G1 (6:8) has an unstable indication as well. The F1 byte is sent to the receive trail trace buffer, and can also be sent to the receive HDLC controller. The M2 byte and/or M1 byte can be sent to the receive HDLC controller. The source of the data transferred to the receive HDLC controller is programmable (F1, M2, M1, or M2 & M1). If both the M2 and M1 byte are programmed to be the source for the receive HDLC controller, they are concatenated as a single data link as opposed to two separate data links.

Once all frame processing has been completed, the ATM cells are passed on to the ATM/Packet Processor with a start of cell indication.

10.9 Fractional Payload Controller

10.9.1 General Description

The Fractional Payload Controller allows the user to utilize a fraction of the DS3/E3 payload for ATM cell or HDLC packets. The unused DS3/E3 payload is considered fractional overhead and can be used as a proprietary data link. The allocation given to the fractional payload is programmable controlled using internal counters or controlled externally. The fractional overhead data can optionally be programmed to transmit all 0's, all 1's, a 1010 pattern, or insert data from an external source.

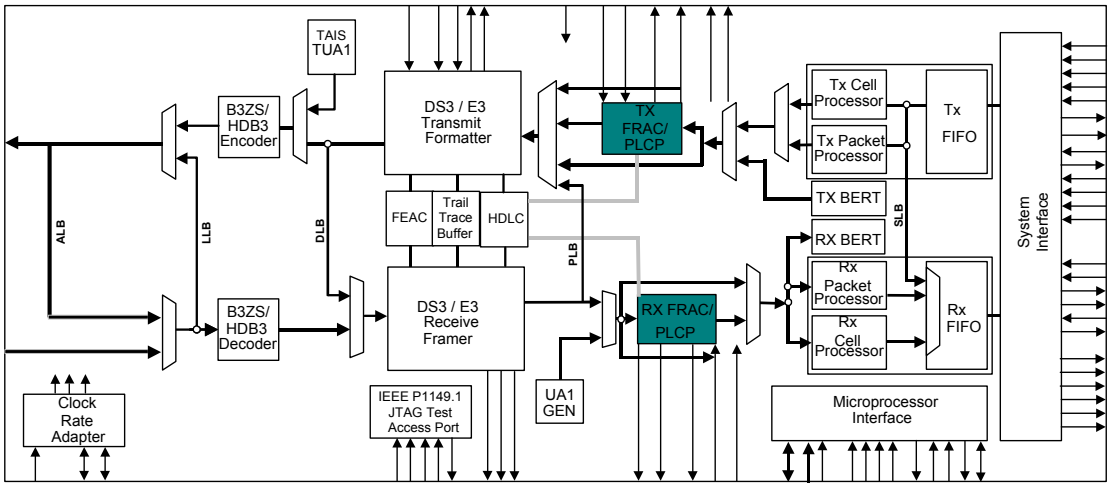
The Fractional Payload Controller de-maps fractional payload and overhead data from the DS3/E3 payload in the receive direction and maps fractional payload and overhead data into the DS3/E3 payload in the transmit direction.

The receive direction extracts the fractional payload and fractional overhead data bits from the receive DS3/E3 payload, performs fractional payload/overhead data demultiplexing, sends the fractional payload to the ATM/packet processor, and sends the fractional overhead data to an external interface.

The transmit direction accepts the fractional overhead from an internal register or the external interface and fractional payload data from the ATM/packet processor, performs fractional overhead/payload data multiplexing, and inserts the fractional overhead and payload data into the transmit DS3/E3 payload.

See Figure 10-34 for the location of the Fractional Payload Controller in the DS316x devices.

Figure 10-34. Fractional Payload Controller Detailed Block Diagram



10.9.2 Features

- **Programmable payload allocation** – The payload data and fractional overhead allocation can be programmed via registers.
- **Externally controlled payload allocation** – The payload data and fractional overhead allocation can be controlled by an external source via pins.
- **Fractional overhead extraction and insertion** – Extracts all fractional overhead from the DS3/E3 payload and sends it to an external serial interface. Inserts all fractional overhead from a serial interface and into the transmit DS3/E3 payload. Optionally, the transmit fractional overhead can be set to insert all 0's, all 1's, or a 1010 pattern.

10.9.3 Transmit Fractional Interface

The Transmit Fractional Interface receives the payload data stream from the ATM/Packet Processor and inserts a fractional overhead stream.

The incoming fractional overhead stream consists of fractional overhead (TFOHn), input fractional overhead enable (TFOHENIn), and output fractional overhead enable (TFOHENOn). TFOHn, TFOHENOn and TFOHENIn are typically referenced to TCLKIn (but also could be referenced to the TLCLKn, TCLKOn/TGCLKn, RCLKOn or RLCLKn clock pins). If external control is enabled, TFOHENIn marks the fractional overhead periods, and TFOHENOn is held low. If internal control is enabled, TFOHENOn marks the fractional overhead periods, and TFOHENIn is ignored. Fractional overhead control is programmable (internal or external). The fractional overhead source is programmable (all 0's, all 1's, a 10 pattern, or TFOH). See the FRAC.TCR Register Definition.

See Section 8.3.3 for specific timing relationships between these pins.

10.9.4 Transmit Fractional Controller

The Transmit Fractional Controller generates the transmit fractional overhead enable output (TFOHENOn) used in internal control mode to insert fractional overhead. The outgoing transmit data stream to the DS3/E3 Framer is divided into frames. Each frame is composed of data groups that have a programmable size (1 – 8191 bits). Each data group is divided into two sections. The first section (Section A) has a programmable size (0 – 8191 bits). The second section (Section B) contains the remaining bits (*g* – *a* bits). See Figure 10-35. The section that contains fractional overhead is programmable (Section A or Section B by setting the *FRAC.TCR*.TSASS register bit). TFOHENOn is high during the fractional overhead section of the data group, and low during the payload section of the data group. TFOHENOn is also low during line overhead/stuff periods.

10.9.5 Receive Fractional Interface

The Receive Fractional Interface receives the DS3/E3 payload from the DS3/E3 Framer, and performs fractional overhead extraction on the payload.

The receive fractional overhead pins are the input fractional overhead enable (RFOHENIn), and the output fractional overhead enable (RFOHENOn). RFOHENIn is sampled on the rising edge of RCLKOn, typically, or it can be referenced to the RLCLKn pin. RFOHENOn is updated on the rising edge of RCLKOn (or alternatively the RLCLKn pin).

If external control is enabled, the receive fractional overhead enable input (RFOHENIn) marks the fractional overhead bits contained in the DS3/E3 payload. RFOHENIn is high while a fractional overhead period is available on RSERn. RFOHENIn is low during payload data or line overhead/stuff periods.

If internal control is enabled, the receive fractional overhead enable output (RFOHENOn) marks the fractional overhead bits in the received DS3/E3 payload. RFOHENOn is high during a fractional overhead bit period on RSERn. RFOHENOn is low during a payload data or line overhead/stuff period. See Section 8.3.3 for specific timing relationships between these pins.

10.9.6 Receive Fractional Controller

The Receive Fractional Controller generates the receive fractional overhead enable output (RFOHENOn) used in internal control mode to extract fractional overhead to the RFOHn pin. The DS3/E3 payload is divided into frames composed of data groups that have a programmable size (1 – 8191 bits). Each data group is divided into two sections. The first section (Section A) has a programmable size (*a*, 0 – 8191 bits). The second section (Section B) contains the remaining bits (*g* – *a* bits). See Figure 10-35. The section that contains fractional overhead is programmable (Section A or Section B by setting the FRAC.RCR.RSASS register bit). RFOHENOn is high during the fractional overhead section of the data group, and low during the payload section of the data group. RFOHENOn is also low during line overhead/stuff periods.

The first bit of a frame is the first bit of a data group. If a frame does not contain an integer number of data groups (*f* / *g* is not an integer), the last data group in the frame will be a short data group. The last bit of the short data group will be the last data period before the start of frame period.

Figure 10-35. Data Group Format

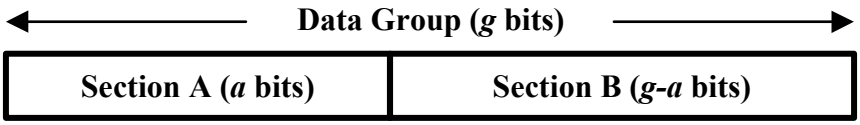
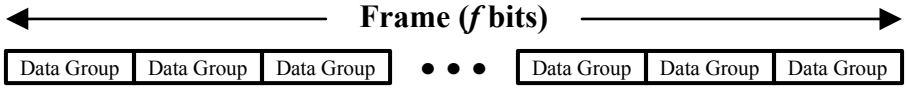


Figure 10-36. Frame Format



10.10 DS3/E3 Framer / Formatter

10.10.1 General Description

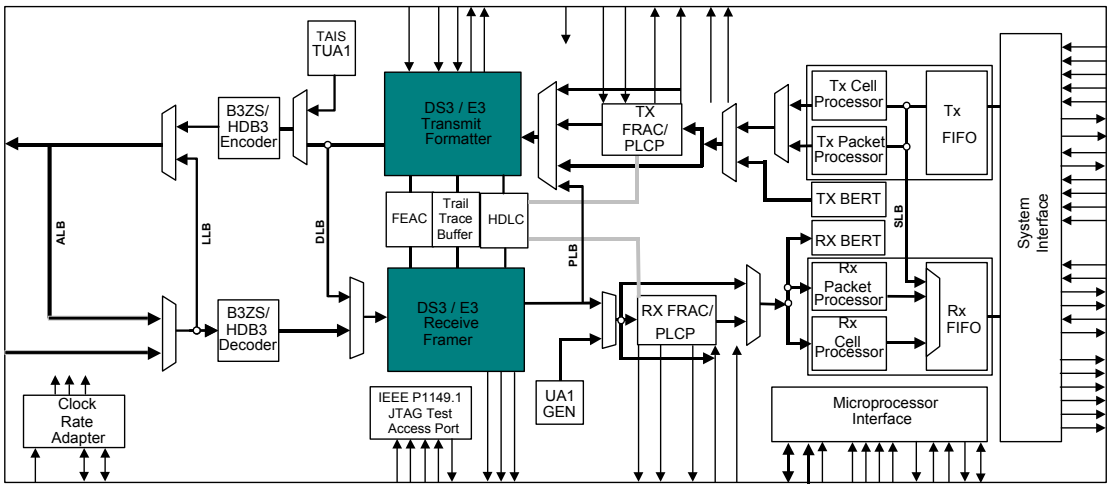
The Receive DS3/E3 Framer receives a unipolar DS3/E3 signal, determines frame alignment and extracts the DS3/E3 overhead in the receive direction. The Transmit DS3/E3 Formatter receives a DS3/E3 payload, generates framing, inserts DS3/E3 overhead, and outputs a unipolar DS3/E3 signal in the transmit direction.

The Receive DS3/E3 Framer receives a DS3/E3 signal, determines the frame alignment, extracts the DS3/E3 overhead, and outputs the payload with frame and overhead

The Transmit DS3/E3 Formatter receives a DS3/E3 payload from the ATM/Packet Processor, generates a DS3/E3 frame, optionally inserts DS3/E3 overhead, and transmits the DS3/E3 signal.

Refer to Figure 10-37 for the location of the DS3/E3 Framer/Formatter blocks in the DS316x devices.

Figure 10-37. Framer Detailed Block Diagram



10.10.2 Features

10.10.2.1 Transmit Formatter

- **Programmable DS3 or E3 formatter** – Accepts a DS3 (M23 or C-bit) or E3 (G.751 or G.832) signal and performs DS3/E3 overhead generation.
- **Arbitrary framing format support** – Generates a signal with an arbitrary framing format. The line overhead/stuff periods are added into the data stream using an overhead mask signal.
- **Generates alarms and errors** – DS3 alarm conditions (AIS, RDI, and Idle) and errors (framing, parity, and FEBE), or E3 alarm conditions (AIS and RDI/RAI) and errors (framing, parity, and REI) can be inserted into the outgoing data stream.
- **Externally controlled serial DS3/E3 overhead insertion port** – Can insert all DS3 or E3 overhead via a serial interface. DS3/E3 overhead insertion is fully controlled via the serial overhead interface.
- **HDLC overhead insertion** – An HDLC channel can be inserted into the DS3 or E3 data stream.
- **FEAC insertion** – A FEAC channel can be inserted into the DS3 or E3 data stream.
- **Trail Trace insertion** – Inputs and inserts the G.832 E3 TR byte.

10.10.2.2 Receive Framer

- **Programmable DS3 or E3 framer** – Accepts a DS3 (M23 or C-bit) or E3 (G.751 or G.832) signal and performs DS3/E3 overhead termination.
- **Arbitrary framing format support** – Accepts a signal with an arbitrary framing format. The Line overhead/stuff periods are removed from the data stream using an overhead mask signal.

- **Detects alarms and errors** – Detects DS3 alarm conditions (SEF, OOMF, OOF, LOF, COFA, AIS, AIC, RDI, and Idle) and errors (framing, parity, and FEBE), or E3 alarm conditions (OOF, LOF, COFA, AIS, and RDI/RAI) and errors (framing, parity, and REI).
- **Serial DS3/E3 overhead extraction port** – Extracts all DS3 or E3 overhead and outputs it on a serial interface.
- **HDLC overhead extraction** – An HDLC channel can be extracted from the DS3 or E3 data stream.
- **FEAC extraction** – A FEAC channel can be extracted from the DS3 or E3 data stream.
- **Trail Trace extraction** – Extracts and outputs the G.832 E3 TR byte.

10.10.3 Transmit Formatter

The Transmit Formatter receives a DS3, E3 or CC52 clear-channel data stream and performs framing generation, error insertion, overhead insertion, and AIS/Idle generation for C-bit DS3, M23 DS3, G.751 E3, G.832 E3, or CC52 clear-channel framing protocols. In clear-channel mode, only AIS/Idle generation is performed.

The bits in a byte are transmitted MSB first, LSB last. When they are input serially, they are input in the order they are to be transmitted. The bits in a byte in an outgoing signal are numbered in the order they are transmitted, 1 (MSB) to 8 (LSB). However, when a byte is stored in a register, the MSB is stored in the highest numbered bit (7), and the LSB is stored in the lowest numbered bit (0). This is to differentiate between a byte in a register and the corresponding byte in a signal.

After all frame formatting is completed, the frame processor inserts a DS3/E3 (or clear channel) data stream into a line data stream (OHM modes only). The line data stream is an upper level signal with a DS3, E3, or clear-channel data stream embedded within the upper level frame. E.g., if a DS3 signal has two line overhead/stuff periods occur between the beginning of one frame, and the beginning of the next frame, there will be 4762 clock periods between the beginning of the two frames (4760 for the DS3 data periods plus 2 for the line overhead/stuff periods).

10.10.4 Receive Framer

The Receive Framer receives the incoming DS3, E3, or clear-channel line/tributary data stream, performs appropriate framing, terminates and extracts the associated overhead bytes, and extracts the DS3, E3, or clear-channel payload data stream (OHM modes only). The line data stream is an upper level signal with a DS3, E3, or clear-channel data stream embedded within the upper level frame. E.g., if a DS3 signal has two line overhead/stuff periods occur between the beginning of one frame, and the beginning of the next frame, there will be 4762 clock periods between the beginning of the two frames (4760 for the DS3 data periods plus 2 for the line overhead/stuff periods).

The Receive Framer processes a C-bit format DS3, M23 format DS3, G.751 format E3, G.832 format E3, or clear-channel data stream, performing framing, performance monitoring, overhead extraction, and generates downstream AIS, if necessary. In clear-channel mode, only performance monitoring and downstream AIS generation are performed.

The bits in a byte are received MSB first, LSB last. When they are output serially, they are output MSB first, LSB last. The bits in a byte in an incoming signal are numbered in the order they are received, 1 (MSB) to 8 (LSB). However, when a byte is stored in a register, the MSB is stored in the highest numbered bit (7), and the LSB is stored in the lowest numbered bit (0). This is to differentiate between a byte in a register and the corresponding byte in a signal.

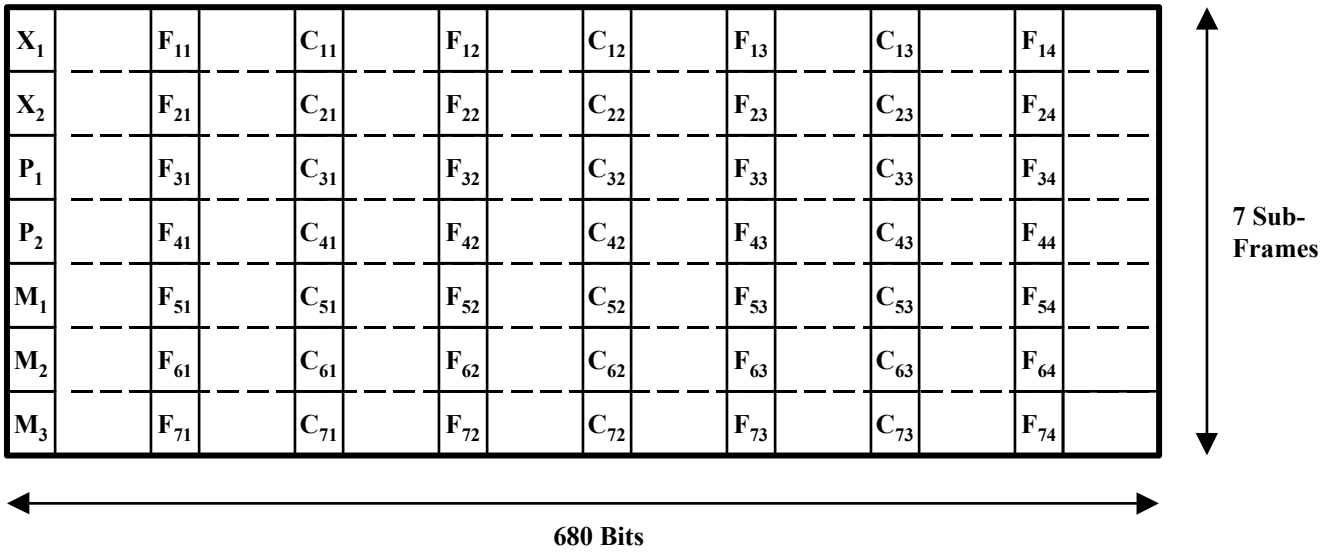
Some bits, bit groups, or bytes (data) are integrated before being stored in a register. Integration requires the data to have the same new data value for five consecutive occurrences before the new data value will be stored in the data register. Unless stated otherwise, integrated data may have an associated unstable indication. Integrated data is considered unstable if the received data value does not match the currently stored (integrated) data value or the previously received data value for eight consecutive occurrences. The unstable condition is terminated when the same value is received for five consecutive occurrences.

10.10.4.1.1 Receive DS3 Framing

DS3 framing determines the DS3 frame boundary. In order to identify the DS3 frame boundary, first the subframe boundary must be found. The subframe boundary is found by identifying the subframe alignment bits F_{X1}, F_{X2}, F_{X3}, and F_{X4}, which have a value of one, zero, zero, and one respectively. See Figure 10-38. Once the subframe boundary is found, the multiframe frame boundary can be found. The multiframe boundary is found by identifying

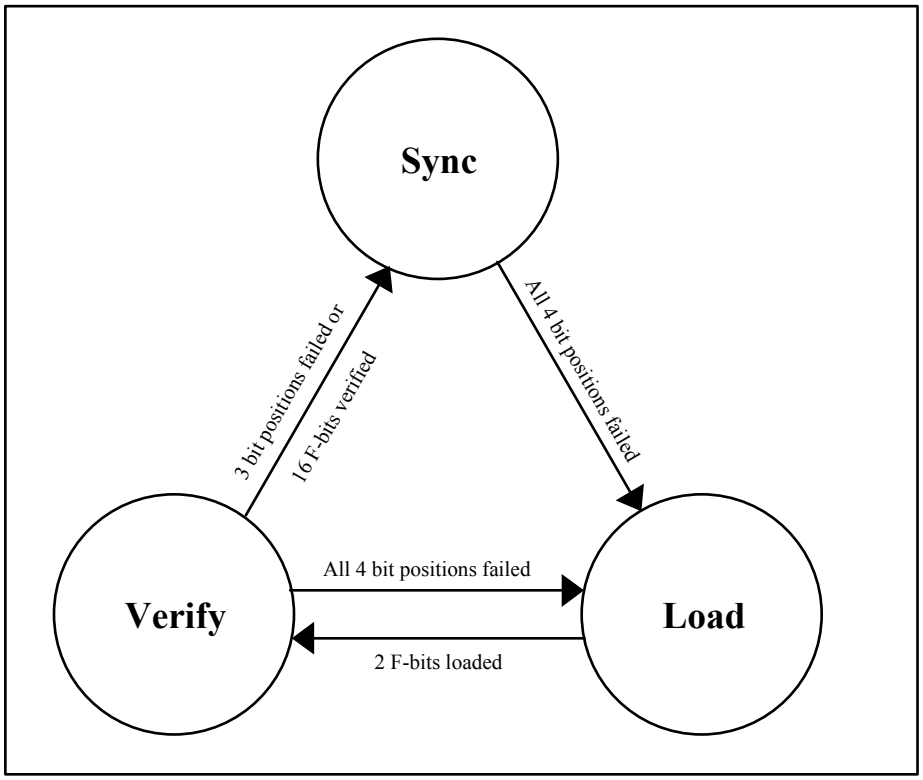
the multiframe alignment bits M_1, M_2, and M_3, which have a value of zero, one, and zero respectively. The DS3 framer is an off-line framer that only updates the data path frame counters when either an out of frame (OOF) or an out of multiframe (OOMF) condition is present. The use of an off-line framer reduces the average time required to reframe, and reduces data loss caused by burst error. The DS3 framer has a Maximum Average Reframe Time (MART) of approximately 1.0 ms.

Figure 10-38. DS3 Frame Format



The subframe framer continually searches four adjacent bit positions for a subframe boundary. A subframe alignment bit (F-bit) checker checks each bit position. All four bit positions must fail before any other bit positions are checked for a subframe boundary. There are 170 possible bit positions that must be checked, and four positions are checked simultaneously. Therefore, up to 43 checks may be needed to identify the subframe boundary. The subframe framer enables the multiframe frame once it has identified a subframe boundary. See Figure 10-39 for the subframe framer state diagram.

Figure 10-39. DS3 Subframe Framer State Diagram



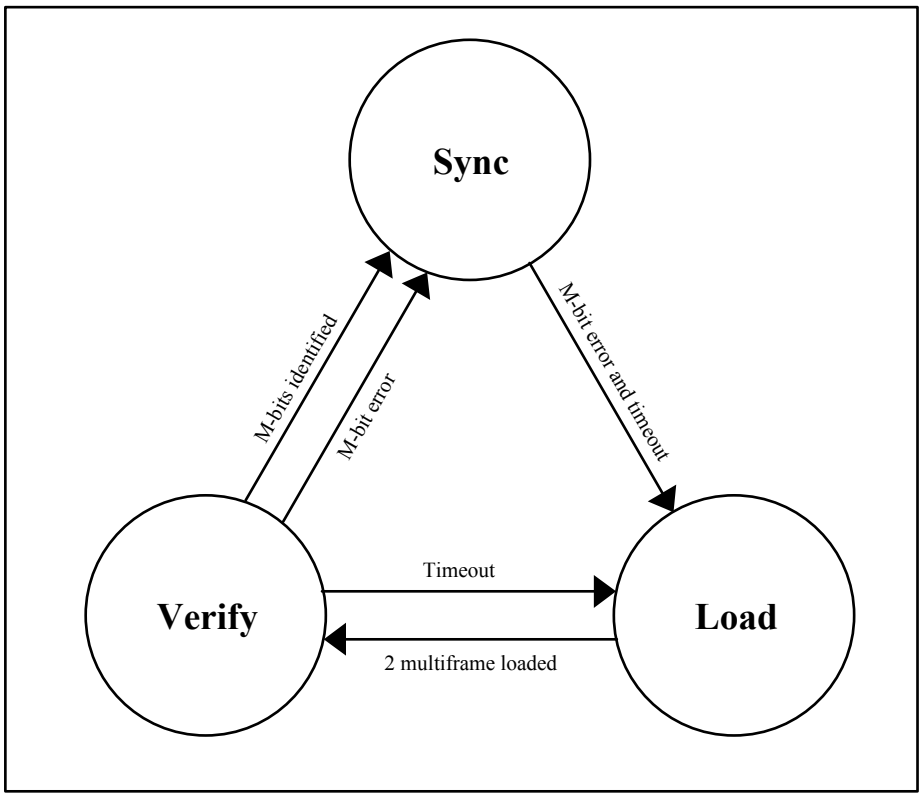
The multiframe framer checks for a multiframe boundary. When the multiframe framer identifies a multiframe boundary, it updates the data path frame counters if either an OOF or OOMF condition is present. The multiframe framer waits until a subframe boundary has been identified. Then, each bit position is checked for the multiframe boundary. The multiframe boundary is found by identifying the three multiframe alignment bits (M-bits). Since there are seven multiframe bits and three bits are required to identify the multiframe boundary, up to 9 checks may be needed to find the multiframe boundary. Once the multiframe boundary is identified, it is checked in each subsequent frame. The data path frame counters are updated if the three multiframe alignment bits are error free, and an OOF or OOMF condition exists. If the multiframe framer checks more than fifteen multiframe bit (X-bits, P-bits, and M-bits) positions without identifying the multiframe boundary, the multiframe framer times out, and forces the subframe framer back into the load state. Refer to Figure 10-40 for the multiframe framer state diagram.

10.10.4.1.2 Receive DS3 Performance Monitoring

Performance monitoring checks the DS3 frame for alarm conditions and errors. The alarm conditions detected are OOMF, OOF, SEF, LOF, COFA, LOS, AIS, Idle, RUA1, and RDI. The errors accumulated are framing, P-bit parity, C-bit parity (C-bit format only), and Far-End Block Error (FEBE) (C-bit format only) errors.

An Out Of MultiFrame (OOMF) condition is declared when a multiframe alignment bit (M-bit) error has been detected in two or more of the last four consecutive DS3 frames, or when a manual resynchronization is requested. An OOMF condition is terminated when no M-bit errors have been detected in the last four consecutive DS3 frames, or when the DS3 framer updates the data path frame counters. Refer to Figure 10-40 for the multiframe framer state diagram.

Figure 10-40. DS3 Multiframe Framer State Diagram



If multiframe alignment OOF is disabled, an Out Of Frame (OOF) condition is declared when three or more out of the last sixteen consecutive subframe alignment bits (F-bits) have been errored, or a manual resynchronization is requested. If multiframe alignment OOF is enabled, an OOF condition is declared when three or more out of the last sixteen consecutive F-bits have been errored, when an OOMF condition is declared, or when a manual resynchronization is requested. If multiframe alignment OOF is disabled, an OOF condition is terminated when none of the last sixteen consecutive F-bits has been errored, or when the DS3 framer updates the data path frame counters. If multiframe alignment OOF is enabled, an OOF condition is terminated when an OOMF condition is not active and none of the last sixteen consecutive F-bits has been errored, or when the DS3 framer updates the data path frame counters. Multiframe alignment OOF is programmable (on or off).

A Severely Errored Frame (SEF) condition is declared when three or more out of the last sixteen consecutive F-bits have been errored, or when a manual resynchronization is requested. An SEF condition is terminated when an OOF condition is absent.

A Loss Of Frame (LOF) condition is declared by the LOF integration counter when it has been active for a total of *T* ms. The LOF integration counter is active (increments count) when an OOF condition is present, it is inactive (holds count) when an OOF condition is absent, and it is reset when an OOF condition is absent for *T* continuous ms. *T* is programmable (0, 1, 2, or 3). An LOF condition is terminated when an OOF condition is absent for *T* continuous ms.

A Change Of Frame Alignment (COFA) is declared when the DS3 framer updates the data path frame counters with a frame alignment that is different from the current data path DS3 frame alignment.

A Loss Of Signal (LOS) condition is declared when the B3ZS encoder is active, and it declares an LOS condition. An LOS condition is terminated when the B3ZS encoder is inactive, or it terminates an LOS condition.

An Alarm Indication Signal (AIS) is a DS3 signal with valid F-bits and M-bits. The X-bits (X_1 and X_2) are set to one, the P-bits (P_1 and P_2) are set to zero, all C-bits (C_{XY}) are set to zero, and the payload bits are set to a 1010 pattern starting with a one immediately after each DS3 overhead bit. An AIS signal is present when a DS3 frame is received with valid F-bits and M-bits, both X-bits set to one, bot P-bits set to zero, all C-bits set to zero, and all but seven or fewer payload data bits matching the DS3 overhead aligned 1010 pattern. An AIS signal is absent when a DS3 frame is received that does not meet the aforementioned criteria for an AIS signal being present. The AIS

integration counter declares an AIS condition when it has been active for a total of 10 to 17 DS3 frames. The AIS integration counter is active (increments count) when an AIS signal is present, it is inactive (holds count) when an AIS signal is absent, and it is reset when an AIS signal is absent for 10 to 17 consecutive DS3 frames. An AIS condition is terminated when an AIS signal is absent for 10 to 17 consecutive DS3 frames.

A Receive Unframed All 1's (RUA1) condition is declared if in each of 4 consecutive 2047 bit windows, five or less zeros are detected and an OOF condition is continuously present. A RUA1 condition is terminated if in each of 4 consecutive 2047 bit windows, six or more zeros are detected or an OOF condition is continuously absent.

An Idle Signal (Idle) is a DS3 signal with valid F-bits, M-bits, and P-bits (P_1 and P_2). The X-bits (X_1 and X_2) are set to one, C_{31}, C_{32}, and C_{33} are set to zero, and the payload bits are set to a 1100 pattern starting with 11 immediately after each overhead bit. In C-bit mode, an Idle Signal is present when a DS3 frame is received with valid F-bits, M-bits, and P-bits, both X-bits set to one, C_{31}, C_{32}, and C_{33} set to zero, and all but seven or fewer payload data bits matching the overhead aligned 1100 pattern. In M23 mode, an Idle signal is present when a DS3 frame is received with valid F-bits, M-bits, and P-bits, both X-bits set to one, and all but seven or fewer payload data bits matching the T3 overhead aligned 1100 pattern. An Idle signal is absent when a DS3 frame is received that does not meet aforementioned criteria for an Idle signal being present. The Idle integration counter declares an Idle condition when it has been active for a total of 10 to 17 DS3 frames. The Idle integration counter is active (increments count) when an Idle signal is present, it is inactive (holds count) when an Idle signal is absent, and it is reset when an Idle signal is absent for 10 to 17 consecutive DS3 frames. An Idle condition is terminated when an Idle signal is absent for 10 to 17 consecutive DS3 frames.

A Remote Defect Indication (RDI) condition (also called a far-end SEF/AIS defect condition) is declared when four consecutive DS3 frames are received with the X-bits (X_1 and X_2) set to zero. An RDI condition is terminated when four consecutive DS3 frames are received with the X-bits set to one.

A DS3 Framing Format Mismatch (DS3FM) condition is declared when the DS3 format programmed (M23, C-bit) does not match the incoming DS3 signal framing format. A DS3FM condition is terminated when the incoming DS3 signal framing format is the same format as programmed. Framing errors are determined by comparing F-bits and M-bits to their expected values. The type of framing errors accumulated is programmable (OOFs, F & M, F, or M). An OOF error increments the count whenever an OOF condition is first detected. An F & M error increments the count once for each F-bit or M-bit that does not match its expected value (up to 31 per DS3 frame). An F error increments the count once for each F-bit that does not match its expected value (up to 28 per DS3 frame). An M error increments the count once for each M-bit that does not match its expected value (up to 3 per DS3 frame).

P-bit parity errors are determined by calculating the parity of the current DS3 frame (payload bits only), and comparing the calculated parity to the P-bits (P_1 and P_2) in the next DS3 frame. If the calculated parity does not match P_1 or P_2, a single P-bit parity error is declared.

C-bit parity errors (C-bit format only) are determined by calculating the parity of the current DS3 frame (payload bits only), and comparing the calculated parity to the C-bits in subframe three (C_{31}, C_{32}, and C_{33}) in the next DS3 frame. If the calculated parity does not match C_{31}, C_{32}, or C_{33}, a single C-bit parity error is declared.

FEBE errors (C-bit format only) are determined by the C-bits in subframe four (C_{41}, C_{42}, and C_{43}). A value of 111 indicates no error and any other value indicates an error.

The receive alarm indication (RAI) bit will be set high in the transmitter when one or more of the indicated alarm conditions is present, and low when all of the indicated alarm conditions are absent. Setting the receive alarm indication on LOS, SEF, LOF, or AIS is individually programmable (on or off).

The Application Identification Channel (AIC) is stored in a register bit. It is determined from the C_{11} bit. The AIC is set to one (C-bit format) if the C_{11} bit is set to one in thirty-one consecutive multiframes. The AIC is set to zero (M23 format) if the C_{11} bit is set to zero in four of the last thirty-one consecutive multiframes. Note: The stored AIC bit must not change when an LOS, OOF, or AIS condition is present.

A FEBE is transmitted by default upon reception of a DS3 frame in which a C-bit parity error or a framing error is detected and counted.

10.10.5 C-bit DS3 Framer/Formatter

10.10.5.1 Transmit C-bit DS3 Frame Processor

The C-bit DS3 frame format is shown in Figure 10-38. Table 10-32 shows the function of each overhead bit in the DS3 Frame.

Table 10-32. C-Bit DS3 Frame Overhead Bit Definitions

Bit	Definition
X_1, X_2	Remote Defect Indication (RDI)
P_1, P_2	Parity Bits
M_1, M_2, and M_3	Multiframe Alignment Bits
F_{XY}	Subframe Alignment Bits
C_{11}	Application Identification Channel (AIC)
C_{12}	Reserved
C_{13}	Far-End Alarm and Control (FEAC) signal
C_{21}, C_{22}, and C_{23}	Unused
C_{31}, C_{32}, and C_{33}	C-bit parity bits
C_{41}, C_{42}, and C_{43}	Far-End Block Error (FEBE) bits
C_{51}, C_{52}, and C_{53}	Path Maintenance Data Link (or HDLC) bits
C_{61}, C_{62}, and C_{63}	Unused
C_{71}, C_{72}, and C_{73}	Unused

X_1 and X_2 are the Remote Defect Indication (RDI) bits (also referred to as the far-end SEF/AIS bits). P_1 and P_2 are the parity bits used for line error monitoring. M_1, M_2, and M_3 are the multiframe alignment bits. F_{XY} are the subframe alignment bits. C_{11} is the Application Identification Channel (AIC). C_{12} is reserved for future network use, and has a value of one. C_{13} is the Far-End Alarm and Control (FEAC) signal. C_{21}, C_{22}, and C_{23} are unused, and have a value of one. C_{31}, C_{32}, and C_{33} are the C-bit parity bits used for path error monitoring. C_{41}, C_{42}, and C_{43} are the Far-End Block Error (FEBE) bits used for remote path error monitoring. C_{51}, C_{52}, and C_{53} are the path maintenance data link (or HDLC) bits. C_{61}, C_{62}, and C_{63} are unused, and have a value of one. C_{71}, C_{72}, and C_{73} are unused, and have a value of one. The X-bit, P-bit, M-bit, C-bit, and F-bit positions are overhead bits, and the other bit positions in the DS3 frame are payload bits.

10.10.5.2 Transmit C-bit DS3 Frame Generation

C-bit DS3 frame generation receives the incoming payload data stream, and overwrites the entire overhead bit locations.

The multiframe alignment bits (M_1, M_2, and M_3) are overwritten with the values zero, one, and zero (010) respectively.

The subframe alignment bits (F_{X1}, F_{X2}, F_{X3}, and F_{X4}) are overwritten with the values one, zero, zero, and one (1001) respectively.

The X-bits (X_1 and X_2) are both overwritten with the Remote Defect Indicator (RDI). The RDI source is programmable (automatic, 1, or 0). If the *T3.TCR*.ARDID is one then the *T3.TCR*.TRDI register bit controls this bit. If the RDI is generated automatically (*T3.TCR*.ARDID=0), the X-bits are set to zero when one or more of the

indicated alarm conditions is present, and set to one when all of the indicated alarm conditions are absent. Automatically setting RDI on LOS, SEF, LOF, or AIS is individually programmable (on or off).

The P-bits (P_1 and P_2) are both overwritten with the calculated payload parity from the previous DS3 frame. The payload parity is calculated by performing modulo 2 addition of all of the payload bits after all frame processing has been completed. P-bit generation is programmable (on or off) via the *T3.TCR*.PBGE register bit. The P-bits will be generated if either P-bit generation is enabled or frame generation is enabled.

The bits C_{11}, C_{12}, C_{21}, C_{22}, C_{23}, C_{61}, C_{62}, C_{63}, C_{71}, C_{72}, and C_{73} are all overwritten with a one.

The bit C_{13} is overwritten with the Far-End Alarm and Control (FEAC) data input from the transmit FEAC controller.

The bits C_{31}, C_{32}, and C_{33} are all overwritten with the calculated payload parity from the previous DS3 frame.

The bits C_{41}, C_{42}, and C_{43} are all overwritten with the Far-End Block Error (FEBE) bit. The FEBE bit can be generated automatically or inserted from a register bit. The FEBE bit source is programmable (automatic or register). If the *T3.TCR*.AFEBED register bit is one then the *T3.TCR*.TFEBE register bit controls this bit. If the FEBE bit is generated automatically, it is zero when at least one C-bit parity error has been detected during the previous frame.

The bits C_{51}, C_{52}, and C_{53} are overwritten with the path maintenance data link input from the HDLC controller.

Once all of the DS3 overhead bits have been overwritten, the data stream is passed on to error insertion. If frame generation is disabled, the incoming DS3 signal is passed on to error insertion. Frame generation is programmable (on or off). Note: P-bit generation may still be performed even if frame generation is disabled.

10.10.5.3 Transmit C-bit DS3 Error Insertion

Error insertion inserts various types of errors into the different DS3 overhead bits. The types of errors that can be inserted are framing errors, P-bit parity errors, C-bit parity errors, and Far-End Block Error (FEBE) errors.

The framing error insertion mode is programmable (F-bit, M-bit, SEF, or OOMF). An F-bit error is a single subframe alignment bit (F_{XY}) error. An M-bit error is a single multiframe alignment bit (M_1, M_2, or M_3) error. An SEF error is an error in all the subframe alignment bits in a subframe (F_{X1}, F_{X2}, F_{X3}, and F_{X4}). An OOMF error is a single multiframe alignment bit (M_1, M_2, or M_3) error in two consecutive DS3 frames.

A P-bit parity error is generated by is inverting the value of the P-bits (P_1 and P_2) in a single DS3 frame. P-bit parity error(s) can be inserted one error at a time, or continuously. The P-bit parity error insertion mode (single or continuous) is programmable.

A C-bit parity error is generated by is inverting the value of the C_{31}, C_{32}, and C_{33} bits in a single DS3 frame. C-bit parity error(s) can be inserted one error at a time, or continuously. The C-bit parity error insertion mode (single or continuous) is programmable.

A FEBE error is generated by forcing the C_{41}, C_{42}, and C_{43} bits in a single multiframe to zero. FEBE error(s) can be inserted one error at a time, or continuously. The FEBE error insertion rate (single or continuous) is programmable.

Each error type (framing, P-bit parity, C-bit parity, or FEBE) has a separate enable. Continuous error insertion mode inserts errors at every opportunity. Single error insertion mode inserts an error at the next opportunity when requested. The framing multi-error modes (SEF or OOMF) insert the indicated number of error(s) at the next opportunities when requested; i.e., a single request will cause multiple errors to be inserted. The requests can be initiated by a register bit(TSEI) or by the manual error insertion input (TMEI). The error insertion initiation type (register or input) is programmable. The insertion of each particular error type is individually enabled. Once all error insertion has been performed, the data stream is passed on to overhead insertion.

10.10.5.4 Transmit C-bit DS3 Overhead Insertion

Overhead insertion can insert any (or all) of the DS3 overhead bits into the DS3 frame. The DS3 overhead bits X_1, X_2, P_1, P_2, M_X, F_{XY}, and C_{XY} can be sourced from the transmit overhead interface (TOHCLKn, TOHn, TOHENn, and TOHSOFn). The P-bits (P_1 and P_2) and C_{31}, C_{32}, and C_{33} bits are received as an error mask (modulo 2 addition of the input bit and the internally generated bit). The DS3 overhead insertion is fully controlled by the transmit overhead interface. If the transmit overhead data enable signal (TOHENn) is driven high, then the bit on the transmit overhead signal (TOHn) is inserted into the output data stream. Insertion of bits using the TOHn signal overwrites internal overhead insertion.

10.10.5.5 Transmit C-bit DS3 AIS/Idle Generation

C-bit DS3 AIS/Idle generation overwrites the data stream with AIS or an Idle signal. If transmit Idle is enabled, the data stream payload is forced to a 1100 pattern with two ones immediately following each DS3 overhead bit. M_1, M_2, and M_3 bits are overwritten with the values zero, one, and zero (010) respectively. F_{X1}, F_{X2}, F_{X3}, and F_{X4} bits are overwritten with the values one, zero, zero, and one (1001) respectively. X_1 and X_2 are overwritten with 11. And, P_1, P_2, C_{31}, C_{32}, and C_{33} are overwritten with the calculated payload parity from the previous output DS3 frame.

If transmit AIS is enabled, the data stream payload is forced to a 1010 pattern with a one immediately following each DS3 overhead bit. M_1, M_2, and M_3 bits are overwritten with the values zero, one, and zero (010) respectively. F_{X1}, F_{X2}, F_{X3}, and F_{X4} bits are overwritten with the values one, zero, zero, and one (1001) respectively. X_1 and X_2 are overwritten with 11. P_1, P_2, C_{31}, C_{32}, and C_{33} are overwritten with the calculated payload parity from the previous output DS3 frame. And, C_{X1}, C_{X2}, and C_{X3} ($X \neq 3$) are overwritten with 000. AIS will overwrite a transmit Idle signal.

10.10.5.5.1 Receive C-bit DS3 Frame Format

The DS3 frame format is shown in Figure 10-38. X_1 and X_2 are the Remote Defect Indication (RDI) bits (also referred to as the far-end SEF/AIS bits). P_1 and P_2 are the parity bits used for line error monitoring. M_1, M_2, and M_3 are the multiframe alignment bits that define the multiframe boundary. F_{XY} are the subframe alignment bits that define the subframe boundary. Note: Both the M-bits and F-bits define the DS3 frame boundary. C_{11} is the Application Identification Channel (AIC). C_{12} is reserved for future network use, and has a value of one. C_{13} is the Far-End Alarm and Control (FEAC) signal. C_{21}, C_{22}, and C_{23} are unused, and have a value of one. C_{31}, C_{32}, and C_{33} are the C-bit parity bits used for path error monitoring. C_{41}, C_{42}, and C_{43} are the Far-End Block Error (FEBE) bits used for remote path error monitoring. C_{51}, C_{52}, and C_{53} are the path maintenance data link (or HDLC) bits. C_{61}, C_{62}, and C_{63} are unused, and have a value of one. C_{71}, C_{72}, and C_{73} are unused, and have a value of one.

10.10.5.5.2 Receive C-bit DS3 Overhead Extraction

Overhead extraction extracts all of the DS3 overhead bits from the C-bit DS3 frame. All the DS3 overhead bits X_1, X_2, P_1, P_2, M_X, F_{XY}, and C_{XY} are output on the receive overhead interface (ROH, ROHSOF, and ROHCLK). The P_1, P_2, C_{31}, C_{32}, and C_{33} bits are output as an error indication (modulo 2 addition of the calculated parity and the bit). In addition, the Application Identification Channel (AIC), which is stored in a register bit, is determined from the C_{11} bit. The AIC is set to one (C-bit format) if the C_{11} bit is set to one in thirty-one consecutive multiframes. The AIC is set to zero (M23 format) if the C_{11} bit is set to zero in four of the last thirty-one consecutive multiframes. Note: The stored AIC bit must not change when an LOS, OOF, or AIS condition is present. The C_{13} bit is sent over to the receive FEAC controller. The C_{51}, C_{52}, and C_{53} bits are sent to the receive HDLC overhead controller.

10.10.6 M23 DS3 Framer/Formatter

10.10.6.1 Transmit M23 DS3 Frame Processor

The M23 DS3 frame format is shown in Figure 10-38. Table 10-33 defines the framing bits for M23 DS3. X_1 and X_2 are the Remote Defect Indication (RDI) bits (also referred to as the far-end SEF/AIS bits). P_1 and P_2 are the parity bits used for line error monitoring. M_1, M_2, and M_3 are the multiframe alignment bits. F_{XY} are the subframe alignment bits. C_{11} is the Application Identification Channel (AIC). C_{X1}, C_{X2}, and C_{X3} are the stuff control bits for tributary #X. The X-bit, P-bit, M-bit, C-bit, and F-bit positions are overhead bits, and the other bit positions in the DS3 frame are payload bits.

Table 10-33. M23 DS3 Frame Overhead Bit Definitions

Bit	Definition
X_1, X_2	Remote Defect Indication (RDI)
P_1, P_2	Parity Bits
M_1, M_2, and M_3	Multiframe Alignment Bits
F_{XY}	Subframe Alignment Bits
C_{11}	Application Identification Channel (AIC)
C_{X1}, C_{X2}, and C_{X3}	Stuff Control Bits for Tributary #X

10.10.6.2 Transmit M23 DS3 Frame Generation

M23 DS3 frame generation receives the incoming payload data stream, and overwrites the entire DS3 overhead bit locations.

The multiframe alignment bits (M_1, M_2, and M_3) are overwritten with the values zero, one, and zero (010) respectively.

The subframe alignment bits (F_{X1}, F_{X2}, F_{X3}, and F_{X4}) are overwritten with the values one, zero, zero, and one (1001) respectively.

The X-bits (X_1 and X_2) are both overwritten with the Remote Defect Indicator (RDI). The RDI source is programmable (automatic, 1, or 0). If the T3.TCR.ARDID is one then the T3.TCR.TRDI register bit controls this bit. If the RDI is generated automatically (T3.TCR.ARDID=0), the X-bits are set to zero when one or more of the indicated alarm conditions is present, and set to one when all of the indicated alarm conditions are absent. Automatically setting RDI on LOS, SEF, LOF, or AIS is individually programmable (on or off).

The P-bits (P_1 and P_2) are both overwritten with the calculated payload parity from the previous DS3 frame. The payload parity is calculated by performing modulo 2 addition of all of the payload bits after all frame processing has been completed. P-bit generation is programmable (on or off). The P-bits will be generated if either P-bit generation is enabled or frame generation is enabled.

If C-bit generation is enabled (T3.TCR.CBGE), the bit C_{11} is overwritten with an alternating one zero pattern, and all of the other C-bits (C_{XY}) are overwritten with zeros. If C-bit generation is disabled, then all of the C-bit timeslots (C_{XY}) will be treated as payload data, and passed through. C-bit generation is programmable (on or off). Note: Overhead insertion may still overwrite the C-bit time slots even if C-bit generation is disabled.

Once all of the DS3 overhead bits have been overwritten, the data stream is passed on to error insertion. If frame generation is disabled, the incoming DS3 signal is passed on directly to error insertion. Frame generation is programmable (on or off). Note: P-bit generation may still be performed even if frame generation is disabled.

10.10.6.3 Transmit M23 DS3 Error Insertion

Error insertion inserts various types of errors into the different DS3 overhead bits. The types of errors that can be inserted are framing errors and P-bit parity errors.

The framing error insertion mode is programmable (F-bit, M-bit, SEF, or OOMF). An F-bit error is a single subframe alignment bit (F_{XY}) error. An M-bit error is a single multiframe alignment bit (M_1, M_2, or M_3) error. An SEF error is an error in all the subframe alignment bits in a subframe (F_{X1}, F_{X2}, F_{X3}, and F_{X4}). An OOMF error is a single multiframe alignment bit (M_1, M_2, or M_3) error in each of two consecutive DS3 frames.

A P-bit parity error is generated by is inverting the value of the P-bits (P_1 and P_2) in a single DS3 frame. P-bit parity error(s) can be inserted one error at a time, or continuously. The P-bit parity error insertion mode (single or continuous) is programmable.

Each error type (framing or P-bit parity) has a separate enable. Continuous error insertion mode inserts errors at every opportunity. Single error insertion mode inserts an error at the next opportunity when requested. The framing multi-error insertion modes (SEF or OOMF) insert the indicated number of error(s) at the next opportunities when requested; i.e., a single request will cause multiple errors to be inserts. The requests can be initiated by a register bit(TSEI) or by the manual error insertion input (TMEI). The error insertion request source (register or input) is programmable. The insertion of each particular error type is individually enabled. Once all error insertion has been performed, the data stream is passed on to overhead insertion.

10.10.6.4 Transmit M23 DS3 Overhead Insertion

Overhead insertion can insert any (or all) of the DS3 overhead bits into the DS3 frame. The DS3 overhead bits X_1, X_2, P_1, P_2, M_X, F_{XY}, and C_{XY} can be sourced from the transmit overhead interface (TOHCLK, TOH, TOHEN, and TOHSOF). The P-bits (P_1 and P_2) are received as an error mask (modulo 2 addition of the input bit and the internally generated bit). The DS3 overhead insertion is fully controlled by the transmit overhead interface. If the transmit overhead data enable signal (TOHEN) is driven high, then the bit on the transmit overhead signal (TOH) is inserted into the output data stream. Insertion of bits using the TOH signal overwrites internal overhead insertion.

10.10.6.5 Transmit M23 DS3 AIS/Idle Generation

M23 DS3 AIS/Idle generation overwrites the data stream with AIS or an Idle signal. If transmit Idle is enabled, the data stream payload is forced to a 1100 pattern with two ones immediately following each DS3 overhead bit. M_1, M_2, and M_3 bits are overwritten with the values zero, one, and zero (010) respectively. F_{X1}, F_{X2}, F_{X3}, and F_{X4} bits are overwritten with the values one, zero, zero, and one (1001) respectively. X_1 and X_2 are overwritten with 11. P_1 and P_2 are overwritten with the calculated payload parity from the previous output DS3 frame. And, C_{31}, C_{32}, and C_{33} are overwritten with 000.

If transmit AIS is enabled, the data stream payload is forced to a 1010 pattern with a one immediately following each DS3 overhead bit. M_1, M_2, and M_3 bits are overwritten with the values zero, one, and zero (010) respectively. F_{X1}, F_{X2}, F_{X3}, and F_{X4} bits are overwritten with the values one, zero, zero, and one (1001) respectively. X_1 and X_2 are overwritten with 11. P_1 and P_2 are overwritten with the calculated payload parity from the previous DS3 frame. And, C_{X1}, C_{X2}, and C_{X3} are overwritten with 000. AIS will overwrite a transmit Idle signal.

10.10.6.5.1 Receive M23 DS3 Frame Format

The DS3 frame format is shown in Figure 10-38. The X_1 and X_2 are the Remote Defect Indication (RDI) bits (also referred to as the far-end SEF/AIS bits). P_1 and P_2 are the parity bits used for line error monitoring. M_1, M_2, and M_3 are the multiframe alignment bits that define the multiframe boundary. F_{XY} are the subframe alignment bits that define the subframe boundary. Note: Both the M-bits and F-bits define the DS3 frame boundary. C_{11} is the Application Identification Channel (AIC). C_{X1}, C_{X2}, and C_{X3} are the stuff control bits for tributary #X.

10.10.6.5.2 Receive M23 DS3 Overhead Extraction

Overhead extraction extracts all of the DS3 overhead bits from the M23 DS3 frame. All the DS3 overhead bits X_1, X_2, P_1, P_2, M_X, F_{XY}, and C_{XY} are output on the receive overhead interface (ROH, ROHSOF, and ROHCLK). The P_1 and P_2 bits are output as an error indication (modulo 2 addition of the calculated parity and the bit). In addition, the Application Identification Channel (AIC) is extracted from the C_{11} bit and stored in a register. The AIC is set to one (C-bit format) if the C_{11} bit is set to one in thirty-one consecutive multiframes. The AIC is set to zero (M23 format) if the C_{11} bit is set to zero in four of the last thirty-one consecutive multiframes. Note: The stored AIC bit must not change when an LOS, OOF, or AIS condition is present.

10.10.6.5.3 Receive DS3 Downstream AIS Generation

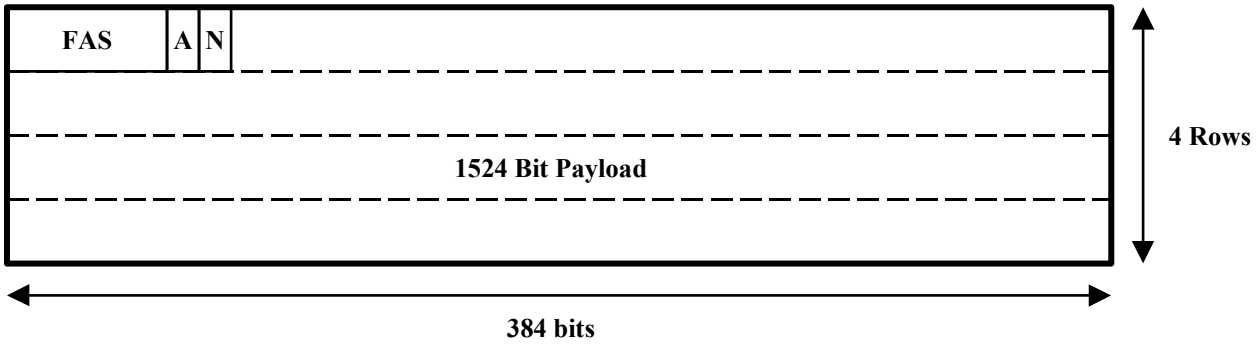
Downstream DS3 AIS (all ‘1’s) can be automatically generated on an OOF, LOS, or AIS condition or manually inserted. If automatic downstream AIS is enabled, downstream AIS is inserted when an LOS or AIS condition is declared, or no earlier than 2.25 ms and no later than 2.75 ms after an OOF condition is declared. Automatic downstream AIS is programmable (on or off). If manual downstream AIS insertion is enabled, downstream AIS is inserted. Manual downstream AIS insertion is programmable (on or off). Downstream AIS is removed when all OOF, LOS, and AIS conditions are terminated and manual downstream AIS insertion is disabled.

10.10.7 G.751 E3 Framer/Formatter

10.10.7.1 Transmit G.751 E3 Frame Processor

The G.751 E3 frame format is shown in Figure 10-41. FAS is the Frame Alignment Signal. A is the Alarm indication bit used to indicate the presence of an alarm to the remote terminal equipment. N is the National use bit reserved for national use.

Figure 10-41. G.751 E3 Frame Format



10.10.7.2 Transmit G.751 E3 Frame Generation

G.751 E3 frame generation receives the incoming payload data stream, and overwrites the entire E3 overhead bit locations.

The first 10 bits of the frame are overwritten with the frame alignment signal (FAS), which has a value of 1111010000b.

The eleventh bit of the frame is overwritten with the alarm indication (A) bit. The A bit can be generated automatically, sourced from the transmit FEAC controller, set to one, or set to zero. The A bit source is programmable (automatic, FEAC, 1, or 0). If the A bit is generated automatically, it is set to one when one or more of the indicated alarm conditions is present, and set to zero when all of the indicated alarm conditions are absent. Automatically setting RDI on LOS, LOF, or AIS is individually programmable (on or off).

The twelfth bit of the frame is overwritten with the national use (N) bit. The N bit can be sourced from the transmit FEAC controller, sourced from the transmit HDLC overhead controller, set to one, or set to zero. The N bit source is programmable (FEAC, HDLC, 1, or 0). Note: The FEAC controller will source one bit per frame regardless of whether the A bit only, the N bit only, or both are programmed to be sourced from the FEAC controller.

Once all of the E3 overhead bits have been overwritten, the data stream is passed on to error insertion. If frame generation is disabled, the incoming E3 signal is passed on directly to error insertion. Frame generation is programmable (on or off).

10.10.7.3 Transmit G.751 E3 Error Insertion

Error insertion inserts framing errors into the frame alignment signal (FAS). The type of error(s) inserted into the FAS is programmable (errored FAS bit or errored FAS). An errored FAS bit is a single bit error in the FAS. An errored FAS is an error in all ten bits of the FAS (a value of 0000101111b is inserted in the FAS). Framing error(s) can be inserted one error at a time, or in four consecutive frames. The framing error insertion number (single or four) is programmable.

Single error insertion mode inserts an error at the next opportunity when requested. The multi-error insertion mode inserts the indicated number of errors at the next opportunities when requested. I.e., a single request will cause multiple errors to be inserted. The requests can be initiated by a register bit (TSEI) or by the manual error insertion input (TMEI). The error insertion initiation type (register or input) is programmable. The insertion of each particular error type is individually enabled.

Once all error insertion has been performed, the data stream is passed on to overhead insertion.

10.10.7.4 Transmit G.751 E3 Overhead Insertion

Overhead insertion can insert any (or all) of the E3 overhead bits into the E3 frame. The FAS, A bit, and N bit can be sourced from the transmit overhead interface (TOHCLK, TOH, TOHEN, and TOHSOF). The E3 overhead insertion is fully controlled by the transmit overhead interface. If the transmit overhead data enable signal (TOHEN) is driven high, then the bit on the transmit overhead signal (TOH) is inserted into the output data stream. Insertion of bits using the TOH signal overwrites internal overhead insertion.

10.10.7.5 Transmit G.751 E3 AIS Generation

G.751 E3 AIS generation overwrites the data stream with AIS. If transmit AIS is enabled, the data stream (payload and E3 overhead) is forced to all ones.

10.10.7.6 Receive G.751 E3 Frame Processor

The G.751 E3 frame format is shown in Figure 10-41. FAS is the Frame Alignment Signal. A is the Alarm indication bit used to indicate the presence of an alarm to the remote terminal equipment. N is the National use bit reserved for national use.

10.10.7.6.1 Receive G.751 E3 Framing

G.751 E3 framing determines the G.751 E3 frame boundary. The frame boundary is found by identifying the frame alignment signal (FAS), which has a value of 1111010000b. The framer is an off-line framer that updates the data path frame counters when an out of frame (OOF) condition has been detected. The use of an off-line framer reduces the average time required to reframe, and reduces data loss caused by burst error. The G.751 E3 framer checks each bit position for the FAS. The frame boundary is set once the FAS is identified. Since, the FAS check is performed one bit at a time, up to 1536 checks may be needed to find the frame boundary. The data path frame counters are updated if an error free FAS is received for two additional frames, and an OOF condition is present, or if a manual frame resynchronization has been initiated.

10.10.7.6.2 Receive G.751 E3 Performance Monitoring

Performance monitoring checks the E3 frame for alarm conditions. The alarm conditions detected are OOF, LOF, COFA, LOS, AIS, RUA1, and RAI. An Out Of Frame (OOF) condition is declared when four consecutive frame alignment signals (FAS) contain one or more errors or at the next FAS check when a manual reframe is requested. An OOF condition is terminated when three consecutive FAS's are error free or the G.751 E3 framer updates the data path frame counters.

A Loss Of Frame (LOF) condition is declared by the LOF integration counter when it has been active for a total of *T* ms. The LOF integration counter is active (increments count) when an OOF condition is present, it is inactive (holds count) when an OOF condition is absent, and it is reset when an OOF condition is absent for *T* continuous ms. *T* is programmable (0, 1, 2, or 3). An LOF condition is terminated when an OOF condition is absent for *T* continuous ms.

A Change Of Frame Alignment (COFA) is declared when the G.751 E3 framer updates the data path frame counters with a frame alignment that is different from the current data path frame alignment.

A Loss Of Signal (LOS) condition is declared when the HDB3 encoder is active, and it declares an LOS condition. An LOS condition is terminated when the HDB3 encoder is inactive, or it terminates an LOS condition.

An Alarm Indication Signal (AIS) condition is declared when 4 or less zeros are detected in each of two consecutive frame periods. An AIS condition is terminated when 5 or more zeros are detected in each of two consecutive frame periods.

A Receive Unframed All 1's (RUA1) condition is declared if in each of 4 consecutive 2047 bit windows, five or less zeros are detected and an OOF condition is continuously present. A RUA1 condition is terminated if in each of 4 consecutive 2047 bit windows, six or more zeros are detected or an OOF condition is continuously absent.

A Remote Alarm Indication (RAI) condition is declared when four consecutive frames are received with the A bit (first bit after the FAS) set to one. An RAI condition is terminated when four consecutive frames are received with the A bit set to zero.

Only framing errors are accumulated. Framing errors are determined by comparing the FAS to its expected value. The type of framing errors accumulated is programmable (OOFs, bit, or word). An OOF error increments the count

whenever an OOF condition is first detected. A bit error increments the count once for each bit in the FAS that does not match its expected value (up to 10 per frame. A word error increments the count once for each FAS that does not match its expected value (up to 1 per frame).

The receive alarm indication (RAI) signal is high when one or more of the indicated alarm conditions is present, and low when all of the indicated alarm conditions are absent. Setting the receive alarm indication on LOS, OOF, LOF, or AIS is individually programmable (on or off).

10.10.7.6.3 Receive G.751 E3 Overhead Extraction

Overhead extraction extracts all of the E3 overhead bits from the G.751 E3 frame. The FAS, A bit, and N bit are output on the receive overhead interface (ROH, ROHSOF, and ROHCLK). In addition, the A bit is integrated and stored in a register along with a change indication, and can be output over the receive FEAC controller. The N bit is integrated and stored in a register along with a change indication, is sent to the receive HDLC overhead controller, and can also be sent to the receive FEAC controller. The bit sent to the receive FEAC controller is programmable (A or N).

10.10.7.6.4 Receive G.751 Downstream AIS Generation

Downstream G.751 E3 AIS can be automatically generated on an OOF, LOS, or AIS condition or manually inserted. If automatic downstream AIS is enabled, downstream AIS is inserted when an LOS, OOF, or AIS condition is declared. Automatic downstream AIS is programmable (on or off). If manual downstream AIS insertion is enabled, downstream AIS is inserted. Manual downstream AIS insertion is programmable (on or off). Downstream AIS is removed when all OOF, LOS, and AIS conditions are terminated and manual downstream AIS insertion is disabled. RPDT will be forced to all ones during downstream AIS.

10.10.8 G.832 E3 Framer/Formatter

10.10.8.1 Transmit G.832 E3 Frame Processor

The G.832 E3 frame format is shown in Figure 10-42.

Figure 10-42. G.832 E3 Frame Format

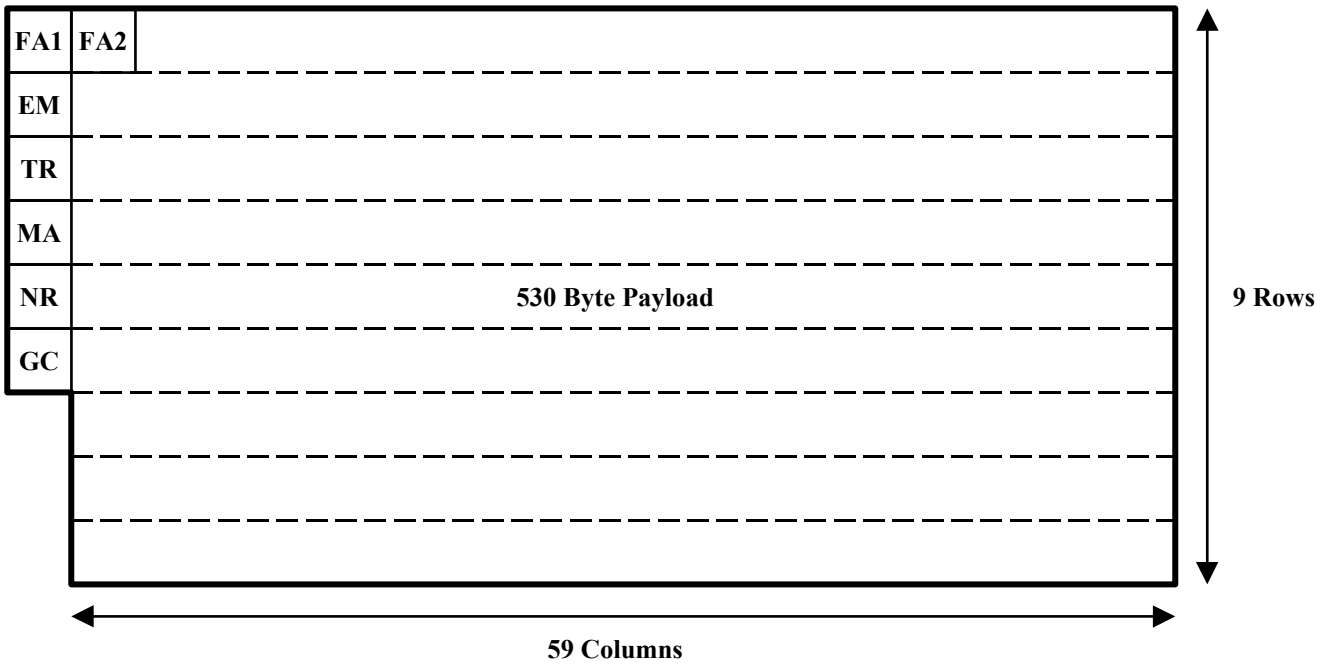
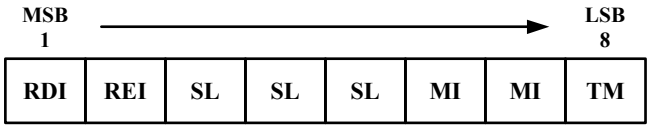


Figure 10-43. MA Byte Format



RDI - Remote Defect Indicator
REI - Remote Error Indicator
SL - Signal Label
MI - Multi-frame Indicator
TM - Timing Marker

Table 10-35 shows the function of each overhead bit in the DS3 Frame

Table 10-34. G.832 E3 Frame Overhead Bit Definitions

Byte	Definition
FA1, FA2	Frame Alignment bytes
EM	Error Monitoring byte
TR	Trail Trace byte
MA	Maintenance and Adaptation byte
NR	Network Operator byte
GC	General-Purpose Communication Channel byte

FA1 and FA2 are the Frame Alignment bytes. EM is the Error Monitoring byte used for path error monitoring. TR is the Trail Trace byte used for end-to-end connectivity verification. MA is the Maintenance and Adaptation byte used for far-end path status and performance monitoring.

NR is the Network Operator byte allocated for network operator maintenance purposes. GC is the General-purpose Communications Channel byte allocated for user communications purposes.

10.10.8.2 Transmit G.832 E3 Frame Generation

G.832 E3 frame generation receives the incoming payload data stream, and overwrites all of the E3 overhead byte locations.

The first two bytes of the first row in the frame are overwritten with the frame alignment bytes FA1 and FA2, which have a value of F6h and 28h respectively.

The first byte in the second row of the frame is overwritten with the EM byte which is a BIP-8 calculated over all of the bytes of the previous frame after all frame processing (frame generation, error insertion, overhead insertion, and AIS generation) has been performed. The first byte in the third row of the frame is overwritten with the TR byte which is input from the transmit trail trace controller.

The first byte in the fourth row of the frame is overwritten with the MA byte (see Figure 10-43), which consists of the RDI bit, REI bit, payload type, multiframe indicator, and timing source indicator.

The RDI (remote defect indicator) bit can be generated automatically, set to one, or set to zero. The RDI source is programmable (automatic, 1, or 0). If the RDI is generated automatically, it is set to one when one or more of the indicated alarm conditions are detected on the receive side, and set to zero when all of the indicated alarm conditions are absent. Automatically setting RDI on LOS, LOF, or AIS is individually programmable (on or off).

The REI (remote error indicator) bit can be generated automatically or inserted from a register bit (*E3G832.TCR*.TFEBE). The REI source is programmable (automatic or register bit). If REI is generated

automatically, it is set to one when at least one parity error has been detected on the receive side during the previous frame.

The payload type is sourced from a register. The three register bits are inserted in the third, fourth, and fifth bits of the MA byte in each frame.

The multiframe indicator and timing marker bits can be directly inserted from a 3-bit register or generated from a 4-bit register. The multiframe indicator and timing marker insertion type is programmable (direct or generated). When the multiframe indicator and timing marker bits are directly inserted, the three register bits are inserted in the last three bits of the MA byte in each frame. When the multiframe indicator and timing marker bits are generated, the four timing source indicator bits are transferred in a four-frame multiframe, MSB first. The multiframe indicator bits (sixth and seventh bits of the MA byte) identify the phase of the multiframe (00, 01, 10, or 11), and the timing marker bit (eighth bit of the MA byte) contains the corresponding timing source indicator bit (TMABR register bits TTI3, TTI2, TTI1, or TTI0 respectively). Note: The initial phase of the multiframe is arbitrarily chosen.

The first byte in the fifth row of the frame is overwritten with the NR byte which can be sourced from a register, from the transmit FEAC controller, or from the transmit HDLC controller. The NR byte source is programmable (register, FEAC, or HDLC). Note: The HDLC controller will source eight bits per frame period regardless of whether the NR byte only, GC byte only, or both are programmed to be sourced from the HDLC controller.

The first byte in the sixth row of the frame is overwritten with the GC byte which can be sourced from a register or from the transmit HDLC controller. The GC byte source is programmable (register or HDLC).

Once all of the E3 overhead bytes have been overwritten, the data stream is passed on to error insertion. If frame generation is disabled, the incoming E3 signal is passed on directly to error insertion. Frame generation is programmable (on or off).

10.10.8.3 Transmit G.832 E3 Error Insertion

Error insertion inserts various types of errors into the different E3 overhead bytes. The types of errors that can be inserted are framing errors, BIP-8 parity errors, and Remote Error Indication (REI) errors.

The type of framing error(s) inserted is programmable (errored frame alignment bit or errored frame alignment word). A frame alignment bit error is a single bit error in the frame alignment word (FA1 or FA2). A frame alignment word error is an error in all sixteen bits of the frame alignment word (the values 09h and D7h are inserted in the FA1 and FA2 bytes respectively). Framing error(s) can be inserted one error at a time, or four consecutive frames. The framing error insertion mode (single or four) is programmable.

The type of BIP-8 error(s) inserted is programmable (errored BIP-8 bit, or errored BIP-8 byte). An errored BIP-8 bit is inverting a single bit error in the EM byte. An errored BIP-8 byte is inverting all eight bits in the EM byte. BIP-8 error(s) can be inserted one error at a time, or continuously. The BIP-8 error insertion mode (single or continuous) is programmable.

An REI error is generated by forcing the second bit of the MA byte to a one. REI error(s) can be inserted one error at a time, or continuously. The REI error insertion mode (single or continuous) is programmable.

Each error type (framing, BIP-8, or REI) has a separate enable. Continuous error insertion mode inserts errors at every opportunity. Single error insertion mode inserts an error at the next opportunity when requested. The framing multi-error insertion mode inserts the indicated number of errors at the next opportunities when requested. I.e., a single request will cause multiple errors to be inserted. The requests can be initiated by a register bit(TSEI) or by the manual error insertion input (TMEI). The error insertion request source (register or input) is programmable. The insertion of each particular error type is individually enabled. Once all error insertion has been performed, the data stream is passed on to overhead insertion.

10.10.8.4 Transmit G.832 E3 Overhead Insertion

Overhead insertion can insert any (or all) of the E3 overhead bytes into the E3 frame. The E3 overhead bytes FA1, FA2, EM, TR, MA, NR, and GC can be sourced from the transmit overhead interface (TOHCLK, TOH, TOHEN, and TOHSOF). The EM byte is sourced as an error mask (modulo 2 addition of the input EM byte and the generated EM byte). The E3 overhead insertion is fully controlled by the transmit overhead interface. If the transmit overhead data enable signal (TOHEN) is driven high, then the bit on the transmit overhead signal (TOH) is inserted into the output data stream. Insertion of bits using the TOH signal overwrites internal overhead insertion.

10.10.8.5 Transmit G.832 E3 AIS Generation

G.832 E3 AIS generation overwrites the data stream with AIS. If transmit AIS is enabled, the data stream (payload and E3 overhead) is forced to all ones.

10.10.8.6 Receive G.832 E3 Frame Processor

The G.832 E3 frame format is shown in Figure 10-42. FA1 and FA2 are the Frame Alignment bytes. EM is the Error Monitoring byte used for path error monitoring. TR is the Trail Trace byte used for end-to-end connectivity verification. MA is the Maintenance and Adaptation byte used for far-end path status and performance monitoring (See Figure 10-43). NR is the Network Operator byte allocated for network operator maintenance purposes. GC is the General-Purpose Communications Channel byte allocated for user communications purposes.

10.10.8.7 Receive G.832 E3 Framing

G.832 E3 framing determines the G.832 E3 frame boundary. The frame boundary is found by identifying the frame alignment bytes FA1 and FA2, which have a value of F6h and 28h respectively. The framer is an off-line framer that updates the data path frame counters when an out of frame (OOF) condition has been detected. The use of an off-line framer reduces the average time required to reframe, and reduces data loss caused by burst error. The G.832 E3 framer checks each bit position for the frame alignment word (FA1 and FA2). The frame boundary is set once the frame alignment word is identified. Since, the frame alignment word check is performed one bit at a time, up to 4296 checks may be needed to find the frame boundary. The data path frame counters are updated if an error free frame alignment word is received for two additional frames, and an OOF condition is present.

10.10.8.8 Receive G.832 E3 Performance Monitoring

Performance monitoring checks the E3 frame for alarm conditions and errors. The alarm conditions detected are OOF, LOF, COFA, LOS, AIS, RUA1, and RDI. The errors accumulated are framing, parity, and Remote Error Indication (REI) errors. An Out Of Frame (OOF) condition is declared when four consecutive frame alignment words (FA1 and FA2) contain one or more errors, when 986 or more frames out of 1,000 frames has a BIP-8 block error, or at the next framing word check when a manual reframe is requested. An OOF condition is terminated when three consecutive frame alignment words (FA1 and FA2) are error free or the G.832 E3 framer updates the data path frame counters.

A Loss Of Frame (LOF) condition is declared by the LOF integration counter when it has been active for a total of *T* ms. The LOF integration counter is active (increments count) when an OOF condition is present, it is inactive (holds count) when an OOF condition is absent, and it is reset when an OOF condition is absent for *T* continuous ms. *T* is programmable (0, 1, 2, or 3). An LOF condition is terminated when an OOF condition is absent for *T* continuous ms.

A Change Of Frame Alignment (COFA) is declared when the G.832 E3 framer updates the data path frame counters with a frame alignment that is different from the current data path frame alignment.

A Loss Of Signal (LOS) condition is declared when the HDB3 encoder is active, and it declares an LOS condition. An LOS condition is terminated when the HDB3 encoder is inactive, or it terminates an LOS condition.

An Alarm Indication Signal (AIS) condition is declared when 7 or less zeros are detected in each of two consecutive frame periods that do not contain a frame alignment word. An AIS condition is terminated when 8 or more zeros are detected in each of two consecutive frame periods.

A Receive Unframed All 1's (RUA1) condition is declared if in each of 4 consecutive 2047 bit windows, five or less zeros are detected and an OOF condition is continuously present. A RUA1 condition is terminated if in each of 4 consecutive 2047 bit windows, six or more zeros are detected or an OOF condition is continuously absent.

A Remote Defect Indication (RDI) condition is declared when four consecutive frames are received with the RDI bit (first bit of MA byte) set to one. An RDI condition is terminated when four consecutive frames are received with the RDI bit set to zero.

Three types of errors are accumulated, framing, parity, and Remote Error Indication (REI) errors. Framing errors are determined by comparing FA1 and FA2 to their expected values. The type of framing errors accumulated is programmable (OOFs, bit, byte, or word). An OOF error increments the count whenever an OOF condition is first detected. A bit error increments the count once for each bit in FA1 and each bit in FA2 that does not match its expected value (up to 16 per frame). A byte error increments the count once for each FA byte (FA1 or FA2) that

does not match its expected value (up to 2 per frame). A word error increments the count once for each FA word (both FA1 and FA2) that does not match its expected value (up to 1 per frame).

Parity errors are determined by calculating the BIP-8 (8-Bit Interleaved Parity) of the current E3 frame (overhead and payload bytes), and comparing the calculated BIP-8 to the EM byte in the next frame. The type of parity errors accumulated is programmable (bit or block). A bit error increments the count once for each bit in the EM byte that does not match the corresponding bit in the calculated BIP-8 (up to 8 per frame). A block error increments the count if any bit in the EM byte does not match the corresponding bit in the calculated BIP-8 (up to 1 per frame).

REI errors are determined by the REI bit (second bit of MA byte). A one indicates an error and a zero indicates no errors.

The receive defect indication (RDI) alarm is transmitted when the receive framer detects one or more of the indicated alarm conditions. The RDI bit is not transmitted when all of the indicated alarm conditions are absent. The RDI bit in the MA byte of the G.832 overhead is set high in the transmit formatter to transmit the alarm. Setting the receive defect indication on LOS, OOF, LOF, or AIS is individually programmable (on or off).

The receive error indication (REI) bit of the MA byte in the transmit frame will transition from low to high once for each frame in which a parity error is detected by the receive framer.

10.10.8.9 Receive G.832 E3 Overhead Extraction

Overhead extraction extracts all of the E3 overhead bytes from the G.832 E3 frame. All of the E3 overhead bytes FA1, FA2, EM, TR, MA, NR, and GC are output on the receive overhead interface (ROH, ROHSOF, and ROHCLK).

The EM byte is output as an error indication (modulo 2 addition of the calculated BIP-8 and the EM byte.

The TR byte is sent to the receive trail trace controller.

The payload type (third, fourth, and fifth bits of the MA byte) is integrated and stored in a register with change and unstable indications. The integrated received payload type is also compared against an expected payload type. If the received and expected payload types do not match (see Table 10-35), a mismatch indication is set.

Table 10-35. Payload Label Match Status

EXPECTED	RECEIVED	STATUS
000	000	Match
000	001	Mismatch
000	XXX	Mismatch
001	000	Mismatch
001	001	Match
001	XXX	Match
XXX	000	Mismatch
XXX	001	Match
XXX	XXX	Match
XXX	YYY	Mismatch

XXX and YYY equal any value other than 000 or 001; XXX ≠ YYY

The multiframe indicator and timing marker bits (sixth, seventh, and eighth bits of the MA byte) can be integrated and stored in three register bits or extracted, integrated, and stored in four register bits. The bits (three or four) are stored with a change indication. The multiframe indicator and timing marker storage type is programmable (integrated or extracted). When the multiframe indicator and timing marker bits are integrated, the last three bits of the MA byte are integrated and stored in three register bits. When the multiframe indicator and timing marker bits are extracted, four timing source indicator bits are transferred in a four-frame multiframe, MSB first. The multiframe indicator bits (sixth and seventh bits of the MA byte) identify the phase of the multiframe (00, 01, 10, or 11). The

timing marker bit (eighth bit of the MA byte) contains the timing source indicator bit indicated by the multiframe indicator bits (first, second, third, or fourth bit respectively). The four timing source indicator bits are extracted from the multiframe, integrated, and stored in four register bits with unstable and change indications.

The NR byte is integrated and stored in a register along with a change indication, it is sent to the receive FEAC controller, and it can be sent to the receive HDLC controller. The byte sent to the receive HDLC controller is programmable (NR or GC).

The GC byte is integrated and stored in a register along with a change indication, and can be sent to the receive HDLC controller. The byte sent to the receive HDLC controller is programmable (NR or GC).

10.10.8.10 Receive G.832 Downstream AIS Generation

Downstream G.832 E3 AIS can be automatically generated on an OOF, LOS, or AIS condition or manually inserted. If automatic downstream AIS is enabled, downstream AIS is inserted when an LOS, OOF, or AIS condition is declared. Automatic downstream AIS is programmable (on or off). If manual downstream AIS insertion is enabled, downstream AIS is inserted. Manual downstream AIS insertion is programmable (on or off). Downstream AIS is removed when all OOF, LOS, and AIS conditions are terminated and manual downstream AIS insertion is disabled. RPDT will be forced to all ones during downstream AIS.

10.10.9 Clear-Channel Frame Processor

10.10.9.1 Transmit Clear-Channel AIS Generation

Clear-channel AIS generation overwrites the data stream with AIS. If transmit AIS is enabled, the data stream (payload) is forced to all ones.

10.10.9.2 Receive Clear-Channel Performance Monitoring

Performance monitoring checks the clear-channel signal for alarm conditions. The alarm conditions detected are LOS and RUA1. A Loss Of Signal (LOS) condition is declared when the B3ZS/HDB3 encoder is active, and it declares an LOS condition. A LOS condition is terminated when the B3ZS/HDB3 encoder is inactive, or it terminates an LOS condition.

A Receive Unframed All 1’s (RUA1) condition is declared if in each of 4 consecutive 2047 bit windows, five or less zeros are detected. A RUA1 condition is terminated if in each of 4 consecutive 2047 bit windows, six or more zeros are detected.

10.10.9.3 Receive Clear-channel Downstream AIS Generation

Downstream clear-channel AIS can be automatically generated on an LOS condition or manually inserted. If automatic downstream AIS is enabled, downstream AIS is inserted when an LOS condition is declared. Automatic downstream AIS is programmable (on or off). If manual downstream AIS insertion is enabled, downstream AIS is inserted. Manual downstream AIS insertion is programmable (on or off). Downstream AIS is removed when all LOS conditions are terminated and manual downstream AIS insertion is disabled. All bits will be forced to ones during downstream AIS.

10.11 HDLC Overhead Controller

10.11.1 General Description

The DS316x devices contain built-in HDLC controllers (one per port) with 256-byte FIFOs for insertion/extraction of DS3 PMDL, G.751 Sn bit and G.832 NR/GC bytes and PLCP NR/GC bytes

The HDLC Overhead Controller de-maps HDLC overhead packets from the DS3/E3 data stream in the receive direction and maps HDLC packets into the DS3/E3 data stream in the transmit direction.

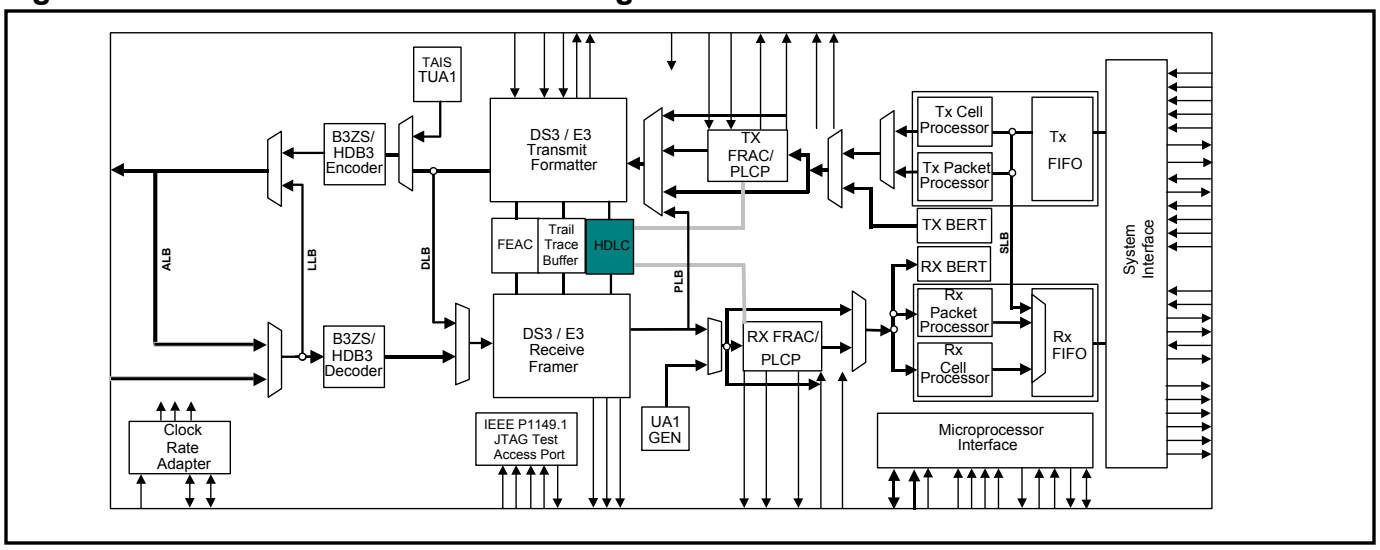
The receive direction performs packet processing and stores the packet data in the FIFO. It removes packet data from the FIFO and outputs the packet data to the microprocessor via the register interface.

The transmit direction inputs the packet data from the microprocessor via the register interface and stores the packet data in the FIFO. It removes the packet data from the FIFO and performs packet processing.

The bits in a byte are received MSB first, LSB last. When they are output serially, they are output MSB first, LSB last. The bits in a byte in an incoming signal are numbered in the order they are received, 1 (MSB) to 8 (LSB). However, when a byte is stored in a register, the MSB is stored in the lowest numbered bit (0), and the LSB is stored in the highest numbered bit (7). This is to differentiate between a byte in a register and the corresponding byte in a signal.

See Figure 10-44 for the location of HDLC controllers within the DS316x devices.

Figure 10-44. HDLC Controller Block Diagram



10.11.2 Features

- **Programmable inter-frame fill** – The inter-frame fill between packets can be all 1's or flags.
- **Programmable FCS generation/monitoring** – An FCS-16 can be generated and appended to the end of the packet, and the FCS can be checked and removed from the end of the packet.
- **Programmable bit reordering** – The packet data can be can be output MSB first or LSB first from the FIFO.
- **Programmable data inversion** – The packet data can be inverted immediately after packet processing on the transmit, and immediately before packet processing on the receive.
- **Fully independent transmit and receive paths**
- **Fully independent Line side and register interface timing** – The data storage can be read from or written to via the microprocessor interface while all line side clocks and signals are inactive, and read from or written to via the line side while all microprocessor interface clocks and signals are inactive.

10.11.3 Transmit FIFO

The Transmit FIFO block contains memory for 256 bytes of data with data status information and controller circuitry for reading and writing the memory. The Transmit FIFO controller functions include filling the memory, tracking the memory fill level, maintaining the memory read and write pointers, and detecting memory overflow and underflow conditions. The Transmit FIFO receives data and status from the microprocessor interface, and stores the data along with the data status information in memory. The Transmit Packet Processor reads the data and data status information from the Transmit FIFO. The Transmit FIFO also outputs FIFO fill status (empty/data storage available/full) via the microprocessor interface. All operations are byte based. The Transmit FIFO is considered empty when its memory does not contain any data. The Transmit FIFO is considered to have data storage available when its memory has a programmable number of bytes or more available for storage. The Transmit FIFO is considered full when it does not have any space available for storage. The Transmit FIFO accepts data from the register interface until full. If the Transmit FIFO is written to while the FIFO is full, the write is ignored, and a FIFO overflow condition is declared. The Transmit Packet Processor reads the Transmit FIFO. If the Transmit Packet Processor attempts to read the Transmit FIFO while it is empty, a FIFO underflow condition is declared.

10.11.4 Transmit HDLC Overhead Processor

The Transmit HDLC Overhead Processor accepts data from the Transmit FIFO, performs bit reordering, FCS processing, stuffing, packet abort sequence insertion, and inter-frame padding.

A byte is read from the Transmit FIFO with a packet end status. When a byte is marked with a packet end indication, the output data stream will be padded with FFh and marked with a FIFO empty indication if the Transmit FIFO contains less than two bytes or transmit packet start is disabled. Transmit packet start is programmable (on or off). When the Transmit Packet Processor reads the Transmit FIFO while it is empty, the output data stream is marked with an abort indication. Once the Transmit FIFO is empty, the output data stream will be padded with interframe fill until the Transmit FIFO contains two or more bytes of data and transmit packet start is enabled.

Bit reordering changes the bit order of each byte. If bit reordering is disabled, the outgoing 8-bit data stream DT[1:8] with DT[1] being the MSB and DT[8] being the LSB is input from the Transmit FIFO with the MSB in TFD[0] and the LSB in TFD[7] of the transmit FIFO data TFD[7:0]. If bit reordering is enabled, the outgoing 8-bit data stream DT[1:8] is input from the Transmit FIFO with the MSB in TFD[7] and the LSB in TFD[0] of the transmit FIFO data TFD[7:0]. DT[1] is the first bit transmitted on the outgoing data stream.

FCS processing calculates an FCS and appends it to the packet. FCS calculation is a CRC-16 calculation over the entire packet. The polynomial used for the CRC-16 is $x^{16} + x^{12} + x^5 + 1$. The CRC-16 is inverted after calculation, and appended to the packet. For diagnostic purposes, an FCS error can be inserted. This is accomplished by appending the calculated CRC-16 without inverting it. FCS error insertion is programmable (on or off). When FCS processing is disabled, the packet is output without appending an FCS. FCS processing is programmable (on or off).

Stuffing inserts control data into the packet to prevent packet data from mimicking flags. Stuffing is halted during FIFO empty periods. The 8-bit parallel data stream is multiplexed into a serial data stream, and bit stuffing is performed. Bit stuffing consists of inserting a '0' directly following any five contiguous '1's. Stuffing is performed from a packet start until a packet end.

Inter-frame padding inserts inter-frame fill between the packet start and end flags when the FIFO is empty. The inter-frame fill can be flags or '1's. If the inter-frame fill is flags, flags (minimum two) are inserted until a packet start is received. If the inter-frame fill is all '1's, an end flag is inserted, ‘1’s are inserted until a packet start is received, and a start flag is inserted after the ‘1’s. The number of '1's between the end flag and start flag may not be an integer number of bytes, however, the inter-frame fill will be at least 15 consecutive '1's. If the FIFO is not empty between a packet end and a packet start, then two flags are inserted between the packet end and packet start. The inter-frame padding type is programmable (flags or ‘1’s).

Packet abort insertion inserts a packet abort sequences as necessary. If a packet abort indication is detected, a packet abort sequence is inserted and inter-frame padding is done until a packet start is detected. The abort sequence is FFh.

Once all packet processing has been completed, the datastream is inserted into the DS3/E3 datastream at the proper locations. If transmit data inversion is enabled, the outgoing data is inverted after packet processing is performed. Transmit data inversion is programmable (on or off).

10.11.5 Receive HDLC Overhead Processor

The Receive HDLC Overhead Packet Processor accepts data from the DS3/E3 Framer or the PLCP Framer and performs packet delineation, inter-frame fill filtering, packet abort detection, destuffing, FCS processing, and bit reordering. If receive data inversion is enabled, the incoming data is inverted before packet processing is performed. Receive data inversion is programmable (on or off).

Packet delineation determines the packet boundary by identifying a packet start flag. Each time slot is checked for a flag sequence (7Eh). Once a flag is found, if it is identified as a start or end flag, and the packet boundary is set. There may be a single flag (both end and start) between packets, there may be an end flag and a start flag with a shared zero (011111101111110) between packets, there may be an end flag and a start flag (two flags) between packets, or there may be an end flag, inter-frame fill, and a start flag between packets. The flag check is performed one bit at a time.

Inter-frame fill filtering removes the inter-frame fill between a start flag and an end flag. All inter-frame fill is discarded. The inter-frame fill can be flags (01111110) or all '1's. When inter-frame fill is all ‘1’s, the number of '1's

between the end flag and the start flag may not be an integer number of bytes. When inter-frame fill is flags, the number of bits between the end flag and the start flag will be an integer number of bytes (flags). Any time there is less than 16 bits between two flags, the data will be discarded.

Packet abort detection searches for a packet abort sequence. Between a packet start flag and a packet end flag, if an abort sequence is detected, the packet is marked with an abort indication, and all subsequent data is discarded until a packet start flag is detected. The abort sequence is seven consecutive ones.

Packet abort detection searches for a packet abort sequence. Between a packet start flag and a packet end flag, if an abort sequence is detected, the packet is marked with an abort indication, and all subsequent data is discarded until a packet start flag is detected. The abort sequence is seven consecutive ones.

Destuffing removes the extra data inserted to prevent data from mimicking a flag or an abort sequence. After a start flag is detected, destuffing is performed until an end flag is detected. Destuffing consists of discarding any '0' that directly follows five contiguous '1's. After destuffing is completed, the serial bit stream is demultiplexed into an 8-bit parallel data stream and passed on with packet start, packet end, and packet abort indications. If there is less than eight bits in the last byte, an invalid packet status is set, and the packet is tagged with an abort indication. If a packet ends with five contiguous '1's, the packet will be processed as a normal packet regardless of whether or not the five contiguous '1's are followed by a '0'.

FCS processing checks the FCS, discards the FCS bytes, and marks FCS erred packets. The FCS is checked for errors, and the last two bytes are removed from the end of the packet. If an FCS error is detected, the packet is marked with an FCS error indication. The HDLC CONTROLLER performs FCS-16 checking. FCS processing is programmable (on or off). If FCS processing is disabled, FCS checking is not performed, and all of the packet data is passed on.

Bit reordering changes the bit order of each byte. If bit reordering is disabled, the incoming 8-bit data stream DT[1:8] with DT[1] being the MSB and DT[8] being the LSB is output to the Receive FIFO with the MSB in RFD[0] and the LSB in RFD[7] of the receive FIFO data RFD[7:0]. If bit reordering is enabled, the incoming 8-bit data stream DT[1:8] is output to the Receive FIFO with the MSB in RFD[7] and the LSB in RFD[0] of the receive FIFO data RFD[7:0]. DT[1] is the first bit received from the incoming data stream.

Once all of the packet processing has been completed, the 8-bit parallel data stream is passed on to the Receive FIFO with packet start, packet end, and packet error indications.

10.11.6 Receive FIFO

The Receive FIFO block contains memory for 256 bytes of data with data status information and controller circuitry for reading and writing the memory. The Receive FIFO Controller controls filling the memory, tracking the memory fill level, maintaining the memory read and write pointers, and detecting memory overflow and underflow conditions. The Receive FIFO accepts data and data status from the Receive Packet Processor and stores the data along with data status information in memory. The data is read from the receive FIFO via the microprocessor interface. The Receive FIFO also outputs FIFO fill status (empty/data available/full) via the microprocessor interface. All operations are byte based. The Receive FIFO is considered empty when it does not contain any data. The Receive FIFO is considered to have data available when there is a programmable number of bytes or more stored in the memory. The Receive FIFO is considered full when it does not have any space available for storage.

The Receive FIFO accepts data from the Receive Packet Processor until full. If a packet start is received while full, the data is discarded and a FIFO overflow condition is declared. If any other packet data is received while full, the current packet being transferred is marked with an abort indication, and a FIFO overflow condition is declared. Once a FIFO overflow condition is declared, the Receive FIFO will discard incoming data until a packet start is received while the Receive FIFO has sixteen or more bytes available for storage. If the Receive FIFO is read while the FIFO is empty, the read is ignored, and an invalid data indication given.

10.12 Trail Trace Controller

10.12.1 General Description

Each port has a dedicated Trail Trace Buffer for E3-G.832 or DS3/E3 PLCP link management

The Trail Trace Controller performs extraction and storage of the incoming G.832 or PLCP trail access point identifier in a 16-byte receive register.

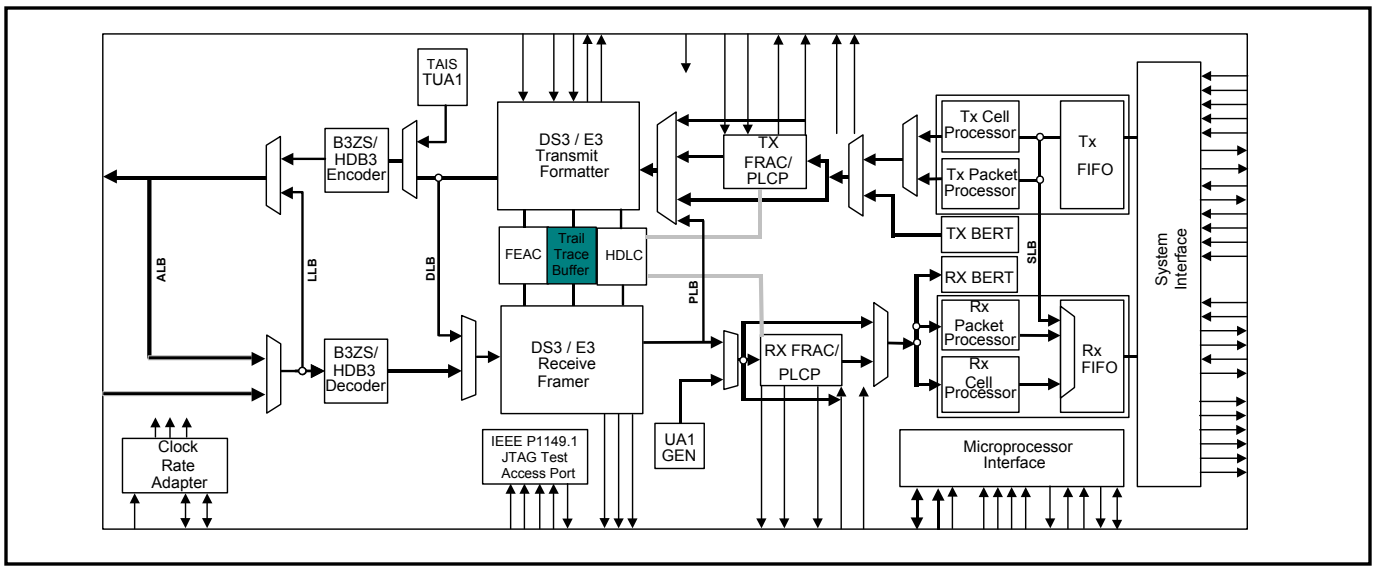
The Trail Trace Controller extracts/inserts E3-G.832 or PLCP trail access point identifiers using a 16-byte register(one for transmit, one for receive). (E3-G.832 and PLCP Framing are mutually exclusive, therefore one controller can be used for both.)

The Trail Trace Controller de-maps a 16-byte trail trace identifier from the E3-G.832 TR Byte of the overhead or PLCP datastream in the receive direction and maps a trace identifier into the E3-G.832 or PLCP datastream in the transmit direction.

The receive direction inputs the trace ID data stream, performs trace ID processing, and stores the trace identifier data in the data storage using line timing. It removes trace identifier data from the data storage and outputs the trace identifier data to the microprocessor via the microprocessor interface using register timing. The data is forced to all ones during LOS, LOF and AIS detection to eliminate false messages

The transmit direction inputs the trace identifier data from the microprocessor via the microprocessor interface and stores the trace identifier data in the data storage using register timing. It removes the trace identifier data from the data storage, performs trace ID processing, and outputs the trace ID data stream. See Figure 10-45 for the location of the Trail Trace Controller with the DS316x devices.

Figure 10-45. Trail Trace Controller Block Diagram



10.12.2 Features

- **Programmable trail trace ID** – The trail trace ID controller can be programmed to handle a 16-byte trail trace identifier (trail trace mode).
- **Programmable transmit trace ID** – All sixteen bytes of the transmit trail trace identifier are programmable.
- **Programmable receive expected trace ID** – A 16-byte expected trail trace identifier can be programmed. Both a mismatch and unstable indication are provided.
- **Programmable trace ID multiframe alignment** – The transmit side can be programmed to perform trail trace multiframe alignment insertion. The receive side can be programmed to perform trail trace multiframe synchronization.
- **Programmable bit reordering** – The trace identifier data can be output MSB first or LSB first from the data storage.
- **Programmable data inversion** – The trace identifier data can be inverted immediately after trace ID processing on the transmit side, and immediately before trail ID processing on the receive side.
- **Fully independent transmit and receive sides**
- **Fully independent Line side and register interface timing** – The data storage can be read from or written to via the microprocessor interface while all line side clocks and signals are inactive, and read from or written to via the line side while all microprocessor interface clocks and signals are inactive.

10.12.3 Functional Description

The bits in a byte are received most significant bit (MSB) first and least significant bit (LSB) last. When they are output serially, they are output MSB first and LSB last. The bits in a byte in an incoming signal are numbered in the order they are received, 1 (MSB) to 8 (LSB). However, when a byte is stored in a register, the MSB is stored in the highest numbered bit (7), and the LSB is stored in the lowest numbered bit (0). This is to differentiate between a byte in a register and the corresponding byte in a signal.

10.12.4 Transmit Data Storage

The Transmit Data Storage block contains memory for 16 bytes of data and controller circuitry for reading and writing the memory. The Transmit Data Storage controller functions include filling the memory and maintaining the memory read and write pointers. The Transmit Data Storage receives data from the microprocessor interface, and stores the data in memory. The Transmit Trace ID Processor reads the data from the Transmit Data Storage. The Transmit Data Storage contains the transmit trail trace identifier. Note: The contents of the transmit trail (path) trace identifier memory will be random data immediately after power-up, and will not change during a reset ($\overline{RST}$ or $\overline{DRST}$ low).

10.12.5 Transmit Trace ID Processor

The Transmit Trace ID Processor accepts data from Transmit Data Storage, processes the data according to the Transmit Trace ID mode, and outputs the serial trace ID data stream.

10.12.6 Transmit Trail Trace Processing

The Transmit Trail Trace Processing accepts data from the Transmit Data Storage performs bit reordering and multiframe alignment insertion.

Bit reordering changes the bit order of each byte. If bit reordering is disabled, the outgoing 8-bit data stream DT[1:8] with DT[1] being the MSB and DT[8] being the LSB is input from the Transmit Data Storage with the MSB in TTD[7] and the LSB in TTD[0] of the transmit trace ID data TTD[7:0]. If bit reordering is enabled, the outgoing 8-bit data stream DT[1:8] is input from the Transmit Data Storage with the MSB is in TTD[0] and the LSB is in TTD[7] of the transmit trace ID data TTD[7:0]. DT[1] is the first bit transmitted on the outgoing data stream.

Multiframe alignment insertion overwrites the MSB of each trail trace byte with the multiframe alignment signal. The MSB of the first byte in the trail trace identifier is overwritten with a one, the MSB of the other fifteen bytes in the trail trace identifier are overwritten with a zero. Multiframe alignment insertion is programmable (on or off).

If transmit data inversion is enabled, the outgoing data is inverted after trail trace processing is performed. Transmit data inversion is programmable (on or off). If transmit trail trace identifier idle (Idle) is enabled, the trail trace data is overwritten with all zeros. Transmit Idle is programmable (on or off).

10.12.7 Receive Trace ID Processor

The Receive Trace ID Processor receives the incoming serial trace ID data stream and processes the incoming data according to the Receive Trace ID mode, and passes the trace ID data on to Receive Data Storage.

The bits in a byte are received MSB first, LSB last. The bits in a byte in an incoming signal are numbered in the order they are received, 1 (MSB) to 8 (LSB). However, when a byte is stored in a register, the MSB is stored in the highest numbered bit (7), and the LSB is stored in the lowest numbered bit (0). This is to differentiate between a byte in a register and the corresponding byte in a signal.

10.12.8 Receive Trail Trace Processing

The Receive Trail Trace Processing accepts an incoming data line and performs trail trace alignment, trail trace extraction, expected trail trace comparison, and bit reordering. If receive data inversion is enabled, the incoming data is inverted before trail trace processing is performed. Receive data inversion is programmable (on or off).

Trail trace alignment determines the trail trace identifier boundary by identifying the multiframe alignment signal. The multiframe alignment signal (MAS) is located in the MSB of each byte (see Figure 10-46). The MAS bits are each checked for the multiframe alignment start bit, which is a one. Once a multiframe alignment start bit is found, the remaining fifteen bits of the MAS are verified as being zero. The MAS check is performed one byte at a time. Multiframe alignment is programmable (on or off). When multiframe alignment is disabled, the incoming bytes are sequentially stored starting with a random byte.

Figure 10-46. Trail Trace Byte (DT = Trail Trace Data)

Bit 1 MSB	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8 LSB
MAS or DT[1]	DT[2]	DT[3]	DT[4]	DT[5]	DT[6]	DT[7]	DT[8]

Trail trace extraction extracts the trail trace identifier from the incoming trail trace data stream, generates a trail trace identifier change indication, detects a trail trace identifier idle (Idle) condition, and detects a trail trace identifier unstable (TIU) condition. The trail trace identifier bytes are stored sequentially with the first byte (MAS equals 1 if trail trace alignment is enabled) being stored in the first byte of memory. If the exact same non-zero trail

trace identifier is received five consecutive times and it is different from the receive trail trace identifier, a receive trail trace identifier update is performed, and the receive trail trace identifier change indication is set.

An Idle condition is declared when an all zeros trail trace identifier is received five consecutive times. An Idle condition is terminated when a non-zero trail trace identifier is received five consecutive times or a TIU condition is declared. A TIU condition is declared if eight consecutive trail trace identifiers are received that do not match either the receive trail trace identifier or the previously stored current trail trace identifier. The TIU condition is terminated when a non-zero trail trace identifier is received five consecutive times or an Idle condition is declared.

Expected trail trace comparison compares the received and expected trail trace identifiers. The comparison is a 7-bit comparison of the seven least significant bits (DT[2:8] (see Figure 10-46) of each trail trace identifier byte (The multiframe alignment signal is ignored). If the received and expected trail trace identifiers do not match, a trail trace identifier mismatch (TIM) condition is declared. If they do match the TIM condition is terminated. The 16-byte expected trail trace identifier is programmable. Expected trail trace comparison is programmable (on or off). If multiframe alignment is disabled, expected trail trace comparison is disabled. Immediately after a reset, the receive trail trace identifier is invalid. All comparisons between the receive trail trace identifier and expected trail trace identifier will match (a TIM condition cannot occur) until after the first receive trail trace identifier update occurs.

Bit reordering changes the bit order of each byte. If bit reordering is disabled, the incoming 8-bit data stream DT[1:8] with DT[1] being the MSB and DT[8] being the LSB is output to the Receive Data Storage with the MSB in RTD[7] and the LSB in RTD[0] of the receive trace ID data RTD[7:0]. If bit reordering is enabled, the incoming 8-bit data stream DT[1:8] is output to the Receive Data Storage with the MSB in RTD[0] and the LSB in RTD[7] of the receive trace ID data RTD[7:0]. DT[1] is the first bit received from the incoming data stream.

Once all of the trail trace processing has been completed, the 8-bit parallel data stream is passed on to the Receive Data Storage.

10.12.9 Receive Data Storage

The Receive Data Storage block contains memory for 48 bytes of data, maintains data status information, and has controller circuitry for reading and writing the memory. The Receive Data Storage controller functions include filling the memory and maintaining the memory read and write pointers. The Receive Data Storage accepts data and data status from the Receive Trace ID Processor, stores the data in memory, and maintains data status information. The data is read from the Receive Data Storage via the microprocessor interface. The Receive Data Storage contains the current trail trace identifier, the receive trail trace identifier, and the expected trail trace identifier.

10.13 FEAC Controller

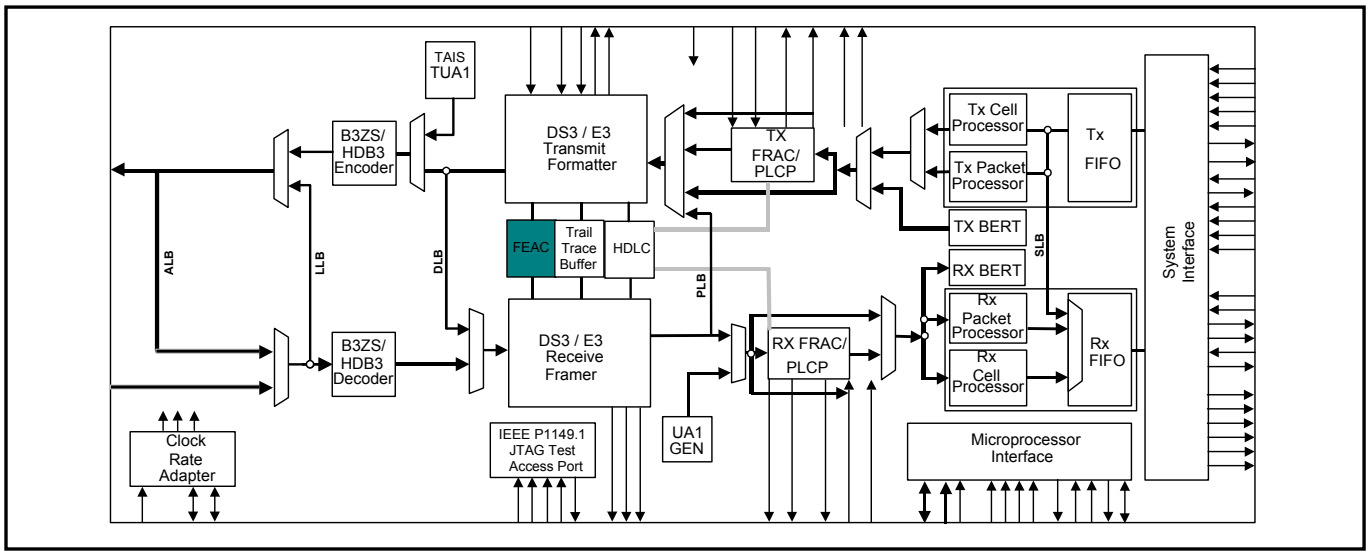
10.13.1 General Description

The FEAC Controller de-maps FEAC codewords from a DS3/E3 data stream in the receive direction and maps FEAC codewords into a DS3/E3 data stream in the transmit direction. The transmit direction de-maps FEAC codewords from a DS3/E3 data stream.

The receive direction performs FEAC processing, and stores the codewords in the FIFO using line timing. It removes the codewords from the FIFO and outputs them to the microprocessor via the register interface.

The transmit direction inputs codewords from the microprocessor via the register interface and stores the codewords. It removes the codewords and performs FEAC processing. See Figure 10-47 for the location of theFEAC Controller in the block diagram

Figure 10-47. FEAC Controller Block Diagram



10.13.2 Features

- **Programmable dual codeword output** – The transmit side can be programmed to output a single codeword ten times, one codeword ten times followed by a second codeword ten times, or a single codeword continuously.
- **Four codeword receive FIFO**
- **Fully independent transmit and receive paths**
- **Fully independent Line side and register side timing** – The FIFO can be read from or written to at the register interface side while all line side clocks and signals are inactive, and read from or written to at the line side while all register interface side clocks and signals are inactive.

10.13.3 Functional Description

The bits in a code are received MSB first, LSB last. When they are output serially, they are output MSB first, LSB last. The bits in a code in an incoming signal are numbered in the order they are received, 1 (MSB) to 6 (LSB). However, when a code is stored in a register, the MSB is stored in the lowest numbered bit (0), and the LSB is stored in the highest numbered bit (5). This is to differentiate between a code in a register and the corresponding code in a signal.

10.13.3.1 Transmit Data Storage

The Transmit Data Storage block contains the registers for two FEAC codes (C{1:6]) and controller circuitry for reading and writing the memory. The Transmit Data Storage receives data from the microprocessor interface, and stores the data in memory. The Transmit FEAC Processor reads the data from the Transmit Data Storage.

10.13.3.2 Transmit FEAC Processor

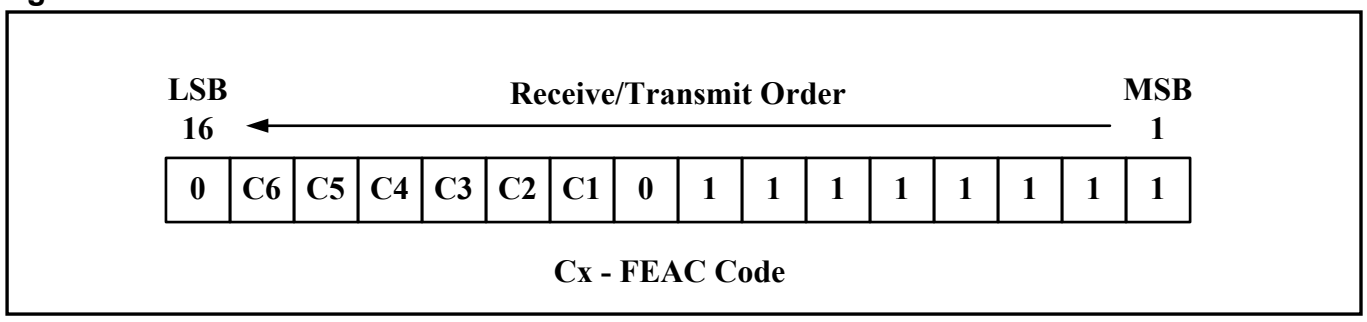
The Transmit FEAC Processor accepts data from the Transmit Data Storage performs FEAC processing. The FEAC codes are read from Transmit Data Storage with the MSB (C[1]) in TFCA[0] or TFCB[0], and the LSB (C[6]) in TFCA[5] or TFCB[5].

FEAC processing has four modes of operation (Idle, single code, dual code, and continuous code). In Idle mode, all ones are output on the outgoing FEAC data stream. In single code mode, the code from TFCA[5:0] is inserted into a codeword (see Figure 10-48), and sent 10 consecutive times. Once the 10 codewords have been sent, all ones are output. In dual code mode, the code from TFCA[5:0] is inserted into a codeword, and sent ten consecutive times. Then the code from TFCB[5:0] is inserted into a codeword, and sent 10 consecutive times. Once both codewords have both been sent 10 times, all ones are output. In continuous mode, the code from TFCA[5:0] is inserted into a codeword, and sent until the mode is changed

10.13.3.3 Receive FEAC Processor

The Receive FEAC Processor accepts an incoming data line and extracts all overhead and performs FEAC code extraction, and Idle detection.

Figure 10-48. FEAC Codeword Format



FEAC code extraction determines the codeword boundary by identifying the codeword sequence and extracts the FEAC code. A FEAC codeword is a repeating 16-bit pattern (see Figure 10-48). The codeword sequence is the pattern (0xxxxxx011111111) that contains each FEAC code (C[6:1]). Each time slot is checked for a codeword sequence. Once a codeword sequence is found, the FEAC code is checked. If the same FEAC code is received in three consecutive codewords without errors, the FEAC code detection indication is set, and the FEAC code is stored in the Receive FIFO with the MSB (C[1]) in RFF[0], and the LSB (C[6]) in RFF[5]. The FEAC code detection indication is cleared if two consecutively received FEAC codewords differ from the current FEAC codeword, or a FEAC Idle condition is detected.

Idle detection detects a FEAC Idle condition. A FEAC idle condition is declared if sixteen consecutive ones are received. The FEAC Idle condition is terminated when the FEAC code detection indication is set.

10.13.3.4 Receive FEAC FIFO

The Receive FIFO block contains memory for four FEAC codes (C{1:6]) and controller circuitry for reading and writing the memory. The Receive FIFO controller functions include filling the memory, tracking the memory fill level, maintaining the memory read and write pointers, and detecting memory overflow and underflow conditions. The Receive FIFO accepts data from the Receive FEAC Processor and stores the data in memory. The data is read from the receive FIFO via the microprocessor interface. The Receive FIFO also outputs FIFO fill status (empty) via the microprocessor interface. All operations are code based (six bits). The Receive FIFO is considered empty when it does not contain any data. The Receive FIFO accepts data from the Receive FEAC Processor until full. If a FEAC code is received while full, the data is discarded and a FIFO overflow condition is declared. If the Receive FIFO is read while the FIFO is empty, the read is ignored.

10.14 Line Encoder/Decoder

10.14.1 General Description

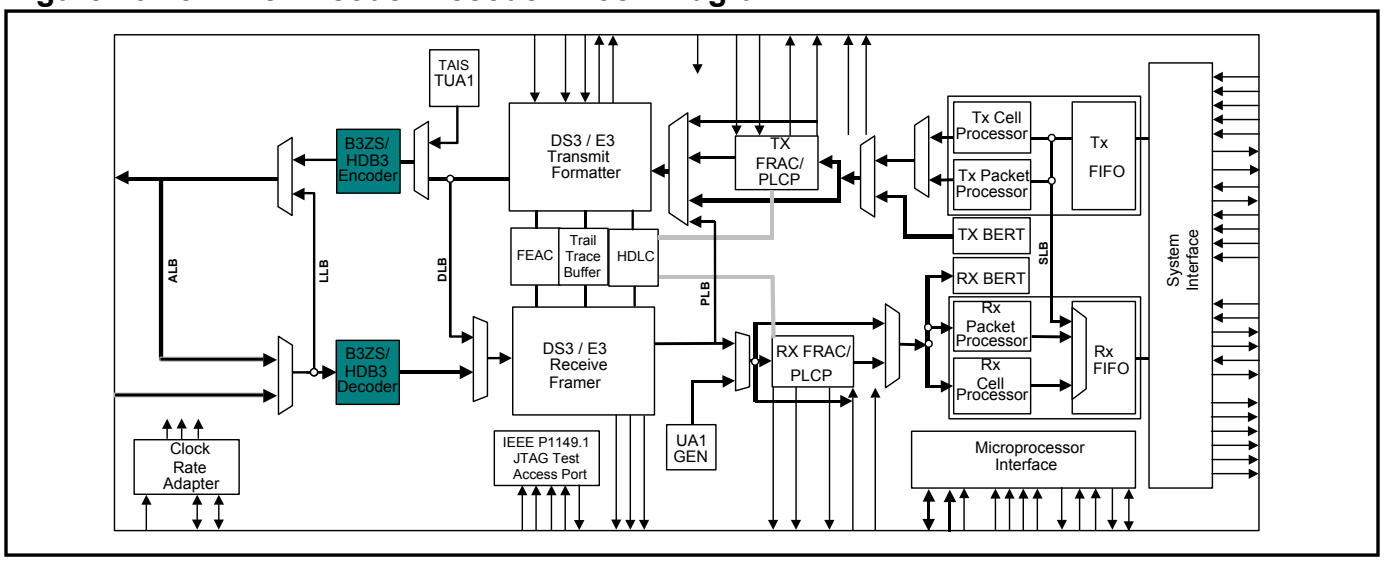
The B3ZS/HDB3 Decoder converts a bipolar signal to a unipolar signal in the receive direction. B3ZS/HDB3 Encoder converts a unipolar signal to a bipolar signal in the transmit direction.

In the transmit direction, the Encoder converts the unipolar signal to a bipolar signal, optionally performing zero suppression encoding (HDB3/B3ZS), optionally inserting errors, and outputs the bipolar signal.

In the receive direction, the Decoder receives a bipolar signal, monitors it for alarms and errors, optionally performing zero suppression decoding (HDB3/B3ZS), and converts it to a unipolar signal.

If the port line interface is configured for a Unipolar mode and the framer is not configured for one of the “-OHM” modes, the BPV detector will count pulses on the RLCVn pin. See Figure 10-49 for the locations of the Line Encoder/ Decoder block in the DS316x devices.

Figure 10-49. Line Encoder/Decoder Block Diagram



10.14.2 Features

- **Performs bipolar to unipolar encoding and decoding** – Converts a unipolar signal into an AMI bipolar signal (POS data, and NEG data) and vice versa.
- **Programmable zero suppression** – B3ZS or HDB3 zero suppression encoding and decoding can be performed, or the bipolar data stream can be left as an AMI encoded data stream.
- **Programmable receive zero suppression code format –** The signature of B3ZS or HDB3 is selectable**.**
- **Generates and detects alarms and errors** – In the receive direction, detects LOS alarm condition BPV errors, and EXZ errors. In the transmit direction, errors can be inserted into the outgoing data stream.

10.14.3 B3ZS/HDB3 Encoder

B3ZS/HDB3 Encoder performs unipolar to bipolar conversion and zero suppression encoding.

Unipolar to bipolar conversion converts the unipolar data stream into an AMI bipolar data stream (POS and NEG). In an AMI bipolar data stream a zero is represented by a zero on both the POS and NEG signals, and a one is represented by a one on a bipolar signal (POS or NEG), and a zero on the other bipolar signal (NEG or POS). Successive ones are represented by ones that are alternately output on the POS and NEG signals. i.e., if a one is represented by a one on POS and a zero on NEG, the next one will be represented by a one on NEG and a zero on POS.

Zero suppression encoding converts an AMI bipolar data stream into a B3ZS or HDB3 encoded bipolar data stream. A B3ZS encoded bipolar signal is generated by inserting a B3ZS signature into the bipolar data stream if both the POS and NEG signals are zero for three consecutive clock periods. An HDB3 encoded bipolar signal is generated by inserting an HDB3 signature into the bipolar data stream if both the POS and NEG signals are zero for four consecutive clock periods. Zero suppression encoding can be disabled which will result in AMI-coded data.

Error insertion is also performed. Error insertion inserts bipolar violation (BPV) or excessive zero (EXZ) errors onto the bipolar signal. A BPV error will be inserted when three consecutive ones occur. An EXZ error will be inserted when three (or four) consecutive zeros on the bipolar signal occur by inhibiting the insertion of a B3ZS (HDB3) signature. There will be at least one intervening pulse between consecutive BPV or EXZ errors. A single BPV or EXZ error inserted will be detected as a single BPV/EXZ error at the far-end, and will not cause any other type of error to be detected. For example, if a BPV error is inserted, the far-end should not also detect a data error.

10.14.4 Transmit Line Interface

The Transmit Line Interface accepts a bipolar data stream from the B3ZS/HDB3 Encoder, performs error insertion, and transmits the bipolar data stream.

Error insertion inserts BPV or EXZ errors into the bipolar signal. When a BPV error is to be inserted, the Transmit Line Interface waits for the next occurrence of three consecutive ones. The first bipolar one is generated according to the normal AMI rules. The second bipolar one is generated by transmitting the same values on TPOS and TNEG as the values for the first one. The third bipolar one is generated according to the normal AMI rules. When an EXZ error is to be inserted, the Transmit Line Interface waits for the next occurrence of three (four) consecutive zeros on the bipolar signal, and inhibits the insertion of a B3ZS (HDB3) signature. There must be at least one intervening one between consecutive BPV or EXZ errors. A single BPV or EXZ error inserted must be detected as a single BPV/EXZ error at the far-end, and not cause any other type of error to be detected. For example, if a BPV error is inserted, the far-end should not also detect a data error. If a second error insertion request of a given type (BPV or EXZ) is initiated before a previous request has been completed, the second request will be ignored.

The outgoing bipolar data stream consists of positive pulse data (TPOSn) and negative pulse data (TNEGn). TPOSn and TNEGn are updated on the rising edge of TLCLKn.

10.14.5 Receive Line Interface

The Receive Line Interface receives a bipolar signal. The incoming bipolar data line consists of positive pulse data (RPOSn), negative pulse data (RNEGn), and clock (RLCLKn) signals. RPOSn and RNEGn are sampled on the rising edge of RLCLKn. The incoming bipolar signal is checked for a Loss Of Signal (LOS) condition, and passed on to B3ZS/HDB3 Decoder. An LOS condition is declared if both RPOSn and RNEGn do not have any transitions for 192 clock cycles. The LOS condition is terminated after 192 clock cycles without any EXZ errors. Note: When zero suppression (B3ZS or HDB3) decoding is disabled, the LOS condition is cleared, and cannot be detected.

10.14.6 B3ZS/HDB3 Decoder

The B3ZS/HDB3 Decoder receives a bipolar signal from the RPOSn/RNEGn pins. The incoming bipolar signal is checked for a Loss of Signal (LOS) condition. An LOS condition is declared if both the positive pulse data and negative pulse data signals do not have any transitions for 192 clock cycles. The LOS condition is terminated after 192 clock cycles without any EXZ errors.

B3ZS/HDB3 Decoder performs EXZ detection, zero suppression decoding, BPV detection, and bipolar to unipolar conversion.

EXZ detection checks the bipolar data stream for excessive zeros (EXZ) errors. In B3ZS mode, an EXZ error is declared whenever there is an occurrence of 3 or more zeros. In HDB3 mode, an EXZ error is declared whenever there is an occurrence of 4 or more zeros. EXZ errors are accumulated in the EXZ counter (*LINE.REXZCR* register).

Zero suppression decoding converts B3ZS or HDB3 encoded bipolar data into an AMI bipolar signal. In B3ZS mode, the encoded bipolar signal is checked for a B3ZS signature. If a B3ZS signature is found, it is replaced with three zeros. In HDB3 mode, the encoded bipolar signal is checked for an HDB3 signature. If an HDB3 signature is found, it is replaced with four zeros. The format of both an HDB3 signature and a B3ZS signature is programmable. When LINE.RCR.REZSF = 0, the decoder will search for a zero followed by a BPV in B3ZS mode, and in HDB3 mode it will search for two zeros followed by a BPV. If LINE.RCR.REZSF = 1, the same criteria is applied with an additional requirement that the BPV must be the opposite polarity of the previous BPV. Refer to Figure 10-50 and Figure 10-51. Zero suppression decoding is also programmable (on or off). Note: Immediately after a reset or a LOS condition, the first B3ZS/HDB3 signature to be detected will not depend upon the polarity of any BPV contained within the signature.

Figure 10-50. B3ZS Signatures

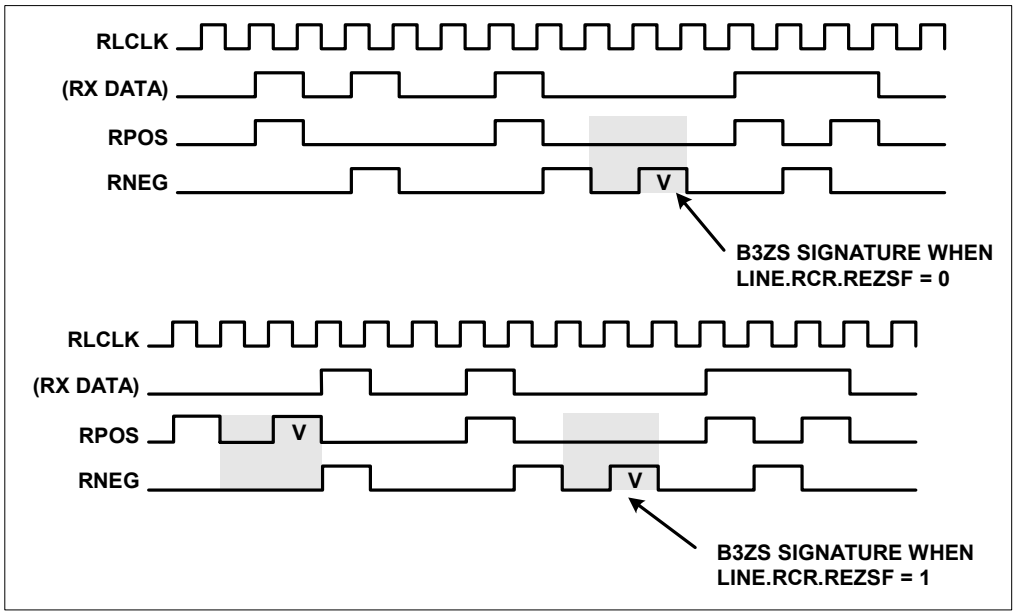
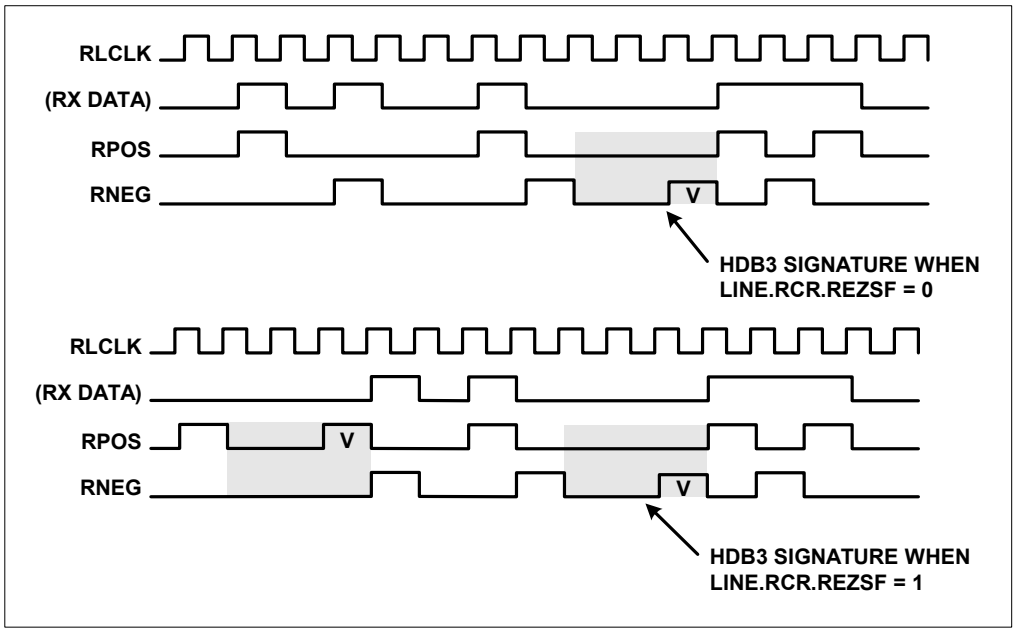


Figure 10-51. HDB3 Signatures



BPV detection checks the bipolar signal for bipolar violation (BPV) errors and E3 code violation (CV) errors. A BPV error is declared if two 1's are detected on RXP or RXN without an intervening 1 on RXN or RXP, and the 1's are not part of a B3ZS/HDB3 signature, or when both RXP and RXN are a one. An E3 coding violation is declared if consecutive BPVs of the same polarity are detected (ITU O.161 definition). E3 CVs are accumulated in the BPV counter (*LINE.RBPVCR* register) if E3 CV detection has been enabled (applicable only in HDB3 mode), otherwise, BPVs are accumulated in the BPV counter. If zero code suppression is disabled, the BPV counter will count all bipolar violations. The BPV counter will count pulses on the RLCVn pin when the device is configured for unipolar mode.

Immediately after a reset (or datapath reset) or a LOS condition, a BPV will not be declared when the first valid one (RPOS high and RNEG low, or RPOS low and RNEG high) is received. Bipolar to unipolar conversion converts the AMI bipolar data into a unipolar signal by OR'ing together the RXP and RXN signals.

10.15 BERT

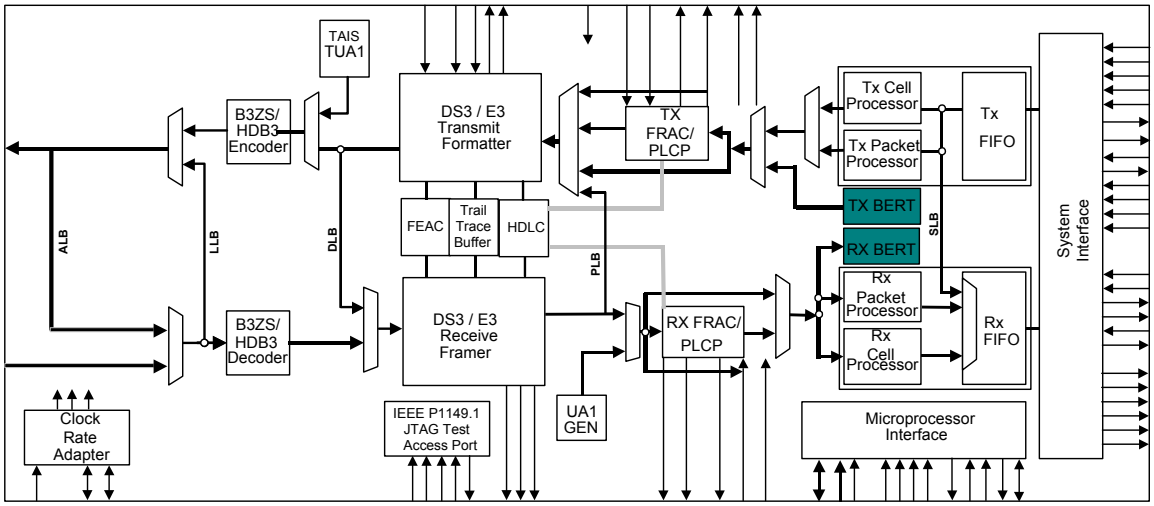
10.15.1 General Description

The BERT is a software-programmable test-pattern generator and monitor capable of meeting most error performance requirements for digital transmission equipment. It will generate and synchronize to pseudo-random patterns with a generation polynomial of the form $x^n + x^y + 1$, where n and y can take on values from 1 to 32 and to repetitive patterns of any length up to 32 bits.

The transmit direction generates the programmable test pattern, and inserts the test pattern payload into the data stream.

The receive direction extracts the test pattern payload from the receive data stream, and monitors the test pattern payload for the programmable test pattern. See Figure 10-52 for the location of the BERT Block within the DS316x devices.

Figure 10-52. BERT Block Diagram



10.15.2 Features

- **Programmable PRBS pattern** – The Pseudo Random Bit Sequence (PRBS) polynomial ($x^n + x^y + 1$) and seed are programmable (length n = 1 to 32, tap y = 1 to n - 1, and seed = 0 to $2^n - 1$).
- **Programmable repetitive pattern** – The repetitive pattern length and pattern are programmable (the length n = 1 to 32 and pattern = 0 to $2^n - 1$).
- **24-bit error count and 32-bit bit count registers**
- **Programmable bit error insertion** – Errors can be inserted individually, on a pin transition, or at a specific rate. The rate $1/10^n$ is programmable (n = 1 to 7).
- **Pattern synchronization at a 10^{-3} BER** – Pattern synchronization will be achieved even in the presence of a random Bit Error Rate (BER) of 10^{-3}.

10.15.3 Configuration and Monitoring

Set *PORT.CR1*.BENA = 1 to enable the BERT.

The following tables show how to configure the on-board BERT to send and receive common patterns. The BERT must be enabled before the pattern is loaded for the pattern load operation to take affect.

Table 10-36. Pseudo-Random Pattern Generation

PATTERN TYPE	BERT.PCR Register				BERT. PCR	BERT. SPR2	BERT. SPR1	BERT.CR
	PTF[4:0] (hex)	PLF[4:0] (hex)	PTS	QRSS				TPIC, RPIC
2^9-1 O.153 (511 type)	04	08	0	0	0x0408	0xFFFF	0xFFFF	0
2^{11}-1 O.152 and O.153 (2047 type)	08	0A	0	0	0x080A	0xFFFF	0xFFFF	0
2^{15}-1 O.151	0D	0E	0	0	0x0D0E	0xFFFF	0xFFFF	1
2^{20}-1 O.153	10	13	0	0	0x1013	0xFFFF	0xFFFF	0
2^{20}-1 O.151 QRSS	02	13	0	1	0x0253	0xFFFF	0xFFFF	0
2^{23}-1 O.151	11	16	0	0	0x1116	0xFFFF	0xFFFF	1

Table 10-37. Repetitive Pattern Generation

PATTERN TYPE	BERT.PCR Register				BERT. PCR	BERT. SPR2	BERT. SPR1
	PTF[4:0] (hex)	PLF[4:0] (hex)	PTS	QRSS			
all 1s	NA	00	1	0	0x0020	0xFFFF	0xFFFF
all 0s	NA	00	1	0	0x0020	0xFFFF	0xFFFE
alternating 1s and 0s	NA	01	1	0	0x0021	0xFFFF	0xFFFE
double alternating and 0s	NA	03	1	0	0x0023	0xFFFF	0xFFFC
3 in 24	NA	17	1	0	0x0037	0xFF20	0x0022
1 in 16	NA	0F	1	0	0x002F	0xFFFF	0x0001
1 in 8	NA	07	1	0	0x0027	0xFFFF	0xFF01
1 in 4	NA	03	1	0	0x0023	0xFFFF	0xFFF1

After configuring these bits, the pattern must be loaded into the BERT. This is accomplished via a zero-to-one transition on BERT.CR.TNPL and BERT.CR.RNPL

Monitoring the BERT requires reading the BERT.SR Register, which contains the Bit Error Count (BEC) bit and the Out of Synchronization (OOS) bit. The BEC bit will be one when the bit error counter is one or more. The OOS will be one when the receive pattern generator is not synchronized to the incoming pattern, which will occur when it receives a minimum 6 bit errors within a 64 bit window. The Receive BERT Bit Count Register (BERT.RBCR1) and the Receive BERT Bit Error Count Register (BERT.RBECR1) will be updated upon the reception of a Performance Monitor Update signal (e.g. BERT.CR.LPMU). This signal will update the registers with the values of the counters since the last update and will reset the counters. Please see section 10.4.5 for more details of the PMU.

10.15.4 Receive Pattern Detection

When the Receive BERT is enabled it can be used as an off-line monitor. The incoming datastream flows to the receive BERT as well as the Cell/Packet Processor. If it is not desired that the datastream flows to the Cell/Packet processor, the user should disable the Receive FIFO by setting the FIFO.RCR.RFRST bit.

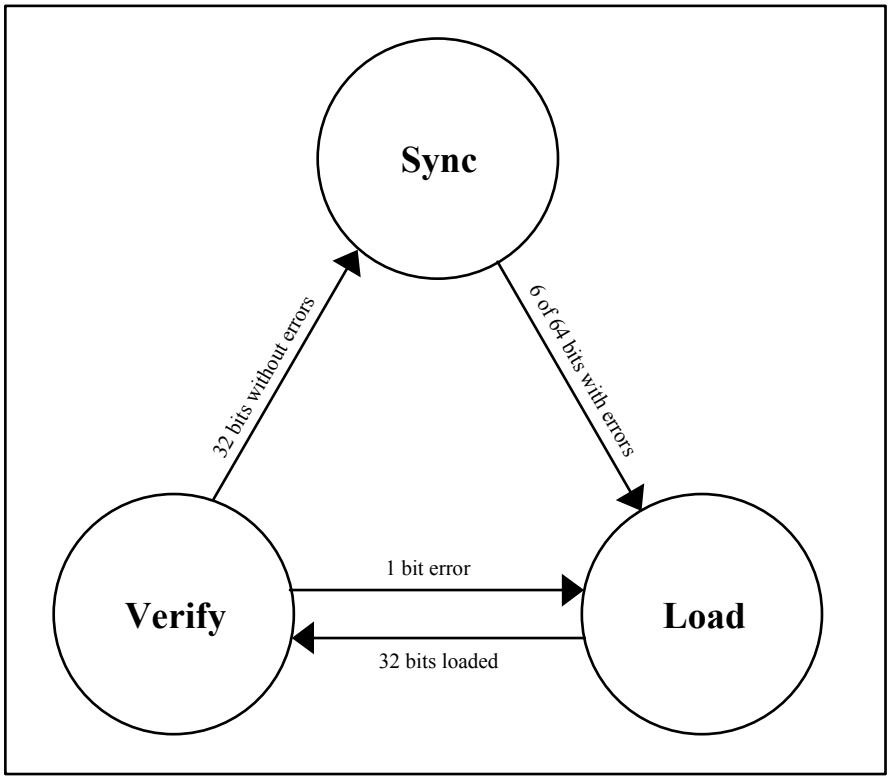
The Receive BERT receives only the payload data and synchronizes the receive pattern generator to the incoming pattern. The receive pattern generator is a 32-bit shift register that shifts data from the least significant bit (LSB) or bit 1 to the most significant bit (MSB) or bit 32. The input to bit 1 is the feedback. For a PRBS pattern (generating polynomial $x^n + x^y + 1$), the feedback is an XOR of bit n and bit y. For a repetitive pattern (length n), the feedback is bit n. The values for n and y are individually programmable (1 to 32). The output of the receive pattern generator is the feedback. If QRSS is enabled, the feedback is an XOR of bits 17 and 20, and the output will be forced to one if the next 14 bits are all zeros. QRSS is programmable (on or off). For PRBS and QRSS patterns, the feedback will be forced to one if bits 1 through 31 are all zeros. Depending on the type of pattern programmed, pattern detection performs either PRBS synchronization or repetitive pattern synchronization.

10.15.4.1 Receive PRBS Synchronization

PRBS synchronization synchronizes the receive pattern generator to the incoming PRBS or QRSS pattern. The receive pattern generator is synchronized by loading 32 data stream bits into the receive pattern generator, and then checking the next 32 data stream bits. Synchronization is achieved if all 32 bits match the incoming pattern. If at least six incoming bits in the current 64-bit window do not match the receive pattern generator, automatic pattern resynchronization is initiated. Automatic pattern resynchronization can be disabled.

Refer to Figure 10-53 for the PRBS synchronization diagram.

Figure 10-53. PRBS Synchronization State Diagram

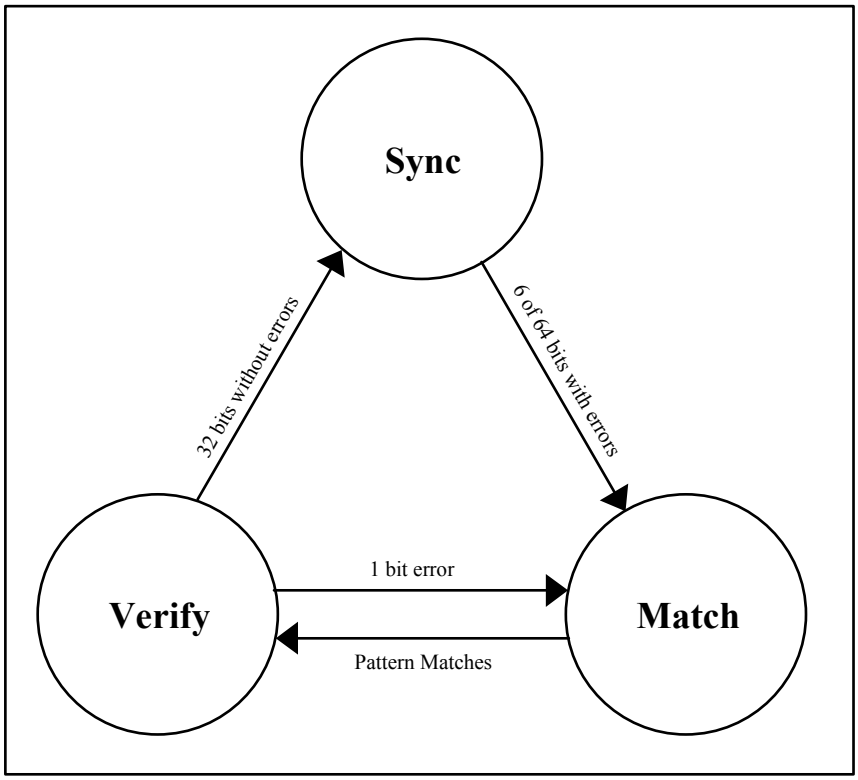


10.15.4.2 Receive Repetitive Pattern Synchronization

Repetitive pattern synchronization synchronizes the receive pattern generator to the incoming repetitive pattern. The receive pattern generator is synchronized by searching each incoming data stream bit position for the repetitive pattern, and then checking the next 32 data stream bits. Synchronization is achieved if all 32 bits match the incoming pattern. If at least six incoming bits in the current 64-bit window do not match the receive PRBS pattern generator, automatic pattern resynchronization is initiated. Automatic pattern resynchronization can be disabled.

Refer to Figure 10-54 for the repetitive pattern synchronization state diagram.

Figure 10-54. Repetitive Pattern Synchronization State Diagram



10.15.4.3 Receive Pattern Monitoring

Receive pattern monitoring monitors the incoming data stream for both an OOS condition and bit errors and counts the incoming bits. An Out Of Synchronization (OOS) condition is declared when the synchronization state machine is not in the “Sync” state. An OOS condition is terminated when the synchronization state machine is in the “Sync” state.

Bit errors are determined by comparing the incoming data stream bit to the receive pattern generator output. If they do not match, a bit error is declared, and the bit error and bit counts are incremented. If they match, only the bit count is incremented. The bit count and bit error count are not incremented when an OOS condition exists.

10.15.5 Transmit Pattern Generation

Pattern Generation generates the outgoing test pattern, and passes it onto Error Insertion. The transmit pattern generator is a 32-bit shift register that shifts data from the least significant bit (LSB) or bit 1 to the most significant bit (MSB) or bit 32. The input to bit 1 is the feedback. For a PRBS pattern (generating polynomial $x^n + x^y + 1$), the feedback is an XOR of bit n and bit y. For a repetitive pattern (length n), the feedback is bit n. The values for n and y are individually programmable (1 to 32). The output of the receive pattern generator is the feedback. If QRSS is enabled, the feedback is an XOR of bits 17 and 20, and the output will be forced to one if the next 14 bits are all zeros. QRSS is programmable (on or off). For PRBS and QRSS patterns, the feedback will be forced to one if bits 1 through 31 are all zeros. When a new pattern is loaded, the pattern generator is loaded with a seed/pattern value before pattern generation starts. The seed/pattern value is programmable ($0 – 2^n - 1$).

10.15.5.1 Transmit Error Insertion

Error insertion inserts errors into the outgoing pattern data stream. Errors are inserted one at a time or at a rate of one out of every 10^n bits. The value of n is programmable (1 to 7 or off). Single bit error insertion can be initiated from the microprocessor interface, or by the manual error insertion input (TMEI). The method of single error insertion is programmable (register or input). If pattern inversion is enabled, the data stream is inverted before the overhead/stuff bits are inserted. Pattern inversion is programmable (on or off).

11 OVERALL REGISTER MAP

The register addresses of the global, test and all four ports are concatenated to cover the address range of 000 to 7FF. The address map requires 11 bits of address, ADR[10:0]. The upper address bit A[10] is decoded for the DS3164 and DS3163 devices. The upper address bit A[10] it is not used by the DS3162 and DS3161 devices and must be tied low at the pin.

The register banks that are not marked with an "X" are not writeable and read back all zeros. Bits that are underlined are read-only; all other bits are read-write.

After Global Reset, all Registers will be reset to their default values.

When writing to registers with unused bits marked with "—", always write a zero to these unused bits and ignore the value read back from these bits.

Configuration registers can be written to and read from during a data path reset ($\overline{\text{DRST}}$ low, and $\overline{\text{RST}}$ high). However, all changes to these registers will be ignored during the data path reset. As a result, all initiating action requiring a "0 to 1" transition must be re-initiated after the data path reset is released.

All counters saturate at their maximum count. A counter register is updated by asserting (low to high transition) the performance monitoring update signal (RPMU). During the counter register update process, the performance monitoring status signal (RPMS) will be deasserted. The counter register update process consists of loading the counter register with the current count, resetting the counter, forcing the zero count status indication low for one clock period, and then asserting RPMS. No events shall be missed during an update procedure.

A latched bit is set when the associated event occurs, and remains set until it is cleared. Once cleared, a latched bit will not be set again until the associated event reoccurs (goes away and comes back). A latched on change bit is a latched bit that is set when the event occurs, and when it goes away. A latched status bit can be cleared using clear on read or clear on write techniques, selectable by the GL.CR1.LSBCRE bit. When clear on read is selected, the latched bits in a latched status register will be cleared after the register is read from. If the device is configured for 16-bit mode, all 16 latched status bits will be cleared. If the device is configured for 8-bit mode, only the 8 bits being accessed will be cleared. When clear on write is selected, the latched bits in a latched status register will be cleared when a logic 1 is written to that bit position. For example, writing a FFFFh to a 16-bit latched status register will clear any latched status bit, whereas writing a 0001h will only clear latched bit 0 of the latched status register.

Reserved bits and registers are implemented in a different mode. Reserved configuration bits and registers can be written and read, however they will not effect the operation of the current mode. Reserved status bits will be zero. Reserved latched status bits cannot be set, however, they may remain set or get set during a mode change. Reserved interrupt enable bits can be written and read, and can cause an interrupt if the associated latched status bit is set. Reserved counter registers and the associated counter will retain the values held before a mode change, however, the associated counter cannot be incremented. A performance monitor update will operate normally. If the data path reset is set during or after a mode change, the latched status bits and counter registers (with the associated counters) will be automatically cleared. If the data path reset is not used, then the latched status bits must be cleared via the register interface in the normal manner. And, the counter registers must be cleared by performing two performance monitor updates. The first to clear the associated counter, and load the current count into the counter register, and the second to clear the counter register.

Table 11-1. Global and Test Register Address Map

Address	Description
000 - 01F	Global registers, Section 12.1
020 – 02F	Unused
030 – 037	UTOPIA/POS-PHY Transmit System bus, Section 12.3
038 - 03F	UTOPIA/POS-PHY Receive System bus, Section 12.3.2
040 – 1FF	Port 1 Register Map
200 – 23F	Test Registers
240 – 3FF	Port 2 Register Map
400 – 43F	Test Registers
440 – 5FF	Port 3 Register Map
600 – 63F	Unused
640 – 6FF	Port 4 Register Map

Each port has a relative address range of 040h to 1FFh. The lower 000h to 03Fh address range is used for global, test and reserved registers. The following table is a map of the registers for each port. The address offset is from the start of each port range of 000h, 200h, 400h and 600h. In a DS3163, writes to registers in port 4 will be ignored and reads from port 4 registers will read back zero values. Similarly, in a DS3161, writes to registers in port 2 will be ignored and reads from port 2 will read back zero values.

NOTE: The $\overline{\text{RDY}}$ signal will not go active if the user attempts to read or write unused ports or unused registers not assigned to any design blocks. The $\overline{\text{RDY}}$ signal will go active if the user writes or reads reserved registers or unused registers within design blocks.

Table 11-2. Per Port Register Address Map

Port 1	Port 2	Port 3	Port 4
040 to 1FF	240 to 3FF	440 to 5FF	640 to 7FF

Address offset	Description
040 - 05F	Port common registers
060 – 07F	BERT
080 – 08B	Reserved
08C – 08F	B3ZS/HDB3 transmit line encoder
090 – 09F	B3ZS/HDB3 receive line decoder
0A0 – 0AF	HDLC Transmit
0B0 – 0BF	HDLC Receive
0C0 – 0CF	FEAC Transmit
0D0 – 0DF	FEAC Receive
0E0 – 0E7	Reserved
0E8 – 0EF	Trail Trace Transmit
0F0 – 0FF	Trail Trace Receive
100 – 117	Reserved
118 – 11F	DS3/E3 Framer Transmit
120 – 13F	DS3/E3 Framer Receive
140 – 147	DS3/E3 Fractional Transmit
148 – 14F	DS3/E3 Fractional Receive
150 – 15F	DS3/E3 PLCP Transmit
160 – 17F	DS3/E3 PLCP Receive
180 – 18F	UTOPIA/POS-PHY Transmit FIFO
190 – 19F	UTOPIA/POS-PHY Receive FIFO
1A0 – 1BF	Transmit Cell/Packet Processor
1C0 – 1FF	Receive Cell/Packet Processor

12 REGISTER MAPS AND DESCRIPTIONS

12.1 Registers Bit Maps

Note: In 8-bit mode, register bits[15:8] correspond to the upper byte, and register bits[7:0] correspond to the lower byte. For example, address 001h is the upper byte (bits [15:8]) and address 000h is the lower byte (bits [7:0]) for register GL.IDR in 8-bit mode.

All registers listed, including those designated Unused and Reserved, will cause the $\overline{RDY}$ signal to go low when written to or read from.

The "—" designation indicates that the bit is not assigned.

12.1.1 Global Register Bit Map

Table 12-1. Global Register Bit Map

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
000	000	GL.IDR	R	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
	001			ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
002	002	GL.CR1	RW	TMEI	MEIMS	GPM1	GPM0	PMU	LSBCRE	RSTDP	RST
	003			GWRM	INTM	DIREN	--	SIW1	SIW0	SIM1	SIM0
004	004	GL.CR2	RW	--	--	--	--	CLAD3	CLAD2	CLAD1	CLAD0
	005			--	--	--	G8KRS2	G8KRS1	G8KRS0	G8K0S	G8KIS
006-008	006-009	UNUSED		--	--	--	--	--	--	--	--
				--	--	--	--	--	--	--	--
00A	00A	GL.GIOCR	RW	GPIO4S1	GPIO4S0	GPIO3S1	GPIO3S0	GPIO2S1	GPIO2S0	GPIO1S1	GPIO1S0
	00B			GPIO8S1	GPIO8S0	GPIO7S1	GPIO7S0	GPIO6S1	GPIO6S0	GPIO5S1	GPIO5S0
00C	00C	UNUSED		--	--	--	--	--	--	--	--
	00D			--	--	--	--	--	--	--	--
010	010	GL.ISR	R	PISR4	PISR3	PISR2	PISR1	--	--	TSSR	GSR
	011			--	--	--	--	--	--	--	--
012	012	GL.ISRIE	RW	PISRIE4	PISRIE3	PISRIE2	PISRIE1	--	--	TSSRIE	GSRIE
	013										
014	014	GL.SR	R	--	--	--	--	--	--	CLOL	GPMS
	015			--	--	--	--	--	--	--	--
016	016	GL.SRL	RL	--	--	--	8KREFL	CLADL	ONESL	CLOLL	GPMSL
	017			--	--	--	--	--	--	--	--
018	018	GL.SRIE	R	--	--	--	--	--	ONESIE	CLOLIE	GPMSIE
	019			--	--	--	--	--	--	--	--
01A	01A	UNUSED		--	--	--	--	--	--	--	--
	01B			--	--	--	--	--	--	--	--
01C	01C	GL.GIORR	R	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1
	01D			--	--	--	--	--	--	--	--
01E	01E	UNUSED		--	--	--	--	--	--	--	--
	01F			--	--	--	--	--	--	--	--

Table 12-2. System Interface Bit Map

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
030	030	SI.TCR	RW	--	--	--	--	TPARP	TFLVI	TSBRE	THECT
	031			--	--	TXAD5	TXAD4	TXAD3	TXAD2	TXAD1	TXAD0
032	032	SI.TSRL	RL	--	--	--	--	--	--	TSCLKAL	TPREL
	033			--	--	--	--	--	--	--	--
034	034	SI.TSRIE	RW	--	--	--	--	--	--	--	TPREIE
	035			--	--	--	--	--	--	--	--
036	036	UNUSED									
	037										
038	038	SI.RCR1	RW	--	RXAD2	RXAD1	RXAD0	RPARP	RFLVI	RSBRE	RHECT
	039			--	--	--	--	--	RMDT2	RMDT1	RMDT0
03A	03A	SI.RCR2	RW	RLBL7	RLBL6	RLBL5	RLBL4	RLBL3	RLBL2	RLBL1	RLBL0
	03B			--	--	RMBL5	RMBL4	RMBL3	RMBL2	RMBL1	RMBL0
03C	03C	SI.RSRL	RL	--	--	--	--	--	--	--	RSCLKA
	03D										
03E	03E	UNUSED	R	--	--	--	--	--	--	--	--
	03F			--	--	--	--	--	--	--	--

Table 12-3. Port Register Bit Map

Note: J and K are variable dependent upon port.

	Port 1	Port 2	Port 3	Port 4
J	0	2	4	6
K	1	3	5	7

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
J40	J40	PORT.CR1	RW	TMEI	MEIM	--	PMUM	PMU	PD	RSTDP	RST
	J41			NAD	PAIS2	PAIS1	PAIS0	LAIS1	LAIS0	BENA	HDSEL
J42	J42	PORT.CR2	RW	RCDIS	PMCPE	FM5	FM4	FM3	FM2	FM1	FM0
	J43			TLEN	Reserved	Reserved	Reserved	RCDV8	LM	Reserved	Reserved
J44	J44	PORT.CR3	RW	P8KRS1	P8KRS0	P8KREF	LOOPT	CLADC	RFTS	TFTS	TLTS
	J45			--	--	RCLKS	RSOFOS	RPFPE	TCLKS	TSOFOS	TPFPE
J46	J46	PORT.CR4	RW	GPIOB3	GPIOB2	GPIOB1	GPIOB0	GPIOA3	GPIOA2	GPIOA1	GPIOA0
	J47			--	--	--	--	SLB	LBM2	LBM1	LBM0
J48	J48	UNUSED		--	--	--	--	--	--	--	--
	J49			--	--	--	--	--	--	--	--
J4A	J4A	PORT.INV1	RW	TOHI	TOHCKI	TSOFII	TNEGI	TPOSI	TLCKI	TCKOI	TCKII
	J4B			TPDEI	TPDTI	--	TPOHSI	TPOHEI	TPOHI	TOHSI	TOHEI
J4C	J4C	PORTINV2	RW	ROHI	ROHCKI	--	RNEGI	RPOSI	RLCKI	RCKOI	--
	J4D			--	RPDTI	RFOHEI	RPOHSI	--	RPOHI	ROHSI	--
J4E	J4E	UNUSED		--	--	--	--	--	--	--	--
	J4F			--	--	--	--	--	--	--	--
J50	J50	PORT.ISR	R	TTSR	FSR	HSR	BSR	SFSR	CPSR	PPSR	FMSR
	J51			--	--	--	--	--	--	PSR	LCSR
J52	J52	PORT.SR	R	--	--	--	--	--	Reserved	Reserved	PMS
	J53			--	--	--	--	--	--	--	--
J54	J54	PORT.SRL	RL	RLCLKA	TCLKIA	--	--	--	Reserved	Reserved	PMSL
	J55			--	--	--	--	--	--	--	--

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
J56	J56	PORT.SRIE	RW	--	--	--	--	--	Reserved	Reserved	PMSIE
	J57			--	--	--	--	--	--	--	--
J58-J5E	J58-J5F	UNUSED		--	--	--	--	--	--	--	--
				--	--	--	--	--	--	--	--

Table 12-4. BERT Register Bit Map

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
J60	J60	BERT.CR	RW	PMUM	LPMU	RNPL	RPIC	MPR	APRD	TNPL	TPIC
	J61			--	--	--	--	--	--	--	--
J62	J62	BERT.PCR	RW	--	QRSS	PTS	PLF4	PLF3	PLF2	PLF1	PLF0
	J63			--	--	--	PTF4	PTF3	PTF2	PTF1	PTF0
J64	J64	BERT.SPR1	RW	BSP7	BSP6	BSP5	BSP4	BSP3	BSP2	BSP1	BSP0
	J65			BSP15	BSP14	BSP13	BSP12	BSP11	BSP10	BSP9	BSP8
J66	J66	BERT.SPR2	RW	BSP23	BSP22	BSP21	BSP20	BSP19	BSP18	BSP17	BSP16
	J67			BSP31	BSP30	BSP29	BSP28	BSP27	BSP26	BSP25	BSP24
J68	J68	BERT.TEICR	RW	--	--	TEIR2	TEIR1	TEIR0	BEI	TSEI	MEIMS
	J69			--	--	--	--	--	--	--	--
J6A	J6A	UNUSED		--	--	--	--	--	--	--	--
	J6B			--	--	--	--	--	--	--	--
J6C	J6C	BERT.SR	R	--	--	--	--	PMS	--	BEC	OOS
	J6D			--	--	--	--	--	--	--	--
J6E	J6E	BERT.SRL	RL	--	--	--	--	PMSL	BEL	BECL	OOSL
	J6F			--	--	--	--	--	--	--	--
J70	J70	BERT.SRIE	RW	--	--	--	--	PMSIE	BEIE	BECIE	OOSIE
	J71			--	--	--	--	--	--	--	--
J72	J72	UNUSED		--	--	--	--	--	--	--	--
	J73			--	--	--	--	--	--	--	--
J74	J74	BERT.RBECR1	R	BEC7	BEC6	BEC5	BEC4	BEC3	BEC2	BEC1	BEC0
	J75			BEC15	BEC14	BEC13	BEC12	BEC11	BEC10	BEC9	BEC8
J76	J76	BERT.RBECR2	R	BEC23	BEC22	BEC21	BEC20	BEC19	BEC18	BEC17	BEC16
	J77			--	--	--	--	--	--	--	--
J78	J78	BERT.RBCR1	R	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0
	J79			BC15	BC14	BC13	BC12	BC11	BC10	BC9	BC8
J7A	J7A	BERT.RBCR2	R	BC23	BC22	BC21	BC20	BC19	BC18	BC17	BC16
	J7B			BC31	BC30	BC29	BC28	BC27	BC26	BC25	BC24
J7C-J7E	J7C	UNUSED		--	--	--	--	--	--	--	--
	J7F			--	--	--	--	--	--	--	--

Table 12-5. Line Register Bit Map

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
J8C	J8C	LINE.TCR	RW	--	--	--	TZSD	EXZI	BPVI	TSEI	MEIMS
	J8D			--	--	--	--	--	--	--	--
J8E	J8E	UNUSED		--	--	--	--	--	--	--	--
	J8F			--	--	--	--	--	--	--	--
J90	J90	LINE.RCR	RW	--	--	--	--	E3CVE	REZSF	RDZSF	RZSD
	J91			--	--	--	--	--	--	--	--
J92	J92	UNUSED		--	--	--	--	--	--	--	--
	J93			--	--	--	--	--	--	--	--
J94	J94	LINE.RSR	R	--	--	--	--	EXZC	--	BPVC	LOS
	J95			--	--	--	--	--	--	--	--
J96	J96	LINE.RSRL	RL	--	--	ZSCDL	EXZL	EXZCL	BPVL	BPVCL	LOSL
	J97			--	--	--	--	--	--	--	--
J98	J98	LINE.RSRIE	RW	--	--	ZSCDIE	EXZIE	EXZCIE	BPVIE	BPVCIE	LOSIE
	J99			--	--	--	--	--	--	--	--
J9A	J9A	UNUSED		--	--	--	--	--	--	--	--
	J9B			--	--	--	--	--	--	--	--
J9C	J9C	LINE.RBPVCR	R	BPV7	BPV6	BPV5	BPV4	BPV3	BPV2	BPV1	BPV0
	J9D			BPV15	BPV14	BPV13	BPV12	BPV11	BPV10	BPV9	BPV8
J9E	J9E	LINE.REXZCR	R	EXZ7	EXZ6	EXZ5	EXZ4	EXZ3	EXZ2	EXZ1	EXZ0
	J9F			EXZ15	EXZ14	EXZ13	EXZ12	EXZ11	EXZ10	EXZ9	EXZ8

12.1.2 HDLC Register Bit Map

Table 12-6. HDLC Register Bit Map

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
JA0	JA0	HDLC.TCR	RW	--	TPSD	TFEI	TIFV	TBRE	TDIE	TFPD	TFRST
	JA1			--	--	--	TDAL4	TDAL3	TDAL2	TDAL1	TDAL0
JA2	JA2	HDLC.TFDR	RW	--	--	--	--	--	--	--	TDPE
	JA3			TFD7	TFD6	TFD5	TFD4	TFD3	TFD2	TFD1	TFD0
JA4	JA4	HDLC.TSR	R	--	--	--	--	--	TFF	TFE	THDA
	JA5			--	--	TFFL5	TFFL4	TFFL3	TFFL2	TFFL1	TFFL0
JA6	JA6	HDLC.TSRL	RL	--	--	TFOL	TFUL	TPEL	--	TFEL	THDAL
	JA7			--	--	--	--	--	--	--	--
JA8	JA8	HDLC.TSRIE	RW	--	--	TFOIE	TFUIE	TPEIE	--	TFEIE	THDAIE
	JA9			--	--	--	--	--	--	--	--
JAA-JAE	JAA	UNUSED		--	--	--	--	--	--	--	--
	JAF			--	--	--	--	--	--	--	--
JB0	JB0	HDLC.RCR	RW	--	--	--	--	RBRE	RDIE	RFPD	RFRST
	JB1			--	--	--	RDAL4	RDAL3	RDAL2	RDAL1	RDAL0
JB2	JB2	UNUSED		--	--	--	--	--	--	--	--
	JB3			--	--	--	--	--	--	--	--
JB4	JB4	HDLC.RSR	R	--	--	--	--	--	RFF	RFE	RHDA
	JB5			--	--	--	--	--	--	--	--
JB6	JB6	HDLC.RSRL	RL	RFOL	--	--	RPEL	RPSL	RFFL	--	RHDAL
	JB7			--	--	--	--	--	--	--	--

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
JB8	JB8	HDLC.RSRIE	RW	RFOIE	--	--	RPEIE	RPSIE	RFFIE	--	RHDAIE
	JB9			--	--	--	--	--	--	--	--
JBA	JBA	UNUSED		--	--	--	--	--	--	--	--
	JBB			--	--	--	--	--	--	--	--
JBC	JBC	HDLC.RFDR	R	--	--	--	--	RPS2	RPS1	RPS0	RFDV
	JBD			RFD7	RFD6	RFD5	RFD4	RFD3	RFD2	RFD1	RFD0
JBE	JBE	UNUSED		--	--	--	--	--	--	--	--
	JBF			--	--	--	--	--	--	--	--

Table 12-7. FEAC Register Bit Map

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
JC0	JC0	FEAC.TCR	RW	--	--	--	--	--	TFCL	TFS1	TFS0
	JC1			--	--	--	--	--	--	--	--
JC2	JC2	FEAC.TFDR	RW	--	--	TFCA5	TFCA4	TFCA3	TFCA2	TFCA1	TFCA0
	JC3			--	--	TFCB5	TFCB4	TFCB3	TFCB2	TFCB1	TFCB0
JC4	JC4	FEAC.TSR	R	--	--	--	--	--	--	--	TFI
	JC5			--	--	--	--	--	--	--	--
JC6	JC6	FEAC.TSRL	RL	--	--	--	--	--	--	--	TFIL
	JC7			--	--	--	--	--	--	--	--
JC8	JC8	FEAC.TSRIE	RW	--	--	--	--	--	--	--	TFIIE
	JC9			--	--	--	--	--	--	--	--
JCA-JCE	JCA	UNUSED		--	--	--	--	--	--	--	--
	JCF			--	--	--	--	--	--	--	--
JD0	JD0	FEAC.RCR	RW	--	--	--	--	--	--	--	RFR
	JD1			--	--	--	--	--	--	--	--
JD2	JD2	UNUSED		--	--	--	--	--	--	--	--
	JD3			--	--	--	--	--	--	--	--
JD4	JD4	FEAC.RSR	R	--	--	--	--	RFFE	--	RFCD	RFI
	JD5			--	--	--	--	--	--	--	--
JD6	JD6	FEAC.RSRL	RL	--	--	--	--	--	RFFOL	RFCDL	RFIL
	JD7			--	--	--	--	--	--	--	--
JD8	JD8	FEAC.RSRIE	RW	--	--	--	--	--	RFFOIE	RFCDIE	RFIIE
	JD9			--	--	--	--	--	--	--	--
JDA	JDA	UNUSED		--	--	--	--	--	--	--	--
	JDB			--	--	--	--	--	--	--	--
JDC	JDC	FEAC.RFDR	R	RFFI	--	RFF5	RFF4	RFF3	RFF2	RFF1	RFF0
	JDD			--	--	--	--	--	--	--	--
JDE	JDE	UNUSED		--	--	--	--	--	--	--	--
	JDF			--	--	--	--	--	--	--	--

Table 12-8. Trail Trace Register Bit Map

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
JE8	JE8	TT.TCR	RW	--	--	--	Reserved	TMAD	TIDLE	TDIE	TBRE
	JE9			--	--	--	--	--	--	--	--
JEA	JEA	TT.TTIAR	R	--	--	Reserved	Reserved	TTIA3	TTIA2	TTIA1	TTIA0
	JEB			--	--	--	--	--	--	--	--
JEC	JEC	TT.TIR	R	TTD7	TTD6	TTD5	TTD4	TTD3	TTD2	TTD1	TTD0
	JED			--	--	--	--	--	--	--	--
JEE	JEE	UNUSED		--	--	--	--	--	--	--	--
	JEF			--	--	--	--	--	--	--	--
JF0	JF0	TT.RCR	RW	--	--	Reserved	Reserved	RMAD	RETCE	RDIE	RBRE
	JF1			--	--	--	--	--	--	--	--
JF2	JF2	TT.RTIAR	R	--	--	Reserved	Reserved	RTIA3	RTIA2	RTIA1	RTIA0
	JF3			--	--	Reserved	Reserved	ETIA3	ETIA2	ETIA1	ETIA0
JF4	JF4	TT.RSR	R	--	--	--	--	--	RTIM	RTIU	RIDL
	JF5			--	--	--	--	--	--	--	--
JF6	JF6	TT.RSRL	RL	--	--	--	--	RTICL	RTIML	RTIUL	RIDLL
	JF7			--	--	--	--	--	--	--	--
JF8	JF8	TT.RSRIE	RW	--	--	--	--	RTICIE	RTIMIE	RTIUIE	RIDLIE
	JF9			--	--	--	--	--	--	--	--
JFA	JFA	UNUSED		--	--	--	--	--	--	--	--
	JFB			--	--	--	--	--	--	--	--
JFC	JFC	TT.RIR	R	RTD7	RTD6	RTD5	RTD4	RTD3	RTD2	RTD1	RTD0
	JFD			--	--	--	--	--	--	--	--
JFE	JFE	TT.EIR	R	ETD7	ETD6	ETD5	ETD4	ETD3	ETD2	ETD1	ETD0
	JFF			--	--	--	--	--	--	--	--
K00-K16	K00-K117	RESERVED		--	--	--	--	--	--	--	--
				--	--	--	--	--	--	--	--

12.1.3 T3 Register Bit Map

Table 12-9. T3 Register Bit Map

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
K18	K18	T3.TCR	RW	--	--	TFEBE	AFEBED	TRDI	ARDID	TFGD	TAIS
	K19			--	--	--	PBGE	TIDLE	CBGD	--	--
K1A	K1A	T3.TEIR	RW	Reserved	CPEIE	PEI	FEIC1	FEIC0	FEI	TSEI	MEIMS
	K1B			--	--	--	--	CCPEIE	CPEI	CFBEIE	FBEI
K1C-K1E	K1C	RESERVED		--	--	--	--	--	--	--	--
	K1F			--	--	--	--	--	--	--	--
K20	K20	T3.RCR	RW	RAILE	RAILD	RAIOD	RAIAD	ROMD	LIP1	LIP0	FRSYNC
	K21			--	COVHD	MAOD	MDAISI	AAISD	ECC	FECC1	FECC0
K22	K22	RESERVED		--	--	--	--	--	--	--	--
	K23			--	--	--	--	--	--	--	--
K24	K24	T3.RSR1	R	OOMF	SEF	--	LOF	RAI	AIS	OOF	LOS
	K25			Reserved	Reserved	--	Reserved	T3FM	AIC	IDLE	RUA1
K26	K26	T3.RSR2	R	--	--	--	--	CPEC	FBEC	PEC	FEC
	K27			--	--	--	--	--	--	--	--

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
K28	K28	T3.RSRL1	RL	OOMFL	SEFL	COFAL	LOFL	RAIL	AISL	OOFL	LOSL
	K29			Reserved	Reserved	Reserved	Reserved	T3FML	AICL	IDLEL	RUA1L
K2A	K2A	T3.RSRL2	RL	--	--	--	--	CPECL	FBECL	PECL	FECL
	K2B			--	--	--	--	CPEL	FBEL	PEL	FEL
K2C	K2C	T3.RSRIE1	RW	OOMFIE	SEFIE	COFAIE	LOFIE	RAIIE	AISIE	OOFIE	LOSIE
	K2D			Reserved	Reserved	Reserved	Reserved	T3FMIE	AICIE	IDLEIE	RUA1IE
K2E	K2E	T3.RSRIE2	RW	--	--	--	--	CPECIE	FBECIE	PECIE	FECIE
	K2F			--	--	--	--	CPEIE	FBEIE	PEIE	FEIE
K30-K32	K30	RESERVED		--	--	--	--	--	--	--	--
	K33			--	--	--	--	--	--	--	--
K34	K34	T3.RFECR	R	FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0
	K35			FE15	FE14	FE13	FE12	FE11	FE10	FE9	FE8
K36	K36	T3.RPECR	R	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
	K37			PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8
K38	K38	T3.RFBECR	R	FBE7	FBE6	FBE5	FBE4	FBE3	FBE2	FBE1	FBE0
	K39			FBE15	FBE14	FBE13	FBE12	FBE11	FBE10	FBE9	FBE8
K3A	K3A	T3.RCPECR	R	CPE7	CPE6	CPE5	CPE4	CPE3	CPE2	CPE1	CPE0
	K3B			CPE15	CPE14	CPE13	CPE12	CPE11	CPE10	CPE9	CPE8
K3C-K3E	K3C	UNUSED		--	--	--	--	--	--	--	--
	K3F			--	--	--	--	--	--	--	--

12.1.4 E3 G.751 Register Bit Map

Table 12-10. E3 G.751 Register Bit Map

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
K18	K18	E3G751.TCR	RW	--	--	Reserved	Reserved	TABC1	TABC0	TFGD	TAIS
	K19			Reserved	--	--	Reserved	Reserved	Reserved	TNBC1	TNBC0
K1A	K1A	E3G751.TEIR	RW	Reserved	Reserved	Reserved	FEIC1	FEIC0	FEI	TSEI	MEIMS
	K1B			--	--	--	--	Reserved	Reserved	Reserved	Reserved
K1C-K1E	K1C	RESERVED		--	--	--	--	--	--	--	--
	K1F			--	--	--	--	--	--	--	--
K20	K20	E3G751.RCR	RW	RAILE	RAILD	RAIOD	RAIAD	ROMD	LIP1	LIP0	FRSYNC
	K21			Reserved	Reserved	DLS	MDAISI	AAISD	ECC	FECC1	FECC0
K22	K22	RESERVED		--	--	--	--	--	--	--	--
	K23			--	--	--	--	--	--	--	--
K24	K24	E3G751.RSR1	R	RAB	RNB	--	LOF	RAI	AIS	OOF	LOS
	K25			Reserved	Reserved	--	Reserved	Reserved	Reserved	Reserved	RUA1
K26	K26	E3G751.RSR2	R	--	--	--	--	Reserved	Reserved	Reserved	FEC
	K27			--	--	--	--	--	--	--	--
K28	K28	E3G751.RSRL1	RL	ACL	NCL	COFAL	LOFL	RAIL	AISL	OOFL	LOSL
	K29			Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RUA1L
K2A	K2A	E3G751.RSRL2	RL	--	--	--	--	Reserved	Reserved	Reserved	FECL
	K2B			--	--	--	--	Reserved	Reserved	Reserved	FEL
K2C	K2C	E3G751.RSRIE1	RW	ACIE	NCIE	COFAIE	LOFIE	RAIIE	AISIE	OOFIE	LOSIE
	K2D			Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RUA1IE
K2E	K2E	E3G751.RSRIE2	RW	--	--	--	--	Reserved	Reserved	Reserved	FECIE
	K2F			--	--	--	--	Reserved	Reserved	Reserved	FEIE

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
K30-K32	K30	RESERVED		--	--	--	--	--	--	--	--
	K33			--	--	--	--	--	--	--	--
K34	K34	E3G751.RFECR	R	FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0
	K35			FE15	FE14	FE13	FE12	FE11	FE10	FE9	FE8
K36-K3A	K36-K3B	RESERVED		--	--	--	--	--	--	--	--
				--	--	--	--	--	--	--	--
K3C-K3E	K3C-K3F	UNUSED		--	--	--	--	--	--	--	--
				--	--	--	--	--	--	--	--

12.1.5 E3 G.832 Register Bit Map

Table 12-11. E3 G.832 Register Bit Map

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
K18	K18	E3G832.TCR	RW	--	--	TFEBE	AFEBED	TRDI	ARDID	TFGD	TAIS
	K19			Reserved	--	--	Reserved	Reserved	TGCC	TNRC1	TNRC0
K1A	K1A	E3G832.TEIR	RW	Reserved	Reserved	Reserved	FEIC1	FEIC0	FEI	TSEI	MEIMS
	K1B			--	--	--	--	Reserved	Reserved	Reserved	Reserved
K1C	K1C	E3G832.TMABR	RW	TPT2	TPT1	TPT0	TTIGD	TTI3	TTI2	TTI1	TTI0
	K1D			--	--	--	--	--	--	--	--
K1E	K1E	E3G832.TNGBR	RW	TNR7	TNR6	TNR5	TNR4	TNR3	TNR2	TNR1	TNR0
	K1F			TGC7	TGC6	TGC5	TGC4	TGC3	TGC2	TGC1	TGC0
K20	K20	E3G832.RCR	RW	RDILE	RDILD	RDIOD	RDIAD	ROMD	LIP1	LIP0	FRSYNC
	K21			Reserved	PEC	DLS	MDAISI	AAISD	ECC	FECC1	FECC0
K22	K22	E3G832.RMACR	RW	--	--	--	--	EPT2	EPT1	EPT0	TIED
	K23			--	--	--	--	--	--	--	--
K24	K24	E3G832.RSR1	R	Reserved	Reserved	--	LOF	RAI	AIS	OOF	LOS
	K25			Reserved	TIU	--	RPTU	RPTM	Reserved	Reserved	RUA1
K26	K26	E3G832.RSR2	R	--	--	--	--	Reserved	FBEC	PEC	FEC
	K27			--	--	--	--	--	--	--	--
K28	K28	E3G832.RSRL1	RL	GCL	NRL	COFAL	LOFL	RAIL	AISL	OOFL	LOSL
	K29			Reserved	--	TIL	RPTUL	RPTML	RPTL	Reserved	RUA1L
K2A	K2A	E3G832.RSRL2	RL	--	--	--	--	Reserved	FBECL	PECL	FECL
	K2B			--	--	--	--	Reserved	FBEL	PEL	FEL
K2C	K2C	E3G832.RSRIE1	RW	GCIE	NRIE	COFAIE	LOFIE	RAIIE	AISIE	OOFIE	LOSIE
	K2D			Reserved	TIUIE	TIIE	RPTUIE	RPTMIE	RPTIE	Reserved	RUA1IE
K2E	K2E	E3G832.RSRIE2	RW	--	--	--	--	Reserved	FBECIE	PECIE	FECIE
	K2F			--	--	--	--	Reserved	FBEIE	PEIE	FEIE
K30	K30	E3G832.RMABR	R	--	RPT2	RPT1	RPT0	TI3	TI2	TI1	TI0
	K31			--	--	--	--	--	--	--	--
K32	K32	E3G832.RNGBR	R	RNR7	RNR6	RNR5	RNR4	RNR3	RNR2	RNR1	RNR0
	K33			RGC7	RGC6	RGC5	RGC4	RGC3	RGC2	RGC1	RGC0
K34	K34	E3G832.RFECR	R	FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0
	K35			FE15	FE14	FE13	FE12	FE11	FE10	FE9	FE8
K36	K36	E3G832.RPECR	R	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
	K37			PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8
K38	K38	E3G832.RFBER	R	FBE7	FBE6	FBE5	FBE4	FBE3	FBE2	FBE1	FBE0
	K39			FBE15	FBE14	FBE13	FBE12	FBE11	FBE10	FBE9	FBE8

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
K3A	K3A	RESERVED		--	--	--	--	--	--	--	--
	K3B			--	--	--	--	--	--	--	--
K3C-K3E	K3C-K3F	UNUSED		--	--	--	--	--	--	--	--
				--	--	--	--	--	--	--	--

12.1.6 Clear-Channel Register Bit Map

Table 12-12. Clear-Channel Register Bit Map

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
K18	K18	CC.TCR	RW	--	--	Reserved	Reserved	Reserved	Reserved	Reserved	TAIS
	K19			Reserved	--	--	Reserved	Reserved	Reserved	Reserved	Reserved
K1A-K1E	K1A	RESERVED		--	--	--	--	--	--	--	--
	K1F			--	--	--	--	--	--	--	--
K20	K20	CC.RCR	RW	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	K21			Reserved	Reserved	Reserved	MDAISI	AAISD	Reserved	Reserved	Reserved
K22	K22	RESERVED		--	--	--	--	--	--	--	--
	K23			--	--	--	--	--	--	--	--
K24	K24	CC.RSR1	R	Reserved	Reserved	--	Reserved	Reserved	Reserved	Reserved	LOS
	K25			Reserved	Reserved	--	Reserved	Reserved	Reserved	Reserved	RUA1
K26	K26	RESERVED		--	--	--	--	--	--	--	--
	K27			--	--	--	--	--	--	--	--
K28	K28	CC.RSRL1	RL	Reserved	Reserved	--	Reserved	Reserved	Reserved	Reserved	LOSL
	K29			Reserved	Reserved	--	Reserved	Reserved	Reserved	Reserved	RUA1L
K2A	K2A	RESERVED		--	--	--	--	--	--	--	--
	K2B			--	--	--	--	--	--	--	--
K2C	K2C	CC.RSRIE1	RW	Reserved	Reserved	--	Reserved	Reserved	Reserved	Reserved	LOSIE
	K2D			Reserved	Reserved	--	Reserved	Reserved	Reserved	Reserved	RUA1IE
K2E-K3A	K2E-K3B	RESERVED		--	--	--	--	--	--	--	--
				--	--	--	--	--	--	--	--
K3C-K3E	K3C-K3F	UNUSED		--	--	--	--	--	--	--	--
				--	--	--	--	--	--	--	--

12.1.7 Fractional Register Bit Map

Table 12-13. Fractional Register Bit Map

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
K40	K40	FRAC.TCR	RW	--	--	--	--	--	TFOSC1	TFOSC0	TSASS
	K41			--	--	--	--	--	--	--	--
K42	K42	FRAC.TDGSR	RW	TDGS7	TDGS6	TDGS5	TDGS4	TDGS3	TDGS2	TDGS1	TDGS0
	K43			--	--	--	TDGS12	TDGS11	TDGS10	TDGS9	TDGS8
K44	K44	FRAC.TSASR	RW	TSAS7	TSAS6	TSAS5	TSAS4	TSAS3	TSAS2	TSAS1	TSAS0
	K45			--	--	--	TSAS12	TSAS11	TSAS10	TSAS9	TSAS8
K46	K46	UNUSED		--	--	--	--	--	--	--	--
	K47			--	--	--	--	--	--	--	--
K48	K48	FRAC.RCR	RW	--	--	--	--	--	--	--	RSASS
	K49			--	--	--	--	--	--	--	--

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
K4A	K4A	FRAC.RDGSR	RW	RDGS7	RDGS6	RDGS5	RDGS4	RDGS3	RDGS2	RDGS1	RDGS0
	K4B			--	--	--	RDGS12	RDGS11	RDGS10	RDGS9	RDGS8
K4C	K4C	FRAC.RSASR	RW	RSAS7	RSAS6	RSAS5	RSAS4	RSAS3	RSAS2	RSAS1	RSAS0
	K4D			--	--	--	RSAS12	RSAS11	RSAS10	RSAS9	RSAS8
K4E	K4E	UNUSED		--	--	--	--	--	--	--	--
	K4F			--	--	--	--	--	--	--	--

Table 12-14. PLCP Register Bit Map

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
K50	K50	PLCP.TCR	RW	--	--	--	TMC1	TMC0	TF1C1	TF1C0	AREID
	K51			--	--	--	--	--	--	--	--
K52	K52	PLCP.TEIR	RW	--	--	FEE	FEIC1	FEIC0	FEI	TSEI	MEIMS
	K53			--	--	REIME	CREIIE	REIEI	PBEE	CPEIE	PEI
K54	K54	PLCP.TFGBR	RW	TREI3	TREI2	TREI1	TREI0	TRAI	TLSS2	TLSS1	TLSS0
	K55			TF17	TF16	TF15	TF14	TF13	TF12	TF11	TF10
K56	K56	PLCP.TM12BR	RW	TM17	TM16	TM15	TM14	TM13	TM12	TM11	TM10
	K57			TM27	TM26	TM25	TM24	TM23	TM22	TM21	TM20
K58	K58	PLCP.TZ12BR	RW	TZ17	TZ16	TZ15	TZ14	TZ13	TZ12	TZ11	TZ10
	K59			TZ27	TZ26	TZ25	TZ24	TZ23	TZ22	TZ21	TZ20
K5A	K5A	PLCP.TZ34BR	RW	TZ37	TZ36	TZ35	TZ34	TZ33	TZ32	TZ31	TZ30
	K5B			TZ47	TZ46	TZ45	TZ44	TZ43	TZ42	TZ41	TZ40
K5C	K5C	PLCP.TZ56BR	RW	TZ57	TZ56	TZ55	TZ54	TZ53	TZ52	TZ51	TZ50
	K5D			TZ67	TZ66	TZ65	TZ64	TZ63	TZ62	TZ61	TZ60
K5E	K5E	UNUSED		--	--	--	--	--	--	--	--
	K5F			--	--	--	--	--	--	--	--
K60	K60	PLCP.RCR	RW	--	RLIE	--	PECC	FEPD	FECC	ECC	FRSYNC
	K61			--	--	--	--	--	--	RHSC1	RHSC0
K62	K62	UNUSED		--	--	--	--	--	--	--	--
	K63			--	--	--	--	--	--	--	--
K64	K64	PLCP.RSR1	R	--	--	REIC	PEC	FEC	RAI	--	OOF
	K65			--	--	--	--	--	--	--	LOF
K66	K66	PLCP.RSR2	R	--	--	--	--	--	--	--	LSSU
	K67			--	--	--	--	--	--	--	--
K68	K68	PLCP.RSRL1	RL	--	--	REICL	PECL	FECL	RAIL	COFAL	OOFL
	K69			--	--	REIL	PEL	FEL	--	--	LOFL
K6A	K6A	PLCP.RSRL2	RL	RZ3L	RZ2L	RZ1L	RM2L	RM1L	RF1L	LSSL	LSSUL
	K6B			--	--	--	--	--	RZ6L	RZ5L	RZ4L
K6C	K6C	PLCP.RSRIE1	RW	--	--	REICIE	PECIE	FECIE	RAIIE	COFAIE	OOFIE
	K6D			--	--	REIIE	PEIE	FEIE	--	--	LOFIE
K6E	K6E	PLCP.RSRIE2	RW	RZ3IE	RZ2IE	RZ1IE	RM2IE	RM1IE	RF1IE	LSSIE	LSSUIE
	K6F			--	--	--	--	--	RZ6IE	RZ5IE	RZ4IE
K70	K70	PLCP.RFECR	R	FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0
	K71			FE15	FE14	FE13	FE12	FE11	FE10	FE9	FE8
K72	K72	PLCP.RPECR	R	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
	K73			PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8
K74	K74	PLCP.RREICR	R	REI7	REI6	REI5	REI4	REI3	REI2	REI1	REI0
	K75			REI15	REI14	REI13	REI12	REI11	REI10	REI9	REI8

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
K76	K76	PLCP.RFGBR	R	--	--	--	--	--	LSS2	LSS1	LSS0
	K77			RF17	RF16	RF15	RF14	RF13	RF12	RF11	RF10
K78	K78	PLCP.RM12BR	R	RM17	RM16	RM15	RM14	RM13	RM12	RM11	RM10
	K79			RM27	RM26	RM25	RM24	RM23	RM22	RM21	RM20
K7A	K7A	PLCP.RZ12BR	R	RZ17	RZ16	RZ15	RZ14	RZ13	RZ12	RZ11	RZ10
	K7B			RZ27	RZ26	RZ25	RZ24	RZ23	RZ22	RZ21	RZ20
K7C	K7C	PLCP.RZ34BR	R	RZ37	RZ36	RZ35	RZ34	RZ33	RZ32	RZ31	RZ30
	K7D			RZ47	RZ46	RZ45	RZ44	RZ43	RZ42	RZ41	RZ40
K7E	K7E	PLCP.RZ56BR	R	RZ57	RZ56	RZ55	RZ54	RZ53	RZ52	RZ51	RZ50
	K7F			RZ67	RZ66	RZ65	RZ64	RZ63	RZ62	RZ61	RZ60

Table 12-15. FIFO Register Bit Map

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
K80	K80	FF.TCR	RW	--	--	--	--	--	--	--	TFRST
	K81			--	--	--	--	--	--	--	--
K82	K82	FF.TLCR	RW	--	--	TFAF5	TFAF4	TFAF3	TFAF2	TFAF1	TFAF0
	K83			--	--	TFAE5	TFAE4	TFAE3	TFAE2	TFAE1	TFAE0
K84	K84	FF.TPAC	RW	--	--	--	TPA4	TPA3	TPA2	TPA1	TPA0
	K85			--	--	--	--	--	--	--	--
K86	K86	UNUSED		--	--	--	--	--	--	--	--
	K87			--	--	--	--	--	--	--	--
K88	K88	FF.TSRL	RL	--	--	--	TFATL	TFSTL	TFITL	TFUL	TFOL
	K89			--	--	--	--	--	--	--	--
K8A	K8A	FF.TSRIE	RW	--	--	--	TFATIE	TFSTIE	TFITIE	TFUIE	TFOIE
	K8B			--	--	--	--	--	--	--	--
K8C-K8F	K8C	UNUSED		--	--	--	--	--	--	--	--
	K8F			--	--	--	--	--	--	--	--
K90	K90	FF.RCR	RW	--	--	--	--	--	--	--	RFRST
	K91			--	--	--	--	--	--	--	--
K92	K92	FF.RLCR	RW	--	--	RFAF5	RFAF4	RFAF3	RFAF2	RFAF1	RFAF0
	K93			--	--	RFAE5	RFAE4	RFAE3	RFAE2	RFAE1	RFAE0
K94	K94	FF.RFPAC	RW	--	--	--	RPA4	RPA3	RPA2	RPA1	RPA0
	K95			--	--	--	--	--	--	--	--
K96	K96	UNUSED		--	--	--	--	--	--	--	--
	K97			--	--	--	--	--	--	--	--
K98	K98	FF.RSRL	RL	--	--	--	--	--	--	--	RFOL
	K99			--	--	--	--	--	--	--	--
K9A	K9A	FF.RSRIE	RW	--	--	--	--	--	--	--	RFOIE
	K9B			--	--	--	--	--	--	--	--
K9C-K9F	K9C	UNUSED		--	--	--	--	--	--	--	--
	K9F			--	--	--	--	--	--	--	--

12.1.8 Transmit Cell Processor Bit Map

Table 12-16. Transmit Cell Processor Register Bit Map

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
KA0	KA0	CP.TCR	RW	--	--	TFCH	TFCP	THSE	TSD	TBRE	TPTE
	KA1			--	--	--	--	TDSE	TDHE	THPE	TCPAD
KA2	KA2	RESERVED		--	--	--	--	--	--	--	--
	KA3			--	--	--	--	--	--	--	--
KA4	KA4	CP.TECC	RW	TCEN7	TCEN6	TCEN5	TCEN4	TCEN3	TCEN2	TCEN1	TCEN0
	KA5			MEIMS	TCER6	TCER5	TCER4	TCER3	TCER2	TCER1	TCER0
KA6	KA6	CP.THMRC	RW	THEM7	THEM6	THEM5	THEM4	THEM3	THEM2	THEM1	THEM0
	KA7			--	--	--	--	--	--	--	--
KAA	KAA	CP.THPC1	RW	THP7	THP6	THP5	THP4	THP3	THP2	THP1	THP0
	KA9			THP15	THP14	THP13	THP12	THP11	THP10	THP9	THP8
KAA	KAA	CP.THPC2	RW	THP23	THP22	THP21	THP20	THP19	THP18	THP17	THP16
	KAB			THP31	THP30	THP29	THP28	THP27	THP26	THP25	THP24
KAC	KAC	CP.TFPPC	RW	TFPP7	TFPP6	TFPP5	TFPP4	TFPP3	TFPP2	TFPP1	TFPP0
	KAD			--	--	--	--	--	--	--	--
KAE	KAE	CP.TSR	R	--	--	--	--	--	--	--	TECF
	KAF			--	--	--	--	--	--	--	--
KB0	KB0	CP.TSRL	RL	--	--	--	--	--	--	--	TECFL
	KB1			--	--	--	--	--	--	--	--
KB2	KB2	CP.TSRIE	RW	--	--	--	--	--	--	--	TECFIE
	KB3			--	--	--	--	--	--	--	--
KB4	KB4	CP.TCCR1	R	TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
	KB5			TCC15	TCC14	TCC13	TCC12	TCC11	TCC10	TCC9	TCC8
KB6	KB6	CP.TCCR2	R	TCC23	TCC22	TCC21	TCC20	TCC19	TCC18	TCC17	TCC16
	KB7			--	--	--	--	--	--	--	--
KB8-KBE	KB8-KBF	RESERVED		--	--	--	--	--	--	--	--
				--	--	--	--	--	--	--	--
KBC-KBE	KBC-KBF	UNUSED		--	--	--	--	--	--	--	--
				--	--	--	--	--	--	--	--

12.1.9 Transmit Packet Processor Bit Map

Table 12-17. Transmit Packet Processor Register Bit Map

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
KA0	KA0	PP.TCR	RW	--	--	TFAD	TF16	TIFV	TSD	TBRE	TPTE
	KA1			--	--	--	--	RES	RES	RES	RES
KA2	KA2	PP.TIFGC	RW	TIFG7	TIFG6	TIFG5	TIFG4	TIFG3	TIFG2	TIFG1	TIFG0
	KA3			--	--	--	--	--	--	--	--
KA4	KA4	PP.TEPC	RW	TPEN7	TPEN6	TPEN5	TPEN4	TPEN3	TPEN2	TPEN1	TPEN0
	KA5			MEIMS	TPER6	TPER5	TPER4	TPER3	TPER2	TPER1	TPER0
KA6-KAC	KA6-KAD	RESERVED		--	--	--	--	--	--	--	--
				--	--	--	--	--	--	--	--
KAE	KAE	PP.TSR	R	--	--	--	--	--	--	--	TEPF
	KAF			--	--	--	--	--	--	--	--

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
KB0	KB0	PP.TSRL	RL	--	--	--	--	--	--	--	TEPFL
	KB1			--	--	--	--	--	--	--	--
KB2	KB2	PP.TSRIE	RW	--	--	--	--	--	--	--	TEPFIE
	KB3			--	--	--	--	--	--	--	--
KB4	KB4	PP.TPCR1	R	TPC7	TPC6	TPC5	TPC4	TPC3	TPC2	TPC1	TPC0
	KB5			TPC15	TPC14	TPC13	TPC12	TPC11	TPC10	TPC9	TPC8
KB6	KB6	PP.TPCR2	R	TPC23	TPC22	TPC21	TPC20	TPC19	TPC18	TPC17	TPC16
	KB7			--	--	--	--	--	--	--	--
KB8	KB8	PP.TBCR1	R	TBC7	TBC6	TBC5	TBC4	TBC3	TBC2	TBC1	TBC0
	KB9			TBC15	TBC14	TBC13	TBC12	TBC11	TBC10	TBC9	TBC8
KBA	KBA	PP.TBCR2	R	TBC23	TBC22	TBC21	TBC20	TBC19	TBC18	TBC17	TBC16
	KBB			TBC31	TBC30	TBC29	TBC28	TBC27	TBC26	TBC25	TBC24
KBC-KBE	KBC-KBF	RESERVED		--	--	--	--	--	--	--	--
				--	--	--	--	--	--	--	--

Table 12-18. Receive Cell Processor Register Bit Map

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
KC0	KC0	CP.RCR1	RW	RROC1	RROC0	RCPAD	RHECD	RHDE	RDD	RBRE	RPTE
	KC1			RDDE	RDHE	RECED	RHPM1	RHPM0	RICFD	RUCFE	RICFE
KC2	KC2	RESERVED		--	--	--	--	--	--	--	--
	KC3			--	--	--	--	--	--	--	--
KC4	KC4	CP.RHPC1	RW	RHP7	RHP6	RHP5	RHP4	RHP3	RHP2	RHP1	RHP0
	KC5			RHP15	RHP14	RHP13	RHP12	RHP11	RHP10	RHP9	RHP8
KC6	KC6	CP.RHPC2	RW	RHP23	RHP22	RHP21	RHP20	RHP19	RHP18	RHP17	RHP16
	KC7			RHP31	RHP30	RHP29	RHP28	RHP27	RHP26	RHP25	RHP24
KC8	KC8	CP.RHPMC1	RW	RHPD7	RHPD6	RHPD5	RHPD4	RHPD3	RHPD2	RHPD1	RHPD0
	KC9			RHPD15	RHPD14	RHPD13	RHPD12	RHPD11	RHPD10	RHPD9	RHPD8
KCA	KCA	CP.RHPMC2	RW	RHPD23	RHPD22	RHPD21	RHPD20	RHPD19	RHPD18	RHPD17	RHPD16
	KCB			RHPD31	RHPD30	RHPD29	RHPD28	RHPD27	RHPD26	RHPD25	RHPD24
KCC	KCC	CP.RLTC	RW	RLT7	RLT6	RLT5	RLT4	RLT3	RLT2	RLT1	RLT0
	KCD			RLT15	RLT14	RLT13	RLT12	RLT11	RLT10	RLT9	RLT8
KCE	KCE	CP.RSR	R	--	--	--	--	--	RECC	RHPC	RCHC
	KCF			--	--	--	--	OOS	--	OCD	LCD
KD0	KD0	CP.RSRL	RL	RECL	RCHL	RIDL	RUDL	RIVDL	RECCL	RHPCL	RCHCL
	KD1			--	--	--	--	OOSL	COCDL	OCDCL	LCDCL
KD2	KD2	CP.RSRIE	RW	RECIE	RCHIE	RIDIE	RUDIE	RIVDIE	RECCIE	RHPCIE	RCHCIE
	KD3			--	--	--	--	OOSIE	COCDIE	OCDCIE	LCDCIE
KD4	KD4	CP.RCCR1	R	RCC7	RCC6	RCC5	RCC4	RCC3	RCC2	RCC1	RCC0
	KD5			RCC15	RCC14	RCC13	RCC12	RCC11	RCC10	RCC9	RCC8
KD6	KD6	CP.RCCR2	R	RCC23	RCC22	RCC21	RCC20	RCC19	RCC18	RCC17	RCC16
	KD7			--	--	--	--	--	--	--	--
KD8	KD8	CP.RECCR1	R	RECC7	RECC6	RECC5	RECC4	RECC3	RECC2	RECC1	RECC0
	KD9			RECC15	RECC14	RECC13	RECC12	RECC11	RECC10	RECC9	RECC8
KDA	KDA	CP.RECCR2	R	RECC23	RECC22	RECC21	RECC20	RECC19	RECC18	RECC17	RECC16
	KDB			--	--	--	--	--	--	--	--
KDC	KDC	CP.RHPCR1	R	RHPC7	RHPC6	RHPC5	RHPC4	RHPC3	RHPC2	RHPC1	RHPC0
	KDD			RHPC15	RHPC14	RHPC13	RHPC12	RHPC11	RHPC10	RHPC9	RHPC8

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
KDE	KDE	CP.RHPCR2	R	--	--	--	--	--	--	--	--
	KDF			RHPC23	RHPC22	RHPC21	RHPC20	RHPC19	RHPC18	RHPC17	RHPC16
KE0	KE0	CP.RCCCR1	R	RCHC7	RCHC6	RCHC5	RCHC4	RCHC3	RCHC2	RCHC1	RCHC0
	KE1			RCHC15	RCHC14	RCHC13	RCHC12	RCHC11	RCHC10	RCHC9	RCHC8
KE2	KE2	CP.RCCCR2	R	RCHC23	RCHC22	RCHC21	RCHC20	RCHC19	RCHC18	RCHC17	RCHC16
	KE3			--	--	--	--	--	--	--	--
KE4	KE4	CP.RFCCR1	R	RFCC7	RFCC6	RFCC5	RFCC4	RFCC3	RFCC2	RFCC1	RFCC0
	KE5			RFCC15	RFCC14	RFCC13	RFCC12	RFCC11	RFCC10	RFCC9	RFCC8
KE6	KE6	CP.RFCCR2	R	RFCC23	RFCC22	RFCC21	RFCC20	RFCC19	RFCC18	RFCC17	RFCC16
	KE7			--	--	--	--	--	--	--	--
KE8-KEE	KE8-KEF	RESERVED		--	--	--	--	--	--	--	--
				--	--	--	--	--	--	--	--
KF0-KFE	KF0-KFF	UNUSED		--	--	--	--	--	--	--	--
				--	--	--	--	--	--	--	--

Table 12-19. Receive Packet Processor Register Bit Map

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
KC0	KC0	PP.RCR	RW	Reserved	Reserved	RFPD	RF16	RFED	RDD	RBRE	RPTE
	KC1			RMNS7	RMNS6	RMNS5	RMNS4	RMNS3	RMNS2	RMNS1	RMNS0
KC2	KC2	PP.RMPSC	RW	RMX7	RMX6	RMX5	RMX4	RMX3	RMX2	RMX1	RMX0
	KC3			RMX15	RMX14	RMX13	RMX12	RMX11	RMX10	RMX9	RMX8
KC4-KCC	KC4-KCD	RESERVED		--	--	--	--	--	--	--	--
				--	--	--	--	--	--	--	--
KCE	KCE	PP.RSR	R	--	--	--	--	--	REPC	RAPC	RSPC
	KCF			--	--	--	--	Reserved	Reserved	Reserved	Reserved
KD0	KD0	PP.RSRL	RL	REPL	RAPL	RIPDL	RSPDL	RLPDL	REPCL	RAPCL	RSPCL
	KD1			--	--	--	--	Reserved	Reserved	Reserved	Reserved
KD2	KD2	PP.RSRIE	RW	REPIE	RAPIE	RIPDIE	RSPDIE	RLPDIE	REPCIE	RAPCIE	RSPCIE
	KD3			--	--	--	--	Reserved	Reserved	Reserved	Reserved
KD4	KD4	PP.RPCR1	R	RPC7	RPC6	RPC5	RPC4	RPC3	RPC2	RPC1	RPC0
	KD5			RPC15	RPC14	RPC13	RPC12	RPC11	RPC10	RPC9	RPC8
KD6	KD6	PP.RPCR2	R	RPC23	RPC22	RPC21	RPC20	RPC19	RPC18	RPC17	RPC16
	KD7			--	--	--	--	--	--	--	--
KD8	KD8	PP.RFPCR1	R	RFPC7	RFPC6	RFPC5	RFPC4	RFPC3	RFPC2	RFPC1	RFPC0
	KD9			RFPC15	RFPC14	RFPC13	RFPC12	RFPC11	RFPC10	RFPC9	RFPC8
KDA	KDA	PP.RFPCR2	R	RFPC23	RFPC22	RFPC21	RFPC20	RFPC19	RFPC18	RFPC17	RFPC16
	KDB			--	--	--	--	--	--	--	--
KDC	KDC	PP.RAPCR1	R	RAPC7	RAPC6	RAPC5	RAPC4	RAPC3	RAPC2	RAPC1	RAPC0
	KDD			RAPC15	RAPC14	RAPC13	RAPC12	RAPC11	RAPC10	RAPC9	RAPC8
KDE	KDE	PP.RAPCR2	R	RAPC23	RAPC22	RAPC21	RAPC20	RAPC19	RAPC18	RAPC17	RAPC16
	KDF			--	--	--	--	--	--	--	--
KE0	KE0	PP.RSPCR1	R	RSPC7	RSPC6	RSPC5	RSPC4	RSPC3	RSPC2	RSPC1	RSPC0
	KE1			RSPC15	RSPC14	RSPC13	RSPC12	RSPC11	RSPC10	RSPC9	RSPC8
KE2	KE2	PP.RSPCR2	R	RSPC23	RSPC22	RSPC21	RSPC20	RSPC19	RSPC18	RSPC17	RSPC16
	KE3			--	--	--	--	--	--	--	--
KE4-KE6	KE4	RESERVED		--	--	--	--	--	--	--	--
	KE7			--	--	--	--	--	--	--	--

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
KE8	KE8	PP.RBCR1	R	RBC7	RBC6	RBC5	RBC4	RBC3	RBC2	RBC1	RBC0
	KE9			RBC15	RBC14	RBC13	RBC12	RBC11	RBC10	RBC9	RBC8
KEA	KEA	PP.RBCR2	R	RBC23	RBC22	RBC21	RBC20	RBC19	RBC18	RBC17	RBC16
	KEB			RBC31	RBC30	RBC29	RBC28	RBC27	RBC26	RBC25	RBC24
KEC	KEC	PP.REBCR1	R	REBC7	REBC6	REBC5	REBC4	REBC3	REBC2	REBC1	REBC0
	KED			REBC15	REBC14	REBC13	REBC12	REBC11	REBC10	REBC9	REBC8
KEE	KEE	PP.REBCR2	R	REBC23	REBC22	REBC21	REBC20	REBC19	REBC18	REBC17	REBC16
	KEF			REBC31	REBC30	REBC29	REBC28	REBC27	REBC26	REBC25	REBC24
KF0-KFE	KF0-KFF	UNUSED		--	--	--	--	--	--	--	--
				--	--	--	--	--	--	--	--

Bits that are underlined are read-only; all other bits are read-write.

12.2 Global Registers

Table 12-20. Global Register Map

Address	Register	Register Description
000h	GL.IDR	Global ID Register
002h	GL.CR1	Global Control Register 1
004h	GL.CR2	Global Control Register 2
006h	--	Unused
008h	--	Unused
00Ah	GL.GIOCR	Global General-Purpose I/O Control Register
00Ch	--	Unused
00Eh	--	Unused
010h	GL.ISR	Global Interrupt Status Register
012h	GL.ISRIE	Global Interrupt Enable Register
014h	GL.SR	Global Status Register
016h	GL.SRL	Global Status Register Latched
018h	GL.SRIE	Global Status Register Interrupt Enable
01Ah	--	Unused
01Ch	GL.GIORR	Global General-Purpose I/O read register
01Eh	--	Unused

12.2.1 Register Bit Descriptions

Register Name: **GL.IDR**
Register Description: **Global ID Register**
Register Address: **000h**

Bit #	15	14	13	12	11	10	9	8
Name	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8

Bit #	7	6	5	4	3	2	1	0
Name	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Bits 15 to 12: Device REV ID Bits 15 to 12 (ID15 to ID12). These bits of the device ID register has same information as the four bits of JTAG REV ID portion of the JTAG ID register. JTAG ID[31:28].

Bits 11 to 0: Device CODE ID Bits 11 to 0 (ID11 to ID0). These bits of the device code ID register has same information as the lower 12 bits of JTAG CODE ID portion of the JTAG ID register. JTAG ID[23:12].

Register Name: **GL.CR1**
Register Description: **Global Control Register 1**
Register Address: **002h**

Bit #	15	14	13	12	11	10	9	8
Name	GWRM	INTM	DIREN	--	SIW1	SIW0	SIM1	SIM0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	TMEI	MEIMS	GPM1	GPM0	PMU	LSBCRE	RSTDP	RST
Default	0	0	0	0	0	0	1	0

Bit 15: Global Write Mode (GWRM) This bit enables the global write mode. When this bit is set, a write to the register of any port will write to the same register in all the ports. Reading the registers of any port is not supported and will read back undefined data.

0 = Normal write mode
1 = Global write mode

Bit 14: $\overline{\text{INT}}$ pin mode (INTM) This bit determines the inactive mode of the $\overline{\text{INT}}$ pin. The $\overline{\text{INT}}$ pin always drives low when active.

0 = Pin is high impedance when not active
1 = Pin drives high when not active

Bit 13: Direct Status Enable (DIREN) This bit selects between the direct status and polled status modes for UTOPIA and POS-PHY.

0 = Polled status mode
1 = Direct status mode

Bits 11 and 10: System Interface Bus Width (SIW[1:0]) These bits configure the system bus width.

00 = 8-bit
01 = 16-bit
1X = 32-bit

Bits 9 and 8: System Interface Mode (SIM[1:0]) These bits configure the system bus mode.

00 = UTOPIA L2
01 = UTOPIA L3
10 = POS-PHY L2
11 = POS-PHY L3 or SPI-3

Bit 7: Transmit Manual Error Insert (TMEI) This bit is used insert an error in all ports and error insertion logic configured for global error insertion. An error(s) is inserted at the next opportunity when this bit transitions from low to high. The GL.CR1.MEIMS bit must be clear for this bit to operate.

Bit 6: Transmit Manual Error Insert Select (MEIMS) This bit is used to select the source of the global manual error insertion signal

0 = Global error insertion using TMEI bit
1 = Global error insertion using the GPIO6 pin

Bits 5 and 4: Global Performance Monitor Update Mode (GPM[1:0]) These bits select the global performance monitor register update mode.

00 = Global PM update using the PMU bit
01 = Global PM update using the GPIO8 pin
1x = One second PM update using the internal one second counter

Bit 3: Global Performance Monitor Update Register (PMU) This bit is used to update all of the performance monitor registers configured to use this bit. When this bit is toggled from low to high the performance registers configured to use this signal will be updated with the latest count value from the counters, and the counters will be reset. The bit should remain high until the performance register update status bit (GL.SR.PMS) goes high, then it should be brought back low which clears the PMS status bit.

Bit 2: Latched Status Bit Clear on Read Enable (LSBCRE). This signal determines when latched status register bits are cleared.

0 = Latched status register bits are cleared on a write
1 = Latched status register bits are cleared on a read

Bit 1: Reset Data Path (RSTDP). When this bit is set, it will force all of the internal data path registers in all ports to their default state. This bit must be set high for a minimum of 100ns. See the Reset and Power-Down section 10.3. Note: The default state is a 1 (after a general reset, this bit will be set to one).

0 = Normal operation
1 = Force all data path registers to their default values

Bit 0: Reset (RST). When this bit is set, all of the internal data path and status and control registers (except this RST bit), on all of the ports, will be reset to their default state. This bit must be set high for a minimum of 100ns. See the Reset and Power-Down in Section 10.3.

0 = Normal operation
1 = Force all internal registers to their default values

Register Name: **GL.CR2**
Register Description: **Global Control Register 2**
Register Address: **004h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	G8KRS2	G8KRS1	G8KRS0	G8K0S	G8KIS
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	CLAD3	CLAD2	CLAD1	CLAD0
Default	0	0	0	0	0	0	0	0

Bits 12 to 10: Global 8KHz Reference Source [2:0] (G8KRS[2:0]). These bits determine the source for the internally generated 8 kHz reference as well as the internal one second reference, which is derived from the Global 8 kHz reference. The source is selected from one of the CLAD clocks or from one of the port 8KREF clock sources.

These bits are ignored when the G8KIS bit = 1.

Table 10-10. Global 8kHz Reference Source Table

GL.CR2. G8KIS	GL.CR2. G8KRS[2:0]	Source
0	**000**	None, the 8KHZ divider is disabled.
0	001	Derived from CLAD DS3 clock output or CLKA pin if CLAD is disabled. (Note: CLAD is disabled after reset)
0	010	Derived from CLAD E3 clock output or CLKB pin if CLAD is disabled
0	011	Derived from CLAD STS-1 clock output or CLKC pin if CLAD is disabled
0	100	Port 1 8KREF source selected by P8KRS[1:0]
0	101	Port 2 8KREF source selected by P8KRS[1:0]
0	110	Port 3 8KREF source selected by P8KRS[1:0]
0	111	Port 4 8KREF source selected by P8KRS[1:0]
1	XXX	GPIO4 pin

Bit 9: Global 8KHz Reference Output Select (G8KOS). This bit determines whether GPIO2 pin is used for the global 8KREFO output signal, or is used as specified by GL.GIOCR.GPIO2S[1:0].

0 = GPIO2 pin mode selected by GL.GIOCR.GPIO2S[1:0]
1 = GPIO2 is the global 8KREFO output signal selected by GL.CR2.8KRS[2:0]

Bit 8: Global 8KHz Reference Input Select (G8KIS). This bit determines whether GPIO4 pin is used for the global 8KREFI input signal, or is used as specified by GL.GIOCR.GPIO4S[1:0]. G8KREFI signal will be low if not selected. Global 8KREF pin signal will be low if not selected.

0 = GPIO4 pin mode selected by GL.GIOCR.GPIO4S[1:0]
1 = GPIO4 is the global 8KREFI input signal for one second timer and ports to use

Bits 3 to 0: CLAD IO Mode [3:0] (CLAD[3:0]). These bits control the CLAD clock IO pins CLKA, CLKB and CLKC.

GL.CR2. **CLAD[3:0]**	**CLKA PIN**	**CLKB PIN**	**CLKC PIN**
00 XX	DS3 clock input	E3 clock input	STS-1 clock input
01 00	DS3 clock input	Low output	Low output
01 01	DS3 clock input	E3 clock output	Low output
01 10	DS3 clock input	Low output	STS-1 clock output
01 11	DS3 clock input	STS-1 clock output	E3 clock output
10 00	E3 clock input	Low output	Low output
10 01	E3 clock input	DS3 clock output	Low output
10 10	E3 clock input	Low output	STS-1 clock output
10 11	E3 clock input	STS-1 clock output	DS3 clock output
11 00	STS-1 clock input	Low output	Low output
11 01	STS-1 clock input	E3 output	Low output
11 10	STS-1 clock input	Low output	DS3 clock output
11 11	STS-1 clock input	DS3 clock output	E3 clock output

Register Name: **GL.GIOCR**
Register Description: **Global General-Purpose I/O Control Register**
Register Address: **00Ah**

Bit #	15	14	13	12	11	10	9	8
Name	GPIO8S1	GPIO8S0	GPIO7S1	GPIO7S0	GPIO6S1	GPIO6S0	GPIO5S1	GPIO5S0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	GPIO4S1	GPIO4S0	GPIO3S1	GPIO3S0	GPIO2S1	GPIO2S0	GPIO1S1	GPIO1S0
Default	0	0	0	0	0	0	0	0

Bits 15 to 14: General-Purpose I/O 8 Select [1:0] (GPIO8S[1:0]). These bits determine the function of the GPIO8 pin. These selections are only valid if **GL.CR1**.GPM[1:0] is not set to 01.

00 = Input
01 = Port 4 B status output selected by PORT.CR4:GPIOB[3:0] in port control registers
10 = Output logic 0
11 = Output logic 1

Bits 13 to 12: General-Purpose I/O 7 Select [1:0] (GPIO7S[1:0]). These bits determine the function of the GPIO7 pin.

00 = Input
01 = Port 4 A status output selected by PORT.CR4:GPIOA[3:0] in port control registers
10 = Output logic 0
11 = Output logic 1

Bits 11 to 10: General-Purpose I/O 6 Select [1:0] (GPIO6S[1:0]). These bits determine the function of the GPIO6 pin. These selections are only valid if **GL.CR1**.MEIMS=0.

00 = Input
01 = Port 3 B status output selected by PORT.CR4:GPIOB[3:0] in port control registers
10 = Output logic 0
11 = Output logic 1

Bits 9 to 8: General-Purpose I/O 5 Select [1:0] (GPIO5S[1:0]). These bits determine the function of the GPIO5 pin.

00 = Input
01 = Port 3 A status output selected by PORT.CR4:GPIOA[3:0] in port control registers
10 = Output logic 0
11 = Output logic 1

Bits 7 to 6: General-Purpose I/O 4 Select [1:0] (GPIO4S[1:0]). These bits determine the function of the GPIO4 pin. These selections are only valid if GL.CR2 .G8KRIS=0.

00 = Input
01 = Port 2 B status output selected by PORT.CR4:GPIOB[3:0] in port control registers
10 = Output logic 0
11 = Output logic 1

Bits 5 to 4: General-Purpose I/O 3 Select [1:0] (GPIO3S[1:0]). These bits determine the function of the GPIO3 pin.

00 = Input
01 = Port 2 A status output selected by PORT.CR4:GPIOA[3:0] in port control registers
10 = Output logic 0
11 = Output logic 1

Bits 3 to 2: General-Purpose I/O 2 Select [1:0] (GPIO2S[1:0]). These bits determine the function of the GPIO2 pin. These selections are only valid if GL.CR2.GKROS=0.

00 = Input
01 = Port 1 B status output selected by PORT.CR4:GPIOB[3:0] in port control registers
10 = Output logic 0
11 = Output logic 1

Bits 1 to 0: General-Purpose I/O 1 Select [1:0] (GPIO1S[1:0]). These bits determine the function of the GPIO1 pin.

00 = Input
01 = Port 1 A status output selected by PORT.CR4:GPIOA[3:0] in port control registers
10 = Output logic 0
11 = Output logic 1

Register Name: **GL.ISR**
Register Description: **Global Interrupt Status Register**
Register Address: **010h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	PISR4	PISR3	PISR2	PISR1	--	--	TSSR	GSR

Bits 15 to 8: Not Used (--)

Bits 7 to 4: Port Interrupt Status Register [4:1] (PISR[4:1]) The corresponding bit is set when any of the bits in the port interrupt status registers (PORT.ISR) are set. The $\overline{INT}$ interrupt pin will be driven low when any bit is set and the corresponding GL.ISRIE.PISRIE[4:1] interrupt enable bit is enabled.

Bit 1: Transmit System Interface Status Register Interrupt Status (TSSR) This bit is set when any of the latched status register bits in the transmit system interface are set and enabled for interrupt. The $\overline{INT}$ pin will be driven low when this bit is set and the *GL.ISRIE*.TSSRIE interrupt enable bit is enabled.

Bit 0: Global Status Register Interrupt Status (GSR) This bit is set when any of the latched status register bits in the global latched status register (GL.SRL) are set and enabled for interrupt. The $\overline{INT}$ interrupt pin will be driven low when this bit is set and the *GL.ISRIE*.GSRIE interrupt enable bit is enabled.

Register Name: **GL.ISRIE**
Register Description: **Global Interrupt Status Register Interrupt Enable**
Register Address: **012h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	PISRIE4	PISRIE3	PISRIE2	PISRIE1	--	--	TSSRIE	GSRIE
Default	0	0	0	0	0	0	0	0

Bits 15 to 8: Not Used (--)

Bits 7 to 4: Port Interrupt Status Register Interrupt Enable [4:1] (PISRIE[4:1]) When any interrupt enable bit in this group is enabled corresponding to a status bit set in the GL.ISR.PISR[4:1] status bit group, the $\overline{INT}$ pin will be driven low.

0 = interrupt disabled
1 = interrupt enabled

Bit 1: Transmit System Interface Status Register Interrupt Status Interrupt Enable (TSSRIE) When this bit is enabled, and the *GL.ISR*.TSSR status bit is set, the $\overline{INT}$ pin will be driven low.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Global Status Register Interrupt Status Interrupt Enable (GSRIE) When this interrupt enable bit is enabled, and the *GL.ISR*.GSR status bit is set, the $\overline{INT}$ pin will be driven low.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **GL.SR**
Register Description: **Global Status Register**
Register Address: **014h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	--	CLOL	GPMS

Bit 1: CLAD Loss of Lock (CLOL) – This bit is set when any of the PLLs in the CLAD are not locked to the reference frequency.

Bit 0: Global Performance Monitoring Update Status (GPMS) This bit is set when all of the port performance register update status bits (*PORT.SR*.PMS), that are enabled for global update control (*PORT.CR1*.PMUM=1), are set. It is an "AND" of all the globally enabled port PMU status bits. In global software update mode, the global update request bit (*GL.CR1*.PMU) should be held high until this status bit goes high.

0 = The associated update request signal is low or not all register updates are completed
1 = The requested performance register updates are all completed

Register Name: **GL.SRL**
Register Description: **Global Status Register Latched**
Register Address: **016h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	8KREFL	CLADL	ONESL	CLOLL	GPMSL

Bit 4: 8K Reference Activity Status Latched (8KREFL) This bit will be set when the 8 kHz reference signal on the GPIO4 pin is active. The GL.CR2.G8KIS bit must be set for the activity to be monitored.

Bit 3: CLAD Reference Clock Activity Status Latched (CLADL) This bit will be set when the CLAD PLL reference clock signal on the CLKA pin is active.

Bit 2: One-Second Status Latched (ONESL) This bit will be set once a second. The GL.ISR.GSR status bit will be set when this bit is set and the GL.SRIE.ONESIE bit is enabled. The $\overline{INT}$ pin will be driven low if this bit is set and the GL.SRIE.ONESIE bit and the GL.ISRIE.GSRIE bit are enabled.

Bit 1: CLAD Loss Of Lock Latched (CLOLL) This bit will be set when the *GL.SR*.CLOL status bit changes from low to high. The *GL.ISR*.GSR bit will be set when this bit is set and the *GL.SRIE*.CLOLIE bit is set and the $\overline{INT}$ pin will be driven low if the *GL.ISRIE*.GSRIE bit is also enabled.

Bit 0: Global Performance Monitoring Update Status Latched (GPMSL) This bit will be set when the GL.SR.GPMS status bit changes from low to high. This bit will set the GL.ISR.GSR status bit if the GL.SRIE.GPMSIE is enabled. This bit will drive the interrupt pin low if the GL.SRIE.GPMSIE bit and the GL.ISRIE.GSRIE bit are enabled.

Register Name: **GL.SRIE**
Register Description: **Global Status Register Interrupt Enable**
Register Address: **018h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	ONESIE	CLOLIE	GPMSIE
Default	0	0	0	0	0	0	0	0

Bit 2: One Second Interrupt Enable (ONESIE) This bit will drive the interrupt pin low when this bit is enabled, the GL.SRL.ONESL bit is set, and the GL.ISRIE.GSRIE bit is enabled.

0 = interrupt disabled
1 = interrupt enabled

Bit 1: CLAD Loss Of Lock Interrupt Enable (CLOLIE) The interrupt pin will be driven when this bit is enabled, the *GL.SRL*.CLOLL is set, and *GL.ISRIE*.GSRIE bit is enabled.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Global Performance Monitoring Update Status Interrupt Enable (GPMSIE) The interrupt pin will be driven when this bit is enabled and the GL.SRL.GPMSL bit is set and the GL.ISRIE.GSRIE bit is enabled.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **GL.GIORR**
Register Description: **Global General-Purpose I/O Read Register**
Register Address: **01Ch**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1

Bits 7 to 0: General-Purpose I/O Status [8:1]] (GPIO[8:1]) These bits reflect the input or output signal on the eight general-purpose I/O pins.

12.3 UTOPIA/POS-PHY System Interface

12.3.1 Transmit System Interface

The transmit system interface block has three registers.

12.3.1.1 Register Map

Table 12-21. Transmit System Interface Register Map

Address	Register	Register Description
030h	SI.TCR	System Interface Transmit Control Register
032h	SI.TSRL	System Interface Transmit Status Register Latched
034h	SI.TSRIE	System Interface Transmit Status Register Interrupt Enable
036h	--	Unused

12.3.1.2 Register Bit Descriptions

Register Name: **SI.TCR**
Register Description: **System Interface Transmit Control Register**
Register Address: **030h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	TXAD5	TXAD4	TXAD3	TXAD2	TXAD1	TXAD0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	TPARP	TFLVI	TSBRE	THECT
Default	0	0	0	0	0	0	0	0

Bits 13 to 8: Transmit Cell/Packet Available Deassertion Time (TXAD[5:0]) – These six bits indicate the amount of data that can be transferred after the cell/packet available signal is deasserted. If more than the indicated amount of data is transferred, a Transmit FIFO overflow may occur.

In UTOPIA mode, only TXAD[2:0] are valid, and they indicate the number of transfers into the FIFO before the Transmit FIFO is full. For UTOPIA Level 2, a value of 00h enables the default mode, which is 5 (TDXA will transition low on the edge that samples payload byte 43 in 8-bit mode, payload bytes 37 and 38 in 16-bit mode, and payload bytes 25, 26, 27, and 28 in 32-bit mode). For UTOPIA Level 3, a value of 00h or 01h enables the default mode. The default for UTOPIA Level 3 is for TDXA to transition low on the clock edge following the edge that samples the start of a cell.

In POS-PHY mode, TXAD[5:0] indicate the number four byte data groups that can be written into the Transmit FIFO before it is full (maximum value 56 or 38h). In POS-PHY Level 2, a value of 00h enables the default mode, which is 1 (For an x-byte transfer, TDXA and TSPA will transition low on the edge that samples byte x-4 in 8-bit mode, bytes x-5 and x-4 in 16-bit mode, and bytes x-7, x-6, x-5, and x-4 in 32-bit mode). In POS-PHY Level 3 (or SPI-3) 8-bit, a value of 00h enables the default mode, which is 1 (For an x-byte transfer, TDXA and TSPA will transition low on the edge that samples byte x-4). For POS-PHY Level 3 (or SPI-3) 16-bit and 32-bit mode, a value of 00h or 01h enables the default mode, which is 2 (For an x-byte transfer, TDXA and TSPA will transition low on the edge that samples bytes x-9 and x-8 in 16-bit mode and bytes x-11, x-10, x-9, and x-8 in 32-bit mode). Note: A packet that is 4x+1, 4x+2, 4x+3, or 4x+4 (where x is an integer) bytes long consumes x+1 four byte data groups of space in the FIFO. This includes 2-byte and 3-byte packets, which consume a four-byte data group of space in the FIFO.

Bit 3: Transmit System Parity Polarity (TPARP) – When 0, the TPAR signal will maintain odd parity (for all 0"s, TPAR is high). When 1, the TPAR signal will maintain even parity (for all 0"s, TPAR is low).

Bit 2: Transmit System Fill Level Inversion (TFLVI) – When 0, the polarity of the TPXA, TDXA, and TSPA signals will be normal (high for data available). When 1, the polarity of the TPXA, TDXA, and TSPA signals will be inverted (low for data available).

Bit 1: Transmit System Interface Byte Reordering Enable (TSBRE) – When 0, byte reordering is disabled, and the first byte transmitted is transferred across the system interface as the most significant byte (TDATA[31:24] in 32-bit mode or TDATA[15:8] in 16-bit mode). When 1, byte reordering is enabled, and the first byte transmitted is transferred across the system interface as the least significant byte (TDATA[7:0]).

Bit 0: Transmit System HEC Transfer (THECT) – When 0, The HEC byte is not transferred across the transmit system interface. When 1, the HEC byte is transferred across the transmit system interface with the cell data.

Register Name: **SI.TSRL**
Register Description: **System Interface Transmit Status Register Latched**
Register Address: **032h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	--	TSCLKAL	TPREL

Bit 1: Transmit System Interface Clock Active (TSCLKAL) – This bit is set when TSCLK is active.

Bit 0: Transmit System Interface Parity Error Latched (TPREL) – This bit is set when a parity error is detected during a data transfer on the Transmit System Interface bus.

Register Name: **SI.TSRIE**
Register Description: **System Interface Transmit Status Register Interrupt Enable**
Register Address: **034h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	--	--	TPREIE
Default	0	0	0	0	0	0	0	0

Bit 0: Transmit System Interface Parity Error Interrupt Enable (TPREIE) – This bit enables an interrupt if the TPREL bit in the TSISRL register is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

12.3.2 Receive System Interface Register Map

The receive system interface block has three registers.

Table 12-22. Receive System Interface Register Map

Address	Register	Register Description
038h	SI.RCR1	Receive System Interface Control Register #1
03Ah	SI.RCR2	Receive System Interface Control Register #2
03Ch	SI.RSRL	Receive System Interface Status Register Latched
03Eh	--	UNUSED

12.3.2.1 Register Bit Descriptions

Register Name: **SI.RCR1**
Register Description: **System Interface Receive Control Register**
Register Address: **038h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	RMDT2	RMDT1	RMDT0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	RXAD2	RXAD1	RXAD0	RPARP	RFLVI	RSBRE	RHECT
Default	0	0	0	0	0	0	0	0

Bits 10 to 8: Receive System RVAL Minimum Deassertion Time (RMDT[2:0]) – These three bits indicate the minimum number of clock cycles that RVAL must remain deasserted between packets transferred from the same port, a transfer of data equal to the maximum burst depth length (if enabled), or before RSX can be asserted. A value of zero, means that RVAL will not deassert between packets transferred from the same port or between transfers of the maximum burst length when no other port has data available. These bits are ignored in UTOPIA and POS-PHY Level 2 modes. Note: The RVAL minimum deassertion time is for optionally extending the time between packet transfers and port changes to allow a POS-PHY Level 3 Link Layer device enough time to deassert $\overline{REN}$ and pause the next data transfer.

Bits 6 to 4: Receive Cell Available Deassertion Time (RXAD[2:0]) – These three bits indicate the number of transfers that will occur after the selected Receive FIFO indicates it is "empty". A value of 000, enables the default mode. The default for UTOPIA Level 2 is 0 (RDXA will transition low on the clock edge following the clock edge that outputs payload byte 48 in 8-bit mode, payload bytes 47 and 48 in 16-bit mode, and payload bytes 45, 46, 47, and 48 in 32-bit mode). The default for UTOPIA Level 3 is for RDXA to transition low on the clock edge that outputs the start of cell. These bits are ignored in POS-PHY mode.

Bit 3: Receive System Parity Polarity (RPARP) – When 0, the RPRTY signal will maintain odd parity (for all 0"s, RPRTY is high). When 1, the RPRTY signal will maintain even parity (for all 0"s, RPRTY is low).

Bit 2: Receive System Fill Level Inversion (RFLVI) – When 0, the polarity of the RPXA and RDXA signals will be normal (high for data available). When 1, the polarity of the RPXA and RDXA signals will be inverted (low for data available).

Bit 1: Receive System Interface Byte Reordering Enable (RSBRE) – When 0, byte reordering is disabled, and the first byte received is transferred across the system interface as the most significant byte (RDATA[31:24] in 32-bit mode or RDATA[15:8] in 16-bit mode). When 1, byte reordering is enabled, and the first byte received is transferred across the system interface as the least significant byte (RDATA[7:0]).

Bit 0: Receive System HEC Transfer Enable (RHECT) – When 0, The HEC byte is not transferred across the receive system interface. When 1, the HEC byte is transferred across the receive system interface with the cell data.

Register Name: **SI.RCR2**
Register Description: **System Interface Receive Control Register #2**
Register Address: **03Ah**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	RMBL5	RMBL4	RMBL3	RMBL2	RMBL1	RMBL0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RLBL7	RLBL6	RLBL5	RLBL4	RLBL3	RLBL2	RLBL1	RLBL0
Default	0	0	0	0	0	0	0	0

Bits 13 to 8: Receive Maximum Burst Length (RMBL[5:0]) – In POS-PHY Level 3, these six bits limit the maximum number of four byte data groups that can be transferred from a port before switching to another port. The maximum number of transfers is RMBL[5:0]+1 in 32-bit mode, 2*(RMBL[5:0]+1} in 16-bit mode, and 4*(RMBL[5:0]+1} in 8-bit mode. Note: if no other port is ready to start a transfer, transfer from the current port will continue if the port contains more data than the almost empty level or contains an end of packet. These bits are ignored in POS-PHY Level 2 or UTOPIA mode. A value of 00h disables the maximum burst length. In 32-bit mode, a value of 01h is treated as 02h.

Bits 7 to 0: Receive System Loopback Bandwidth Limit (RLBL[7:0]) – These eight bits limit the maximum bandwidth of a single port during system loopback. For RLBL[7:0] equals *x,* the bandwidth will be limited to 1/*x* of the maximum system interface bandwidth. In 8-bit and 16-bit mode, a value of 00h is treated as 01h. In 32-bit mode, a value of 01h or 00h is treated as 02h.

Register Name: **SI.RSRL**
Register Description: **System Interface Receive Status Register Latched**
Register Address: **03Ch**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	--	--	RSCLKAL

Bit 0: Receive System Interface Clock Active Latched (RSCLKAL) – This bit is set when RSCLK is active.

12.4 Per Port Common

12.4.1 Register Bit Descriptions

Table 12-23. Per Port Common Register Map

Address	Register	Register Description
(0,2,4,6)40h	PORT.CR1	Port Control Register 1
(0,2,4,6)42h	PORT.CR2	Port Control Register 2
(0,2,4,6)44h	PORT.CR3	Port Control Register 3
(0,2,4,6)46h	PORT.CR4	Port Control Register 4
(0,2,4,6)48h	--	Unused
(0,2,4,6)4Ah	PORT.INV1	Port IO Invert Control Register 1
(0,2,4,6)4Ch	PORTINV2	Port IO Invert Control Register 2
(0,2,4,6)4Eh	--	Unused
(0,2,4,6)50h	PORT.ISR	Port Interrupt Status Register
(0,2,4,6)52h	PORT.SR	Port Status Register
(0,2,4,6)54h	PORT.SRL	Port Status Register Latched
(0,2,4,6)56h	PORT.SRIE	Port Status Register Interrupt Enable
(0,2,4,6)58h	--	Unused
(0,2,4,6)5Ah	--	Unused
(0,2,4,6)5Ch	--	Unused
(0,2,4,6)5Eh	--	Unused

Register Name: **PORT.CR1**
Register Description: **Port Control Register 1**
Register Address: **(0,2,4,6)40h**

Bit #	15	14	13	12	11	10	9	8
Name	NAD	PAIS2	PAIS1	PAIS0	LAIS1	LAIS0	BENA	HDSEL
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	TMEI	MEIM	--	PMUM	PMU	PD	RSTDP	RST
Default	0	0	--	0	0	1	1	0

Bit 15: Nibble Align Disable (NAD). This bit is used to disable the nibble alignment of the transmit ATM cells in direct mapped DS3 or E3 G.832 framing modes. It must be set when in DS3 M23 mode and the C-bits are used for ATM payload.

0 = Nibble alignment enabled
1 = Nibble alignment disabled

Bits 14 to 12: Payload AIS Select [2:0] (PAIS[2:0]). This bit controls when an unframed all ones signal is forced on the receive data path after the receive framer and payload loopback mux. Default: Payload AIS always sent.

PAIS[2:0] PORT.CR1	When AIS is sent	AIS Code
000	Always	UA1
001	When LLB (no DLB) active	UA1
010	When PLB active	UA1
011	When LLB(no DLB) or PLB active	UA1
100	When LOS (no DLB) active	UA1
101	When OOF active	UA1
110	When OOF, LOS. LLB (no DLB), or PLB active	UA1
111	Never	none

Bits 11 to 10: Line AIS Select [1:0] (LAIS[1:0). These bits control when a DS3 framed AIS or an unframed all ones signal is to be transmitted on TPOSn/TNEGn and/or TXPn/TXNn. The signal on TPOSn/TNEGn can be AMI or unipolar. This signal is sent even when in diagnostic loopback and always over-rides signals from the framers. Default: AIS sent if DLB is enabled.

LAIS[1:0] PORT.CR1	Frame Mode	Description	AIS Code
00	DS3	Automatic AIS when DLB is enabled (PORT.CR4.LBM = 1XX)	DS3AIS
00	E3	Automatic AIS when DLB is enabled	UA1
00	Clear Channel	Automatic AIS when DLB is enabled	UA1
01	Any	Send UA1	UA1
10	DS3	Send AIS	DS3AIS
10	E3 or Clear Channel	Send AIS	UA1
11	Any	Disable	none

Bit 9: BERT Enable (BENA). This bit is used to enable the transmit and receive BERT logic. The BERT pattern will be the payload data replacing the cell or packet data from the system interface.

0 = BERT logic disabled and powered down
1 = BERT logic enabled

Note: Data on the receive side will flow to the Cell/Packet processor regardless of the setting of BENA. The packet processor could detect packets even if not desired. To disable possible packets on the system interface, set the FIFO.RCR.RFRST bit.

Bit 8: HDLC Select (HDSEL). This bit is used to select the source of the receive HDLC controller and the destination of the transmit HDLC controller when in DS3 or E3 PLCP mode. When not in any PLCP mode, this bit has no meaning and the HDLC controllers are connected to the DS3 or E3 framers if in DS3 or E3 mode.

0 = Connect HDLC controller to DS3 or E3 framers
1 = Connect HDLC controller to PLCP framers

Bit 7: Transmit Manual Error Insert (TMEI) This bit is used to insert errors in all error insertion logic configured to use this bit when *PORT.CR1*.MEIM=0. The error(s) will be inserted when this bit is toggled low to high.

Bit 6: Transmit Manual Error Insert Mode (MEIM). These bits select the method transmit manual error insertion for this port for error generators configured to use the external TMEI signal. The global updates are controlled by the GL.CR1.MEIMS bit.

0 = Port software update via *PORT.CR1*.TMEI
1 = Global update source

Bit 4: Performance Monitor Update Mode (PMUM). These bits select the method of updating the performance monitor registers. The global updates are controlled by the *GL.CR1*.GPM[1:0] bits.

0 = Port software update
1 = Global update

Bit 3: Performance Monitor Register Update (PMU) This bit is used to update all of the performance monitor registers configured to use this bit when *PORT.CR1*.PMUM=0. The performance registers configured to use this signal will be updated with the latest count value and the counters reset when this bit is toggled low to high. The bit should remain high until the performance register update status bit (*PORT.SR*.PMS) goes high, then it should be brought back low which clears the PMS status bit.

Bit 2: Power-Down (PD). When this bit is set, the digital logic for this port are powered down and considered “out of service”. The logic is powered down by stopping the clocks. See the Reset and Power-Down Section 10.3.

0 = Normal operation
1 = Power-down port circuits (default state)

Bit 1: Reset Data Path (RSTDP). When this bit is set, it will force all of the internal data path registers, in this port to their default state. This bit must be set high for a minimum of 100ns and then set back low. See the Reset and Power-Down Section 10.3. Note: The Default State of this bit is 1 (after a general reset (port or global), this bit will be set to one).

0 = Normal operation
1 = Force all data path registers to their default values

Bit 0: Reset (RST). When this bit is set, it will force all the internal data path and status and control registers (except this RST bit) of this port to their default state. See the Reset and Power-Down Section 10.3. This bit must be set high for a minimum of 100ns and then set back low. This software bit is logically OR’ed with the inverted hardware signal $\overline{\text{RST}}$ and the GL.CR1.RST bit.

0 = Normal operation
1 = Force all internal registers to their default values

Register Name: **PORT.CR2**
Register Description: **Port Control Register 2**
Register Address: **(0,2,4,6)42h**

Bit #	15	14	13	12	11	10	9	8
Name	TLEN	Reserved	Reserved	Reserved	RCDV8	LM	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RCDIS	PMCPE	FM5	FM4	FM3	FM2	FM1	FM0
Default	0	0	0	0	0	0	0	0

Bit 15: Transmit Line IO Signal Enable (TLEN). This bit is used to enable to transmit line interface output pins TLCLKn, TPOSn/TDATn and TNEGn.

0 = Disable, force outputs low
1 = Enable normal operation

Bit 11: Receive ATM Cell Delineation Verify 8 Enable (RCDV8). This bit determines the number of good cells required for the ATM cell delineator state machine to transition from the “Verify” state to the “Update” state. This setting also determines how many valid cells required to clear the OCD status bit.

0 = Six valid ATM cells are required (typical for framed cells)
1 = Eight valid ATM cells are required (typical for unframed cells)

Bit 10: Port Interface Mode (LM). The **LM** bit selects main port interface operational modes.

Table 10-31. Line Mode Select Bits - LM

LINE.TCR.**TZSD** & LINE.RCR.**RZSD**	**LM** (PORT.CR2)	**Line Code**
0	0	B3ZS/HDB3
1	0	AMI
X	1	UNI

Bit 7: Receive Cell Delineator Disable (RCDIS). This bit determines if the ATM cell delineator in the ATM cell processor is active in PLCP modes. This ATM cell delineator in the ATM cell processor is always active in non-PLCP ATM cell modes.

0 = ATM cell delineation is determined in the ATM cell processor
1 = ATM cell delineation is determined in the PLCP framer (Note: RCDIS = 1 is not a recommended mode.)

Bit 6: POS-PHY Mode Cell Processor Enable (PMCPE). This bit determines the associated transmit and receive port interface processing (cell/packet) to be performed in the POS-PHY mode. It is only active in POS-PHY mode when PLCP is not enabled. When PLCP is enabled in POS-PHY mode, cell processing is performed.

0 = Packet processing will be performed
1 = Cell processing will be performed

Bits 5 to 0: Framing mode (FM[5:0]). The FM[5:0] bits select main framing operational modes. Default: DS3 C-bit.

FM[5:0]	DESCRIPTION	LINE CODE	SYSTEM	FIGURE
0 00 000	DS3 C-bit	B3ZS/AMI/UNI	ATM/PKT	Figure 6-1
0 00 001	DS3 C-bit - OHM	UNI	ATM/PKT	Figure 6-2
0 00 010	DS3 C-bit Internal Fractional	B3ZS/AMI/UNI	ATM/PKT	Figure 6-3
0 00 011	DS3 C-bit External Fractional	B3ZS/AMI/UNI	ATM/PKT	Figure 6-4
0 00 100	DS3 C-bit PLCP	B3ZS/AMI/UNI	ATM	Figure 6-6
0 00 101	DS3 C-bit PLCP - OHM	UNI	ATM	Figure 6-7
0 00 110	DS3 C-bit Flexible Fractional	B3ZS/AMI/UNI	ATM/PKT	Figure 6-5
0 01 000	DS3 M23	B3ZS/AMI/UNI	ATM/PKT	Figure 6-1
0 01 001	DS3 M23 - OHM	UNI	ATM/PKT	Figure 6-2
0 01 010	DS3 M23 Internal Fractional	B3ZS/AMI/UNI	ATM/PKT	Figure 6-3
0 01 011	DS3 M23 External Fractional	B3ZS/AMI/UNI	ATM/PKT	Figure 6-4
0 01 100	DS3 M23 PLCP	B3ZS/AMI/UNI	ATM	Figure 6-6
0 01 101	DS3 M23 PLCP - OHM	UNI	ATM	Figure 6-7
0 01 110	DS3 M23 Flexible Fractional	B3ZS/AMI/UNI	ATM/PKT	Figure 6-5
0 10 000	E3 G.751	HDB3/AMI/UNI	ATM/PKT	Figure 6-1
0 10 001	E3 G.751 – OHM	UNI	ATM/PKT	Figure 6-2
0 10 010	E3 G.751 Internal Fractional	HDB3/AMI/UNI	ATM/PKT	Figure 6-3
0 10 011	E3 G.751 External Fractional	HDB3/AMI/UNI	ATM/PKT	Figure 6-4
0 10 100	E3 G.751 PLCP	HDB3/AMI/UNI	ATM	Figure 6-6
0 10 101	E3 G.751 PLCP – OHM	UNI	ATM	Figure 6-7
0 10 110	E3 G.751 Flexible Fractional	HDB3/AMI/UNI	ATM/PKT	Figure 6-5
0 11 000	E3 G.832	HDB3/AMI/UNI	ATM/PKT	Figure 6-1
0 11 001	E3 G.832- OHM	UNI	ATM/PKT	Figure 6-2
0 11 010	E3 G.832 Internal Fractional	HDB3/AMI/UNI	ATM/PKT	Figure 6-3
0 11 011	E3 G.832 External Fractional	HDB3/AMI/UNI	ATM/PKT	Figure 6-4
0 11 100	Reserved			
0 11 101	Reserved			
0 11 110	E3 G.832 Flexible Fractional	HDB3/AMI/UNI	ATM/PKT	Figure 6-5
1 00 0X0	DS3 Clear Channel	B3ZS/AMI/UNI	ATM/PKT	Figure 6-8
1 00 001	DS3 Clear Channel—OHM	UNI	ATM/PKT	Figure 6-9
1 00 011	DS3 Clear Channel—OHM Octet Aligned	UNI	ATM/PKT	Figure 6-10
1 01 0X0	STS-1 Clear Channel	B3ZS/AMI/UNI	ATM/PKT	Figure 6-8
1 01 001	STS-1 Clear Channel—OHM	UNI	ATM/PKT	Figure 6-9
1 01 011	STS-1 Clear Channel—OHM Octet Aligned	UNI	ATM/PKT	Figure 6-10
1 1X 0X0	E3 Clear Channel	HDB3/AMI/UNI	ATM/PKT	Figure 6-8
1 1X 001	E3 Clear Channel —OHM	UNI	ATM/PKT	Figure 6-9
1 1X 011	E3 Clear Channel—OHM Octet Aligned	UNI	ATM/PKT	Figure 6-10

Register Name: **PORT.CR3**
Register Description: **Port Control Register 3**
Register Address: **(0,2,4,6)44h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	RCLKS	RSOFOS	RPFPE	TCLKS	TSOFOS	TPFPE
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	P8KRS1	P8KRS0	P8KREF	LOOPT	CLADC	RFTS	TFTS	TLTS
Default	0	0	0	0	0	0	0	0

Bit 13: Receive Clock Output Select (RCLKS). This bit is used to select the function of the RPOHCLKn / RGCLKn / RCLKOn pins. See Table 10-29.

0 = Selects the RGCLKn signal, RPOHCLKn signal, or the drive low pin function.
1 = Selects RCLKOn signal.

Bit 12: Receive Start Of Frame Output Select (RSOFOS). This bit is to select the function of the RSOFOn / RDENn pins. See Table 10-28.

0 = Selects RDENn signal.
1 = Selects RSOFOn signal.

Bit 11: Receive PLCP/Fractional Port Enable (RPFPE). This bit is used to enable the receive PLCP/Fractional port pins. See tables in section 10.5.9.2.

0 = Disable receive PLCP/Fractional port pins
1 = Enable receive PLCP/Fractional port pins

Bit 10: Transmit Clock Output Select (TCLKS). This bit is used to select the function of the TPOHCLKn / TGCLKn / TCLKOn pins. See Table 10-22.

0 = Selects TGCLKn or TPOHCLKn signal.
1 = Selects TCLKOn signal.

Bit 9: Transmit Start Of Frame Output Select (TSOFOS). This bit is used to select the function of the TSOFOn / TDENn pins. See Table 10-21.

0 = Selects TDENn signal.
1 = Selects TSOFOn signal.

Bit 8: Transmit PLCP/Fractional Port Enable (TPFPE). This bit is used to enable the transmit PLCP/fractional port pins. See tables in section 10.5.9.1.

0 = Disable transmit PLCP/Fractional port pins
1 = Enable transmit PLCP/Fractional port pins

Bits 7 and 6: Port 8 kHz Reference Source Select [1:0] (P8KRS[1:0]). These bits select the source of the 8 kHz reference from the port sources. The 8K reference for this port can be used as the global 8K reference source. See Table 10-11.

Table 10-11. Port 8kHz Reference Source Table

PORT.CR3.P8KRS[1:0]	Source
0X	Receive PLCP 8kHZ output
10	Receive RLCLKn pin
11	Transmit internal framer clock (based on TCLKIn pin or CLAD clock)

Bit 5: Port 8 kHz Reference Source (P8KREF). This bit selects the source of the 8 kHz reference for PLCP trailer operation and one-second timer.

0 = 8 kHz reference from global source
1 = 8 kHz reference from this ports selected source

Bit 4: Loop Time Enable (LOOPT). When this bit is set, the port is in loop time mode. The transmit clock is set to the receive clock from the RLCLKn pin or the recovered clock from the CLAD clock and the TCLKIn pin is not used. This function of this bit is conditional on other control bits. See Table 10-3 for more details.

0 = Normal transmit clock operation
1 = Transmit using the receive clock

Bit 3: CLAD Transmit Clock Source Control (CLADC). This bit is used to enable the CLAD clocks as the source of the internal transmit clock. This function of this bit is conditional on other control bits. See Table 10-3 for more details.

0 = Use CLAD clocks for the transmit clock as appropriate
1 = Do not use CLAD clocks for the transmit clock – (if no loopback is enabled, TCLKIn is the source)

Bit 2: Receive Framer IO Signal Timing Select (RFTS). This bit controls the timing reference for the signals on the receive framer interface IO pins. The pins controlled are RSERn, RSOFOn / RDENn / RFOHENn and RFOHENn. See Table 10-7 for more details.

0 = Use output clocks for timing reference
1 = Use input clocks for timing reference

Bit 1: Transmit Framer IO Signal Timing Select (TFTS). This bit controls the timing reference for the signals on the transmit framer interface IO pins. The pins controlled are TOHMIn / TSOFIn, TFOHn / TSERn, TFOHENIn and TSOFOn / TDENn / TFOHENOn. See Table 10-6 for more details.

0 = Use output clocks for timing reference
1 = Use input clocks for timing reference

Bit 0: Transmit Line IO Signal Timing Select (TLTS). This bit controls the timing reference for the signals on the transmit line interface IO pins. The pins controlled are TPOSn / TDATn and TNEGn / TOHMOn. See Table 10-5 for more details.

0 = Use output clocks for timing reference
1 = Use input clocks for timing reference

Register Name: **PORT.CR4**
Register Description: **Port Control Register 4**
Register Address: **(0,2,4,6)46h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	SLB	LBM2	LBM1	LBM0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	GPIOB3	GPIOB2	GPIOB1	GPIOB0	GPIOA3	GPIOA2	GPIOA1	GPIOA0
Default	0	0	0	0	0	0	0	0

Bit 11: System Bus Loopback (SLB). This bit enables the system bus loopback mode per port when the bit is set. ATM cells and/or HDLC packets are looped back from the transmit system bus to the receive system bus through the FIFOs. See Figure 10-9 for the block diagram highlighting loopback features.

Bits 10 to 8: Loopback Mode [2:0] (LBM[2:0]). These bits select the loopback modes for analog loopback (ALB), line loopback (LLB), payload loopback (PLB) and diagnostic loopback (DLB). See Table 10-15 for the loopback select codes. Default: No Loopback.

LBM[2:0]	ALB	LLB	PLB	DLB
000	0	0	0	0
001	1	0	0	0
010	0	1	0	0
011	0	0	1	0
10X	0	0	0	1
110	0	1	0	1

111	0	0	0	1

Bits 7 to 4: General-Purpose I/O B Output Select[3:0] (GPIOB[3:0]) These bits determine which alarm status signal to output on the GPIO2(port 1), GPIO4(port 2), GPIO6(port 3) or GPIO8(port 4) pins. The GPIO pin must be enabled by setting the bits in the GL.GIOCR and either GL.CR1 or GL.CR2 registers to output the selected alarm signal. See Table 10-13. See Table 10-14 for the alarm select codes.

Bits 3 to 0: General-Purpose I/O A Output Select[3:0] (GPIOA[3:0]) These bits determine which alarm status signal to output on the GPIO1(port 1), GPIO3(port 2), GPIO5(port 3) or GPIO7(port 4) pins. The GPIO pin must be enabled for output by setting the bits in the GL.GIOCR register. See Table 10-13 for configuration settings. See Table 10-14 below for the alarm select codes.

Table 10-14. GPIO Port Alarm Monitor Select

PORT.CR4 GPIO(A/B)[3:0]	LINE LOS	DS3/E3 OOF	DS3/E3 LOF	DS3/E3 AIS	DS3/E3 RAI	DS3 IDLE	PLCP OOF	PLCP LOF	PLCP RAI	ATM OCD	ATM LCD
0000	X										
0001		X									
0010			X								
0011				X							
0100					X						
0101						X					
0110							X				
0111								X			
1000									X		
1001										X	
1010											X
1011	X		X	X							
1100								X			X
1101	X		X	X				X			X
1110					X	X			X		
1111	X	X	X	X	X	X	X	X	X	X	X

Register Name: **PORT.INV1**
Register Description: **Port IO Invert Control Register 1**
Register Address: **(0,2,4,6)4Ah**

Bit #	15	14	13	12	11	10	9	8
Name	TPDEI	TPDTI	--	TPOHSI	TPOHEI	TPOHI	TOHSI	TOHEI
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	TOHI	TOHCKI	TSOFII	TNEGI	TPOSI	TLCKI	TCKOI	TCKII
Default	0	0	0	0	0	0	0	0

Bit 15: TPDENOn Invert (TPDEI). This bit inverts the TPDENOn pin when set.

Bit 14: TPDATn Invert (TPDTI). This bit inverts the TPDATn pin when set.

Bit 12: TPOHSOFn / TSOFOn / TDENn/ TFOHENOn Invert (TPOHSI). This bit inverts the TPOHSOFn / TSOFOn / TDENn / TFOHENOn pin when set.

Bit 11: TPOHENn / TFOHENIn / TPDENIn Invert (TPOHEI). This bit inverts the TPOHENIn / TFOHENIn / TPDENIn pin when set.

Bit 10: TPOHn / TFOHn / TSERn Invert (TPOHI). This bit inverts the TPOHn / TFOHn / TSERn pin when set.

Bit 9: TOHSOFn Invert (TOHSI). This bit inverts the TOHSOFn pin when set.

Bit 8: TOHENn Invert (TOHEI). This bit inverts the TOHENn pin when set.

Bit 7: TOHn Invert (TOHI). This bit inverts the TOHn pin when set.

Bit 6: TOHCLKn Invert (TOHCKI). This bit inverts the TOHCLKn pin when set.

Bit 5: TSOFIn / TOHMIn Invert (TSOFII). This bit inverts the TSOFIn / TOHMIn pin when set.

Bit 4: TNEGn / TOHMOn Invert (TNEGI). This bit inverts the TNEGn / TOHMOn pin when set.

Bit 3: TPOSn / TDATn Invert (TPOSI). This bit inverts the TPOSn / TDATn pin when set.

Bit 2: TLCLKn Invert (TLCKI). This bit inverts the TLCLKn pin when set.

Bit 1: TCLKOn / TGCLKn / TPOHCLKn Invert (TCKOI). This bit inverts the TCLKOn / TGCLKn / TPOHCLKn pin when set.

Bit 0: TCLKIn Invert (TCKII). This bit inverts the TCLKIn pin when set.

Register Name: **PORTINV2**
Register Description: **Port IO Invert Control Register 2**
Register Address: **(0,2,4,6)4Ch**

Bit #	15	14	13	12	11	10	9	8
Name	--	RPDTI	RFOHEI	RPOHSI	--	RPOHI	ROHSI	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	ROHI	ROHCKI	--	RNEGI	RPOSI	RLCKI	RCKOI	--
Default	0	0	0	0	0	0	0	0

Bit 14: RPDATn Invert (RPDTI). This bit inverts the RPDATn pin when set.

Bit 13: RFOHENIn / RPDENIn Invert (RFOHEI). This bit inverts the RFOHENIn / RPDENIn pin when set.

Bit 12: RPOHSOFn / RSOFOn / RDENn / RFOHENOn Invert (RPOHSI). This bit inverts the RPOHSOFn / RSOFOn / RDENn / RFOHENOn pin when set.

Bit 10: RPOHn / RSERn Invert (RPOHI). This bit inverts the RPOHn / RSERn pin when set.

Bit 9: ROHSOFn Invert (ROHSI). This bit inverts the ROHSOFn pin when set.

Bit 7: ROHn Invert (ROHI). This bit inverts the ROHn pin when set.

Bit 6: ROHCLKn Invert (ROHCKI). This bit inverts the ROHCLKn pin when set.

Bit 4: RNEGn / RLCVn / ROHMIn Invert (RNEGI). This bit inverts the RNEGn / RLCVn / ROHMIn when set.

Bit 3: RPOSn / RDATn Invert (RPOSI). This bit inverts the RPOSn / RDATn pin when set.

Bit 2: RLCLKn Invert (RLCKI). This bit inverts the RLCLKn pin when set.

Bit 1: RCLKOn / RGCLKn / RPOHCLKn Invert (RCKOI). This bit inverts the RCLKOn / RGCLKn / RPOHCLKn pin when set.

Register Name: **PORT.ISR**
Register Description: **Port Interrupt Status Register**
Register Address: **(0,2,4,6)50h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	PSR	LCSR

Bit #	7	6	5	4	3	2	1	0
Name	TTSR	FSR	HSR	BSR	SFSR	CPSR	PPSR	FMSR

Bit 9: Port Status Register Interrupt Status (PSR) This bit is set when any of the latched status register bits, that are enabled for interrupt, in the *PORT.SRL* register are set. The interrupt pin will be driven when this bit is set and the corresponding GL.ISRIE.PISRIE[4:1] is set.

Bit 8: Line Code Status Register Interrupt Status (LCSR) This bit is set when any of the latched status register bits, that are enabled for interrupt, in the B3ZS/HDB3 Line Encoder/Decoder block are set. The interrupt pin will be driven when this bit is set and the corresponding GL.ISRIE.PISRIE[4:1] is set.

Bit 7: Trail Trace Status Register Interrupt Status (TTSR) This bit is set when any of the latched status register bits, that are enabled for interrupt, in the trail trace block are set. The interrupt pin will be driven when this bit is set and the corresponding GL.ISRIE.PISRIE[4:1] is set.

Bit 6: FEAC Status Register Interrupt Status (FSR) This bit is set when any of the latched status register bits, that are enabled for interrupt, in the FEAC block are set. The interrupt pin will be driven when this bit is set and the corresponding GL.ISRIE.PISRIE[4:1] is set.

Bit 5: HDLC Status Register Interrupt Status (HSR) This bit is set when any of the latched status register bits, that are enabled for interrupt, in the HDLC block are set. The interrupt pin will be driven when this bit is set and the corresponding GL.ISRIE.PISRIE[4:1] is set.

Bit 4: BERT Status Register Interrupt Status (BSR) This bit is set when any of the latched status register bits, that are enabled for interrupt, in the BERT block are set. The interrupt pin will be driven when this bit is set and the corresponding GL.ISRIE.PISRIE[4:1] is set.

Bit 3: System FIFO Status Register Interrupt Status (SFSR) This bit is set when any of the latched status register bits, that are enabled for interrupt, in either the transmit or receive FIFO block are set. The interrupt pin will be driven when this bit is set and the corresponding GL.ISRIE.PISRIE[4:1] is set.

Bit 2: Cell/Packet Status Register Interrupt Status (CPSR) This bit is set when any of the latched status register bits, that are enabled for interrupt, in the active transmit or receive cell processor or packet processor block are set. The interrupt pin will be driven when this bit is set and the corresponding GL.ISRIE.PISRIE[4:1] is set.

Bit 1: PLCP Status Register Interrupt Status (PPSR) This bit is set when any of the latched status register bits, that are enabled for interrupt, in the active PLCP block are set. The interrupt pin will be driven when this bit is set and the corresponding GL.ISRIE.PISRIE[4:1] is set.

Bit 0: Framer Status Register Interrupt Status (FMSR) This bit is set when any of the latched status register bits, that are enabled for interrupt, in the active DS3 or E3 framer block are set. The interrupt pin will be driven when this bit is set and the corresponding GL.ISRIE.PISRIE[4:1] is set.

Register Name: **PORT.SR**
Register Description: **Port Status Register**
Register Address: **(0,2,4,6)52h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	Reserved	Reserved	PMS

Bit 0: Performance Monitoring Update Status (PMS) This bits indicates the status of all active performance monitoring register and counter update signals in this port. It is an “AND” of all update status bits and is not set until all performance registers are updated and the counters reset. In software update modes, the update request bit PORT.CR1.PMU should be held high until this status bit goes high.

0 = The associated update request signal is low
1 = The requested performance register updates are all completed

Register Name: **PORT.SRL**
Register Description: **Port Status Register Latched**
Register Address: **(0,2,4,6)54h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	RLCLKA	TCLKIA	--	--	--	Reserved	Reserved	PMSL

Bit 7: Receive Line Clock Activity Status Latched (RLCLKA) This bit will be set when the signal on the RLCLKn pin for this port is active.

Bit 6: Transmit Input Clock Activity Status Latched (TCLKIA) This bit will be set when the signal on the TCLKIn pin for this port is active.

Bit 0: Performance Monitoring Update Status Latched (PMSL) This bit will be set when the *PORT.SR*.PMS status bit changes from low to high. This bit will also set the *PORT.ISR*.PSR status bit if the *PORT.SRIE*.PMUIE bit is enabled. The interrupt pin will be driven when this bit is set, the *PORT.SRIE*.PMUIE bit is set, and the *PORT.SRIE*.PMSIE bit are set.

Register Name: **PORT.SRIE**
Register Description: **Port Status Register Interrupt Enable**
Register Address: **(0,2,4,6)56h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	Reserved	Reserved	PMSIE
Default	0	0	0	0	0	0	0	0

Bit 0: Performance Monitoring Update Latched Status Interrupt Enable (PMSIE) The interrupt pin will be driven when this bit is enabled and the *PORT.SRL*.PMSL bit is set and the bit in GL.ISRIE.PISRIE[4:1] that corresponds to this port is enabled.

12.5 BERT

12.5.1 BERT Register Map

The BERT utilizes twelve registers.

Note: The BERT Registers will be cleared when GL.CR1.RSTDP or PORT.CR1.RSTDP or PORT.CR1.PD is set.

Table 12-24. BERT Register Map

Address	Register	Register Description
(0,2,4,6)60h	BERT.CR	BERT Control Register
(0,2,4,6)62h	BERT.PCR	BERT Pattern Configuration Register
(0,2,4,6)64h	BERT.SPR1	BERT Seed/Pattern Register #1
(0,2,4,6)66h	BERT.SPR2	BERT Seed/Pattern Register #2
(0,2,4,6)68h	BERT.TEICR	BERT Transmit Error Insertion Control Register
(0,2,4,6)6Ah	--	Unused
(0,2,4,6)6Ch	BERT.SR	BERT Status Register
(0,2,4,6)6Eh	BERT.SRL	BERT Status Register Latched
(0,2,4,6)70h	BERT.SRIE	BERT Status Register Interrupt Enable
(0,2,4,6)72h	--	Unused
(0,2,4,6)74h	BERT.RBECR1	BERT Receive Bit Error Count Register #1
(0,2,4,6)76h	BERT.RBECR2	BERT Receive Bit Error Count Register #2
(0,2,4,6)78h	BERT.RBCR1	BERT Receive Bit Count Register #1
(0,2,4,6)7Ah	BERT.RBCR2	BERT Receive Bit Count Register #2
(0,2,4,6)7Ch	--	Unused
(0,2,4,6)7Eh	--	Unused

12.5.2 BERT Register Bit Descriptions

Register Name: **BERT.CR**
Register Description: **BERT Control Register**
Register Address: **(0,2,4,6)60h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	PMUM	LPMU	RNPL	RPIC	MPR	APRD	TNPL	TPIC
Default	0	0	0	0	0	0	0	0

Bit 7: Performance Monitoring Update Mode (PMUM) – When 0, a performance monitoring update is initiated by the LPMU register bit. When 1, a performance monitoring update is initiated by the global or port PMU register bit. Note: If the LPMU bit or the global or port PMU bit is one, changing the state of this bit may cause a performance monitoring update to occur.

Bit 6: Local Performance Monitoring Update (LPMU) – This bit causes a performance monitoring update to be initiated if local performance monitoring update is enabled (PMUM = 0). A 0 to 1 transition causes the performance monitoring registers to be updated with the latest data, and the counters reset (0 or 1). For a second performance monitoring update to be initiated, this bit must be set to 0, and back to 1. If LPMU goes low before the PMS bit goes high; an update might not be performed. This bit has no affect when PMUM=1.

Bit 5: Receive New Pattern Load (RNPL) – A zero to one transition of this bit will cause the programmed test pattern (QRSS, PTS, PLF[4:0}, PTF[4:0], and BSP[31:0]) to be loaded in to the receive pattern generator. This bit must be changed to zero and back to one for another pattern to be loaded. Loading a new pattern will forces the receive pattern generator out of the “Sync” state which causes a resynchronization to be initiated. Note: QRSS, PTS, PLF[4:0}, PTF[4:0], and BSP[31:0] must not change from the time this bit transitions from 0 to 1 until four receive clock cycles after this bit transitions from 0 to 1. Register bit PORT.CR1.BENA must be set and the receive clock running in order for the pattern load to take affect.

Bit 4: Receive Pattern Inversion Control (RPIC) – When 0, the receive incoming data stream is not altered. When 1, the receive incoming data stream is inverted.

Bit 3: Manual Pattern Resynchronization (MPR) – A zero to one transition of this bit will cause the receive pattern generator to resynchronize to the incoming pattern. This bit must be changed to zero and back to one for another resynchronization to be initiated. Note: A manual resynchronization forces the receive pattern generator out of the “Sync” state.

Bit 2: Automatic Pattern Resynchronization Disable (APRD) – When 0, the receive pattern generator will automatically resynchronize to the incoming pattern if six or more times during the current 64-bit window the incoming data stream bit and the receive pattern generator output bit did not match. When 1, the receive pattern generator will not automatically resynchronize to the incoming pattern.

Bit 1: Transmit New Pattern Load (TNPL) – A zero to one transition of this bit will cause the programmed test pattern (QRSS, PTS, PLF[4:0}, PTF[4:0], and BSP[31:0]) to be loaded in to the transmit pattern generator. This bit must be changed to zero and back to one for another pattern to be loaded. Note: QRSS, PTS, PLF[4:0}, PTF[4:0], and BSP[31:0] must not change from the time this bit transitions from 0 to 1 until four transmit clock cycles after this bit transitions from 0 to 1. Register bit PORT.CR1.BENA must be set and the receive clock running in order for the pattern load to take affect.

Bit 0: Transmit Pattern Inversion Control (TPIC) – When 0, the transmit outgoing data stream is not altered. When 1, the transmit outgoing data stream is inverted.

Register Name: **BERT.PCR**
Register Description: **BERT Pattern Configuration Register**
Register Address: **(0,2,4,6)62h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	PTF4	PTF3	PTF2	PTF1	PTF0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	QRSS	PTS	PLF4	PLF3	PLF2	PLF1	PLF0
Default	0	0	0	0	0	0	0	0

Bits 12 to 8: Pattern Tap Feedback (PTF[4:0]) – These five bits control the PRBS “tap” feedback of the pattern generator. The “tap” feedback will be from bit y of the pattern generator (y = PTF[4:0] +1). These bits are ignored when programmed for a repetitive pattern. For a PRBS signal, the feedback is an XOR of bit n and bit y.

Bit 6: QRSS Enable (QRSS) – When 0, the pattern generator configuration is controlled by PTS, PLF[4:0], and PTF[4:0], and BSP[31:0]. When 1, the pattern generator configuration is forced to a PRBS pattern with a generating polynomial of $x^{20} + x^{17} + 1$. The output of the pattern generator will be forced to one if the next fourteen output bits are all zero.

Bit 5: Pattern Type Select (PTS) – When 0, the pattern is a PRBS pattern. When 1, the pattern is a repetitive pattern.

Bits 4 to 0: Pattern Length Feedback (PLF[4:0]) – These five bits control the “length” feedback of the pattern generator. The “length” feedback will be from bit n of the pattern generator (n = PLF[4:0] +1). For a PRBS signal, the feedback is an XOR of bit n and bit y. For a repetitive pattern the feedback is bit n.

Register Name: **BERT.SPR1**
Register Description: **BERT Seed/Pattern Register #1**
Register Address: **(0,2,4,6)64h**

Bit #	15	14	13	12	11	10	9	8
Name	BSP15	BSP14	BSP13	BSP12	BSP11	BSP10	BSP9	BSP8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	BSP7	BSP6	BSP5	BSP4	BSP3	BSP2	BSP1	BSP0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: BERT Seed/Pattern (BSP[15:0]) – Lower sixteen bits of 32 bits. Register description follows next register.

Register Name: **BERT.SPR2**
Register Description: **BERT Seed/Pattern Register #2**
Register Address: **(0,2,4,6)66h**

Bit #	15	14	13	12	11	10	9	8
Name	BSP31	BSP30	BSP29	BSP28	BSP27	BSP26	BSP25	BSP24
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	BSP23	BSP22	BSP21	BSP20	BSP19	BSP18	BSP17	BSP16
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: BERT Seed/Pattern (BSP[31:16]) - Upper 16 bits of 32 bits.

BERT Seed/Pattern (BSP[31:0]) – These 32 bits are the programmable seed for a transmit PRBS pattern, or the programmable pattern for a transmit or receive repetitive pattern. BSP(31) will be the first bit output on the transmit side for a 32-bit repetitive pattern or 32-bit length PRBS. BSP(31) will be the first bit input on the receive side for a 32-bit repetitive pattern.

Register Name: **BERT.TEICR**
Register Description: **BERT Transmit Error Insertion Control Register**
Register Address: **(0,2,4,6)68h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	TEIR2	TEIR1	TEIR0	BEI	TSEI	MEIMS
Default	0	0	0	0	0	0	0	0

Bits 5 to 3: Transmit Error Insertion Rate (TEIR[2:0]) – These three bits indicate the rate at which errors are inserted in the output data stream. One out of every 10^n bits is inverted. TEIR[2:0] is the value n. A TEIR[2:0] value of 0 disables error insertion at a specific rate. A TEIR[2:0] value of 1 result in every 10^{th} bit being inverted. A TEIR[2:0] value of 2 result in every 100^{th} bit being inverted. Error insertion starts when this register is written to with a TEIR[2:0] value that is non-zero. If this register is written to during the middle of an error insertion process, the new error rate will be started after the next error is inserted.

TEIR[2:0]	Error Rate
000	Disabled
001	$1*10^{-1}$
010	$1*10^{-2}$
011	$1*10^{-3}$
100	$1*10^{-4}$
101	$1*10^{-5}$
110	$1*10^{-6}$
111	$1*10^{-7}$

Bit 2: Bit Error Insertion Enable (BEI) – When 0, single bit error insertion is disabled. When 1, single bit error insertion is enabled.

Bit 1: Transmit Single Error Insert (TSEI) – This bit causes a bit error to be inserted in the transmit data stream if manual error insertion is disabled (MEIMS = 0) and single bit error insertion is enabled. A 0 to 1 transition causes a single bit error to be inserted. For a second bit error to be inserted, this bit must be set to 0, and back to 1. Note: If MEIMS is low, and this bit transitions more than once between error insertion opportunities, only one error will be inserted.

Bit 0: Manual Error Insert Mode Select (MEIMS) – When 0, error insertion is initiated by the TSEI register bit. When 1, error insertion is initiated by the transmit manual error insertion signal (TMEI). Note: If TMEI or TSEI is one, changing the state of this bit may cause a bit error to be inserted.

Register Name: **BERT.SR**
Register Description: **BERT Status Register**
Register Address: **(0,2,4,6)6Ch**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	PMS	--	BEC	OOS

Bit 3: Performance Monitoring Update Status (PMS) – This bit indicates the status of the receive performance monitoring register (counters) update. This bit will transition from low to high when the update is completed. PMS will be forced low when the LPMU bit (PMUM = 0) or the global or port PMU bit (PMUM=1) goes low.

Bit 1: Bit Error Count (BEC) – When 0, the bit error count is zero. When 1, the bit error count is one or more. This bit is cleared when the user updates the BERT counters via the PMU bit (BERT.CR).

Bit 0: Out Of Synchronization (OOS) – When 0, the receive pattern generator is synchronized to the incoming pattern. When 1, the receive pattern generator is not synchronized to the incoming pattern.

Register Name: **BERT.SRL**
Register Description: **BERT Status Register Latched**
Register Address: **(0,2,4,6)6Eh**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	PMSL	BEL	BECL	OOSL

Bit 3: Performance Monitoring Update Status Latched (PMSL) – This bit is set when the PMS bit transitions from 0 to 1.

Bit 2: Bit Error Latched (BEL) – This bit is set when a bit error is detected.

Bit 1: Bit Error Count Latched (BECL) – This bit is set when the BEC bit transitions from 0 to 1.

Bit 0: Out Of Synchronization Latched (OOSL) – This bit is set when the OOS bit changes state.

Register Name: **BERT.SRIE**
Register Description: **BERT Status Register Interrupt Enable**
Register Address: **(0,2,4,6)70h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	PMSIE	BEIE	BECIE	OOSIE
Default	0	0	0	0	0	0	0	0

Bit 3: Performance Monitoring Update Status Interrupt Enable (PMSIE) – This bit enables an interrupt if the PMSL bit is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 2: Bit Error Interrupt Enable (BEIE) – This bit enables an interrupt if the BEL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 1: Bit Error Count Interrupt Enable (BECIE) – This bit enables an interrupt if the BECL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Out Of Synchronization Interrupt Enable (OOSIE) – This bit enables an interrupt if the OOSL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **BERT.RBECR1**
Register Description: **BERT Receive Bit Error Count Register #1**
Register Address: **(0,2,4,6)74h**

Bit #	15	14	13	12	11	10	9	8
Name	BEC15	BEC14	BEC13	BEC12	BEC11	BEC10	BEC9	BEC8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	BEC7	BEC6	BEC5	BEC4	BEC3	BEC2	BEC1	BEC0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Bit Error Count (BEC[15:0]) – Lower sixteen bits of 24 bits. Register description follows next register.

Register Name: **BERT.RBECR2**
Register Description: **BERT Receive Bit Error Count Register #2**
Register Address: **(0,2,4,6)76h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	BEC23	BEC22	BEC21	BEC20	BEC19	BEC18	BEC17	BEC16
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Bit Error Count (BEC[23:16]) - Upper 8-bits of Register.

Bit Error Count (BEC[23:0]) – These twenty-four bits indicate the number of bit errors detected in the incoming data stream. This count stops incrementing when it reaches a count of FF FFFFh. This bit error counter will not increment when an OOS condition exists. This register is updated via the PMU signal (see section 10.4.5)

Register Name: **BERT.RBCR1**
Register Description: **Receive Bit Count Register #1**
Register Address: **(0,2,4,6)78h**

Bit #	15	14	13	12	11	10	9	8
Name	BC15	BC14	BC13	BC12	BC11	BC10	BC9	BC8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Bit Count (BC[15:0]) – Lower sixteen bits of 32 bits. Register description follows next register.

Register Name: **BERT.RBCR2**
Register Description: **Receive Bit Count Register #2**
Register Address: **(0,2,4,6)7Ah**

Bit #	15	14	13	12	11	10	9	8
Name	BC31	BC30	BC29	BC28	BC27	BC26	BC25	BC24
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	BC23	BC22	BC21	BC20	BC19	BC18	BC17	BC16
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Bit Count (BC[31:16]) - Upper 16 bits of 32 bits.

Bit Count (BC[31:0]) – These thirty-two bits indicate the number of bits in the incoming data stream. This count stops incrementing when it reaches a count of FFFF FFFFh. This bit counter will not increment when an OOS condition exists. This register is updated via the PMU signal (see section 10.4.5)

12.6 B3ZS/HDB3 Line Encoder/Decoder

12.6.1 Transmit Side Line Encoder/Decoder Register Map

The transmit side utilizes one register.

Table 12-25. Transmit Side B3ZS/HDB3 Line Encoder/Decoder Register Map

Address	Register	Register Description
(0,2,4,6)8Ch	LINE.TCR	Line Transmit Control Register
(0,2,4,6)8Eh	--	Unused

12.6.1.1 Register Bit Descriptions

Register Name: **LINE.TCR**
Register Description: **Line Transmit Control Register**
Register Address: **(0,2,4,6)8Ch**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	TZSD	EXZI	BPVI	TSEI	MEIMS
Default	0	0	0	0	0	0	0	0

Bit 4: Transmit Zero Suppression Encoding Disable (TZSD) – When 0, the B3ZS/HDB3 Encoder performs zero suppression (B3ZS or HDB3) and AMI encoding. When 1, zero suppression (B3ZS or HDB3) encoding is disabled, and only AMI encoding is performed.

Bit 3: Excessive Zero Insert Enable (EXZI) – When 0, excessive zero (EXZ) event insertion is disabled. When 1, EXZ event insertion is enabled.

Bit 2: Bipolar Violation Insert Enable (BPVI) – When 0, bipolar violation (BPV) insertion is disabled. When 1, BPV insertion is enabled.

Bit 1: Transmit Single Error Insert (TSEI) – This bit causes an error of the enabled type(s) to be inserted in the transmit data stream if manual error insertion is disabled (MEIMS = 0). A 0 to 1 transition causes a single error to be inserted. For a second error to be inserted, this bit must be set to 0, and back to 1. Note: If MEIMS is low, and this bit transitions more than once between error insertion opportunities, only one error will be inserted.

Bit 0: Manual Error Insert Mode Select (MEIMS) – When 0, error insertion is initiated by the TSEI register bit. When 1, error insertion is initiated by the transmit manual error insertion signal (TMEI). Note: If TMEI or TSEI is one, changing the state of this bit may cause an error to be inserted.

12.6.2 Receive Side Line Encoder/Decoder Register Map

The receive side utilizes six registers.

Table 12-26. Receive Side B3ZS/HDB3 Line Encoder/Decoder Register Map

Address	Register	Register Description
(0,2,4,6)90h	LINE.RCR	Line Receive Control Register
(0,2,4,6)92h	--	Unused
(0,2,4,6)94h	LINE.RSR	Line Receive Status Register
(0,2,4,6)96h	LINE.RSRL	Line Receive Status Register Latched
(0,2,4,6)98h	LINE.RSRIE	Line Receive Status Register Interrupt Enable
(0,2,4,6)9Ah	--	Unused
(0,2,4,6)9Ch	LINE.RBPVCR	Line Receive Bipolar Violation Count Register
(0,2,4,6)9Eh	LINE.REXZCR	Line Receive Excessive Zero Count Register

12.6.2.1 Register Bit Descriptions

Register Name: **LINE.RCR**
Register Description: **Line Receive Control Register**
Register Address: **(0.2.4.6)90h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	E3CVE	REZSF	RDZSF	RZSD
Default	0	0	0	0	0	0	0	0

Bit 3: E3 Code Violation Enable (E3CVE) – When 0, the bipolar violation count will be a count of bipolar violations. When 1, the bipolar violation count will be a count of E3 line coding violations. Note: E3 line coding violations are defined as consecutive bipolar violations of the same polarity in ITU O.161. This bit is ignored in B3ZS mode.

Bit 2: Receive BPV Error Detection Zero Suppression Code Format (REZSF) – When 0, BPV error detection detects a B3ZS signature if a zero is followed by a bipolar violation (BPV), and an HDB3 signature if two zeros are followed by a BPV. When 1, BPV error detection detects a B3ZS signature if a zero is followed by a BPV that has the opposite polarity of the BPV in the previous B3ZS signature, and an HDB3 signature if two zeros are followed by a BPV that has the opposite polarity of the BPV in the previous HDB3 signature. Note: Immediately after a reset, this bit is ignored. The first B3ZS signature is defined as a zero followed by a BPV, and the first HDB3 signature is defined as two zeros followed by a BPV. All subsequent B3ZS/HDB3 signatures will be determined by the setting of this bit.

Note: The default setting (REZSF = 0) conforms to ITU O.162. The default setting may falsely decode actual BPVs that are not codewords. It is recommended that REZSF be set to one for most applications. This setting is more robust to accurately detect codewords.

Bit 1: Receive Zero Suppression Decoding Zero Suppression Code Format (RDZSF) – When 0, zero suppression decoding detects a B3ZS signature if a zero is followed by a bipolar violation (BPV), and an HDB3 signature if two zeros are followed by a BPV. When 1, zero suppression decoding detects a B3ZS signature if a zero is followed by a BPV that has the opposite polarity of the BPV in the previous B3ZS signature, and an HDB3 signature if two zeros are followed by a BPV that has the opposite polarity of the BPV in the previous HDB3 signature. Note: Immediately after a reset ($\overline{\text{DRST}}$ or $\overline{\text{RST}}$ low), this bit is ignored. The first B3ZS signature is defined as a zero followed by a BPV, and the first HDB3 signature is defined as two zeros followed by a BPV. All subsequent B3ZS/HDB3 signatures will be determined by the setting of this bit.

Bit 0: Receive Zero Suppression Decoding Disable (RZSD) – When 0, the B3ZS/HDB3 Decoder performs zero suppression (B3ZS or HDB3) and AMI decoding. When 1, zero suppression (B3ZS or HDB3) decoding is disabled, and only AMI decoding is performed.

Register Name: **LINE.RSR**
Register Description: **Line Receive Status Register**
Register Address: **(0.2.4.6)94h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	EXZC	--	BPVC	LOS

Bit 3: Excessive Zero Count (EXZC) – When 0, the excessive zero count is zero. When 1, the excessive zero count is one or more.

Bit 1: Bipolar Violation Count (BPVC) – When 0, the bipolar violation count is zero. When 1, the bipolar violation count is one or more.

Bit 0: Loss Of Signal (LOS) – When 0, the receive line is not in a loss of signal (LOS) condition. When 1, the receive line is in an LOS condition. See Section 10.14.4.

Note: When zero suppression (B3ZS or HDB3) decoding is disabled, the LOS condition is cleared, and cannot be detected.

Register Name: **LINE.RSRL**
Register Description: **Line Receive Status Register Latched**
Register Address: **(0.2.4.6)96h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	ZSCDL	EXZL	EXZCL	BPVL	BPVCL	LOSL

Bit 5: Zero Suppression Code Detect Latched (ZSCDL) – This bit is set when a B3ZS or HDB3 signature is detected.

Bit 4: Excessive Zero Latched (EXZL) – This bit is set when an excessive zero event is detected on the incoming bipolar data stream.

Bit 3: Excessive Zero Count Latched (EXZCL) – This bit is set when the LINE.RSR.EXZC bit transitions from zero to one.

Bit 2: Bipolar Violation Latched (BPVL) – This bit is set when a bipolar violation (or E3 LCV if enabled) is detected on the incoming bipolar data stream.

Bit 1: Bipolar Violation Count Latched (BPVCL) – This bit is set when the LINE.RSR.BPVC bit transitions from zero to one.

Bit 0: Loss of Signal Change Latched (LOSL) – This bit is set when the LINE.RSR.LOS bit changes state.

Register Name: **LINE.RSRIE**
Register Description: **Line Receive Status Register Interrupt Enable**
Register Address: **(0.2.4.6)98h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	ZSCDIE	EXZIE	EXZCIE	BPVIE	BPVCIE	LOSIE
Default	0	0	0	0	0	0	0	0

Bit 5: Zero Suppression Code Detect Interrupt Enable (ZSCDIE) – This bit enables an interrupt if the *LINE.RSRL*.ZSCDL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 4: Excessive Zero Interrupt Enable (EXZIE) – This bit enables an interrupt if the *LINE.RSRL*.EXZL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 3: Excessive Zero Count Interrupt Enable (EXZCIE) – This bit enables an interrupt if the *LINE.RSRL*.EXZCL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 2: Bipolar Violation Interrupt Enable (BPVIE) – This bit enables an interrupt if the *LINE.RSRL*.BPVL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 1: Bipolar Violation Count Interrupt Enable (BPVCIE) – This bit enables an interrupt if the *LINE.RSRL*.BPVCL bit and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set. is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Loss Of Signal Interrupt Enable (LOSIE) – This bit enables an interrupt if the *LINE.RSRL*.LOSL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **LINE.RBPVCR**
Register Description: **Line Receive Bipolar Violation Count Register**
Register Address: **(0.2.4.6)9Ch**

Bit #	15	14	13	12	11	10	9	8
Name	BPV15	BPV14	BPV13	BPV12	BPV11	BPV10	BPV9	BPV8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	BPV7	BPV6	BPV5	BPV4	BPV3	BPV2	BPV1	BPV0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Bipolar Violation Count (BPV[15:0]) – These sixteen bits indicate the number of bipolar violations detected on the incoming bipolar data stream. This register is updated via the PMU signal (see Section 10.4.5).

Register Name: **LINE.REXZCR**
Register Description: **Line Receive Excessive Zero Count Register**
Register Address: **(0.2.4.6)9Eh**

Bit #	15	14	13	12	11	10	9	8
Name	EXZ15	EXZ14	EXZ13	EXZ12	EXZ11	EXZ10	EXZ9	EXZ8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	EXZ7	EXZ6	EXZ5	EXZ4	EXZ3	EXZ2	EXZ1	EXZ0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Excessive Zero Count (EXZ[15:0]) – These sixteen bits indicate the number of excessive zero conditions detected on the incoming bipolar data stream. This register is updated via the PMU signal (see Section 10.4.5).

12.7 HDLC

12.7.1 HDLC Transmit Side Register Map

The transmit side utilizes five registers.

Table 12-27. Transmit Side HDLC Register Map

Address	Register	Register Description
(0,2,4,6)A0h	HDLC.TCR	HDLC Transmit Control Register
(0,2,4,6)A2h	HDLC.TFDR	HDLC Transmit FIFO Data Register
(0,2,4,6)A4h	HDLC.TSR	HDLC Transmit Status Register
(0,2,4,6)A6h	HDLC.TSRL	HDLC Transmit Status Register Latched
(0,2,4,6)A8h	HDLC.TSRIE	HDLC Transmit Status Register Interrupt Enable
(0,2,4,6)AAh	--	Unused
(0,2,4,6)ACh	--	Unused
(0,2,4,6)AEh	--	Unused

12.7.1.1 Register Bit Descriptions

Register Name: **HDLC.TCR**
Register Description: **HDLC Transmit Control Register**
Register Address: **(0,2,4,6)A0h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	TDAL4	TDAL3	TDAL2	TDAL1	TDAL0
Default	0	0	0	0	1	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	TPSD	TFEI	TIFV	TBRE	TDIE	TFPD	TFRST
Default	0	0	0	0	0	0	0	0

Bits 12 to 8: Transmit HDLC Data Storage Available Level (TDAL[4:0]) – These five bits indicate the minimum number of bytes ([TDAL*8}+1) that must be available for storage (do not contain data) in the Transmit FIFO for HDLC data storage to be available. For example, a value of 21 (15h) results in HDLC data storage being available (THDA=1) when the Transmit FIFO has 169 (A9h) bytes or more available for storage, and HDLC data storage not being available (THDA=0) when the Transmit FIFO has 168 (A8h) bytes or less available for storage.

Bit 6: Transmit Packet Start Disable (TPSD) – When 0, the Transmit Packet Processor will continue sending packets after the current packet end. When 1, the Transmit Packet Processor will stop sending packets after the current packet end.

Bit 5: Transmit FCS Error Insertion (TFEI) – When 0, the calculated FCS (inverted CRC-16) is appended to the packet. When 1, the inverse of the calculated FCS (non-inverted CRC-16) is appended to the packet causing an FCS error. This bit is ignored if transmit FCS processing is disabled (TFPD = 1).

Bit 4: Transmit Inter-frame Fill Value (TIFV) – When 0, inter-frame fill is done with the flag sequence (7Eh). When 1, inter-frame fill is done with all ‘1’s.

Bit 3: Transmit Bit Reordering Enable (TBRE) – When 0, bit reordering is disabled (The first bit transmitted is the LSB of the Transmit FIFO Data byte TFD[0]). When 1, bit reordering is enabled (The first bit transmitted is the MSB of the Transmit FIFO Data byte TFD[7]).

Bit 2: Transmit Data Inversion Enable (TDIE) – When 0, the outgoing data is directly output from packet processing. When 1, the outgoing data is inverted before being output from packet processing.

Bit 1: Transmit FCS Processing Disable (TFPD) – This bit controls whether or not an FCS is calculated and appended to the end of each packet. When 0, the calculated FCS bytes are appended to the end of the packet. When 1, the packet is transmitted without an FCS.

Bit 0: Transmit FIFO Reset (TFRST) – When 0, the Transmit FIFO will resume normal operations, however, data is discarded until a start of packet is received after RAM power-up is completed. When 1, the Transmit FIFO is emptied, any transfer in progress is halted, the FIFO RAM is powered down, and all incoming data is discarded (all TFDR register writes are ignored).

Register Name: **HDLC.TFDR**
Register Description: **HDLC Transmit FIFO Data Register**
Register Address: **(0,2,4,6)A2h**

Bit #	15	14	13	12	11	10	9	8
Name	TFD7	TFD6	TFD5	TFD4	TFD3	TFD2	TFD1	TFD0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	--	--	TDPE
Default	0	0	0	0	0	0	0	0

Note: The FIFO data and status are loaded into the Transmit FIFO when the Transmit FIFO Data (TFD[7:0]) is written (upper byte write). When read, the value of these bits is always zero.
Bits 15 to 8: Transmit FIFO Data (TFD[7:0]) – These eight bits are the packet data to be stored in the Transmit FIFO. TFD[7] is the MSB, and TFD[0] is the LSB. If bit reordering is disabled, TFD[0] is the first bit transmitted, and TFD[7] is the last bit transmitted. If bit reordering is enabled, TFD[7] is the first bit transmitted, and TFD[0] is the last bit transmitted.

Bit 0: Transmit FIFO Data Packet End (TDPE) – When 0, the Transmit FIFO data is not a packet end. When 1, the Transmit FIFO data is a packet end.

Register Name: **HDLC.TSR**
Register Description: **HDLC Transmit Status Register**
Register Address: **(0,2,4,6)A4h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	TFFL5	TFFL4	TFFL3	TFFL2	TFFL1	TFFL0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	TFF	TFE	THDA

Bits 13 to 8: Transmit FIFO Fill Level (TFFL[5:0]) – These six bits indicate the number of eight byte groups available for storage (do not contain data) in the Transmit FIFO. E.g., a value of 21 (15h) indicates the FIFO has 168 (A8h) to 175 (AFh) bytes are available for storage.

Bit 2: Transmit FIFO Full (TFF) – When 0, the Transmit FIFO contains 255 or less bytes of data. When 1, the Transmit FIFO is full.

Bit 1: Transmit FIFO Empty (TFE) – When 0, the Transmit FIFO contains at least one byte of data. When 1, the Transmit FIFO is empty.

Bit 0: Transmit HDLC Data Storage Available (THDA) – When 0, the Transmit FIFO has less storage space available in the Transmit FIFO than the Transmit HDLC data storage available level (TDAL[4:0]). When 1, the Transmit FIFO has the same or more storage space available than the Transmit FIFO HDLC data storage available level.

Register Name: **HDLC.TSRL**
Register Description: **HDLC Transmit Status Register Latched**
Register Address: **(0,2,4,6)A6h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	TFOL	TFUL	TPEL	--	TFEL	THDAL

Bit 5: Transmit FIFO Overflow Latched (TFOL) – This bit is set when a Transmit FIFO overflow condition occurs.

Bit 4: Transmit FIFO Underflow Latched (TFUL) – This bit is set when a Transmit FIFO underflow condition occurs. An underflow condition results in a loss of data.

Bit 3: Transmit Packet End Latched (TPEL) – This bit is set when an end of packet is read from the Transmit FIFO.

Bit 1: Transmit FIFO Empty Latched (TFEL) – This bit is set when the TFE bit transitions from 0 to 1.

Note: This bit is also set when HDLC.TCR.TFRST is deasserted.

Bit 0: Transmit HDLC Data Available Latched (THDAL) – This bit is set when the THDA bit transitions from 0 to 1.

Note: This bit is also set when HDLC.TCR.TFRST is deasserted.

Register Name: **HDLC.TSRIE**
Register Description: **HDLC Transmit Status Register Interrupt Enable**
Register Address: **(0,2,4,6)A8h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	TFOIE	TFUIE	TPEIE	--	TFEIE	THDAIE
Default	0	0	0	0	0	0	0	0

Bit 5: Transmit FIFO Overflow Interrupt Enable (TFOIE) – This bit enables an interrupt if the TFOL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 4: Transmit FIFO Underflow Interrupt Enable (TFUIE) – This bit enables an interrupt if the TFUL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 3: Transmit Packet End Interrupt Enable (TPEIE) – This bit enables an interrupt if the TPEL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 2: Transmit FIFO Full Interrupt Enable (TFFIE) – This bit enables an interrupt if the TFFL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 1: Transmit FIFO Empty Interrupt Enable (TFEIE) – This bit enables an interrupt if the TFEL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Transmit HDLC Data Available Interrupt Enable (THDAIE) – This bit enables an interrupt if the THDAL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

12.7.2 HDLC Receive Side Register Map

The receive side utilizes five registers.

Table 12-28. Receive Side HDLC Register Map

Address	Register	Register Description
(0,2,4,6)B0h	HDLC.RCR	HDLC Receive Control Register
(0,2,4,6)B2h	--	Unused
(0,2,4,6)B4h	HDLC.RSR	HDLC Receive Status Register
(0,2,4,6)B6h	HDLC.RSRL	HDLC Receive Status Register Latched
(0,2,4,6)B8h	HDLC.RSRIE	HDLC Receive Status Register Interrupt Enable
(0,2,4,6)BAh	--	Unused
(0,2,4,6)BCh	HDLC.RFDR	HDLC Receive FIFO Data Register
(0,2,4,6)BEh	--	Unused

12.7.2.1 Register Bit Descriptions

Register Name: **HDLC.RCR**
Register Description: **HDLC Receive Control Register**
Register Address: **(0,2,4,6)B0h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	RDAL4	RDAL3	RDAL2	RDAL1	RDAL0
Default	0	0	0	0	1	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	RBRE	RDIE	RFPD	RFRST
Default	0	0	0	0	0	0	0	0

Bits 13 to 8: Receive HDLC Data Available Level (RDAL[4:0]) – These five bits indicate the minimum number of eight byte groups that must be stored (contain data) in the Receive FIFO before HDLC data is considered to be available (RHDA=1). For example, a value of 21 (15h) results in HDLC data being available when the Receive FIFO contains 168 (A8h) bytes or more.

Bit 3: Receive Bit Reordering Enable (RBRE) – When 0, bit reordering is disabled (The first bit received is in the LSB of the Receive FIFO Data byte RFD[0]). When 1, bit reordering is enabled (The first bit received is in the MSB of the Receive FIFO Data byte RFD[7]).

Bit 2: Receive Data Inversion Enable (RDIE) – When 0, the incoming data is directly passed on for packet processing. When 1, the incoming data is inverted before being passed on for packet processing.

Bit 1: Receive FCS Processing Disable (RFPD) – When 0, FCS processing is performed (the packets have an FCS appended). When 1, FCS processing is disabled (the packets do not have an FCS appended).

Bit 0: Receive FIFO Reset (RFRST) – When 0, the Receive FIFO will resume normal operations, however, data is discarded until a start of packet is received after RAM power-up is completed. When 1, the Receive FIFO is emptied, any transfer in progress is halted, the FIFO RAM is powered down, the RHDA bit is forced low, and all incoming data is discarded.

Register Name: **HDLC.RSR**
Register Description: **HDLC Receive Status Register**
Register Address: **(0,2,4,6)B4h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	RFF	RFE	RHDA

Bit 2: Receive FIFO Full (RFF) – When 0, the Receive FIFO contains 255 or less bytes of data. When 1, the Receive FIFO is full.

Bit 1: Receive FIFO Empty (RFE) – When 0, the Receive FIFO contains at least one byte of data. When 1, the Receive FIFO is empty.

Bit 0: Receive HDLC Data Available (RHDA) – When 0, the Receive FIFO contains less data than the Receive HDLC data available level (RDAL[4:0]). When 1, the Receive FIFO contains the same or more data than the Receive HDLC data available level.

Register Name: **HDLC.RSRL**
Register Description: **HDLC Receive Status Register Latched**
Register Address: **(0,2,4,6)B6h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	RFOL	--	--	RPEL	RPSL	RFFL	--	RHDAL

Bit 7: Receive FIFO Overflow Latched (RFOL) – This bit is set when a Receive FIFO overflow condition occurs. An overflow condition results in a loss of data.

Bit 4: Receive Packet End Latched (RPEL) – This bit is set when an end of packet is stored in the Receive FIFO.

Bit 3: Receive Packet Start Latched (RPSL) – This bit is set when a start of packet is stored in the Receive FIFO.

Bit 2: Receive FIFO Full Latched (RFFL) – This bit is set when the RFF bit transitions from 0 to 1.

Bit 0: Receive HDLC Data Available Latched (RHDAL) – This bit is set when the RHDA bit transitions from 0 to 1.

Register Name: **HDLC.RSRIE**
Register Description: **HDLC Receive Status Register Interrupt Enable**
Register Address: **(0,2,4,6)B8h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RFOIE	--	--	RPEIE	RPSIE	RFFIE	--	RHDAIE
Default	0	0	0	0	0	0	0	0

Bit 7: Receive FIFO Overflow Interrupt Enable (RFOIE) – This bit enables an interrupt if the RFOL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 4: Receive Packet End Interrupt Enable (RPEIE) – This bit enables an interrupt if the RPEL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 3: Receive Packet Start Interrupt Enable (RPSIE) – This bit enables an interrupt if the RPSL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 2: Receive FIFO Full Interrupt Enable (RFFIE) – This bit enables an interrupt if the RFFL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Receive HDLC Data Available Interrupt Enable (RHDAIE) – This bit enables an interrupt if the RHDAL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **HDLC.RFDR**
Register Description: **HDLC Receive FIFO Data Register**
Register Address: **(0,2,4,6)BCh**

Bit #	15	14	13	12	11	10	9	8
Name	RFD7	RFD6	RFD5	RFD4	RFD3	RFD2	RFD1	RFD0
Default	X	X	X	X	X	X	X	X

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	RPS2	RPS1	RPS0	RFDV
Default	0	0	0	0	X	X	X	0

Note: The FIFO data and status are updated when the Receive FIFO Data (RFD[7:0]) is read (upper byte read). When this register is read eight bits at a time, a read of the lower byte will reflect the status of the next read of the upper byte, and reading the upper byte when RFDV=0 may result in a loss of data.

Bits 15 to 8: Receive FIFO Data (RFD[7:0]) – These eight bits are the packet data stored in the Receive FIFO. RFD[7] is the MSB, and RFD[0] is the LSB. If bit reordering is disabled, RFD[0] is the first bit received, and RFD[7] is the last bit received. If bit reordering is enabled, RFD[7] is the first bit received, and RFD[0] is the last bit received.

Bits 3 to 1: Receive Packet Status (RPS[2:0]) – These three bits indicate the status of the received packet and packet data.

000 = packet middle
001 = packet start.
010 = reserved
011 = reserved
100 = packet end: good packet
101 = packet end: FCS errored packet.
110 = packet end: invalid packet (a non-integer number of bytes).
111 = packet end: aborted packet.

Bit 0: Receive FIFO Data Valid (RFDV) – When 0, the Receive FIFO data (RFD[7:0]) is invalid (the Receive FIFO is empty). When 1, the Receive FIFO data (RFD[7:0]) is valid.

12.8 FEAC Controller

12.8.1 FEAC Transmit Side Register Map

The transmit side utilizes five registers.

Table 12-29. FEAC Transmit Side Register Map

Address	Register	Register Description
(0,2,4,6)C0h	FEAC.TCR	FEAC Transmit Control Register
(0,2,4,6)C2h	FEAC.TFDR	FEAC Transmit Data Register
(0,2,4,6)C4h	FEAC.TSR	FEAC Transmit Status Register
(0,2,4,6)C6h	FEAC.TSRL	FEAC Transmit Status Register Latched
(0,2,4,6)C8h	FEAC.TSRIE	FEAC Transmit Status Register Interrupt Enable
(0,2,4,6)CAh	--	Unused
(0,2,4,6)CCh	--	Unused
(0,2,4,6)CEh	--	Unused

12.8.1.1 Register Bit Descriptions

Register Name: **FEAC.TCR**
Register Description: **FEAC Transmit Control Register**
Register Address: **(0,2,4,6)C0h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	1	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	TFCL	TFS1	TFS0
Default	0	0	0	0	0	0	0	0

Bit 2: Transmit FEAC Codeword Load (TFCL) – A 0 to 1 transition on this bit loads the transmit FEAC processor mode select bits (TFS[1:0]), and transmit FEAC codes (TFCA[5:0] and TFCB[5:0]). Note: Whenever a FEAC codeword is loaded, any current FEAC codeword transmission in progress will be immediately halted, and the new FEAC codeword transmission will be started based on the new values for TFS[1:0], TFCA[5:0], and TFCB[5:0]..

Bits 1 to 0: Transmit FEAC Codeword Select (TFS[1:0]) – These two bits control the transmit FEAC processor mode. The TFCL bit loads the mode set by this bit.

00 = Idle (all ones)
01 = single code (send code TFCA ten times and send all ones)
10 = dual code (send code TFCA ten times, send code TFCB ten times, and send all ones)
11 = continuous code (send code TFCA continuously)

Register Name: **FEAC.TFDR**
Register Description: **Transmit FEAC Data Register**
Register Address: **(0,2,4,6)C2h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	TFCB5	TFCB4	TFCB3	TFCB2	TFCB1	TFCB0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	TFCA5	TFCA4	TFCA3	TFCA2	TFCA1	TFCA0
Default	0	0	0	0	0	0	0	0

Bits 13 to 8: Transmit FEAC Code B (TFCB[5:0]) – These six bits are the transmit FEAC code B data to be stored inserted into codeword B. TFCB[5] is the LSB (last bit transmitted) of the FEAC code (C[6]), and TFCB[0] is the MSB (first bit transmitted) of the FEAC code (C[1]).

Bits 5 to 0: Transmit FEAC Code A (TFCA[5:0]) – These six bits are the transmit FEAC code A data to be stored inserted into codeword A. TFCA[5] is the LSB (last bit transmitted) of the FEAC code (C[6]), and TFCA[0] is the MSB (first bit transmitted) of the FEAC code (C[1]).

Register Name: **FEAC.TSR**
Register Description: **FEAC Transmit Status Register**
Register Address: **(0,2,4,6)C4h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	--	--	TFI

Bit 0: Transmit FEAC Idle (TFI) – When 0, the Transmit FEAC processor is sending a FEAC codeword. When 1, the Transmit FEAC processor is sending an Idle signal (all ones).

Register Name: **FEAC.TSRL**
Register Description: **FEAC Transmit Status Register Latched**
Register Address: **(0,2,4,6)C6h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	--	--	TFIL

Bit 0: Transmit FEAC Idle Latched (TFIL) – This bit is set when the TFI bit transitions from 0 to 1. Note: Immediately after a reset, this bit will be set to one.

Register Name: **FEAC.TSRIE**
Register Description: **FEAC Transmit Status Register Interrupt Enable**
Register Address: **(0,2,4,6)C8h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	--	--	TFIIE
Default	0	0	0	0	0	0	0	0

Bit 0: Transmit FEAC Idle Interrupt Enable (TFIIE) – This bit enables an interrupt if the TFIL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

12.8.2 FEAC Receive Side Register Map

The receive side utilizes five registers.

Table 12-30. FEAC Receive Side Register Map

Address	Register	Register Description
(0,2,4,6)D0h	FEAC.RCR	FEAC Receive Control Register
(0,2,4,6)D2h	--	Unused
(0,2,4,6)D4h	FEAC.RSR	FEAC Receive Status Register
(0,2,4,6)D6h	FEAC.RSRL	FEAC Receive Status Register Latched
(0,2,4,6)D8h	FEAC.RSRIE	FEAC Receive Status Register Interrupt Enable
(0,2,4,6)DAh	--	Unused
(0,2,4,6)DCh	FEAC.RFDR	FEAC Receive FIFO Data Register
(0,2,4,6)DEh	--	Unused

12.8.2.1 Register Bit Descriptions

Register Name: **FEAC.RCR**
Register Description: **FEAC Receive Control Register**
Register Address: **(0,2,4,6)D0h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	1	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	--	--	RFR
Default	0	0	0	0	0	0	0	0

Bit 0: Receive FEAC Reset (RFR) –When 0, the Receive FEAC Processor and Receive FEAC FIFO will resume normal operations. When 1, the Receive FEAC controller is reset. The FEAC FIFO is emptied, any transfer in progress is halted, and all incoming data is discarded.

Register Name: **FEAC.RSR**
Register Description: **FEAC Receive Status Register**
Register Address: **(0,2,4,6)D4h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	RFFE	--	RFCD	RFI

Bit 3: Receive FEAC FIFO Empty (RFFE) – When 0, the Receive FIFO contains at least one code. When 1, the Receive FIFO is empty.

Bit 1: Receive FEAC Codeword Detect (RFCD) – When 0, the Receive FEAC Processor is not currently receiving a FEAC codeword. When 1, the Receive FEAC Processor is currently receiving a FEAC codeword.

Bit 0: Receive FEAC Idle (RFI) – When 0, the Receive FEAC processor is not receiving a FEAC Idle signal (all ones). When 1, the Receive FEAC processor is receiving a FEAC Idle signal.

Register Name: **FEAC.RSRL**
Register Description: **FEAC Receive Status Register Latched**
Register Address: **(0,2,4,6)D6h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	RFFOL	RFCDL	RFIL

Bit 2: Receive FEAC FIFO Overflow Latched (RFFOL) – This bit is set when a Receive FIFO overflow condition occurs. An overflow condition results in a loss of data.

Bit 1: Receive FEAC Codeword Detect Latched (RFCDL) – This bit is set when the RFCD bit transitions from 0 to 1.

Bit 0: Receive FEAC Idle Latched (RFIL) – This bit is set when the RFI bit transitions from 0 to 1. Note: Immediately after a reset, this bit will be set to one.

Register Name: **FEAC.RSRIE**
Register Description: **FEAC Receive Status Register Interrupt Enable**
Register Address: **(0,2,4,6)D8h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	RFFOIE	RFCDIE	RFIIE
Default	0	0	0	0	0	0	0	0

Bit 2: Receive FEAC FIFO Overflow Interrupt Enable (RFFOIE) – This bit enables an interrupt if the RFFOL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 1: Receive FEAC Codeword Detect Interrupt Enable (RFCDIE) – This bit enables an interrupt if the RFCDL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Receive FEAC Idle Interrupt Enable (RFIIE) – This bit enables an interrupt if the RFIL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **FEAC.RFDR**
Register Description: **FEAC Receive FIFO Data Register**
Register Address: **(0,2,4,6)DCh**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RFFI	--	RFF5	RFF4	RFF3	RFF2	RFF1	RFF0
Default	0	0	0	0	0	0	0	0

Bit 7: Receive FEAC FIFO Data Invalid (RFFI) – When 0, the Receive FIFO data (RFF[5:0]) is valid. When 1, the Receive FIFO data is invalid (Receive FIFO is empty).

Bits 5 to 0: Receive FEAC FIFO Data (RFF[5:0]) – These six bits are the FEAC code data stored in the Receive FIFO. RFF[5] is the LSB (last bit received) of the FEAC code (C[6]), and RFF[0] is the MSB (first bit received) of the FEAC code (C[1]). The Receive FEAC FIFO data (RFF[5:0]) is updated when it is read (lower byte read).

12.9 Trail Trace

12.9.1 Trail Trace Transmit Side

The transmit side utilizes three registers. Register Map

Table 12-31. Transmit Side Trail Trace Register Map

Address	Register	Register Description
(0,2,4,6)E8h	TT.TCR	Trail Trace Transmit Control Register
(0,2,4,6)EAh	TT.TTIAR	Trail Trace Transmit Identifier Address Register
(0,2,4,6)ECh	TT.TIR	Trail Trace Transmit Identifier Register
(0,2,4,6)EEh	--	Unused

12.9.1.1 Register Bit Descriptions

Register Name: **TT.TCR**
Register Description: **Trail Trace Transmit Control Register**
Register Address: **(0,2,4,6)E8h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	Reserved	TMAD	TIDLE	TDIE	TBRE
Default	0	0	0	0	0	0	0	0

Bit 3: Transmit Multiframe Alignment Insertion Disable (TMAD) – When 0, multiframe alignment signal (MAS) insertion is enabled, and the first bit transmitted of each trail trace byte is overwritten with an MAS bit. When 1, MAS insertion is disabled, and the trail trace bytes from the Transmit Data Storage are output without being modified.

Bit 2: Transmit Trail Trace Identifier Idle (TIDLE) – When 0, the programmed transmit trail trace identifier will be transmitted. When 1, all zeros will be transmitted.

Bit 1: Transmit Data Inversion Enable (TDIE) – When 0, the outgoing data from trail trace processing is output directly. When 1, the outgoing data from trail trace processing is inverted before being output.

Bit 0: Transmit Bit Reordering Enable (TBRE) – When 0, bit reordering is disabled (The first bit transmitted is the MSB *TT.TIR*.TTD[7] of the byte). When 1, bit reordering is enabled (The first bit transmitted is the LSB *TT.TIR*.TTD[0] of the byte).

Register Name: **TT.TTIAR**
Register Description: **Trail Trace Transmit Identifier Address Register**
Register Address: **(0,2,4,6)EAh**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	Reserved	Reserved	TTIA3	TTIA2	TTIA1	TTIA0
Default	0	0	0	0	0	0	0	0

Bits 3 to 0: Transmit Trail Trace Identifier Address (TTIA[3:0]) – These four bits indicate the transmit trail trace identifier byte to be read/written by the next memory access. Address 0h indicates the first byte of the transmit trail trace identifier. Note: The value of these bits increments with each transmit trail trace identifier memory access (when these bits are Fh, a memory access will return them to 0h).

Register Name: **TT.TIR**
Register Description: **Trail Trace Transmit Identifier Register**
Register Address: **(0,2,4,6)ECh**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	TTD7	TTD6	TTD5	TTD4	TTD3	TTD2	TTD1	TTD0
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Transmit Trail Trace Identifier Data (TTD[7:0]) – These eight bits are the transmit trail trace identifier data. The transmit trail trace identifier address will be incremented whenever these bits are read or written (when address location Fh is read or written, the address will return to 0h).

12.9.2 Trail Trace Receive Side Register Map

The receive side utilizes seven registers.

Table 12-32. Trail Trace Receive Side Register Map

Address	Register	Register Description
(0,2,4,6)F0h	TT.RCR	Trail Trace Receive Control Register
(0,2,4,6)F2h	TT.RIAR	Trail Trace Receive Identifier Address Register
(0,2,4,6)F4h	TT.RSR	Trail Trace Receive Status Register
(0,2,4,6)F6h	TT.RSRL	Trail Trace Receive Status Register Latched
(0,2,4,6)F8h	TT.RSRIE	Trail Trace Receive Status Register Interrupt Enable
(0,2,4,6)FAh	--	Unused
(0,2,4,6)FCh	TT.RIR	Trail Trace Receive Identifier Register
(0,2,4,6)FEh	TT.EIR	Trail Trace Expected Identifier Register

12.9.2.1 Register Bit Descriptions

Register Name: **TT.RCR**
Register Description: **Trail Trace Receive Control Register**
Register Address: **(0,2,4,6)F0h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	Reserved	Reserved	RMAD	RETCE	RDIE	RBRE
Default	0	0	0	0	0	0	0	0

Bit 3: Receive Multiframe Alignment Disable (RMAD) – When 0, multiframe alignment is performed. When 1, multiframe alignment is disabled and the trail trace bytes are stored starting with a random byte.

Bit 2: Receive Expected Trail Trace Comparison Enable (RETCE) – When 0, expected trail trace comparison is disabled. When 1, expected trail trace comparison is performed. Note: When the RMAD bit is one, expected trail trace comparison is disabled regardless of the setting of this bit.

Bit 1: Receive Data Inversion Enable (RDIE) – When 0, the incoming data is directly passed on for trail trace processing. When 1, the incoming data is inverted before being passed on for trail trace processing.

Bit 0: Receive Bit Reordering Enable (RBRE) – When 0, bit reordering is disabled (The first bit received is the MSB *TT.RIR*.RTD[7] of the byte). When 1, bit reordering is enabled (The first bit received is the LSB *TT.RIR*.RTD[0] of the byte).

Register Name: **TT.RTIAR**
Register Description: **Trail Trace Receive Identifier Address Register**
Register Address: **(0,2,4,6)F2h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	Reserved	Reserved	ETIA3	ETIA2	ETIA1	ETIA0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	Reserved	Reserved	RTIA3	RTIA2	RTIA1	RTIA0
Default	0	0	0	0	0	0	0	0

Bits 11 to 8: Expected Trail Trace Identifier Address (ETIA[3:0]) – These four bits indicate the expected trail trace identifier byte to be read/written by the next memory access. Address 0h indicates the first byte of the expected trail trace identifier. Note: The value of these bits increments with each expected trail trace identifier memory access (when these bits are Fh, a memory access will return them to 0h).

Bits 3 to 0: Receive Trail Trace Identifier Address (RTIA[3:0]) – These four bits indicate the receive trail trace identifier byte to be read by the next memory access. Address 0h indicates the first byte of the receive trail trace identifier. Note: The value of these bits increments with each receive trail trace identifier memory access (when these bits are Fh, a memory access will return them to 0h).

Register Name: **TT.RSR**
Register Description: **Trail Trace Receive Status Register**
Register Address: **(0,2,4,6)F4h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	RTIM	RTIU	RIDL

Bit 2: Receive Trail Trace Identifier Mismatch (RTIM)

0 = Received and expected trail trace identifiers match.
1 = Received and expected trail trace identifiers do not match; trail trace identifier mismatch (TIM) declared.

Bit 1: Receive Trail Trace Identifier Unstable (RTIU)

0 = Received trail trace identifier is not unstable
1 = Received trail trace identifier is in an unstable condition (TIU); TIU is declared when eight consecutive trail trace identifiers are received that do not match either the receive trail trace identifier or the previously stored current trail trace identifier.

Bit 0: Receive Trail Trace Identifier Idle (RIDL)

0 = Received trail trace identifier is not in idle condition.
1 = Received trail trace identifier is in idle condition. Idle condition is declared upon the reception of an all zeros trail trace identifier five consecutive times.

Register Name: **TT.RSRL**
Register Description: **Trail Trace Receive Status Register Latched**
Register Address: **(0,2,4,6)F6h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	RTICL	RTIML	RTIUL	RIDLL

Bit 3: Receive Trail Trace Identifier Change Latched (RTICL) – This bit is set when the receive trail trace identifier is updated.

Bit 2: Receive Trail Trace Identifier Mismatch Latched (RTIML) – This bit is set when the *TT.RSR*.RTIM bit transitions from 0 to 1.

Bit 1: Receive Trail Trace Identifier Unstable Latched (RTIUL) – This bit is set when the *TT.RSR*.RTIU bit transitions from 0 to 1.

Bit 0: Receive Trail Trace Identifier Idle Latched (RIDLL) – This bit is set when the *TT.RSR*.RIDL bit transitions from 0 to 1.

Register Name: **TT.RSRIE**
Register Description: **Trail Trace Receive Status Register Interrupt Enable**
Register Address: **(0,2,4,6)F8h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	RTICIE	RTIMIE	RTIUIE	RIDLIE
Default	0	0	0	0	0	0	0	0

Bit 3: Receive Trail Trace Identifier Change Interrupt Enable (RTICIE) – This bit enables an interrupt if the *TT.RSRL*.RTICL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 2: Receive Trail Trace Identifier Mismatch Interrupt Enable (RTIMIE) – This bit enables an interrupt if the *TT.RSRL*.RTIML bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 1: Receive Trail Trace Identifier Unstable Interrupt Enable (RTIUIE) – This bit enables an interrupt if the *TT.RSRL*.RTIUL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Receive Trail Trace Identifier Idle Interrupt Enable (RIDLIE) – This bit enables an interrupt if the *TT.RSRL*.RIDLL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **TT.RIR**
Register Description: **Trail Trace Receive Identifier Register**
Register Address: **(0,2,4,6)FCh**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RTD7	RTD6	RTD5	RTD4	RTD3	RTD2	RTD1	RTD0
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive Trail Trace Identifier Data (RTD[7:0]) – These eight bits are the receive trail trace identifier data. The receive trail trace identifier address will be incremented whenever these bits are read (when byte Fh is read, the address will return to 0h).

Register Name: **TT.EIR**
Register Description: **Trail Trace Expected Identifier Register**
Register Address: **(0,2,4,6)FEh**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	ETD7	ETD6	ETD5	ETD4	ETD3	ETD2	ETD1	ETD0
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Expected Trail Trace Identifier Data (ETD[7:0]) – These eight bits are the expected trail trace identifier data. The expected trail trace identifier address will be incremented whenever these bits are read or written (when byte Fh is read or written, the address will return to 0h).

12.10 DS3/E3 Framer

12.10.1 Transmit DS3

The transmit DS3 utilizes two registers.

Table 12-33. Transmit DS3 Framer Register Map

Address	Register	Register Description
(1,3,5,7)18h	T3.TCR	T3 Transmit Control Register
(1,3,5,7)1Ah	T3.TEIR	T3 Transmit Error Insertion Register
(1,3,5,7)1Ch	--	Reserved
(1,3,5,7)1Eh	--	Reserved

12.10.1.1 Register Bit Descriptions

Register Name: **T3.TCR**
Register Description: **T3 Transmit Control Register**
Register Address: **(1,3,5,7)18h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	PBGE	TIDLE	CBGD	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	TFEBE	AFEBED	TRDI	ARDID	TFGC	TAIS
Default	0	0	0	0	0	0	0	0

Bit 12: P-bit Generation Enable (PBGE) – When 0, Transmit Frame Processor P-bit generation is disabled. If transmit frame generation is also disabled, the P-bit overhead periods in the incoming DS3 signal will be passed through to overhead insertion. When 1, Transmit Frame Processor P-bit generation is enabled. The P-bit overhead periods in the incoming DS3 signal will be overwritten even if transmit frame generation is disabled

Bit 11: Transmit DS3 Idle Signal (TIDLE) –

0 = Transmit DS3 Idle signal is not inserted
1 = Transmit DS3 Idle signal is inserted into the DS3 frame.

Bit 10: C-bit Generation Disable (CBGD) (M23 mode only) – When 0, Transmit Frame Processor C-bit generation is enabled. The C-bit overhead periods in the incoming M23 DS3 signal will be overwritten with zeros. When 1, Transmit Frame Processor C-bit generation is disabled. The C-bit overhead periods in the incoming M23 DS3 signal will be treated as payload, and passed through to overhead insertion. This bit is ignored in C-bit DS3 mode.

Note: If CBGD = 1, PORT.CR1.NAD must also be set to 1.

Bit 5: Transmit FEBE Error (TFEBE) – When automatic far-end block error generation is defeated (AFEBED = 1), the inverse of this bit is inserted into the bits C_{41}, C_{42}, and C_{43}. Note: a far-end block error value of zero (TFEBE=1) indicates a far-end block error. This bit is ignored in M23 DS3 mode.

Bit 4: Automatic FEBE Defeat (AFEBED) – When 0, a far-end block error is automatically generated based upon the receive C-bit parity errors or framing errors. When 1, a far-end block error is inserted from the register bit TFEBE. This bit is ignored in M23 DS3 mode.

Bit 3: Transmit RDI Alarm (TRDI) – When automatic RDI generation is defeated (ARDID = 1), the inverse of this bit is inserted into the X-bits (X_1 and X_2). Note: an RDI value of zero (TRDI=1) indicates an alarm.

Bit 2: Automatic RDI Defeat (ARDID) – When 0, the RDI is automatically generated based received DS3 alarms. When 1, the RDI is inserted from the register bit TRDI.

Bit 1: Transmit Frame Generation Control (TFGC) – When this bit is zero, the Transmit Frame Processor frame generation is enabled. The DS3 overhead positions in the incoming DS3 payload will be overwritten with the internally generated DS3 overhead. When this bit is one, the Transmit Frame Processor frame generation is disabled. The DS3 overhead positions in the incoming DS3 payload will be passed through to error insertion. Note: Frame generation will still overwrite the P-bits if PBGE = 1. Also, the DS3 overhead periods can still be overwritten by overhead insertion.

Bit 0: Transmit Alarm Indication Signal (TAIS) –

0 = Transmit Alarm Indication Signal is not inserted
1 = Transmit Alarm Indication Signal is inserted into data stream payload

Register Name: **T3.TEIR**
Register Description: **T3 Transmit Error Insertion Register**
Register Address: **(1,3,5,7)1Ah**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	CCPEIE	CPEI	CFBEIE	FBEI
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	Reserved	CPEIE	PEI	FEIC1	FEIC0	FEI	TSEI	MEIMS
Default	0	0	0	0	0	0	0	0

Bit 11: Continuous C-bit Parity Error Insertion Enable (CCPEIE) – When 0, single C-bit parity error insertion is enabled. When 1, continuous C-bit parity error insertion is enabled, and C-bit parity errors will be transmitted continuously if CPEI is high.

Bit 10: C-bit Parity Error Insertion Enable (CPEI) – When 0, C-bit parity error insertion is disabled. When 1, C-bit parity error insertion is enabled.

Bit 9: Continuous Far-End Block Error Insertion Enable (CFBEIE) – When 0, single far-end block error insertion is enabled. When 1, continuous far-end block error insertion is enabled, and far-end block errors will be transmitted continuously if FBEI is high.

Bit 8: Far-End Block Error Insertion Enable (FBEI) – When 0, far-end block error insertion is disabled. When 1, far-end block error insertion is enabled.

Bit 6: Continuous P-bit Parity Error Insertion Enable (CPEIE) – When 0, single P-bit parity error insertion is enabled. When 1, continuous P-bit parity error insertion is enabled, and P-bit parity errors will be transmitted continuously if PEI is high.

Bit 5: P-bit Parity Error Insertion Enable (PEI) – When 0, P-bit parity error insertion is disabled. When 1, P-bit parity error insertion is enabled.

Bits 4 to 3: Framing Error Insertion Control (FEIC[1:0]) – These two bits control the framing error event to be inserted.

00 = F-bit error.
01 = M-bit error.
10 = SEF error.
11 = OOMF error.

Bit 2: Framing Error Insertion Enable (FEI) – When 0, framing error insertion is disabled. When 1, framing error insertion is enabled.

Bit 1: Transmit Single Error Insert (TSEI) – This bit causes an error of the enabled type(s) to be inserted in the transmit data stream if manual error insertion is disabled (MEIMS = 0). A 0 to 1 transition causes a single error to be inserted. For a second error to be inserted, this bit must be set to 0, and back to 1. Note: If MEIMS is low, and this bit transitions more than once between error insertion opportunities, only one error will be inserted.

Bit 0: Manual Error Insert Mode Select (MEIMS) – When 0, error insertion is initiated by the TSEI register bit. When 1, error insertion is initiated by the transmit manual error insertion signal (TMEI). Note: If TMEI or TSEI is one, changing the state of this bit may cause an error to be inserted.

12.10.2 Receive DS3 Register Map

The receive DS3 utilizes eleven registers. Two registers are shared for C-Bit and M23 DS3 modes. The M23 DS3 mode does not use the RFEBER or RCPECR count registers.

Table 12-34. Receive DS3 Framer Register Map

Address	Register	Register Description
(1,3,5,7)20h	T3.RCR	T3 Receive Control Register
(1,3,5,7)22h	--	Reserved
(1,3,5,7)24h	T3.RSR1	T3 Receive Status Register #1
(1,3,5,7)26h	T3.RSR2	T3 Receive Status Register #2
(1,3,5,7)28h	T3.RSRL1	T3 Receive Status Register Latched #1
(1,3,5,7)2Ah	T3.RSRL2	T3 Receive Status Register Latched #2
(1,3,5,7)2Ch	T3.RSRIE1	T3 Receive Status Register Interrupt Enable #1
(1,3,5,7)2Eh	T3.RSRIE2	T3 Receive Status Register Interrupt Enable #2
(1,3,5,7)30h	--	Reserved
(1,3,5,7)32h	--	Reserved
(1,3,5,7)34h	T3.RFECR	T3 Receive Framing Error Count Register
(1,3,5,7)36h	T3.RPECR	T3 Receive P-bit Parity Error Count Register
(1,3,5,7)38h	T3.RFBECR	T3 Receive Far-End Block Error Count Register
(1,3,5,7)3Ah	T3.RCPECR	T3 Receive C-bit Parity Error Count Register
(1,3,5,7)3Ch	--	Unused
(1,3,5,7)3Eh	--	Unused

12.10.2.1 Register Bit Descriptions

Register Name: **T3.RCR**
Register Description: **T3 Receive Control Register**
Register Address: **(1,3,5,7)20h**

Bit #	15	14	13	12	11	10	9	8
Name	Reserved	COVHD	MAOD	MDAISI	AAISD	ECC	FECC1	FECC0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RAILE	RAILD	RAIOD	RAIAD	ROMD	LIP1	LIP0	FRSYNC
Default	0	0	0	0	0	0	0	0

Bit 14: C-bit Overhead Masking Disable (COVHD) – When 0, the C-bit positions will be marked as overhead (RDENn=0). When 1, the C-bit positions will be marked as data (RDENn=1). This bit is ignored in C-bit DS3 mode or when the ROMD bit is set to one.

Bit 13: Multiframe Alignment OOF Disable (MAOD) – When 0, an OOF condition is declared whenever an OOMF or SEF condition is declared. When 1, an OOF condition is declared only when an SEF condition is declared.

Bit 12: Manual Downstream AIS Insertion (MDAISI) – When 0, manual downstream AIS insertion is disabled. When 1, manual downstream AIS insertion is enabled.

Bit 11: Automatic Downstream AIS Disable (AAISD) – When 0, the presence of an LOS, OOF, or AIS condition will cause downstream AIS to be inserted. When 1, the presence of an LOS, OOF, or AIS condition will not cause downstream AIS to be inserted.

Bit 10: Error Count Control (ECC) – When 0, framing errors, P-bit parity errors, C-bit parity errors, and far-end block errors will not be counted if an OOF or AIS condition is present. P-bit parity errors, C-bit parity errors, and far-end block errors will also not be counted during the DS3 frame in which an OOF condition is terminated, and the next DS3 frame. When 1, framing errors, P-bit parity errors, C-bit parity errors, and far-end block errors will be counted regardless of the presence of an OOF or AIS condition.

Bits 9 to 8: Framing Error Count Control (FECC[1:0]) – These two bits control the type of framing error events that are counted.

00 = count OOF occurrences (counted regardless of the setting of the ECC bit).
01 = count M bit and F bit errors.
10 = count only F bit errors.
11 = count only M bit errors.

Bit 7: Receive Alarm Indication on LOF Enable (RAILE) – When 0, an LOF condition does not affect the receive alarm indication signal (RAI). When 1, an LOF condition will cause the transmit DS3 X-bits to be set to zero if transmit automatic RDI is enabled.

Bit 6: Receive Alarm Indication on LOS Disable (RAILD) – When 0, an LOS condition will cause the transmit DS3 X-bits to be set to zero if transmit automatic RDI is enabled. When 1, an LOS condition does not affect the RAI signal.

Bit 5: Receive Alarm Indication on SEF Disable (RAIOD) – When 0, an SEF condition will cause the transmit DS3 X-bits to be set to zero if transmit automatic RDI is enabled. When 1, an SEF condition does not affect the RAI signal.

Bit 4: Receive Alarm Indication on AIS Disable (RAIAD) – When 0, an AIS condition will cause the transmit DS3 X-bits to be set to zero if transmit automatic RDI is enabled. When 1, an AIS condition does not affect the RAI signal.

Bit 3: Receive Overhead Masking Disable (ROMD) – When 0, the DS3 overhead positions in the outgoing DS3 payload will be marked as overhead by RDENn. When 1, the DS3 overhead positions in the outgoing DS3 payload will be marked as payload data by RDENn. When this bit is set to one, the COVHD bit is ignored.

Bits 2 to 1: LOF Integration Period (LIP[1:0]) – These two bits determine the OOF integration period for declaring LOF.

00 = OOF is integrated for 3 ms before declaring LOF
01 = OOF is integrated for 2 ms before declaring LOF
10 = OOF is integrated for 1 ms before declaring LOF.
11 = LOF is declared at the same time as OOF.

Bit 0: Force Framer Resynchronization (FRSYNC) – A 0 to 1 transition forces an OOF, SEF, and OOMF condition. The bit must be cleared and set to one again to force another resynchronization

Register Name: **T3.RSR1**
Register Description: **T3 Receive Status Register #1**
Register Address: **(1,3,5,7)24h**

Bit #	15	14	13	12	11	10	9	8
Name	Reserved	Reserved	--	Reserved	T3FM	AIC	IDLE	RUA1

Bit #	7	6	5	4	3	2	1	0
Name	OOMF	SEF	--	LOF	RDI	AIS	OOF	LOS

Bit 11: T3 Framing Format Mismatch (T3FM) – This bit indicates the DS3 framer is programmed for a framing format (C-bit or M23) that is different than the format indicated by the incoming DS3 signal.

Bit 10: Application Identification Channel (AIC) – This bit indicates the current state of the Application Identification Channel (AIC) from the C_{11} bit. AIC = 1 is C-bit mode, AIC = 0 is M23 mode.

Bit 9: DS3 Idle Signal (IDLE) – When 0, the receive frame processor is not in a **DS3** idle signal (Idle) condition. When 1, the receive frame processor is in an Idle condition.

Bit 8: Receive Unframed All 1's (RUA1) – When 0, the receive frame processor is not in a receive unframed all 1's (RUA1) condition. When 1, the receive frame processor is in an RUA1 condition.

Bit 7: Out Of MultiFrame (OOMF) – When 0, the receive frame processor is not in an out of multiframe (OOMF) condition. When 1, the receive frame processor is in an OOMF condition.

Bit 6: Severely Errored Frame (SEF) – When 0, the receive frame processor is not in a severely errored frame (SEF) condition. When 1, the receive frame processor is in an SEF condition.

Bit 4: Loss Of Frame (LOF) – When 0, the receive framer is not in a loss of frame (LOF) condition. When 1, the receive frame processor is in an LOF condition.

Bit 3: Remote Defect Indication (RDI) – This bit indicates the current state of the remote defect indication (RDI)
Bit 2: Alarm Indication Signal (AIS) – When 0, the receive frame processor is not in an alarm indication signal (AIS) condition. When 1, the receive frame processor is in an AIS condition.

Bit 1: Out Of Frame (OOF) – When 0, the receive framer is not in an out of frame (OOF) condition. When 1, the receive frame processor is in an OOF condition.

Bit 0: Loss Of Signal (LOS) – When 0, the receive framer is not in a loss of signal (LOS) condition. When 1, the receive framer is in an LOS condition.

Register Name: **T3.RSR2**
Register Description: **T3 Receive Status Register #2**
Register Address: **(1,3,5,7)26h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	CPEC	FBEC	PEC	FEC

Bit 3: C-bit Parity Error Count (CPEC) – When 0, the C-bit parity error count is zero. When 1, the C-bit parity error count is one or more. This bit is set to zero in M23 DS3 mode.

Bit 2: Remote Error Indication Count (FBEC) – When 0, the remote error indication count is zero. When 1, the remote error indication count is one or more. This bit is set to zero in M23 DS3 mode.

Bit 1: P-bit Parity Error Count (PEC) – When 0, the P-bit parity error count is zero. When 1, the P-bit parity error count is one or more.

Bit 0: Framing Error Count (FEC) – When 0, the framing error count is zero. When 1, the framing error count is one or more. The type of framing error event counted is determined by T3.RCR.FECC[1:0]

Register Name: **T3.RSRL1**
Register Description: **T3 Receive Status Register Latched #1**
Register Address: **(1,3,5,7)28h**

Bit #	15	14	13	12	11	10	9	8
Name	Reserved	Reserved	Reserved	Reserved	T3FML	AICL	IDLEL	RUA1L

Bit #	7	6	5	4	3	2	1	0
Name	OOMFL	SEFL	COFAL	LOFL	RAIL	AISL	OOFL	LOSL

Bit 11: T3 Framing Format Mismatch Latched (T3FML) – This bit is set when the T3FM bit transitions from zero to one.

Bit 10: Application Identification Channel Change Latched (AICL) – This bit is set when the AIC bit changes state.

Bit 9: DS3 Idle Signal Change Latched (IDLEL) – This bit is set when the IDLE bit changes state.

Bit 8: Receive Unframed All 1's Change Latched (RUA1L) – This bit is set when the RUA1 bit changes state.

Bit 7: Out Of MultiFrame Change Latched (OOMFL) – This bit is set when the OOMF bit changes state.

Bit 6: Severely Errored Frame Change Latched (SEFL) – This bit is set when the SEF bit changes state.

Bit 5: Change Of Frame Alignment Latched (COFAL) – This bit is set when the data path frame counters are updated with a new DS3 frame alignment that is different from the previous DS3 frame alignment.

Bit 4: Loss Of Frame Change Latched (LOFL) – This bit is set when the LOF bit changes state.

Bit 3: Remote Defect Indication Change Latched (RDIL) – This bit is set when the RDI bit changes state.

Bit 2: Alarm Indication Signal Change Latched (AISL) – This bit is set when the AIS bit changes state.

Bit 1: Out Of Frame Change Latched (OOFL) – This bit is set when the OOF bit changes state.

Bit 0: Loss Of Signal Change Latched (LOSL) – This bit is set when the LOS bit changes state.

Register Name: **T3.RSRL2**
Register Description: **T3 Receive Status Register Latched #2**
Register Address: **(1,3,5,7)2Ah**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	CPEL	FBEL	PEL	FEL

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	CPECL	FBECL	PECL	FECL

Bit 11: C-bit Parity Error Latched (CPEL) – This bit is set when a C-bit parity error is detected. This bit is set to zero in M23 DS3 mode.

Bit 10: Remote Error Indication Latched (FBEL) – This bit is set when a far-end block error is detected. This bit is set to zero in M23 DS3 mode.

Bit 9: P-bit Parity Error Latched (PEL) – This bit is set when a P-bit parity error is detected.

Bit 8: Framing Error Latched (FEL) – This bit is set when a framing error is detected. The type of framing error event that causes this bit to be set is determined by T3.RCR.FECC[1:0]

Bit 3: C-bit Parity Error Count Latched (CPECL) – This bit is set when the CPEC bit transitions from zero to one. This bit is set to zero in M23 DS3 mode.

Bit 2: Remote Error Indication Count Latched (FBECL) – This bit is set when the FBEC bit transitions from zero to one. This bit is set to zero in M23 DS3 mode.

Bit 1: P-bit Parity Error Count Latched (PECL) – This bit is set when the PEC bit transitions from zero to one.

Bit 0: Framing Error Count Latched (FECL) – This bit is set when the FEC bit transitions from zero to one.

Register Name: **T3.RSRIE1**
Register Description: **T3 Receive Status Register Interrupt Enable #1**
Register Address: **(1,3,5,7)2Ch**

Bit #	15	14	13	12	11	10	9	8
Name	Reserved	Reserved	Reserved	Reserved	T3FMIE	AICIE	IDLEIE	RUA1IE
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	OOMFIE	SEFIE	COFAIE	LOFIE	RAIIE	AISIE	OOFIE	LOSIE
Default	0	0	0	0	0	0	0	0

Bit 11: T3 Framing Format Mismatch Interrupt Enable (T3FMIE) – This bit enables an interrupt if the T3FML bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 10: Application Identification Channel Interrupt Enable (AICIE) – This bit enables an interrupt if the AICL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 9: DS3 Idle Signal Change Interrupt Enable (IDLEIE) – This bit enables an interrupt if the IDLEL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 8: Receive Unframed All 1's Interrupt Enable (RUA1IE) – This bit enables an interrupt if the RUA1L bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 7: Out Of Multiframe Interrupt Enable (OOMFIE) – This bit enables an interrupt if the OOMFL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 6: Severely Errored Frame Interrupt Enable (SEFIE) – This bit enables an interrupt if the SEFL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 5: Change Of Frame Alignment Interrupt Enable (COFAIE) – This bit enables an interrupt if the COFAL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 4: Loss Of Frame Interrupt Enable (LOFIE) – This bit enables an interrupt if the LOFL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 3: Remote Defect Indication Interrupt Enable (RDIIE) – This bit enables an interrupt if the RDIL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 2: Alarm Indication Signal Interrupt Enable (AISIE) – This bit enables an interrupt if the AISL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 1: Out Of Frame Interrupt Enable (OOFIE) – This bit enables an interrupt if the OOFL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Loss Of Signal Interrupt Enable (LOSIE) – This bit enables an interrupt if the LOSL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **T3.RSRIE2**
Register Description: **T3 Receive Status Register Interrupt Enable #2**
Register Address: **(1,3,5,7)2Eh**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	CPEIE	FBEIE	PEIE	FEIE
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	CPECIE	FBECIE	PECIE	FECIE
Default	0	0	0	0	0	0	0	0

Bit 11: C-bit Parity Error Interrupt Enable (CPEIE) – This bit enables an interrupt if the CPEL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 10: Remote Error Interrupt Enable (FBEIE) – This bit enables an interrupt if the FBEL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 9: P-bit Parity Error Interrupt Enable (PEIE) – This bit enables an interrupt if the PEL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 8: Framing Error Interrupt Enable (FEIE) – This bit enables an interrupt if the FEL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 3: C-bit Parity Error Count Interrupt Enable (CPECIE) – This bit enables an interrupt if the CPECL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 2: Far-End Block Error Count Interrupt Enable (FBECIE) – This bit enables an interrupt if the FBECL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 1: P-bit Parity Error Count Interrupt Enable (PECIE) – This bit enables an interrupt if the PECL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Framing Error Count Interrupt Enable (FECIE) – This bit enables an interrupt if the FECL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **T3.RFECR**
Register Description: **T3 Receive Framing Error Count Register**
Register Address: **(1,3,5,7)34h**

Bit #	15	14	13	12	11	10	9	8
Name	FE15	FE14	FE13	FE12	FE11	FE10	FE9	FE8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Framing Error Count (FE[15:0]) – These sixteen bits indicate the number of framing error events on the incoming **DS3** data stream. This register is updated via the PMU signal (see Section 10.4.5).

Register Name: **T3.RPECR**
Register Description: **T3 Receive P-Bit Parity Error Count Register**
Register Address: **(1,3,5,7)36h**

Bit #	15	14	13	12	11	10	9	8
Name	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: P-bit Parity Error Count (PE[15:0]) – These sixteen bits indicate the number of P-bit parity errors detected on the incoming **DS3** data stream. This register is updated via the PMU signal (see Section 10.4.5).

Register Name: **T3.RFBECR**
Register Description: **T3 Receive Far-End Block Error Count Register**
Register Address: **(1,3,5,7)38h**

Bit #	15	14	13	12	11	10	9	8
Name	FBE15	FBE14	FBE13	FBE12	FBE11	FBE10	FBE9	FBE8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	FBE7	FBE6	FBE5	FBE4	FBE3	FBE2	FBE1	FBE0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Far-End Block Error Count (FBE[15:0]) – These sixteen bits indicate the number of far-end block errors detected on the incoming DS3 data stream. The associated counter will not increment in M23 DS3 mode. This register is updated via the PMU signal (see Section 10.4.5).

Register Name: **T3.RCPECR**
Register Description: **T3 Receive C-Bit Parity Error Count Register**
Register Address: **(1,3,5,7)3Ah**

Bit #	15	14	13	12	11	10	9	8
Name	CPE15	CPE14	CPE13	CPE12	CPE11	CPE10	CPE9	CPE8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	CPE7	CPE6	CPE5	CPE4	CPE3	CPE2	CPE1	CPE0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: C-bit Parity Error Count (CPE[15:0]) – These sixteen bits indicate the number of C-bit parity errors detected on the incoming DS3 data stream. The associated counter will not increment in M23 DS3 mode. This register is updated via the PMU signal (see Section 10.4.5).

12.10.3 Transmit G.751 E3

The transmit G.751 E3 utilizes two registers.

12.10.3.1 Register Map

Table 12-35. Transmit G.751 E3 Framer Register Map

Address	Register	Register Description
(1,3,5,7)18h	E3G751.TCR	E3 G.751 Transmit Control Register
(1,3,5,7)1Ah	E3G751.TEIR	E3 G.751 Transmit Error Insertion Register
(1,3,5,7)1Ch	--	Reserved
(1,3,5,7)1Eh	--	Reserved

12.10.3.2 Register Bit Descriptions

Register Name: **E3G751.TCR**
Register Description: **E3 G.751 Transmit Control Register**
Register Address: **(1,3,5,7)18h**

Bit #	15	14	13	12	11	10	9	8
Name	Reserved	--	--	Reserved	Reserved	Reserved	TNBC1	TNBC0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	Reserved	Reserved	TABC1	TABC0	TFGC	TAIS
Default	0	0	0	0	0	0	0	0

Bits 9 to 8: Transmit N Bit Control (TNBC[1:0]) – These two bits control the source of the N bit.

00 = 1
01 = transmit data from HDLC controller.
10 = transmit data from FEAC controller.
11 = 0

Note: If TNBC[1:0] is 10 and TABC[1:0] is 01, both the N bit and A bit will carry the same transmit FEAC controller (one bit per frame period), however, the N bit and A bit in the same frame may or may not be equal.

Bits 3 to 2: Transmit A Bit Control (TABC[1:0]) – These two bits control the source of the A bit.

00 = automatically generated based upon received E3 alarms.
01 = transmit from the FEAC controller.
10 = 0
11 = 1

Note: If TABC[1:0] is 01 and TNBC[1:0] is 10, both the A bit and N bit will carry the same transmit FEAC controller (one bit per frame period), however, the A bit and N bit in the same frame may or may not be equal.

Bit 1: Transmit Frame Generation Control (TFGC) – When this bit is zero, the Transmit Frame Processor frame generation is enabled. The E3 overhead positions in the incoming E3 payload will be overwritten with the internally generated E3 overhead. When this bit is one, the Transmit Frame Processor frame generation is disabled. The E3 overhead positions in the incoming E3 payload will be passed through to error insertion. Note: The E3 overhead periods can still be overwritten by overhead insertion.

Bit 0: Transmit Alarm Indication Signal (TAIS) – When 0, the normal signal is transmitted. When 1, the output E3 data stream is forced to all ones (AIS).

Register Name: **E3G751.TEIR**
Register Description: **E3 G.751 Transmit Error Insertion Register**
Register Address: **(1,3,5,7)1Ah**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	Reserved	FEIC1	FEIC0	FEI	TSEI	MEIMS
Default	0	0	0	0	0	0	0	0

Bits 4 to 3: Framing Error Insert Control (FEIC[1:0]) – These two bits control the framing error event to be inserted.

00 = single bit error in one frame.
01 = word error in one frame.
10 = single bit error in four consecutive frames.
11 = word error in four consecutive frames.

Bit 2: Framing Error Insertion Enable (FEI) – When 0, framing error insertion is disabled. When 1, framing error insertion is enabled.

Bit 1: Transmit Single Error Insert (TSEI) – This bit causes an error of the enabled type(s) to be inserted in the transmit data stream if manual error insertion is disabled (MEIMS = 0). A 0 to 1 transition causes a single error to be inserted. For a second error to be inserted, this bit must be set to 0, and back to 1. Note: If MEIMS is low, and this bit transitions more than once between error insertion opportunities, only one error will be inserted.

Bit 0: Manual Error Insert Mode Select (MEIMS) – When 0, error insertion is initiated by the TSEI register bit. When 1, error insertion is initiated by the transmit manual error insertion signal (TMEI). Note: If TMEI or TSEI is one, changing the state of this bit may cause an error to be inserted.

12.10.4 Receive G.751 E3 Register Map

The receive G.751 E3 utilizes eight registers.

Table 12-36. Receive G.751 E3 Framer Register Map

Address	Register	Register Description
(1,3,5,7)20h	E3G751.RCR	E3 G.751 Receive Control Register
(1,3,5,7)22h	--	Reserved
(1,3,5,7)24h	E3G751.RSR1	E3 G.751 Receive Status Register #1
(1,3,5,7)26h	E3G751.RSR2	E3 G.751 Receive Status Register #2
(1,3,5,7)28h	E3G751.RSRL1	E3 G.751 Receive Status Register Latched #1
(1,3,5,7)2Ah	E3G751.RSRL2	E3 G.751 Receive Status Register Latched #2
(1,3,5,7)2Ch	E3G751.RSRIE1	E3 G.751 Receive Status Register Interrupt Enable #1
(1,3,5,7)2Eh	E3G751.RSRIE2	E3 G.751 Receive Status Register Interrupt Enable #2
(1,3,5,7)30h	--	Reserved
(1,3,5,7)32h	--	Reserved
(1,3,5,7)34h	E3G751.RFECR	E3 G.751 Receive Framing Error Count Register
(1,3,5,7)36h	--	Reserved
(1,3,5,7)38h	--	Reserved
(1,3,5,7)3Ah	--	Reserved
(1,3,5,7)3Ch	--	Unused
(1,3,5,7)3Eh	--	Unused

12.10.4.1 Register Bit Descriptions

Register Name: **E3G751.RCR**
Register Description: **E3 G.751 Receive Control Register**
Register Address: **(1,3,5,7)20h**

Bit #	15	14	13	12	11	10	9	8
Name	Reserved	Reserved	DLS	MDAISI	AAISD	ECC	FECC1	FECC0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RAILE	RAILD	RAIOD	RAIAD	ROMD	LIP1	LIP0	FRSYNC
Default	0	0	0	0	0	0	0	0

Bit 13: Receive FEAC Data Link Source (DLS) – When 0, the receive FEAC controller will be sourced from the N bit. When 1, the receive FEAC controller will be sourced from the A bit.

Bit 12: Manual Downstream AIS Insertion (MDAISI) – When 0, manual downstream AIS insertion is disabled. When 1, manual downstream AIS insertion is enabled.

Bit 11: Automatic Downstream AIS Disable (AAISD) – When 0, the presence of an LOS, OOF, or AIS condition will cause downstream AIS to be inserted. When 1, the presence of an LOS, OOF, or AIS condition will not cause downstream AIS to be inserted.

Bit 10: Error Count Control (ECC) – When 0, framing errors will not be counted if an OOF or AIS condition is present. When 1, framing errors will be counted regardless of the presence of an OOF or AIS condition.

Bits 9 to 8: Framing Error Count Control (FECC[1:0]) – These two bits control the type of framing error events that are counted.

00 = count OOF occurrences (counted regardless of the setting of the ECC bit)..
01 = count each bit error in the FAS (up to 10 per frame).
10 = count frame alignment signal (FAS) errors (up to one per frame).
11 = reserved

Bit 7: Receive Alarm Indication on LOF Enable (RAILE) – When 0, an LOF condition does not affect the receive alarm indication signal (RAI). When 1, an LOF condition will cause the transmit E3 A bit to be set to one if transmit automatic RAI is enabled.

Bit 6: Receive Alarm Indication on LOS Disable (RAILD) – When 0, an LOS condition will cause the transmit E3 A bit to be set to one if transmit automatic RAI is enabled. When 1, an LOS condition does not affect the RAI signal.

Bit 5: Receive Alarm Indication on OOF Disable (RAIOD) – When 0, an OOF condition will cause the transmit E3 A bit to be set to one if transmit automatic RAI is enabled. When 1, an OOF condition does not affect the RAI signal.

Bit 4: Receive Alarm Indication on AIS Disable (RAIAD) – When 0, an AIS condition will cause the transmit E3 A bit to be set to one if transmit automatic RAI is enabled. When 1, an AIS condition does not affect the RAI signal.

Bit 3: Receive Overhead Masking Disable (ROMD) – When 0, the E3 overhead positions in the outgoing E3 payload will be marked as overhead by RDENn. When 1, the E3 overhead positions in the outgoing E3 payload will be marked as data by RDENn.

Bits 2 to 1: LOF Integration Period (LIP[1:0]) – These two bits determine the OOF integration period for declaring LOF.

00 = OOF is integrated for 3 ms before declaring LOF
01 = OOF is integrated for 2 ms before declaring LOF.
10 = OOF is integrated for 1 ms before declaring LOF
11 = LOF is declared at the same time as OOF

Bit 0: Force Framer Resynchronization (FRSYNC) – A 0 to 1 transition forces an OOF condition at the FAS check. This bit must be cleared and set to one again to force another resynchronization

Register Name: **E3G751.RSR1**
Register Description: **E3 G.751 Receive Status Register #1**
Register Address: **(1,3,5,7)24h**

Bit #	15	14	13	12	11	10	9	8
Name	Reserved	Reserved	--	Reserved	Reserved	Reserved	Reserved	RUA1

Bit #	7	6	5	4	3	2	1	0
Name	RAB	RNB	--	LOF	RDI	AIS	OOF	LOS

Bit 8: Receive Unframed All 1's (RUA1) – When 0, the receive frame processor is not in a receive unframed all 1's (RUA1) condition. When 1, the receive frame processor is in an RUA1 condition.

Bit 7: Receive A Bit (RAB) – This bit is the integrated A bit extracted from the E3 frame.

Bit 6: Receive N Bit (RNB) – This bit is the integrated N bit extracted from the E3 frame.

Bit 4: Loss Of Frame (LOF) – When 0, the receive frame processor is not in a loss of frame (LOF) condition. When 1, the receive frame processor is in an LOF condition.

Bit 3: Remote Alarm Indication (RDI) – This bit indicates the current state of the remote alarm indication (RDI).

Bit 2: Alarm Indication Signal (AIS) – When 0, the receive frame processor is not in an alarm indication signal (AIS) condition. When 1, the receive frame processor is in an AIS condition.

Bit 1: Out Of Frame (OOF) – When 0, the receive frame processor is not in an out of frame (OOF) condition. When 1, the receive frame processor is in an OOF condition.

Bit 0: Loss Of Signal (LOS) – When 0, the receive loss of signal (LOS) input (RLOS) is low. When 1, RLOS is high.

Register Name: **E3G751.RSR2**
Register Description: **E3 G.751 Receive Status Register #2**
Register Address: **(1,3,5,7)26h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	Reserved	Reserved	Reserved	FEC

Bit 0: Framing Error Count (FEC) – When 0, the framing error count is zero. When 1, the framing error count is one or more.

Register Name: **E3G751.RSRL1**
Register Description: **E3 G.751 Receive Status Register Latched #1**
Register Address: **(1,3,5,7)28h**

Bit #	15	14	13	12	11	10	9	8
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RUA1L

Bit #	7	6	5	4	3	2	1	0
Name	ACL	NCL	COFAL	LOFL	RDIL	AISL	OOFL	LOSL

Bit 8: Receive Unframed All 1's Change Latched (RUA1L) – This bit is set when the RUA1 bit changes state.

Bit 7: A Bit Change Latched (ACL) – This bit is set when the RAB bit changes state.

Bit 6: N Bit Change Latched (NCL) – This bit is set when the RNB bit changes state.

Bit 5: Change Of Frame Alignment Latched (COFAL) – This bit is set when the data path frame counters are updated with a new frame alignment that is different from the previous frame alignment.

Bit 4: Loss Of Frame Change Latched (LOFL) – This bit is set when the LOF bit changes state.

Bit 3: Remote Alarm Indication Change Latched (RDIL) – This bit is set when the RDI bit changes state.

Bit 2: Alarm Indication Signal Change Latched (AISL) – This bit is set when the AIS bit changes state.

Bit 1: Out Of Frame Change Latched (OOFL) – This bit is set when the OOF bit changes state.

Bit 0: Loss Of Signal Change Latched (LOSL) – This bit is set when the LOS bit changes state.

Register Name: **E3G751.RSRL2**
Register Description: **E3 G.751 Receive Status Register Latched #2**
Register Address: **(1,3,5,7)2Ah**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	Reserved	Reserved	Reserved	FEL

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	Reserved	Reserved	Reserved	FECL

Bit 8: Framing Error Latched (FEL) – This bit is set when a framing error is detected.

Bit 0: Framing Error Count Latched (FECL) – This bit is set when the FEC bit transitions from zero to one.

Register Name: **E3G751.RSRIE1**
Register Description: **E3 G.751 Receive Status Register Interrupt Enable #1**
Register Address: **(1,3,5,7)2Ch**

Bit #	15	14	13	12	11	10	9	8
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RUA1IE
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	ACIE	NCIE	COFAIE	LOFIE	RDIIE	AISIE	OOFIE	LOSIE
Default	0	0	0	0	0	0	0	0

Bit 8: Receive Unframed All-Ones Interrupt Enable (RUA1IE) – This bit enables an interrupt if the RUA1L bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 7: A Bit Change Interrupt Enable (ACIE) – This bit enables an interrupt if the ACL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 6: N Bit Change Interrupt Enable (NCIE) – This bit enables an interrupt if the NCL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 5: Change Of Frame Alignment Interrupt Enable (COFAIE) – This bit enables an interrupt if the COFAL bit and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port are set.

0 = interrupt disabled
1 = interrupt enabled

Bit 4: Loss Of Frame Interrupt Enable (LOFIE) – This bit enables an interrupt if the LOFL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 3: Remote Alarm Indication Interrupt Enable (RDIIE) – This bit enables an interrupt if the RDIL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 2: Alarm Indication Signal Interrupt Enable (AISIE) – This bit enables an interrupt if the AISL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 1: Out Of Frame Interrupt Enable (OOFIE) – This bit enables an interrupt if the OOFL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Loss Of Signal Interrupt Enable (LOSIE) – This bit enables an interrupt if the LOSL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **E3G751.RSRIE2**
Register Description: **E3 G.751 Receive Status Register Interrupt Enable #2**
Register Address: **(1,3,5,7)2Eh**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	Reserved	Reserved	Reserved	FEIE
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	Reserved	Reserved	Reserved	FECIE
Default	0	0	0	0	0	0	0	0

Bit 8: Framing Error Interrupt Enable (FEIE) – This bit enables an interrupt if the FEL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Framing Error Count Interrupt Enable (FECIE) – This bit enables an interrupt if the FECL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **E3G751.RFECR**
Register Description: **E3 G.751 Receive Framing Error Count Register**
Register Address: **(1,3,5,7)34h**

Bit #	15	14	13	12	11	10	9	8
Name	FE15	FE14	FE13	FE12	FE11	FE10	FE9	FE8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Framing Error Count (FE[15:0]) – These sixteen bits indicate the number of framing error events on the incoming E3 data stream. This register is updated via the PMU signal (see Section 10.4.5).

12.10.5 Transmit G.832 E3 Register Map

The transmit G.832 E3 utilizes four registers.

Table 12-37. Transmit G.832 E3 Framer Register Map

Address	Register	Register Description
(1,3,5,7)18h	E3G832.TCR	E3 G.832 Transmit Control Register
(1,3,5,7)1Ah	E3G832.TEIR	E3 G.832 Transmit Error Insertion Register
(1,3,5,7)1Ch	E3G832.TMABR	E3 G.832 Transmit MA Byte Register
(1,3,5,7)1Eh	E3G832.TNGBR	E3 G.832 Transmit NR and GC Byte Register

12.10.5.1 Register Bit Descriptions

Register Name: **E3G832.TCR**
Register Description: **E3 G.832 Transmit Control Register**
Register Address: **(1,3,5,7)18h**

Bit #	15	14	13	12	11	10	9	8
Name	Reserved	--	--	Reserved	Reserved	TGCC	TNRC1	TNRC0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	TFEBE	AFEBED	TRDI	ARDID	TFGC	TAIS
Default	0	0	0	0	0	0	0	0

Bit 10: Transmit GC Byte Control (TGCC) – When 0, the GC byte is inserted from the transmit HDLC controller. When 1, the GC byte is inserted from the GC byte register.

Note: If bit TGCC is 0 and TNRC[1:0] is 01, both the GC byte and NR byte will carry the same transmit HDLC controller (eight bits per frame period), however, the GC byte and NR byte in the same frame may or may not be equal.

Bits 9 to 8: Transmit NR Byte Control (TNRC[1:0]) – These two bits control the source of the NR byte.

00 = all ones.
01 = transmit from the HDLC controller.
10 = transmit from the FEAC controller.
11 = NR byte register.

Note: If TNRC[1:0] is 01 and TGCC is 0, both the NR byte and GC byte will carry the same transmit HDLC controller (eight bits per frame period), however, the NR byte and GC byte in the same frame may or may not be equal.

Bit 5: Transmit REI Error (TFEBE) – When automatic REI generation is defeated (AFEBED = 1), this bit is inserted into the second bit of the MA byte.

Bit 4: Automatic REI Defeat (AFEBED) – When 0, the REI is automatically generated based upon the transmit remote error indication (TREI) signal. When 1, the REI is inserted from the register bit TFEBE.

Bit 3: Transmit RDI Alarm (TRDI) – When automatic RDI generation is defeated (ARDID = 1), this bit is inserted into the first bit of the MA byte.

Bit 2: Automatic RDI Defeat (ARDID) – When 0, the RDI is automatically generated based upon the received E3 alarms. When 1, the RDI is inserted from the register bit TRDI.

Bit 1: Transmit Frame Generation Control (TFGC) – When this bit is zero, the Transmit Frame Processor frame generation is enabled. The E3 overhead positions in the incoming E3 payload will be overwritten with the internally generated E3 overhead. When this bit is one, the Transmit Frame Processor frame generation is disabled. The E3 overhead positions in the incoming E3 payload will be passed through to error insertion. Note: The E3 overhead periods can still be overwritten by overhead insertion.

Bit 0: Transmit Alarm Indication Signal (TAIS) – When 0, the normal signal is transmitted. When 1, the E3 output data stream is forced to all ones (AIS).

Register Name: **E3G832.TEIR**
Register Description: **E3 G.832 Transmit Error Insertion Register**
Register Address: **(1,3,5,7)1Ah**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	Reserved	Reserved	CFBEIE	FBEI
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	PBEE	CPEIE	PEI	FEIC1	FEIC0	FEI	TSEI	MEIMS
Default	0	0	0	0	0	0	0	0

Bit 9: Continuous Remote Error Indication Error Insertion Enable (CFBEIE) – When 0, single remote error indication (REI) error insertion is enabled. When 1, continuous REI error insertion is enabled, and REI errors will be transmitted continuously if FEBI is high.

Bit 8: Remote Error Indication Error Insertion Enable (FBEI) – When 0, REI error insertion is disabled. When 1, REI error insertion is enabled.

Bit 7: Parity Block Error Enable (PBEE) – When 0, a parity error is generated by inverting a single bit in the EM byte. When 1, a parity error is generated by inverting all eight bits in the EM byte.

Bit 6: Continuous Parity Error Insertion Enable (CPEIE) – When 0, single parity (BIP-8) error insertion is enabled. When 1, continuous parity error insertion is enabled, and parity errors will be transmitted continuously if PEI is high.

Bit 5: Parity Error Insertion Enable (PEI) – When 0, parity error insertion is disabled. When 1, parity error insertion is enabled.

Bits 4 to 3: Framing Error Control (FEIC[1:0]) – These two bits control the framing error event to be inserted.

00 = single bit error in one frame.
01 = word error in one frame.
10 = single bit error in four consecutive frames.
11 = word error in four consecutive frames.

Bit 2: Framing Error Insertion Enable (FEI) – When 0, framing error insertion is disabled. When 1, framing error insertion is enabled.

Bit 1: Transmit Single Error Insert (TSEI) – This bit causes an error of the enabled type(s) to be inserted in the transmit data stream if manual error insertion is disabled (MEIMS = 0). A 0 to 1 transition causes a single error to be inserted. For a second error to be inserted, this bit must be set to 0, and back to 1. Note: If MEIMS is low, and this bit transitions more than once between error insertion opportunities, only one error will be inserted.

Bit 0: Manual Error Insert Mode Select (MEIMS) – When 0, error insertion is initiated by the TSEI register bit. When 1, error insertion is initiated by the transmit manual error insertion signal (TMEI). Note: If TMEI or TSEI is one, changing the state of this bit may cause an error to be inserted.

Register Name: **E3G832.TMABR**
Register Description: **E3 G.832 Transmit MA Byte Register**
Register Address: **(1,3,5,7)1Ch**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	TPT2	TPT1	TPT0	TTIGD	TTI3	TTI2	TTI1	TTI0
Default	0	0	0	0	0	0	0	0

Bits 7 to 5: Transmit Payload Type (TPT[2:0]) – These bits determines the value transmitted in the payload type (third, fourth, and fifth bits in the MA byte).

Bit 4: Transmit Timing Source Indicator Bit Generation Disable (TTIGD) – When 0, the last three bits of the MA byte (MA[6:8]) are generated from the four timing source indicator bits TTI[3:0]. When 1, TTI[3] is ignored and TTI[2:0] are directly inserted into the last three bits of the MA byte.

Bits 3 to 0: Transmit Timing Source Indication (TTI[3:0]) – These four bits make up the timing source indicator bits.

Register Name: **E3G832.TNGBR**
Register Description: **E3 G.832 Transmit NR and GC Byte Register**
Register Address: **(1,3,5,7)1Eh**

Bit #	15	14	13	12	11	10	9	8
Name	TGC7	TGC6	TGC5	TGC4	TGC3	TGC2	TGC1	TGC0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	TNR7	TNR6	TNR5	TNR4	TNR3	TNR2	TNR1	TNR0
Default	0	0	0	0	0	0	0	0

Bits 15 to 8: Transmit GC Byte (TGC[7:0]) – These eight bits are the GC byte to be inserted into the E3 frame.

Bits 7 to 0: Transmit NR Byte (TNR[7:0]) – These eight bits are the NR byte to be inserted into the E3 frame.

12.10.6 Receive G.832 E3 Register Map

The receive G.832 E3 utilizes thirteen registers.

Table 12-38. Receive G.832 E3 Framer Register Map

Address	Register	Register Description
(1,3,5,7)20h	E3G832.RCR	E3 G.832 Receive Control Register
(1,3,5,7)22h	E3G832.RMACR	E3 G.832 Receive MA Byte Control Register
(1,3,5,7)24h	E3G832.RSR1	E3 G.832 Receive Status Register #1
(1,3,5,7)26h	E3G832.RSR2	E3 G.832 Receive Status Register #2
(1,3,5,7)28h	E3G832.RSRL1	E3 G.832 Receive Status Register Latched #1
(1,3,5,7)2Ah	E3G832.RSRL2	E3 G.832 Receive Status Register Latched #2
(1,3,5,7)2Ch	E3G832.RSRIE1	E3 G.832 Receive Status Register Interrupt Enable #1
(1,3,5,7)2Eh	E3G832.RSRIE2	E3 G.832 Receive Status Register Interrupt Enable #2
(1,3,5,7)30h	E3G832.RMABR	E3 G.832 Receive MA Byte Register
(1,3,5,7)32h	E3G832.RNGBR	E3 G.832 Receive NR and GC Byte Register
(1,3,5,7)34h	E3G832.RFECR	E3 G.832 Receive Framing Error Count Register
(1,3,5,7)36h	E3G832.RPECR	E3 G.832 Receive Parity Error Count Register
(1,3,5,7)38h	E3G832.RFBER	E3 G.832 Receive Remote Error Indication Count Register
(1,3,5,7)3Ah	--	Reserved
(1,3,5,7)3Ch	--	Unused
(1,3,5,7)3Eh	--	Unused

12.10.6.1 Register Bit Descriptions

Register Name: **E3G832.RCR**
Register Description: **E3 G.832 Receive Control Register**
Register Address: **(1,3,5,7)20h**

Bit #	15	14	13	12	11	10	9	8
Name	Reserved	PEC	DLS	MDAISI	AAISD	ECC	FECC1	FECC0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RDILE	RDILD	RDIOD	RDIAD	ROMD	LIP1	LIP0	FRSYNC
Default	0	0	0	0	0	0	0	0

Bit 14: Parity Error Count (PEC) – When 0, BIP-8 block errors (EM byte) are detected (no more than one per frame). When 1, BIP-8-bit errors are detected (up to 8 per frame).

Bit 13: Receive HDLC Data Link Source (DLS) – When 0, the receive HDLC data link will be sourced from the GC byte. When 1, the receive HDLC data link will be sourced from the NR byte.

Bit 12: Manual Downstream AIS Insertion (MDAISI) – When 0, manual downstream AIS insertion is disabled. When 1, manual downstream AIS insertion is enabled.

Bit 11: Automatic Downstream AIS Disable (AAISD) – When 0, the presence of an LOS, OOF, or AIS condition will cause downstream AIS to be inserted. When 1, the presence of an LOS, OOF, or AIS condition will not cause downstream AIS to be inserted.

Bit 10: Error Count Control (ECC) – When 0, framing errors, parity errors, and REI errors will not be counted if an OOF or AIS condition is present. Parity errors and REI errors will also not be counted during the E3 frame in which an OOF or AIS condition is terminated, and the next E3 frame. When 1, framing errors, parity errors, and REI errors will be counted regardless of the presence of an OOF or AIS condition.

Bits 9 to 8: Framing Error Count Control (FECC[1:0]) – These two bits control the type of framing error events that are counted.

00 = count OOF occurrences (counted regardless of the setting of the ECC bit).
01 = count each bit error in FA1 and FA2 (up to 16 per frame).
10 = count frame alignment word (FA1 and FA2) errors (up to one per frame).
11 = count FA1 byte errors and FA2 byte errors (up to 2 per frame).

Bit 7: Receive Defect Indication on LOF Enable (RDILE) – When 0, an LOF condition does not affect the receive defect indication signal (RDI). When 1, an LOF condition will cause the transmit E3 RDI bit to be set to one if transmit automatic RDI is enabled.

Bit 6: Receive Defect Indication on LOS Disable (RDILD) – When 0, an LOS condition will cause the transmit E3 RDI bit to be set to one if transmit automatic RDI is enabled. When 1, an LOS condition does not affect the RDI signal.

Bit 5: Receive Defect Indication on OOF Disable (RDIOD) – When 0, an OOF condition will cause the transmit E3 RDI bit to be set to one if transmit automatic RDI is enabled. When 1, an OOF condition does not affect the RDI signal.

Bit 4: Receive Defect Indication on AIS Disable (RDIAD) – When 0, an AIS condition will cause the transmit E3 RDI bit to be set to one if transmit automatic RDI is enabled. When 1, an AIS condition does not affect the RDI signal.

Bit 3: Receive Overhead Masking Disable (ROMD) – When 0, the E3 overhead positions in the outgoing E3 payload will be marked as overhead by RDENn. When 1, the E3 overhead positions in the outgoing E3 payload will be marked as data by RDENn.

Bits 2 to 1: LOF Integration Period (LIP[1:0]) – These two bits determine the OOF integration period for declaring LOF.

00 = OOF is integrated for 3 ms before declaring LOF.
01 = OOF is integrated for 2 ms before declaring LOF.
10 = OOF is integrated for 1 ms before declaring LOF.
11 = LOF is declared at the same time as OOF.

Bit 0: Force Framer Resynchronization (FRSYNC) – A 0 to 1 transition forces. an OOF condition at the next framing word check. This bit must be cleared and set to one again to force another resynchronization.

Register Name: **E3G832.RMACR**
Register Description: **E3 G.832 Receive MA Byte Control Register**
Register Address: **(1,3,5,7)22h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	EPT2	EPT1	EPT0	TIED
Default	0	0	0	0	0	0	0	0

Bits 3 to 1: Expected Payload Type (EPT[2:0]) – These three bits contain the expected value of the payload type.

Bit 0: Timing Source Indicator Bit Extraction Disable (TIED) – When 0, the four timing source indications bits are extracted from the last three bits of the MA byte (MA[6:8]), and stored in a register. When 1, timing source indicator bit extraction is disabled, and the last three bits of the MA byte are integrated and stored in a register.

Register Name: **E3G832.RSR1**
Register Description: **E3 G.832 Receive Status Register #1**
Register Address: **(1,3,5,7)24h**

Bit #	15	14	13	12	11	10	9	8
Name	Reserved	--	--	RPTU	RPTM	Reserved	Reserved	RUA1

Bit #	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	--	LOF	RAI	AIS	OOF	LOS

Bit 12: Receive Payload Type Unstable (RPTU) – When 0, the receive payload type is stable. When 1, the receive payload type is unstable.

Bit 11: Receive Payload Type Mismatch (RPTM) – When 0, the receive payload type and expected payload type match. When 1, the receive payload type and expected payload type do not match.

Bit 8: Receive Unframed All 1's (RUA1) – When 0, the receive frame processor is not in a receive unframed all 1's (RUA1) condition. When 1, the receive frame processor is in an RUA1 condition.

Bit 4: Loss Of Frame (LOF) – When 0, the receive frame processor is not in a loss of frame (LOF) condition. When 1, the receive frame processor is in an LOF condition.

Bit 3: Remote Defect Indication (RDI) – This bit indicates the current state of the remote defect indication (RDI).

Bit 2: Alarm Indication Signal (AIS) – When 0, the receive frame processor is not in an alarm indication signal (AIS) condition. When 1, the receive frame processor is in an AIS condition.

Bit 1: Out Of Frame (OOF) – When 0, the receive frame processor is not in an out of frame (OOF) condition. When 1, the receive frame processor is in an OOF condition.

Bit 0: Loss Of Signal (LOS) – When 0, the receive loss of signal (LOS) input (RLOS) is low. When 1, RLOS is high.

Register Name: **E3G832.RSR2**
Register Description: **E3 G.832 Receive Status Register #2**
Register Address: **(1,3,5,7)26h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	Reserved	FBEC	PEC	FEC

Bit 2: Remote Error Indication Count (FBEC) – When 0, the remote error indication count is zero. When 1, the remote error indication count is one or more.

Bit 1: Parity Error Count (PEC) – When 0, the parity error count is zero. When 1, the parity error count is one or more.

Bit 0: Framing Error Count (FEC) – When 0, the framing error count is zero. When 1, the framing error count is one or more.

Register Name: **E3G832.RSRL1**
Register Description: **E3 G.832 Receive Status Register Latched #1**
Register Address: **(1,3,5,7)28h**

Bit #	15	14	13	12	11	10	9	8
Name	Reserved	--	TIL	RPTUL	RPTML	RPTL	Reserved	RUA1L

Bit #	7	6	5	4	3	2	1	0
Name	GCL	NRL	COFAL	LOFL	RDIL	AISL	OOFL	LOSL

Bit 13: Timing Source Indication Change Latched (TIL) – This bit is set when the TI[3:0] bits change state.

Bit 12: Receive Payload Type Unstable Latched (RPTUL) – This bit is set when the RPTU bit transitions from zero to one.

Bit 11: Receive Payload Type Mismatch Latched (RPTML) – This bit is set when the RPTM bit transitions from zero to one.

Bit 10: Receive Payload Type Change Latched (RPTL) – This bit is set when the RPT[2:0] bits change state.

Bit 8: Receive Unframed All 1's Change Latched (RUA1L) – This bit is set when the RUA1 bit changes state.

Bit 7: GC Byte Change Latched (GCL) – This bit is set when the RGC byte changes state.

Bit 6: NR Byte Change Latched (NRL) – This bit is set when the RNR byte changes state.

Bit 5: Change Of Frame Alignment Latched (COFAL) – This bit is set when the data path frame counters are updated with a new frame alignment that is different from the previous frame alignment.

Bit 4: Loss Of Frame Change Latched (LOFL) – This bit is set when the LOF bit changes state.

Bit 3: Remote Defect Indication Change Latched (RDIL) – This bit is set when the RDI bit changes state.

Bit 2: Alarm Indication Signal Change Latched (AISL) – This bit is set when the AIS bit changes state.

Bit 1: Out Of Frame Change Latched (OOFL) – This bit is set when the OOF bit changes state.

Bit 0: Loss Of Signal Change Latched (LOSL) – This bit is set when the LOS bit changes state.

Register Name: **E3G832.RSRL2**
Register Description: **E3 G.832 Receive Status Register Latched #2**
Register Address: **(1,3,5,7)2Ah**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	Reserved	FBEL	PEL	FEL

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	Reserved	FBECL	PECL	FECL

Bit 10: Remote Error Indication Latched (FBEL) – This bit is set when a remote error indication is detected.

Bit 9: Parity Error Latched (PEL) – This bit is set when a BIP-8 parity error is detected.

Bit 8: Framing Error Latched (FEL) – This bit is set when a framing error is detected.

Bit 2: Remote Error Indication Count Latched (FBECL) – This bit is set when the FBEC bit transitions from zero to one.

Bit 1: Parity Error Count Latched (PECL) – This bit is set when the PEC bit transitions from zero to one.

Bit 0: Framing Error Count Latched (FECL) – This bit is set when the FEC bit transitions from zero to one.

Register Name: **E3G832.RSRIE1**
Register Description: **E3 G.832 Receive Status Register Interrupt Enable #1**
Register Address: **(1,3,5,7)2Ch**

Bit #	15	14	13	12	11	10	9	8
Name	Reserved	--	TIIE	RPTUIE	RPTMIE	RPTIE	Reserved	RUA1IE
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	GCIE	NRIE	COFAIE	LOFIE	RAIIE	AISIE	OOFIE	LOSIE
Default	0	0	0	0	0	0	0	0

Bit 13: Timing Indication Interrupt Enable (TIIE) – This bit enables an interrupt if the TIL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 12: Receive Payload Type Unstable Interrupt Enable (RPTUIE) – This bit enables an interrupt if the RPTUL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 11: Receive Payload Type Mismatch Interrupt Enable (RPTMIE) – This bit enables an interrupt if the RPTML bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 10: Receive Payload Type Interrupt Enable (RPTIE) – This bit enables an interrupt if the RPTL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 8: Receive Unframed All 1's Interrupt Enable (RUA1IE) – This bit enables an interrupt if the RUA1L bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 7: GC Byte Interrupt Enable (GCIE) – This bit enables an interrupt if the GCL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 6: NR Byte Interrupt Enable (NRIE) – This bit enables an interrupt if the NRL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 5: Change Of Frame Alignment Interrupt Enable (COFAIE) – This bit enables an interrupt if the COFAL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 4: Loss Of Frame Interrupt Enable (LOFIE) – This bit enables an interrupt if the LOFL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 3: Remote Defect Indication Interrupt Enable (RDIIE) – This bit enables an interrupt if the RDIL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 2: Alarm Indication Signal Interrupt Enable (AISIE) – This bit enables an interrupt if the AISL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 1: Out Of Frame Interrupt Enable (OOFIE) – This bit enables an interrupt if the OOFL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Loss Of Signal Interrupt Enable (LOSIE) – This bit enables an interrupt if the LOSL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **E3G832.RSRIE2**
Register Description: **E3 G.832 Receive Status Register Interrupt Enable #2**
Register Address: **(1,3,5,7)2Eh**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	Reserved	FBEIE	PEIE	FEIE
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	Reserved	FBECIE	PECIE	FECIE
Default	0	0	0	0	0	0	0	0

Bit 10: Remote Error Indication Interrupt Enable (FBEIE) – This bit enables an interrupt if the FBEL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 9: Parity Error Interrupt Enable (PEIE) – This bit enables an interrupt if the PEL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 8: Framing Error Interrupt Enable (FEIE) – This bit enables an interrupt if the FEL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 2: Remote Error Indication Count Interrupt Enable (FBECIE) – This bit enables an interrupt if the FBECL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 1: Parity Error Count Interrupt Enable (PECIE) – This bit enables an interrupt if the PECL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Framing Error Count Interrupt Enable (FECIE) – This bit enables an interrupt if the FECL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **E3G832.RMABR**
Register Description: **E3 G.832 Receive MA Byte Register**
Register Address: **(1,3,5,7)30h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	RPT2	RPT1	RPT0	TI3	TI2	TI1	TI0
Default	0	0	0	0	0	0	0	0

Bits 6 to 4: Receive Payload Type (RPT[2:0]) – These three bits are the integrated version of the payload type (MA[3:5]) from the MA byte.

Bits 3 to 0: Receive Timing Source Indication (TI[3:0]) – When timing source indicator extraction is enabled, these four bits are the integrated version of the four timing source indicator bits extracted from the last three bits of the MA byte (MA[6:8]). When timing source indicator bit extraction is disabled, TI[3] is zero, and TI[2:0] contain the integrated version of the last three bits of the MA byte.

Register Name: **E3G832.RNGBR**
Register Description: **E3 G.832 Receive NR and GC Byte Register**
Register Address: **(1,3,5,7)32h**

Bit #	15	14	13	12	11	10	9	8
Name	RGC7	RGC6	RGC5	RGC4	RGC3	RGC2	RGC1	RGC0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RNR7	RNR6	RNR5	RNR4	RNR3	RNR2	RNR1	RNR0
Default	0	0	0	0	0	0	0	0

Bits 15 to 8: Receive GC Byte (RGC[7:0]) – These eight bits are the integrated version of the GC byte as extracted from the E3 frame.

Bits 7 to 0: Receive NR Byte (RNR[7:0]) – These eight bits are the integrated version of the NR byte as extracted from the E3 frame.

Register Name: **E3G832.RFECR**
Register Description: **E3 G.832 Receive Framing Error Count Register**
Register Address: **(1,3,5,7)34h**

Bit #	15	14	13	12	11	10	9	8
Name	FE15	FE14	FE13	FE12	FE11	FE10	FE9	FE8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Framing Error Count (FE[15:0]) – These sixteen bits indicate the number of framing error events on the incoming E3 data stream. This register is updated via the PMU signal (see Section 10.4.5).

Register Name: **E3G832.RPECR**
Register Description: **E3 G.832 Receive Parity Error Count Register**
Register Address: **(1,3,5,7)36h**

Bit #	15	14	13	12	11	10	9	8
Name	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Parity Error Count (PE[15:0]) – These sixteen bits indicate the number of parity (BIP-8) errors detected on the incoming E3 data stream. This register is updated via the PMU signal (see Section 10.4.5).

Register Name: **E3G832.RFBER**
Register Description: **E3 G.832 Receive Remote Error Indication Count Register**
Register Address: **(1,3,5,7)38h**

Bit #	15	14	13	12	11	10	9	8
Name	FBE15	FBE14	FBE13	FBE12	FBE11	FBE10	FBE9	FBE8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	FBE7	FBE6	FBE5	FBE4	FBE3	FBE2	FBE1	FBE0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Remote Error Indication Count (FBE[15:0]) – These sixteen bits indicate the number of remote error indications detected on the incoming E3 data stream. This register is updated via the PMU signal (see Section 10.4.5).

12.10.7 Transmit Clear Channel

The transmit clear-channel mode utilizes one register.

12.10.7.1 Register Map

Table 12-39. Transmit Clear-Channel Register Map

Address	Register	Register Description
(1,3,5,7)18h	CC.TCR	Clear-Channel Transmit Control Register
(1,3,5,7)1Ah	--	Reserved
(1,3,5,7)1Ch	--	Reserved
(1,3,5,7)1Eh	--	Reserved

12.10.7.2 Register Bit Descriptions

Register Name: **CC.TCR**
Register Description: **Clear-Channel Transmit Control Register**
Register Address: **(1,3,5,7)18h**

Bit #	15	14	13	12	11	10	9	8
Name	Reserved	--	--	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	Reserved	Reserved	Reserved	Reserved	Reserved	TAIS
Default	0	0	0	0	0	0	0	0

Bit 0: Transmit Alarm Indication Signal (TAIS) – When 0, the normal signal is transmitted. When 1, the output clear-channel data stream is forced to all ones (AIS). Note: This bit is logically ORed with the TAIS input signal.

12.10.8 Receive Clear Channel

The receive clear-channel mode utilizes four registers.

12.10.8.1 Register Map

Table 12-40. Receive Clear-Channel Register Map

Address	Register	Register Description
(1,3,5,7)20h	CC.RCR	Clear-Channel Receive Control Register
(1,3,5,7)22h	--	Reserved
(1,3,5,7)24h	CC.RSR1	Clear-Channel Receive Status Register #1
(1,3,5,7)26h	--	Reserved
(1,3,5,7)28h	CC.RSRL1	Clear-Channel Receive Status Register Latched #1
(1,3,5,7)2Ah	--	Reserved
(1,3,5,7)2Ch	CC.RSRIE1	Clear-Channel Receive Status Register Interrupt Enable #1
(1,3,5,7)2Eh	--	Reserved
(1,3,5,7)30h	--	Reserved
(1,3,5,7)32h	--	Reserved
(1,3,5,7)34h	--	Reserved
(1,3,5,7)36h	--	Reserved
(1,3,5,7)38h	--	Reserved
(1,3,5,7)3Ah	--	Reserved
(1,3,5,7)3Ch	--	Unused
(1,3,5,7)3Eh	--	Unused

12.10.8.2 Register Bit Descriptions

Register Name: **CC.RCR**
Register Description: **Clear-Channel Receive Control Register**
Register Address: **(1,3,5,7)20h**

Bit #	15	14	13	12	11	10	9	8
Name	Reserved	Reserved	Reserved	MDAISI	AAISD	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

Bit 12: Manual Downstream AIS Insertion (MDAISI) – When 0, manual downstream AIS insertion is disabled. When 1, manual downstream AIS insertion is enabled.

Bit 11: Automatic Downstream AIS Disable (AAISD) – When 0, the presence of an LOS condition will cause downstream AIS to be inserted. When 1, the presence of an LOS condition will not cause downstream AIS to be inserted.

Register Name: **CC.RSR1**
Register Description: **Clear-Channel Receive Status Register #1**
Register Address: **(1,3,5,7)24h**

Bit #	15	14	13	12	11	10	9	8
Name	Reserved	Reserved	--	Reserved	Reserved	Reserved	Reserved	RUA1
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	--	Reserved	Reserved	Reserved	Reserved	LOS
Default	0	0	0	0	0	0	0	0

Bit 8: Receive Unframed All Ones (RUA1) – When 0, the receive frame processor is not in a receive unframed all 1's (RUA1) condition. When 1, the receive frame processor is in an RUA1 condition.

Bit 0: Loss Of Signal (LOS) – When 0, the receive loss of signal (LOS) input (RLOS) is low. When 1, RLOS is high.

Register Name: **CC.RSRL1**
Register Description: **Clear-Channel Receive Status Register Latched #1**
Register Address: **(1,3,5,7)28h**

Bit #	15	14	13	12	11	10	9	8
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RUA1L
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LOSL
Default	0	0	0	0	0	0	0	0

Bit 8: Receive Unframed All Ones Latched (RUA1L) – This bit is set when the RUA1 bit changes state.

Bit 0: Loss Of Signal Change Latched (LOSL) – This bit is set when the LOS bit changes state.

Register Name: **CC.RSRIE1**
Register Description: **Clear-Channel Receive Status Register Interrupt Enable #1**
Register Address: **(1,3,5,7)2Ch**

Bit #	15	14	13	12	11	10	9	8
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RUA1IE
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LOSIE
Default	0	0	0	0	0	0	0	0

Bit 8: Receive Unframed All-Ones Interrupt Enable (RUA1IE) – This bit enables an interrupt if the RUA1L bit is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Loss Of Signal Interrupt Enable (LOSIE) – This bit enables an interrupt if the LOSL bit is set.

0 = interrupt disabled
1 = interrupt enabled

12.11 Fractional DS3/E3

12.11.1 Fractional Transmit Side Register Map

The transmit side utilizes three registers.

Table 12-41. Fractional Transmit Side Register Map

Address	Register	Register Description
(1,3,5,7)40h	FRAC.TCR	Fractional Transmit Control Register
(1,3,5,7)42h	FRAC.TDGSR	Fractional Transmit Data Group Size Register
(1,3,5,7)44h	FRAC.TSASR	Fractional Transmit Section A Size Register
(1,3,5,7)46h	--	Unused

12.11.1.1 Register Bit Descriptions

Register Name: **FRAC.TCR**
Register Description: **Fractional Transmit Control Register**
Register Address: **(1,3,5,7)40h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	TFOSC1	TFOSC0	TSASS
Default	0	0	0	0	0	0	0	0

Bits 2 to 1: Transmit Fractional Overhead Source Control (TFOSC[1:0]) – These two bits control the source of the transmit fractional overhead.

00 = all zeros.
01 = all ones.
10 = 1010 pattern
11 = external (TFOH)

Bit 0: Transmit Section A Source Select (TSASS)

0 = Section A contains fractional overhead
1 = Section A contains payload data

Register Name: **FRAC.TDGSR**
Register Description: **Fractional Transmit Data Group Size Register**
Register Address: **(1,3,5,7)42h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	TDGS12	TDGS11	TDGS10	TDGS9	TDGS8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	TDGS7	TDGS6	TDGS5	TDGS4	TDGS3	TDGS2	TDGS1	TDGS0
Default	0	0	0	0	0	0	0	0

Bits 12 to 0: Transmit Data Group Size (TDGS[12:0]) – These thirteen bits indicate the number of bits contained within each transmit data group. A values of 0000h and 0001h both result in a transmit data group size of one bit.

Register Name: **FRAC.TSASR**
Register Description: **Fractional Transmit Section A Size Register**
Register Address: **(1,3,5,7)44h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	TSAS12	TSAS11	TSAS10	TSAS9	TSAS8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	TSAS7	TSAS6	TSAS5	TSAS4	TSAS3	TSAS2	TSAS1	TSAS0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Transmit Section A Size (TSAS[12:0]) – These thirteen bits indicate the number of bits contained within Section A of each transmit data group. If TSAS[12:0] is equal to or greater than the data group size (TDGSR.TDGS[12:0]), only “Section A” data will be transmitted.

12.11.2 Fractional Receive Side Register Map

The receive side utilizes three registers.

Table 12-42. Receive Side Register Map

Address	Register	Register Description
(1,3,5,7)48h	FRAC.RCR	Fractional Receive Control Register
(1,3,5,7)4Ah	FRAC.RDGSR	Fractional Receive Data Group Size Register
(1,3,5,7)4Ch	FRAC.RSASR	Fractional Receive Section A Size Register
(1,3,5,7)4Eh	--	Unused

12.11.2.1 Register Bit Descriptions

Register Name: **FRAC.RCR**
Register Description: **Fractional Receive Control Register**
Register Address: **(1,3,5,7)48h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	--	--	RSASS
Default	0	0	0	0	0	0	0	0

Bit 0: Receive Section A Source Select (RSASS) – When 0, Section A of each receive data group will contain fractional overhead. When 1, Section A of each receive data group will contain payload data.

Register Name: **FRAC.RDGSR**
Register Description: **Fractional Receive Data Group Size Register**
Register Address: **(1,3,5,7)4Ah**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	RDGS12	RDGS11	RDGS10	RDGS9	RDGS8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RDGS7	RDGS6	RDGS5	RDGS4	RDGS3	RDGS2	RDGS1	RDGS0
Default	0	0	0	0	0	0	0	0

Bits 12 to 0: Receive Data Group Size (RDGS[12:0]) – These thirteen bits indicate the number of bits contained within each receive data group. A values of 0000h and 0001h both result in a receive data group size of one bit.

Register Name: **FRAC.RSASR**
Register Description: **Fractional Receive Section A Size Register**
Register Address: **(1,3,5,7)4Ch**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	RSAS12	RSAS11	RSAS10	RSAS9	RSAS8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RSAS7	RSAS6	RSAS5	RSAS4	RSAS3	RSAS2	RSAS1	RSAS0
Default	0	0	0	0	0	0	0	0

Bits 12 to 0: Receive Section A Size (RSAS[12:0]) – These thirteen bits indicate the number of bits contained within Section A of each receive data group. If RSAS[12:0] is equal to or greater than the data group size (*FRAC.RDGSR*.RDGS[12:0]), all data will be marked as “Section A” data.

12.12 DS3/E3 PLCP

12.12.1 Transmit Side PLCP

The transmit side utilizes seven registers.

12.12.1.1 Register Map

Table 12-43. Transmit Side PLCP Register Map

Address	Register	Register Description
(1,3,5,7)50h	PLCP.TCR	PLCP Transmit Control Register
(1,3,5,7)52h	PLCP.TEIR	PLCP Transmit Error Insertion Register
(1,3,5,7)54h	PLCP.TFGBR	PLCP Transmit F1 and G1 Byte Register
(1,3,5,7)56h	PLCP.TM12BR	PLCP Transmit M1 and M2 Byte Register
(1,3,5,7)58h	PLCP.TZ12BR	PLCP Transmit Z1 and Z2 Byte Register
(1,3,5,7)5Ah	PLCP.TZ34BR	PLCP Transmit Z3 and Z4 Byte Register
(1,3,5,7)5Ch	PLCP.TZ56BR	PLCP Transmit Z5 and Z6 Byte Register
(1,3,5,7)5Eh	--	Unused

12.12.1.2 Register Bit Descriptions

Register Name: **PLCP.TCR**
Register Description: **PLCP Transmit Control Register**
Register Address: **(1,3,5,7)50h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	TMC1	TMC0	TF1C1	TF1C0	AREID
Default	0	0	0	0	0	0	0	0

Bits 4 to 3: Transmit M2 and M1 Byte Control (TMC[1:0]) – These two bits control the source of the transmit M2 and M1 bytes.

00 = concatenated M1 and M2 (128 kHz) from transmit HDLC controller.
01 = M2 (64 kHz) from transmit HDLC controller; M1 from M1 byte register (PLCP.TM12BR).
10 = M2 from M2 byte register; M1 (64 kHz) from transmit HDLC controller.
11 = M2 from M2 byte register; M1 from M1 byte register

Bits 2 to 1: Transmit F1 Byte Control (TF1C[1:0]) – These two bits control the source of the transmit F1 byte.

00 = transmit Trail Trace controller.
01 = transmit HDLC controller.
10 = F1 byte register (PLCP.TFGBR).
11 = reserved

Note: If TMC[1:0] is 00 and TF1C[1:0] is 01, the F1 byte will be invalid. If TMC[1:0] is 01 and TF1C[1:0] is 01, both M2 and F1 will carry the transmit HDLC data link. If TMC[1:0] is 10 and TF1C[1:0] is 01, both M1 and F1 will carry the transmit HDLC data link. When F1 and M# both carry the transmit HDLC data link, the F1 byte and M# byte in the same frame may or may not be equal.

Bit 0: Automatic REI Defeat (AREID) – When 0, the REI is automatically generated based upon the parity (BIP-8) errors detected in the receive PLCP Frame Processor. When 1, the REI is inserted from the G1 register bits TREI[3:0].

Register Name: **PLCP.TEIR**
Register Description: **PLCP Transmit Error Insertion Register**
Register Address: **(1,3,5,7)52h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	REIME	CREIIE	REIEI	PBEE	CPEIE	PEI
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	FEE	FEIC1	FEIC0	FEI	TSEI	MEIMS
Default	0	0	0	0	0	0	0	0

Bit 13: Remote Error Indication Maximum Error (REIME) – When 0, an REI error is generated by inserting a value of 1h (single error) into the REI bits (G1[1:4]). When 1, an REI error is generated by inserting a value of 8h (eight errors) into the REI bits.

Bit 12: Continuous Remote Error Indication Error Insertion Enable (CREIIE) – When 0, single remote error indication (REI) error insertion is enabled. When 1, continuous REI error insertion is enabled, and REI errors will be continuously transmitted if REIEI is high.

Bit 11: Remote Error Indication Error Insertion Enable (REIEI) – When 0, REI error insertion is disabled. When 1, REI error insertion is enabled.

Bit 10: Parity Block Error Enable (PBEE) – When 0, a parity error is generated by inverting a single bit in the B1 byte. When 1, a parity error is generated by inverting all eight bits in the B1 byte.

Bit 9: Continuous Parity Error Insertion Enable (CPEIE) – When 0, single parity (BIP-8) error insertion is enabled. When 1, continuous parity error insertion is enabled, and parity errors will be transmitted continuously if PEI is high.

Bit 8: Parity Error Insertion Enable (PEI) – When 0, parity (BIP-8) error insertion is disabled. When 1, parity (BIP-8) error insertion is enabled.

Bit 5: Framing Byte Error Enable (FEE) – When 0, a framing bit error is generated by inverting a single bit in the indicated byte. When 1, a framing byte error is generated by inverting all eight bits of the indicated byte.

Bits 4 to 3: Framing Error Control (FEIC[1:0]) – These two bits control the type of framing error event to be inserted.

00 = single A1 or A2 error (1 per subframe maximum).
01 = single POI (P#) error (1 per 2 subframes maximum).
10 = both an A1 and an A2 error in the same subframe.
11 = two POI (P#) errors in consecutive subframes.

Bit 2: Framing Error Insertion Enable (FEI) – When 0, framing error insertion is disabled. When 1, framing error insertion is enabled.

Bit 1: Transmit Single Error Insert (TSEI) – This bit causes an error of the enabled type(s) to be inserted in the transmit data stream if manual error insertion is disabled (MEIMS = 0). A 0 to 1 transition causes a single error to be inserted. For a second error to be inserted, this bit must be set to 0, and back to 1. Note: If MEIMS is low, and this bit transitions more than once between error insertion opportunities, only one error will be inserted.

Bit 0: Manual Error Insert Mode Select (MEIMS) – When 0, error insertion is initiated by the TSEI register bit. When 1, error insertion is initiated by the transmit manual error insertion signal (TMEI). Note: If TMEI or TSEI is one, changing the state of this bit may cause an error to be inserted.

Register Name: **PLCP.TFGBR**
Register Description: **PLCP Transmit F1 and G1 Byte Register**
Register Address: **(1,3,5,7)54h**

Bit #	15	14	13	12	11	10	9	8
Name	TF17	TF16	TF15	TF14	TF13	TF12	TF11	TF10
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	TREI3	TREI2	TREI1	TREI0	TRAI	TLSS2	TLSS1	TLSS0
Default	0	0	0	0	0	0	0	0

Bits 15 to 8: Transmit F1 Byte (TF1[7:0]) – These eight bits are the F1 byte to be inserted into the transmit PLCP frame.

Bits 7 to 4: Transmit REI Setting (TREI[3:0]) – When automatic REI generation is defeated (PLCP.TCR.AREID = 0), these bits are inserted into the REI bits (G1[1:4]).

Bit 3: Transmit RAI Setting (TRAI) –This bit is inserted into the RAI bits (G1[5]).

Bits 2 to 0: Transmit Link Status Signal (TLSS[2:0]) – These three bits are the transmit link status signal (G1[6:8]) to be inserted into the transmit PLCP frame.

Register Name: **PLCP.TM12BR**
Register Description: **PLCP Transmit M1 and M2 Byte Register**
Register Address: **(1,3,5,7)56h**

Bit #	15	14	13	12	11	10	9	8
Name	TM27	TM26	TM25	TM24	TM23	TM22	TM21	TM20
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	TM17	TM16	TM15	TM14	TM13	TM12	TM11	TM10
Default	0	0	0	0	0	0	0	0

Bits 15 to 8: Transmit M2 Byte (TM2[7:0]) – These eight bits are the M2 byte to be inserted into the transmit PLCP frame.

Bits 7 to 0: Transmit M1 Byte (TM1[7:0]) – These eight bits are the M1 byte to be inserted into the transmit PLCP frame.

Register Name: **PLCP.TZ12BR**
Register Description: **PLCP Transmit Z1 and Z2 Byte Register**
Register Address: **(1,3,5,7)58h**

Bit #	15	14	13	12	11	10	9	8
Name	TZ27	TZ26	TZ25	TZ24	TZ23	TZ22	TZ21	TZ20
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	TZ17	TZ16	TZ15	TZ14	TZ13	TZ12	TZ11	TZ10
Default	0	0	0	0	0	0	0	0

Bits 15 to 8: Transmit Z2 Byte (TZ2[7:0]) – These eight bits are the Z2 byte to be inserted into the transmit PLCP frame.

Bits 7 to 0: Transmit Z1 Byte (TZ1[7:0]) – These eight bits are the Z1 byte to be inserted into the transmit PLCP frame.

Register Name: **PLCP.TZ34BR**
Register Description: **PLCP Transmit Z3 and Z4 Byte Register**
Register Address: **(1,3,5,7)5Ah**

Bit #	15	14	13	12	11	10	9	8
Name	TZ47	TZ46	TZ45	TZ44	TZ43	TZ42	TZ41	TZ40
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	TZ37	TZ36	TZ35	TZ34	TZ33	TZ32	TZ31	TZ30
Default	0	0	0	0	0	0	0	0

Bits 15 to 8: Transmit Z4 Byte (TZ4[7:0]) – These eight bits are the Z4 byte to be inserted into the transmit PLCP frame (This bits are unused in E3 mode).

Bits 7 to 0: Transmit Z3 Byte (TZ3[7:0]) – These eight bits are the Z3 byte to be inserted into the transmit PLCP frame.

Register Name: **PLCP.TZ56BR**
Register Description: **PLCP Transmit Z5 and Z6 Byte Register**
Register Address: **(1,3,5,7)5Ch**

Bit #	15	14	13	12	11	10	9	8
Name	TZ67	TZ66	TZ65	TZ64	TZ63	TZ62	TZ61	TZ60
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	TZ57	TZ56	TZ55	TZ54	TZ53	TZ52	TZ51	TZ50
Default	0	0	0	0	0	0	0	0

Bits 15 to 8: Transmit Z6 Byte (TZ6[7:0]) – These eight bits are the Z6 byte to be inserted into the transmit PLCP frame (This bits are unused in E3 mode).

Bits 7 to 0: Transmit Z5 Byte (TZ5[7:0]) – These eight bits are the Z5 byte to be inserted into the transmit PLCP frame (This bits are unused in E3 mode).

12.12.2 Receive Side PLCP Register Map

The receive side utilizes thirteen registers.

Table 12-44. Receive Side PLCP Register Map

Address	Register	Register Description
(1,3,5,7)60h	PLCP.RCR	PLCP Receive Control Register
(1,3,5,7)62h	--	Unused
(1,3,5,7)64h	PLCP.RSR1	PLCP Receive Status Register #1
(1,3,5,7)66h	PLCP.RSR2	PLCP Receive Status Register #2
(1,3,5,7)68h	PLCP.RSRL1	PLCP Receive Status Register Latched #1
(1,3,5,7)6Ah	PLCP.RSRL2	PLCP Receive Status Register Latched #2
(1,3,5,7)6Ch	PLCP.RSRIE1	PLCP Receive Status Register Interrupt Enable #1
(1,3,5,7)6Eh	PLCP.RSRIE2	PLCP Receive Status Register Interrupt Enable #2
(1,3,5,7)70h	PLCP.RFECR	PLCP Receive Framing Error Count Register
(1,3,5,7)72h	PLCP.RPECR	PLCP Receive P-bit Parity Error Count Register
(1,3,5,7)74h	PLCP.RPECR	PLCP Receive REI Error Count Register
(1,3,5,7)76h	PLCP.RFGBR	PLCP Receive F1 and G1 Byte Register
(1,3,5,7)78h	PLCP.RM12BR	PLCP Receive M1 and M2 Byte Register
(1,3,5,7)7Ah	PLCP.RZ12BR	PLCP Receive Z1 and Z2 Byte Register
(1,3,5,7)7Ch	PLCP.RZ34BR	PLCP Receive Z3 and Z4 Byte Register
(1,3,5,7)7Eh	PLCP.RZ56BR	PLCP Receive Z5 and Z6 Byte Register

12.12.2.1 Register Bit Descriptions

Register Name: **PLCP.RCR**
Register Description: **PLCP Receive Control Register**
Register Address: **(1,3,5,7)60h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	RHSC1	RHSC0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	RLIE	--	PECC	FEPD	FECC	ECC	FRSYNC
Default	0	0	0	0	0	0	0	0

Bits 9 to 8: Receive HDLC Source Control (RHSC[1:0]) – These two bits control the source of the receive HDLC controller.

00 = F1 byte.
01 = M1 byte.
10 = M2 byte.
11 = M2 and M1 byte.

Bit 6: Receive LOF Integration Enable (RLIE) – When 0, the receive Loss Of Frame (LOF) integration counter is disabled. When 1, the receive LOF integration counter is enabled.

Bit 4: Parity Error Count Control (PECC) – When 0, BIP-8 (B1 byte) bit errors are detected (up to 8 per frame). When 1, BIP-8 block errors are detected (no more than one per frame). Note: The transmit REI bits are affected by the setting of this bit as the REI bits reflect the number of BIP-8 errors detected/counted.

Bit 3: Framing Error POI Disable (FEPD) – When 0, Path Overhead Indicator (POI) byte (P#) and framing alignment byte (A1 & A2) errors are detected. When 1, only A1 & A2 errors are detected. Note: This bit is ignored when OOF events are counted (FECC=1)

Bit 2: Framing Error Count Control (FECC) – This bit controls the type of framing error events that are counted. When 0, A1 byte errors, A2 byte errors, and P# byte errors (up to 3 per subframe) are counted. When 1, OOF events are counted.

Bit 1: Error Count Control (ECC) – When 0, framing errors, BIP-8 parity errors, and REI errors will not be counted during an OOF condition (BIP-8 parity error counting will resume in the second full frame after an OOF condition is cleared). When 1, framing errors, BIP-8 parity errors, and REI errors will be counted during an OOF condition.

Bit 0: Force Framer Resynchronization (FRSYNC) – A 0 to 1 transition forces the framer into the "Search state. Once the framer acquires lock, the data path frame counters will be updated regardless of whether an OOF condition exists or not. The bit must be cleared and set to one again to force another resynchronization

Register Name: **PLCP.RSR1**
Register Description: **PLCP Receive Status Register #1**
Register Address: **(1,3,5,7)64h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	LOF

Bit #	7	6	5	4	3	2	1	0
Name	--	--	REIC	PEC	FEC	RAI	--	OOF

Bit 8: Loss Of Frame (LOF) – When 0, the receive line interface is not in a loss of frame (LOF) condition. When 1, the receive line interface is in an LOF condition.

Bit 5: Remote Error Indication Count (REIC) – When 0, the remote error indication count is zero. When 1, the remote error indication count is one or more.

Bit 4: Parity Error Count (PEC) – When 0, the parity error count is zero. When 1, the parity error count is one or more.

Bit 3: Framing Error Count (FEC) – When 0, the framing error count is zero. When 1, the framing error count is one or more.

Bit 2: Remote Alarm Indication (RAI) – This bit indicates the current state of the remote alarm indication (RAI) which is the fifth bit of the G1 byte (G1[5]).

Bit 0: Out Of Frame (OOF) – When 0, the receive frame processor is not in an out of frame (OOF) condition. When 1, the receive frame processor is in an OOF condition.

Register Name: **PLCP.RSR2**
Register Description: **PLCP Receive Status Register #2**
Register Address: **(1,3,5,7)66h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	--	--	LSSU

Bit 0: Receive Link Status Signal Unstable (LSSU) – When 0, the receive link states signal is stable. When 1, the receive link states signal is unstable.

Register Name: **PLCP.RSRL1**
Register Description: **PLCP Receive Status Register Latched #1**
Register Address: **(1,3,5,7)68h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	REIL	PEL	FEL	--	--	LOFL

Bit #	7	6	5	4	3	2	1	0
Name	--	--	REICL	PECL	FECL	RAIL	COFAL	OOFL

Bit 13: Remote Error Indication Latched (REIL) – This bit is set when a far-end block error is detected.

Bit 12: Parity Error Latched (PEL) – This bit is set when a BIP-8 parity error is detected.

Bit 11: Framing Error Latched (FEL) – This bit is set when a framing error is detected.

Bit 8: Loss Of Frame Change Latched (LOFL) – This bit is set when the LOF bit changes state.

Bit 5: Remote Error Indication Count Latched (REICL) – This bit is set when the REIC bit transitions from zero to one.

Bit 4: Parity Error Count Latched (PECL) – This bit is set when the PEC bit transitions from zero to one.

Bit 3: Framing Error Count Latched (FECL) – This bit is set when the FEC bit transitions from zero to one.

Bit 2: Remote Defect Indication Change Latched (RAIL) – This bit is set when the RAI bit changes state.

Bit 1: Change Of Frame Alignment Latched (COFAL) – This bit is set when the data path frame counters are updated with a new frame alignment that is different from the previous frame alignment.

Bit 0: Out Of Frame Change Latched (OOFL) – This bit is set when the OOF bit changes state.

Register Name: **PLCP.RSRL2**
Register Description: **PLCP Receive Status Register Latched #2**
Register Address: **(1,3,5,7)6Ah**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	RZ6L	RZ5L	RZ4L

Bit #	7	6	5	4	3	2	1	0
Name	RZ3L	RZ2L	RZ1L	RM2L	RM1L	RF1L	LSSL	LSSUL

Bit 10: Receive Z6 Byte Change Latched (RZ6L) – This bit is set when the RZ6[7:0] bits change state (This bit is zero in E3 mode).

Bit 9: Receive Z5 Byte Change Latched (RZ5L) – This bit is set when the RZ5[7:0] bits change state (This bit is zero in E3 mode).

Bit 8: Receive Z4 Byte Change Latched (RZ4L) – This bit is set when the RZ4[7:0] bits change state (This bit is zero in E3 mode).

Bit 7: Receive Z3 Byte Change Latched (RZ3L) – This bit is set when the RZ3[7:0] bits change state.

Bit 6: Receive Z2 Byte Change Latched (RZ2L) – This bit is set when the RZ2[7:0] bits change state.

Bit 5: Receive Z1 Byte Change Latched (RZ1L) – This bit is set when the RZ1[7:0] bits change state.

Bit 4: Receive M2 Byte Change Latched (RM2L) – This bit is set when the RM2[7:0] bits change state.

Bit 3: Receive M1 Byte Change Latched (RM1L) – This bit is set when the RM1[7:0] bits change state.

Bit 2: Receive F1 Byte Change Latched (RF1L) – This bit is set when the RF1[7:0] bits change state.

Bit 1: Receive Link Status Signal Change Latched (LSSL) – This bit is set when the LSS[2:0] bits change state.

Bit 0: Receive Link Status Signal Unstable Change Latched (LSSUL) – This bit is set when the LSSU bit changes state.

Register Name: **PLCP.RSRIE1**
Register Description: **PLCP Receive Status Register Interrupt Enable #1**
Register Address: **(1,3,5,7)6Ch**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	REIIE	PEIE	FEIE	--	--	LOFIE
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	REICIE	PECIE	FECIE	RAIIE	COFAIE	OOFIE
Default	0	0	0	0	0	0	0	0

Bit 13: Remote Error Indication Interrupt Enable (REIIE) – This bit enables an interrupt if the REIL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 12: Parity Error Interrupt Enable (PEIE) – This bit enables an interrupt if the PEL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 11: Framing Error Interrupt Enable (FEIE) – This bit enables an interrupt if the FEL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 8: Loss Of Frame Interrupt Enable (LOFIE) – This bit enables an interrupt if the LOFL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 5: Remote Error Indication Count Interrupt Enable (REICIE) – This bit enables an interrupt if the REICL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 4: Parity Error Count Interrupt Enable (PECIE) – This bit enables an interrupt if the PECL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 3: Framing Error Count Interrupt Enable (FECIE) – This bit enables an interrupt if the FECL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 2: Remote Defect Indication Interrupt Enable (RAIIE) – This bit enables an interrupt if the RAIL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 1: Change Of Frame Alignment Interrupt Enable (COFAIE) – This bit enables an interrupt if the COFAL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Out Of Frame Interrupt Enable (OOFIE) – This bit enables an interrupt if the OOFL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **PLCP.RSRIE2**
Register Description: **PLCP Receive Status Register Interrupt Enable #2**
Register Address: **(1,3,5,7)6Eh**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	RZ6IE	RZ5IE	RZ4IE
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RZ3IE	RZ2IE	RZ1IE	RM2IE	RM1IE	RF1IE	LSSIE	LSSUIE
Default	0	0	0	0	0	0	0	0

Bit 10: Receive Z6 Byte Interrupt Enable (RZ6IE) – This bit enables an interrupt if the RZ6L bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set. (This bit is unused in E3 mode).

0 = interrupt disabled
1 = interrupt enabled

Bit 9: Receive Z5 Byte Interrupt Enable (RZ5IE) – This bit enables an interrupt if the RZ5L bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set. (This bit is unused in E3 mode).

0 = interrupt disabled
1 = interrupt enabled

Bit 8: Receive Z4 Byte Interrupt Enable (RZ4IE) – This bit enables an interrupt if the RZ4L bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set. (This bit is unused in E3 mode).

0 = interrupt disabled
1 = interrupt enabled

Bit 7: Receive Z3 Byte Interrupt Enable (RZ3IE) – This bit enables an interrupt if the RZ3L bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 6: Receive Z2 Byte Interrupt Enable (RZ2IE) – This bit enables an interrupt if the RZ2L bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 5: Receive Z1 Byte Interrupt Enable (RZ1IE) – This bit enables an interrupt if the RZ1L bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 4: Receive M2 Byte Interrupt Enable (RM2IE) – This bit enables an interrupt if the RM2L bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 3: Receive M1 Byte Interrupt Enable (RM1IE) – This bit enables an interrupt if the RM1L bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 2: Receive F1 Byte Interrupt Enable (RF1IE) – This bit enables an interrupt if the RF1L bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 1: Receive Link Status Signal Interrupt Enable (LSSIE) – This bit enables an interrupt if the LSSL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Receive Link Status Signal Unstable Interrupt Enable (LSSUIE) – This bit enables an interrupt if the LSSUL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **PLCP.RFECR**
Register Description: **PLCP Receive Framing Error Count Register**
Register Address: **(1,3,5,7)70h**

Bit #	15	14	13	12	11	10	9	8
Name	FE15	FE14	FE13	FE12	FE11	FE10	FE9	FE8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Framing Error Count (FE[15:0]) – These sixteen bits indicate the number of framing error events on the incoming PLCP data stream. This register is updated via the PMU signal (see Section 10.4.5).

Register Name: **PLCP.RPECR**
Register Description: **PLCP Receive Parity Error Count Register**
Register Address: **(1,3,5,7)72h**

Bit #	15	14	13	12	11	10	9	8
Name	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Parity Error Count (PE[15:0]) – These sixteen bits indicate the number of parity (BIP-8) errors detected on the incoming PLCP data stream. This register is updated via the PMU signal (see Section 10.4.5).

Register Name: **PLCP.RREICR**
Register Description: **PLCP Receive Remote Error Indication Count Register**
Register Address: **(1,3,5,7)74h**

Bit #	15	14	13	12	11	10	9	8
Name	REI15	REI14	REI13	REI12	REI11	REI10	REI9	REI8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	REI7	REI6	REI5	REI4	REI3	REI2	REI1	REI0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Remote Error Indication Count (REI[15:0]) – These sixteen bits indicate the number of remote error indication errors detected on the incoming PLCP data stream. This register is updated via the PMU signal (see Section 10.4.5).

Register Name: **PLCP.RFGBR**
Register Description: **PLCP Receive F1 and G1 Byte Register**
Register Address: **(1,3,5,7)76h**

Bit #	15	14	13	12	11	10	9	8
Name	RF17	RF16	RF15	RF14	RF13	RF12	RF11	RF10
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	LSS2	LSS1	LSS0
Default	0	0	0	0	0	0	0	0

Bits 15 to 8: Receive F1 Byte (RF1[7:0]) – These eight bits are the integrated version of the F1 byte as extracted from the receive PLCP frame.

Bits 2 to 0: Receive Link Status Signal (LSS[2:0]) – These three bits are the integrated version of the receive link status signal (G1[6:8]) as extracted from the receive PLCP frame.

Register Name: **PLCP.RM12BR**
Register Description: **PLCP Receive M1 and M2 Byte Register**
Register Address: **(1,3,5,7)78h**

Bit #	15	14	13	12	11	10	9	8
Name	RM27	RM26	RM25	RM24	RM23	RM22	RM21	RM20
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RM17	RM16	RM15	RM14	RM13	RM12	RM11	RM10
Default	0	0	0	0	0	0	0	0

Bits 15 to 8: Receive M2 Byte (RM2[7:0]) – These eight bits are the integrated version of the M2 byte as extracted from the receive PLCP frame.

Bits 7 to 0: Receive M1 Byte (RM1[7:0]) – These eight bits are the integrated version of the M1 byte as extracted from the receive PLCP frame.

Register Name: **PLCP.RZ12BR**
Register Description: **PLCP Receive Z1 and Z2 Byte Register**
Register Address: **(1,3,5,7)7Ah**

Bit #	15	14	13	12	11	10	9	8
Name	RZ27	RZ26	RZ25	RZ24	RZ23	RZ22	RZ21	RZ20
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RZ17	RZ16	RZ15	RZ14	RZ13	RZ12	RZ11	RZ10
Default	0	0	0	0	0	0	0	0

Bits 15 to 8: Receive Z2 Byte (RZ2[7:0]) – These eight bits are the integrated version of the Z2 byte as extracted from the receive PLCP frame.

Bits 7 to 0: Receive Z1 Byte (RZ1[7:0]) – These eight bits are the integrated version of the Z1 byte as extracted from the receive PLCP frame.

Register Name: **PLCP.RZ34BR**
Register Description: **PLCP Receive Z3 and Z4 Byte Register**
Register Address: **(1,3,5,7)7Ch**

Bit #	15	14	13	12	11	10	9	8
Name	RZ47	RZ46	RZ45	RZ44	RZ43	RZ42	RZ41	RZ40
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RZ37	RZ36	RZ35	RZ34	RZ33	RZ32	RZ31	RZ30
Default	0	0	0	0	0	0	0	0

Bits 15 to 8: Receive Z4 Byte (RZ4[7:0]) – These eight bits are the integrated version of the Z4 byte as extracted from the receive PLCP frame (This bits are zero in E3 mode).

Bits 7 to 0: Receive Z3 Byte (RZ3[7:0]) – These eight bits are the integrated version of the Z3 byte as extracted from the receive PLCP frame.

Register Name: **PLCP.RZ56BR**
Register Description: **PLCP Receive Z5 and Z6 Byte Register**
Register Address: **(1,3,5,7)7Eh**

Bit #	15	14	13	12	11	10	9	8
Name	RZ67	RZ66	RZ65	RZ64	RZ63	RZ62	RZ61	RZ60
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RZ57	RZ56	RZ55	RZ54	RZ53	RZ52	RZ51	RZ50
Default	0	0	0	0	0	0	0	0

Bits 15 to 8: Receive Z6 Byte (RZ6[7:0]) – These eight bits are the integrated version of the Z6 byte as extracted from the receive PLCP frame (This bits are zero in E3 mode).

Bits 7 to 0: Receive Z5 Byte (RZ5[7:0]) – These eight bits are the integrated version of the Z5 byte as extracted from the receive PLCP frame (This bits are zero in E3 mode).

12.13 FIFO Registers

12.13.1 Transmit FIFO Register Map

The transmit FIFO block has five registers.

Table 12-45. Transmit FIFO Register Map

Address	Register	Register Description
(1,3,5,7)80h	FF.TCR	FIFO Transmit Control Register
(1,3,5,7)82h	FF.TLCR	FIFO Transmit Level Control Register
(1,3,5,7)84h	FF.TPAC	FIFO Transmit Port Address Control Register
(1,3,5,7)86h	--	Unused
(1,3,5,7)88h	FF.TSRL	FIFO Transmit Status Register Latched
(1,3,5,7)8Ah	FF.TSRIE	FIFO Transmit Status Register Interrupt Enable
(1,3,5,7)8Ch	--	Unused
(1,3,5,7)8Eh	--	Unused

12.13.1.1 Register Bit Descriptions

Register Name: **FF.TCR**
Register Description: **FIFO Transmit Control Register**
Register Address: **(1,3,5,7)80h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	--	--	TFRST
Default	0	0	0	0	0	0	0	1

Bit 0: Transmit FIFO Reset (TFRST) – When 0, the Transmit FIFO will resume normal operations, however, data is discarded until a start of packet/cell is received after RAM power-up is completed. When 1, the Transmit FIFO is emptied, any transfer in progress is halted, the FIFO RAM is powered down, the associated TDXA is forced low, and all incoming data is discarded. If the port was selected when the reset was initiated, the port will be deselected, and must be reselected ($\overline{\text{TEN}}$ deasserted with address on TADR or TSX asserted with address on TDATA) before any transfer will occur.

Register Name: **FF.TLCR**
Register Description: **FIFO Transmit Level Control Register**
Register Address: **(1,3,5,7)82h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	TFAE5	TFAE4	TFAE3	TFAE2	TFAE1	TFAE0
Default	0	0	0	1	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	TFAF5	TFAF4	TFAF3	TFAF2	TFAF1	TFAF0
Default	0	0	0	1	0	0	0	0

Bits 13 to 8: Transmit FIFO Almost Empty Level (TFAE[5:0]) – In POS-PHY packet processing mode, these six bits indicate the maximum number of four byte groups that can be stored in the Transmit FIFO for it to be considered "almost empty". E.g., a value of 30 (1Eh) results in the FIFO being "almost empty" when it contains 120 (78h) bytes or less. In cell processing mode, these bits are ignored.

Bits 5 to 0: Transmit FIFO Almost Full Level (TFAF[5:0]) – In POS-PHY packet processing mode, these six bits indicate the maximum number of four byte groups that can be available in the Transmit FIFO for it to be considered "almost full". E.g., a value of 30 (1Eh) results in the FIFO being "almost full" when it has 120 (78h) bytes or less available. In cell processing mode, TFAF[5:2] are ignored, and TFAF[1:0] indicate the maximum number of cells that can be available in the Transmit FIFO for it to be considered "almost full".

Register Name: **FF.TPAC**
Register Description: **FIFO Transmit Port Address Control Register**
Register Address: **(1,3,5,7)84h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	TPA4	TPA3	TPA2	TPA1	TPA0
Default	0	0	0	0	0	0	0	0

Bits 4 to 0: Transmit FIFO System Port Address (TPA[4:0]) – These five bits set the Transmit FIFO system interface port address used to poll the Transmit FIFO for fill status, and select it for data transfer. In Level 2 mode, if bits TPA[4:0] are set to a value of 1Fh, the port is disabled.

Register Name: **FF.TSRL**
Register Description: **FIFO Transmit Status Register Latched**
Register Address: **(1,3,5,7)88h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	TFATL	TFSTL	TFITL	TFUL	TFOL

Bit 4: Transmit FIFO Aborted Transfer Latched (TFATL) – This bit is set when a transfer is aborted. An aborted transfer does not occur in UTOPIA mode. In POS-PHY mode, an aborted transfer occurs when a packet error (a transfer with TERR and TEOP asserted) occurs. An aborted transfer is stored in the transmit FIFO with an abort indication.

Bit 3: Transmit FIFO Short Transfer Latched (TFSTL) – This bit is set when a "short transfer" is received. In UTOPIA mode, a "short transfer" occurs when a start of cell (a transfer with TSOC asserted) occurs before the previous cell transfer has been completed. In POS-PHY mode, a "short transfer" occurs when a start of packet (a transfer with TSOP asserted) occurs after a previous start of packet, but before an end of packet (a transfer with TEOP asserted). In UTOPIA mode, the short transfer data is discarded. In POS-PHY mode, a short transfer is stored in the transmit FIFO with an abort indication.

Bit 2: Transmit FIFO Invalid Transfer Latched (TFITL) – This bit is set when an "invalid transfer" is initiated. In UTOPIA mode, an "invalid transfer" occurs when additional cell data is transferred after the last transfer of a cell and before a transfer with TSOC asserted. In POS-PHY mode, an "invalid transfer" occurs when packet data is transferred after an end of packet, but before a start of packet (this includes another end of packet transfer). The invalid transfer data is discarded.

Bit 1: Transmit FIFO Underflow Latched (TFUL) – This bit is set when a Transmit FIFO underflow condition occurs. An underflow condition results in a loss of data.

Bit 0: Transmit FIFO Overflow Latched (TFOL) – This bit is set when a Transmit FIFO overflow condition occurs. An overflow condition results in a loss of data.

Register Name: **FF.TSRIE**
Register Description: **FIFO Transmit Status Register Interrupt Enable**
Register Address: **(1,3,5,7)8Ah**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	TFATIE	TFSTIE	TFITIE	TFUIE	TFOIE
Default	0	0	0	0	0	0	0	0

Bit 4: Transmit FIFO Aborted Transfer Interrupt Enable (TFATIE) – This bit enables an interrupt if the TFATL bit in the *FF.TSRL* register is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 3: Transmit FIFO Short Transfer Interrupt Enable (TFSTIE) – This bit enables an interrupt if the TFSTL bit in the *FF.TSRL* register is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 2: Transmit FIFO Invalid Transfer Interrupt Enable (TFITIE) – This bit enables an interrupt if the TFITL bit in the *FF.TSRL* register is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled
1 = interrupt enabled

Bit 1: Transmit FIFO Underflow Interrupt Enable (TFUIE) – This bit enables an interrupt if the TFUL bit in the *FF.TSRL* register is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Transmit FIFO Overflow Interrupt Enable (TFOIE) – This bit enables an interrupt if the TFOL bit in the *FF.TSRL* register is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled

1 = interrupt enabled

12.13.2 Receive FIFO Register Map

The receive FIFO block has five registers.

Table 12-46. Receive FIFO Register Map

Address	Register	Register Description
(1,3,5,7)90h	FF.RCR	FIFO Receive Control Register
(1,3,5,7)92h	FF.RLCR	FIFO Receive Level Control Register
(1,3,5,7)94h	FF.RPAC	FIFO Receive Port Address Control Register
(1,3,5,7)96h	--	Unused
(1,3,5,7)98h	FF.RSRL	FIFO Receive Status Register Latched
(1,3,5,7)9Ah	FF.RSRIE	FIFO Receive Status Register Interrupt Enable
(1,3,5,7)9Ch	--	Unused
(1,3,5,7)9Eh	--	Unused

12.13.2.1 Register Bit Descriptions

Register Name: **FF.RCR**
Register Description: **FIFO Receive Control Register**
Register Address: **(1,3,5,7)90h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	--	--	RFRST
Default	0	0	0	0	0	0	0	1

Bit 0: Receive FIFO Reset (RFRST) – When 0, the Receive FIFO will resume normal operations, however, data is discarded until a start of packet/cell is received after RAM power-up is completed. When 1, the Receive FIFO is emptied, any transfer in progress is halted, the FIFO RAM is powered down, the associated RDXA signal is forced low, and all incoming data is discarded. If the port was selected when the reset was initiated, the port will be deselected, and must be reselected ($\overline{REN}$) deasserted with address on RADR or RSX asserted with address on RDATA) before any transfer will occur.

Register Name: **FF.RLCR**
Register Description: **FIFO Receive Level Control Register**
Register Address: **(1,3,5,7)92h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	RFAE5	RFAE4	RFAE3	RFAE2	RFAE1	RFAE0
Default	0	0	0	1	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	RFAF5	RFAF4	RFAF3	RFAF2	RFAF1	RFAF0
Default	0	0	0	1	0	0	0	0

Bits 13 to 8: Receive FIFO Almost Empty Level (RFAE[5:0]) – In POS-PHY packet processing mode, these six bits indicate the maximum number of four byte groups that can be stored in the Receive FIFO for it to be considered "almost empty". E.g., a value of 30 (1Eh) results in the FIFO being "almost empty" when it contains 120 (78h) bytes or less. In cell processing mode, RFAE[5:2] are ignored, and RFAE[1:0] indicate the maximum number of cells that can be stored in the Receive FIFO for it to be considered "almost empty".

Bits 5 to 0: Receive FIFO Almost Full Level (RFAF[5:0]) – In POS-PHY packet processing mode, these six bits indicate the maximum number of four byte groups that can be available in the Receive FIFO for it to be considered "almost full". E.g., a value of 30 (1Eh) results in the FIFO being "almost full" when it has 120 (78h) bytes or less available. In cell processing mode, these bits are ignored.

Register Name: **FF.RFPAC**
Register Description: **FIFO Receive Port Address Control Register**
Register Address: **(1,3,5,7)94h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	RPA4	RPA3	RPA2	RPA1	RPA0
Default	0	0	0	0	0	0	0	0

Bits 4 to 0: Receive FIFO System Port Address (RPA[4:0]) – These five bits set the Receive FIFO system interface port address used to poll the Receive FIFO for fill status, and select it for data transfer. Each port in the device must have a different port address. In Level 2 mode, if bits RPA[4:0] are set to a value of 1Fh, the port is disabled.

Register Name: **FF.RSRL**
Register Description: **FIFO Receive Status Register Latched**
Register Address: **(1,3,5,7)98h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	--	--	RFOL

Bit 0: Receive FIFO Overflow Latched (RFOL) – This bit is cleared when a logic one is written to this bit, and set when a Receive FIFO overflow condition occurs. An overflow condition results in a loss of data.

Register Name: **FF.RSRIE**
Register Description: **FIFO Receive Status Register Interrupt Enable**
Register Address: **(1,3,5,7)9Ah**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	--	--	RFOIE
Default	0	0	0	0	0	0	0	0

Bit 0: Receive FIFO Overflow Interrupt Enable (RFOIE) – This bit enables an interrupt if the RFOL bit in the *FF.RSRL* register is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled

1 = interrupt enabled

12.14 Cell/Packet Processor

12.14.1 Transmit Cell Processor Register Map

The transmit cell processor block has eleven registers. Note: These registers are shared with the transmit packet processors.

Table 12-47. Transmit Cell Processor Register Map

ADDRESS	REGISTER	REGISTER DESCRIPTION
(1,3,5,7)A0h	CP.TCR	Cell Processor Transmit Control Register
(1,3,5,7)A2h	--	Reserved
(1,3,5,7)A4h	CP.TECC	Cell Processor Transmit Erred Cell Control Register
(1,3,5,7)A6h	CP.THMRC	Cell Processor Transmit HEC Error Mask Control Register
(1,3,5,7)A8h	CP.THPC1	Cell Processor Transmit Header Pattern Control Register #1
(1,3,5,7)AAh	CP.THPC2	Cell Processor Transmit Header Pattern Control Register #2
(1,3,5,7)ACh	CP.TFPPC	Cell Processor Transmit Fill Cell Payload Pattern Control Register
(1,3,5,7)AEh	CP.TSR	Cell Processor Transmit Status Register
(1,3,5,7)B0h	CP.TSRL	Cell Processor Transmit Status Register Latched
(1,3,5,7)B2h	CP.TSRIE	Cell Processor Transmit Status Register Interrupt Enable
(1,3,5,7)B4h	CP.TCCR1	Cell Processor Transmit Cell Count Register #1
(1,3,5,7)B6h	CP.TCCR2	Cell Processor Transmit Cell Count Register #2
(1,3,5,7)B8h	--	Reserved
(1,3,5,7)BAh	--	Reserved
(1,3,5,7)BCh	--	Unused
(1,3,5,7)BEh	--	Unused

12.14.1.1 Register Bit Descriptions

Register Name: **CP.TCR**
Register Description: **Cell Processor Transmit Control Register**
Register Address: **(1,3,5,7)A0h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	TDSE	TDHE	THPE	TCPAD
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	TFCH	TFCP	THSE	TSD	TBRE	TCPD
Default	0	0	0	0	0	0	0	0

Bit 11: Transmit DSS Scrambling Enable (TDSE) – When 0, self-synchronous scrambling is enabled. When 1, DSS scrambling is enabled. DSS mode is only applicable for un-framed or clear channel framing and bit synchronous modes. This bit is ignored if scrambling is disabled. Note: In byte synchronous and cell pass-through modes self-synchronous scrambling is enabled regardless of the setting of this bit.

Bit 10: Transmit DQDB HEC Processing Enable (TDHE) – When 0, the HEC is calculated over all four-header bytes. When 1, only the last three header bytes are used for HEC calculation.

Bit 9: Transmit HEC Pass-through Enable (THPE) – When 0, the calculated HEC byte will overwrite the HEC byte in the cell. When 1, the HEC byte in the cell is passed through. Note: The calculated HEC is always inserted into cells that are received without a HEC byte.

Bit 8: Transmit HEC Coset Polynomial Addition Disable (TCPAD) – When 0, the HEC coset polynomial addition is performed prior to inserting the HEC byte. When 1, HEC coset polynomial addition is disabled

Bit 5: Transmit Fill Cell Header Type (TFCH) – When 0, an idle cell header (00 00 00 01h) will be used in fill cells. When 1, a programmable header will be used in fill cells. The setting of this bit does not affect the contents of the cell payload bytes.

Bit 4: Transmit Fill Cell Payload Type (TFCP) – When 0, an idle cell payload byte (6Ah) will be used in each payload byte fill cells. When 1, a programmable cell payload byte will be used in each payload byte fill cells. The setting of this bit does not affect the contents of the cell header bytes.

Bit 3: Transmit Cell Header Scrambling Enable (THSE) – When 0, only the cell payload will be scrambled. When 1, the entire data stream (cell header and payload) is scrambled. This bit is ignored if scrambling is disabled, or DSS scrambling is enabled. When cell pass-through mode is enabled, the entire data stream will be scrambled if scrambling is enabled.

Bit 2: Transmit Scrambling Disable (TSD) – When 0, scrambling is performed. When 1, scrambling is disabled.

Bit 1: Transmit Bit Reordering Enable (TBRE) – When 0, bit reordering is disabled (The first bit transmitted is from the MSB of the transmit FIFO byte TFD[7]). When 1, bit reordering is enabled (The first bit transmitted is from the LSB of the transmit FIFO byte TFD[0]).

Bit 0: Transmit Pass-Through Enable (TPTE) – When 0, pass-through mode is disabled and cell processing is enabled. When 1, all cell processing functions except scrambling and bit reordering are disabled and the cell processor is in pass-through mode.

Register Name: **CP.TECC**
Register Description: **Cell Processor Transmit Errored Cell Control Register**
Register Address: **(1,3,5,7)A4h**

Bit #	15	14	13	12	11	10	9	8
Name	MEIMS	TCER6	TCER5	TCER4	TCER3	TCER2	TCER1	TCER0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	TCEN7	TCEN6	TCEN5	TCEN4	TCEN3	TCEN2	TCEN1	TCEN0
Default	0	0	0	0	0	0	0	0

Bit 15: Manual Error Insert Mode Select (MEIMS) – When 0, the transmit manual error insertion signal (TMEI) will not cause errors to be inserted. When 1, TMEI will causes an error to be inserted when it transitions from a 0 to a 1. Note: Enabling TMEI does not disable error insertion using TCER[6:0] and TCEN[7:0].

Manual error insertion is available at the global level, but not on a per port basis for the cell processor. (PORT.CR1.MEIM must be set for global error insertion to insert a packet error.)

Bits 14 to 8: Transmit Errored Cell Insertion Rate (TCER[6:0]) – These seven bits indicate the rate at which errored cells are to be output. One out of every $x * 10^y$ cells is to be an errored cell. TCER[3:0] is the value x, and TCER[6:4] is the value y, which has a maximum value of 6. If TCER[3:0] has a value of 0h errored cell insertion is disabled. If TCER[6:4] has a value of 6xh or 7xh the errored cell rate will be $x * 10^6$. A TCER[6:0] value of 01h results in every cell being errored. A TCER[6:0] value of 0Fh results in every 15^{th} cell being errored. A TCER[6:0] value of 11h results in every 10^{th} cell being errored. Errored cell insertion starts when the TECC register is written with a TCER[3:0] value that is non-zero. If the TECC register is written to during the middle of an errored cell insertion process, the current process is halted, and a new process will be started using the new values of TCER[6:0] and TCEN[7:0}. Errored cell insertion ends when TCEN[7:0] errored cells have been transmitted.

TCER[3:0] - X	TCER[6:4] - Y	TCER[6:0]	ERROR RATE ($x * 10^y$)
0h	XXh	X0h	DISABLED
1h	0Xh	01h	1 out of 1 cells
Fh	0Xh	0Fh	1 out of 15 cells
1h	1Xh	11h	1 out of 10 cells
1h	6Xh	61h	1 out of 10^6 cells
1h	7Xh	71h	1 out of 10^6 cells

Bits 7 to 0: Transmit Errored Cell Insertion Number (TCEN[7:0]) – These eight bits indicate the total number of errored cells to be transmitted. A value of FFh results in continuous errored cell insertion at the specified rate.

Register Name: **CP.THMRC**
Register Description: **Cell Processor Transmit HEC Error Mask Control Register**
Register Address: **(1,3,5,7)A6h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	THEM7	THEM6	THEM5	THEM4	THEM3	THEM2	THEM1	THEM0
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Transmit HEC Error Mask (THEM[7:0]) –These bits control the error insertion into the HEC byte. Setting these bits will corrupt the associated HEC bit during cell error insertion. Based on the value set in this register, the far end will detect three types of errors: an error in the HEC, a single bit error in the header, or multiple bit errors in the header. Default (THEM[7:0] = 00h) is no error inserted. If a single bit error is selected, the table below also shows which bit of the 32-bit HEC header will be corrupted. Table 12-48 indicates the type of error inserted by a specific mask value. Note: If a single bit error is inserted in the HEC, and the far-end has single bit error correction enabled, this will cause the indicated header bit to be corrupted.

Table 12-48. HEC Error Mask

Value	Error Type	Bit	Value	Error Type	Bit	Value	Error Type	Bit
01h-02h	HEC	–	32h-37h	Multi	–	87h-88h	Multi	–
03h	Multi	-	38h	Single	29	89h	Single	25
04h	HEC	–	39h-3Fh	Multi	–	90h-9Ah	Multi	–
05h-06h	Multi	–	40h	HEC	–	9Bh	Single	02
07h	Single	32	41h-42h	Multi	–	9Ch-A1h	Multi	–
08h	HEC	–	43h	Single	11	A2h	Single	12
09h-0Ah	Multi	–	44h-50h	Multi	–	A3h-A7h	Multi	–
0Bh	Single	09	51h	Single	13	A8h	Single	21
0Ch-0Dh	Multi	–	52h-53h	Multi	–	A9h-AAh	Multi	–
0Eh	Single	31	54h	Single	22	ABh	Single	14
0Fh	Multi	–	55h-56h	Multi	–	ACh-ADh	Multi	–
10h	HEC	–	57h	Single	20	AEh	Single	19
11h-14h	Multi	–	58h	Single	06	AFh	Multi	–
15h	Single	24	59h-5Ah	Multi	–	B0h	Single	05
16h	Single	08	5Bh	Single	18	B1h-B5h	Multi	–
17h-1Dh	Multi	–	5Ch-66h	Multi	–	B6h	Single	17
1Eh	Single	30	67h	Single	04	B7h-C6h	Multi	–
1Fh	Multi	–	68h-6Ah	Multi	–	C7h	Single	26
20h	HEC	–	6Bh	Single	16	C8h-CDh	Multi	–
21h-29h	Multi	–	6Ch-6Fh	Multi	–	CEh	Single	03
2Ah	Single	23	70h	Single	28	CFh-D5h	Multi	–
2Bh	Multi	–	71h-7Fh	Multi	–	D6h	Single	15
2Ch	Single	07	80h	HEC	–	D7h-DFh	Multi	–
2Dh-30h	Multi	–	81h-85h	Multi	–	E0h	Single	27
31h	Single	01	86h	Single	10	E1h-FFh	Multi	–

Register Name: **CP.THPC1**
Register Description: **Cell Processor Transmit Header Pattern Control Register #1**
Register Address: **(1,3,5,7)A8h**

Bit #	15	14	13	12	11	10	9	8
Name	THP15	THP14	THP13	THP12	THP11	THP10	THP9	THP8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	THP7	THP6	THP5	THP4	THP3	THP2	THP1	THP0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Transmit Programmable Header Pattern (THP[15:0]) – Lower sixteen bits of 32 bits. Register description follows next register.

Register Name: **CP.THPC2**
Register Description: **Cell Processor Transmit Header Pattern Control Register #2**
Register Address: **(1,3,5,7)AAh**

Bit #	15	14	13	12	11	10	9	8
Name	THP31	THP30	THP29	THP28	THP27	THP26	THP25	THP24
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	THP23	THP22	THP21	THP20	THP19	THP18	THP17	THP16
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Transmit Programmable Header Pattern (THP[31:16]) Upper sixteen bits of 32 bits.

Transmit Programmable Header Pattern (THP[31:0]) – These thirty-two bits indicate the header bit pattern to be used in the header of fill cells when the *CP.TCR* register bit TFCH is set.

Register Name: **CP.TFPPC**
Register Description: **Cell Processor Transmit Fill Cell Payload Pattern Control Register**
Register Address: **(1,3,5,7)ACh**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	TFPP7	TFPP6	TFPP5	TFPP4	TFPP3	TFPP2	TFPP1	TFPP0
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Transmit Fill Cell Payload Pattern (TFPP[7:0]) – These eight bits indicate the value to be placed in the payload bytes of the fill cells when the *CP.TCR* register bit TFCP is set..

Register Name: **CP.TSR**
Register Description: **Cell Processor Transmit Status Register**
Register Address: **(1,3,5,7)AEh**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	--	--	TECF

Bit 0: Transmit Errored Cell Insertion Finished (TECF) – This bit is set when the number of errored cells indicated by the TCEN[7:0] bits in the TECC register have been transmitted. This bit is cleared when errored cell insertion is disabled, or a new errored cell insertion process is initiated.

Register Name: **CP.TSRL**
Register Description: **Cell Processor Transmit Status Register Latched**
Register Address: **(1,3,5,7)B0h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	--	--	TECFL

Bit 0: Transmit Errored Cell Insertion Finished Latched (TECFL) – This bit is set when the TECF bit in the *CP.TSR* register transitions from zero to one.

Register Name: **CP.TSRIE**
Register Description: **Cell Processor Transmit Status Register Interrupt Enable**
Register Address: **(1,3,5,7)B2h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	--	--	TECFIE
Default	0	0	0	0	0	0	0	0

Bit 0: Transmit Errored Cell Insertion Finished Interrupt Enable (TECFIE) – This bit enables an interrupt if the TECFL bit in the *CP.TSRL* register is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **CP.TCCR1**
Register Description: **Cell Processor Transmit Cell Count Register #1**
Register Address: **(1,3,5,7)B4h**

Bit #	15	14	13	12	11	10	9	8
Name	TCC15	TCC14	TCC13	TCC12	TCC11	TCC10	TCC9	TCC8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Transmit Cell Count (TCC[15:0]) – Lower sixteen bits of 24 bits. Register description follows next register.

Register Name: **CP.TCCR2**
Register Description: **Cell Processor Transmit Cell Count Register #2**
Register Address: **(1,3,5,7)B6h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	TCC23	TCC22	TCC21	TCC20	TCC19	TCC18	TCC17	TCC16
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Transmit Cell Count (TCC[23:16]) - Upper 8 bits of Register.

Transmit Cell Count (TCC[23:0]) – These twenty-four bits indicate the number of cells extracted from the Transmit FIFO and output in the outgoing data stream. This register is updated via the PMU signal (see Section 10.4.5).

12.14.2 Receive Cell Processor

The receive cell processor block has eighteen registers.

12.14.2.1 Register Map

Table 12-49. Receive Cell Processor Register Map

Address	Register	Register Description
(1,3,5,7)C0h	CP.RCR1	Cell Processor Receive Control Register #1
(1,3,5,7)C2h	--	Reserved
(1,3,5,7)C4h	CP.RHPC1	Cell Processor Receive Header Pattern Control Register #1
(1,3,5,7)C6h	CP.RHPC2	Cell Processor Receive Header Pattern Control Register #2
(1,3,5,7)C8h	CP.RHPMC1	Cell Processor Receive Header Pattern Mask Control Register #1
(1,3,5,7)CAh	CP.RHPMC2	Cell Processor Receive Header Pattern Mask Control Register #2
(1,3,5,7)CCh	CP.RLTC	Cell Processor Receive LCD Threshold Control Register
(1,3,5,7)CEh	CP.RCPSR	Cell Processor Receive Status Register
(1,3,5,7)D0h	CP.RCPSRL	Cell Processor Receive Status Register Latched
(1,3,5,7)D2h	CP.RCPSRIE	Cell Processor Receive Register Interrupt Enable
(1,3,5,7)D4h	CP.RCCR1	Cell Processor Receive Cell Count Register #1
(1,3,5,7)D6h	CP.RCCR2	Cell Processor Receive Cell Count Register #2
(1,3,5,7)D8h	CP.RECCR1	Cell Processor Receive Errored Cell Count Register #1
(1,3,5,7)DAh	CP.RECCR2	Cell Processor Receive Errored Cell Count Register #2
(1,3,5,7)DCh	CP.RHPCR1	Cell Processor Receive Header Pattern Count Register #1
(1,3,5,7)DEh	CP.RHPCR2	Cell Processor Receive Header Pattern Count Register #2
(1,3,5,7)E0h	CP.RCCCR1	Cell Processor Receive Corrected Cell Count Register #1
(1,3,5,7)E2h	CP.RCCCR2	Cell Processor Receive Corrected Cell Count Register #2
(1,3,5,7)E4h	CP.RFCCR1	Cell Processor Receive Filtered Cell Count Register #1
(1,3,5,7)E6h	CP.RFCCR2	Cell Processor Receive Filtered Cell Count Register #2
(1,3,5,7)E8h	--	Reserved
(1,3,5,7)EAh	--	Reserved
(1,3,5,7)ECh	--	Reserved
(1,3,5,7)EEh	--	Reserved
(1,3,5,7)F0h	--	Unused
(1,3,5,7)F2h	--	Unused
(1,3,5,7)F4h	--	Unused
(1,3,5,7)F6h	--	Unused
(1,3,5,7)F8h	--	Unused
(1,3,5,7)FAh	--	Unused
(1,3,5,7)FCh	--	Unused
(1,3,5,7)FEh	--	Unused

12.14.2.2 Register Bit Descriptions

Register Name: **CP.RCR1**
Register Description: **Cell Processor Receive Control Register #1**
Register Address: **(1,3,5,7)C0h**

Bit #	15	14	13	12	11	10	9	8
Name	RDDE	RDHE	RECED	RHPM1	RHPM0	RICFD	RUCFE	RICFE
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RROC1	RROC0	RCPAD	RHECD	RHDE	RDD	RBRE	RPTE
Default	0	0	0	0	0	0	0	0

Bit 15: Receive DSS De-scrambling Enable (RDDE) – When 0, self-synchronous de-scrambling is enabled. When 1, DSS de-scrambling is enabled. DSS mode is only applicable for un-framed or clear channel framing and bit synchronous modes. This bit is ignored if de-scrambling is disabled. Note: In byte synchronous and cell pass-through modes, self-synchronous de-scrambling is enabled regardless of the setting of this bit.

Bit 14: Receive DQDB HEC Processing Enable (RDHE) – When 0, the HEC is calculated over all four-header bytes. When 1, only the last three header bytes are used for HEC calculation.

Bit 13: Receive Errored Cell Extraction Disable (RECED) – When 0, errored cells are extracted. When 1, errored cells are passed on.

Bits 12 to 11: Receive Header Pattern Comparison Mode (RHPM[1:0]) – These two bits control the operation of the header pattern comparison function.

00 = Count match: Cells that match the header pattern are counted.
01 = Count no match - Cells that do not match the header pattern are counted.
10 = Discard match - Cells that match the header pattern are counted and discarded.
11 = Discard no match - Cells that do not match the header pattern are counted and discarded.

Bit 10: Receive Idle Cell Filtering Disable (RICFD) – When 0, idle cells are discarded. When 1, idle cells are passed on.

Bit 9: Receive Unassigned Cell Filtering Enable (RUCFE) – When 0, unassigned cells are passed on. When 1, unassigned cells are counted and discarded.

Bit 8: Receive Invalid Cell Filtering Enable (RICFE) – When 0, invalid cells are passed on. When 1, invalid cells are discarded.

Bits 7 to 6: Receive Error Monitoring Required OK Cells (RROC[1:0]) – These two bits indicate the number of good cells required to transition from the "Detection" state to the "Correction" state, which enables single bit correction of the header (see Figure 10-26).

00 = 1 good cell is required.
01 = 2 good cells are required.
10 = 4 good cells are required.
11 = 8 good cells are required.

Bit 5: Receive HEC Coset Polynomial Addition Disable (RCPAD) – When 0, the HEC coset polynomial addition is performed prior to checking the HEC byte. When 1, HEC coset polynomial addition is disabled

Bit 4: Receive Header Error Correction Disable (RHECD) – When 0, single bit header error correction is enabled. When 1, header error correction is disabled and all errors are treated as an uncorrectable error.

Bit 3: Receive Cell Header De-scrambling Enable (RHDE) – When 0, only the cell payload will be descrambled. When 1, the entire data stream (cell header and payload) is descrambled. This bit is ignored if de-scrambling is disabled or DSS de-scrambling is enabled. When cell pass-through mode is enabled, the entire data stream will be de-scrambled if de-scrambling is enabled.

Bit 2: Receive De-scrambling Disable (RDD) – When 0, de-scrambling is performed. When 1, de-scrambling is disabled.

Bit 1: Receive Bit Reordering Enable (RBRE) – When 0, bit reordering is disabled (The first bit received is stored in the MSB of the receive FIFO byte). When 1, bit reordering is enabled (The first bit received is stored in the LSB of the receive FIFO byte).

Bit 0: Receive Pass-Through Enable (RPTE) – When 0, pass-through mode is disabled and cell processing is enabled. When 1, the cell processor is in pass-through mode, and all cell processing functions except de-scrambling and bit reordering are disabled.

Register Name: **CP.RHPC1**
Register Description: **Cell Processor Receive Header Pattern Control Register #1**
Register Address: **(1,3,5,7)C4h**

Bit #	15	14	13	12	11	10	9	8
Name	RHP15	RHP14	RHP13	RHP12	RHP11	RHP10	RHP9	RHP8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RHP7	RHP6	RHP5	RHP4	RHP3	RHP2	RHP1	RHP0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Receive Header Pattern (RHP[15:0]) – Lower sixteen bits of 32 bits. Register description follows next register.

Register Name: **CP.RHPC2**
Register Description: **Cell Processor Receive Header Pattern Control Register #2**
Register Address: **(1,3,5,7)C6h**

Bit #	15	14	13	12	11	10	9	8
Name	RHP31	RHP30	RHP29	RHP28	RHP27	RHP26	RHP25	RHP24
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RHP23	RHP22	RHP21	RHP20	RHP19	RHP18	RHP17	RHP16
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Receive Header Pattern (RHP[31:16]) - Upper 16 bits of 32 bits.

Receive Header Pattern (RHP[31:0]) – These 32 bits indicate the receive header bit pattern to be detected by the header pattern comparison function.

Register Name: **CP.RHPMC1**
Register Description: **Cell Processor Receive Header Pattern Mask Control Register #1**
Register Address: **(1,3,5,7)C8h**

Bit #	15	14	13	12	11	10	9	8
Name	RHPD15	RHPD14	RHPD13	RHPD12	RHPD11	RHPD10	RHPD9	RHPD8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RHPD7	RHPD6	RHPD5	RHPD4	RHPD3	RHPD2	RHPD1	RHPD0
Default	0	0	0	0	0	0	0	0

Bit 15 to 0: Receive Header Pattern Comparison Disable (RHPD[15:0]) – Lower sixteen bits of 32 bits. Register description follows next register.

Register Name: **CP.RHPMC2**
Register Description: **Cell Processor Receive Header Pattern Mask Control Register #2**
Register Address: **(1,3,5,7)CAh**

Bit #	15	14	13	12	11	10	9	8
Name	RHPD31	RHPD30	RHPD29	RHPD28	RHPD27	RHPD26	RHPD25	RHPD24
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RHPD23	RHPD22	RHPD21	RHPD20	RHPD19	RHPD18	RHPD17	RHPD16
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Receive Header Pattern Comparison Disable (RHPD[31:16]) - Upper 16 bits of 32 bits.

Receive Header Pattern Comparison Disable (RHPD[31:0]) – These 32 bits indicate whether or not the associated header bit is checked by the header pattern comparison function. If RHPD[x] is high, the header bit x is ignored during the header pattern comparison (don't care). If RHPD[x] is low, the associated bit in the header must match RHP[x] in the receive header pattern control register RHPC.

Register Name: **CP.RLTC**
Register Description: **Cell Processor Receive LCD Threshold Control Register**
Register Address: **(1,3,5,7)CCh**

Bit #	15	14	13	12	11	10	9	8
Name	RLT15	RLT14	RLT13	RLT12	RLT11	RLT10	RLT9	RLT8
Default	0	0	0	0	0	0	0	1

Bit #	7	6	5	4	3	2	1	0
Name	RLT7	RLT6	RLT5	RLT4	RLT3	RLT2	RLT1	RLT0
Default	0	1	1	0	1	0	0	0

Bits 15 to 0: Receive LCD Threshold (RLT[15:0]) – These sixteen bits indicate the number of consecutive cell periods the cell delineation state machine must be in an Out of Cell Delineation (OCD) condition before it declares or terminate a Loss of Cell Delineation (LCD) condition. A value of 0000h causes LCD to be declared at the same time as OCD. The register has a default value after reset of 360 (decimal).

Register Name: **CP.RSR**
Register Description: **Cell Processor Receive Status Register**
Register Address: **(1,3,5,7)CEh**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	OOS	--	OCD	LCD

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	RECC	RHPC	RCHC

Bit 11: Out Of Sync (OOS) – This read only bit indicates that a DSS Out Of Sync (OOS) state exists. DSS OOS occurs when the DSS Scrambler Synchronization state machine is in the "Load" or "Verify" state, and DSS scrambling has been enabled.

Bit 9: Out Of Cell Delineation (OCD) – This read only bit indicates that an Out of Cell Delineation condition (OCD) exists. When DSS scrambling is disabled, OCD occurs when the HEC Error Monitoring state machine is in the "OCD" state. When DSS scrambling is enable, OCD occurs when the DSS OCD Detection state machine is in the "OCD" state.

Bit 8: Loss Of Cell Delineation (LCD) – This read only bit indicate that a Loss of Cell Delineation state exists. LCD occurs when OCD persists for the period programmed in the LCD threshold control register RLTC.

Bit 2: Receive Errored Header Cell Count (RECC) – This read only bit indicates that the receive errored header cell count is non-zero.

Bit 1: Receive Header Pattern Cell Count (RHPC) – This read only bit indicates that the receive header pattern comparison cell count is non-zero.

Bit 0: Receive Corrected Cell Count (RCHC) – This read only bit indicates that the receive corrected header cell count is non-zero.

Register Name: **CP.RSRL**
Register Description: **Cell Processor Receive Status Register Latched**
Register Address: **(1,3,5,7)D0h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	OOSL	COCDL	OCDCL	LCDCL

Bit #	7	6	5	4	3	2	1	0
Name	RECL	RCHL	RIDL	RUDL	RIVDL	RECCL	RHPCL	RCHCL

Bit 11: Out Of Sync Change Latched (OOSL) – This bit is set when the OOS bit in the *CP.RSR* register changes state.

Bit 10: Change Of Cell Delineation Latched (COCDL) – This bit is set when the data path cell counters are updated with a new cell delineation that is different from the previous cell delineation

Bit 9: Out Of Cell Delineation Change Latched (OCDCL) –.This bit is set when the OCD bit in the *CP.RSR* register changes state. Note: Immediately after a reset, this bit will be set to one.

Bit 8: Loss Of Cell Delineation Change Latched (LCDCL) – This bit is set when the LCD bit in the *CP.RSR* register changes state

Bit 7: Receive Errored Header Cell Latched (RECL) – This bit is set when a cell with an errored header is discarded.

Bit 6: Receive Corrected Header Cell Latched (RCHL) – This bit is set when a cell with a single header error is corrected.

Bit 5: Receive Idle Cell Detection Latched (RIDL) – This bit is set when an idle cell is discarded.

Bit 4: Receive Unassigned Cell Detection Latched (RUDL) – This bit is set when an unassigned cell is discarded.

Bit 3: Receive Invalid Cell Detection Latched (RIVDL) – This bit is set when an invalid cell is discarded.

Bit 2: Receive Errored Header Cell Count Latched (RECCL) – This bit is set when the RECC bit in the *CP.RSR* register transitions from zero to one.

Bit 1: Receive Header Pattern Cell Count Latched (RHPCL) – This bit is set when the RHPC bit in the *CP.RSR* register transitions from zero to one.

Bit 0: Receive Corrected Header Cell Count Latched (RCHCL) – This bit is set when the RCHC bit in the *CP.RSR* register transitions from zero to one.

Register Name: **CP.RSRIE**
Register Description: **Cell Processor Receive Status Register Interrupt Enable**
Register Address/Type: **(1,3,5,7)D2h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	OOSIE	COCDIE	OCDCIE	LCDCIE
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RECIE	RCHIE	RIDIE	RUDIE	RIVDIE	RECCIE	RHPCIE	RCHCIE
Default	0	0	0	0	0	0	0	0

Bit 11: Out Of Sync Change Interrupt Enable (OOSIE) – This bit enables an interrupt if the OOSL bit in the *CP.RSRL* register is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 10: Change Of Cell Delineation Interrupt Enable (COCDIE) – This bit enables an interrupt if the COCDL bit in the *CP.RSRL* register is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 9: Out Of Cell Delineation Change Interrupt Enable (OCDCIE) – This bit enables an interrupt if the OCDCL bit in the *CP.RSRL* register is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 8: Loss Of Cell Delineation Change Interrupt Enable (LCDCIE) – This bit enables an interrupt if the LCDCL bit in the *CP.RSRL* register is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 7: Receive Errored Header Cell Interrupt Enable (RECIE) – This bit enables an interrupt if the RECL bit in the CP.RSRL register is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 6: Receive Corrected Header Cell Interrupt Enable (RCHIE) – This bit enables an interrupt if the RCHL bit in the *CP.RSRL* register is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 5: Receive Idle Cell Detection Interrupt Enable (RIDIE) – This bit enables an interrupt if the RIDL bit in the *CP.RSRL* register is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 4: Receive Unassigned Cell Detection Interrupt Enable (RUDIE) – This bit enables an interrupt if the RUDL bit in the CP.RSRL register is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 3: Receive Invalid Cell Detection Interrupt Enable (RIVDIE) – This bit enables an interrupt if the RIVDL bit in the *CP.RSRL* register is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 2: Receive Errored Header Cell Count Interrupt Enable (RECCIE) – This bit enables an interrupt if the RECCL bit in the *CP.RSRL* register is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 1: Receive Header Pattern Cell Count Interrupt Enable (RHPCIE) – This bit enables an interrupt if the RHFCL bit in the CP.RSRL register is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Receive Corrected Header Cell Count Interrupt Enable (RCHCIE) – This bit enables an interrupt if the RCHCL bit in the *CP.RSRL* register is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **CP.RCCR1**
Register Description: **Cell Processor Receive Cell Count Register #1**
Register Address: **(1,3,5,7)D4h**

Bit #	15	14	13	12	11	10	9	8
Name	RCC15	RCC14	RCC13	RCC12	RCC11	RCC10	RCC9	RCC8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RCC7	RCC6	RCC5	RCC4	RCC3	RCC2	RCC1	RCC0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Receive Cell Count (RCC[15:0]) – Lower sixteen bits of 24 bits. Register description follows next register.

Register Name: **CP.RCCR2**
Register Description: **Cell Processor Receive Cell Count Register #2**
Register Address: **(1,3,5,7)D6h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RCC23	RCC22	RCC21	RCC20	RCC19	RCC18	RCC17	RCC16
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive Cell Count (RCC[23:16]) - Upper 8 bits of Register.

Receive Cell Count (RCC[23:0]) – These twenty-four bits indicate the number of cells stored in the receive FIFO. Note: Cells discarded due to system loopback or an overflow condition will be included in this count.

This register is updated via the PMU signal (see Section 10.4.5).

Register Name: **CP.RECCR1**
Register Description: **Cell Processor Receive Errored Header Count Register #1**
Register Address: **(1,3,5,7)D8h**

Bit #	15	14	13	12	11	10	9	8
Name	RECC15	RECC14	RECC13	RECC12	RECC11	RECC10	RECC9	RECC8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RECC7	RECC6	RECC5	RECC4	RECC3	RECC2	RECC1	RECC0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Receive Errored Header Count (RECC[15:0]) – Lower sixteen bits of 24 bits. Register description follows next register.

Register Name: **CP.RECCR2**
Register Description: **Cell Processor Receive Errored Header Count Register #2**
Register Address: **(1,3,5,7)DAh**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RECC23	RECC22	RECC21	RECC20	RECC19	RECC18	RECC17	RECC16
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive Errored Header Count (RECC[23:16])

Receive Errored Header Count (RECC[23:0]) – These twenty-four bits indicate the number of cells received with uncorrected header errors and discarded. If errored cell extraction is disabled, this count will be zero. Cells included in this count will not be included in any other count.

This register is updated via the PMU signal (see Section 10.4.5).

Register Name: **CP.RHPCR1**
Register Description: **Cell Processor Receive Header Pattern Cell Count Register #1**
Register Address: **(1,3,5,7)DCh**

Bit #	15	14	13	12	11	10	9	8
Name	RHPC15	RHPC14	RHPC13	RHPC12	RHPC11	RHPC10	RHPC9	RHPC8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RHPC7	RHPC6	RHPC5	RHPC4	RHPC3	RHPC2	RHPC1	RHPC0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Receive Header Pattern Comparison Cell Count (RHPC[15:0]) – Lower sixteen bits of 24 bits. Register description follows next register.

Register Name: **CP.RHPCR2**
Register Description: **Cell Processor Receive Header Pattern Cell Count Register #2**
Register Address: **(1,3,5,7)DEh**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RHPC23	RHPC22	RHPC21	RHPC20	RHPC19	RHPC18	RHPC17	RHPC16
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive Header Pattern Comparison Cell Count (RHPC[23:16]) - Upper 8 bits of Register**.**

Receive Header Pattern Comparison Cell Count (RHPC[23:0]) – These twenty-four bits indicate the number of cells identified during the header pattern comparison processes. In the header pattern comparison count and discard match modes, this will be a count of cells with a matching header. In the header pattern comparison count and discard no match modes, this will be a count of cells without a matching header. In the header pattern comparison count (match and no match) modes, this count will also be included in the receive cell count registers. In the header pattern comparison discard (match or no match) modes, this count will not be included in any other count.

This register is updated via the PMU signal (see Section 10.4.5).

Register Name: **CP.RCCCR1**
Register Description: **Cell Processor Receive Corrected Cell Count Register #1**
Register Address: **(1,3,5,7)E0h**

Bit #	15	14	13	12	11	10	9	8
Name	RCHC15	RCHC14	RCHC13	RCHC12	RCHC11	RCHC10	RCHC9	RCHC8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RCHC7	RCHC6	RCHC5	RCHC4	RCHC3	RCHC2	RCHC1	RCHC0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Receive Corrected Header Count (RCHC[15:0]) – Lower sixteen bits of 24 bits. Register description follows next register.

Register Name: **CP.RCCCR2**
Register Description: **Cell Processor Receive Corrected Cell Count Register #2**
Register Address: **(1,3,5,7)E2h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RCHC23	RCHC22	RCHC21	RCHC20	RCHC19	RCHC18	RCHC17	RCHC16
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive Corrected Header Count (RCHC[23:16]) - Upper 8 bits of Register.

Receive Corrected Header Count (RCHC[23:0]) – These twenty-four bits indicate the number of cells that have had header errors corrected. If header error correction is disabled, this count will be zero. This count will be included in the receive cell count registers (*CP.RCCR*), receive filtered idle/unassigned/invalid cell count registers (*CP.RFCCR*), or receive header pattern cell count registers (*CP.RHPCR*).

This register is updated via the PMU signal (see Section 10.4.5).

Register Name: **CP.RFCCR1**
Register Description: **Cell Processor Receive Filtered Idle/Unassigned/Invalid Cell Count Register #1**
Register Address: **(1,3,5,7)E4h**

Bit #	15	14	13	12	11	10	9	8
Name	RFCC15	RFCC14	RFCC13	RFCC12	RFCC11	RFCC10	RFCC9	RFCC8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RFCC7	RFCC6	RFCC5	RFCC4	RFCC3	RFCC2	RFCC1	RFCC0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Receive Filtered Cell Count (RFCC[15:0]) – Lower sixteen bits of 24 bits. Register description follows next register.

Register Name: **CP.RFCCR2**
Register Description: **Cell Processor Receive Filtered Idle/Unassigned/Invalid Cell Count Register #2**
Register Address: **(1,3,5,7)E6h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RFCC23	RFCC22	RFCC21	RFCC20	RFCC19	RFCC18	RFCC17	RFCC16
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive Filtered Cell Count (RFCC[23:16]) - Upper 8 bits of Register.

Receive Filtered Cell Count (RFCC[23:0]) – These twenty-four bits indicate the number of cells that were discarded during the cell filtering processes (idle, unassigned, and/or invalid). If all cell filtering is disabled, this count will be zero. Cells included in this count will not be included in any other count.

This register is updated via the PMU signal (see Section 10.4.5).

12.14.3 Transmit Packet Processor Register Map

The transmit packet processor block utilizes ten registers. Note: These registers are shared with the transmit cell processor registers.

Table 12-50. Transmit Packet Processor Register Map

Address	Register	Register Description
(1,3,5,7)A0h	PP.TCR	Packet Processor Transmit Control Register
(1,3,5,7)A2h	PP.TIFGC	Packet Processor Transmit Inter-Frame Gapping Control Register
(1,3,5,7)A4h	PP.TEPC	Packet Processor Transmit Errored Packet Control Register
(1,3,5,7)A6h	--	Reserved
(1,3,5,7)A8h	--	Reserved
(1,3,5,7)AAh	--	Reserved
(1,3,5,7)ACh	--	Reserved
(1,3,5,7)AEh	PP.TSR	Packet Processor Transmit Status Register
(1,3,5,7)B0h	PP.TSRL	Packet Processor Transmit Status Register Latched
(1,3,5,7)B2h	PP.TSRIE	Packet Processor Transmit Status Register Interrupt Enable
(1,3,5,7)B4h	PP.TPCR1	Packet Processor Transmit Packet Count Register #1
(1,3,5,7)B6h	PP.TPCR2	Packet Processor Transmit Packet Count Register #2
(1,3,5,7)B8h	PP.TBCR1	Packet Processor Transmit Byte Count Register #1
(1,3,5,7)BAh	PP.TBCR2	Packet Processor Transmit Byte Count Register #2
(1,3,5,7)BCh	--	Unused
(1,3,5,7)BEh	--	Unused

12.14.3.1 Register Bit Descriptions

Register Name: **PP.TCR**
Register Description: **Packet Processor Transmit Control Register**
Register Address: **(1,3,5,7)A0h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	TFAD	TF16	TIFV	TSD	TBRE	TPTE
Default	0	0	0	0	0	0	0	0

Bit 5: Transmit FCS Append Disable (TFAD) – This bit controls whether or not an FCS is appended to the end of each packet. When 0, the calculated FCS bytes are appended to the end of the packet. When 1, the packet is transmitted without an FCS.

Bit 4: Transmit FCS-16 Enable (TF16) – When 0, the FCS processing uses a 32-bit FCS. When 1, the FCS processing uses a 16-bit FCS

Bit 3: Transmit Bit Synchronous Inter-frame Fill Value (TIFV) – When 0, inter-frame fill is done with the flag sequence (7Eh). When 1, inter-frame fill is done with all ones. This bit is ignored in octet-aligned mode.

Bit 2: Transmit Scrambling Disable (TSD) – When 0, scrambling is performed. When 1, scrambling is disabled.

Bit 1: Transmit Bit Reordering Enable (TBRE) – When 0, bit reordering is disabled (The first bit transmitted is from the MSB of the transmit FIFO byte). When 1, bit reordering is enabled (The first bit transmitted is from the LSB of the transmit FIFO byte).

Bit 0: Transmit Pass-Through Enable (TPTE) – When 0, pass-through mode is disabled and packet processing is enabled. When 1, the packet processor is in pass-through mode and all packet processing functions except scrambling and bit reordering are disabled.

Register Name: **PP.TIFGC**
Register Description: **Packet Processor Transmit Inter-Frame Gapping Control Register**
Register Address: **(1,3,5,7)A2h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	TIFG7	TIFG6	TIFG5	TIFG4	TIFG3	TIFG2	TIFG1	TIFG0
Default	0	0	0	0	0	0	0	1

Bits 7 to 0: Transmit Inter-Frame Gapping (TIFG[7:0]) – These eight bits indicate the number of additional flags and bytes of inter-frame fill to be inserted between packets. The number of flags and bytes of inter-frame fill between packets will be at least the value of TIFG[7:0] plus 1. Note: If inter-frame fill is set to all 1's, a TFIG value of 2 or 3 will result in a flag, at least two bytes of 1's, and a flag between packets.

Register Name: **PP.TEPC**
Register Description: **Packet Processor Transmit Errored Packet Control Register**
Register Address: **(1,3,5,7)A4h**

Bit #	15	14	13	12	11	10	9	8
Name	MEIMS	TPER6	TPER5	TPER4	TPER3	TPER2	TPER1	TPER0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	TPEN7	TPEN6	TPEN5	TPEN4	TPEN3	TPEN2	TPEN1	TPEN0
Default	0	0	0	0	0	0	0	0

Bit 15: Manual Error Insert Mode Select (MEIMS) – When 0, the transmit manual error insertion signal (TMEI) will not cause errors to be inserted. When 1, TMEI will causes an error to be inserted when it transitions from a 0 to a 1. Note: Enabling TMEI does not disable error insertion using TPER[6:0] and TPEN[7:0].

Manual Error Insertion is available at the global level but not on a per port basis for the packet processor. (PORT.CR1.MEIM must be set for global error insertion to insert a packet error.)

Bits 14 to 8: Transmit Errored Packet Insertion Rate (TPER[6:0]) – These seven bits indicate the rate at which errored packets are to be output. One out of every x * 10^y packets is to be an errored packet. TPER[3:0] is the value x, and TPER[6:4] is the value y, which has a maximum value of 6. If TPER[3:0] has a value of 0h errored packet insertion is disabled. If TPER[6:4] has a value of 6xh or 7xh the errored packet rate will be x * 10^6. A TPER[6:0] value of 01h results in every packet being errored. A TPER[6:0] value of 0Fh results in every 15^{th} packet being errored. A TPER[6:0] value of 11h result in every 10^{th} packet being errored. Errored packet insertion starts when the *PP.TEPC* register is written with a TPER[3:0] value that is non-zero. If the *PP.TEPC* register is written to during the middle of an errored packet insertion process, the current process is halted, and a new process will be started using the new values of TPER[6:0] and TPEN[7:0}. Errored packet insertion ends when TPEN[7:0] errored packets have been transmitted.

Bits 7 to 0: Transmit Errored Packet Insertion Number (TPEN[7:0]) – These eight bits indicate the total number of errored packets to be transmitted. A value of FFh results in continuous errored packet insertion at the specified rate.

Register Name: **PP.TSR**
Register Description: **Packet Processor Transmit Status Register**
Register Address: **(1,3,5,7)AEh**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	--	--	TEPF

Bit 0: Transmit Errored Packet Insertion Finished (TEPF) – This bit is set when the number of errored packets indicated by the TPEN[7:0] bits in the *PP.TEPC* register have been transmitted. This bit is cleared when errored packet insertion is disabled, or a new errored packet insertion process is initiated.

Register Name: **PP.TSRL**
Register Description: **Packet Processor Transmit Status Register Latched**
Register Address: **(1,3,5,7)B0h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	--	--	TEPFL

Bit 0: Transmit Errored Packet Insertion Finished Latched (TEPFL) – This bit is set when the TEPF bit in the *PP.TSR* register transitions from zero to one.

Register Name: **PP.TSRIE**
Register Description: **Packet Processor Transmit Status Register Interrupt Enable**
Register Address: **(1,3,5,7)B2h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	--	--	TEPFIE
Default	0	0	0	0	0	0	0	0

Bit 0: Transmit Errored Packet Insertion Finished Interrupt Enable (TEPFIE) – This bit enables an interrupt if the TEPFL bit in the *PP.TSRL* register is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **PP.TPCR1**
Register Description: **Packet Processor Transmit Packet Count Register #1**
Register Address: **(1,3,5,7)B4h**

Bit #	15	14	13	12	11	10	9	8
Name	TPC15	TPC14	TPC13	TPC12	TPC11	TPC10	TPC9	TPC8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	TPC7	TPC6	TPC5	TPC4	TPC3	TPC2	TPC1	TPC0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Transmit Packet Count (TPC[15:0]) – Lower sixteen bits of 24 bits. Register description follows next register.

Register Name: **PP.TPCR2**
Register Description: **Packet Processor Transmit Packet Count Register #2**
Register Address: **(1,3,5,7)B6h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	TPC23	TPC22	TPC21	TPC20	TPC19	TPC18	TPC17	TPC16
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Transmit Packet Count (TPC[23:16]) - Upper 8 bits of Register.

Transmit Packet Count (TPC[23:0]) – These twenty-four bits indicate the number of packets extracted from the Transmit FIFO and output in the outgoing data stream. This register is updated via the PMU signal (see Section 10.4.5).

Register Name: **PP.TBCR1**
Register Description: **Packet Processor Transmit Byte Count Register #1**
Register Address: **(1,3,5,7)B8h**

Bit #	15	14	13	12	11	10	9	8
Name	TBC15	TBC14	TBC13	TBC12	TBC11	TBC10	TBC9	TBC8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	TBC7	TBC6	TBC5	TBC4	TBC3	TBC2	TBC1	TBC0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Transmit Byte Count (TBC[15:0]) – Lower sixteen bits of 32 bits. Register description follows next register.

Register Name: **PP.TBCR2**
Register Description: **Packet Processor Transmit Byte Count Register #2**
Register Address: **(1,3,5,7)BAh**

Bit #	15	14	13	12	11	10	9	8
Name	TBC31	TBC30	TBC29	TBC28	TBC27	TBC26	TBC25	TBC24
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	TBC23	TBC22	TBC21	TBC20	TBC19	TBC18	TBC17	TBC16
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Transmit Byte Count (TBC[31:16]) - Upper 16 bits of 32 bits.

Transmit Byte Count (TBC[31:0]) – These thirty-two bits indicate the number of packet bytes inserted in the outgoing data stream. This register is updated via the PMU signal (see Section 10.4.5).

12.14.4 Receive Packet Processor Register Map

The receive packet processor block has seventeen registers.

Table 12-51. Receive Packet Processor Register Map

Address	Register	Register Description
(1,3,5,7)C0h	PP.RCR	Packet Processor Receive Control Register
(1,3,5,7)C2h	PP.RMPSC	Packet Processor Receive Maximum Packet Size Control Register
(1,3,5,7)C4h	--	Reserved
(1,3,5,7)C6h	--	Reserved
(1,3,5,7)C8h	--	Reserved
(1,3,5,7)CAh	--	Reserved
(1,3,5,7)CCh	--	Reserved
(1,3,5,7)CEh	PP.RSR	Packet Processor Receive Status Register
(1,3,5,7)D0h	PP.RSRL	Packet Processor Receive Status Register Latched
(1,3,5,7)D2h	PP.RSRIE	Packet Processor Receive Status Register Interrupt Enable
(1,3,5,7)D4h	PP.RPCR1	Packet Processor Receive Packet Count Register #1
(1,3,5,7)D6h	PP.RPCR2	Packet Processor Receive Packet Count Register #2
(1,3,5,7)D8h	PP.RFPCR1	Packet Processor Receive FCS Erred Packet Count Register #1
(1,3,5,7)DAh	PP.RFPCR2	Packet Processor Receive FCS Erred Packet Count Register #2
(1,3,5,7)DCh	PP.RAPCR1	Packet Processor Receive Aborted Packet Count Register #1
(1,3,5,7)DEh	PP.RAPCR2	Packet Processor Receive Aborted Packet Count Register #2
(1,3,5,7)E0h	PP.RSPCR1	Packet Processor Receive Size Violation Packet Count Register #1
(1,3,5,7)E2h	PP.RSPCR2	Packet Processor Receive Size Violation Packet Count Register #2
(1,3,5,7)E4h	--	Reserved
(1,3,5,7)E6h	--	Reserved
(1,3,5,7)E8h	PP.RBCR1	Packet Processor Receive Byte Count Register #1
(1,3,5,7)EAh	PP.RBCR2	Packet Processor Receive Byte Count Register #2
(1,3,5,7)ECh	PP.REBCR1	Packet Processor Receive Errored Byte Count Register #1
(1,3,5,7)EEh	PP.REBCR2	Packet Processor Receive Errored Byte Count Register #2
(1,3,5,7)F0h	--	Unused
(1,3,5,7)F2h	--	Unused
(1,3,5,7)F4h	--	Unused
(1,3,5,7)F6h	--	Unused
(1,3,5,7)F8h	--	Unused
(1,3,5,7)FAh	--	Unused
(1,3,5,7)FCh	--	Unused
(1,3,5,7)FEh	--	Unused

12.14.4.1 Register Bit Descriptions

Register Name: **PP.RCR**
Register Description: **Packet Processor Receive Control Register**
Register Address: **(1,3,5,7)C0h**

Bit #	15	14	13	12	11	10	9	8
Name	RMNS7	RMNS6	RMNS5	RMNS4	RMNS3	RMNS2	RMNS1	RMNS0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	RFPD	RF16	RFED	RDD	RBRE	RPTE
Default	0	0	0	0	0	0	0	0

Bits 15 to 8: Receive Minimum Packet Size (RMNS[7:0]) – These eight bits indicate the minimum allowable packet size in bytes. The size includes the FCS bytes, but excludes bit/byte stuffing. Note: In FCS-32 mode, packets with six bytes are the minimum packet size allowed, in FCS-16 mode, packets with four bytes are the minimum packet size allowed, and when FCS processing is disabled, packets with two bytes are the minimum packet size allowed. Packets less than the minimum size will be aborted.

Bit 5: Receive FCS Processing Disable (RFPD) – When 0, FCS processing is performed (the packets have an FCS appended). When 1, FCS processing is disabled (the packets do not have an FCS appended).

Bit 4: Receive FCS-16 Enable (RF16) – When 0, the error checking circuit uses a 32-bit FCS. When 1, the error checking circuit uses a 16-bit FCS. This bit is ignored when FCS processing is disabled.

Bit 3: Receive FCS Extraction Disable (RFED) – When 0, the FCS bytes are discarded. When 1, the FCS bytes are passed on. This bit is ignored when FCS processing is disabled.

Bit 2: Receive De-scrambling Disable (RDD) – When 0, de-scrambling is performed. When 1, de-scrambling is disabled.

Bit 1: Receive Bit Reordering Enable (RBRE) – When 0, bit reordering is disabled (The first bit received is stored in the MSB of the receive FIFO byte RFD[7]). When 1, bit reordering is enabled (The first bit received is stored in the LSB of the receive FIFO byte RFD[0]).

Bit 0: Receive Pass-Through Enable (RPTE) – When 0, pass-through mode is disabled and packet processing is enabled. When 1, pass-through mode is enabled, and all packet-processing functions except de-scrambling and bit reordering are disabled.

Register Name: **PP.RMPSC**
Register Description: **Packet Processor Receive Maximum Packet Size Control Register**
Register Address: **(1,3,5,7)C2h**

Bit #	15	14	13	12	11	10	9	8
Name	RMX15	RMX14	RMX13	RMX12	RMX11	RMX10	RMX9	RMX8
Default	0	0	0	0	0	1	1	0

Bit #	7	6	5	4	3	2	1	0
Name	RMX7	RMX6	RMX5	RMX4	RMX3	RMX2	RMX1	RMX0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Receive Maximum Packet Size (RMX[15:0]) – These sixteen bits indicate the maximum allowable packet size in bytes. The size includes the FCS bytes, but excludes bit/byte stuffing. Note: If the maximum packet length is less than the minimum packet length, all packets will be aborted. When packet processing is disabled, these sixteen bits indicate the "packet" size the incoming data is to be broken into.

Register Name: **PP.RSR**
Register Description: **Packet Processor Receive Status Register**
Register Address: **(1,3,5,7)CEh**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	Reserved	Reserved	Reserved	Reserved

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	REPC	RAPC	RSPC

Bit 2: Receive FCS Errored Packet Count (REPC) – This read only bit indicates that the receive FCS errored packet count is non-zero.

Bit 1: Receive Aborted Packet Count (RAPC) – This read only bit indicates that the receive aborted packet count is non-zero.

Bit 0: Receive Size Violation Packet Count (RSPC) – This read only bit indicates that the receive size violation packet count is non-zero.

Register Name: **PP.RSRL**
Register Description: **Packet Processor Receive Status Register Latched**
Register Address: **(1,3,5,7)D0h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	Reserved	Reserved	Reserved	Reserved

Bit #	7	6	5	4	3	2	1	0
Name	REPL	RAPL	RIPDL	RSPDL	RLPDL	REPCL	RAPCL	RSPCL

Bit 7: Receive FCS Errored Packet Latched (REPL) – This bit is set when a packet with an errored FCS is detected.

Bit 6: Receive Aborted Packet Latched (RAPL) – This bit is set when a packet with an abort indication is detected.

Bit 5: Receive Invalid Packet Detected Latched (RIPDL) – This bit is set when a packet with a non-integer number of bytes is detected.

Bit 4: Receive Small Packet Detected Latched (RSPDL) – This bit is set when a packet smaller than the minimum packet size is detected.

Bit 3: Receive Large Packet Detected Latched (RLPDL) – This bit is set when a packet larger than the maximum packet size is detected.

Bit 2: Receive FCS Errored Packet Count Latched (REPCL) – This bit is set when the REPC bit in the RPPSR register transitions from zero to one.

Bit 1: Receive Aborted Packet Count Latched (RAPCL) – This bit is set when the RAPC bit in the RPPSR register transitions from zero to one.

Bit 0: Receive Size Violation Packet Count Latched (RSPCL) – This bit is set when the RSPC bit in the RPPSR register transitions from zero to one.

Register Name: **PP.RSRIE**
Register Description: **Packet Processor Receive Status Register Interrupt Enable**
Register Address: **(1,3,5,7)D2h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	REPIE	RAPIE	RIPDIE	RSPDIE	RLPDIE	REPCIE	RAPCIE	RSPCIE
Default	0	0	0	0	0	0	0	0

Bit 7: Receive FCS Errored Packet Interrupt Enable (REPIE) – This bit enables an interrupt if the REPL bit in the *PP.RSRL* register is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 6: Receive Aborted Packet Interrupt Enable (RAPIE) – This bit enables an interrupt if the RAPL bit in the *PP.RSRL* register is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 5: Receive Invalid Packet Detected Interrupt Enable (RIPDIE) – This bit enables an interrupt if the RIPDL bit in the *PP.RSRL* register is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 4: Receive Small Packet Detected Interrupt Enable (RSPDIE) – This bit enables an interrupt if the RSPDL bit in the *PP.RSRL* register is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 3: Receive Large Packet Detected Interrupt Enable (RLPDIE) – This bit enables an interrupt if the RLPDL bit in the *PP.RSRL* register is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 2: Receive FCS Errored Packet Count Interrupt Enable (REPCIE) – This bit enables an interrupt if the REPCL bit in the *PP.RSRL* register is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set. Must be set low when the packets do not have an FCS appended.

0 = interrupt disabled
1 = interrupt enabled

Bit 1: Receive Aborted Packet Count Interrupt Enable (RAPCIE) – This bit enables an interrupt if the RAPCL bit in the *PP.RSRL* register is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Receive Size Violation Packet Count Interrupt Enable (RSPCIE) – This bit enables an interrupt if the RSPCL bit in the *PP.RSRL* register is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **PP.RPCR1**
Register Description: **Packet Processor Receive Packet Count Register #1**
Register Address: **(1,3,5,7)D4h**

Bit #	15	14	13	12	11	10	9	8
Name	RPC15	RPC14	RPC13	RPC12	RPC11	RPC10	RPC9	RPC8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RPC7	RPC6	RPC5	RPC4	RPC3	RPC2	RPC1	RPC0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Receive Packet Count (RPC[15:0]) – Lower sixteen bits of 24 bits. Register description follows next register.

Register Name: **PP.RPCR2**
Register Description: **Packet Processor Receive Packet Count Register #2**
Register Address: **(1,3,5,7)D6h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RPC23	RPC22	RPC21	RPC20	RPC19	RPC18	RPC17	RPC16
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive Packet Count (RPC[23:16]) - Upper 8 bits of Register.

Receive Packet Count (RPC[23:0]) – These twenty-four bits indicate the number of packets stored in the receive FIFO without an abort indication. Note: Packets discarded due to system loopback or an overflow condition will be included in this count.

This register is updated via the PMU signal (see Section 10.4.5).

Register Name: **PP.RFPCR1**
Register Description: **Packet Processor Receive FCS Errored Packet Count Register #1**
Register Address: **(1,3,5,7)D8h**

Bit #	15	14	13	12	11	10	9	8
Name	RFPC15	RFPC14	RFPC13	RFPC12	RFPC11	RFPC10	RFPC9	RFPC8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RFPC7	RFPC6	RFPC5	RFPC4	RFPC3	RFPC2	RFPC1	RFPC0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Receive FCS Errored Packet Count (RFPC[15:0]) – Lower sixteen bits of 24 bits. Register description follows next register.

Register Name: **PP.RFPCR2**
Register Description: **Packet Processor Receive FCS Errored Packet Count Register #2**
Register Address: **(1,3,5,7)DAh**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RFPC23	RFPC22	RFPC21	RFPC20	RFPC19	RFPC18	RFPC17	RFPC16
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive FCS Errored Packet Count (RFPC[7:0])

Receive FCS Errored Packet Count (RFPC[23:0]) – These twenty-four bits indicate the number of packets received with an FCS error. The byte count for these packets is included in the receive aborted byte count register *PP.REBCR*.

This register is updated via the PMU signal (see Section 10.4.5).

Register Name: **PP.RAPCR1**
Register Description: **Packet Processor Receive Aborted Packet Count Register #1**
Register Address: **(1,3,5,7)DCh**

Bit #	15	14	13	12	11	10	9	8
Name	RAPC15	RAPC14	RAPC13	RAPC12	RAPC11	RAPC10	RAPC9	RAPC8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RAPC7	RAPC6	RAPC5	RAPC4	RAPC3	RAPC2	RAPC1	RAPC0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Receive Aborted Packet Count (RAPC[15:0]) – Lower sixteen bits of 24 bits. Register description follows next register.

Register Name: **PP.RAPCR2**
Register Description: **Packet Processor Receive Aborted Packet Count Register #2**
Register Address: **(1,3,5,7)DEh**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RAPC23	RAPC22	RAPC21	RAPC20	RAPC19	RAPC18	RAPC17	RAPC16
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive Aborted Packet Count (RAPC[23:16]) - Upper 8 bits of Register.

Receive Aborted Packet Count (RAPC[23:0]) – These twenty-four bits indicate the number of packets received with a packet abort indication. The byte count for these packets is included in the receive aborted byte count register *PP.REBCR*.

This register is updated via the PMU signal (see Section 10.4.5).

Register Name: **PP.RSPCR1**
Register Description: **Packet Processor Receive Size Violation Packet Count Register #1**
Register Address: **(1,3,5,7)E0h**

Bit #	15	14	13	12	11	10	9	8
Name	RSPC15	RSPC14	RSPC13	RSPC12	RSPC11	RSPC10	RSPC9	RSPC8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RSPC7	RSPC6	RSPC5	RSPC4	RSPC3	RSPC2	RSPC1	RSPC0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Receive Size Violation Packet Count (RSPC[15:0]) – Lower sixteen bits of 24 bits. Register description follows next register.

Register Name: **PP.RSPCR2**
Register Description: **Packet Processor Receive Size Violation Packet Count Register #2**
Register Address: **(1,3,5,7)E2h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RSPC23	RSPC22	RSPC21	RSPC20	RSPC19	RSPC18	RSPC17	RSPC16
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive Size Violation Packet Count (RSPC[23:16]) - Upper 8 bits of Register.

Receive Size Violation Packet Count (RSPC[23:0]) – These twenty-four bits indicate the number of packets received with a packet size violation (below minimum, above maximum, or non-integer number of bytes). The byte count for these packets is included in the receive aborted byte count register *PP.REBCR*.

Register Name: **PP.RBCR1**
Register Description: **Packet Processor Receive Byte Count Register #1**
Register Address: **(1,3,5,7)E8h**

Bit #	15	14	13	12	11	10	9	8
Name	RBC15	RBC14	RBC13	RBC12	RBC11	RBC10	RBC9	RBC8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RBC7	RBC6	RBC5	RBC4	RBC3	RBC2	RBC1	RBC0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Receive Byte Count (RBC[15:0]) – Lower sixteen bits of 32 bits. Register description follows next register.

Register Name: **PP.RBCR2**
Register Description: **Packet Processor Receive Byte Count Register #2**
Register Address: **(1,3,5,7)EAh**

Bit #	15	14	13	12	11	10	9	8
Name	RBC31	RBC30	RBC29	RBC28	RBC27	RBC26	RBC25	RBC24
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RBC23	RBC22	RBC21	RBC20	RBC19	RBC18	RBC17	RBC16
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Receive Byte Count (RBC[31:16]) - Upper 16 bits of 32 bits.

Receive Byte Count (RBC[31:0]) – These thirty-two bits indicate the number of bytes contained in packets stored in the receive FIFO without an error indication. Note: Bytes discarded due to FCS extraction, system loopback, FIFO reset, or an overflow condition may be included in this count.

This register is updated via the PMU signal (see Section 10.4.5).

Register Name: **PP.REBCR1**
Register Description: **Packet Processor Receive Errored Byte Count Register #1**
Register Address: **(1,3,5,7)ECh**

Bit #	15	14	13	12	11	10	9	8
Name	REBC15	REBC14	REBC13	REBC12	REBC11	REBC10	REBC9	REBC8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	REBC7	REBC6	REBC5	REBC4	REBC3	REBC2	REBC1	REBC0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Receive Errored Byte Count (REBC[15:0]) – Lower sixteen bits of 32 bits. Register description follows next register.

Register Name: **PP.REBCR2**
Register Description: **Packet Processor Receive Errored Byte Count Register #2**
Register Address: **(1,3,5,7)EEh**

Bit #	15	14	13	12	11	10	9	8
Name	REBC31	REBC30	REBC29	REBC28	REBC27	REBC26	REBC25	REBC24
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	REBC23	REBC22	REBC21	REBC20	REBC19	REBC18	REBC17	REBC16
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Receive Errored Byte Count (REBC[31:16]) - Upper 16 bits of 32 bits.

Receive Errored Byte Count (REBC[31:0]) – These thirty-two bits indicate the number of bytes contained in packets stored in the receive FIFO with an error indication. Note: Bytes discarded due to FCS extraction, system loopback, FIFO reset, or an overflow condition may be included in this count.

This register is updated via the PMU signal (see Section 10.4.5).

13 JTAG INFORMATION

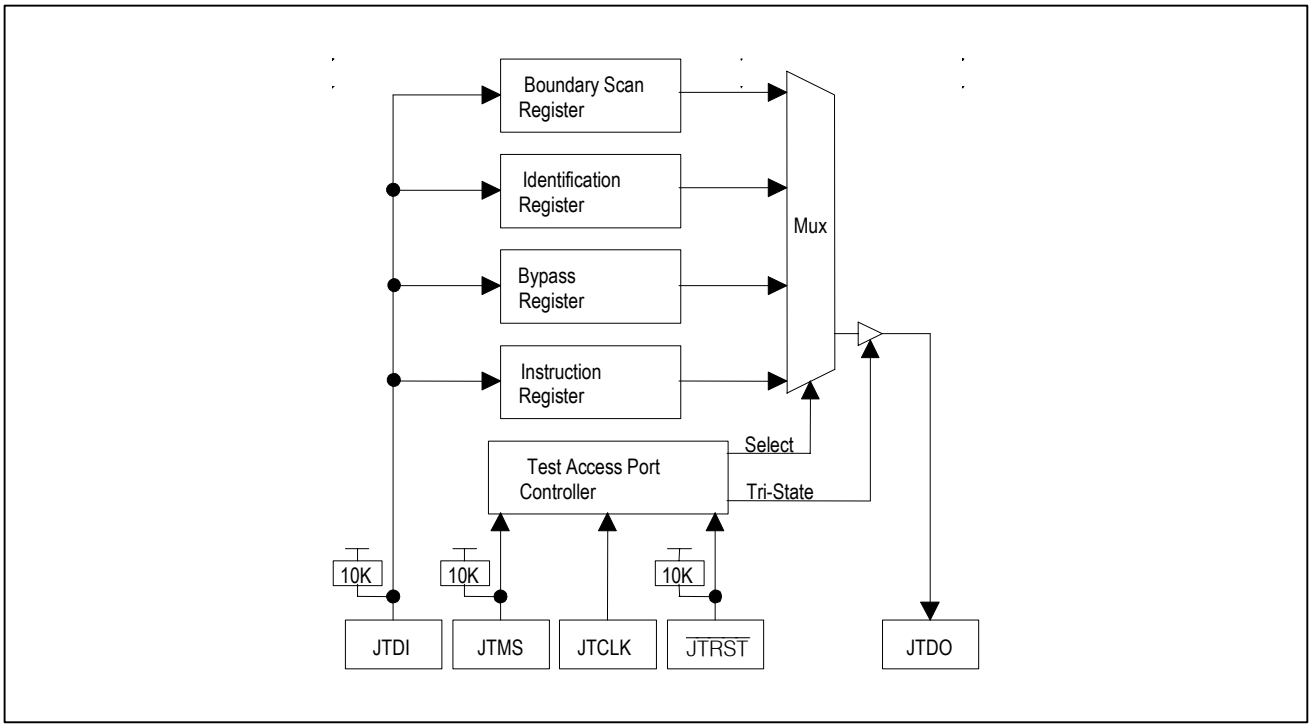
13.1 JTAG Description

This device supports the standard instruction codes SAMPLE/PRELOAD, BYPASS, and EXTEST. Optional public instructions included are HIGHZ, CLAMP, and IDCODE. The device contains the following items, which meet the requirements set by the IEEE 1149.1 Standard Test Access Port (TAP) and Boundary Scan Architecture:

Test Access Port (TAP)
TAP Controller
Instruction Register
Bypass Register
Boundary Scan Register
Device Identification Register

The Test Access Port has the necessary interface pins, namely JTCLK, JTDI, JTDO, and JTMS, and the optional $\overline{\text{JTRST}}$ input. Details on these pins can be found in Section 8. Refer to IEEE 1149.1-1990, IEEE 1149.1a-1993, and IEEE 1149.1b-1994 for details about the Boundary Scan Architecture and the Test Access Port.

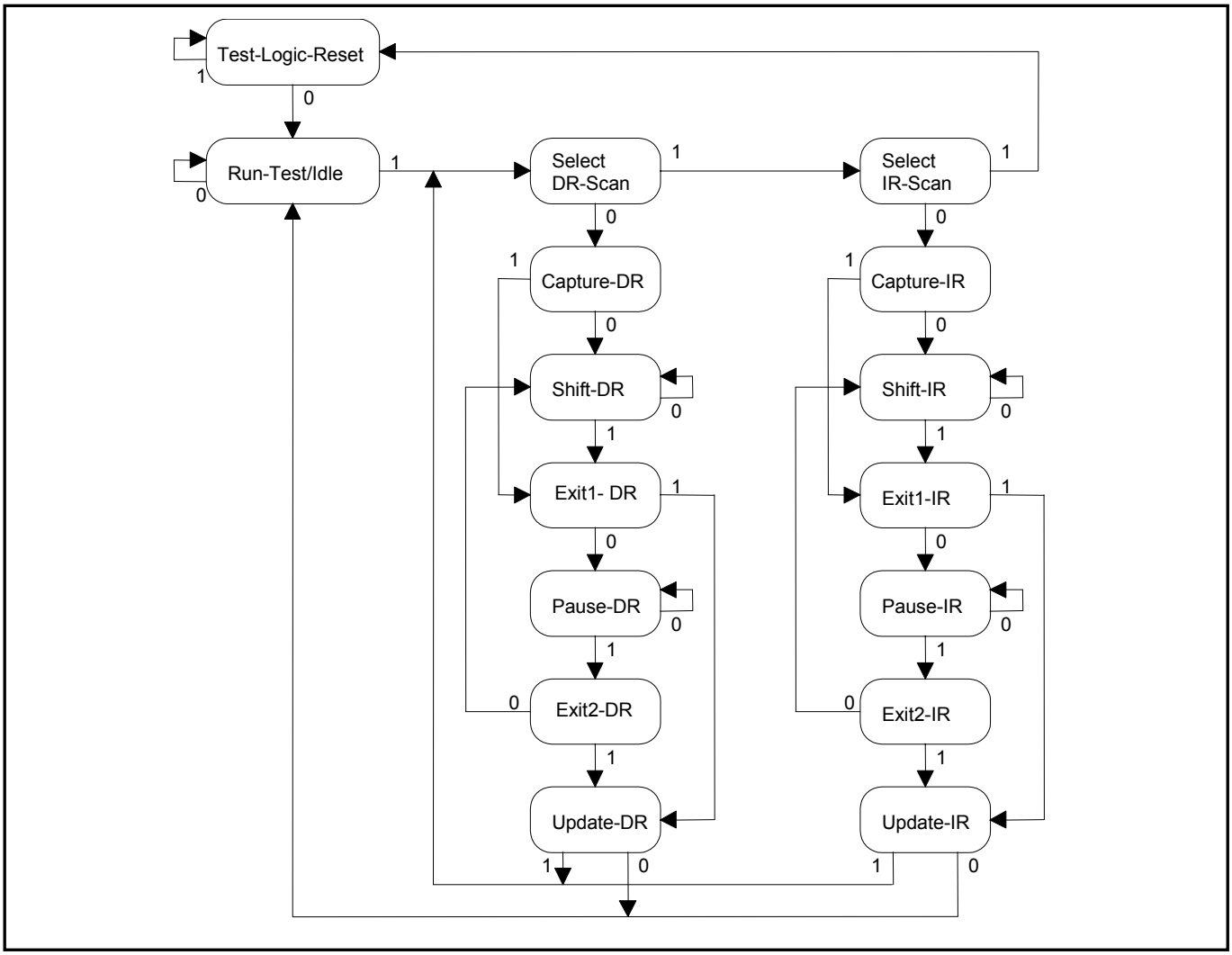
Figure 13-1. JTAG Block Diagram



13.2 JTAG TAP Controller State Machine Description

This section covers the details on the operation of the Test Access Port (TAP) Controller State Machine. See Figure 13-2 for details on each of the states described below. The TAP controller is a finite state machine that responds to the logic level at JTMS on the rising edge of JTCLK.

Figure 13-2. JTAG TAP Controller State Machine



Test-Logic-Reset. When $\overline{\text{JTRST}}$ is changed from low to high, the TAP controller starts in the Test-Logic-Reset state, and the Instruction Register is loaded with the **IDCODE** instruction. All system logic and I/O pads on the device operate normally. This state can also be reached from any other state by holding JTMS high and clocking JTCLK five times.

Run-Test-Idle. Run-Test-Idle is used between scan operations or during specific tests. The Instruction Register and Test Register remain idle.

Select-DR-Scan. All test registers retain their previous state. With JTMS low, a rising edge of JTCLK moves the controller into the Capture-DR state and initiates a scan sequence. JTMS high moves the controller to the Select-IR-Scan state.

Capture-DR. Data may be parallel loaded into the Test Data register selected by the current instruction. If the instruction does not call for a parallel load or the selected register does not allow parallel loads, the Test Register remains at its current value. On the rising edge of JTCLK, the controller goes to the Shift-DR state if JTMS is low or to the Exit1-DR state if JTMS is high.

Shift-DR. The Test Data Register selected by the current instruction is connected between JTDI and JTDO and shifts data one stage towards its serial output on each rising edge of JTCLK. If a Test Register selected by the current instruction is not placed in the serial path, it maintains its previous state.

Exit1-DR. While in this state, a rising edge on JTCLK with JTMS high puts the controller in the Update-DR state that terminates the scanning process. A rising edge on JTCLK with JTMS low puts the controller in the Pause-DR state.

Pause-DR. Shifting of the Test registers is halted while in this state. All Test registers selected by the current instruction retain their previous state. The controller remains in this state while JTMS is low. A rising edge on JTCLK with JTMS high puts the controller in the Exit2-DR state.

Exit2-DR. While in this state, a rising edge on JTCLK with JTMS high puts the controller in the Update-DR state and terminate the scanning process. A rising edge on JTCLK with JTMS low puts the controller in the Shift-DR state.

Update-DR. A falling edge on JTCLK while in the Update-DR state latches the data from the shift register path of the Test registers into the data output latches. This prevents changes at the parallel output due to changes in the shift register. A rising edge on JTCLK with JTMS low, puts the controller in the Run-Test-Idle state. With JTMS high, the controller enters the Select-DR-Scan state.

Select-IR-Scan. All Test registers retain their previous state. The Instruction register remains unchanged during this state. With JTMS low, a rising edge on JTCLK moves the controller into the Capture-IR state and initiates a scan sequence for the Instruction register. JTMS high during a rising edge on JTCLK puts the controller back into the Test-Logic-Reset state.

Capture-IR. The Capture-IR state is used to load the shift register in the Instruction register with a fixed value of 001. This value is loaded on the rising edge of JTCLK. If JTMS is high on the rising edge of JTCLK, the controller enters the Exit1-IR state. If JTMS is low on the rising edge of JTCLK, the controller enters the Shift-IR state.

Shift-IR. In this state, the shift register in the Instruction register is connected between JTDI and JTDO and shifts data one stage for every rising edge of JTCLK towards the serial output. The parallel registers, as well as all Test registers, remain at their previous states. A rising edge on JTCLK with JTMS high moves the controller to the Exit1-IR state. A rising edge on JTCLK with JTMS low keeps the controller in the Shift-IR state while moving data one stage through the Instruction shift register.

Exit1-IR. A rising edge on JTCLK with JTMS low puts the controller in the Pause-IR state. If JTMS is high on the rising edge of JTCLK, the controller enters the Update-IR state and terminate the scanning process.

Pause-IR. Shifting of the Instruction register is halted temporarily. With JTMS high, a rising edge on JTCLK puts the controller in the Exit2-IR state. The controller remains in the Pause-IR state if JTMS is low during a rising edge on JTCLK.

Exit2-IR. A rising edge on JTCLK with JTMS high put the controller in the Update-IR state. The controller loops back to the Shift-IR state if JTMS is low during a rising edge of JTCLK in this state.

Update-IR. The instruction shifted into the Instruction shift register is latched into the parallel output on the falling edge of JTCLK as the controller enters this state. Once latched, this instruction becomes the current instruction. A rising edge on JTCLK with JTMS low, puts the controller in the Run-Test-Idle state. With JTMS high, the controller enters the Select-DR-Scan state.

13.3 JTAG Instruction Register and Instructions

The instruction register contains a shift register as well as a latched parallel output and is 3 bits in length. When the TAP controller enters the Shift-IR state, the instruction shift register is connected between JTDI and JTDO. While in the Shift-IR state, a rising edge on JTCLK with JTMS low shifts data one stage toward the serial output at JTDO. A rising edge on JTCLK in the Exit1-IR state or the Exit2-IR state with JTMS high moves the controller to the Update-IR state. The falling edge of that same JTCLK latches the data in the instruction shift register to the instruction parallel output. Instructions supported by the device and their respective operational binary codes are shown in Table 13-1.

Table 13-1. JTAG Instruction Codes

INSTRUCTIONS	SELECTED REGISTER	INSTRUCTION CODES
EXTEST	Boundary Scan	000
IDCODE	Device Identification	001
SAMPLE/PRELOAD	Boundary Scan	010
CLAMP	Bypass	011
HIGHZ	Bypass	100
----	Bypass	101
----	Bypass	110
BYPASS	Bypass	111

SAMPLE/PRELOAD. This is a mandatory instruction for the IEEE 1149.1 specification. This instruction supports two functions. The digital I/Os of the device can be sampled at the boundary scan register without interfering with the normal operation of the device and the boundary scan register can be pre-loaded for the EXTEST instruction. The positive edge of JTCLK in the Capture-DR state samples all digital input pins into the boundary scan register. The boundary scan register is connected between JTDI and JTDO. The data on JTDI pin is clocked into the boundary scan register and the data captured in the Capture-DR state is shifted out the TDO pin in the Shift-DR state.

EXTEST. This is a mandatory instruction for the IEEE 1149.1 specification. This instruction allows testing of all interconnections to the device. When the EXTEST instruction is latched in the instruction register, the following actions occur. Once enabled by the Update-IR state, the parallel outputs of all digital output pins are driven according to the values in the boundary scan registers on the positive edge of JTCLK. The boundary scan register is connected between JTDI and JTDO. The positive edge of JTCLK in the Capture-DR state samples all digital input pins into the boundary scan register. The negative edge of JTCLK in the Update-DR state causes all of the digital output pins to be driven according to the values in the boundary scan registers that have been shifted in during the Shift-DR state. The outputs are returned to their normal mode or HIZ mode at the positive edge of JTCLK during the Update-IR state when an instruction other than EXTEST or CLAMP is activated.

BYPASS. This is a mandatory instruction for the IEEE 1149.1 specification. When the BYPASS instruction is latched into the parallel instruction register, JTDI connects to JTDO through the 1-bit bypass test register. This allows data to pass from JTDI to JTDO not affecting the device's normal operation. This mode can be used to bypass one or more chips in a system with multiple chips that have their JTAG scan chain connected in series. The chips not in bypass can then be tested with the normal JTAG modes.

IDCODE. This is a mandatory instruction for the IEEE 1149.1 specification. When the IDCODE instruction is latched into the parallel instruction register, the identification test register is selected. The device identification code is loaded into the identification register on the rising edge of JTCLK following entry into the Capture-DR state. Shift-DR can be used to shift the identification code out serially through JTDO. During Test-Logic-Reset, the identification code is forced into the instruction register's parallel output.

HIGHZ. All digital outputs are placed into a high-impedance state. The bypass register is connected between JTDI and JTDO. The outputs are put into the HIZ mode when the HIZ instruction is loaded in the Update-IR state and on the positive edge of JTCLK. The outputs are returned to their normal mode or driven from the boundary scan register at the positive edge of JTCLK during the Update-IR state when an instruction other than HIZ is activated.

CLAMP. All digital output pins output data from the boundary scan parallel output while connecting the bypass register between JTDI and JTDO. The outputs do not change during the CLAMP instruction. If the previous instruction was not EXTEST, the outputs will be driven according to the values in the boundary scan register at the positive edge of JTCLK in the Update-IR state. The typical use of this instruction is in a system that has the JTAG scan chain of multiple chips connected in series, and all of the chips have their outputs initialized using the EXTEST mode. Then some of the chips are left initialized using the CLAMP mode and others have their IO controlled using the EXTEST mode. This reduces the size of the scan chain during the partial testing of the system.

13.4 JTAG ID Codes

Table 13-2. JTAG ID Codes

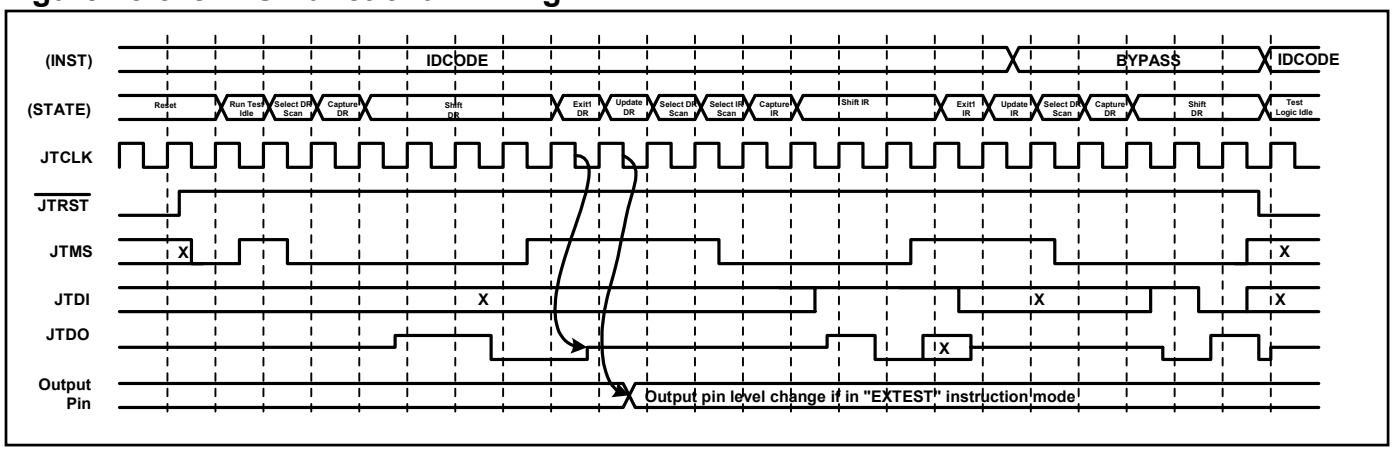
DEVICE	REVISION ID[31:28]	DEVICE CODE ID[27:12]	MANUFACTURER'S CODE ID[11:1]	REQUIRED ID[0]
DS3161	Consult factory	0000000001000000	00010100001	1
DS3162	Consult factory	0000000001000001	00010100001	1
DS3163	Consult factory	0000000001000010	00010100001	1
DS3164	Consult factory	0000000001000011	00010100001	1

13.5 JTAG Functional Timing

This functional timing for the JTAG circuits shows:

- The JTAG controller starting from reset state
- Shifting out the first 4 LSB bits of the IDCODE
- Shifting in the BYPASS instruction (111) while shifting out the mandatory X01 pattern
- Shifting the TDI pin to the TDO pin through the bypass shift register
- An asynchronous reset occurs while shifting

Figure 13-3. JTAG Functional Timing



13.6 I/O Pins

All input, output, and inout pins are inout pins in JTAG mode.

14 PIN ASSIGNMENT

Table 14-1 details the breakdown of the assigned pins for each device.

Table 14-1. Pin Assignment Breakdown

I/O SIGNALS	DS3164	DS3163	DS3162	DS3161
	259	229	199	169
VDD	41	41	41	41
VSS	68	68	68	68
Total	368 assigned pins	338 assigned pins	308 assigned pins	278 assigned pins

Figure 14-1. DS3164 Pin Assignments—400-Lead BGA

Note: Green indicates VSS, Red indicates VDD, and Yellow indicates System Interface balls. Blank cells indicate No Connect balls.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	VSS	VDD	RPOS1				TSOFO1	TLCLK1	TPDENO1	RPDAT3	RCLKO3	RLCLK3	TCLKO3	TCLKI3	RNEG3	TADR[1]	TPRTY	TADR[0]	TEN*	VSS
B	MODE	ROHSOF1	RNEG1	TCLKI1			TSOFI1	RLCLK1	TPDAT1	TPDENO3	RSER3	RSOFO3	RPDENI3	TNEG3	RPOS3	RST*	TMOD[0]	TMOD[1]	TDATA[9]	VDD
C	GPIO[5]	GPIO[6]	A[10]	TPOS1	TPDENI1		TOHSOF1	TOHCLK1	RPDAT1	TPDAT3	TLCLK3	TSOFO3	TSER3	TPOS3	TADR[4]	TDATA[21]	TDATA[19]	TDATA[20]	TDATA[25]	TDATA[8]
D		A[5]	A[9]	TNEG1	ROHCLK1	RPDENI1	TCLKO1	TOH1	RCLKO1	ROH1	TOH3	TSOFI3	TPDENI3	ROHSOF3	TADR[3]	TDATA[22]	TDATA[26]	TDATA[27]	TDXA[4]	TDXA[2]
E	A[1]	A[4]	A[8]	JTRST*	TOHEN1	TSER1		RSOFO1	RSER1	ROH3	TOHCLK3	TOHSOF3	ROHCLK3	TOHEN3	TADR[2]	TDATA[23]	RDATA[27]	RDATA[20]	TDXA[3]	RDXA[4]
F			JTCLK	JTMS	GPIO[1]	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDD	RDATA[31]	RDATA[26]	RDXA[3]	RDXA[2]	TDATA[24]
G		A[3]	A[7]	JTDO	GPIO[2]	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDD	RDATA[30]	RDATA[25]	REN*	RDATA[19]	RDATA[17]
H	A[0]	A[2]	A[6]			VDD	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDD	RDATA[29]	RDATA[24]	RDATA[22]	RDATA[18]	RDATA[16]
J			JTDI		D[15]	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	RDATA[28]	RDATA[23]	RDATA[21]	RERR	TSCLK
K	CLKA	RDY*	RD*	WR*	VDD_CLAD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	TSPA	TDXA[1]	RVAL	RDXA[1]	RPRTY
L	CLKB	CLKC	CS*	INT*	WIDTH	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	REOP	RSOX	RMOD[0]	RMOD[1]	RDATA[0]
M			TEST*			VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	RDATA[15]	RDATA[11]	RDATA[2]	RDATA[1]	RSCLK
N		ALE	D[6]	D[11]		VDD	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDD	RDATA[14]	RDATA[10]	RDATA[5]	RDATA[4]	RDATA[3]
P	D[0]	D[2]	D[7]	D[12]	GPIO[4]	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDD	RDATA[13]	RDATA[9]	RDATA[8]	RDATA[7]	RDATA[6]
R			HIZ*	D[13]	GPIO[3]	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDD	RDATA[12]	RDATA[16]	RADR[2]	RADR[1]	RADR[0]
T		D[3]	D[8]	D[14]	TOHEN2	TSER2		RSOFO2	RSER2	ROH4	TOHCLK4	TOHSOF4	ROHCLK4	TOHEN4	TDATA[30]	TDATA[17]	TDATA[18]	TDATA[1]	RADR[4]	RADR[3]
U	D[1]	D[4]	D[9]	TNEG2	ROHCLK2	RPDENI2	TCLKO2	TOH2	RCLKO2	ROH2	TOH4	TSOFI4	TPDENI4	ROHSOF4	TDATA[31]	TDATA[29]	TDATA[28]	TDATA[6]	TDATA[3]	TDATA[0]
V	GPIO[7]	GPIO[8]	D[10]	TPOS2	TPDENI2		TOHSOF2	TOHCLK2	RPDAT2	TPDAT4	TLCLK4	TSOFO4	TSER4	TPOS4	TEOP	TDATA[15]	TDATA[12]	TDATA[5]	TDATA[4]	TDATA[2]
W	VDD	D[5]	RNEG2	TCLKI2			TSOFI2	RLCLK2	TPDAT2	TPDENO4	RSER4	RSOFO4	RPDENI4	TNEG4	RPOS4	TSOX	TDATA[14]	TDATA[11]	TDATA[10]	TDATA[7]
Y	VSS	ROHSOF2	RPOS2				TSOFO2	TLCLK2	TPDENO2	RPDAT4	RCLKO4	RLCLK4	TCLKO4	TCLKI4	RNEG4	TSX	TERR	TDATA[13]	VDD	VSS

Figure 14-2. DS3163 Pin Assignments—400-Lead BGA

Note: Green indicates VSS, Red indicates VDD, and Yellow indicates System Interface balls. Blank cells indicate No Connect balls.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	VSS	VDD	RPOS1				TSOFO1	TLCLK1	TPDENO1	RPDAT3	RCLKO3	RLCLK3	TCLKO3	TCLKI3	RNEG3	TADR[1]	TPRTY	TADR[0]	TEN*	VSS
B	MODE	ROHSOF1	RNEG1	TCLKI1			TSOFI1	RLCLK1	TPDAT1	TPDENO3	RSER3	RSOFO3	RPDENI3	TNEG3	RPOS3	RST*	TMOD[0]	TMOD[1]	TDATA[9]	VDD
C	GPIO[5]	GPIO[6]	A[10]	TPOS1	TPDENI1		TOHSOF1	TOHCLK1	RPDAT1	TPDAT3	TLCLK3	TSOFO3	TSER3	TPOS3	TADR[4]	TDATA[21]	TDATA[19]	TDATA[20]	TDATA[25]	TDATA[8]
D		A[5]	A[9]	TNEG1	ROHCLK1	RPDENI1	TCLKO1	TOH1	RCLKO1	ROH1	TOH3	TSOFI3	TPDENI3	ROHSOF3	TADR[3]	TDATA[22]	TDATA[26]	TDATA[27]	TDXA[4]	TDXA[2]
E	A[1]	A[4]	A[8]	JTRST*	TOHEN1	TSER1		RSOFO1	RSER1	ROH3	TOHCLK3	TOHSOF3	ROHCLK3	TOHEN3	TADR[2]	TDATA[23]	RDATA[27]	RDATA[20]	TDXA[3]	RDXA[4]
F			JTCLK	JTMS	GPIO[1]	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDD	RDATA[31]	RDATA[26]	RDXA[3]	RDXA[2]	TDATA[24]
G		A[3]	A[7]	JTDO	GPIO[2]	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDD	RDATA[30]	RDATA[25]	REN*	RDATA[19]	RDATA[17]
H	A[0]	A[2]	A[6]			VDD	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDD	RDATA[29]	RDATA[24]	RDATA[22]	RDATA[18]	RDATA[16]
J			JTDI		D[15]	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	RDATA[28]	RDATA[23]	RDATA[21]	RERR	TSCLK
K	CLKA	RDY*	RD*	WR*	VDD_CLAD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	TSPA	TDXA[1]	RVAL	RDXA[1]	RPRTY
L	CLKB	CLKC	CS*	INT*	WIDTH	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	REOP	RSOX	RMOD[0]	RMOD[1]	RDATA[0]
M			TEST*			VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	RDATA[15]	RDATA[11]	RDATA[2]	RDATA[1]	RSCLK
N		ALE	D[6]	D[11]		VDD	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDD	RDATA[14]	RDATA[10]	RDATA[5]	RDATA[4]	RDATA[3]
P	D[0]	D[2]	D[7]	D[12]	GPIO[4]	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDD	RDATA[13]	RDATA[9]	RDATA[8]	RDATA[7]	RDATA[6]
R			HIZ*	D[13]	GPIO[3]	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDD	RDATA[12]	RDATA[16]	RADR[2]	RADR[1]	RADR[0]
T		D[3]	D[8]	D[14]	TOHEN2	TSER2		RSOFO2	RSER2						TDATA[30]	TDATA[17]	TDATA[18]	TDATA[1]	RADR[4]	RADR[3]
U	D[1]	D[4]	D[9]	TNEG2	ROHCLK2	RPDENI2	TCLKO2	TOH2	RCLKO2	ROH2					TDATA[31]	TDATA[29]	TDATA[28]	TDATA[6]	TDATA[3]	TDATA[0]
V	GPIO[7]	GPIO[8]	D[10]	TPOS2	TPDENI2		TOHSOF2	TOHCLK2	RPDAT2						TEOP	TDATA[15]	TDATA[12]	TDATA[5]	TDATA[4]	TDATA[2]
W	VDD	D[5]	RNEG2	TCLKI2			TSOFI2	RLCLK2	TPDAT2							TSOX	TDATA[14]	TDATA[11]	TDATA[10]	TDATA[7]
Y	VSS	ROHSOF2	RPOS2				TSOFO2	TLCLK2	TPDENO2							TSX	TERR	TDATA[13]	VDD	VSS

Figure 14-3. DS3162 Pin Assignments—400-Lead BGA

Note: Green indicates VSS, Red indicates VDD, and Yellow indicates System Interface balls. Blank cells indicate No Connect balls.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	VSS	VDD	RPOS1				TSOFO1	TLCLK1	TPDENO1							TADR[1]	TPRTY	TADR[0]	TEN*	VSS
B	MODE	ROHSOF1	RNEG1	TCLKI1			TSOFI1	RLCLK1	TPDAT1							RST*	TMOD[0]	TMOD[1]	TDATA[9]	VDD
C	GPIO[5]	GPIO[6]	A[10]	TPOS1	TPDENI1		TOHSOF1	TOHCLK1	RPDAT1						TADR[4]	TDATA[21]	TDATA[19]	TDATA[20]	TDATA[25]	TDATA[8]
D		A[5]	A[9]	TNEG1	ROHCLK1	RPDENI1	TCLKO1	TOH1	RCLKO1	ROH1					TADR[3]	TDATA[22]	TDATA[26]	TDATA[27]	TDXA[4]	TDXA[2]
E	A[1]	A[4]	A[8]	JTRST*	TOHEN1	TSER1		RSOFO1	RSER1						TADR[2]	TDATA[23]	RDATA[27]	RDATA[20]	TDXA[3]	RDXA[4]
F			JTCLK	JTMS	GPIO[1]	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDD	RDATA[31]	RDATA[26]	RDXA[3]	RDXA[2]	TDATA[24]
G		A[3]	A[7]	JTDO	GPIO[2]	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDD	RDATA[30]	RDATA[25]	REN*	RDATA[19]	RDATA[17]
H	A[0]	A[2]	A[6]			VDD	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDD	RDATA[29]	RDATA[24]	RDATA[22]	RDATA[18]	RDATA[16]
J			JTDI		D[15]	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	RDATA[28]	RDATA[23]	RDATA[21]	RERR	TSCLK
K	CLKA	RDY*	RD*	WR*	VDD_CLAD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	TSPA	TDXA[1]	RVAL	RDXA[1]	RPRTY
L	CLKB	CLKC	CS*	INT*	WIDTH	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	REOP	RSOX	RMOD[0]	RMOD[1]	RDATA[0]
M			TEST*			VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	RDATA[15]	RDATA[11]	RDATA[2]	RDATA[1]	RSCLK
N		ALE	D[6]	D[11]		VDD	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDD	RDATA[14]	RDATA[10]	RDATA[5]	RDATA[4]	RDATA[3]
P	D[0]	D[2]	D[7]	D[12]	GPIO[4]	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDD	RDATA[13]	RDATA[9]	RDATA[8]	RDATA[7]	RDATA[6]
R			HIZ*	D[13]	GPIO[3]	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDD	RDATA[12]	TDATA[16]	RADR[2]	RADR[1]	RADR[0]
T		D[3]	D[8]	D[14]	TOHEN2	TSER2		RSOFO2	RSER2						TDATA[30]	TDATA[17]	TDATA[18]	TDATA[1]	RADR[4]	RADR[3]
U	D[1]	D[4]	D[9]	TNEG2	ROHCLK2	RPDENI2	TCLKO2	TOH2	RCLKO2	ROH2					TDATA[31]	TDATA[29]	TDATA[28]	TDATA[6]	TDATA[3]	TDATA[0]
V	GPIO[7]	GPIO[8]	D[10]	TPOS2	TPDENI2		TOHSOF2	TOHCLK2	RPDAT2						TEOP	TDATA[15]	TDATA[12]	TDATA[5]	TDATA[4]	TDATA[2]
W	VDD	D[5]	RNEG2	TCLKI2			TSOFI2	RLCLK2	TPDAT2							TSOX	TDATA[14]	TDATA[11]	TDATA[10]	TDATA[7]
Y	VSS	ROHSOF2	RPOS2				TSOFO2	TLCLK2	TPDENO2							TSX	TERR	TDATA[13]	VDD	VSS

Figure 14-4 DS3161 Pin Assignments—400-Lead BGA

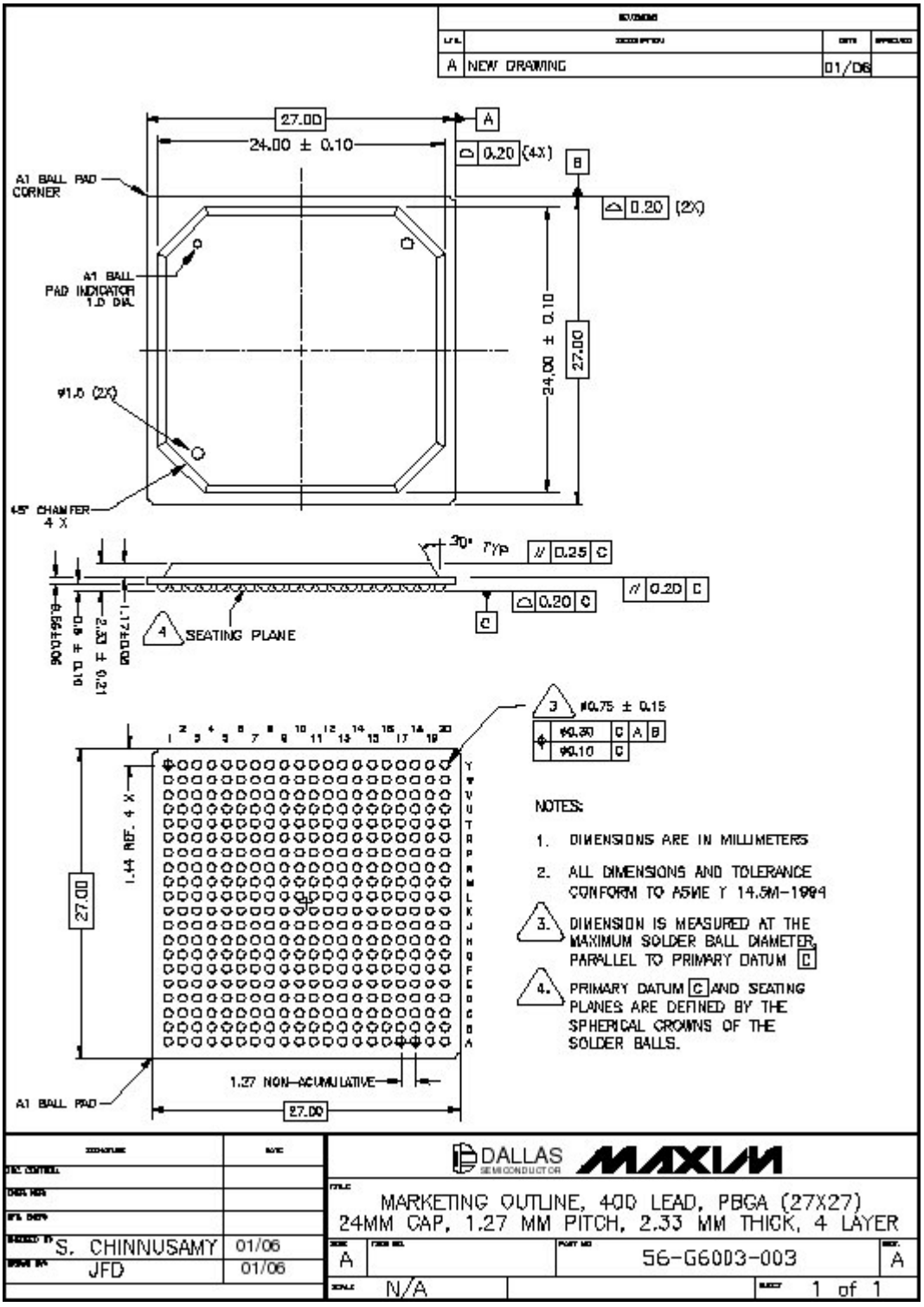
Note: Green indicates VSS, Red indicates VDD, and Yellow indicates System Interface balls. Blank cells indicate No Connect balls.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	VSS	VDD	RPOS1				TSOFO1	TLCLK1	TPDENO1							TADR[1]	TPRTY	TADR[0]	TEN*	VSS
B	MODE	ROHSOF1	RNEG1	TCLKI1			TSOFI1	RLCLK1	TPDAT1							RST*	TMOD[0]	TMOD[1]	TDATA[9]	VDD
C	GPIO[5]	GPIO[6]	A[10]	TPOS1	TPDENI1		TOHSOF1	TOHCLK1	RPDAT1						TADR[4]	TDATA[21]	TDATA[19]	TDATA[20]	TDATA[25]	TDATA[8]
D		A[5]	A[9]	TNEG1	ROHCLK1	RPDENI1	TCLKO1	TOH1	RCLKO1	ROH1					TADR[3]	TDATA[22]	TDATA[26]	TDATA[27]	TDXA[4]	TDXA[2]
E	A[1]	A[4]	A[8]	JTRST*	TOHEN1	TSER1		RSOFO1	RSER1						TADR[2]	TDATA[23]	RDATA[27]	RDATA[20]	TDXA[3]	RDXA[4]
F			JTCLK	JTMS	GPIO[1]	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDD	RDATA[31]	RDATA[26]	RDXA[3]	RDXA[2]	TDATA[24]
G		A[3]	A[7]	JTDO	GPIO[2]	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDD	RDATA[30]	RDATA[25]	REN*	RDATA[19]	RDATA[17]
H	A[0]	A[2]	A[6]			VDD	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDD	RDATA[29]	RDATA[24]	RDATA[22]	RDATA[18]	RDATA[16]
J			JTDI		D[15]	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	RDATA[28]	RDATA[23]	RDATA[21]	RERR	TSCLK
K	CLKA	RDY*	RD*	WR*	VDD_CLAD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	TSPA	TDXA[1]	RVAL	RDXA[1]	RPRTY
L	CLKB	CLKC	CS*	INT*	WIDTH	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	REOP	RSOX	RMOD[0]	RMOD[1]	RDATA[0]
M			TEST*			VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	RDATA[15]	RDATA[11]	RDATA[2]	RDATA[1]	RSCLK
N		ALE	D[6]	D[11]		VDD	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDD	RDATA[14]	RDATA[10]	RDATA[5]	RDATA[4]	RDATA[3]
P	D[0]	D[2]	D[7]	D[12]	GPIO[4]	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDD	RDATA[13]	RDATA[9]	RDATA[8]	RDATA[7]	RDATA[6]
R			HIZ*	D[13]	GPIO[3]	VDD	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDD	RDATA[12]	TDATA[16]	RADR[2]	RADR[1]	RADR[0]
T		D[3]	D[8]	D[14]											TDATA[30]	TDATA[17]	TDATA[18]	TDATA[1]	RADR[4]	RADR[3]
U	D[1]	D[4]	D[9]												TDATA[31]	TDATA[29]	TDATA[28]	TDATA[6]	TDATA[3]	TDATA[0]
V	GPIO[7]	GPIO[8]	D[10]												TEOP	TDATA[15]	TDATA[12]	TDATA[5]	TDATA[4]	TDATA[2]
W	VDD	D[5]														TSOX	TDATA[14]	TDATA[11]	TDATA[10]	TDATA[7]
Y	VSS															TSX	TERR	TDATA[13]	VDD	VSS

15 PACKAGE MECHANICAL DIMENSIONS

(The package drawing(s) in this data sheet may not reflect the most current specifications. The package number provided for each package is a link to the latest package outline information.)

15.1 400-Lead TE-PBGA (27mm x 27mm, 1.27mm Pitch) (56-G6003-003)



16 PACKAGE THERMAL INFORMATION

PARAMETER	VALUE
Target Ambient Temperature Range	-40°C to +85°C
Die Junction Temperature Range	-40°C to +125°C
Theta-JA, Still Air	12.6°C/W (Note 1)

Note 1: Theta-JA is based on the package mounted on a 4-layer JEDEC board and measured in a JEDEC test chamber.

The 36 thermal V_{SS} balls in the center 6x6 matrix must be thermally and electrically connected to the internal GND plane of the PC board to achieve these thermal characteristics.

17 DC ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Input, Bidirectional or Open Drain
Output Lead Range with Respect to V_{SS}.....-0.3V to +5.5V
Supply Voltage (V_{DD}) Range with Respect to V_{SS}.....-0.3V to +3.63V
Ambient Operating Temperature Range.....-40°C to +85°C
Junction Operating Temperature Range.....-40°C to +125°C
Storage Temperature Range.....-55°C to +125°C
Soldering Temperature Range.....See IPC/JEDEC J-STD-020 Specification.

These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time can affect device reliability. Ambient Operating Temperature Range is assuming the device is mounted on a JEDEC standard test board in a convection cooled JEDEC test enclosure.

Note: *The typical values listed below are not production tested.*

Table 17-1. Recommended DC Operating Conditions

(V_{DD} = 3.3V ±5%, T_j = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logic 1	V_{IH}		2.0		5.5	V
Logic 0	V_{IL}		-0.3		+0.8	V
Supply (V_{DD}) ±5%	V_{DD}		3.135	3.300	3.465	V

Table 17-2. DC Electrical Characteristics

(T_j = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (V_{DD} = 3.465V) (Notes 1, 2)	I_{DD}	DS3164			468	mA
		DS3163			381	
		DS3162			300	
		DS3161			218	
Power-Down Current (All DISABLE Bits Set) (Note 2)	I_{DDD}	DS3164		70	105	mA
		DS3163			72	
		DS3162			46	
		DS3161			20	
Lead Capacitance	C_{IO}			7		pF
Input Leakage	I_{IL}		-10		+10	µA
Input Leakage (Inputs Pins with Internal Pullup Resistors)	I_{ILP}		-350		+10	µA
Output Leakage (when High Impedance)	I_{LO}		-10		+10	µA
Output Voltage (I_{OH} = -4.0mA)	V_{OH}	4mA outputs	2.4			V
Output Voltage (I_{OL} = +4.0mA)	V_{OL}	4mA outputs			0.4	V
Output Voltage (I_{OH} = -6.0mA)	V_{OH}	6mA outputs	2.4			V
Output Voltage (I_{OL} = +6.0mA)	V_{OL}	6mA outputs			0.4	V

Note 1: Mode: STS-1 data rate, transmitting all ones, all clocks = 52MHz, digital outputs without load.
Note 2: All outputs loaded with rated capacitance; all inputs between V_{DD} and V_{SS}; inputs with pullups connected to V_{DD}.

Table 17-3. Output Pin Drive

PIN NAME	TYPE	DRIVE STRENGTH (mA)
TLCLKn	O	6
TPOSn /TDATn	O	6
TNEGn/TOHMOn	O	6
TXPn	O	N/A (analog)
TXNn	O	N/A (analog)
TOHCLKn	O	4
TOHSOFn	O	4
ROHn	O	4
ROHCLKn	O	4
ROHSOFn	O	4
TPOHCLKn/ TCLKOn/TGCLKn	O	6
TPOHSOFn/TSOFOn /TDENn/TFOHENOn	O	6
TPDATn	O	6
TPDENOn	O	6
RPOHn/RSERn	O	6
RPOHCLKn/ RCLKOn/RGCLKn	O	6
RPOHSOFn/RSOFOn/ RDENn/RFOHENOn	O	6
TDXA[1]/TPXA	Oz	6
TDXA[4:2]	O	6
TSPA	Oz	6
RDATA[31:0]	Oz	6
$\overline{\text{RPRTY}}$	O	6
RDXA[1]/RPXA/RSX	Oz	6
RDXA[4:2]	O	6
RSOX	Oz	6
REOP	Oz	6
RVAL	Oz	6
RMOD[1:0]	Oz	6
RERR	Oz	6
D[15:0]	IO	4
$\overline{\text{RDY}}$	Oz	6
$\overline{\text{INT}}$	Oz	6
GPIO[7:0]	IO	4
JTDO	Oz	4
CLKB	IO	6
CLKC	IO	6

18 AC TIMING CHARACTERISTICS

There are several common AC characteristic definitions. These generic definitions are shown below in Figure 18-1, Figure 18-2, Figure 18-3, and Figure 18-4. Definitions that are specific to a given interface are shown in that interface's subsection.

Figure 18-1. Clock Period and Duty Cycle Definitions

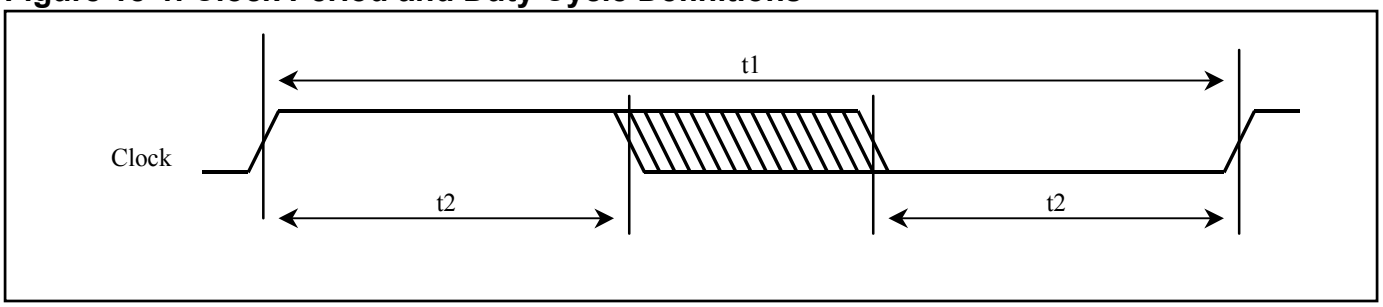


Figure 18-2. Rise Time, Fall Time, and Jitter Definitions

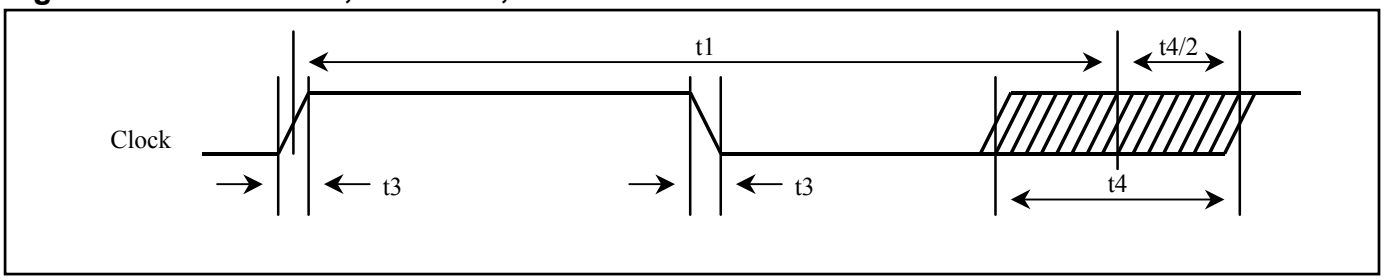


Figure 18-3. Hold, Setup, and Delay Definitions (Rising Clock Edge)

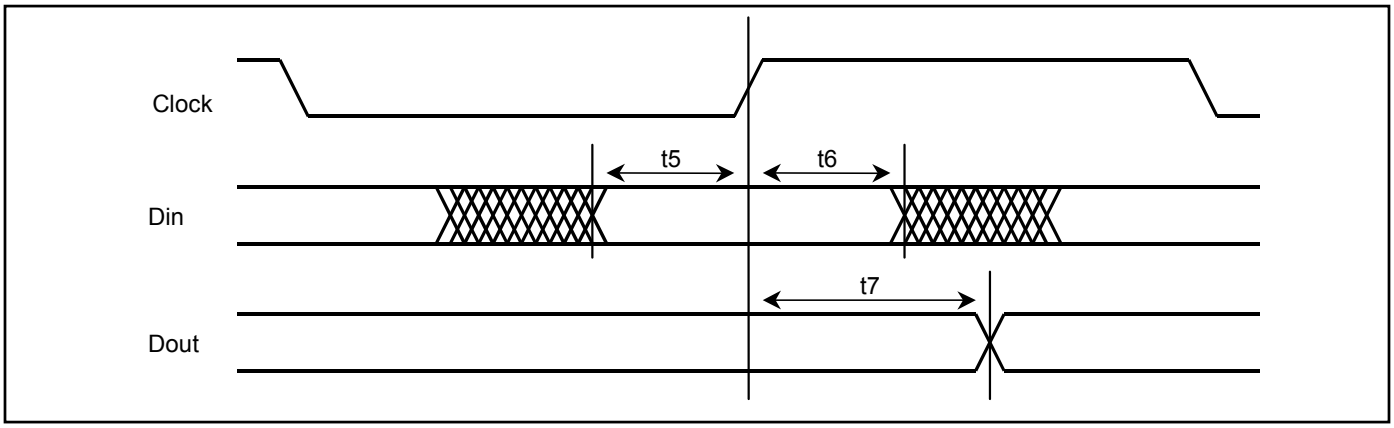


Figure 18-4. Hold, Setup, and Delay Definitions (Falling Clock Edge)

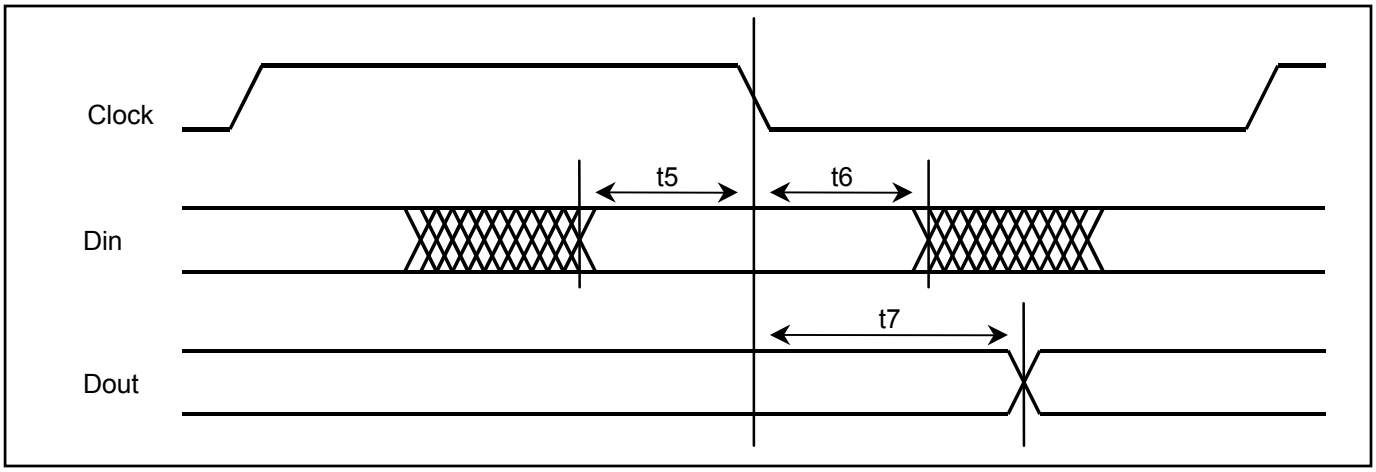


Figure 18-5. To/From Hi-Z Delay Definitions (Rising Clock Edge)

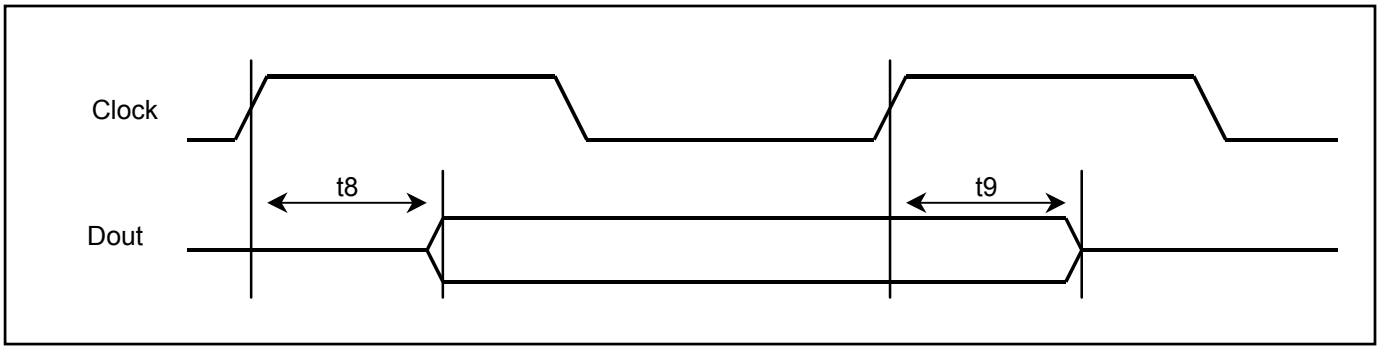
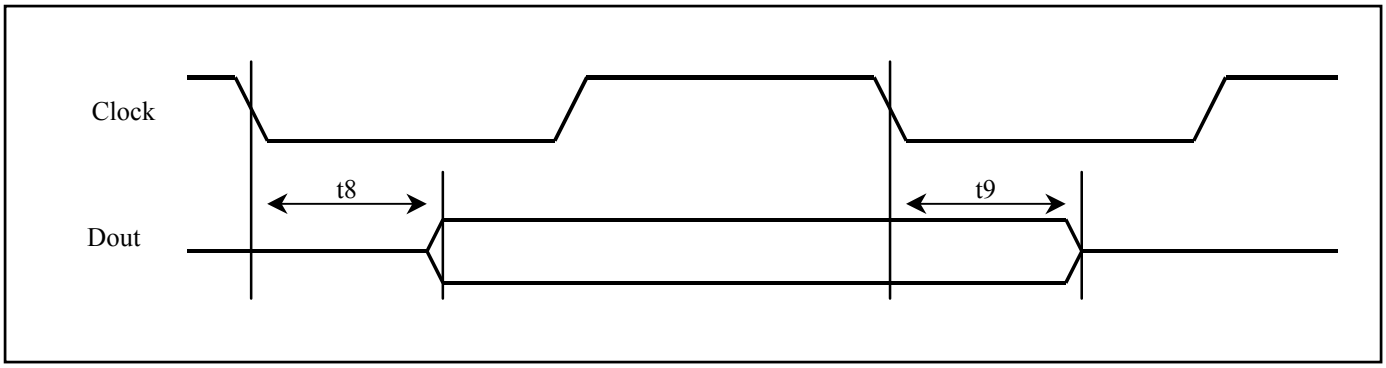


Figure 18-6. To/From Hi-Z Delay Definitions (Falling Clock Edge)



18.1 Fractional Port Characteristics

All AC timing characteristics are specified with a 25pF capacitive load on all output pins, V_{IH} = 2.4V and V_{IL} = 0.8V. The voltage threshold for all timing measurements is VDD/2. The generic timing definitions shown in Figure 18-1, Figure 18-2, Figure 18-3, Figure 18-4, Figure 18-5, and Figure 18-6 apply to this interface.

Table 18-1. Fractional Port Timing

(V_{DD} = 3.3V ±5%, T_j = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLK Period	t1	(Note 1)	19.23			ns
CLK Clock Duty Cycle (t2/t1)	t2/t1	(Note 2)	40	50	60	%
CLK Rise or Fall times (20% to 80%)	t3	(Note 2)			4	ns
DIN to CLK Setup Time	t5	(Note 3)	3			ns
		(Note 4)	7			ns
CLK to DIN Hold Time	t6	(Note 3)	1			ns
		(Note 4)	1			ns
CLK to DOUT Delay	t7	(Note 5)	2		11	ns
		(Note 6)	2		9	ns

Note 1: Any mode, 52MHz TCLKIn, RLCLKn input clocks.
Note 2: Any mode, TCLKIn, RLCLKn input clocks.
Note 3: TCLKIn, RLCLKn clock inputs to TOHMIn/TSOFIn, TFOHn/TSERn, TFOHENIn, RFOHENIn inputs.
Note 4: TCLKOn, RCLKOn clock outputs to TOHMIn/TSOFIn, TFOHn/TSERn, TFOHENOn, RFOHENOn inputs.
Note 5: TCLKIn, RLCLKn clock input to TSOFOn/TDENn, RSERn, RSOFOn/RDENn, TPDENOn, TPDATn, and RPDATn outputs.
Note 6: TCLKOn, RCLKOn clock output to TSOFOn/TDENn, RSERn, RSOFOn/RDENn, TPDENOn, TPDATn and RPDATn outputs.

18.2 Line interface AC Characteristics

All AC timing characteristics are specified with a 25pF capacitive load on all output pins, V_{IH} = 2.4V and V_{IL} = 0.8V. The voltage threshold for all timing measurements is VDD/2. The generic timing definitions shown in Figure 18-1, Figure 18-2, Figure 18-3, Figure 18-4, Figure 18-5, and Figure 18-6 apply to this interface.

Table 18-2. Line interface Timing

(V_{DD} = 3.3V ±5%, T_j = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLK Period	t1	(Note 1)	19.23			ns
CLK Clock Duty Cycle (t2/t1)	t2/t1	(Note 2)	40	50	60	%
CLK Rise or Fall times (20% to 80 %)	t3	(Note 2)			4	ns
DIN to CLK Setup Time	t5	(Note 3)	4			ns
CLK to DIN Hold Time	t6	(Note 3)	0			ns
CLK to DOUT Delay	t7	(Note 4)	2		10	ns
		(Note 5)	2		8	ns

Note 1: Any mode, 52MHz TCLKIn, RLCLKn input clocks.
Note 2: Any mode, TCLKIn, RLCLKn input clocks.
Note 3: RLCLKn clock inputs to RPOSn/RDATn, RNEGn/RLCVn/ROHMIn inputs.
Note 4: TCLKIn, RLCLKn clock input to TPOSn/TDATn, TNEGn/TOHMOn outputs.
Note 5: TLCLKn, TCLKOn, RCLKOn clock output to TPOSn/TDATn, TNEGn/TOHMOn outputs.

18.3 Misc pin AC Characteristics

All AC timing characteristics are specified with a 25pF capacitive load on all output pins, V_{IH} = 2.4V and V_{IL} = 0.8V. The voltage threshold for all timing measurements is VDD/2. The generic timing definitions shown in Figure 18-1, Figure 18-2, Figure 18-3, Figure 18-4, Figure 18-5, and Figure 18-6 apply to this interface.

Table 18-3. Miscellaneous Pin Timing

(V_{DD} = 3.3V ±5%, T_j = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Asynchronous Input High, Low Time	t1, t2	(Note 1)	500			ns
Asynchronous Input Rise, Fall Time	t3	(Note 1)			10	ns

Note 1: TMEI (GPIO), PMU (GPIO), 8KREFI(GPIO) and $\overline{RST}$ inputs.

18.4 Overhead Port AC Characteristics

All AC timing characteristics are specified with a 25pF capacitive load on all output pins, V_{IH} = 2.4V and V_{IL} = 0.8V. The voltage threshold for all timing measurements is VDD/2. The generic timing definitions shown in Figure 18-1, Figure 18-2, Figure 18-3, Figure 18-4, Figure 18-5, and Figure 18-6 apply to this interface.

Table 18-4. Overhead Port Timing

(V_{DD} = 3.3V ±5%, T_j = -40°C to +125°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLK Period	t1	(Note 1)	500			ns
CLK Clock High and Low Time	t1, t2	(Note 1)	200			ns
DIN to CLK Setup Time	t5	(Note 2)	20			ns
CLK to DIN Hold Time	t6	(Note 2)	20			ns
CLK to DOUT Delay	t7	(Note 3)	-20		20	ns

Note 1: TOHCLKn, TPOHCLKn, ROHCLKn, RPOHCLKn output clocks.
Note 2: TOHCLKn, TPOHCLKn clock falling edge outputs to TOHn, TOHENn, TPOHn, TPOHENn inputs.
Note 3: TOHCLKn, TPOHCLKn, ROHCLKn, RPOHCLKn clock falling edge outputs to TOHSOFn, TPOHSOFn, ROHn, ROHSOF, RPOHn, RPOHSOFn outputs.

18.5 System Interface AC Characteristics

The AC characteristics of the system interface depend upon the mode of the interface. While UTOPIA vs. POS-PHY mode does not have an effect on the AC characteristics, Level 2 vs. Level 3 does. Therefore, there are two tables: one for Level 2 (Table 18-5) and one for Level 3 (Table 18-6). The generic timing definitions shown in Figure 18-1, Figure 18-2, Figure 18-3, Figure 18-5, and Figure 18-6 apply to this interface.

Table 18-5. System Interface Level 2 Timing

(V_{DD} = 3.3V ±5%, T_j = -40°C to +125°C.)

SIGNAL NAME(S)	SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS	NOTES
RSCLK and TSCLK	f1	Clock Frequency (1/t1)	0		52	MHz	1
RSCLK and TSCLK	t2/t1	Clock Duty Cycle	40	50	60	%	1
RSCLK and TSCLK	t3	Rise/Fall Times			2	ns	1,2
RADR and $\overline{REN}$	t5	Hold Time from RSCLK	0			ns	1
RADR and $\overline{REN}$	t6	Setup Time to RSCLK	3.5			ns	1
RDATA, RPRTY, RPXA, RSOX, REOP, RVAL, RMOD, and RERR	t7	Delay from RSCLK	2		12	ns	1,3
RDATA, RPRTY, RPXA, RSOX, REOP, RVAL, RMOD, and RERR	t8	From Hi-Z Delay from RSCLK	2		12	ns	1,3
RDATA, RPRTY, RPXA, RSOX, REOP, RVAL, RMOD, and RERR	t9	To Hi-Z Delay from RSCLK	2		15	ns	1,3
TDATA, TPRTY, TADR, $\overline{TEN}$, TSOX, TEOP, TMOD, and TERR	t5	Hold Time from TSCLK	0			ns	1
TDATA, TPRTY, TADR, $\overline{TEN}$, TSOX, TEOP, TMOD, and TERR	t6	Setup Time to TSCLK	3			ns	1
TPXA and TSPA	t7	Delay from TSCLK	2		12	ns	1,3
TPXA and TSPA	t8	From Hi-Z Delay from TSCLK	2		12	ns	1,3
TPXA and TSPA	t9	To Hi-Z Delay from TSCLK	2		15	ns	1,3

Note 1: The input/output timing reference level for all signals is VDD/2.

Note 2: Rise and fall times are measured at output side with the output unloaded. Rise time is measured from 20% to 80% V_{OH}. Fall time is measured from 80% to 20% V_{OH}.

Note 3: These times are met with a 30pF, 300Ω load on the associated output pin.

Table 18-6. System Interface Level 3 Timing

(V_{DD} = 3.3V ±5%, T_j = -40°C to +125°C.)

SIGNAL NAME(S)	SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS	NOTES
RSCLK and TSCLK	f1	Clock Frequency (1/t1)	0		66	MHz	1
RSCLK and TSCLK	t2/t1	Clock Duty Cycle	40	50	60	%	1
RSCLK and TSCLK	t3	Rise/Fall Times			2	ns	1,2
RADR and $\overline{REN}$	t5	Hold Time from RSCLK	0			ns	1
RADR and $\overline{REN}$	t6	Setup Time to RSCLK	3.5			ns	1
RDATA, RPRTY, RPXA, RSOX, REOP, RVAL, RMOD, and RERR	t7	Delay from RSCLK	2		9.5	ns	1,3
TDATA, TPRTY, TADR, $\overline{TEN}$, TSOX, TEOP, TMOD, and TERR	t5	Hold Time from TSCLK	0			ns	1
TDATA, TPRTY, TADR, $\overline{TEN}$, TSOX, TEOP, TMOD, and TERR	t6	Setup Time to TSCLK	3.5			ns	1
TPXA and TSPA	t7	Delay from TSCLK	2		9.5	ns	1,3

Note 1: The input/output timing reference level for all signals is VDD/2.

Note 2: Rise and fall times are measured at output side with the output unloaded. Rise time is measured from 20% to 80% V_{OH}. Fall time is measured from 80% to 20% V_{OH}.

Note 3: These times are met with a 30pF, 300Ω load on the associated output pin.

18.6 Micro Interface AC Characteristics

The AC characteristics for the external bus interface.

Table 18-7. Micro Interface Timing

(V_{DD} = 3.3 ±5%, Tj = -40°C to 125°C.)

SIGNAL NAME(S)	SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS	NOTES
A[N:0]	t1a	Setup Time to $\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Active	10			ns	1
ALE	t1b	Setup Time to $\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Active	10			ns	1,2
A[N:0]	t2	Setup Time to ALE Inactive	2			ns	1,2
A[N:0]	t3	Hold Time from ALE Inactive	2			ns	1,2
ALE	t4	Pulse Width	5			ns	1,2
A[N:0], ALE	t5	Hold Time from $\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Inactive	0			ns	1
$\overline{CS}$, R/$\overline{W}$	t6	Setup Time to $\overline{RD}$, $\overline{WR}$ Active	0			ns	1
D[15:0]	t8	Output Delay Time from $\overline{RD}$, $\overline{DS}$ Active			30	ns	1
$\overline{RD}$, $\overline{WR}$, $\overline{DS}$	t9a	Pulse Width if not Using RDY Handshake	35			ns	1,4
$\overline{RD}$, $\overline{WR}$, $\overline{DS}$	t9b	Delay from RDY	15			ns	1
D[15:0]	t10	Output Deassert Delay Time from $\overline{RD}$, $\overline{DS}$ Inactive	2		10	ns	1,3
$\overline{CS}$, R/$\overline{W}$	t12	Hold Time from $\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Inactive	0			ns	1
D[15:0]	t13	Input Setup Time to $\overline{WR}$, $\overline{DS}$ Inactive	10			ns	1
D[15:0]	t14	Input Hold Time from $\overline{WR}$, $\overline{DS}$ Inactive	5			ns	1
RDY	t15	Delay Time from $\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Active	5			ns	1
RDY	t16	Delay Time from $\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Inactive	0			ns	1
RDY	t17	Enable Delay Time from $\overline{CS}$ Active			12	ns	1
RDY	t18	Disable Delay Time from $\overline{CS}$ Inactive			10	ns	1
RDY	t19	Ending High Pulse Width	1			ns	1
R/$\overline{W}$	t20	Setup Time to $\overline{DS}$ Active	2			ns	1
R/$\overline{W}$	t21	Hold Time to $\overline{DS}$ Inactive	2			ns	1

Note 1: The input/output timing reference level for all signals is VDD/2. Transition time (80/20%)on $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$ inputs is 5 ns max.

Note 2: Multiplexed mode timing only.

Note 3: D[15:0] output valid until not driven.

Note 4: Timing required if not using RDY handshake.

Figure 18-7. Micro Interface Nonmultiplexed Read/Write Cycle

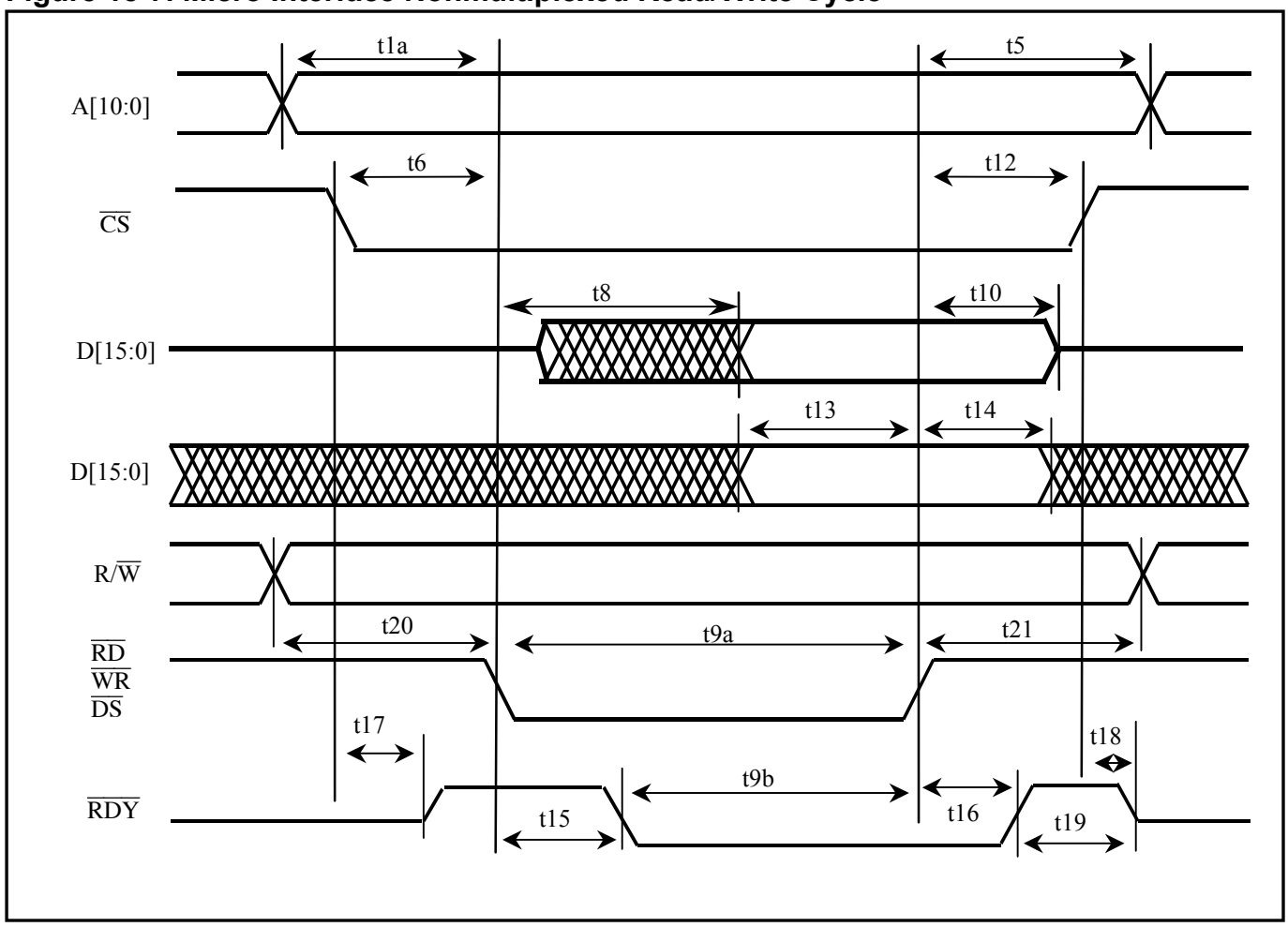
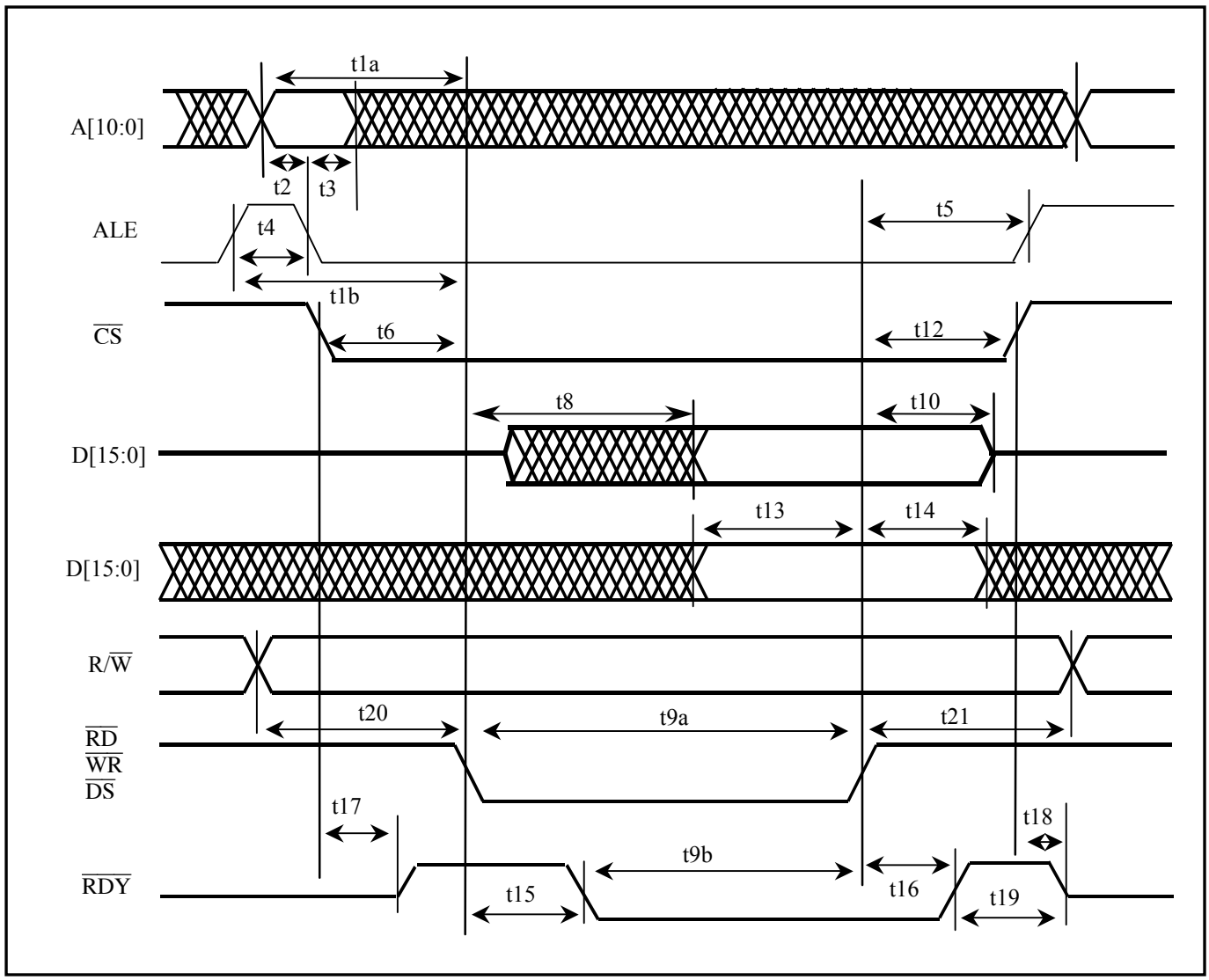


Figure 18-8. Micro Interface Multiplexed Read Cycle



18.7 CLAD Jitter Characteristics

PARAMETER	MIN	TYP	MAX	UNITS
Intrinsic Jitter (UI_{P-P})			0.025	UI_{P-P}
Intrinsic Jitter (UI_{RMS})			0.0045	UI_{RMS}
Peak Jitter Transfer			1.75	dB

18.8 JTAG Interface AC Characteristics

All AC timing characteristics are specified with a 50pF capacitive load on JTDO pin and 25pF capacitive load on all other digital output pins, V_{IH} = 2.4V and V_{IL} = 0.8V. The voltage threshold for all timing measurements is VDD/2. The generic timing definitions shown Figure 18-1, Figure 18-2, Figure 18-3, Figure 18-5, and Figure 18-6 apply to this interface.

Table 18-8. JTAG Interface Timing

(V_{DD} = 3.3V ±5%, T_j = -40°C to +125°C.)

SIGNAL NAME(S)	SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS	NOTES
JTCLK	f1	Clock Frequency (1/t1)	0		10	MHz	
JTCLK	t2	Clock High or Low Period	20			ns	
JTCLK	t3	Rise/Fall Times			5	ns	
JTMS and JTDI	t5	Hold Time from JTCLK Rising Edge	10			ns	
JTMS and JTDI	t6	Setup Time to JTCLK Rising Edge	10			ns	
JTDO	t7	Delay from JTCLK Falling Edge	0		20	ns	
JTDO	t8	Delay out of Hi-Z from JTCLK Falling Edge	0		20	ns	
JTDO	t9	Delay to Hi-Z from JTCLK Falling Edge	0		20	ns	
Any Digital Output	t7	Delay from JTCLK Falling Edge	0		20	ns	1
Any Digital Output	t7	Delay from JTCLK Rising Edge	0		20	ns	2
Any Digital Output	t8	Delay out of Hi-Z from JTCLK Falling Edge	0		20	ns	1
Any Digital Output	t9	Delay into Hi-Z from JTCLK Falling Edge	0		20	ns	1
Any Digital Output	t8	Delay out of Hi-Z from JTCLK Rising Edge	0		20	ns	2,3
Any Digital Output	t9	Delay into Hi-Z from JTCLK Rising Edge	0		20	ns	2,3

Note 1: Change during Update-DR state.

Note 2: Change during Update-IR state to or from EXTEST mode.

Note 3: Change during Update-IR state to or from HIZ mode.

19 REVISION HISTORY

REVISION	DESCRIPTION
072204	New product release (DS3164).
030905	New product releases (DS3161/DS3162/DS3163). Added power supply and power-down values for DS3161/2/3. Corrected register bit map (GL.RIORR). Clarified CP.TCR.TDSE and RCR.RDDE to state that DSS mode is only applicable for unframed modes and bit synchronous modes. Removed Note 3 from *DC Electrical Characteristics* since A2 fixes the problem with TEN and REN. Changed Input leakage for inputs with internal pullups from -300µA to -350µA. Added TLCLK to reference clock sources for TPOS/TNEG in *Line Interface AC Characteristics* table. Updated register bit map for PORT.INV. Corrected wording of use of unused bits located in *Overall Register Map* section. Added TLEN bit to PORT.CR2.
113006	Added lead-free package note to *Ordering Information* table (page 1). Updated Package Information (Section 15).

Maxim/Dallas Semiconductor cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim/Dallas Semiconductor product. No circuit patent licenses are implied. Maxim/Dallas Semiconductor reserves the right to change the circuitry and specifications without notice at any time.

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600

© 2005 Maxim Integrated Products • Printed USA

DALLAS SEMICONDUCTOR MAXIM are registered trademarks of Maxim Integrated Products, Inc., and Dallas Semiconductor Corporation.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View DS3164 on WIN SOURCE
- Maxim Integrated Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management