



**THE DATASHEET OF
FCD360N65S3R0**



FCD360N65S3R0

MOSFET – Power, N-Channel, SUPERFET III, Easy Drive

650 V, 10 A, 360 mΩ

Description

SUPERFET III MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III MOSFET Easy drive series helps manage EMI issues and allows for easier design implementation.

Features

- 700 V @ $T_J = 150^\circ\text{C}$
- Typ. $R_{DS(on)} = 310\text{ m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 18\text{ nC}$)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)} = 173\text{ pF}$)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

Applications

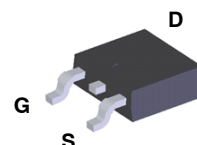
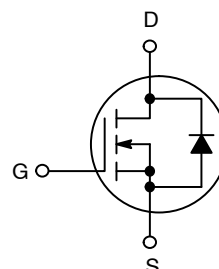
- Computing / Display Power Supplies
- Telecom / Server Power Supplies
- Industrial Power Supplies
- Lighting / Charger / Adapter



ON Semiconductor®

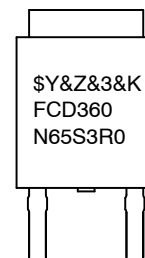
www.onsemi.com

V_{DSS}	$R_{DS(on)}\text{ MAX}$	$I_D\text{ MAX}$
650 V	360 mΩ @ 10 V	10 A



D-PAK
TO-252
CASE 369AS

MARKING DIAGRAM



\$Y = ON Semiconductor Logo
&Z = Assembly Plant Code
&3 = Data Code (Year & Week)
&K = Lot
FCD360N65S3R0 = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FCD360N65S3R0

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise noted)

Symbol	Parameter	Value	Unit
V _{DSS}	Drain to Source Voltage	650	V
V _{GSS}	Gate to Source Voltage	- DC	±30
		- AC (f > 1 Hz)	±30
I _D	Drain Current:	- Continuous (T _C = 25°C)	10
		- Continuous (T _C = 100°C)	6
I _{DM}	Drain Current:	- Pulsed (Note 1)	25
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	40	mJ
I _{AS}	Avalanche Current (Note 2)	2.1	A
E _{AR}	Repetitive Avalanche Energy (Note 1)	0.83	mJ
dv/dt	MOSFET dv/dt	100	V/ns
	Peak Diode Recovery dv/dt (Note 3)	20	
P _D	Power Dissipation	(T _C = 25°C)	83
		Derate Above 25°C	0.67
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150	°C
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I_{AS} = 2.1 A, R_G = 25 Ω, starting T_J = 25 °C.
3. I_{SD} ≤ 5 A, di/dt ≤ 200 A/μS, V_{DD} ≤ 400 V, starting T_J = 25 °C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max.	1.5	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient, Max. Note 4)	52	

4. Device on 1 in² pad 2 oz copper pad on 1.5 x 1.5 in. board of FR-4 material.

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity [†]
FCD360N65S3R0	FCD360N65S3R0	TO-252	Tape and Reel	330 mm	16 mm	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	V _{GS} = 0 V, I _D = 1 mA, T _J = 25°C	650	–	–	V
		V _{GS} = 0 V, I _D = 1 mA, T _J = 150°C	700	–	–	V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 1 mA, Referenced to 25°C	–	0.68	–	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 650 V, V _{GS} = 0 V	–	–	1	μA
		V _{DS} = 520 V, T _C = 125°C	–	0.58	–	
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±30 V, V _{DS} = 0 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 0.2 mA	2.5	–	4.5	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 5 A	–	310	360	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 5 A	–	6	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 400 V, V _{GS} = 0 V, f = 1 MHz	–	730	–	pF
C _{oss}	Output Capacitance		–	15	–	pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	–	173	–	pF
C _{oss(er.)}	Energy Related Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	–	26	–	pF
Q _{g(tot)}	Total Gate Charge at 10V	V _{DS} = 400 V, I _D = 5 A, V _{GS} = 10 V (Note 5)	–	18	–	nC
Q _{gs}	Gate to Source Gate Charge		–	4.3	–	nC
Q _{gd}	Gate to Drain "Miller" Charge		–	7.6	–	nC
ESR	Equivalent Series Resistance	f = 1 MHz	–	1	–	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 400 V, I _D = 5 A, V _{GS} = 10 V, R _g = 4.7 Ω (Note 5)	–	12	–	ns
t _r	Turn-On Rise Time		–	11	–	ns
t _{d(off)}	Turn-Off Delay Time		–	34	–	ns
t _f	Turn-Off Fall Time		–	10	–	ns

SOURCE-DRAIN DIODE CHARACTERISTICS

I _S	Maximum Continuous Source to Drain Diode Forward Current	–	–	10	A	
I _{SM}	Maximum Pulsed Source to Drain Diode Forward Current	–	–	25	A	
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 5 A	–	–	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 5 A, dI _F /dt = 100 A/μs	–	241	–	ns
Q _{rr}	Reverse Recovery Charge		–	2.4	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

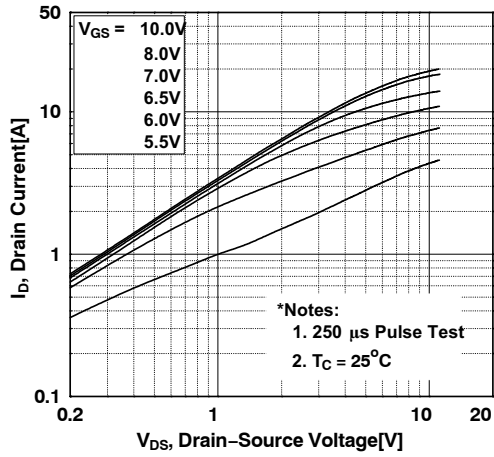


Figure 1. On-Region Characteristics

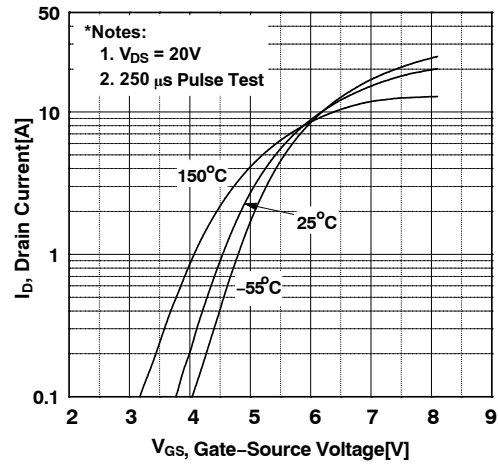


Figure 2. Transfer Characteristics

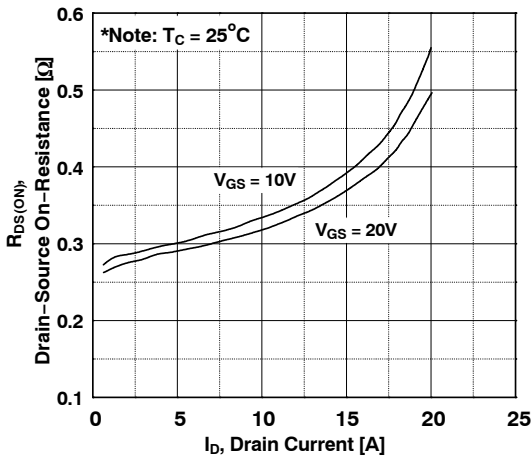


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

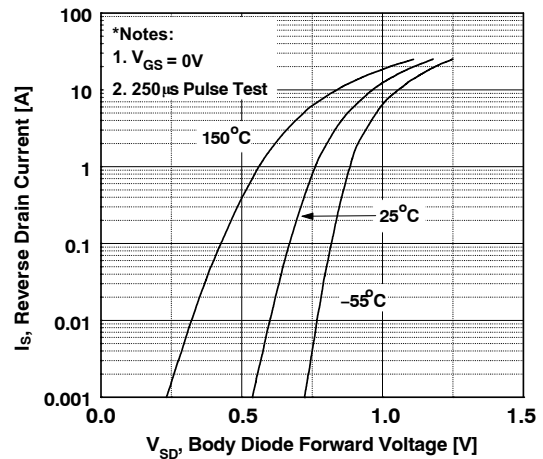


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

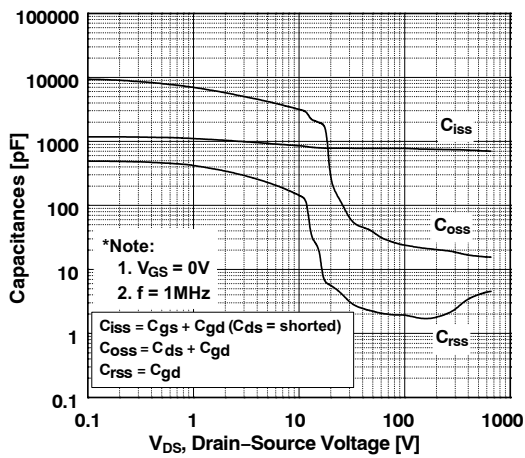


Figure 5. Capacitance Characteristics

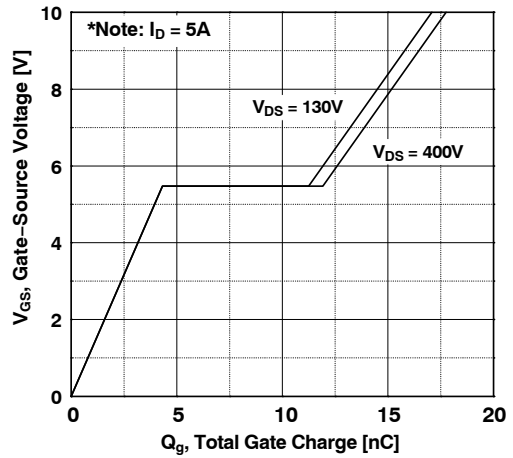


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

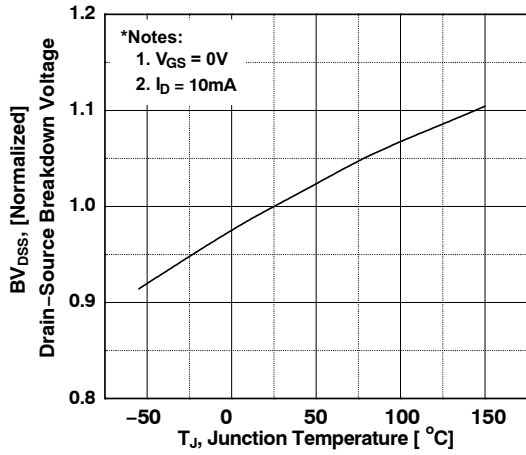


Figure 7. Breakdown Voltage Variation vs. Temperature

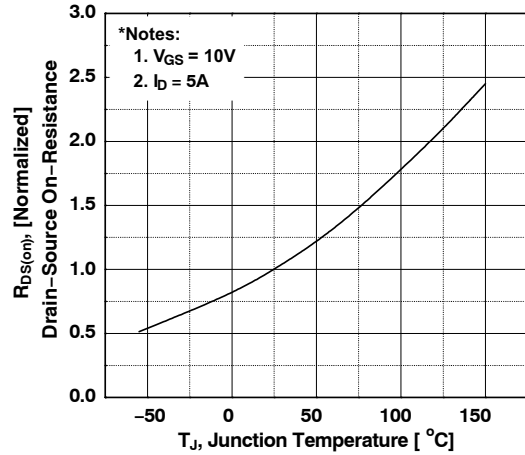


Figure 8. On-Resistance Variation vs. Temperature

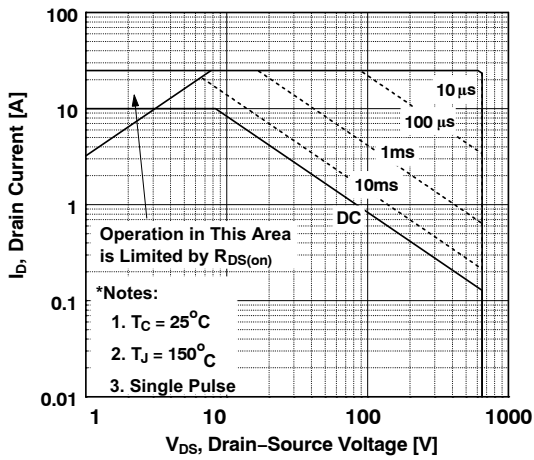


Figure 9. Maximum Safe Operating Area

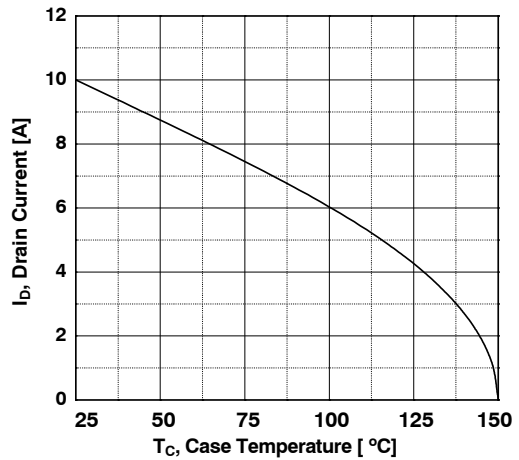


Figure 10. Maximum Drain Current vs. Case Temperature

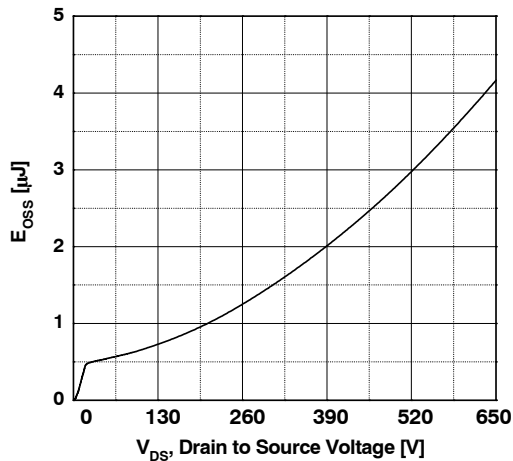


Figure 11. E_{oss} vs. Drain to Source Voltage

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TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

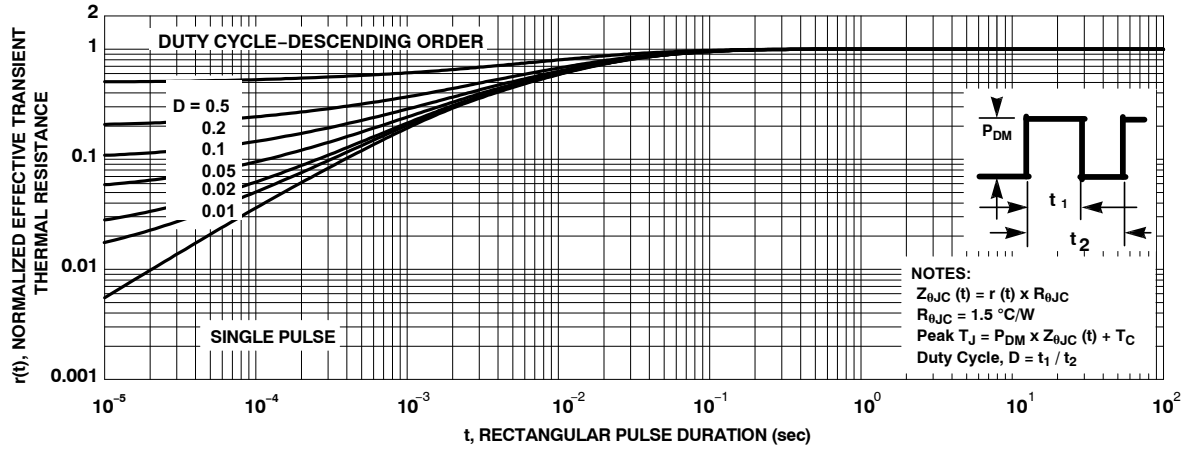


Figure 12. Transient Thermal Response Curve

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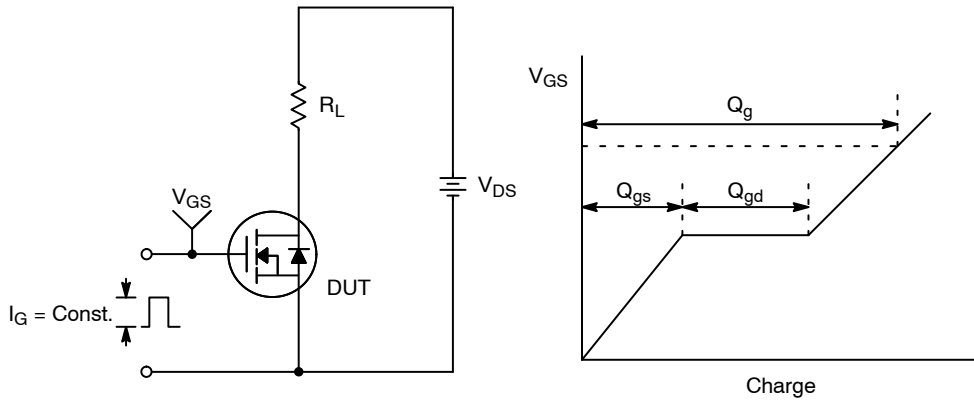


Figure 13. Gate Charge Test Circuit & Waveform

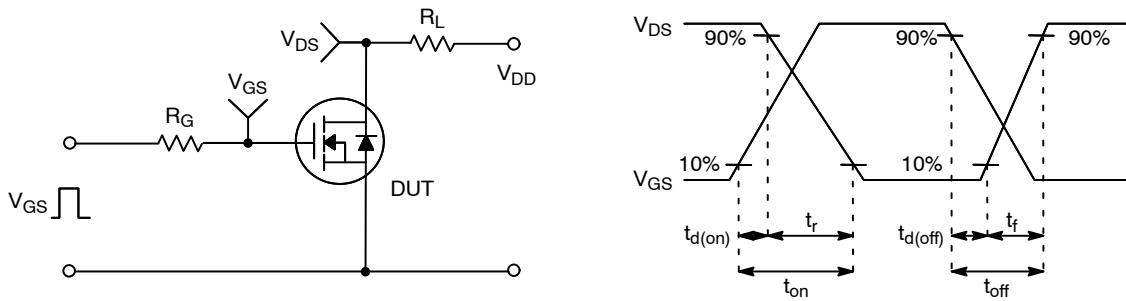


Figure 14. Resistive Switching Test Circuit & Waveforms

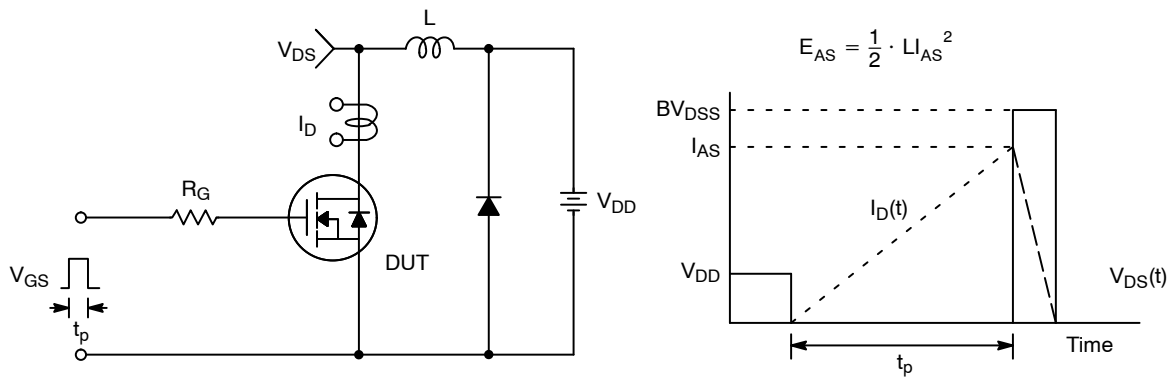


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

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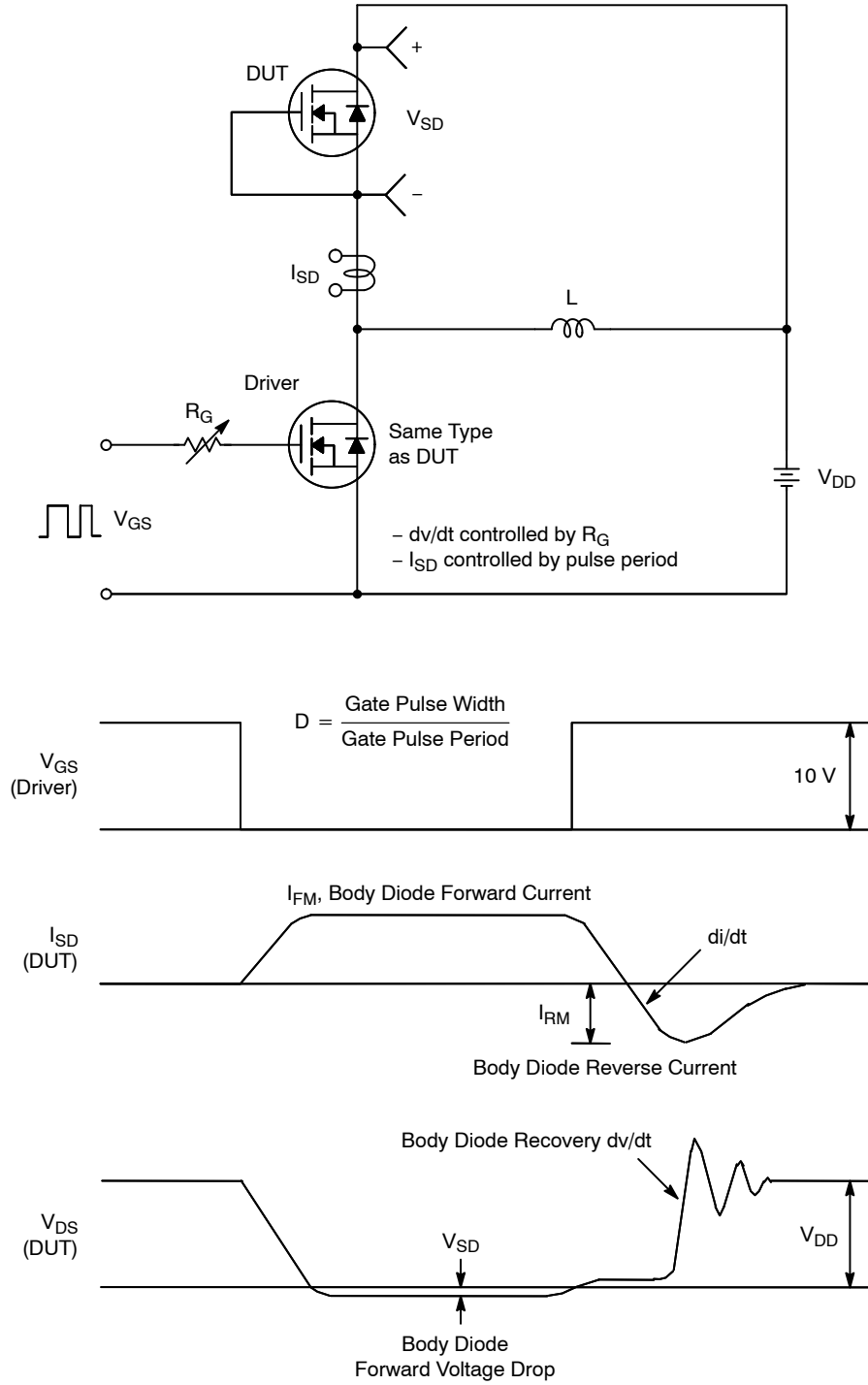
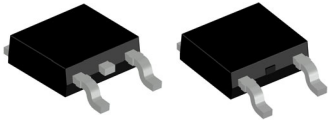


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

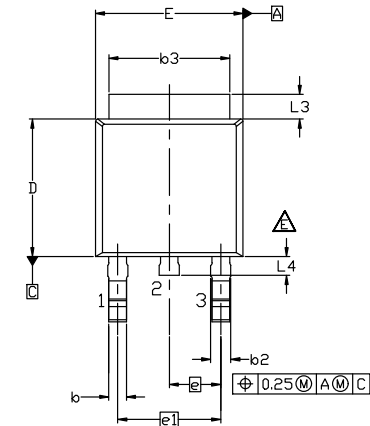
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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

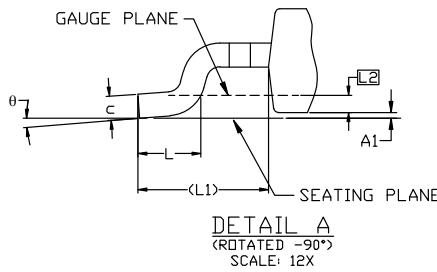
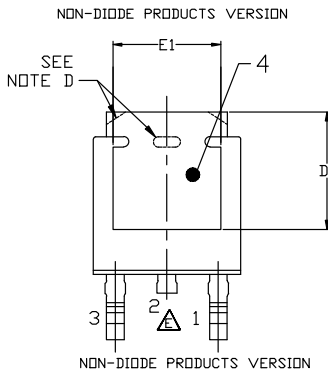


DPAK3 6.10x6.54x2.29, 4.57P CASE 369AS ISSUE B

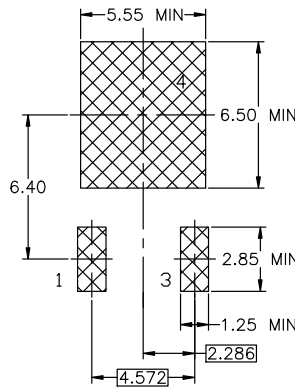
DATE 20 DEC 2023



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE F, VARIATION AA.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2018.
 - D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
 - E) FOR DIODE PRODUCTS, L4 IS 0.25 MM MAX PLASTIC BODY STUB WITHOUT CENTER LEAD.
 - F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
 - G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TD228P991X239-3N.



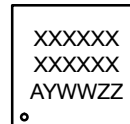
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.18	2.29	2.39
A1	0.00	-	0.127
b	0.64	0.77	0.89
b2	0.76	0.95	1.14
b3	5.21	5.34	5.46
c	0.45	0.53	0.61
c2	0.45	0.52	0.58
D	5.97	6.10	6.22
D1	5.21	---	---
E	6.35	6.54	6.73
E1	4.32	---	---
e	2.286 BSC		
e1	4.572 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	1.08	1.27
L4	---	---	1.02
θ	0°	---	10°



LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

GENERIC MARKING DIAGRAM*



*This information is generic. Please refer to device data sheet for actual part marking. Pb-free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

XXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ZZ = Assembly Lot Code

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