



**THE DATASHEET OF  
FDMC8010DC**



# MOSFET – N-Channel, DUAL COOL<sup>®</sup> 33, POWERTRENCH<sup>®</sup> 30 V, 157 A, 1.28 mΩ

## FDMC8010DC



PQFN8 3.3X3.3, 0.65P  
CASE 483AY  
DUAL COOL 33

### General Description

This N-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process. Advancements in both silicon and DUAL COOL package technologies have been combined to offer the lowest  $r_{DS(on)}$  while maintaining excellent switching performance by extremely low Junction-to-Ambient thermal resistance.

### Features

- DUAL COOL Top Side Cooling PQFN Package
- Max  $r_{DS(on)}$  = 1.28 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 37\text{ A}$
- Max  $r_{DS(on)}$  = 1.74 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 32\text{ A}$
- High Performance Technology for Extremely Low  $r_{DS(on)}$
- These Devices are Pb-Free and are RoHS Compliant

### Applications

- Load Switch
- Motor Bridge Switch
- Synchronous Rectifier

### MOSFET MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

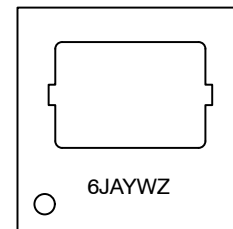
Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage (Note 4)	$\pm 20$	V
$I_D$	Drain Current		A
	–Continuous $T_C = 25^\circ\text{C}$ (Note 6)	157	
	–Continuous $T_C = 100^\circ\text{C}$ (Note 6)	99	
	–Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	37	
	–Pulsed (Note 5)	788	
EAS	Single Pulse Avalanche Energy (Note 3)	337	mJ
$P_D$	Power Dissipation $T_C = 25^\circ\text{C}$	50	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	3.0	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

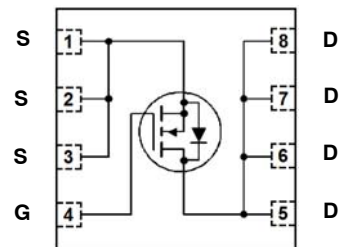
Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Bottom Drain)	2.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	42	

### MARKING DIAGRAM



- 6J = Specific Device Code
- A = Assembly Plant Code
- YW = Date Code (Year and Week)
- Z = Lot Code

### PIN CONNECTIONS



### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 2 of this data sheet.

# FDMC8010DC

## PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Quantity
FDMC8010DC	6J	DUAL COOL 33	13"	12 mm	3000 Units

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V	30			V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25°C		15		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V			10	μA
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V			100	nA

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	1.0	1.4	3.0	V
ΔV <sub>GS(th)</sub> /ΔT <sub>J</sub>	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25°C		-5		mV/°C
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 37 A		0.91	1.28	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 32 A		1.2	1.74	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 37 A, T <sub>J</sub> = 125°C		1.34	1.89	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 37 A		231		S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz		4720	7080	pF
C <sub>oss</sub>	Output Capacitance			1540	2310	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			136	205	pF
R <sub>g</sub>	Gate Resistance		0.1	0.5	1.1	Ω

### SWITCHING CHARACTERISTICS

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 37 A, V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω		15	26	ns
t <sub>r</sub>	Rise Time			7	14	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			40	64	ns
t <sub>f</sub>	Fall Time			5	10	ns
Q <sub>g(TOT)</sub>	Total Gate Charge at 10 V	V <sub>DD</sub> = 15 V I <sub>D</sub> = 37 A		67	94	nC
Q <sub>g(TOT)</sub>	Total Gate Charge at 4.5 V			32	44	nC
Q <sub>gs</sub>	Gate to Source Charge			10		nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge			7.5		nC

### DRAIN-SOURCE DIODE CHARACTERISTICS

V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 2.3 A (Note 2)		0.7	1.2	V
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = 37 A (Note 2)		0.8	1.3	
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 37 A, di/dt = 100 A/μs		55	88	ns
Q <sub>rr</sub>	Reverse Recovery Charge			48	76	nC

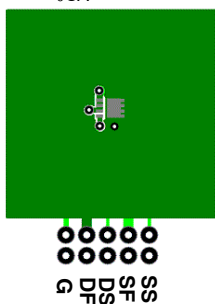
# FDMC8010DC

## THERMAL CHARACTERISTICS

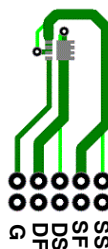
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Top Source)	5.0	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Bottom Drain)	2.5	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	42	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	105	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1c)	29	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1d)	40	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1e)	19	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1f)	23	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1g)	30	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1h)	79	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1i)	17	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1j)	26	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1k)	12	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1l)	16	

### NOTES:

- $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a. 42°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 105°C/W when mounted on a minimum pad of 2 oz copper

- Still air, 20.9x10.4x12.7 mm Aluminum Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper.
  - Still air, 20.9x10.4x12.7 mm Aluminum Heat Sink, minimum pad of 2 oz copper.
  - Still air, 45.2x41.4x11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper.
  - Still air, 45.2x41.4x11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper.
  - 200FPM Airflow, No Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper.
  - 200FPM Airflow, No Heat Sink, minimum pad of 2 oz copper.
  - 200FPM Airflow, 20.9x10.4x12.7 mm Aluminum Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper.
  - 200FPM Airflow, 20.9x10.4x12.7 mm Aluminum Heat Sink, minimum pad of 2 oz copper.
  - 200FPM Airflow, 45.2x41.4x11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in<sup>2</sup> pad of 2 oz copper.
  - 200FPM Airflow, 45.2x41.4x11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper.
- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
  - $E_{AS}$  of 337 mJ is based on starting  $T_J = 25^\circ\text{C}$ ,  $L = 3$  mH,  $I_{AS} = 15$  A,  $V_{DD} = 30$  V,  $V_{GS} = 10$  V, 100% test at  $L = 0.1$  mH,  $I_{AS} = 49$  A.
  - As an N-ch device, the negative  $V_{GS}$  rating is for low duty cycle pulse occurrence only. No continuous rating is implied.
  - Pulse  $I_d$  measured at 250 μs, refer to Figure 11 SOA graph for more details.
  - Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

TYPICAL CHARACTERISTICS

$T_J = 25^\circ\text{C}$  Unless Otherwise Noted

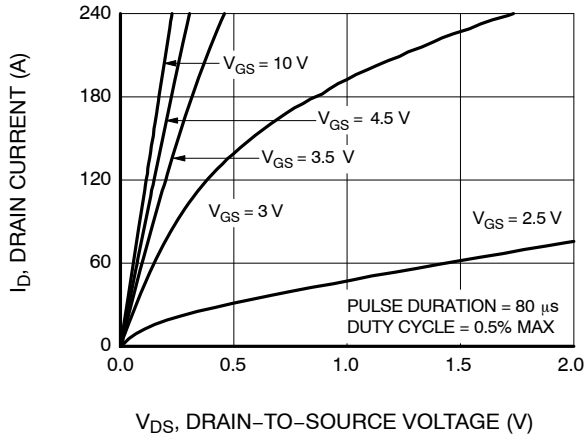


Figure 1. On-Region Characteristics

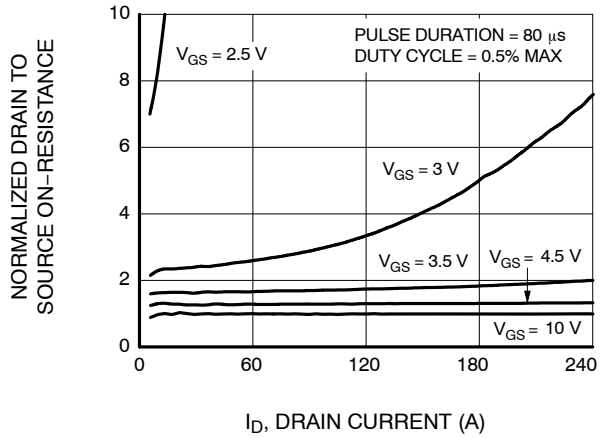


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

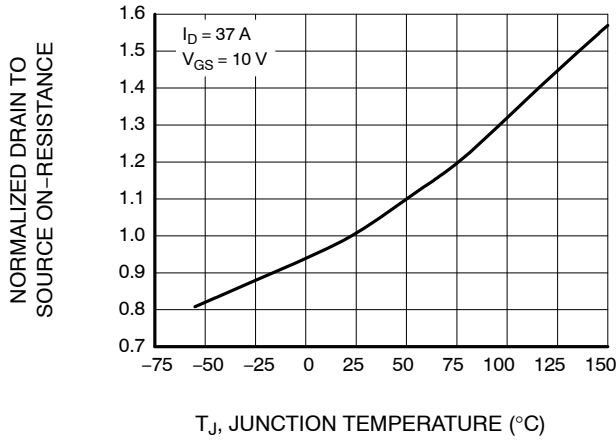


Figure 3. Normalized On Resistance vs Junction Temperature

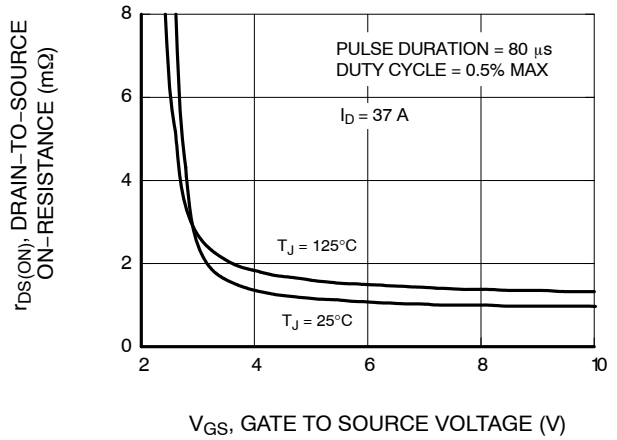


Figure 4. On-Resistance vs Gate to Source Voltage

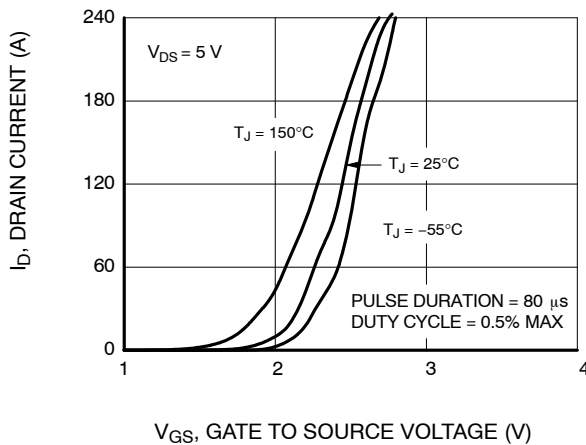


Figure 5. Transfer Characteristics

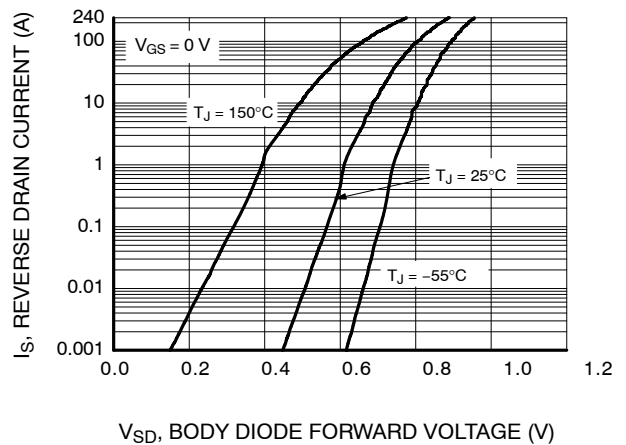


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

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## TYPICAL CHARACTERISTICS (continued)

$T_J = 25^\circ\text{C}$  Unless Otherwise Noted

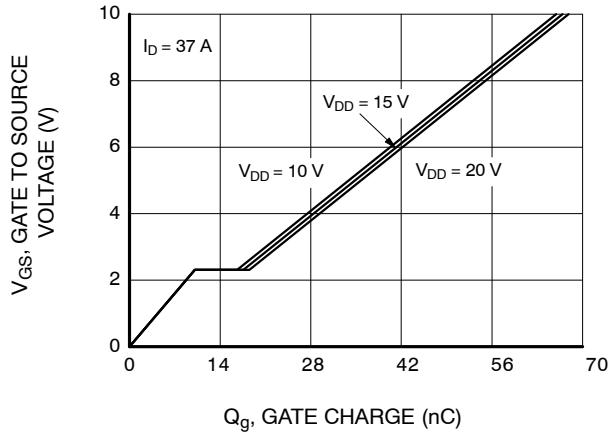


Figure 7. Gate Charge Characteristics

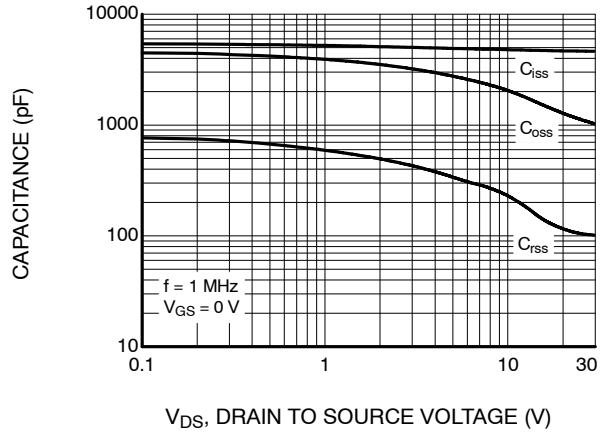


Figure 8. Capacitance vs Drain to Source Voltage

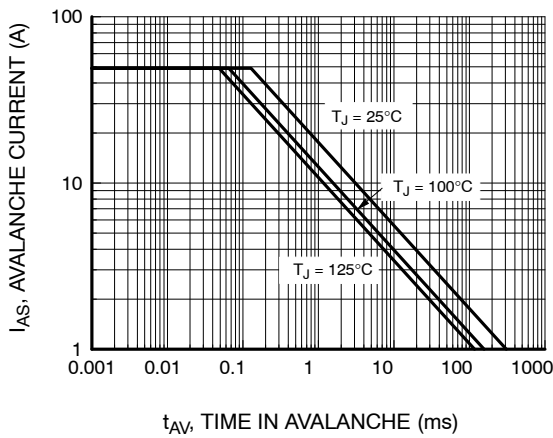


Figure 9. Unclamped Inductive Switching Capability

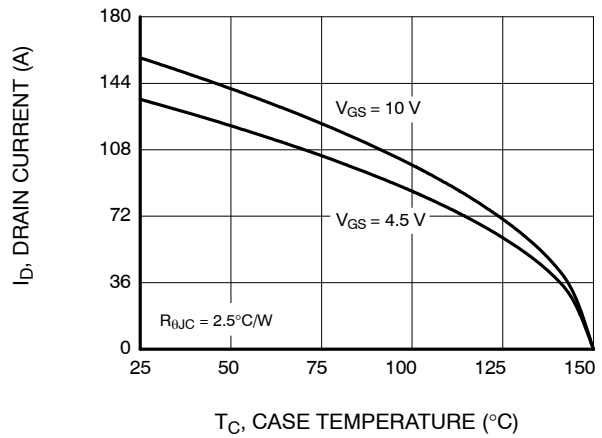


Figure 10. Maximum Continuous Drain Current vs Case Temperature

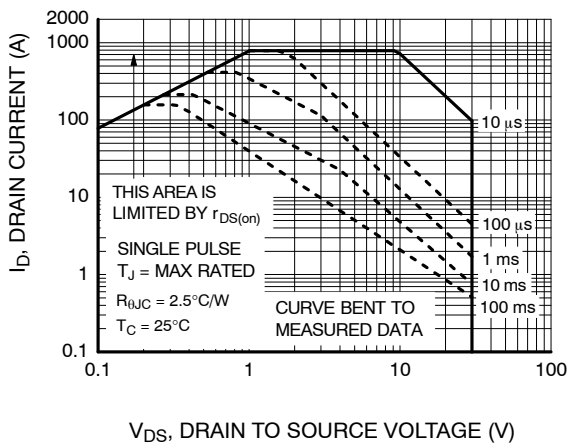


Figure 11. Forward Bias Safe Operating Area

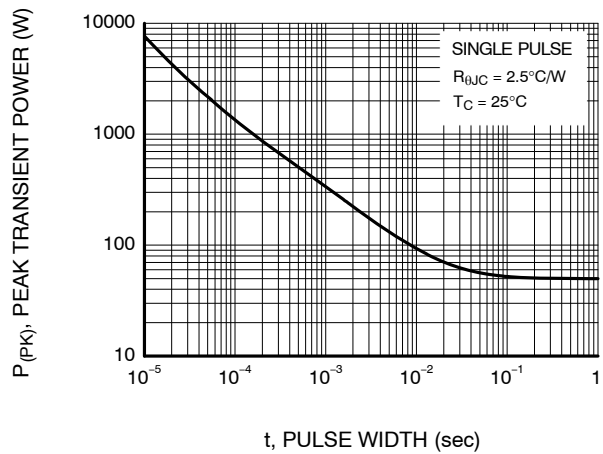
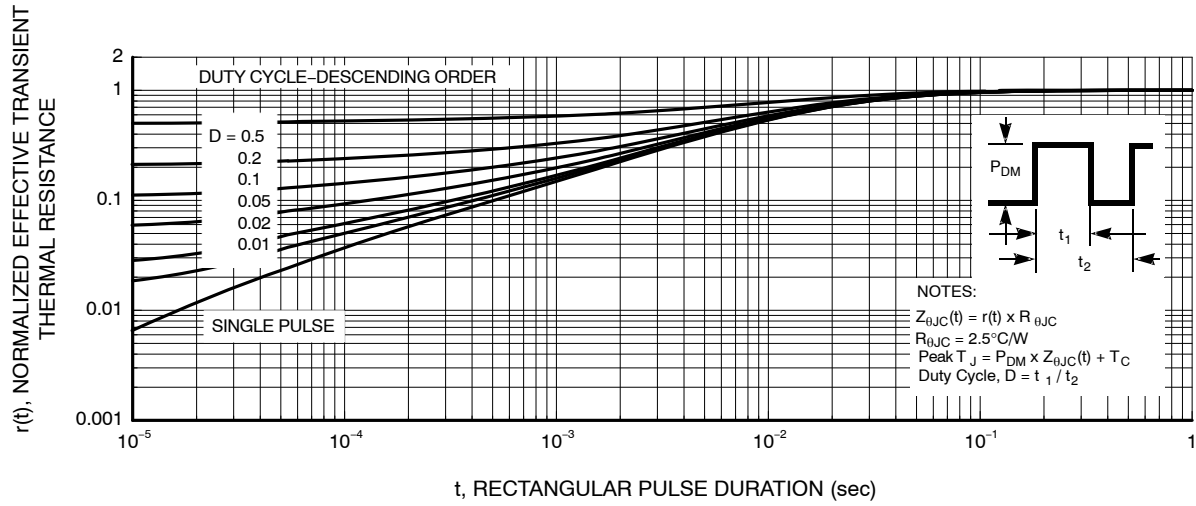


Figure 12. Single Pulse Maximum Power Dissipation

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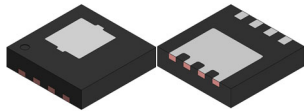
## TYPICAL CHARACTERISTICS (continued)

$T_J = 25^\circ\text{C}$  Unless Otherwise Noted



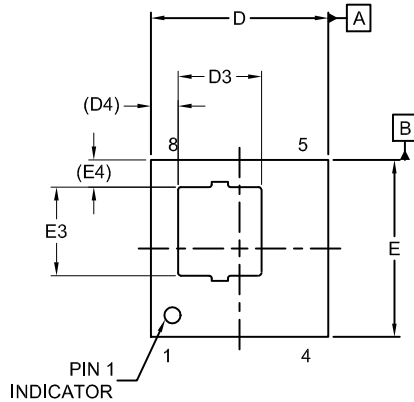
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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

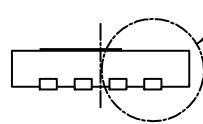


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ISSUE A

DATE 08 SEP 2021



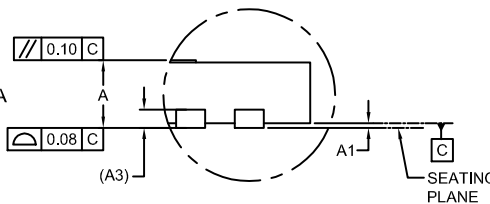
TOP VIEW



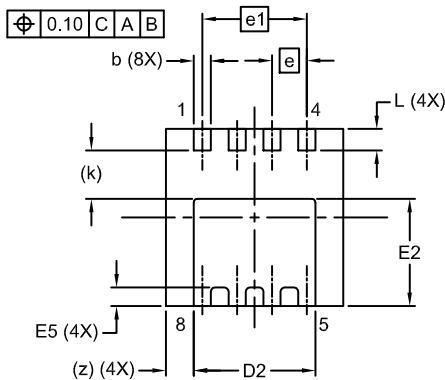
FRONT VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

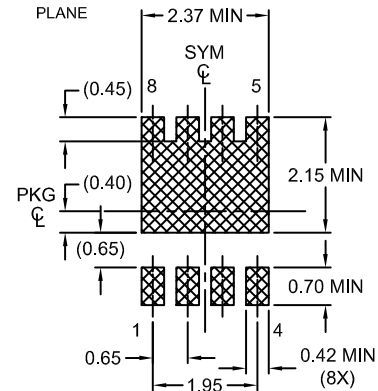


DETAIL A  
SCALE: 2X



BOTTOM VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.20 REF		
b	0.27	0.32	0.37
D	3.20	3.30	3.40
D2	2.17	2.27	2.37
D3	1.45	1.55	1.65
D4	0.51 REF		
E	3.20	3.30	3.40
E2	1.85	1.95	2.05
E3	1.55	1.65	1.75
E4	0.51 REF		
E5	0.24	0.34	0.44
e	0.65 BSC		
e1	1.95 BSC		
k	0.90 REF		
L	0.30	0.40	0.50
z	0.52 REF		



LAND PATTERN  
RECOMMENDATION

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