THE DATASHEET OF

IR3820AMTR1PBF

Sup*IR*Buck™

HIGHLY INTEGRATED 14A
WIDE-INPUT VOLTAGE, SYNCHRONOUS BUCK REGULATOR

Features

- Wide Input Voltage Range 2.5V to 21V
- Wide Output Voltage Range 0.6V to 12V
- Continuous 14A Load Capability
- 300kHz High Frequency Operation
- Programmable Over-Current Protection
- Programmable PGood Output
- Hiccup Current Limit
- Precision Reference Voltage (0.6V)
- Programmable Soft-Start
- Pre-Bias Start-up
- Thermal Protection
- Thermally Enhanced Package
- Small Size 5mmx6mm QFN
- Pb-Free (RoHS Compliant)

Applications

- Distributed Point-of-Loads
- Server and Workstations
- Embedded Systems
- Storage Systems
- DDR Applications
- Graphics Cards
- Game Consoles
- Computing Peripheral Voltage Regulators

Description

The IR3820A **Sup*IR*Buck*TM*** is an easy-to-use, fully integrated and highly efficient DC/DC regulator. The onboard switching controller and MOSFETs make the IR3820A a space-efficient solution, providing accurate power delivery for low output voltage applications.

The IR3820A operates from a single 4.5V to 14V input supply and generates an output voltage adjustable from 0.6V to 0.8*Vin at loads up to 14A.

A versatile regulator offering programmability of startup time, power good threshold and current limit, the IR3820A's fixed 300kHz switching frequency allows the use of small external components.

The IR3820A also features important protection functions, such as Pre-Bias startup, hiccup current limit and thermal shutdown to provide the required system level security in the event of fault conditions.

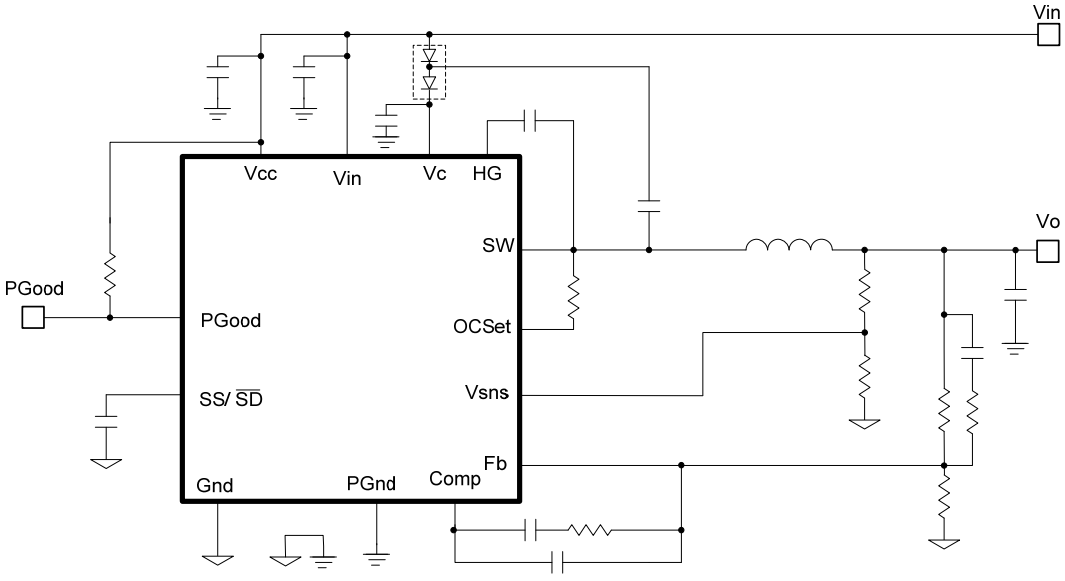


Fig. 1. Typical application diagram

ABSOLUTE MAXIMUM RATINGS

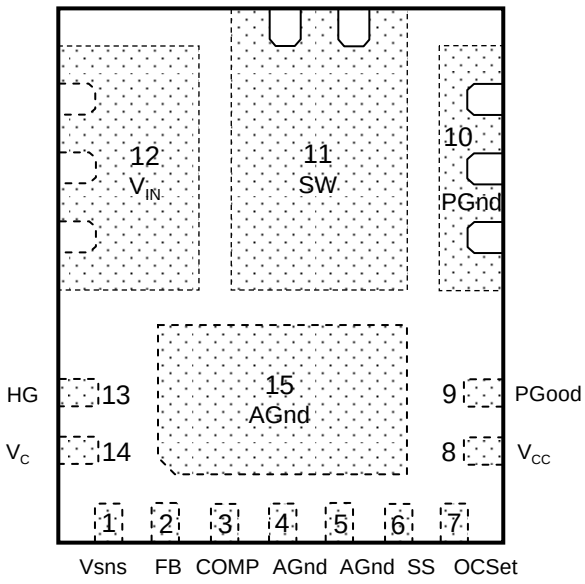
(Voltages referenced to GND)

- V_{IN} Supply Voltage ---------- -0.3V to 24V
- Vcc Supply Voltage ---------- -0.3V to 16V
- Vc Supply Voltage ---------- -0.3V to 30V
- SW ---------- -0.3V to 30V
- PGood ---------- -0.3V to 16V
- Fb,COMP,SS,Vsns ---------- -0.3V to 3.5V
- OCSet ---------- 10mA
- AGnd to PGnd ---------- -0.3V to +0.3V
- Storage Temperature Range ---------- -65°C To 150°C
- Operating Junction Temperature Range ---------- -40°C To 150°C
- ESD Classification ---------- JEDEC, JESD22-A114
- Moisture Sensitivity Level ---------- JEDEC Level 3 @ 260ºC

Caution: *Stresses beyond those listed under "Absolute Maximum Rating" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to "Absolute Maximum Rating" conditions for extended periods may affect device reliability.*

PACKAGE INFORMATION

5mm x 6mm POWER QFN



$\theta_{JA} = 35°C/W$

$\theta_{J\text{-}PCB} = 2°C/W$

Fig. 2: Package outline (Top view)

ORDERING INFORMATION

PACKAGE DESIGNATOR	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER REEL
M	IR3820AMTRPbF	15	4000
M	IR3820AMTR1PbF	15	750

Block Diagram

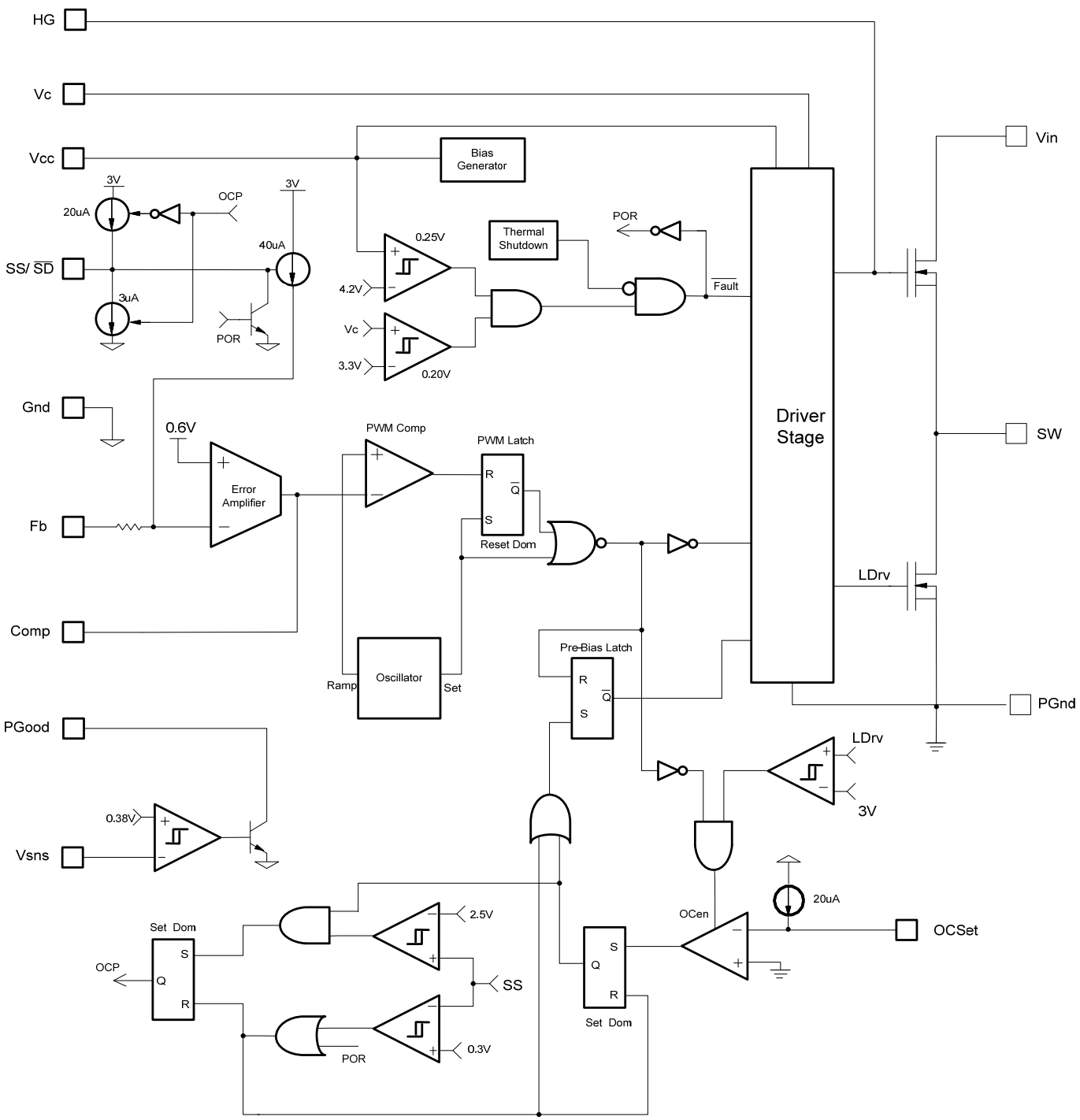


Fig. 3. Simplified block diagram of the IR3820A.

Pin Description

Pin	Name	Description
1	Vsns	PGood sense pin. Use two external resistors to program the power good threshold.
2	Fb	Inverting input to the error amplifier. This pin is connected directly to the output of the regulator via resistor divider to set the output voltage and provide feedback to the error amplifier.
3	Comp	Output of error amplifier.
4	AGnd	Signal ground for internal reference and control circuitry.
5	AGnd	Signal ground for internal reference and control circuitry.
6	SS/SD	Soft start / shutdown. This pin provides user programmable soft-start function. Connect an external capacitor from this pin to signal ground (AGnd) to set the start up time of the output voltage. The converter can be shutdown by pulling this pin below 0.3V.
7	OCSet	Current limit set point. A resistor from this pin to SW pin will set the current limit threshold.
8	V_{CC}	This pin provides biasing voltage for the internal blocks of the IC. It also powers the low side driver. A minimum of 0.1uF, high frequency capacitor must be connected from this pin to power ground (PGnd).
9	PGood	Power Good status pin. Output is open collector. Connect a pull up resistor from this pin to Vcc.
10	PGnd	Power Ground. This pin serves as a separated ground for the MOSFET drivers and should be connected to the system's power ground plane.
11	SW	Switch node. This pin is connected to the output inductor
12	V_{IN}	Input voltage connection pin
13	HG	This pin is connected to the high side Mosfet gate. Connect a small capacitor from this pin to switch node (SW).
14	V_C	This pin powers the high side driver and must be connected to a voltage higher than input voltage. A minimum of 0.1uF high frequency capacitor must be connected from this pin to the power ground (PGnd).
15	AGnd	Signal ground for internal reference and control circuitry.

Pins 4, 5 and 15 need to be connected together on system board.

Recommended Operating Conditions

Symbol	Definition	Min	Max	Units
V_{in}	Input Voltage	2.5	21	V
V_{cc}	Supply Voltage	4.5	14	
V_c	Supply Voltage	Vin + 5V	28	
V_o	Output Voltage	0.6	12	
I_o *Note1*	Output Current	0	14	A
T_j	Junction Temperature	-40	125	°C

Electrical Specifications

Unless otherwise specified, these specification apply over Vin=V_{cc}=V_c=12V, 0°C<T_j(Ic)<105°C.
Typical values are specified at T_a = 25°C.

Parameter	Symbol	Test Condition	Min	TYP	MAX	Units
Power Loss						
Power Loss	P_{loss}	Vcc=V_{in}=12V, Vc=24V, V_o=1.8V, I_o=14A, L=1.0uH, *Note3*		3.7		W
MOSFET $R_{ds(on)}$						
Top Switch	$R_{ds(on)\_Top}$	I_D=13A, Tj(MOSFET)=25°C		6.9	8.7	mΩ
Bottom Switch	$R_{ds(on)\_Bot}$	I_D=13A, Tj(MOSFET)=25°C		6.9	8.7	
Reference Voltage						
Feedback Voltage	V_{FB}			0.6		V
Accuracy		0°C<Tj<105°C	-1.35		+1.35	%
		-40°C<Tj<105°C, *Note2*	-1.5		+1.5	%
Supply Current						
V_{CC} Supply Current (Static)	$I_{CC(Static)}$	SS=0V, No Switching		10	13	mA
V_C Supply Current (Static)	$I_{C(Static)}$	SS=0V, No Switching		4.5	7	
V_{CC} Supply Current (Dynamic)	$I_{CC(Dynamic)}$	SS=3V, V_c=24V, V_{cc}=V_{in}=12V. V_o=1.8V, Io=0A		15	22	
V_C Supply Current (Dynamic)	$I_{C(Dynamic)}$	SS=3V, V_c=24V, V_{cc}=V_{in}=12V. V_o=1.8V, Io=0A		15	22	
Under Voltage Lockout						
V_{CC}-Start-Threshold	V_{CC}_UVLO(R)	Supply ramping up	4.0		4.4	V
V_{CC}-Stop-Threshold	V_{CC}_UVLO(F)	Supply ramping down	3.7		4.1	
V_{CC}-Hysteresis		Supply ramping up and down	0.15	0.25	0.3	
V_C-Start-Threshold	V_C_UVLO(R)	Supply ramping up	3.1		3.5	
V_C-Stop-Threshold	V_C_UVLO(F)	Supply ramping down	2.85		3.25	
V_C-Hysteresis		Supply ramping up and down	0.15	0.2	0.25	

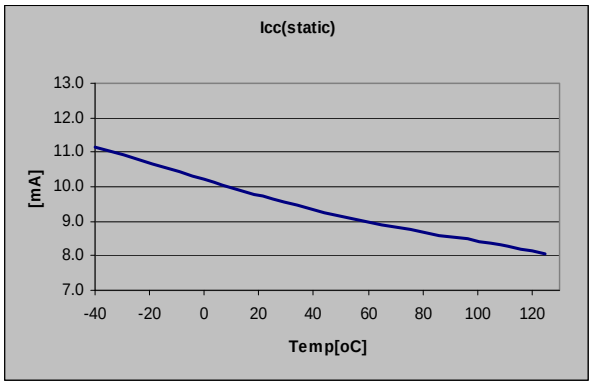
Parameter	SYM	Test Condition	Min	TYP	MAX	Units
Oscillator						
Frequency	F_S		270	300	330	kHz
Ramp Amplitude	V_{ramp}	*Note3*		1.25		V
Min Pulse Width	$D_{min(ctrl)}$	*Note3*		80		ns
Max Duty Cycle	D_{max}	Fb=0V	80			%
Error Amplifier						
Input Bias Current	I_{FB1}	SS=3V		-0.1	-0.5	µA
Input Bias Current	I_{FB2}	SS=0V	20	35	50	µA
Source/Sink Current	I(source/Sink)		50	70	90	µA
Transconductance	gm		1000	1300	1600	µmho
Soft Start/SD						
Soft Start Current	I_{SS}	SS=0V	15	20	28	µA
Shutdown Output Threshold	SD				0.25	V
Power Good						
Vsns Low Trip Point	Vsns(trip)	Vsns Ramping Down	0.35	0.38	0.41	V
Hysteresis	PGood(Hys)		15	27.5	40	mV
PGood Output Low Voltage	PG(voltage)	I_{PGood}=4mA		0.25	0.5	V
Input Bias Current	Isns		0	0.3	1	µA
Over Current Protection						
OCSET Current	I_{OCSET}		15	20	26	µA
Hiccup Current	I_{Hiccup}	*Note3*		3		µA
Hiccup Duty Cycle	Hiccup(duty)	I_{Hiccup} / I_{SS} , *Note3*		15		%
Thermal Shutdown						
Thermal Shutdown Threshold		*Note3*		140		°C
Thermal Shutdown Hysteresis		*Note3*		20		°C

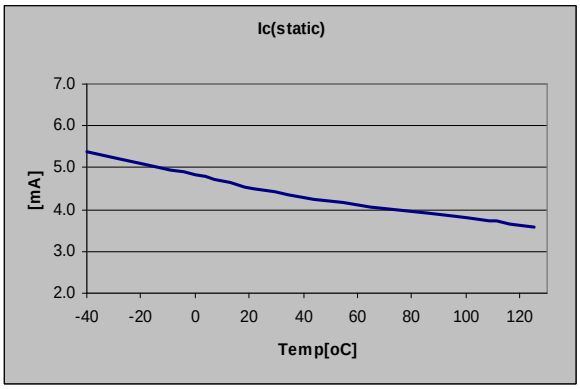
Note1: Continuous output current determined by input and output voltage setting and the thermal environment.

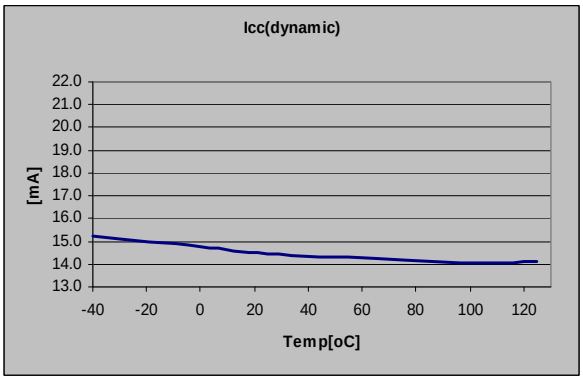
Note2: Cold temperature performance is guaranteed via correlation using statistical quality control. Not tested in production.

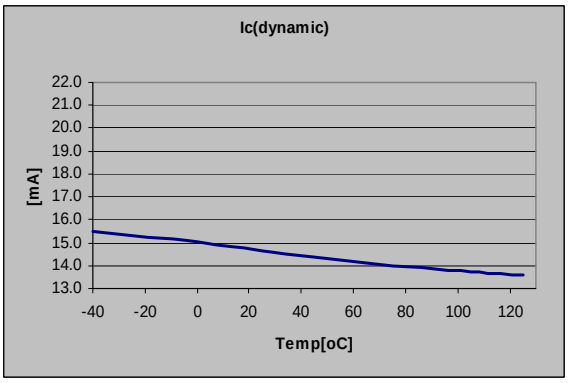
Note3: Guaranteed by Design but not tested in production.

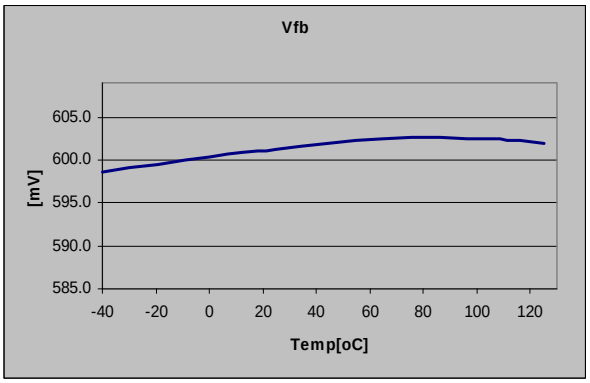
TYPICAL OPERATING CHARACTERISTICS (-40°C - 125°C)

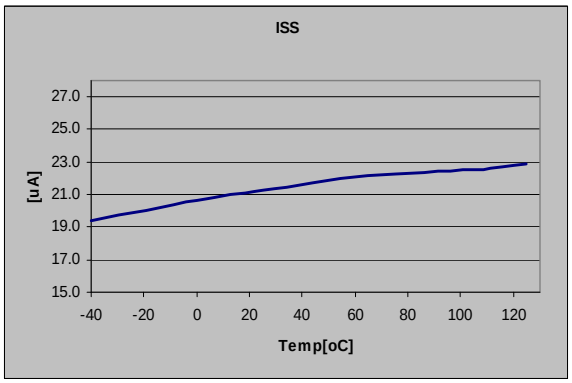


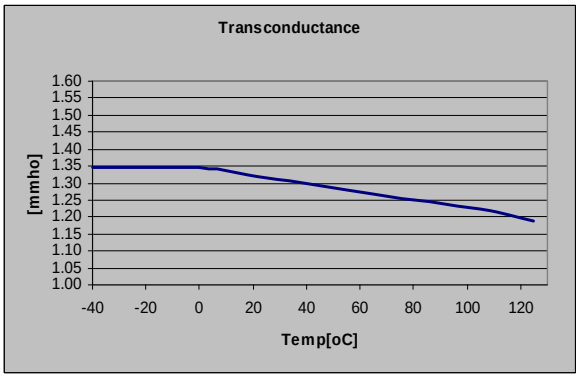


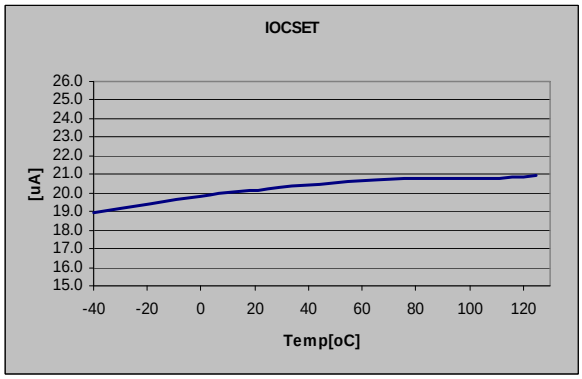












Circuit Description

THEORY OF OPERATION

The IR3820A is a voltage mode PWM synchronous regulator and operates with a fixed 300kHz switching frequency, allowing the use of small external components.

The output voltage is set by feedback pin (Fb) and the internal reference voltage (0.6V). These are two inputs to error amplifier. The error signal between these two inputs is amplified and it is compared to a fixed frequency linear sawtooth ramp.

A trailing edge modulation is used for generating fixed frequency pulses (PWM) which drives the internal N-channel MOSFETs.

The internal oscillator circuit uses on-chip circuitry, eliminating the need for external components.

The IR3820A operates with single input voltage from 4.5V to 14V allowing an extended operating input voltage range.

The over-current protection is performed by sensing current through the $R_{DS(on)}$ of low side MOSFET. This method enhances the converter's efficiency and reduces cost by eliminating a current sense resistor. The current limit is programmable by using an external resistor.

Under-Voltage Lockout

The under-voltage lockout circuit monitors the two input supplies (Vcc and Vc) and assures that the MOSFET driver outputs remain in the off state whenever the supply voltage drops below set thresholds. Lockout occurs if Vcc or Vc fall below 4.3V and 3.3V respectively. Normal operation resumes once Vcc and Vc rise above the set values.

Thermal Shutdown

Temperature sensing is provided inside the IR3820A. The trip threshold is typically set to 140°C. When trip threshold is exceeded, thermal shutdown turns off both MOSFETs. Thermal shutdown is not latched and automatic restart is initiated when the sensed temperature drops within the operating range. There is a 20°C hysteresis in the thermal shutdown threshold.

Pre-Bias Startup

The IR3820A is able to start up into pre-charged output, which prevents oscillation and disturbances of the output voltage.

The output starts in asynchronous fashion and keeps the synchronous MOSFET off until the first gate signal for control MOSFET is generated. Figure 4 shows a typical Pre-Bias condition at start up.

Depending on system configuration, a specific amount of output capacitors may be required to prevent discharging the output voltage.

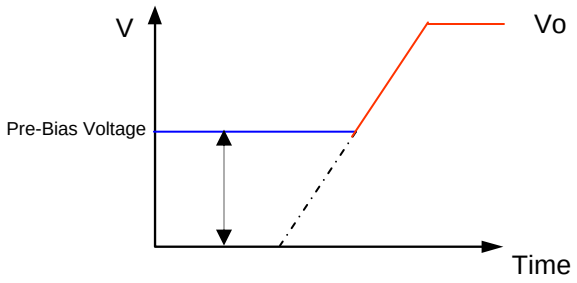


Fig. 4: Pre-Bias start up

Shutdown

The output can be shutdown by pulling the soft-start pin below 0.3V. This can easily be done by using an external small signal transistor. During shutdown both MOSFET drivers will be turned off. Normal operation will resume by cycling soft start pin.

Power Good

The IR3820A provides an open collector power good signal which reports the status of the output. The output is sensed through the dedicated Vsns pin. The power good threshold can be externally programmed using two external resistors. The power good comparator is internally set to 0.38V (typical).

Soft-Start

The IR3820A has programmable soft-start to control the output voltage rise and limit the inrush current during start-up.

To ensure correct start-up, the soft-start sequence initiates when Vcc and Vc rise above their threshold and generate the Power On Ready (POR) signal. The soft-start function operates by sourcing current to charge an external capacitor to about 3V.

Initially, the soft-start function clamps the output of error amplifier by injecting a current (40uA) into the Fb pin and generates a voltage about 0.96V (40ux24K) across the negative input of error amplifier (see figure 5).

The magnitude of the injected current is inversely proportional to the voltage at the soft-start pin. As the soft-start voltage ramps up, the injected current decreases linearly and so does the voltage at negative input of error amplifier.

When the soft-start capacitor is around 1V, the voltage at the positive input of the error amplifier is approximately 0.6V.

The output of error amplifier will start increasing and generating the first PWM signal. As the soft-start capacitor voltage continues to rise up, the current flowing into the Fb pin will keep decreasing.

The feedback voltage increases linearly as the soft start voltage ramps up. When soft-start voltage is around 2V, the output voltage reaches the steady state and the injected current is zero.

Figure 6 shows the theoretical operating waveforms during soft-start.

The output voltage start-up time is the time period when soft-start capacitor voltage increases from 1V to 2V.

The start-up time will be dependent on the size of the external soft-start capacitor and can be estimated by:

$$20\mu A * \frac{T_{start}}{C_{ss}} = 2V - 1V$$

For a given start-up time, the soft-start capacitor can be estimated as:

$$C_{SS} \cong 20\mu A * T_{start}(ms) \qquad --(1)$$

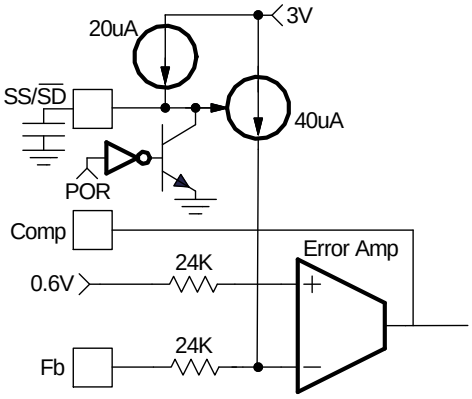


Fig. 5: Soft-Start circuit for IR3820A

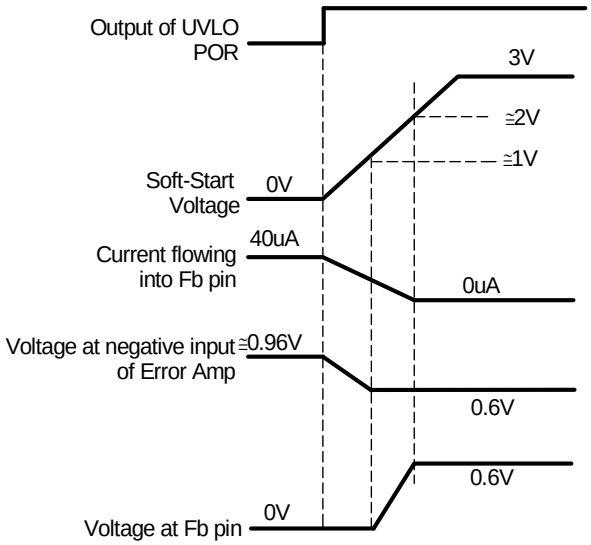


Fig. 6: Theoretical operation waveforms during soft-start

Over-Current Protection

The over-current protection is performed by sensing current through the $R_{DS(on)}$ of the low side MOSFET. This method enhances the converter's efficiency and reduces cost by eliminating a current sense resistor. As shown in figure 7, an external resistor (R_{SET}) is connected between OCSet pin and the inductor point which sets the current limit set point.

The internal current source develops a voltage across R_{SET}. When the low side MOSFET is turned on, the inductor current flows through the Q2 and results a voltage which is given by:

$$V_{OCSet} = (I_{OCSet} * R_{OCSet}) - (R_{DS(on)} * I_L) \quad --(2)$$

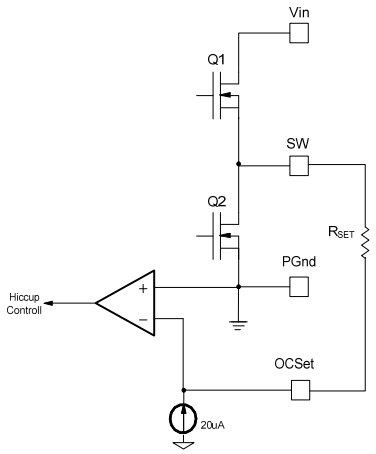


Fig. 7: Connection of over current sensing resistor

The critical inductor current can be calculated by setting:

$$V_{OCSet} = (I_{OCSet} * R_{OCSet}) - (R_{DS(on)} * I_L) = 0$$

$$I_{SET} = I_{L(critical)} = \frac{R_{OCSet} * I_{OCSet}}{R_{DS(on)}} \quad --(3)$$

An over-current is detected if the OCSet pin goes below ground. This trips the OCP comparator and cycles the soft start function in hiccup mode.

The hiccup is performed by charging and discharging the soft-start capacitor in a certain slope rate. As shown in figure 8 a 3uA current source is used to discharge the soft-start capacitor.

The OCP comparator resets after every soft start cycle. The converter stays in this mode until the overload or short circuit is removed. The converter will automatically recover.

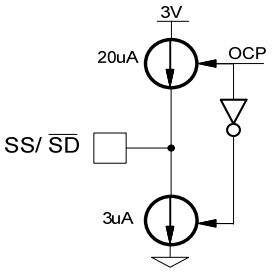


Fig. 8: 3uA current source for discharging soft-start capacitor during hiccup

The OCP circuit starts sampling current when the low gate drive is about 3V. The OCSet pin is internally clamped about 1.5V during on time of high side gate to prevent false trigging, figure 9 shows the OCSet pin during one switching cycle. As shown, there is about 150ns delay to mask the dead time. Since this node contains switching noises, this delay also functions as a filter.

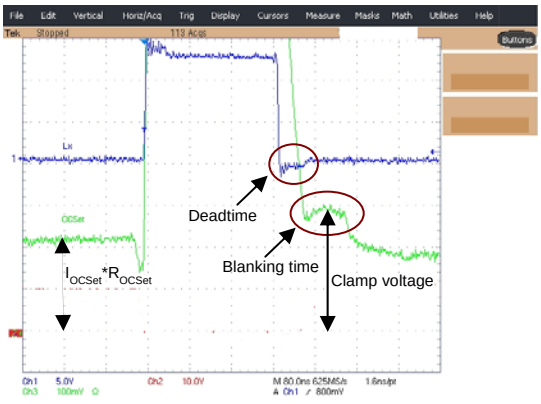


Fig. 9: OCset pin during normal condition
Ch1: Inductor point, Ch3:OCSet

The value of R_{SET} should be checked in an actual circuit to ensure that the over-current protection circuit activates as expected. The IR3820A current limit is designed primarily as disaster preventing, and doesn't operate as a precision current regulator.

Application Information

Design Example:

The following example is a typical application for the IR3820A. The application circuit is shown in page 17.

$V_{in} = 12V, (13.2V, max)$

$V_o = 1.8V$

$I_o = 14\,A$

$\Delta V_o \leq 30\,mV$

$F_s = 300\,kHz$

Output Voltage Programming

Output voltage is programmed by reference voltage and external voltage divider. The Fb pin is the inverting input of the error amplifier, which is internally referenced to 0.6V. The divider is ratioed to provide 0.6V at the Fb pin when the output is at its desired value. The output voltage is defined by using the following equation:

$$V_o = V_{ref} * \left(1 + \frac{R_8}{R_9}\right) \quad --(4)$$

When an external resistor divider is connected to the output as shown in figure 10.

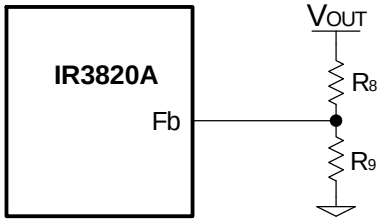


Fig. 10: Typical application of the IR3820A for programming the output voltage

Equation (4) can be rewritten as:

$$R_9 = R_8 * \left(\frac{V_{ref}}{V_O - V_{ref}}\right) \quad --(5)$$

For the calculated values of R_8 and R_9 see feedback compensation section.

Soft-Start Programming

The soft-start timing can be programmed by selecting the soft-start capacitance value. The start-up time of the converter can be calculated by using:

$$C_{SS} \cong 20\mu A * T_{start} \quad --(1)$$

Where T_{start} is the desired start-up time (ms)
For a start-up time of 11ms, the soft-start capacitor will be 0.22uF.

Vc supply for single input voltage

To drive the high-side switch, it is necessary to supply a gate voltage at least 4V greater than the bus voltage. This is achieved by using a charge pump configuration as shown in figure 11. This method is simple and inexpensive. The operation of the circuit is as follows: when the lower MOSFET is turned on, the capacitor (C1) is pulled down to ground and charges, up to V_{BUS} value, through the diode (D1). The bus voltage will be added to this voltage when upper MOSFET turns on in next cycle, and providing supply voltage (Vc) through diode (D2). Vc is approximately:

$$V_C \cong 2 * V_{bus} - (V_{D1} + V_{D2}) \quad --(6)$$

Capacitors in the range of 0.1uF are generally adequate for most applications. The diodes must be a fast recovery device to minimize the amount of charge fed back from the charge pump capacitor into V_{BUS}. The diodes need to be able to block the full power rail voltage, which is seen when the high-side MOSFET is switched on. For low-voltage application, schottky diodes can be used to minimize forward drop across the diodes at start up.

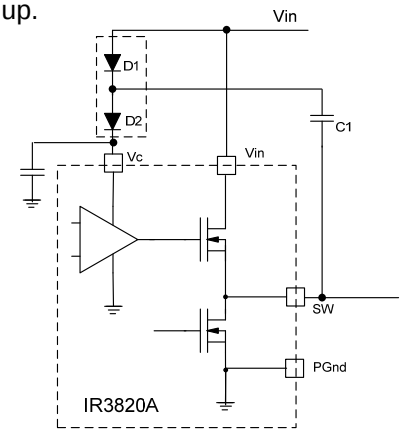


Fig. 11: Charge pump circuit to generate Vc voltage

Input Capacitor Selection

The input filter capacitor should be selected based on how much ripple the supply can tolerate on the DC input line. The ripple current generated during the on time of upper MOSFET should be provided by the input capacitor. The RMS value of this ripple is expressed by:

$$I_{RMS} = I_o * \sqrt{D*(1-D)} \quad \text{--(7)}$$

Where: $D = \frac{V_o}{V_{in}}$

D is the Duty Cycle

I_{RMS} is the RMS value of the input capacitor current.

Io is the output current.

For Io=14A and D=0.15, the I_{RMS}=5A.

Ceramic capacitors are recommended due to their peak current capabilities. They also feature low ESR and ESL at higher frequency which enables better efficiency.

Use 3x10uF, 16V ceramic capacitors.

Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. A low inductor value causes a large ripple current, resulting in the smaller size, faster response to a load transient but poor efficiency and high output noise. Generally, the selection of the inductor value can be reduced to the desired maximum ripple current in the inductor (Δi). The optimum point is usually found between 20% and 50% ripple of the output current.

For the buck converter, the inductor value for the desired operating ripple current can be determined using the following:

$$V_{in} - V_o = L * \frac{\Delta i}{\Delta t}; \quad \Delta t = D * \frac{1}{F_s}$$

$$L = (V_{in} - V_o) * \frac{V_o}{V_{in} * \Delta i * F_s} \quad \text{--(8)}$$

Where:

V_{in} = *Maximum input voltage*

V_o = *Output Voltage*

Δi = *Inductor ripple current*

F_s = *Switching frequency*

Δt = *Turn on time*

D = *Duty cycle*

If $\Delta i \approx 40\%(I_o)$, then the output inductor will be:

L = 1.0uH

Delta MPL-104 series provides a range of inductors in different values and low profile suitable for large currents.

Output Capacitor Selection

The voltage ripple and transient requirements determine the output capacitors' type and values. The criteria is normally based on the value of the Effective Series Resistance (ESR). However the actual capacitance value and the Equivalent Series Inductance (ESL) are other contributing components. These components can be described as:

$$\Delta V_o = \Delta V_{o(ESR)} + \Delta V_{o(ESL)} + \Delta V_{o(C)}$$

$$\Delta V_{o(ESR)} = \Delta I_L * ESR \quad \text{--(9)}$$

$$\Delta V_{o(ESL)} = \left(\frac{V_{in}}{L}\right) * ESL$$

$$\Delta V_{o(C)} = \frac{\Delta I_L}{8 * C_o * F_s}$$

ΔV_o = *Output voltage ripple*

ΔI_L = *Inductor ripple current*

Since the output capacitor has a major role in the overall performance of the converter and determine the result of transient response, selection of the capacitor is critical. The IR3820A can perform well with all types of capacitors.

As a rule the capacitor must have low enough ESR to meet output ripple and load transient requirements, yet have high enough ESR to satisfy stability requirements.

The goal for this design is to meet the voltage ripple requirement in the smallest possible capacitor size. Therefore, a ceramic capacitor is selected due to its low ESR and small size. Six of the Panasonic ECJ2FB0J226M (22uF, 6.3V, X5R and EIA 0805 case size) are a good choice.

In the case of tantalum or low ESR electrolytic capacitors, the ESR dominates the output voltage ripple, equation (9) can be used to calculate the required ESR for the specific voltage ripple.

Feedback Compensation

The IR3820A is a voltage mode controller; the control loop is a single voltage feedback path including error amplifier and error comparator. To achieve fast transient response and accurate output regulation, a compensation circuit is necessary. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency and adequate phase margin (greater than 45º).

The output LC filter introduces a double pole, –40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180º (see figure 13). The resonant frequency of the LC filter expressed as follows:

$$F_{LC} = \frac{1}{2\ \pi\sqrt{L_o\ C_o}} \quad ---(11)$$

Figure 13 shows gain and phase of the LC filter. Since we already have 180º phase shift from the output filter alone, the system risks being unstable.

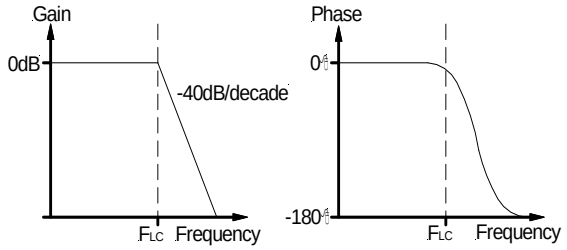


Fig. 13: Gain and Phase of LC filter

The IR3820A's error amplifier is a differential-input transconductance amplifier. The output is available for DC gain control or AC phase compensation.

The error amplifier can be compensated either in type II or type III compensation. When it is used in type II compensation the transconductance properties of the error amplifier become evident and can be used to cancel one of the output filter poles. This will be accomplished with a series RC circuit from Comp pin to ground as shown in figure 14.

This method requires that the output capacitor should have enough ESR to satisfy stability requirements. In general the output capacitor's ESR generates a zero typically at 5kHz to 50kHz which is essential for an acceptable phase margin.

The ESR zero of the output capacitor expressed as follows:

$$F_{ESR} = \frac{1}{2*\pi*ESR*C_o} \quad ---(12)$$

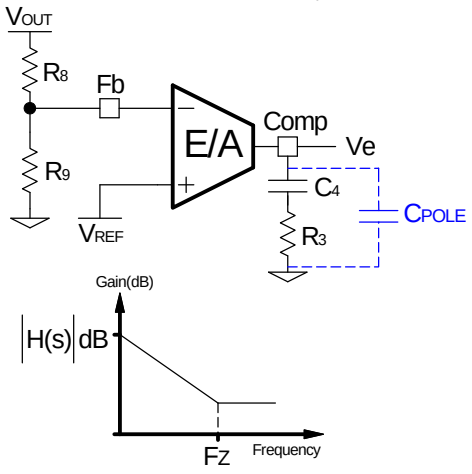


Fig. 14: TypeII compensation network and its asymptotic gain plot

The transfer function (Ve/Vo) is given by:

$$H(s) = g_m * \frac{R_9}{R_9 + R_8} * \frac{1 + sR_3C_4}{sC_4} \quad ---(13)$$

The (s) indicates that the transfer function varies as a function of frequency. This configuration introduces a gain and zero, expressed by:

$$[H(s)] = \left(g_m * \frac{R_9}{R_9 + R_8}\right) * R_3 \quad ---(14)$$

$$F_z = \frac{1}{2\pi * R_3 * C_4} \quad ---(15)$$

The gain is determined by the voltage divider and error amplifier's transconductance gain.
First select the desired zero-crossover frequency (Fo):

$$F_o > F_{ESR}\ and\ F_o \le (1/5 \sim 1/10) * F_s$$

Use the following equation to calculate R3:

$$R_3 = \frac{V_{osc} * F_o * F_{ESR} * (R_8 + R_9)}{V_{in} * F_{LC}^2 * R_9 * g_m} \quad ---(16)$$

Where:
V_{in} = Maximum Input Voltage
V_{osc} = Oscillator Ramp Voltage
F_o = Crossover Frequency
F_{ESR} = Zero Frequency of the Output Capacitor
F_{LC} = Resonant Frequency of the Output Filter
R_8 and R_9 = Feedback Resistor Dividers
g_m = Error Amplifier Transconductance

To cancel one of the LC filter poles, place the zero before the LC filter resonant frequency pole:

$$F_z = 75\% F_{LC}$$

$$F_z = 0.75 * \frac{1}{2\pi\sqrt{L_o * C_o}} \quad ---(17)$$

Use equations (15) and (16) to calculate C4.
One more capacitor is sometimes added in parallel with C4 and R3. This introduces one more pole which is mainly used to suppress the switching noise.
The additional pole is given by:

$$F_P = \frac{1}{2\pi * R_3 * \frac{C_4 * C_{POLE}}{C_4 + C_{POLE}}}$$

The pole sets to one half of switching frequency which results in the capacitor C_{POLE}:

$$C_{POLE} = \frac{1}{\pi * R_3 * F_s - \frac{1}{C_4}} \cong \frac{1}{\pi * R_3 * F_s}$$

$$For\ F_P << \frac{F_s}{2}$$

For a general solution for unconditional stability for any type of output capacitors, in a wide range of ESR values we should implement local feedback with a compensation network (type III). The typically used compensation network for voltage-mode controller is shown in figure 15.

In such a configuration, the transfer function is given by:

$$\frac{V_e}{V_o} = \frac{1 - g_m Z_f}{1 + g_m Z_{IN}}$$

The error amplifier gain is independent of the transconductance under the following condition:

$$g_m * Z_f >> 1 \ and \ \ g_m * Z_{in} >> 1 \quad ---(18)$$

By replacing Z_{in} and Z_f according to figure 15, the transformer function can be expressed as:

$$H(s) = \frac{1}{sR_8(C_4 + C_3)} * \frac{(1 + sR_3C_4) * [1 + sC_7(R_8 + R_{10})]}{\left[1 + sR_3\left(\frac{C_4 * C_3}{C_4 + C_3}\right)\right] * (1 + sR_{10}C_7)}$$

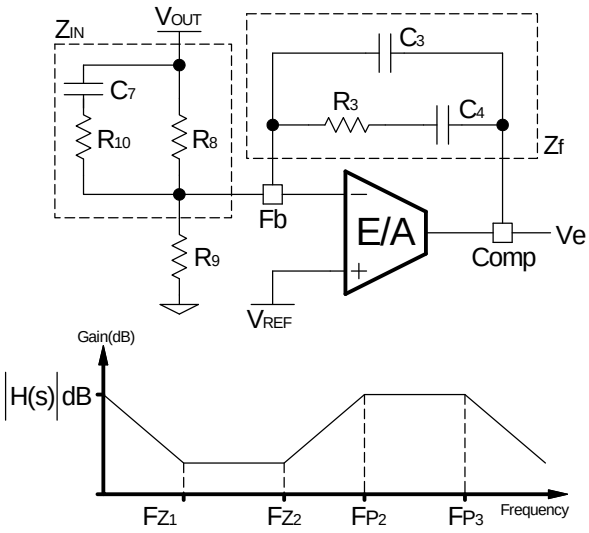


Fig.15: Compensation network with local feedback and its asymptotic gain plot

As known, the transconductance amplifier has high impedance (current source) output, therefore, consideration should be taken when loading the error amplifier output. It may exceed its source/sink output current capability, so that the amplifier will not be able to swing its output voltage over the necessary range.

The compensation network has three poles and two zeros and they are expressed as follows:

$$F_{P1} = 0$$

$$F_{P2} = \frac{1}{2\pi * R_{10} * C_7}$$

$$F_{P3} = \frac{1}{2\pi * R_3\left(\frac{C_4 * C_3}{C_4 + C_3}\right)} \cong \frac{1}{2\pi * R_3 * C_3}$$

$$F_{z1} = \frac{1}{2\pi * R_3 * C_4}$$

$$F_{z2} = \frac{1}{2\pi * C_7 * (R_8 + R_{10})} \cong \frac{1}{2\pi * C_7 * R_8}$$

Cross over frequency is expressed as:

$$F_o = R_3 * C_7 * \frac{V_{in}}{V_{osc}} * \frac{1}{2\pi * L_o * C_o}$$

Based on the frequency of the zero generated by the output capacitor and its ESR versus crossover frequency, the compensation type can be different. The table below shows the compensation types and location of crossover frequency.

Compensator type	F_{ESR} vs. F_o	Output capacitor
Type II(PI)	$F_{LC}<F_{ESR}<F_o<F_{s/2}$	Electrolytic , Tantalum
Type III (PID) **Method A**	$F_{LC}<F_o<F_{ESR}<F_{s/2}$	Tantalum, ceramic
Type III(PID) **Method B**	$F_{LC}<F_o<F_{s/2}<F_{ESR}$	Ceramic

Table1- The compensation type and location of F_{ESR} versus F_o

The details of these compensation types are discussed in application note AN-1043 which can be downloaded from IR's website at www.irf.com.

For this design we have:

V_{in}=12V
V_o=1.8V
V_{osc}=1.25V
V_{ref}=0.6V
g_m=1000umoh
L_o=1.0uH
C_o=6x22uF, ESR=0.5mOhm
F_s=300kHz

The value of the capacitance used in the compensator design must be the small signal value. For instance, the small signal capacitance of the 22uF capacitor used in this design is 12uF at 1.8 VDC bias and 600 kHz frequency. It is this value that must be used for all computations related to the compensation. The small signal value may be obtained from the manufacturer's datasheets, design tools or SPICE models. Alternatively, they may also be inferred from measuring the power stage transfer function of the converter and measuring the double pole frequency *FLC* and using equation (11) to compute the small signal *Co.*

These result to:

F_{LC}=18.76kHz
F_{ESR}=4.4MHz
$F_{s/2}$=300kHz

Select crossover frequency:

$$F_o < F_{ESR} \text{ and } F_o \le (1/5 \sim 1/10) * F_s$$

Fo=60kHz

Since: *FLC<Fo<Fs/2<FESR*, type III method B is selected to place the poles and zeros.

The following design rules will give a crossover frequency approximately one-tenth of the switching frequency. The higher the band width, the potentially faster the load transient response.

The DC gain will be large enough to provide high DC-regulation accuracy (typically -5dB to -12dB). The phase margin should be greater than 45° for overall stability.

Desired Phase Boost: $\Theta_{max} = 70^\circ$

$$F_{Z2} = F_o * \sqrt{\frac{1-Sin\Theta}{1+Sin\Theta}}$$

$$F_{Z2} = 10.58kHz$$

$$F_{P2} = F_o * \sqrt{\frac{1+Sin\Theta}{1-Sin\Theta}}$$

$$F_{P2} = 340.28kHz$$

$$Select:\ F_{Z1} = 0.5 * F_{Z2} \ \ and \ \ F_{P3} = 0.5 * F_s$$

$$Select: C_7 = 180pF$$

$$R_3 = \frac{2\pi * F_o * L_o * C_o * V_{OSC}}{C_7 * V_{in}},\ R_3 = 15.71K\Omega,\ check R_3 \ge \frac{2}{g_m}$$

$$Select: R_3 = 15.80K\Omega$$

$$Calculate\ C_4\ and\ C_3:$$

$$C_4 = \frac{1}{2\pi * F_{Z1} * R_3};\ C_4 = 1.9nF, Select:\ C_4 = 2.2nF$$

$$C_3 = \frac{1}{2\pi * F_{P3} * R_3};\ C_3 = 67.15pF, Select: C_3 = 39pF$$

$$Calculate\ R_{10}, R_8\ and\ R_9:$$

$$R_{10} = \frac{1}{2\pi * C_7 * F_{P2}};\ R_{10} = 2.60K\Omega,\ check R_{10} \ge \frac{1}{g_m}$$

$$Select: R_{10} = 2.61K\Omega$$

$$R_8 = \frac{1}{2\pi * C_7 * F_{Z2}} - R_{10};\ R_8 = 80.97K\Omega, Select: R_8 = 80.6K\Omega$$

$$R_9 = \frac{V_{ref}}{V_o - V_{ref}} * R_8;\ R_9 = 40.30K\Omega, Select: R_9 = 40.2K\Omega$$

Programming the Current-Limit

The Current-Limit threshold can be set by connecting a resistor (R_{SET}) from drain of the low-side MOSFET to the OCSet pin. The resistor can be calculated by using equation (3).

The $R_{DS(on)}$ has a positive temperature coefficient and it should be considered for the worse case operation. This resistor must be placed close to the IC, place a small ceramic capacitor from this pin to power ground (PGnd) for noise rejection purposes.

$$I_{SET} = I_{L(critical)} = \frac{R_{OCSet} * I_{OCSet}}{R_{DS(on)}} \quad --(3)$$

$$R_{DS(on)} = 6.9m\Omega * \upsilon = 6.9m\Omega * 1.5 = 10.35m\Omega$$

where :

υ *: Temperature Dependency*

Note : Use 9.3 mΩ for low - side MOSFET if 5V is used for V_{cc}

$$I_{SET} = (I_o * 1.5) + \frac{\Delta i}{2}$$

where :

I_o *: Max Output Current*

Δi *: Inductor ripple current*

$$\Delta i = (V_{in} - V_o) * \frac{V_o}{V_{in} * L * F_s}$$

$$I_{SET} = (14A * 1.5) + 2.55A = 23.55A$$

$$R_{OCSet} = R_7 = 12.1K\Omega$$

Setting the Power Good Threshold

Power Good threshold can be programmed by using two external resistors (see figure 16).

The following formula can be used to set the threshold:

$$R_2 = \frac{0.38V}{0.9 * V_{out} - 0.38V} * R_1 \quad --(19)$$

Where:

0.38V is reference of the internal comparator

0.9*Vout is selectable threshold for power good, for this design it is 1.62V.

Select R_1=10KOhm

Using (18): R_2=3.06KOhm

Select R_2=3.09K

Use a pull up resistor (4.99K) from PGood pin to Vcc.

Layout Consideration

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Start to place the power components, making all the connection in the top layer with wide, copper filled areas.

The inductor, output capacitor and the IR3820A should be as close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place the input capacitor directly to the Vin pin of IR3820A. To reduce the ESR replace the single input capacitor with two parallel units.

The feedback part of the system should be kept away from the inductor and other noise sources.

The critical bypass components such as capacitors for Vcc and Vc should be close to their respective pins. It is important to place the feedback components including feedback resistors and compensation components close to Fb and Comp pins.

In a multilayer PCB use one layer as a power ground plane and have a control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point.

The Power QFN is a thermally enhanced package. Based on thermal performance it is recommended to use at least a 4-layers PCB. To effectively remove heat from the device the exposed pad should be connected to the ground plane using vias.

Typical Application for IR3820A
12V to 1.8V @ 14A

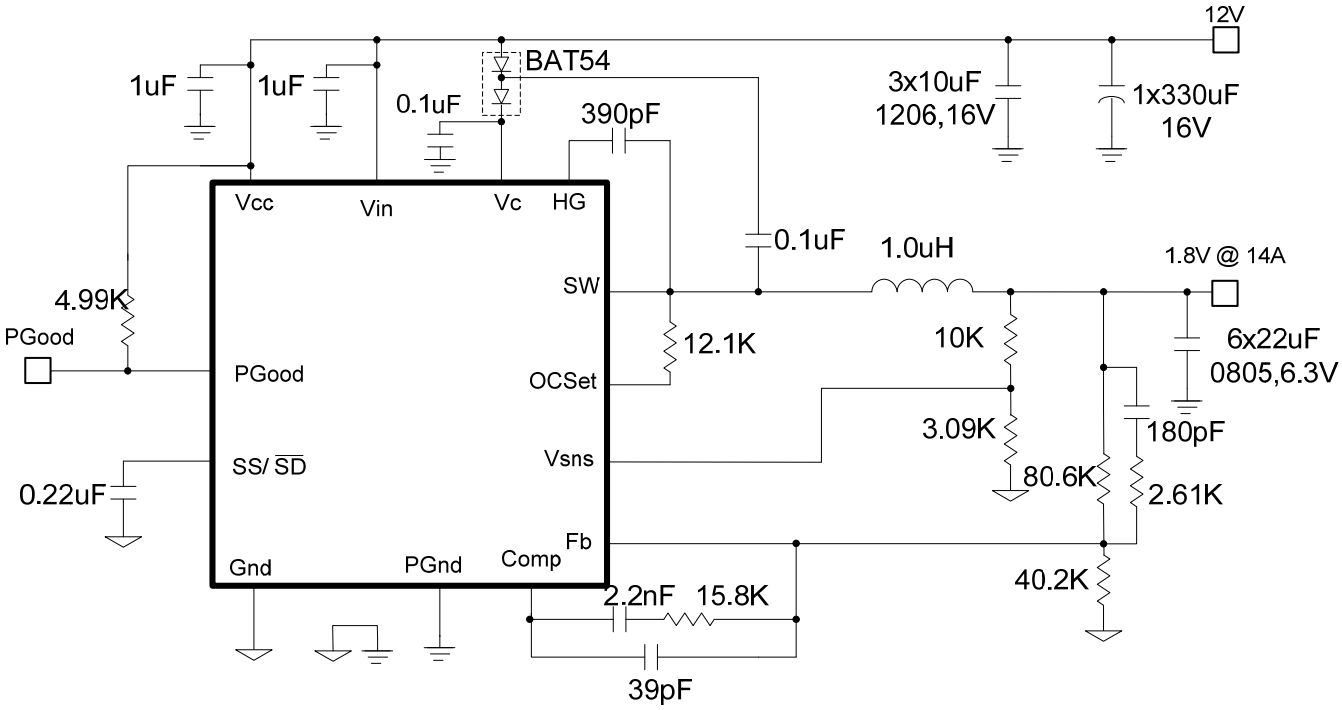


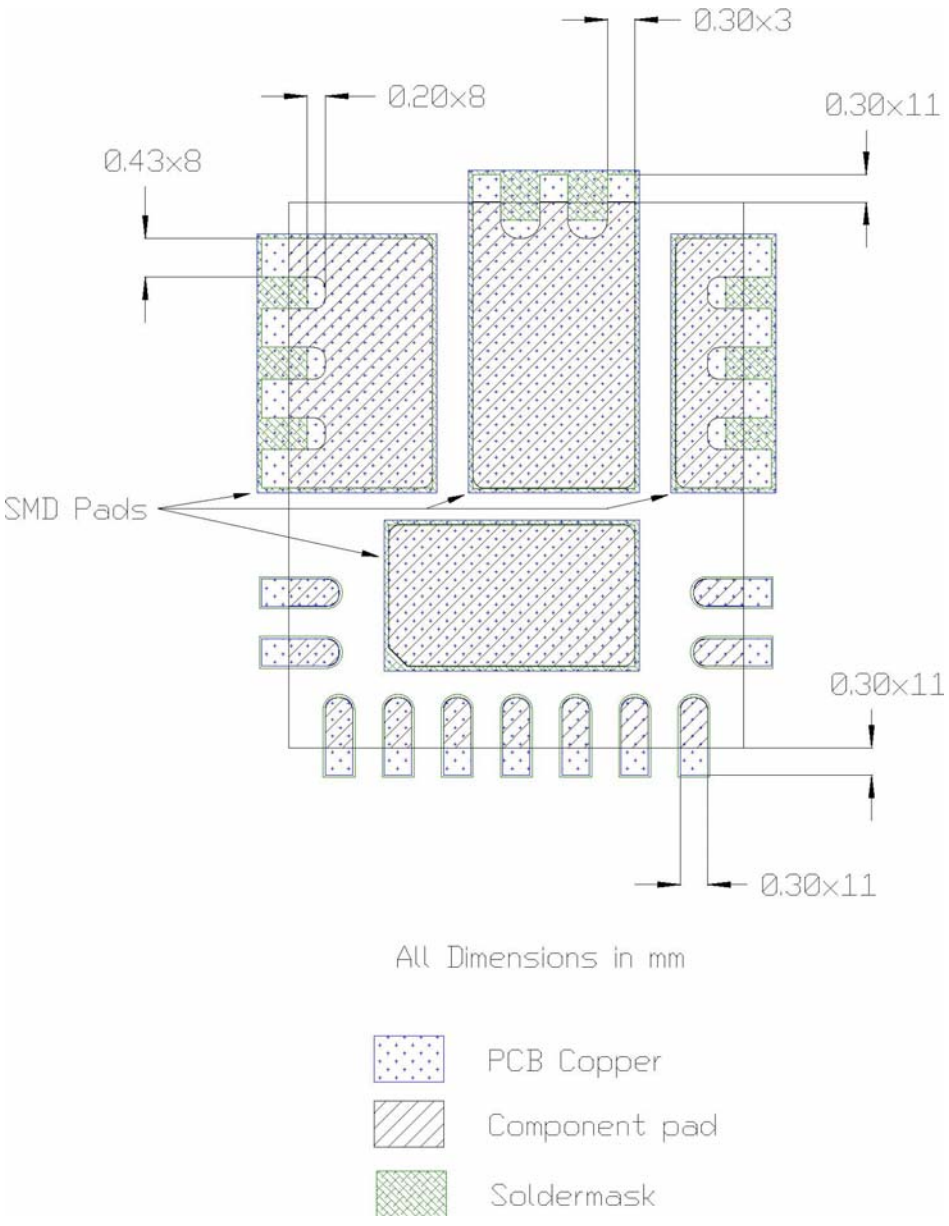
Fig.16: Typical Application circuit for 12V to 1.8V at 14A using ceramic output capacitors

PCB Metal and Components Placement

The lead lands (the 11 IC pins) width should be equal to the nominal part lead width. The minimum lead-to-lead spacing should be ≥ 0.2mm to minimize shorting.

Lead land length should be equal to the maximum part lead length + 0.3 mm outboard extension. The outboard extension ensures a large and inspectable toe fillet.

The pad lands (the 4 big pads other than the 11 IC pins) length and width should be equal to maximum part pad length and width. However, the minimum metal-to-metal spacing should be no less than 0.17mm for 2 oz. Copper; no less than 0.1mm for 1 oz. Copper and no less than 0.23mm for 3 oz. Copper.

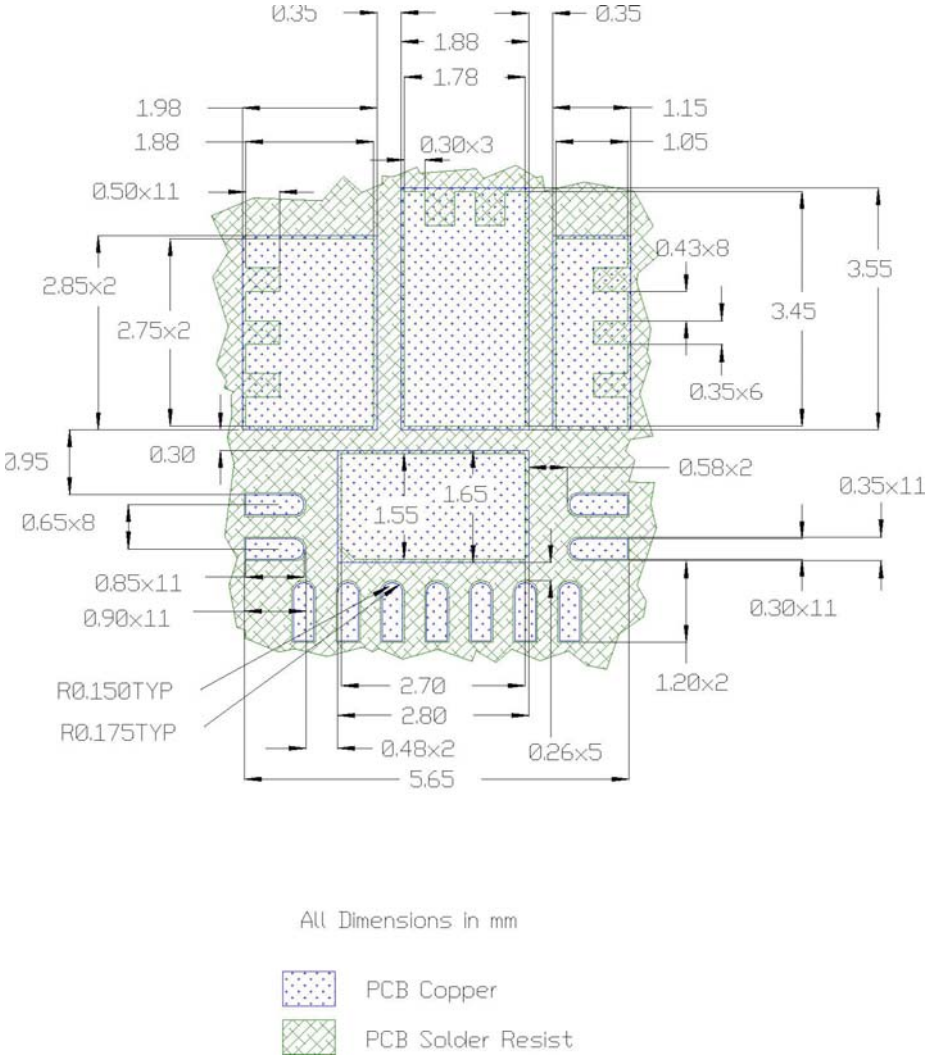


Solder Resist

It is recommended that the lead lands are Non Solder Mask Defined (NSMD). The solder resist should be pulled away from the metal lead lands by a minimum of 0.025mm to ensure NSMD pads.

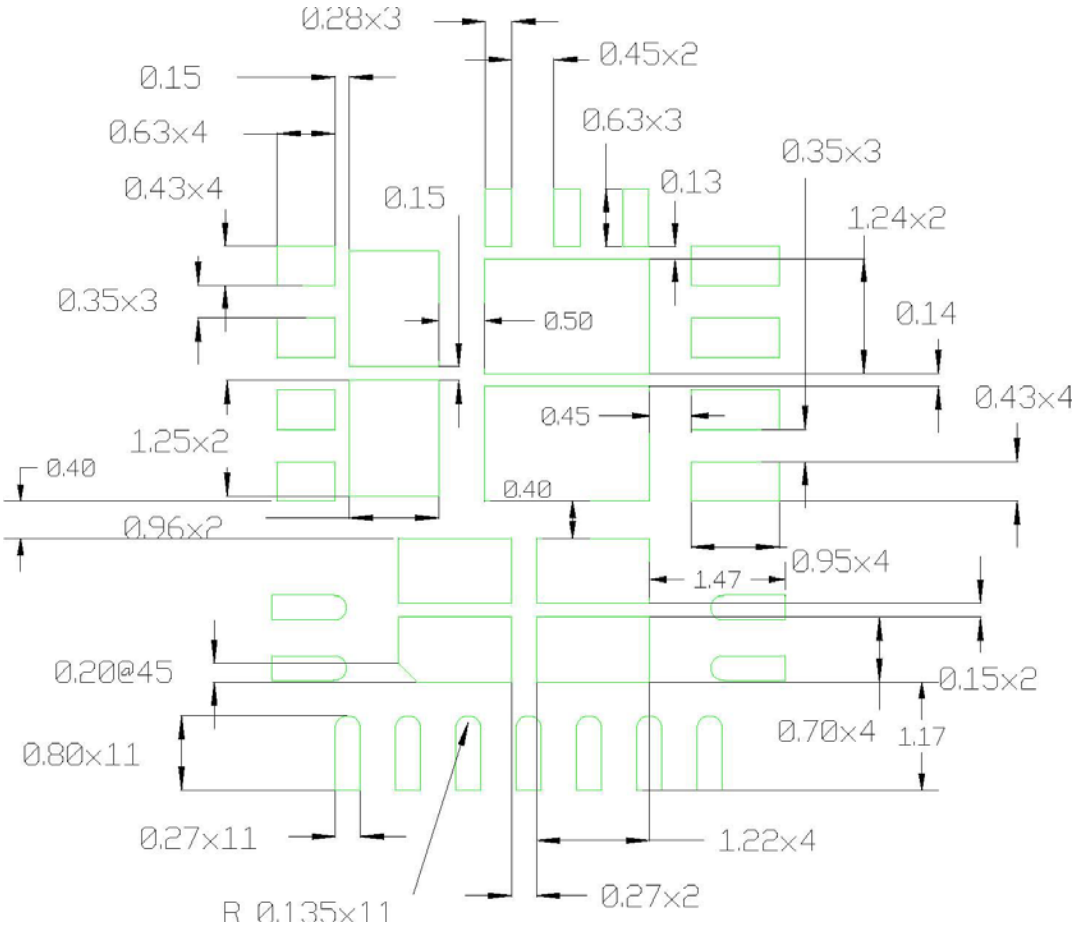
The land pad should be Solder Mask Defined (SMD), with a minimum overlap of the solder resist onto the copper of 0.05mm to accommodate solder resist mis-alignment.

Ensure that the solder resist in between the lead lands and the pad land is ≥ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.

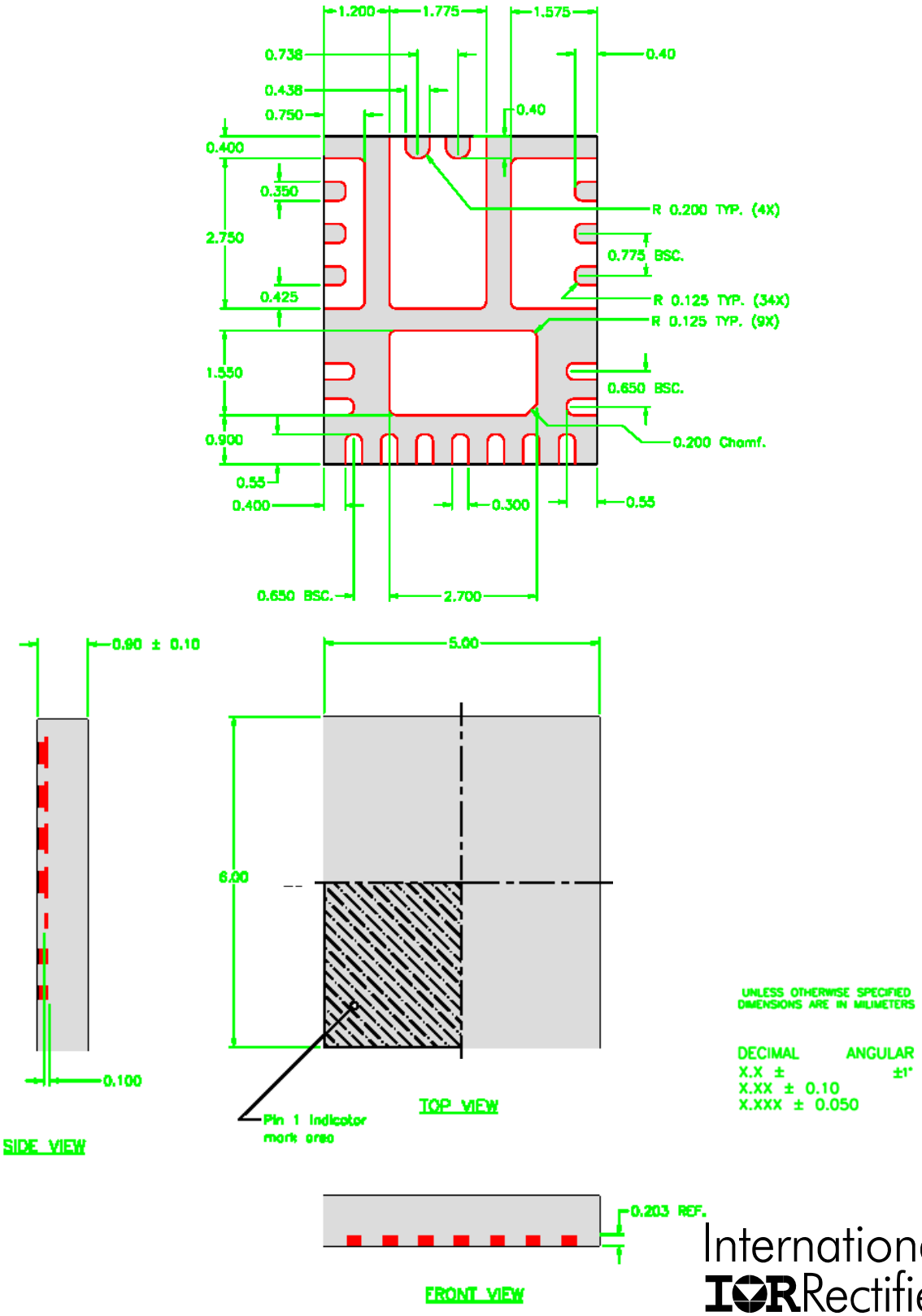


Stencil Design

- The Stencil apertures for the lead lands should be approximately 80% of the area of the lead lads. Reducing the amount of solder deposited will minimize the occurrences of lead shorts. If too much solder is deposited on the center pad the part will float and the lead lands will be open.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.



Stencil Aperture
All Dimensions in mm



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