



**THE DATASHEET OF  
IRFS7434TRLPBF**



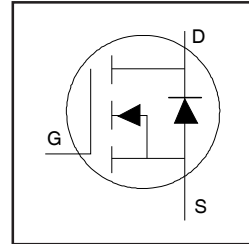
## Applications

- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters

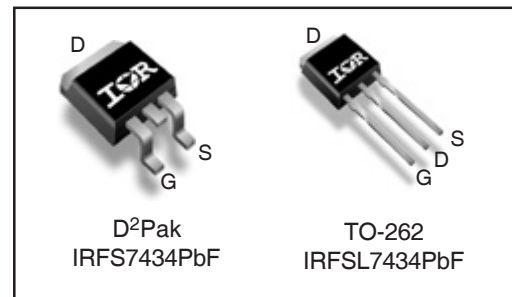
## Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free

## HEXFET® Power MOSFET



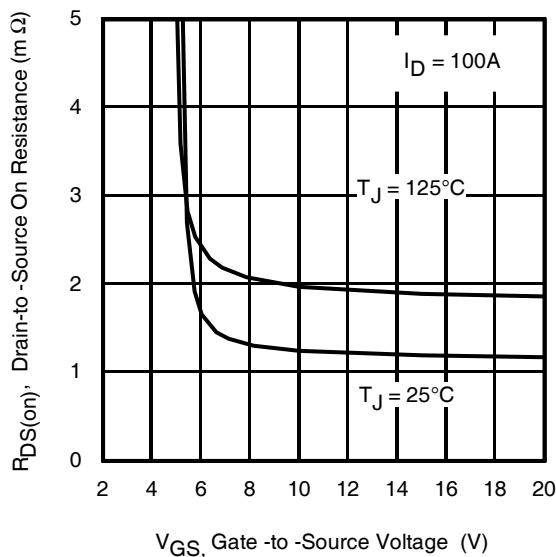
$V_{DSS}$		<b>40V</b>
$R_{DS(on)}$	typ.	<b>1.25mΩ</b>
	max.	<b>1.6mΩ</b>
$I_D$ (Silicon Limited)		<b>320A</b> ①
$I_D$ (Package Limited)		<b>195A</b>



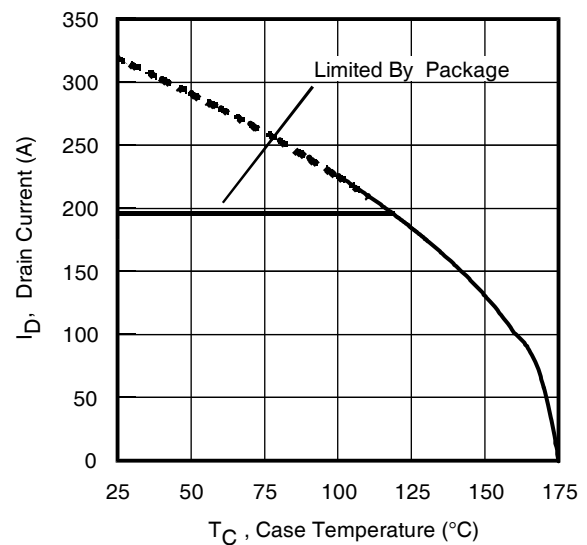
<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

## Ordering Information

Base part number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IRFSL7434PbF	TO-262	Tube	50	IRFSL7434PbF
IRFS7434PbF	D2Pak	Tube	50	IRFS7434PbF
		Tape and Reel Left	800	IRFS7434TRLpBf



**Fig 1.** Typical On-Resistance vs. Gate Voltage



**Fig 2.** Maximum Drain Current vs. Case Temperature

**Absolute Maximum Ratings**

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	320 <sup>①</sup>	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	226 <sup>①</sup>	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Wire Bond Limited)	195	
$I_{DM}$	Pulsed Drain Current <sup>②</sup>	1270 *	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	294	W
	Linear Derating Factor	1.96	W/ $^\circ\text{C}$
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
dv/dt	Peak Diode Recovery <sup>④</sup>	5.0	V/ns
$T_J$	Operating Junction and	-55 to + 175	$^\circ\text{C}$
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)		

**Avalanche Characteristics**

$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy <sup>③</sup>	490	mJ
$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy <sup>④</sup>	1098	
$I_{AR}$	Avalanche Current <sup>②</sup>	See Fig. 14, 15 , 22a, 22b	A
$E_{AR}$	Repetitive Avalanche Energy <sup>②</sup>		mJ

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case <sup>⑧</sup>	—	0.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) , D <sup>2</sup> Pak <sup>⑩</sup>	—	40	

**Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0\text{V}$ , $I_D = 250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	32	—	mV/ $^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D = 5\text{mA}$ <sup>②</sup>
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	1.25	1.6	m $\Omega$	$V_{GS} = 10\text{V}$ , $I_D = 100\text{A}$ <sup>⑤</sup>
			1.8	—	m $\Omega$	$V_{GS} = 6.0\text{V}$ , $I_D = 50\text{A}$ <sup>⑤</sup>
$V_{GS(th)}$	Gate Threshold Voltage	2.2	3.0	3.9	V	$V_{DS} = V_{GS}$ , $I_D = 250\mu\text{A}$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	1.0	$\mu\text{A}$	$V_{DS} = 40\text{V}$ , $V_{GS} = 0\text{V}$
				150		$V_{DS} = 40\text{V}$ , $V_{GS} = 0\text{V}$ , $T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20\text{V}$
$R_G$	Internal Gate Resistance	—	2.1	—	$\Omega$	

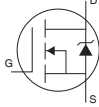
**Notes:**

- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 195A by source bonding technology . Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
  - ② Repetitive rating; pulse width limited by max. junction temperature.
  - ③ Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.099\text{mH}$   
 $R_G = 50\Omega$ ,  $I_{AS} = 100\text{A}$ ,  $V_{GS} = 10\text{V}$ .
  - ④  $I_{SD} \leq 100\text{A}$ ,  $di/dt \leq 1307\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$ .
  - ⑤ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
  - ⑥  $C_{OSS}$  eff. (TR) is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
  - ⑦  $C_{OSS}$  eff. (ER) is a fixed capacitance that gives the same energy as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
  - ⑧  $R_\theta$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .
  - ⑨ Limited by  $T_{Jmax}$  starting  $T_J = 25^\circ\text{C}$ ,  $L = 1\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 47\text{A}$ ,  $V_{GS} = 10\text{V}$ .
  - ⑩ When mounted on 1" square PCB (FR-4 or G-10 Material).  
Please refer to AN-994 for more details:  
<http://www.irf.com/technical-info/appnotes/an-994.pdf>
- \* Pulse drain current is limited at 780A by source bonding technology.

**Dynamic @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$g_{fs}$	Forward Transconductance	211	—	—	S	$V_{DS} = 10\text{V}$ , $I_D = 100\text{A}$
$Q_g$	Total Gate Charge	—	216	324	nC	$I_D = 100\text{A}$ $V_{DS} = 20\text{V}$ $V_{GS} = 10\text{V}$ ⑤ $I_D = 100\text{A}$ , $V_{DS} = 0\text{V}$ , $V_{GS} = 10\text{V}$
$Q_{gs}$	Gate-to-Source Charge	—	51	—		
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	77	—		
$Q_{sync}$	Total Gate Charge Sync. ( $Q_g - Q_{gd}$ )	—	139	—		
$t_{d(on)}$	Turn-On Delay Time	—	24	—		
$t_r$	Rise Time	—	68	—	ns	$V_{DD} = 20\text{V}$ $I_D = 30\text{A}$ $R_G = 2.7\Omega$ $V_{GS} = 10\text{V}$ ⑤
$t_{d(off)}$	Turn-Off Delay Time	—	115	—		
$t_f$	Fall Time	—	68	—		
$C_{iss}$	Input Capacitance	—	10820	—	pF	$V_{GS} = 0\text{V}$ $V_{DS} = 25\text{V}$ $f = 1.0\text{ MHz}$ , See Fig. 5 $V_{GS} = 0\text{V}$ , $V_{DS} = 0\text{V}$ to $32\text{V}$ ⑦, See Fig. 12 $V_{GS} = 0\text{V}$ , $V_{DS} = 0\text{V}$ to $32\text{V}$ ⑥
$C_{oss}$	Output Capacitance	—	1540	—		
$C_{riss}$	Reverse Transfer Capacitance	—	1140	—		
$C_{oss}$ eff. (ER)	Effective Output Capacitance (Energy Related)	—	1880	—		
$C_{oss}$ eff. (TR)	Effective Output Capacitance (Time Related)	—	2208	—		

**Diode Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	320 ①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ②	—	—	1270*		
$V_{SD}$	Diode Forward Voltage	—	0.9	1.3	V	$T_J = 25^\circ\text{C}$ , $I_S = 100\text{A}$ , $V_{GS} = 0\text{V}$ ⑤
$dv/dt$	Peak Diode Recovery ④	—	5.0	—	V/ns	$T_J = 175^\circ\text{C}$ , $I_S = 100\text{A}$ , $V_{DS} = 40\text{V}$
$t_{rr}$	Reverse Recovery Time	—	38	—	ns	$T_J = 25^\circ\text{C}$ $V_R = 34\text{V}$ , $T_J = 125^\circ\text{C}$ $I_F = 100\text{A}$
$Q_{rr}$	Reverse Recovery Charge	—	50	—		
		—	50	—	nC	$T_J = 25^\circ\text{C}$ $di/dt = 100\text{A}/\mu\text{s}$ ⑤ $T_J = 125^\circ\text{C}$
$I_{RPM}$	Reverse Recovery Current	—	1.9	—	A	$T_J = 25^\circ\text{C}$

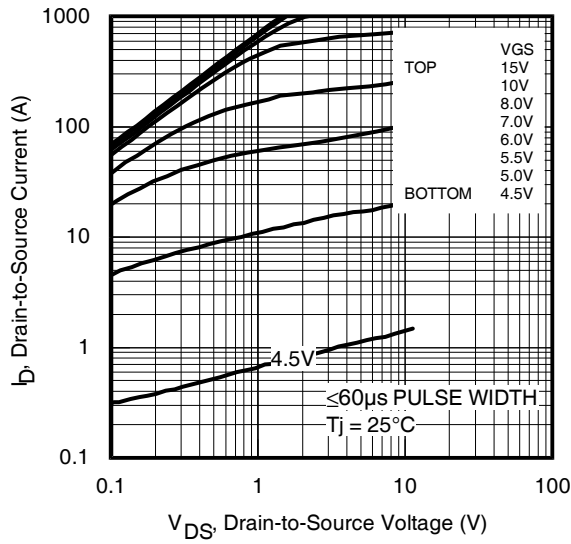


Fig 3. Typical Output Characteristics

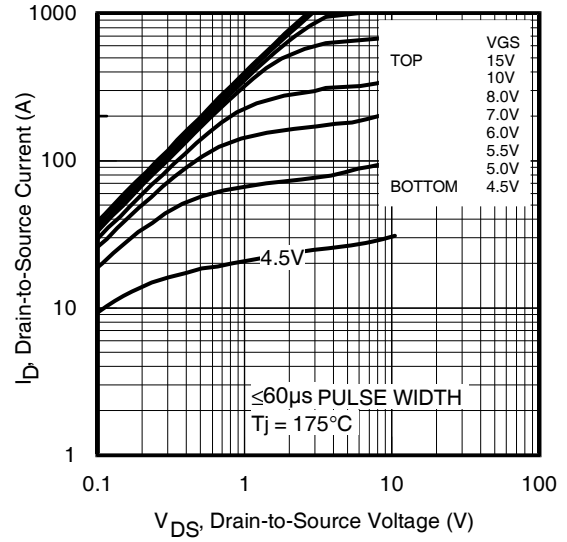


Fig 4. Typical Output Characteristics

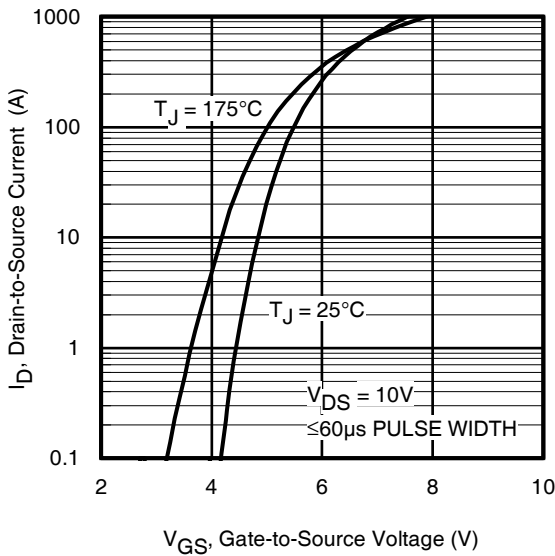


Fig 5. Typical Transfer Characteristics

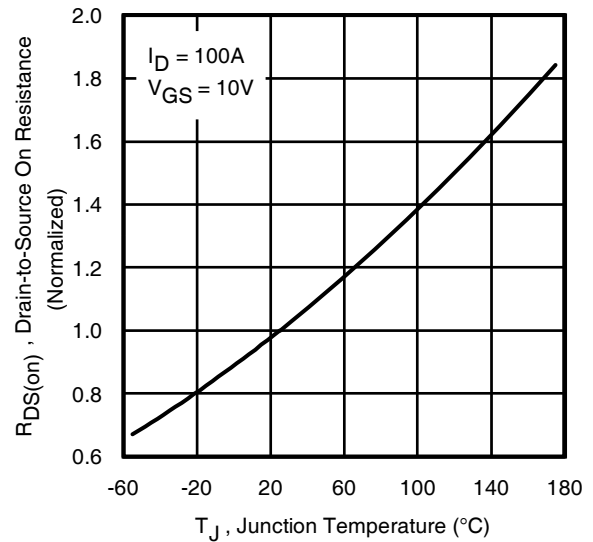


Fig 6. Normalized On-Resistance vs. Temperature

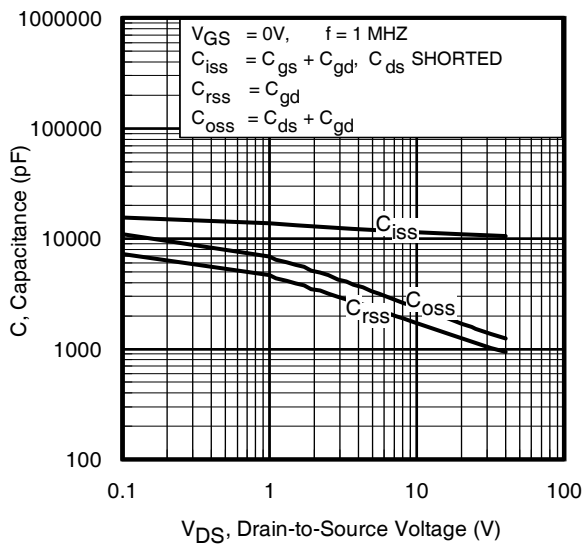


Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

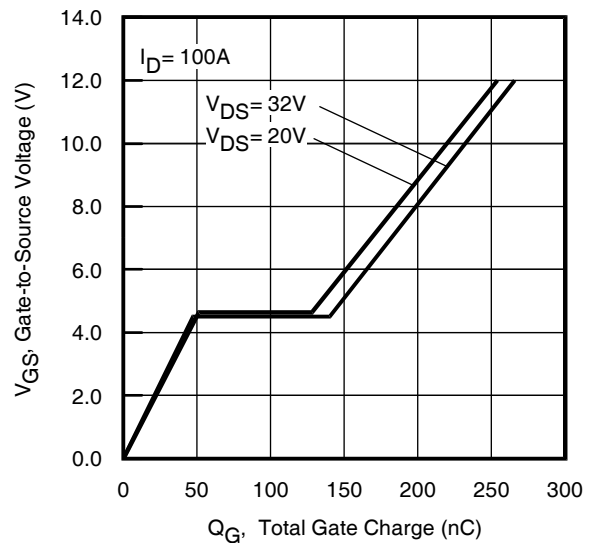


Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage

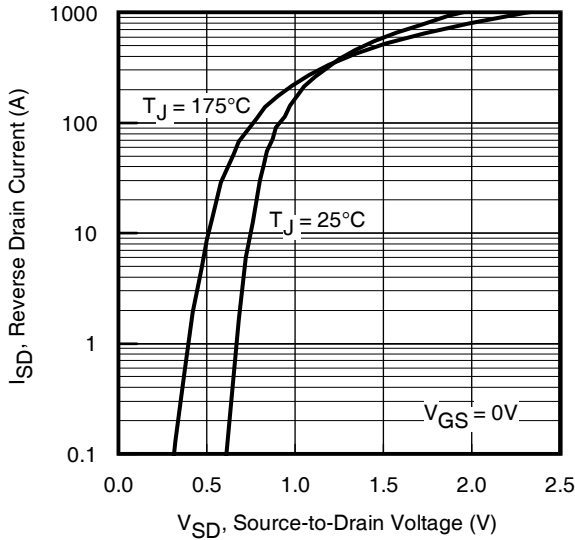


Fig 9. Typical Source-Drain Diode Forward Voltage

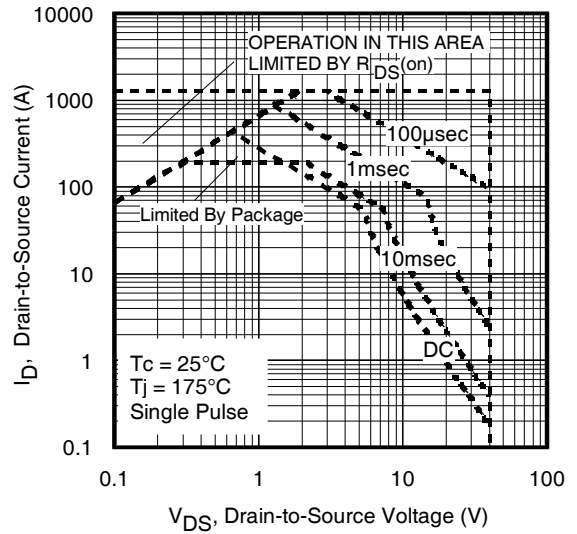


Fig 10. Maximum Safe Operating Area

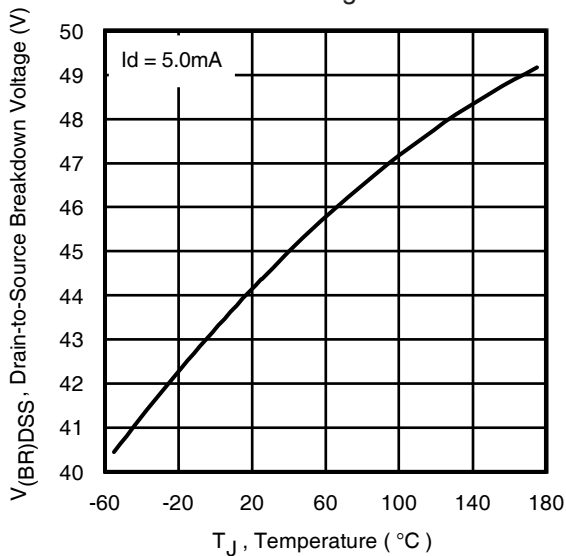


Fig 11. Drain-to-Source Breakdown Voltage

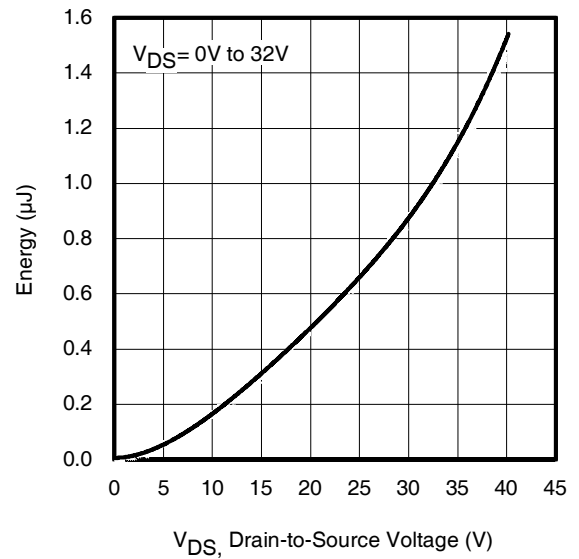


Fig 12. Typical  $C_{OSS}$  Stored Energy

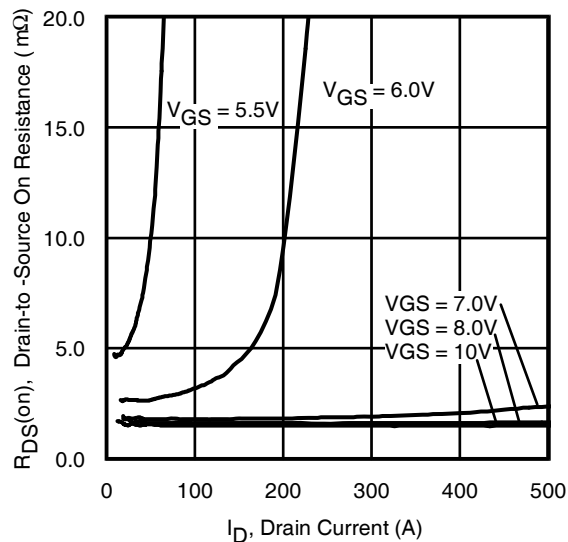


Fig 13. Typical On-Resistance vs. Drain Current

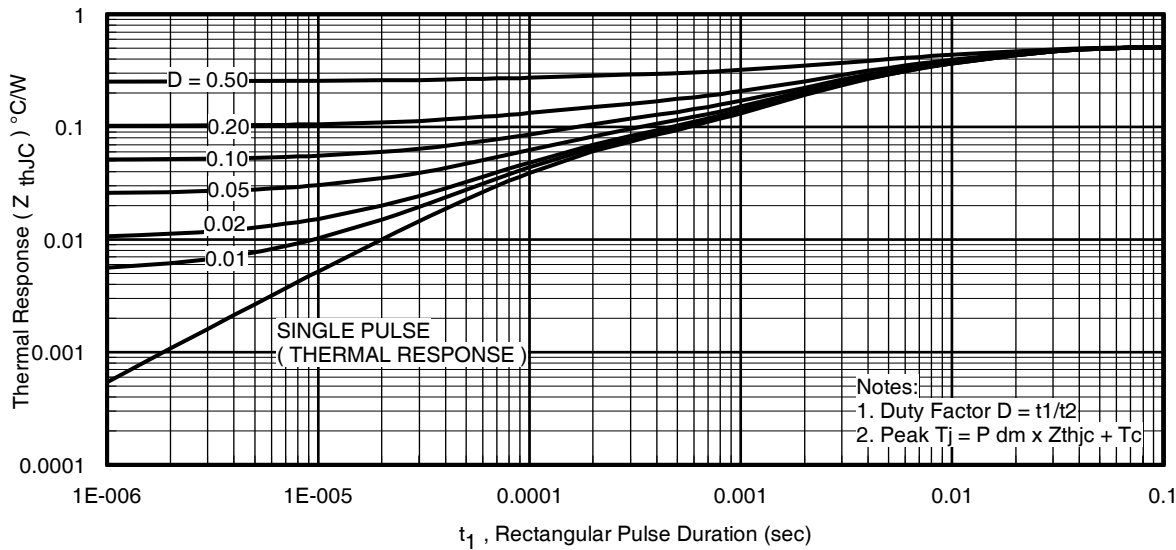


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

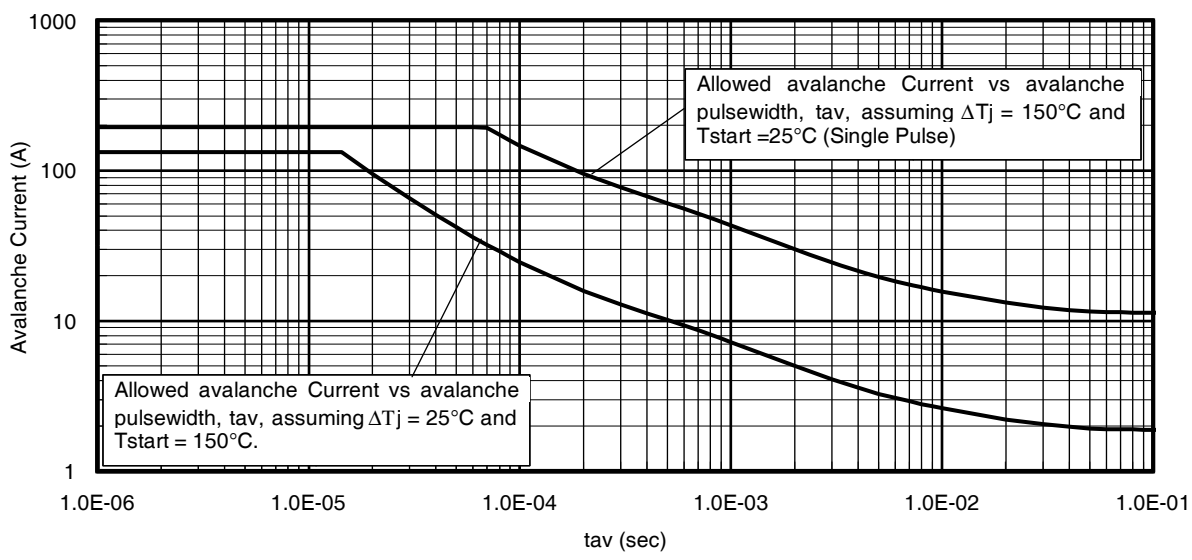


Fig 14. Avalanche Current vs. Pulse width

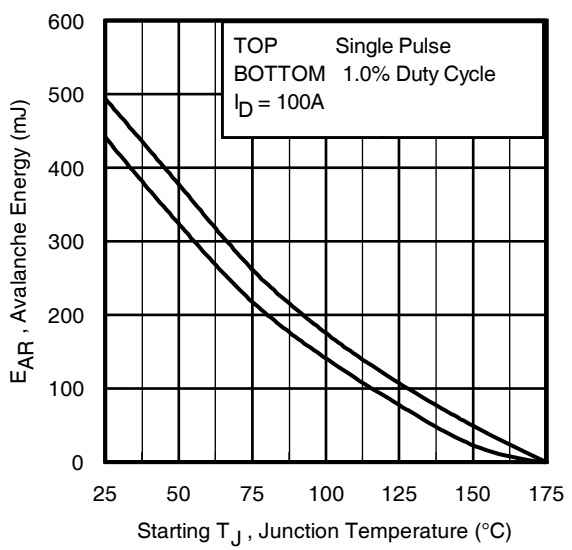


Fig 15. Maximum Avalanche Energy vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 14, 15:**  
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 22a, 22b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [ 1.3 \cdot BV \cdot Z_{th} ]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

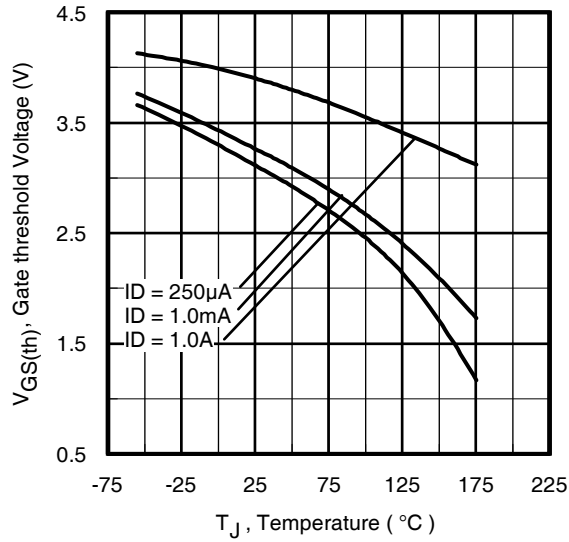


Fig 16. Threshold Voltage vs. Temperature

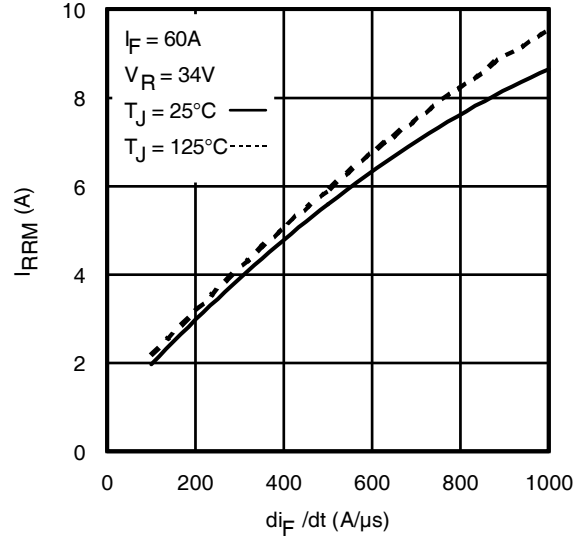


Fig 17 - Typical Recovery Current vs.  $di_f/dt$

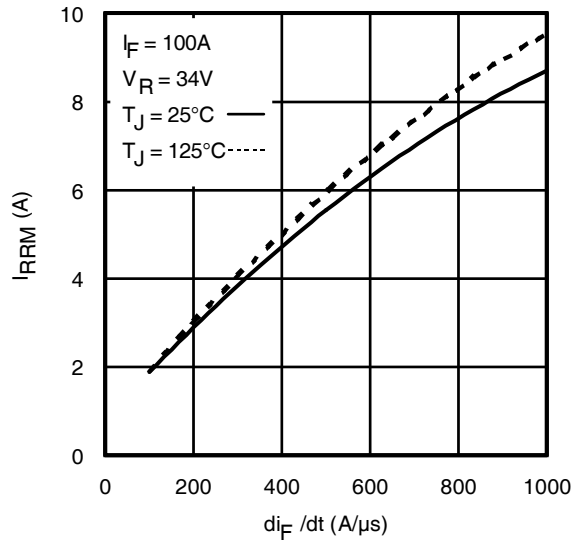


Fig 18 - Typical Recovery Current vs.  $di_f/dt$

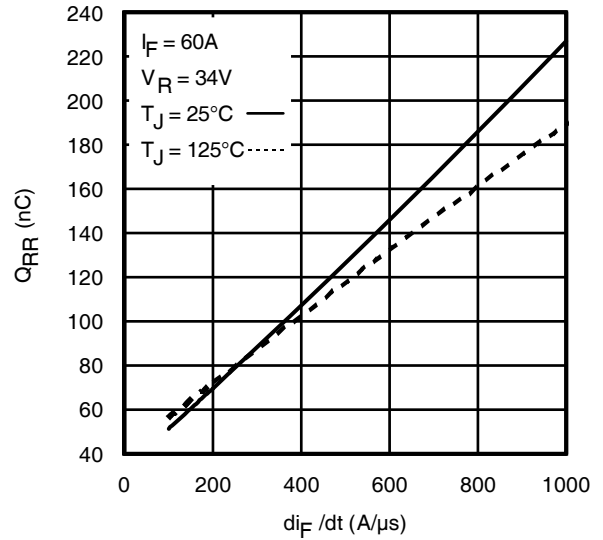


Fig 19 - Typical Stored Charge vs.  $di_f/dt$

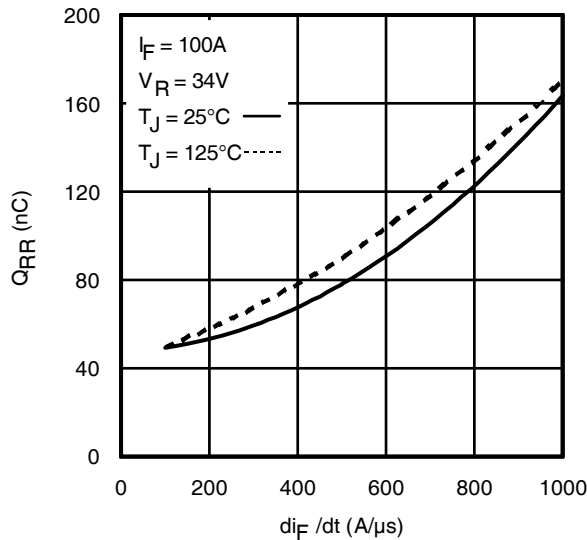
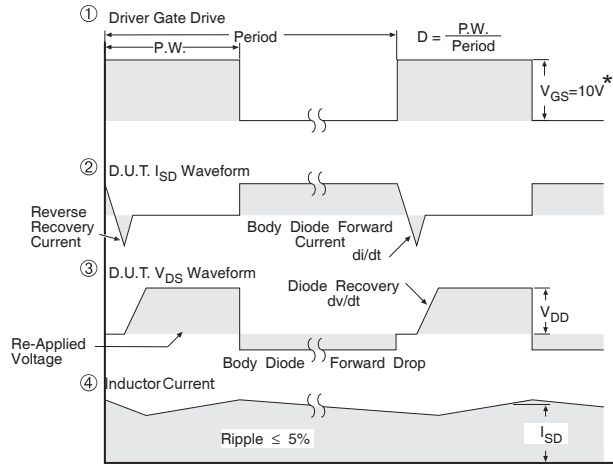
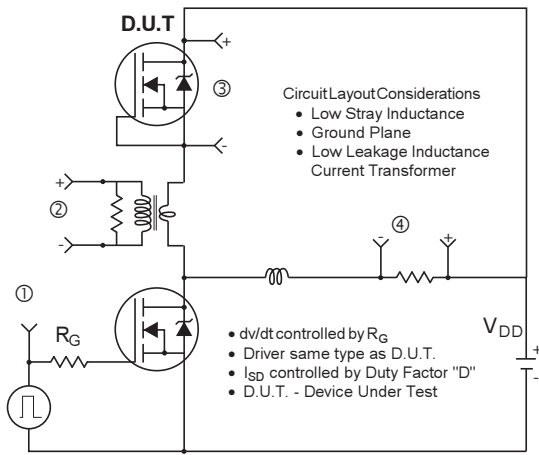
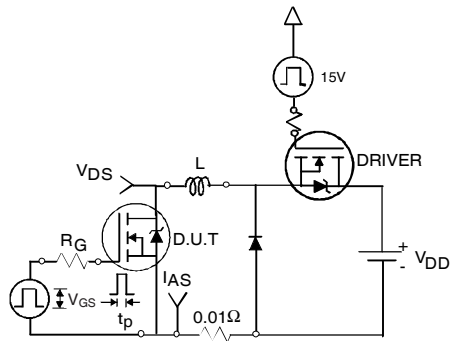


Fig 20 - Typical Stored Charge vs.  $di_f/dt$

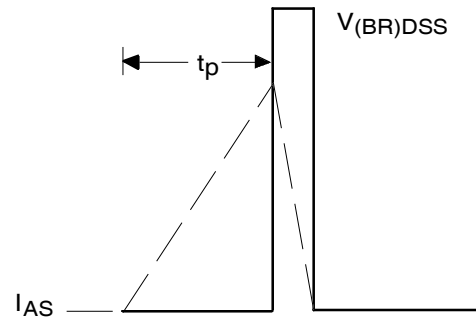


\*  $V_{GS} = 5V$  for Logic Level Devices

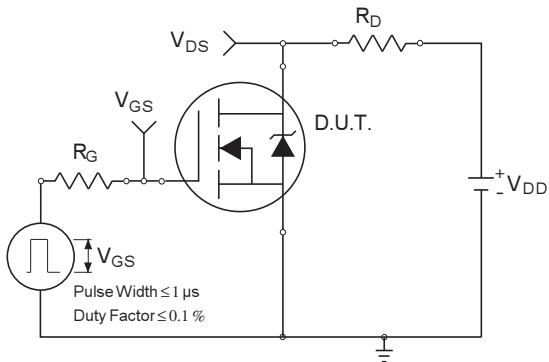
**Fig 21. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs**



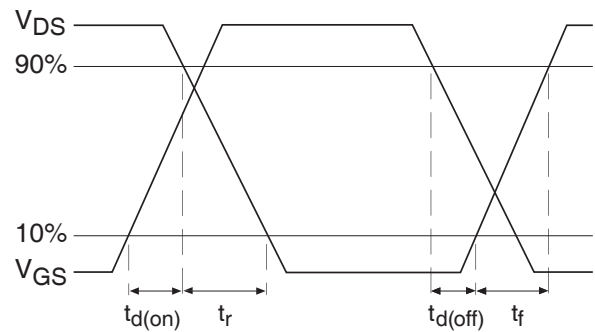
**Fig 22a. Unclamped Inductive Test Circuit**



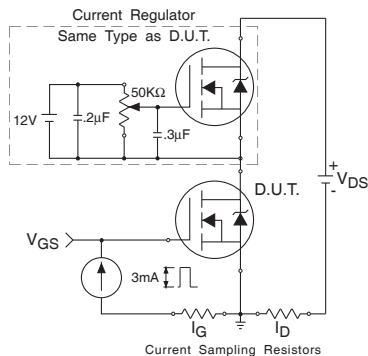
**Fig 22b. Unclamped Inductive Waveforms**



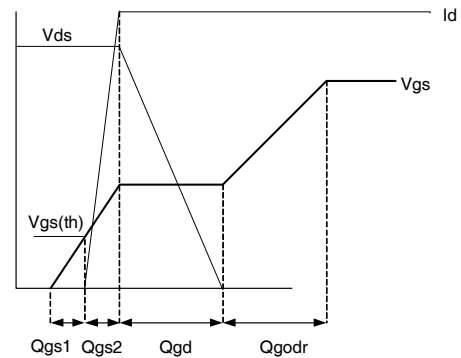
**Fig 23a. Switching Time Test Circuit**



**Fig 23b. Switching Time Waveforms**



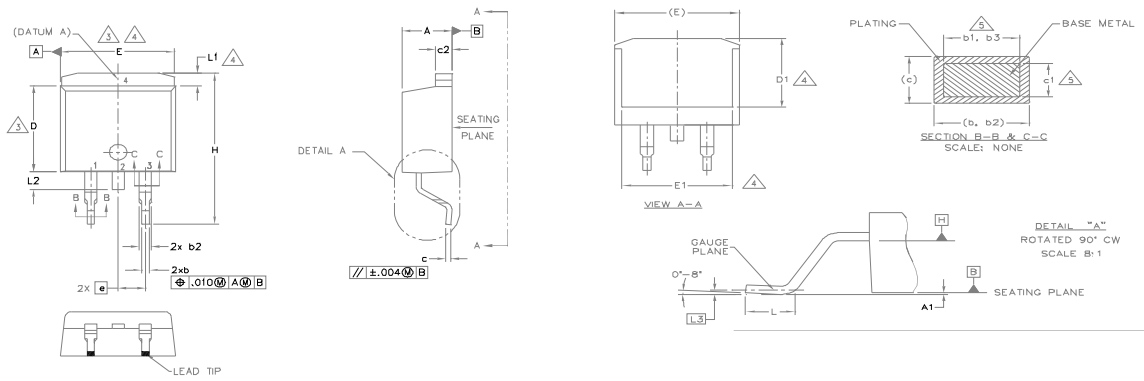
**Fig 24a. Gate Charge Test Circuit**



**Fig 24b. Gate Charge Waveform**

# D<sup>2</sup>Pak (TO-263AB) Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	5
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245	-	4
e	2.54 BSC		.100 BSC		4
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	-	1.68	-	.066	
L2	-	1.78	-	.070	
L3	0.25 BSC		.010 BSC		

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
  3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [,.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
  4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
  5. DIMENSION b1, b3 AND c1 APPLY TO BASE METAL ONLY.
  6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
  7. CONTROLLING DIMENSION: INCH.
  8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

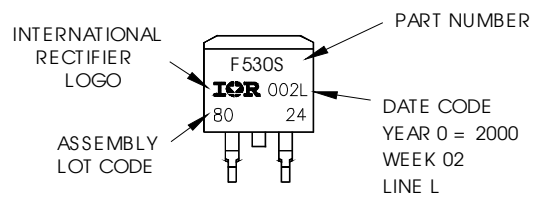
LEAD ASSIGNMENTS

- DIODES
- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
  - 2, 4.- CATHODE
  - 3.- ANODE
- HEXFET
- 1.- GATE
  - 2, 4.- DRAIN
  - 3.- SOURCE
- IGBTs, CoPACK
- 1.- GATE
  - 2, 4.- COLLECTOR
  - 3.- EMITTER

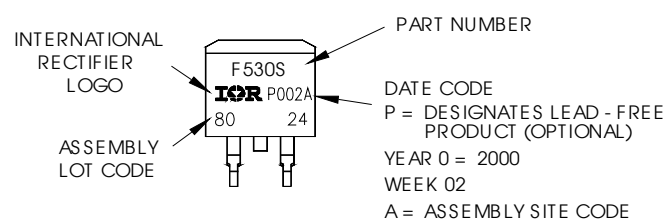
## D<sup>2</sup>Pak (TO-263AB) Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH LOT CODE 8024 ASSEMBLED ON WW 02, 2000 IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position indicates "Lead - Free"



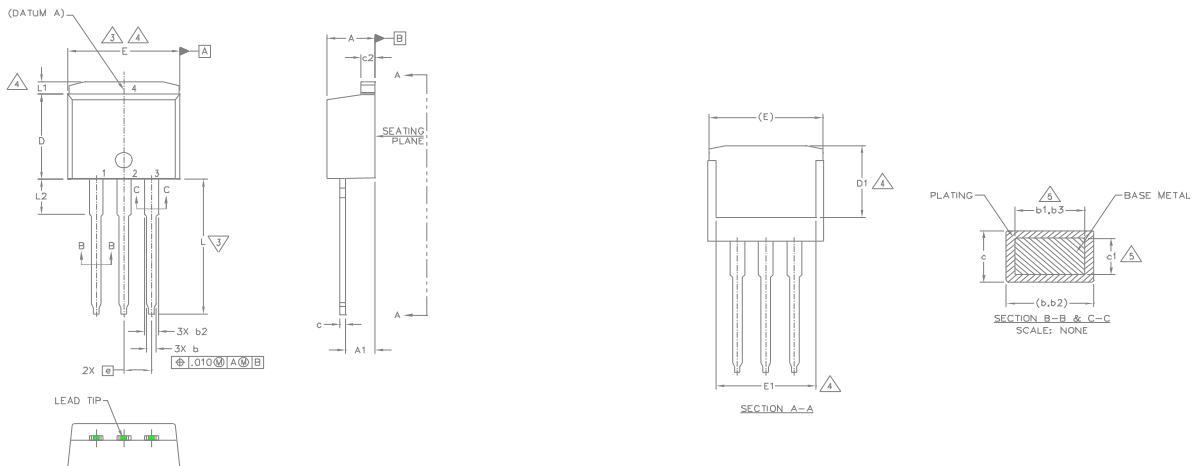
OR



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

# TO-262 Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245	-	4
e	2.54 BSC		.100 BSC		
L	13.46	14.10	.530	.555	
L1	-	1.65	-	.065	4
L2	3.56	3.71	.140	.146	

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
  3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
  4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
  5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
  6. CONTROLLING DIMENSION: INCH.
  7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

LEAD ASSIGNMENTS

- IGBTs, CoPACK
- 1.- GATE
  - 2.- COLLECTOR
  - 3.- EMITTER
  - 4.- COLLECTOR

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

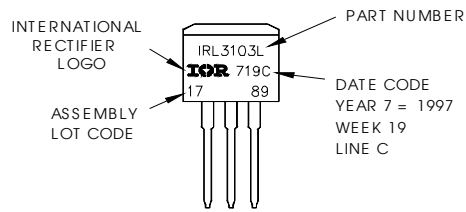
DIODES

- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
- 2, 4.- CATHODE
- 3.- ANODE

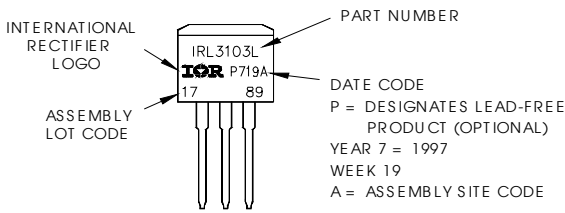
## TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"

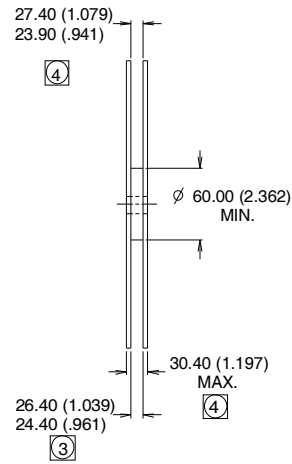
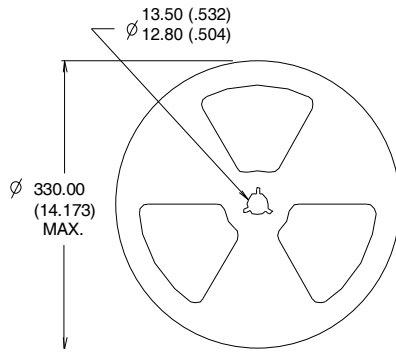
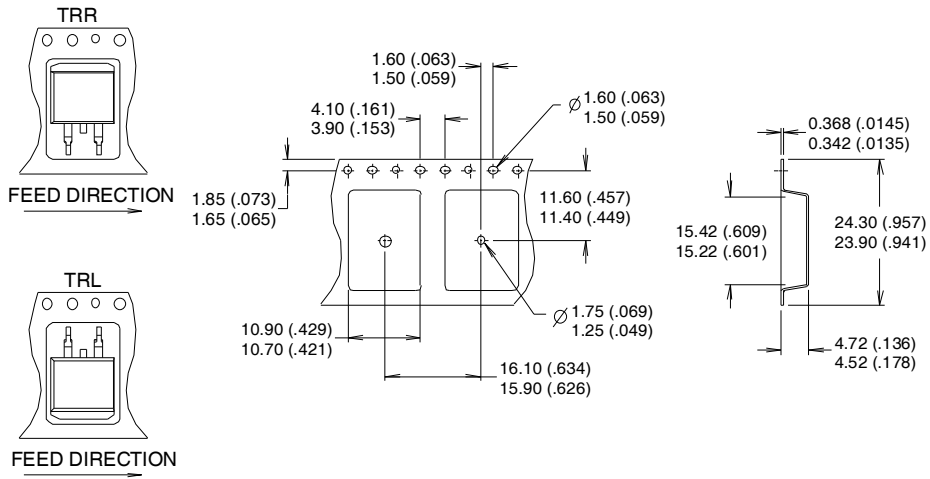


OR



Note: For the most current drawing please refer to IRF website at <http://www.irf.com/package/>

D<sup>2</sup>Pak (TO-263AB) Tape & Reel Information Dimensions are shown in millimeters (inches)



- NOTES:
1. CONFORMS TO EIA-418.
  2. CONTROLLING DIMENSION: MILLIMETER.
  - ③ DIMENSION MEASURED @ HUB.
  - ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

**Qualification information†**

Qualification level	Industrial	
	(per JEDEC JESD47F )††	
Moisture Sensitivity Level	D <sup>2</sup> Pak	MSL1
	TO-262	N/A
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier’s web site: <http://www.irf.com/product-info/reliability>

†† Applicable version of JEDEC standard at the time of product release.

**Revision History**

Date	Comment
11/19/2014	<ul style="list-style-type: none"> <li>• Updated <math>E_{AS(L=1mH)} = 1098mJ</math> on page 2</li> <li>• Updated note 9 “Limited by <math>T_{Jmax}</math>, starting <math>T_J = 25^{\circ}C</math>, <math>L = 1mH</math>, <math>R_G = 50\Omega</math>, <math>I_{AS} = 47A</math>, <math>V_{GS} = 10V</math>”. on page 2</li> <li>• Updated package outline on page 9 and 10.</li> </ul>

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