



**THE DATASHEET OF
IRLR8103**

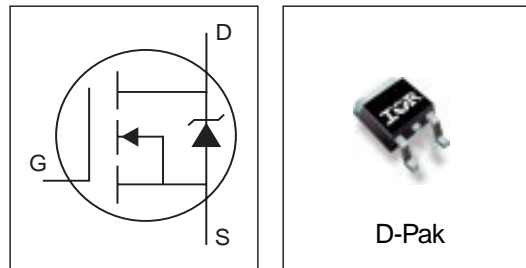


- N-Channel Application-Specific MOSFETs
- Ideal for CPU Core DC-DC Converters
- Low Conduction Losses
- Low Switching Losses
- Minimizes Parallel MOSFETs for high current applications

HEXFET® Chipset for DC-DC Converters

Description

These new devices employ advanced HEXFET® power MOSFET technology to achieve an unprecedented balance of on-resistance and gate charge. The reduced conduction and switching losses make them ideal for high efficiency DC-DC converters that power the latest generation of microprocessors.



Both the IRLR8103 and IRLR8503 have been optimized and are 100% tested for all parameters that are critical in synchronous buck converters including $R_{DS(on)}$, gate charge and Cdv/dt-induced turn-on immunity. The IRLR8103 offers particularly low $R_{DS(on)}$ and high Cdv/dt immunity for synchronous FET applications. The IRLR8503 offers an extremely low combination of Q_{sw} & $R_{DS(on)}$ for reduced losses in control FET applications.

DEVICE RATINGS (typ.)

	IRLR8103	IRLR8503
V_{DS}	30V	30V
$R_{DS(on)}$	6 mΩ	12 mΩ
Q_G	45 nC	15 nC
Q_{sw}	20.3 nC	5.4 nC
Q_{oss}	23 nC	23 nC

The package is designed for vapor phase, infrared, convection, or wave soldering techniques. Power dissipation of greater than 80W is possible in a typical PCB mount application.

Absolute Maximum Ratings

Parameter	Symbol	IRLR8103	IRLR8503	Units
Drain-Source Voltage	V_{DS}	30		V
Gate-Source Voltage	V_{GS}	±20		
Continuous Drain or Source Current ($V_{GS} \geq 10V$)	$T_A = 25^\circ C$	89 ^⑤	49 ^⑤	A
	$T_L = 90^\circ C$	61 ^⑤	34 ^⑤	
Pulsed Drain Current ^①	I_{DM}	350	196	
Power Dissipation	$T_A = 25^\circ C$	89	62	W
	$T_L = 90^\circ C$	42	30	
Junction & Storage Temperature Range	T_J, T_{STG}	-55 to 150		°C
Continuous Source Current (Body Diode)	I_S	89 ^⑤	49 ^⑤	A
Pulsed Source Current ^①	I_{SM}	350	196	

Thermal Resistance

Parameter		Max.		Units
Maximum Junction-to-Ambient PCB ^③	$R_{\theta JA}$	50		°C/W
Maximum Junction-to-Case	$R_{\theta JC}$	1.4	2.0	°C/W

IRLR8103/IRLR8503

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Electrical Characteristics		IRLR8103			IRLR8503			Units	Conditions
Parameter		Min	Typ	Max	Min	Typ	Max		
Drain-to-Source Breakdown Voltage*	V_{DS}	30	-	-	30	-	-	V	$V_{GS} = 0V, I_D = 250\mu A$
Static Drain-Source on Resistance*	$R_{DS(on)}$	-	6	7.0	-	12	16	m Ω	$V_{GS} = 10V, I_D = 15A$ ②
		-	7	8.5	-	14	18	m Ω	$V_{GS} = 4.5V, I_D = 15A$ ②
Gate Threshold Voltage*	$V_{GS(th)}$	2.0	-	-	1.0	-	-	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
Drain-Source Leakage Current*	I_{DSS}	-	-	30	-	-	30	μA	$V_{DS} = 24V, V_{GS} = 0$
		-	-	150	-	-	150		$V_{DS} = 24V, V_{GS} = 0,$ $T_j = 100^\circ C$
Gate-Source Leakage Current*	I_{GSS}	-	-	± 100	-	-	± 100	nA	$V_{GS} = \pm 20V$
Total Gate Chg Cont FET*	Q_G	-	50	-	-	15	-	nC	$V_{GS} = 5V, I_D = 15A, V_{DS} = 16V$
Total Gate Chg Sync FET*	Q_G	-	45	-	-	13	-		$V_{GS} = 5V, V_{DS} < 100mV$
Pre-Vth Gate-Source Charge	Q_{GS1}	-	17	-	-	3.7	-		$V_{DS} = 16V, I_D = 15A$
Post-Vth Gate-Source Charge	Q_{GS2}	-	4.3	-	-	1.3	-		
Gate to Drain Charge	Q_{GD}	-	16	-	-	4.1	-		
Switch Chg($Q_{GS2} + Q_{GD}$)*	Q_{sw}	-	20.3	-	-	5.4	-		
Output Charge*	Q_{oss}	-	23	-	-	23	-	$V_{DS} = 16V, V_{GS} = 0$	
Gate Resistance	R_G	-	1.5	-	-	2.0	-	Ω	
Turn-on Delay Time	$t_d(on)$	-	TBD	-	-	TBD	-	ns	$V_{DD} = 16V, I_D = 15A$
Rise Time	t_r	-	TBD	-	-	TBD	-		$V_{GS} = 5V$
Turn-off Delay Time	$t_d(off)$	-	TBD	-	-	TBD	-		Clamped Inductive Load
Fall Time	t_f	-	TBD	-	-	TBD	-		See test diagram Fig 19.
Input Capacitance	C_{iss}	-	TBD	-	-	TBD	-	pF	$V_{DS} = 16V, V_{GS} = 0$
Output Capacitance	C_{oss}	-	TBD	-	-	TBD	-		
Reverse Transfer Capacitance	C_{rss}	-	TBD	-	-	TBD	-		

Source-Drain Rating & Characteristics

Parameter		Min	Typ	Max	Min	Typ	Max	Units	Conditions
Diode Forward Voltage*	V_{SD}	-	-	0.9	-	-	1.0	V	$I_S = 15A$ ②, $V_{GS} = 0V$
Reverse Recovery Charge④	Q_{rr}	-	100	-	-	89	-	nC	$di/dt \sim 700A/\mu s$ $V_{DS} = 16V, V_{GS} = 0V, I_S = 15A$
Reverse Recovery Charge (with Parallel Schottky)④	$Q_{rr(s)}$	-	77	-	-	75	-		$di/dt = 700A/\mu s$ (with 10BQ040) $V_{DS} = 16V, V_{GS} = 0V, I_S = 15A$

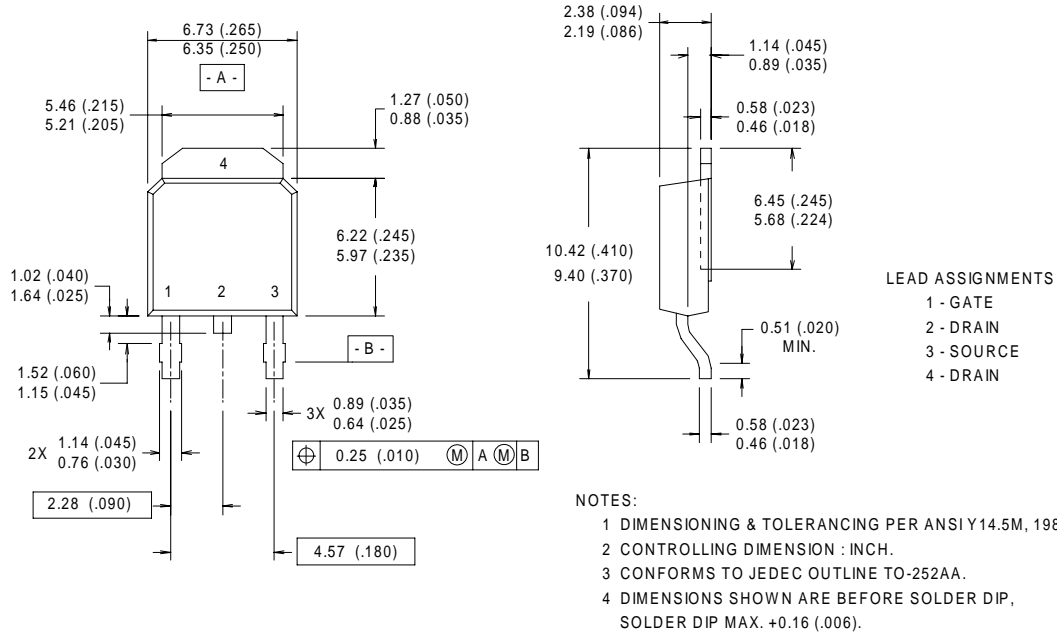
Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. ④ Typ = measured - Q_{oss}
 ② Pulse width $\leq 300 \mu s$; duty cycle $\leq 2\%$. ⑤ Calculated continuous current based on maximum allowable Junction temperature; package limitation current = 20A
 ③ When mounted on 1 inch square copper board, $t < 10$ sec. * Devices are 100% tested to these parameters.

Package Outline

TO-252AA Outline

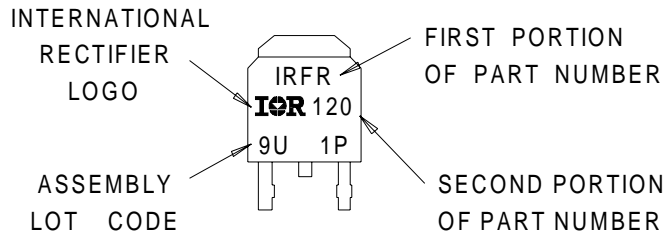
Dimensions are shown in millimeters (inches)



Part Marking Information

TO-252AA (D-PARK)

EXAMPLE : THIS IS AN IRFR120
 WITH ASSEMBLY
 LOT CODE 9U1P

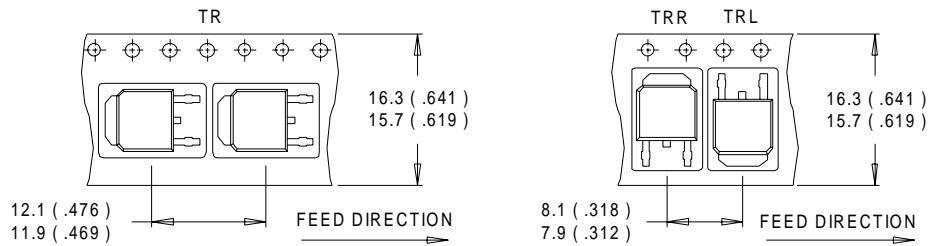


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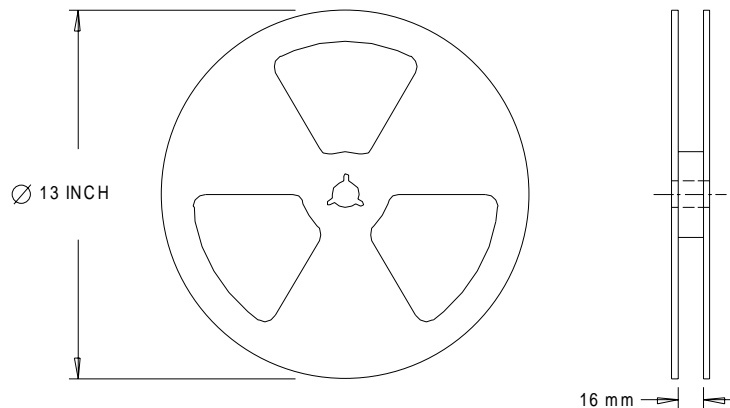
Tape & Reel Information

TO-252AA



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

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WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331

IR GREAT BRITAIN: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020

IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200

IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590

IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111

IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086

IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 838 4630

IR TAIWAN: 16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673, Taiwan Tel: 886-2-2377-9936

<http://www.irf.com/> Data and specifications subject to change without notice. 11/98

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