THE DATASHEET OF

ISL78229ARZ

ISL78229

2-Phase Boost Controller with Drivers and I²C/PMBus

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The ISL78229 is an automotive grade (AEC-Q100 Grade 1), 2-phase 55V synchronous boost controller that simplifies the design of high power boost applications. It integrates strong half-bridge drivers, an analog/digital tracking input, comprehensive protection functions, and a PMBus interface for added control and telemetry.

The ISL78229 enables a simple, modular design for systems requiring power and thermal scalability. It offers peak-current mode control for fast line response and simple compensation. Its synchronous 2-phase architecture enables it to support higher current while reducing the size of input and output capacitors. The integrated drivers feature programmable adaptive dead time control, offering flexibility in power stage design. The ISL78229 offers a 90° output clock and supports 1-, 2-, and 4-phases.

The ISL78229 offers a highly robust solution for the most demanding environments. Its unique soft-start control prevents large negative current even in extreme cases, such as a restart under high output pre-bias on high volume capacitances. It also offers two levels of cycle-by-cycle OCP, average current limiting, input OVP, output UVP/OVP, and internal OTP. A thermistor input provides external OTP for the power-stage elements. In the event of a fault, the ISL78229 offers individually programmable latch-off or hiccup recovery for each fault type.

Also integrated are several functions that ease system design. A unique tracking input controls the output voltage, allowing it to track either a digital duty cycle (PWM) signal or an analog reference. The ISL78229 provides input average current limiting so the system can deliver transient bursts of high load current while limiting the average current to avoid overheating. The ISL78229 PMBus interface provides fault reporting, telemetry, and system control to support functional safety qualification.

Related Literature

For a full list of related documents, visit our website

- ISL78229 product page

Features

- Input/output voltage range: 5V to 55V, withstands 60V transients
- Supports synchronous or standard boost topology
- Peak current mode control with adjustable slope compensation
- Secondary average current control loop
- Integrated 5V 2A sourcing/3A sinking N-channel MOSFET drivers
- Switching frequency: 50kHz to 1.1MHz per phase
- External synchronization
- Programmable minimum duty cycle
- Programmable adaptive dead time control
- Optional diode emulation and phase dropping
- PWM and analog track function
- Forced PWM operation with negative current limiting and protection
- Comprehensive protection/fault reporting
- Selectable hiccup or latch-off fault response
- I²C/PMBus compatible digital interface
- AEC-Q100 qualified, Grade 1: -40°C to +125°C
- 6mmx6mm 40 Ld WFQFN (Wettable Flank QFN) package

Applications

- Automotive power systems (for example, 12V to 24V, 12V to 48V, etc.)
  - Trunk audio amplifiers
  - Start-stop systems
  - Automotive boost applications
- Industrial and telecommunication power supplies

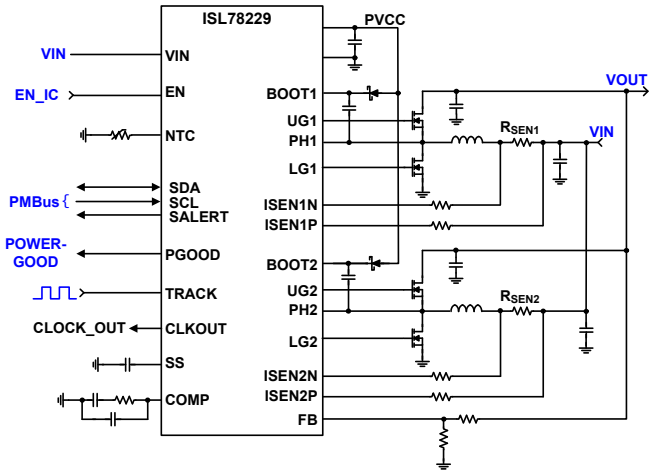
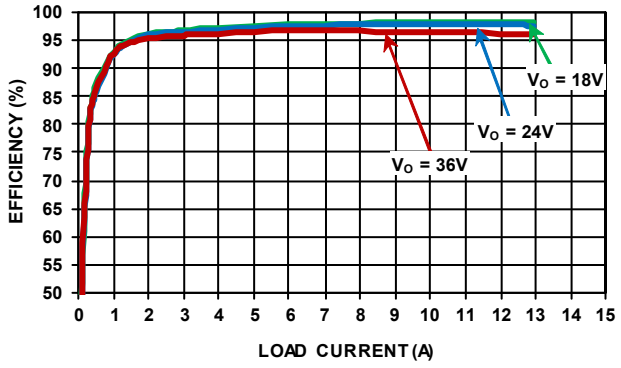


FIGURE 1. SIMPLIFIED APPLICATION SCHEMATIC, 2-PHASE SYNCHRONOUS BOOST



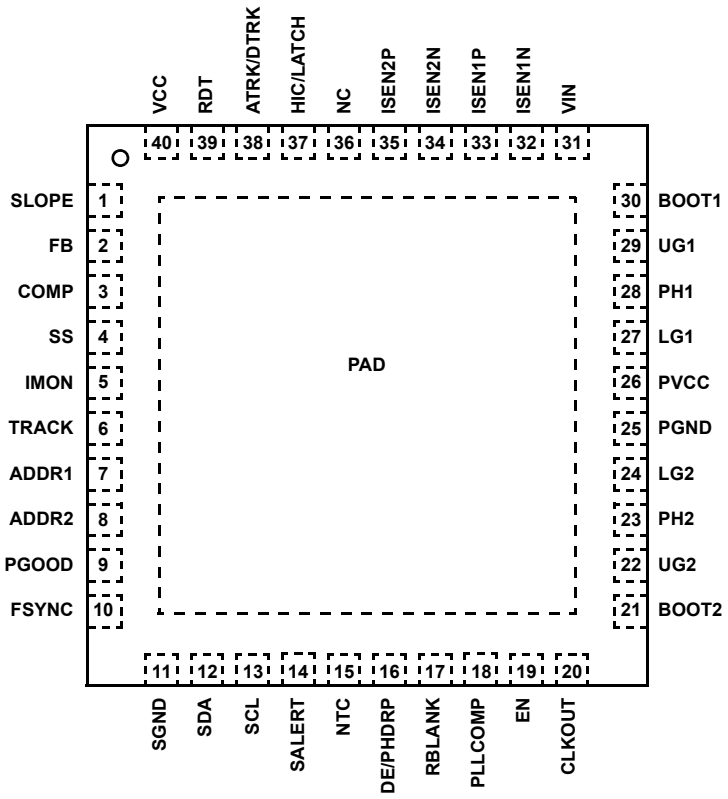
NOTE: (See Typical Application in Figure 4 on page 8.)

FIGURE 2. EFFICIENCY CURVES, V_{IN} = 12V, T_A = +25°C

Table of Contents

Pin Configuration

40 LD 6x6 WFQFN
TOP VIEW



Functional Pin Description

PIN NAME	PIN #	DESCRIPTION
SLOPE	1	Programs the slope of the internal slope compensation. A resistor should be connected from the SLOPE pin to GND. Refer to "Adjustable Slope Compensation" on page 33 for information about how to select this resistor value.
FB	2	The inverting input of the error amplifier for the voltage regulation loop. A resistor network must be placed between the FB pin and the output rail to set the boost converter's output voltage. Refer to "Output Voltage Setting" on page 65 for more details. This pin also has output overvoltage and undervoltage comparators. Refer to "Output Undervoltage Fault" on page 36 and "Output Overvoltage Fault" on page 36 for more details.
COMP	3	The output of the transconductance error amplifier (Gm1) for the output voltage regulation loop. Place the compensation network between the COMP pin and ground. Refer to "Output Voltage Regulation Loop" on page 26 for more details. The COMP pin voltage can also be controlled by the constant current control loop error amplifier (Gm2) output through a diode (D_{CC}) when the constant current control loop is used to control the input average current. Refer to "Constant Current Control (CC)" on page 37 for more details.
SS	4	A capacitor placed from SS to ground sets up the soft-start ramp rate and in turn, determines the soft-start time. Refer to "Soft-Start" on page 31 for more details.
IMON	5	The average current monitor pin for the sum of the two phases' inductor currents. It is used for average current limiting and average current protection functions. The sourcing current from the IMON pin is the sum of the two CSA's outputs plus a fixed 17µA offset current. With each CSA sensing individual phase's inductor current, the IMON signal represents the sum of the two phases' inductor currents and is the input current for the boost. Place a resistor in parallel with a capacitor from IMON to ground. The IMON pin output current signal builds up the average voltage signal representing the average current sense signals. A constant average current limiting function and an average current protection are implemented based on the IMON signal. • Constant Average Current Limiting: A Constant Current (CC) control loop is implemented to limit the IMON average current signal using a 1.6V reference, which ultimately limits the total input average current to a constant level. • Average Current Protection: If the IMON pin voltage is higher than 2V, the part goes into either Hiccup or Latch-off fault protection as described in "Fault Response Register SET_FAULT_RESPONSE (D2h)" on page 35. Refer to "Average Current Sense for 2 Phases - IMON" on page 32 for more details.

Functional Pin Description (Continued)

PIN NAME	PIN #	DESCRIPTION
TRACK	6	External reference input pin for the IC output voltage regulation loop to follow. The input reference signal can be either a digital or analog signal selected by the ATRK/DTRK pin configuration. If the TRACK function is not used, connect the TRACK pin to VCC and the internal VREF_DAC works as the reference. Refer to "Digital/Analog TRACK Function" on page 26 for more details.
ADDR1	7	ADDR1, a logic input in combination with ADDR2, selects one of four bus addresses. Refer to "Device Identification Address and Read/Write" on page 42 for more details.
ADDR2	8	ADDR2, a logic input in combination with ADDR1, selects one of four bus addresses. Refer to "Device Identification Address and Read/Write" on page 42 for more details.
PGOOD	9	Provides an open-drain power-good signal. Pull up this pin with a resistor to this IC's VCC for proper function. When the output voltage is within OV/UV thresholds and soft-start is completed, the internal PGOOD open-drain transistor is open and PGOOD is pulled HIGH. It is pulled low when output UV/OV or input OV conditions are detected. Refer to "PGOOD Signal" on page 31 for more details.
FSYNC	10	A dual-function pin for switching frequency setting and synchronization defined as follows: • The PWM switching frequency can be programmed by a resistor R_{FSYNC} from this pin to ground. The PWM frequency refers to a single-phase switching frequency in this datasheet. The typical programmable frequency range is 50kHz to 1.1MHz. • The PWM switching frequency can also be synchronized to an external clock applied on the FSYNC pin. The FSYNC pin detects the input clock signal's rising edge to be synchronized with. The typical detectable minimum pulse width of the input clock is 20ns. The rising edge of LG1 is delayed by 35ns from the rising edge of the input clock signal at the FSYNC pin. When the internal clock is locked to the external clock, it latches to the external clock. If the external clock on the FSYNC pin is removed, the switching frequency oscillator shuts down. The part then detects a PLL_LOCK fault and goes to either Hiccup mode or Latch-off mode as described in "Fault Response Register SET_FAULT_RESPONSE (D2h)" on page 35. If the part is set in Hiccup mode, the part restarts with the frequency set by R_{FSYNC}.
SGND	11	Signal ground pin that the internal sensitive analog circuits refer to. Connect this pin to a large copper ground plane free from large noisy signals. In layout power flow planning, avoid having the noisy high frequency pulse current flowing through the ground area around the IC.
SDA	12	Serial bus data input/output. Requires pull-up.
SCL	13	Serial bus clock input. Requires pull-up.
SALERT	14	PMBus Alert Output. An open-drain output that is pulled low when a fault condition is detected. Requires pull-up. Refer to "Fault Flag Register FAULT_STATUS (D0h) and SALERT Signal" on page 34 for more details.
NTC	15	External temperature sensor input. An NTC resistor from this pin to GND can be used as the external temperature sensing component. A 20µA current sources out of this pin. The voltage at this pin is 20µA times the NTC resistor, which represents the temperature. The voltage on this pin is converted by the internal ADC and stored in the NTC register which can be read over the PMBus. Refer to "External Temperature Monitoring and Protection (NTC Pin)" on page 38 for more details.
DE/PHDRP	16	Used to select Diode Emulation mode (DE), Phase Dropping (PH_DROP) mode, or Continuous Conduction Mode (CCM). There are 3 configurable modes: 1. DE mode; 2. DE plus PH_DROP mode; 3. CCM mode. Refer to Table 2 on page 34 for the three configurable options. The phase dropping mode is **not allowed** with external synchronization.
RBLANK	17	A resistor from this pin to ground programs the blanking time for current sensing after the PWM is ON (LG is ON). This blanking time is also called t_{MINON} time, meaning the minimum ON-time when a PWM pulse is ON. Refer to "Minimum On-Time (Blank Time) Consideration" on page 30 for information about R_{BLANK}.
PLLCOMP	18	The compensation node for the switching frequency clock's Phase Lock Loop (PLL). A second order passive loop filter connected between this pin and ground compensates the PLL. Refer to "Oscillator and Synchronization" on page 29 for more details.
EN	19	A threshold-sensitive enable input for the controller. When the EN pin is driven above 1.2V, the ISL78229 is enabled and the internal LDO is activated to power up PVCC followed by a start-up procedure. Driving the EN pin below 0.95V disables the IC and clears all fault states. Refer to "Enable" on page 31 for more details.
CLKOUT	20	Outputs a clock signal with same frequency to one phase's switching frequency. The rising edge signal on the CLKOUT pin is delayed by 90° from the rising edge of LG1 of the same IC. With CLKOUT connected to the FSYNC pin of the second ISL78229, a 4-phase interleaving operation can be achieved. Refer to "Oscillator and Synchronization" on page 29 for more details.

Functional Pin Description (Continued)

PIN NAME	PIN #	DESCRIPTION
BOOT2	21	Provides bias voltage to the Phase 2 high-side MOSFET driver. A bootstrap circuit creates a voltage suitable to drive the external N-channel MOSFET. A 0.47µF ceramic capacitor in series with a 1.5Ω resistor are recommended between the BOOT2 and PH2 pins. In the typical configuration, PVCC provides the bias to BOOT2 through a fast switching diode. In applications in which a high-side driver is not needed (for example, a standard boost application), BOOT2 is recommended to be connected to ground. The ISL78229 IC can detect BOOT2 being grounded during start-up and both the Phase 1 and Phase 2 high-side drivers are disabled. In addition, PH1 and PH2 should also be tied to ground.
UG2	22	Phase 2 high-side gate driver output. Disable this output by tying either BOOT1 and PH1 to ground or BOOT2 and PH2 to ground.
PH2	23	This pin represents the return path for the Phase 2 high-side gate drive. Connect this pin to the source of the Phase 2 high-side MOSFETs and the drain of the low-side MOSFETs.
LG2	24	Phase 2 low-side gate driver output. It should be connected to the Phase 2 low-side MOSFETs' gates.
PGND	25	Provides the return path for the low-side MOSFET drivers. This pin carries a noisy driving current, so the traces connecting from this pin to the low-side MOSFET source and PVCC decoupling capacitor ground pad should be as short as possible. All the sensitive analog signal traces should not share common traces with this driver return path. Connect this pin to the ground copper plane (wiring away from the IC instead of connecting through the IC bottom PAD) through several vias as close as possible to the IC.
PVCC	26	Output of the internal linear regulator that provides bias for the low-side driver, high-side driver (PVCC connected to BOOTx through diodes) and VCC bias (PVCC and VCC are typically connected through a small resistor like 10Ω or smaller, which helps to filter out the noises from PVCC to VCC). The PVCC operating range is 4.75V to 5.5V. A minimum 10µF decoupling ceramic capacitor should be used between PVCC and PGND. Refer to "Internal 5.2V LDO" on page 39 for more details.
LG1	27	Phase 1 low-side gate driver output. It should be connected to the Phase 1 low-side MOSFETs' gates.
PH1	28	Connect this pin to the source of the Phase 1 high-side MOSFETs and the drain of the low-side MOSFETs. This pin represents the return path for the Phase 1 high-side gate drive.
UG1	29	Phase 1 high-side MOSFET gate drive output. Disable this output by tying either BOOT1 and PH1 to ground or BOOT2 and PH2 to ground.
BOOT1	30	Provides bias voltage to the Phase 1 high-side MOSFET driver. A bootstrap circuit creates a voltage suitable to drive the external N-channel MOSFET. A 0.47µF ceramic capacitor in series with a 1.5Ω resistor are recommended between BOOT1 and PH1 pins. In a typical configuration, PVCC provides the bias to BOOT1 through a fast switching diode. In applications in which a high-side driver is not needed (for example, standard boost application), the BOOT1 is recommended to be connected to ground. The ISL78229 IC can detect BOOT1 being grounded during start-up and both the Phase 1 and Phase 2 high-side drivers are disabled. In addition, PH1 and PH2 should also be tied to ground.
VIN	31	Connect the supply rail to this pin. Typically, connect the boost input voltage to this pin. The VIN pin can also be supplied by a separate input source independent from the boost power stage input source. This pin is connected to the input of the internal linear regulator, generating the power necessary to operate the chip. The DC voltage applied to the VIN should not exceed 55V during normal operation. VIN can withstand transients up to 60V, but in this case, the device's overvoltage protection stops it from switching to protect itself. Refer to "Input Overvoltage Fault" on page 35 for more details.
ISEN1N	32	The negative potential input to the Phase 1 current sense amplifier. This amplifier continuously senses the Phase 1 inductor current through a power current sense resistor in series with the inductor. The sensed current signal is used for current mode control, peak current limiting, average current limiting, and diode emulation.
ISEN1P	33	The positive potential input to the Phase 1 current sense amplifier.
ISEN2N	34	The negative potential input to the Phase 2 current sense amplifier. This amplifier continuously senses the Phase 2 inductor current through a power current sense resistor in series with the inductor. The sensed current signal is used for current mode control, peak current limiting, average current limiting, and diode emulation.
ISEN2P	35	The positive phase input to the Phase 2 current sense amplifier.
NC	36	Not connected. This pin is not electrically connected internally.
HIC/LATCH	37	Selects either the Hiccup or Latch-off response to faults, including output overvoltage (monitoring the FB pin), output undervoltage (monitoring the FB pin, default inactive), V_{IN} overvoltage (monitoring the FB pin), peak overcurrent protection (OC2), average current protection (monitoring the IMON pin), and over-temperature protection (monitoring the NTC pin), etc. Set HIC/LATCH = HIGH to activate the Hiccup fault response. Set HIC/LATCH = LOW to activate the Latch-off fault response. Either toggling the EN pin or recycling VCC POR resets the IC from Latch-off status. Refer to "Fault Response Register SET_FAULT_RESPONSE (D2h)" on page 35 and Table 3 on page 41 for more details.

Functional Pin Description (Continued)

PIN NAME	PIN #	DESCRIPTION
ATRK/DTRK	38	The logic input pin to select the input signal format options for the TRACK pin. Pull this pin HIGH for the TRACK pin to accept analog input signals. Pull this pin LOW for the TRACK pin to accept digital input signals. Refer to "Digital/Analog TRACK Function" on page 26 for more details.
RDT	39	A resistor connected from this pin to ground programs the dead times between UGx OFF to LGx ON and LGx OFF to UGx ON to prevent shoot-through. Refer to "Driver Configuration" on page 25 for the selection of R_{DT}.
VCC	40	IC bias power input pin for the internal analog circuitry. A minimum 1µF ceramic capacitor should be used between VCC and ground for noise decoupling purposes. VCC is typically biased by PVCC or an external bias supply with voltage ranging from 4.75V to 5.5V. Because PVCC provides the pulsing drive current, a small resistor (10Ω or smaller) between PVCC and VCC can help filter out the noises from PVCC to VCC.
PAD	-	Bottom thermal pad. It is not used as an electrical connection to the IC. In layout it must be connected to a PCB large ground copper plane that does not contain noisy power flows. Put multiple vias (as many as possible) in this pad connecting to the ground copper plane to help reduce the IC's θ_{JA}.

Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	TEMP. RANGE (°C)	TAPE AND REEL (UNITS) (Note 1)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL78229ARZ	ISL7822 9ARZ	-40 to +125	-	40 Ld 6x6 WFQFN	L40.6x6C
ISL78229ARZ-T	ISL7822 9ARZ	-40 to +125	4k	40 Ld 6x6 WFQFN	L40.6x6C
ISL78229ARZ-T7A	ISL7822 9ARZ	-40 to +125	250	40 Ld 6x6 WFQFN	L40.6x6C
ISL78229EV1Z	Evaluation Board				

NOTES:

1. Refer to TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), refer to the ISL78229 product information page. For more information about MSL, refer to TB363.

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

PART NUMBER	TOPOLOGY	PMBus	NTC	TRACK FUNCTION	PACKAGE
ISL78229	2-Phase Boost Controller	Yes	Yes	Yes	40 Ld 6x6 WFQFN
ISL78227	2-Phase Boost Controller	No	No	Yes	32 Ld 5x5 WFQFN

Block Diagram

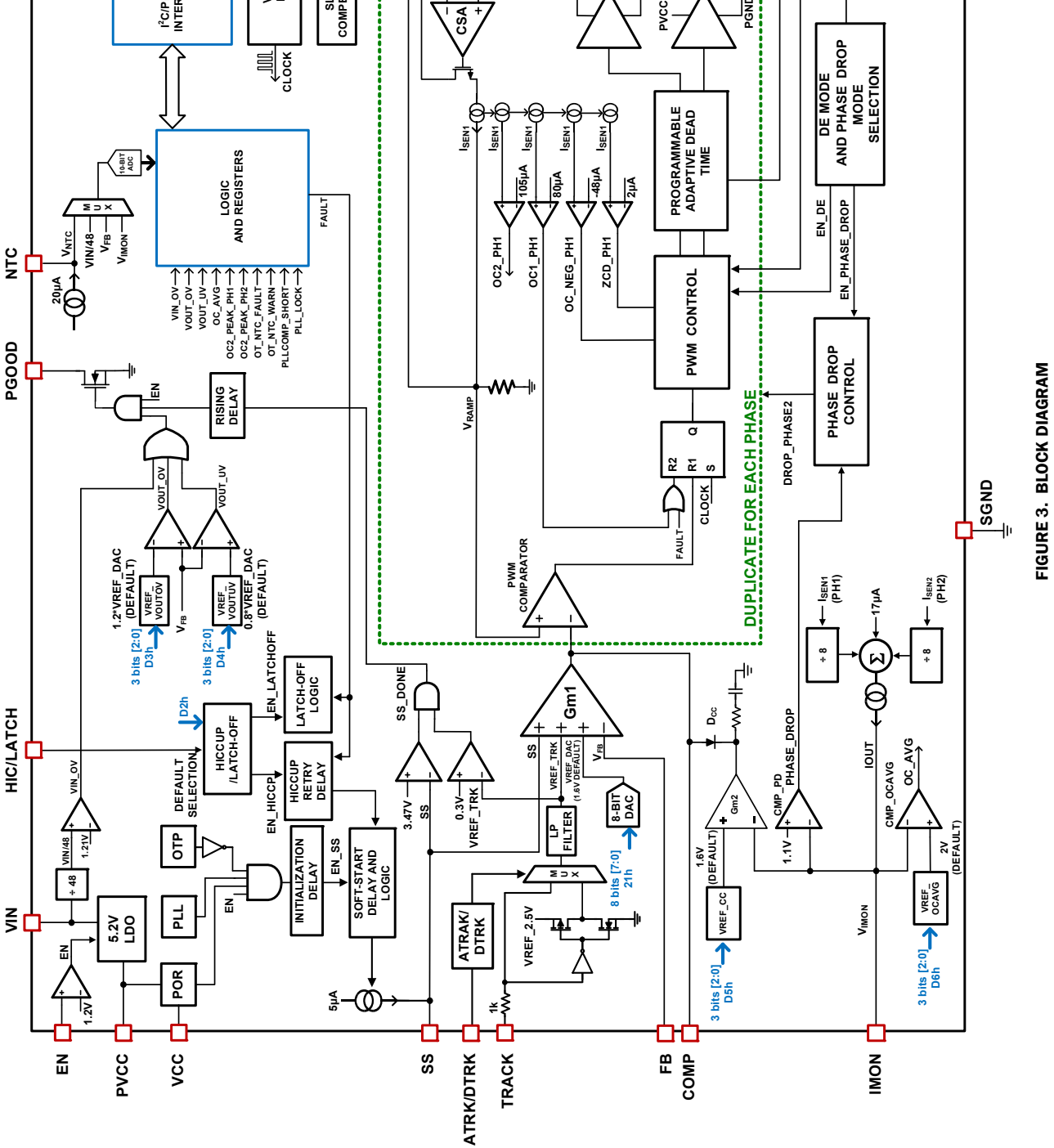
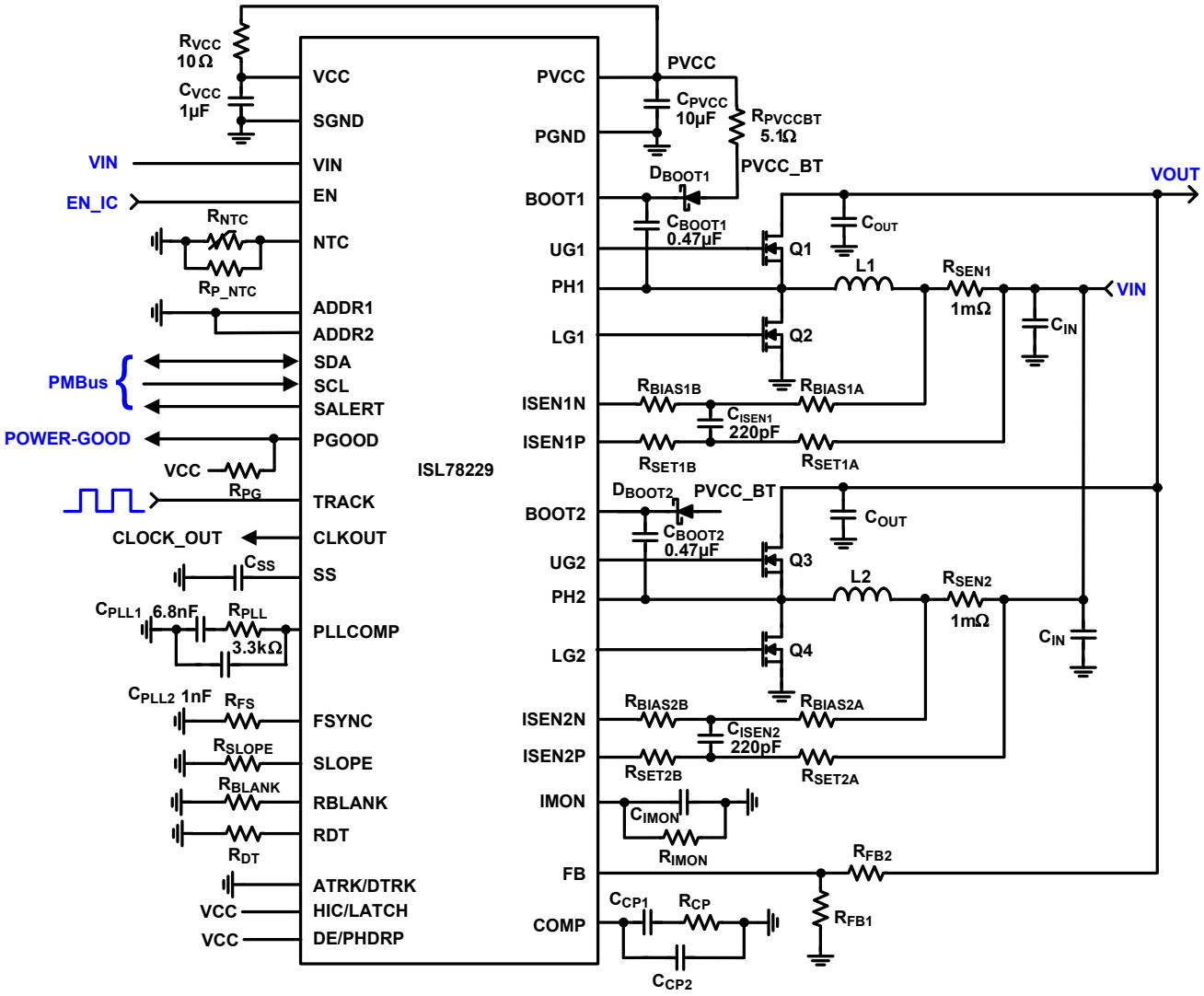


FIGURE 3. BLOCK DIAGRAM

Typical Application - 2-Phase Synchronous Boost



ATRK/DTRK:
= VCC to track analog signal
= GND to track digital signal

HIC/LATCH:
= VCC for HICCUP mode
= GND for LATCHOFF mode

DE/PHDRP:
= VCC for DE mode
= FLOAT for DE and Phase-Drop mode
= GND for CCM mode

Q1, Q2, Q3, Q4: 2 BUK9Y6R0-60E in parallel

FIGURE 4. TYPICAL APPLICATION - 2-PHASE SYNCHRONOUS BOOST

Absolute Maximum Ratings

VIN . . . . . - 0.3V to +60V
PH1, PH2 . . . . . - 0.3V to +60V
. . . . . -10V(<20ns Pulse Width, 25µJ)
BOOT1, BOOT2, UG1, UG2 . . . . . - 0.3V to +65.0V
Upper Driver Supply Voltage, V_{BOOT} - V_{PH} . . . . . - 0.3V to +6.5V
. . . . . -0.3V to +0.9V (<10ns)
PVCC, VCC . . . . . - 0.3V to +6.5V
ISEN1P, ISEN1N, ISEN2P, ISEN2N . . . . . - 0.3V to +60V
V_{ISENxP} - V_{ISENxN} . . . . . ±0.6V
All Other Pins . . . . . - 0.3V to VCC + 0.3V
ESD Rating
Human Body Model (Tested per AEC-Q100-002) 2kV
Charged Device Model (Tested per AEC-Q100-011)
Corner Pins (Note 6) . . . . . N/A
All Other Pins 500V
Latch-Up Rating (Tested per AEC-Q100-004) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
40 Ld 6x6 WFQFN Package (Notes 4, 5)	28	1.2

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

VIN . . . . . 5V to +55V
PVCC, VCC . . . . . 4.75V to 5.5V
PH1, PH2 . . . . . - 0.3V to +55V
Upper Driver Supply Voltage, V_{BOOTx} - V_{PHx} . . . . . 3.5V to 6V
ISEN1P to ISEN1N and ISEN2P to ISEN2N Differential Voltage . . . . ±0.3V
ISEN1P, ISEN1N, ISEN2P, ISEN2N Common-Mode Voltage . . . . 4V to 55V
Operational Junction Temperature Range (Automotive) . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. Refer to TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
6. Per AEC-Q100-011 Paragraph 1.3.9, QFNs have no corner pins.

Electrical Specifications

Refer to Figure 3 on page 7 and Typical Application Schematics (page 8). Operating conditions unless otherwise noted: V_{IN} = 12V, V_{PVCC} = 5.2V, and V_{VCC} = 5.2V, T_A = -40°C to +125°C (Note 8). Typical values are at T_A = +25°C.
Boldface limits apply across the operating temperature range, -40°C to +125°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
SUPPLY INPUT						
Input Voltage Range	V_{IN}	Switching, under the condition of internal LDO having dropout (V_{IN} - PVCC) less than 0.25V	**5**		**55**	V
Input Supply Current to the VIN Pin (IC Enabled)	I_{Q_SW}	EN = 5V, V_{IN} = 12V, PVCC = V_{CC}, BOOT1 and BOOT2 supplied by PVCC, R_{FSYNC} = 40.2k (f_{SW} = 300kHz), LGx = OPEN, UGx = OPEN		8.0	**10.0**	mA
	I_{Q_NON-SW}	EN = 5V, V_{IN} = 12V, PVCC = V_{CC}, BOOT1 and BOOT2 supplied by PVCC, non-switching, LGx = OPEN, UGx = OPEN		6.0	**8.5**	mA
Input Supply Current to the VIN Pin (IC Shutdown)	$I_{\_SD\_VIN\_55V}$	EN = GND, V_{IN} = 55V		0.2	**1.0**	µA
Input Bias Current (IC Shutdown) to Each of ISEN1P/ISEN1N/ISEN2P/ISEN2N Pins	$I_{\_SD\_ISENxP/N}$	EN = GND, V_{IN} = 55V ISEN1P (or ISEN1N/ISEN2P/ISEN2N) = 55V	**-1**	0	**1**	µA
INPUT OVERVOLTAGE PROTECTION						
VIN OVP Rising Threshold (Switching Disable)		EN = 5V, V_{IN} rising	**56.5**	58.0	**59.5**	V
VIN OVP Trip Delay		EN = 5V, V_{IN} rising		5		µs
INTERNAL LINEAR REGULATOR						
LDO Voltage (PVCC pin)	V_{PVCC}	V_{IN} = 6V to 55V, C_{PVCC} = 4.7µF, I_{PVCC} = 10mA	**5.0**	5.2	**5.4**	V
LDO Saturation Dropout Voltage (PVCC pin)	$V_{DROPOUT}$	V_{IN} = 4.9V, C_{PVCC} = 4.7µF, I_PVCC = 80mA		0.3		V
LDO Current Limit (PVCC pin)	I_{OC_LDO}	V_{IN} = 6V, V_{PVCC} = 4.5V	**130**	195	**250**	mA
LDO Output Short Current Limit (PVCC pin)	I_{OCFB_LDO}	V_{IN} = 6V, V_{PVCC} = 0V	**50**	100	**160**	mA

Electrical Specifications

Refer to Figure 3 on page 7 and Typical Application Schematics (page 8). Operating conditions unless otherwise noted: V_{IN} = 12V, V_{PVCC} = 5.2V, and V_{VCC} = 5.2V, T_A = -40°C to +125°C (Note 8). Typical values are at T_A = +25°C.
Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
POWER-ON RESET (For both PVCC and VCC)						
Rising V_{VCC} POR Threshold	V_{PORH_VCC}		**4.35**	4.50	**4.75**	V
Falling V_{VCC} POR Threshold	V_{PORL_VCC}		**4.05**	4.15	**4.25**	V
V_{VCC} POR Hysteresis	V_{PORHYS_VCC}			0.4		V
Rising V_{PVCC} POR Threshold	V_{PORH_PVCC}		**4.35**	4.50	**4.75**	V
Falling V_{PVCC} POR Threshold	V_{PORL_PVCC}		**3.0**	3.2	**3.4**	V
V_{PVCC} POR Hysteresis	V_{PORHYS_PVCC}			1.3		V
Soft-Start Delay	t_{SS_DLY}	From POR rising to initiation of soft-start. R_{FSYNC} = 61.9k, f_{SW} = 200kHz, PLLCOMP pin network of R_{PLL} = 3.24k, C_{PLL1} = 6.8nF and C_{PLL2} = 1nF		0.85		ms
EN						
Enable Threshold	V_{ENH}	EN rising	**1.13**	1.21	**1.33**	V
	V_{ENL}	EN falling	**0.85**	0.95	**1.10**	V
	V_{EN_HYS}	Hysteresis		250		mV
Input Impedance		EN = 4V	**2**	6		MΩ
PWM SWITCHING FREQUENCY						
PWM Switching Frequency (per phase)	F_{OSC}	R_{FSYNC} = 249kΩ (0.1%)	**46.0**	50.2	**54.5**	kHz
		R_{FSYNC} = 82.5kΩ (0.1%)	**142**	150	**156**	kHz
		R_{FSYNC} = 40.2kΩ (0.1%)	**290**	300	**310**	kHz
		R_{FSYNC} = 10kΩ (0.1%)	**990**	1100	**1170**	kHz
Minimum Adjustable Switching Frequency				50		kHz
Maximum Adjustable Switching Frequency				1100		kHz
FSYNC Pin Voltage				0.5		V
Minimum ON-Time (Blanking Time) on LGx	t_{MINON_1}	Minimum duty cycle, C_{UG} = C_{LG} = OPEN R_{BLANK} = 80kΩ (0.1%)	**315**	410	**525**	ns
	t_{MINON_2}	Minimum duty cycle, C_{UG} = C_{LG} = OPEN R_{BLANK} = 50kΩ (0.1%)	**175**	260	**325**	ns
	t_{MINON_3}	Minimum duty cycle, C_{UG} = C_{LG} = OPEN R_{BLANK} = 25kΩ (0.1%)	**100**	140	**180**	ns
	t_{MINON_4}	Minimum duty cycle, C_{UG} = C_{LG} = OPEN R_{BLANK} = 10k	**75**	90	**105**	ns
Maximum Duty Cycle	D_{MAX}	D_{MAX} = T_LG_ ON/t_{SW}, V_{COMP} = 3.5V, f_{SW} = 300kHz, R_{DT} = 18.2kΩ, C_{UG} = OPEN, C_{LG} = OPEN	**88.5**	89.0	**90.5**	%
SYNCHRONIZATION (FSYNC Pin)						
Minimum Synchronization Frequency at FSYNC Input				50		kHz
Maximum Synchronization Frequency at FSYNC Input				1100		kHz
Input High Threshold	V_{IH}		**3.5**			V
Input Low Threshold	V_{IL}				**1.5**	V

Electrical Specifications

Refer to Figure 3 on page 7 and Typical Application Schematics (page 8). Operating conditions unless otherwise noted: V_{IN} = 12V, V_{PVCC} = 5.2V, and V_{VCC} = 5.2V, T_A = -40°C to +125°C (Note 8). Typical values are at T_A = +25°C.
Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
Input Minimum Pulse Width - Rise-to-Fall			**20**			ns
Input Minimum Pulse Width - Fall-to-Rise			**20**			ns
Delay Time from Input Pulse Rising to LG1 Rising Edge Minus Dead Time t_{DT1}		C_{LG} = OPEN, R_{DT} = 50kΩ		35		ns
Input Impedance		Input impedance before synchronization mode		1		kΩ
		Input impedance after synchronization mode		200		MΩ
CLKOUT						
$CLKOUT_H$		I_{CLKOUT} = 500µA	**V_{CC} -0.5**	V_{CC} - 0.1		V
$CLKOUT_L$		I_{CLKOUT} = -500µA		0.1	**0.4**	V
Output Pulse Width		C_{CLKOUT} = 100pF, t_{SW} is each phase's switching period		1/12 * t_{SW}		
Phase Shift from LG1 Rising Edge to CLKOUT Pulse Rising Edge		C_{LG1} = OPEN, C_{CLKOUT} = OPEN, f_{SW} = 300kHz, t_{DT1} = 60ns (refer to Figure 65 on page 29 for the timing diagram)		87		°
SOFT-START						
Soft-Start Current	I_{SS}		**4.5**	5.0	**5.5**	µA
Minimum Soft-Start Prebias Voltage				0		V
Maximum Soft-Start Prebias Voltage				1.6		V
Soft-Start Prebias Voltage Accuracy		V_{FB} = 500mV	**-25**	0	**25**	mV
Soft-Start Clamp Voltage	$V_{SSCLAMP}$		**3.25**	3.47	**3.70**	V
HICCUP RETRY DELAY (Refer to "Fault Response Register SET_FAULT_RESPONSE (D2h)" on page 35 for more details)						
Hiccup Retry Delay		If Hiccup fault response selected		500		ms
REFERENCE VOLTAGE FOR OUTPUT VOLTAGE REGULATION						
System Reference Accuracy		Measured at the FB pin	**1.576**	1.600	**1.620**	V
FB Pin Input Bias Current		V_{FB} = 1.6V, TRACK = Open	**-0.05**	0.01	**0.05**	µA
ERROR AMPLIFIER FOR OUTPUT VOLTAGE REGULATION (Gm1)						
Transconductance Gain				2		mA/V
Output Impedance				7.5		MΩ
Unity Gain Bandwidth		C_{COMP} = 100pF from COMP pin to GND		3.3		MHz
Slew Rate		C_{COMP} = 100pF from COMP pin to GND		±3		V/µs
Output Current Capability				±300		µA
Maximum Output Voltage			**3.5**	3.7		V
Minimum Output Voltage				0.1	**0.3**	V
PWM CORE						
SLOPE Pin Voltage			**480**	500	**520**	mV
SLOPE Accuracy		R_{SLOPE} = 20k (0.1%)	**-20**	0	**20**	%
		R_{SLOPE} = 40.2k (0.1%)	**-20**	3	**20**	%

Electrical Specifications

Refer to Figure 3 on page 7 and Typical Application Schematics (page 8). Operating conditions unless otherwise noted: V_{IN} = 12V, V_{PVCC} = 5.2V, and V_{VCC} = 5.2V, T_A = -40°C to +125°C (Note 8). Typical values are at T_A = +25°C.
Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
Duty Cycle Matching		V_{RSENx} = 30mV, R_{SETx} = 665Ω (0.1%), R_{SLOPE} = 27k, f_{SW} = 150kHz, V_{COMP} = 2.52V, Measure $(T_{ON\_LG2} - T_{ON\_LG1})/(T_{ON\_LG2} + T_{ON\_LG1})*2$		3		%
CURRENT SENSE AMPLIFIER						
Minimum ISENxN and ISENxP Common-Mode Voltage Range		Accuracy becomes worse when lower than 4V		4		V
Maximum ISENxN and ISENxP Common-Mode Voltage Range				55		V
Maximum Input Differential Voltage Range	$V_{ISENxP} - V_{ISENxN}$			±0.3		V
ISENxP/ISENxN Bias Current	I_{SENxP/N_BIAS}	Sourcing out of pin, EN = 5V, $V_{ISENxN} = V_{ISENxP}$, V_{CM} = 4V to 55V	**100**	123	**150**	µA
ZCD DETECTION - CSA						
Zero Crossing Detection (ZCD) Threshold	V_{ZCD_CSA}	Measures voltage threshold before R_{SEN} at CSA inputs (equivalent to the voltage across the current sense shunt resistor), R_{SET} = 665Ω (0.1%)	**-4.0**	1.3	**6.0**	mV
PHASE DROPPING						
V_{IMON} Phase-Drop Falling Threshold, to Drop Phase 2	$V_{PHDRP\_TH\_F}$	When V_{IMON} falls below $V_{PHDRP\_TH\_F}$, drop off Phase 2	**1.0**	1.1	**1.2**	V
V_{IMON} Phase-Add Rising Threshold, to Add Phase 2	$V_{PHADD\_TH\_R}$	When V_{IMON} rise above $V_{PHADD\_TH\_R}$, add back Phase 2	**1.05**	1.15	**1.25**	V
V_{IMON} Phase-Drop Threshold Hysteresis	V_{PHDRP_HYS}	When $V_{IMON} < V_{PHDRP\_TH\_F} - V_{PHDrop\_HYS}$, Add back Phase 2	**45**	50	**55**	mV
PEAK OVERCURRENT CYCLE-BY-CYCLE LIMITNG (OC1)						
Peak Current Cycle-by-Cycle Limit Threshold for Individual Phase	V_{OC1}	Cycle-by-cycle current limit threshold (I_{OC1_TH} = 80µA, compared with I_{SENx}). Measures the voltage threshold before R_{SETx} at CSA Inputs (equivalent to the voltage across the current sense shunt resistor), R_{SETx} = 665Ω (0.1%)	**40**	53	**65**	mV
Peak Current Cycle-by-Cycle Limit Trip Delay		C_{LG} = OPEN, from the time V_{OC1} tripped to LG falling		50		ns
PEAK OVERCURRENT FAULT PROTECTION (OC2) (Refer to "Peak Overcurrent Fault (OC2_PEAK)" on page 37 for more details)						
Peak Current Fault Protection Threshold for Individual Phase	V_{OC2}	Peak current hiccup protection threshold (I_{OC2_TH} = 105µA, compared with I_{SENx}). Measures the voltage threshold before R_{SETx} at CSA Inputs (equivalent to the voltage across the current sense shunt resistor), R_{SETx} = 665Ω (0.1%)	**55**	70	**85**	mV
OC2 Trip Blanking Time				3		cycles
NEGATIVE CURRENT CYCLE-BY-CYCLE LIMITNG (OC_NEG)						
Negative Current Cycle-by-Cycle Limit Threshold for Individual Phase	V_{OC_NEG}	Negative Current Cycle-by-Cycle Limit ($I_{OC\_NEG\_TH}$ = -48µA, compared with I_{SENx}). Measures the voltage threshold before R_{SETx} at CSA Inputs (equivalent to the voltage across the current sense shunt resistor), R_{SET} = 665Ω (0.1%)		-32		mV

Electrical Specifications

Refer to Figure 3 on page 7 and Typical Application Schematics (page 8). Operating conditions unless otherwise noted: V_{IN} = 12V, V_{PVCC} = 5.2V, and V_{VCC} = 5.2V, T_A = -40°C to +125°C (Note 8). Typical values are at T_A = +25°C.
Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
AVERAGE CONSTANT CURRENT CONTROL LOOP						
IMON Current Accuracy		V_{RSENx} = 30mV, R_{SETx} = 665Ω (0.1%), with ISENxP/N pins biased at 4V or 55V common-mode voltage	**27.0**	28.3	**29.5**	µA
IMON Offset Current		V_{RSENx} = 0V, R_{SET} = 665Ω (0.1%), with ISENxP/N pins biased at 4V or 55V common-mode voltage	**16**	17	**18**	µA
Constant Current Control Reference Accuracy	$VREF_{CC}$	Measure the IMON pin	**1.575**	1.600	**1.625**	V
AVERAGE OVERCURRENT FAULT PROTECTION (OC_AVG) (Refer to "Average Overcurrent Fault (OC_AVG)" on page 38 for more details)						
OC_AVG Fault Threshold at the IMON Pin			**1.9**	2.0	**2.1**	V
OC_AVG Fault Trip Delay				1		µs
GATE DRIVERS						
UG Source Resistance	R_{UG_SOURCE}	100mA source current, V_{BOOT} - V_{PH} = 4.4V		1.2		Ω
UG Source Current	I_{UG_SOURCE}	V_{UG} - V_{PH} = 2.5V, V_{BOOT} - V_{PH} = 4.4V		2		A
UG Sink Resistance	R_{UG_SINK}	100mA sink current, V_{BOOT} - V_{PH} = 4.4V		0.6		Ω
UG Sink Current	I_{UG_SINK}	V_{UG} - V_{PH} = 2.5V, V_{BOOT} - V_{PH} = 4.4V		2.0		A
LG Source Resistance	R_{LG_SOURCE}	100mA source current, PVCC = 5.2V		1.2		Ω
LG Source Current	I_{LG_SOURCE}	V_{LG} - PGND = 2.5V, PVCC = 5.2V		2.0		A
LG Sink Resistance	R_{LG_SINK}	100mA sink current, PVCC = 5.2V		0.55		Ω
LG Sink Current	I_{LG_SINK}	V_{LG} - PGND = 2.5V, PVCC = 5.2V		3		A
UG to PH Internal Resistor				50		kΩ
LG to PGND Internal Resistor				50		kΩ
BOOT-PH UVLO Detection Threshold			**2.8**	3.0	**3.2**	V
BOOT-PH UVLO Detection Threshold Hysteresis			**0.09**	0.15	**0.22**	V
Dead Time Delay - UG Falling to LG Rising	t_{DT1}	C_{UG} = C_{LG} = OPEN, R_{DT} = 10k (0.1%)	**55**	70	**85**	ns
Dead Time Delay - LG Falling to UG Rising	t_{DT2}	C_{UG} = C_{LG} = OPEN, R_{DT} = 10k (0.1%)	**65**	80	**95**	ns
Dead Time Delay - UG Falling to LG Rising	t_{DT1}	C_{UG} = C_{LG} = OPEN, R_{DT} = 18.2kΩ (0.1%)	**85**	100	**115**	ns
Dead Time Delay - LG Falling to UG Rising	t_{DT2}	C_{UG} = C_{LG} = OPEN, R_{DT} = 18.2kΩ (0.1%)	**95**	110	**125**	ns
Dead Time Delay - UG Falling to LG Rising	t_{DT1}	C_{UG} = C_{LG} = OPEN, R_{DT} = 50kΩ (0.1%)	**185**	210	**240**	ns
Dead Time Delay - LG Falling to UG Rising	t_{DT2}	C_{UG} = C_{LG} = OPEN, R_{DT} = 50kΩ (0.1%)	**205**	230	**260**	ns
Dead Time Delay - UG Falling to LG Rising	t_{DT1}	C_{UG} = C_{LG} = OPEN, R_{DT} = 64.9kΩ (0.1%)	**235**	265	**295**	ns
Dead Time Delay - LG Falling to UG Rising	t_{DT2}	C_{UG} = C_{LG} = OPEN, R_{DT} = 64.9kΩ (0.1%)	**260**	290	**320**	ns
OUTPUT OVERVOLTAGE DETECTION/PROTECTION (Monitors the FB Pin, refer to "Output Overvoltage Fault" on page 36 for more details)						
FB Overvoltage Rising Trip Threshold	V_{FBOV_RISE}	Percentage of VDAC output reference (default V_{REF} = 1.6V) Selectable hiccup/latch-off response.	**118**	120	**122**	%
FB Overvoltage Falling Recovery Threshold	V_{FBOV_FALL}	Percentage of VDAC output reference (default V_{REF} = 1.6V) Selectable hiccup/latch-off response.	**114**	116	**118**	%

Electrical Specifications

Refer to Figure 3 on page 7 and Typical Application Schematics (page 8). Operating conditions unless otherwise noted: V_{IN} = 12V, V_{PVCC} = 5.2V, and V_{VCC} = 5.2V, T_A = -40°C to +125°C (Note 8). Typical values are at T_A = +25°C.
Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
Overvoltage Threshold Hysteresis				4		%
FB Overvoltage Trip Delay				1		us
OUTPUT UNDERVOLTAGE DETECTION (Monitor the FB Pin, refer to "Output Undervoltage Fault" on page 36 for more details)						
Undervoltage Falling Trip Threshold	$V_{FBUVREF\_FALL}$	Percentage of VDAC output reference (default V_{REF} = 1.6V)	**78**	80	**82**	%
Undervoltage Rising Recovery Threshold	$V_{FBUVREF\_RISE}$	Percentage of VDAC output reference (default V_{REF} = 1.6V)	**82.5**	84.0	**86.5**	%
Undervoltage Threshold Hysteresis				4		%
POWER-GOOD MONITOR (PGOOD Pin)						
PGOOD Leakage Current		PGOOD HIGH, V_{PGOOD} = 5V			**1**	µA
PGOOD Low Voltage		PGOOD LOW, I_{PGOOD} = 0.5mA		0.06	**0.4**	V
PGOOD Rising Delay (DE mode)		The PGOOD rising delay from V_{SSPIN} = $V_{SSPCLAMP}$ (3.47V) and VREF_TRK ≥0.3V to PGOOD HIGH when DE mode is selected (DE/PHDRP = VCC or FLOAT)		0.5		ms
PGOOD Rising Delay (CCM mode)		The PGOOD rising delay from V_{SSPIN} = $V_{SSPCLAMP}$ (3.47V) and VREF_TRK ≥0.3V to PGOOD HIGH when CCM mode is selected (DE/PHDRP = GND)		100		ms
PGOOD Falling Blanking Time				10		µs
ADDR1, ADDR2, HIC/LATCH, ATRK/DTRK PIN DIGITAL LOGIC INPUT						
Input Leakage Current		EN <1V	**-1**		**1**	µA
Input Pull-Down Current		EN >2V, pin voltage = 2.1V	**0.7**	1.0	**2.0**	µA
Logic Input Low					**0.8**	V
Logic Input High			**2.1**			V
DE/PHDRP PIN DIGITAL LOGIC INPUT (HIGH/LOW/FLOAT)						
Input Leakage Current			-1		1	µA
Float Impedance - Pin to VCC		Pin = GND	**100**	200	**300**	kΩ
Float Impedance - Pin to GND		Pin = VCC	**100**	200	**300**	kΩ
Output Voltage on Float Pin		Pin = FLOAT	**2.1**	2.6	**2.7**	V
Tri-State Input Voltage MAX					3	V
Tri-State Input Voltage MIN			**1.8**			V
Logic Input Low		Pin voltage falling			**0.7**	V
Logic Input High		Pin voltage rising	**V_{CC} -0.4**			V
TRACK PIN - DIGITAL INPUT LOGIC						
Input Leakage Current		EN <1V, pin voltage = 5V, V_{CC} = 0V	**-1**		**1**	µA
Input Pull-Up Current		EN >2V, pin voltage = 0V, V_{CC} = 5V	**0.8**	1.1	**1.5**	µA
Input Pull-Up Current Compliance Voltage		EN >2V, pin open		2.5		V
Logic Input Low		Pin voltage falling			**0.8**	V
Logic Input High		Pin voltage rising	2			V

Electrical Specifications

Refer to Figure 3 on page 7 and Typical Application Schematics (page 8). Operating conditions unless otherwise noted: V_{IN} = 12V, V_{PVCC} = 5.2V, and V_{VCC} = 5.2V, T_A = -40°C to +125°C (Note 8). Typical values are at T_A = +25°C.
Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
Duty Cycle Conversion (FB accuracy)		0% duty cycle input, measure at the FB pin		0		V
		25% duty cycle input, frequency = 400kHz, measure at the FB pin	**0.600**	0.625	**0.650**	V
		50% duty cycle input, frequency = 400kHz, measure at the FB pin	**1.218**	1.253	**1.288**	V
		60% duty cycle input, measure at the FB pin	**1.45**	1.49	**1.53**	V
TRACK PIN - ANALOG INPUT						
Input Leakage Current		V_{TRACK} = 1.6V, leakage current into this pin to ground	**-1.0**	-0.6	**-0.3**	µA
TRACK Input Reference Voltage Range		VREF_DAC = 1.6V	0		**1.6**	V
TRACK Input Reference Voltage Accuracy		Measure at the FB pin, V_{TRACK} = 1.5V	**-4.0**	-0.5	**4.0**	%
		Measure at the FB pin, V_{TRACK} = 0.5V	**-6.0**	1.8	**6.0**	%
TRACK SS_DONE Detection Threshold			**0.29**	0.30	**0.31**	V
PMBus INTERFACE (SCL and SDA INPUT PINS)						
Logic Input Voltage High			**2.1**			V
Logic Input Voltage Low					**0.8**	V
Hysteresis				0.55		V
SDA Output Voltage Low		I_{OUT} = -3mA		0.1	**0.4**	V
Input Current				1	**2**	µA
Input Capacitance				5		pF
Clock Frequency					**400**	kHz
SCL Falling Edge to SDA Valid Time					**1**	µs
SALERT PIN OUTPUT						
Output Voltage Low		I_{OUT} = -3mA		0.1	**0.4**	V
Output High Leakage Current		V_{SALERT} = 5.2V		0	**1**	µA
NTC PIN						
Input Leakage Current		EN <1V	**-1**	0	**1**	µA
Output Sourcing Current (from Pin to Ground)		EN >2V, pin voltage = 0V	**19**	20	**21**	µA
Output Current Source Compliance Voltage		EN >2V		V_{CC}		V
Default NTC Warning Threshold		NTC pin voltage falling		450		mV
Default NTC Fault Protection Threshold		NTC pin voltage falling		300		mV
INTERNAL 8-BIT DAC						
Minimum Output Voltage		LSB = 8mV		8		mV
Maximum Output Voltage		LSB = 8mV		2.048		V
INTERNAL 10-BIT ADC (ALTERNATIVELY SAMPLING VOLTAGES OF NTC, FB, VIN/48 AND IMON PINS)						
Minimum Input Voltage		LSB = 2mV		2		mV
Maximum Input Voltage		LSB = 2mV		2.048		V

Electrical Specifications

Refer to Figure 3 on page 7 and Typical Application Schematics (page 8). Operating conditions unless otherwise noted: V_{IN} = 12V, V_{PVCC} = 5.2V, and V_{VCC} = 5.2V, T_A = -40°C to +125°C (Note 8). Typical values are at T_A = +25°C.

Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
OVER-TEMPERATURE PROTECTION						
Over-Temperature Trip Point				160		°C
Over-Temperature Recovery Threshold				145		°C

NOTES:

7. Compliance to datasheet limits are assured by one or more methods: production test, characterization, and/or design.
8. The IC is tested in conditions with minimum power dissipations in the IC, meaning $T_A \approx T_J$.

Performance Curves

Unless otherwise specified, operating conditions for the oscilloscope waveforms are V_{IN} = 12V, V_{OUT} = 36V and T_A = +25°C.

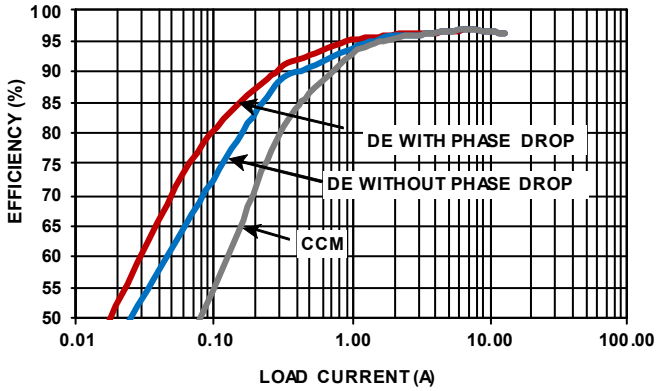


FIGURE 5. EFFICIENCY vs LOAD, 2-PHASE BOOST, 3 MODES OPERATION, f_{SW} = 200kHz, V_{IN} = 12V, V_{OUT} = 36V, T_A = +25°C

NOTE: (See Typical Application in Figure 4 on page 8.)

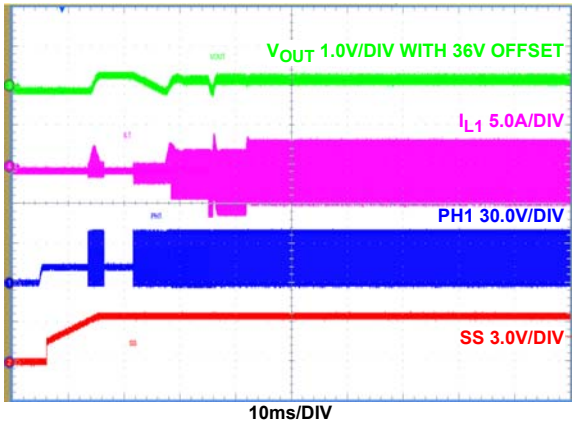


FIGURE 6. EN INTO PREBIASED OUTPUT, CCM MODE (DE/PHDRP = GND), I_{OUT} = 0A

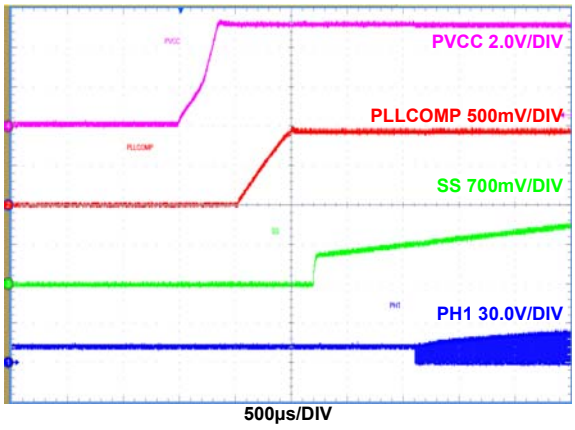


FIGURE 7. EN ON AND INITIALIZATION TO START-UP, I_{OUT} = 0A

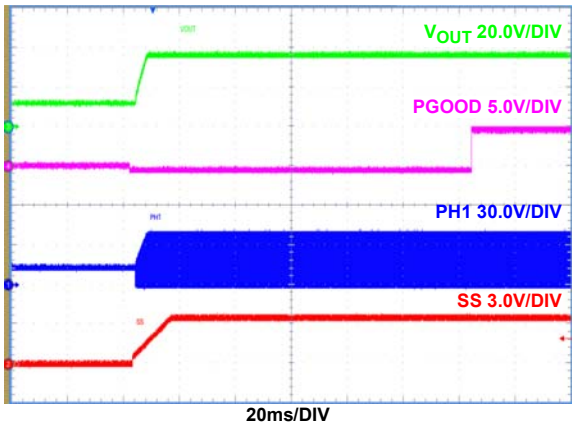


FIGURE 8. SOFT-START, CCM MODE (DE/PHDRP = GND), I_{OUT} = 8A

Performance Curves

Unless otherwise specified, operating conditions for the oscilloscope waveforms are V_{IN} = 12V, V_{OUT} = 36V and T_A = +25°C. **(Continued)**

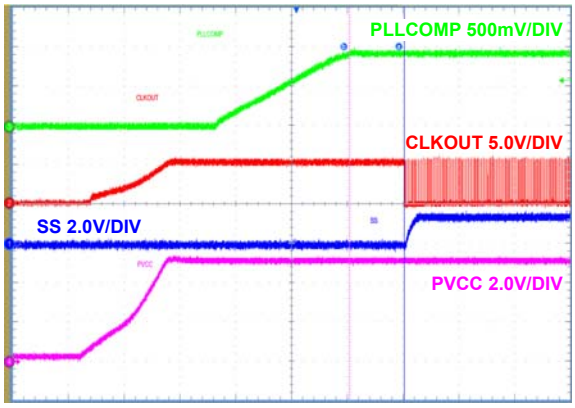


FIGURE 9. EN ON AND INITIALIZATION TO START-UP, I_{OUT} = 0A

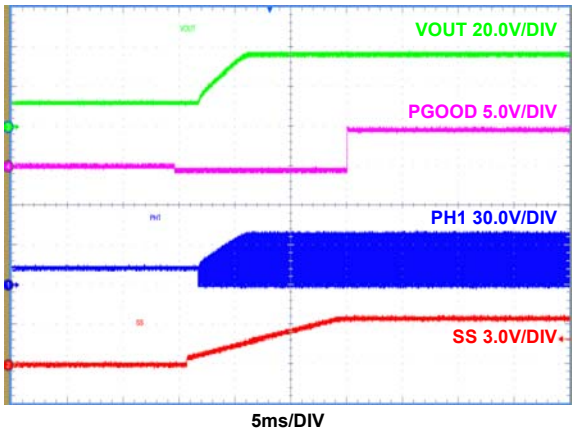


FIGURE 10. SOFT-START, DE+PHDROP MODE (DE/PHDRP = FLOAT), I_{OUT} = 8A

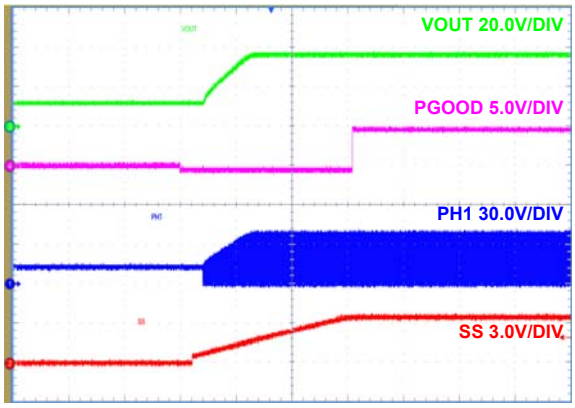


FIGURE 11. SOFT-START, DE MODE (DE/PHDRP = V_{CC}), I_{OUT} = 8A

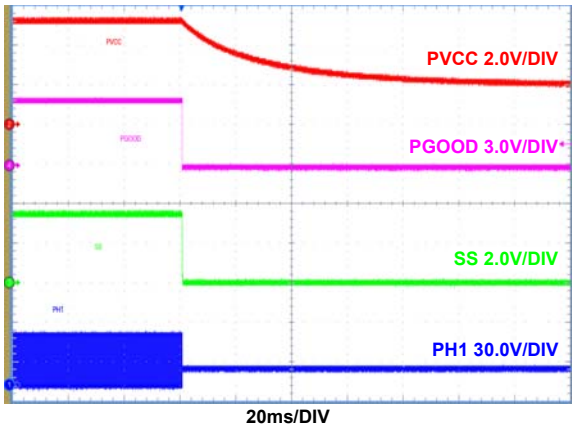


FIGURE 12. EN SHUTDOWN, PVCC/PGOOD/SS FALL, I_{OUT} = 0A

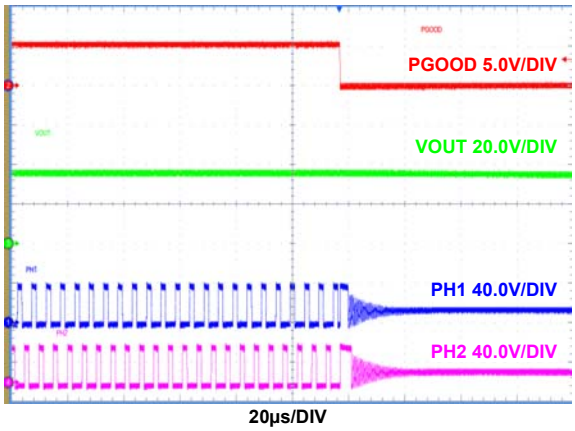


FIGURE 13. EN SHUTDOWN, I_{OUT} = 8A

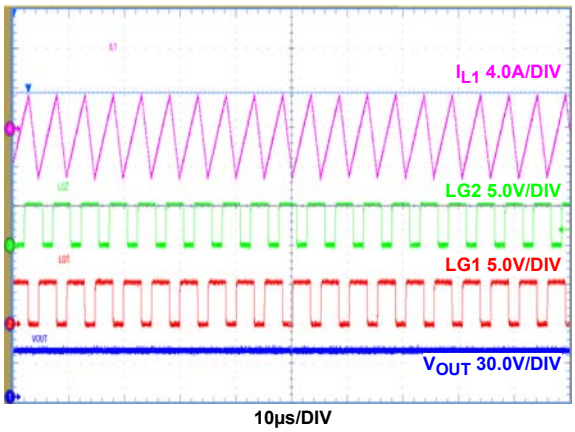


FIGURE 14. CCM MODE (DE/PHDRP = GND), PHASE 1 INDUCTOR RIPPLE CURRENT, I_{OUT} = 0A

Performance Curves

Unless otherwise specified, operating conditions for the oscilloscope waveforms are V_{IN} = 12V, V_{OUT} = 36V and T_A = +25°C. **(Continued)**

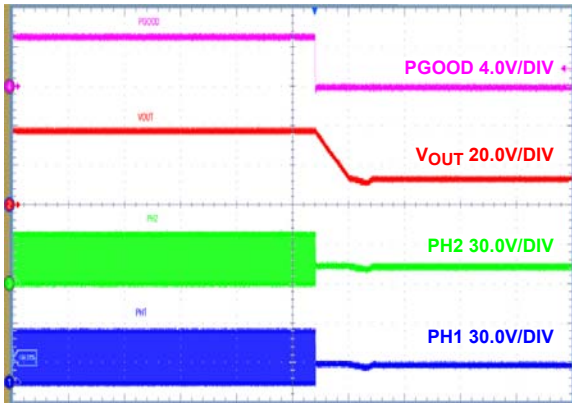


FIGURE 15. EN SHUTDOWN, I_{OUT} = 8A

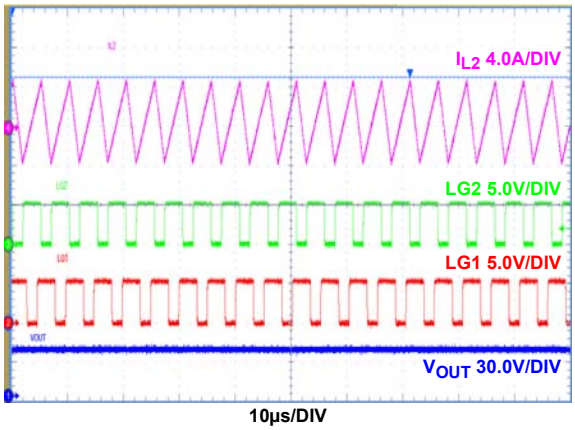


FIGURE 16. CCM MODE (DE/PHDRP = GND), PHASE 2 INDUCTOR RIPPLE CURRENT, I_{OUT} = 0A

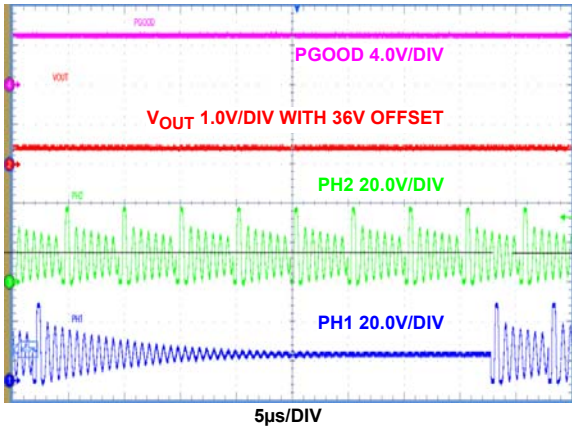


FIGURE 17. DE MODE (DE/PHDRP = V_{CC}), DIODE EMULATION OPERATION, PULSE SKIPPING, I_{OUT} = 0A

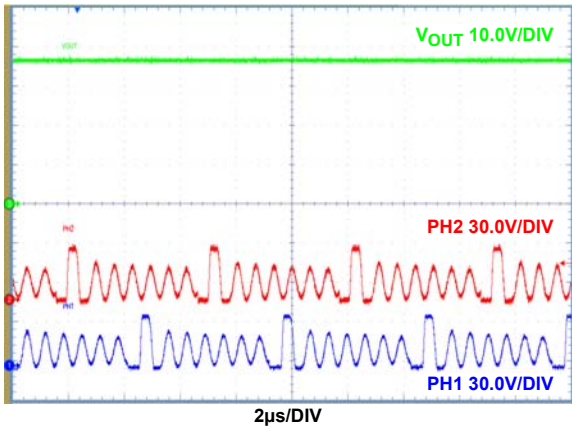


FIGURE 18. DE MODE (DE/PHDRP = V_{CC}), DIODE EMULATION OPERATION, I_{OUT} = 29mA

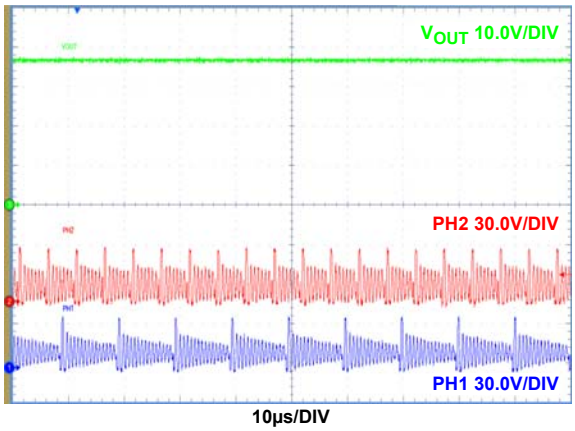


FIGURE 19. DE MODE (DE/PHDRP = V_{CC}), PH1 AND PH2 DIODE EMULATION OPERATION, PULSE SKIPPING, I_{OUT} = 7mA

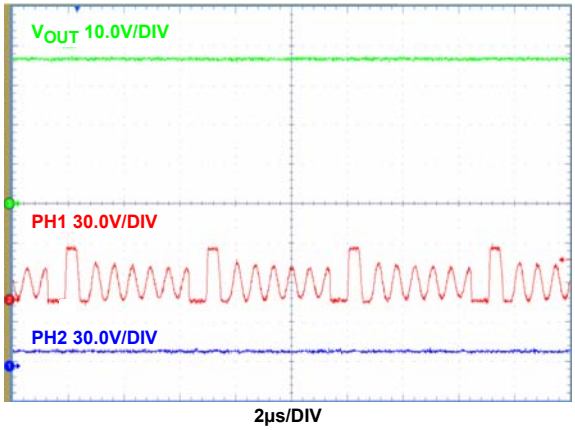


FIGURE 20. DE+PH_DROP MODE (DE/PHDRP = FLOAT), PH1 DIODE EMULATION WITH PH2 DROPPED, I_{OUT} = 29mA

Performance Curves

Unless otherwise specified, operating conditions for the oscilloscope waveforms are V_{IN} = 12V, V_{OUT} = 36V and T_A = +25°C. **(Continued)**

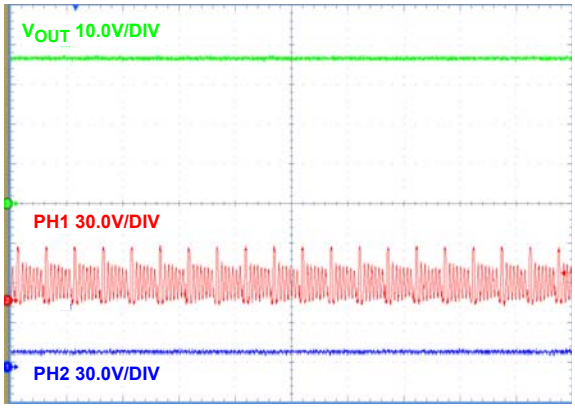


FIGURE 21. DE+PHDRP MODE (DE/PHDRP = FLOAT), PH1 DIODE EMULATION WITH PH2 DROPPED, I_{OUT} = 7mA

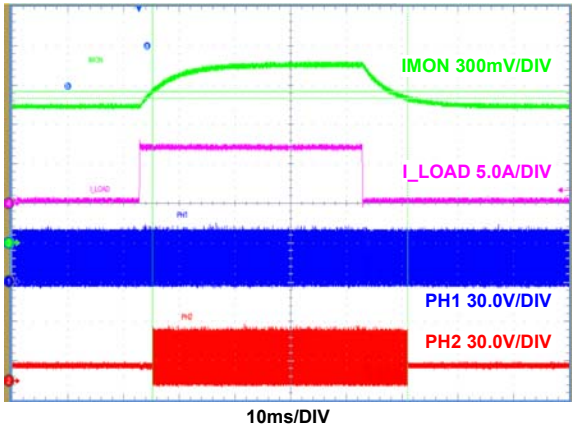


FIGURE 22. DE+PHDRP MODE (DE/PHDRP = FLOAT), PH2 ADDED AND DROPPED, UNDER TRANSIENT STEP LOAD OF 1A TO 8A

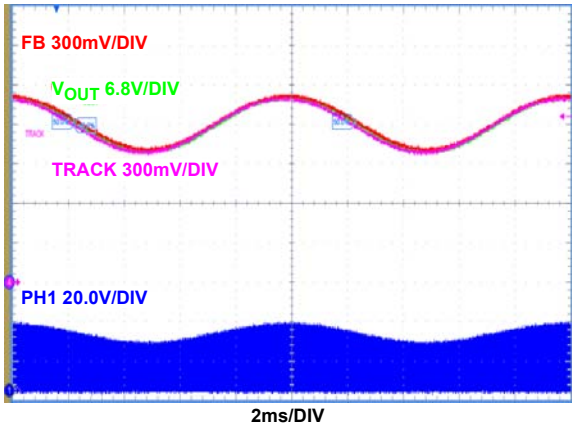


FIGURE 23. ANALOG TRACKING 100Hz SINUSOIDAL SIGNAL, CCM MODE (DE/PHDRP = GND), ATRK/DTRAK = V_{CC}, I_{OUT} = 1A

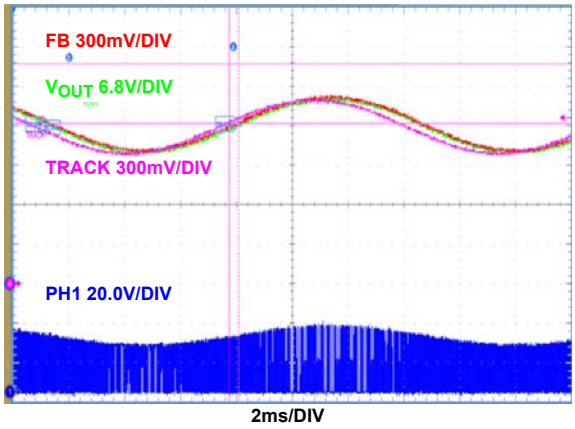


FIGURE 24. ANALOG TRACKING 300Hz SINUSOIDAL SIGNAL AT THE TRACK PIN, CCM MODE (DE/PHDRP = GND), ATRK/DTRAK = V_{CC}, I_{OUT} = 1A

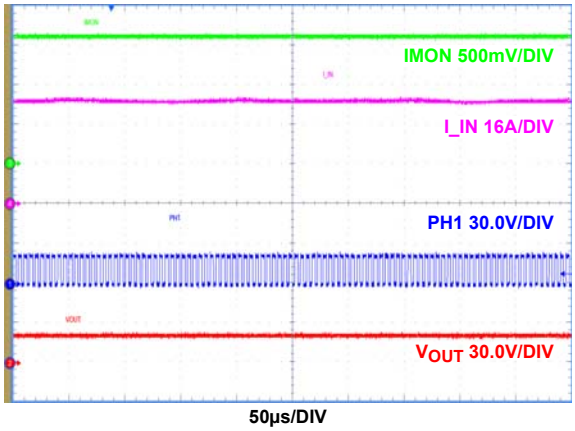


FIGURE 25. STEADY-STATE OPERATION OF INPUT CONSTANT CURRENT MODE, I_{IN} CONTROLLED AT 43A CONSTANT, V_{OUT} = 19.5V

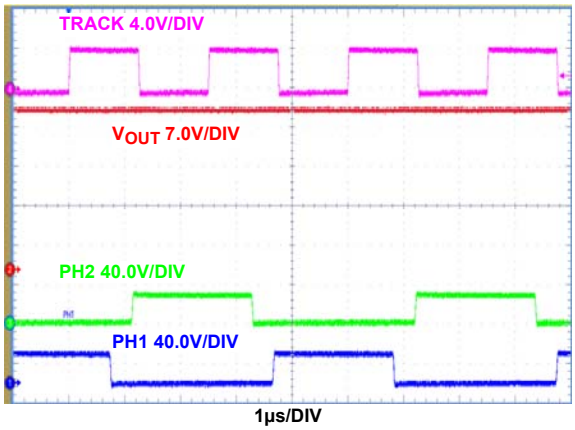


FIGURE 26. DIGITAL TRACKING (TRACKING SIGNAL, FREQUENCY = 400kHz, D_TRACK = 0.5), V_{OUT} = 28.3V

Performance Curves

Unless otherwise specified, operating conditions for the oscilloscope waveforms are V_{IN} = 12V, V_{OUT} = 36V and T_A = +25°C. **(Continued)**

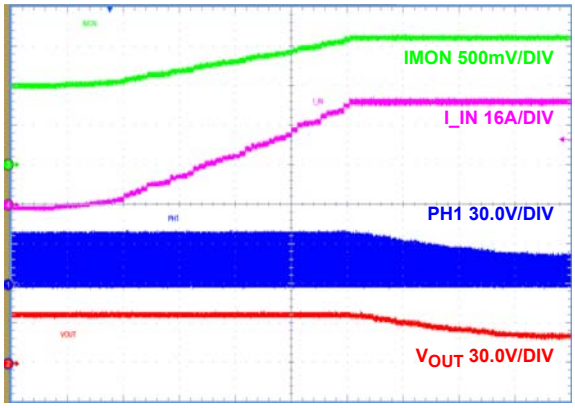


FIGURE 27. LOAD CURRENT KEEP INCREASING FROM NO LOAD TO OVERLOAD (25A), V_{OUT} STARTS TO DROP WHEN INPUT CONSTANT CURRENT MODE STARTS TO WORK, INPUT CURRENT IS FINALLY CONTROLLED TO BE CONSTANT

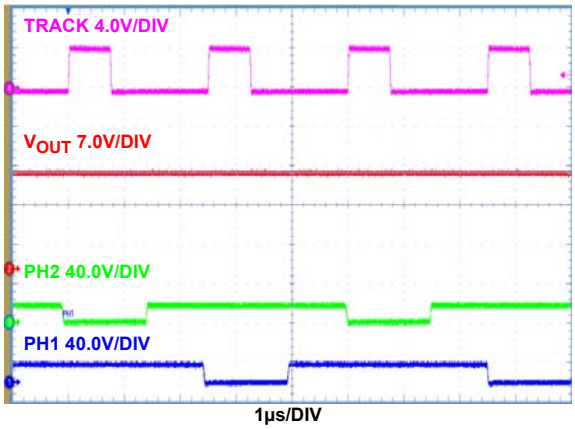


FIGURE 28. DIGITAL TRACKING (TRACKING SIGNAL, FREQUENCY = 400kHz, D_TRACK = 0.3), V_{OUT} = 17V

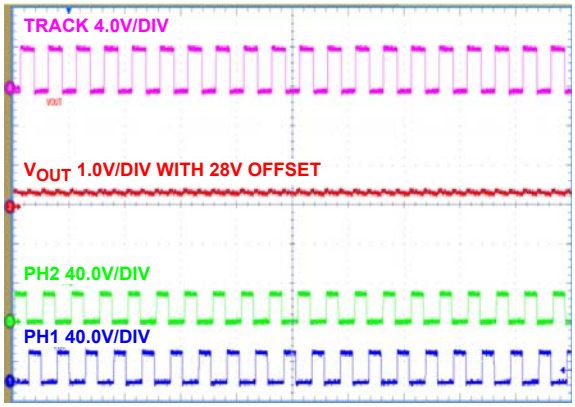


FIGURE 29. DIGITAL TRACKING, (TRACKING SIGNAL, FREQUENCY = 200kHz, D_TRACK = 0.5), V_{OUT} = 28.3V

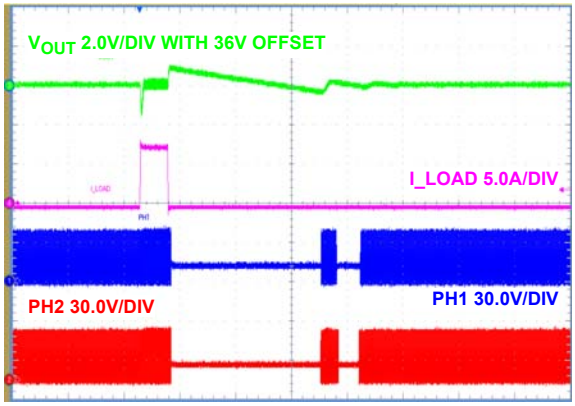


FIGURE 30. DE MODE (DE/PHDRP = V_{CC}), TRANSIENT RESPONSE, I_{OUT} = 0.03 TO 8A STEP LOAD

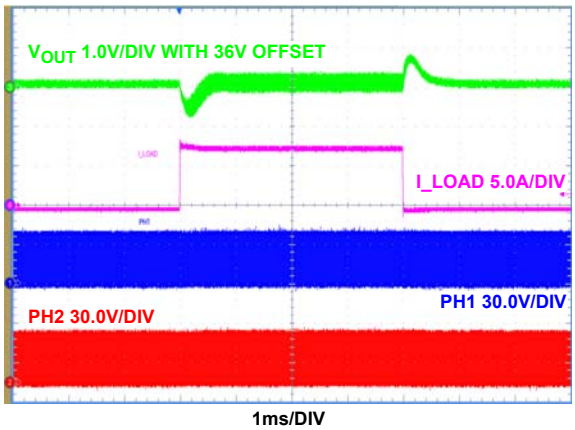


FIGURE 31. CCM MODE (DE/PHDRP = GND), TRANSIENT RESPONSE, I_{OUT} = 0 TO 8A STEP LOAD

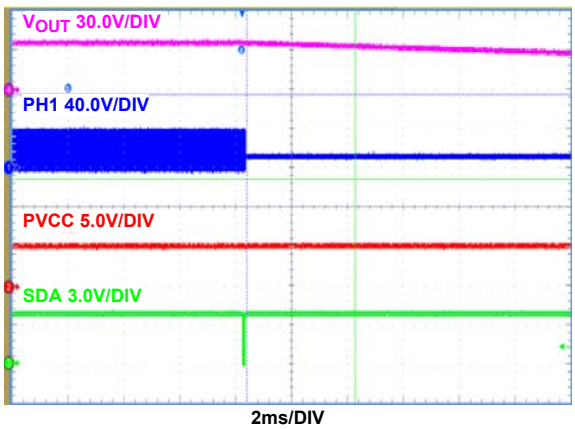


FIGURE 32. SHUTDOWN VIA PMBus COMMAND OPERATION, OFF

Performance Curves

Unless otherwise specified, operating conditions for the oscilloscope waveforms are V_{IN} = 12V, V_{OUT} = 36V and T_A = +25°C. **(Continued)**

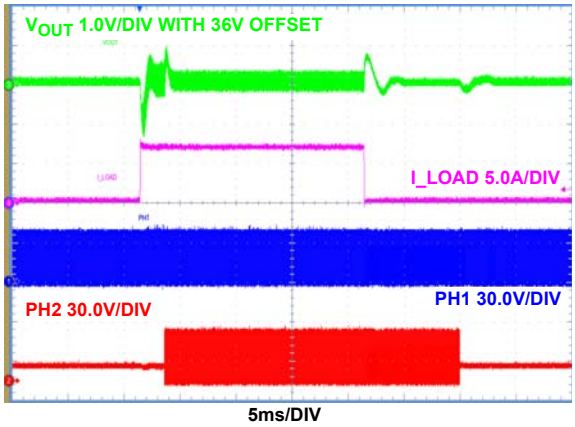


FIGURE 33. DE+PH_DROP MODE (DE/PHDRP = FLOAT), TRANSIENT RESPONSE, I_{OUT} = 1A TO 8A STEP LOAD

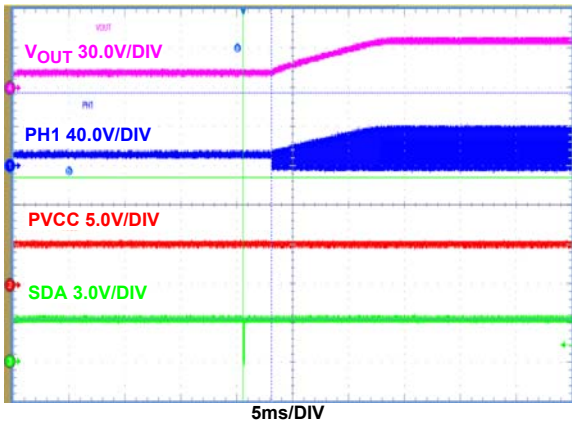


FIGURE 34. ENABLE VIA PMBus COMMAND OPERATION, ON

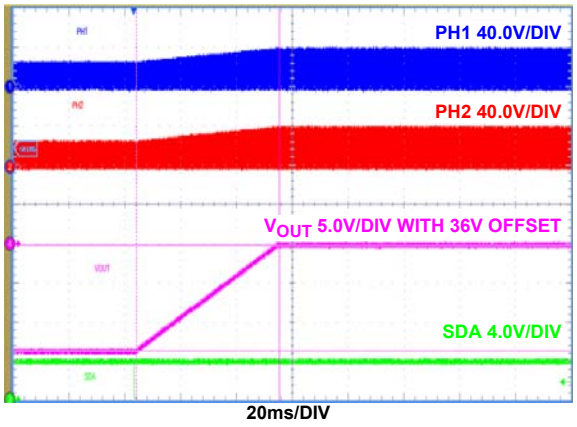


FIGURE 35. PMBus COMMAND VOUT_COMMAND CHANGES VREF_DAC FROM 1V TO 1.6V. VOUT_TRANSITION_RATE SETS VREF_DAC CHANGING SLEW RATE AT 12.5mV/ms

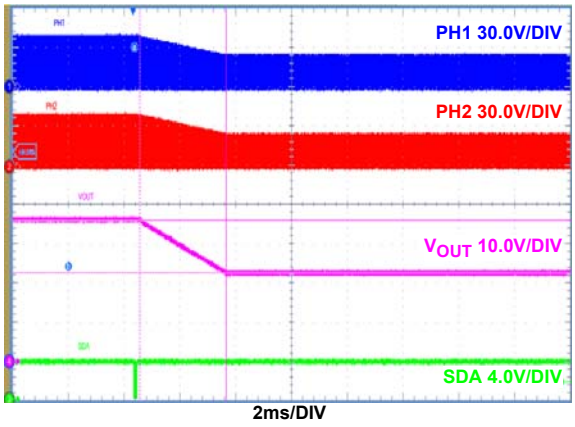


FIGURE 36. PMBus COMMAND VOUT_COMMAND CHANGES VREF_DAC FROM 1.6V TO 1V. VOUT_TRANSITION_RATE SETS VREF_DAC CHANGING SLEW RATE AT 200mV/ms

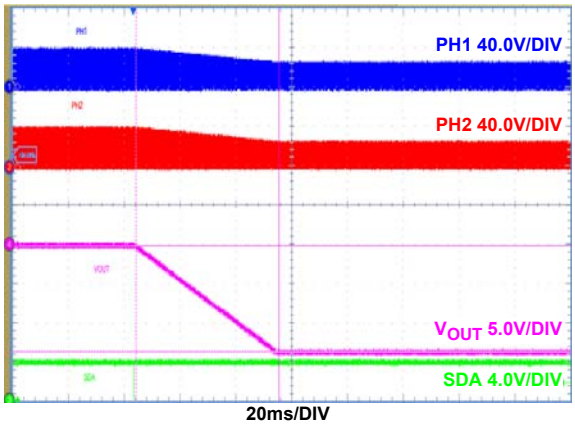


FIGURE 37. PMBus COMMAND VOUT_COMMAND CHANGES VREF_DAC FROM 1.6V TO 1V. VOUT_TRANSITION_RATE SETS VREF_DAC CHANGING SLEW RATE AT 12.5mV/ms

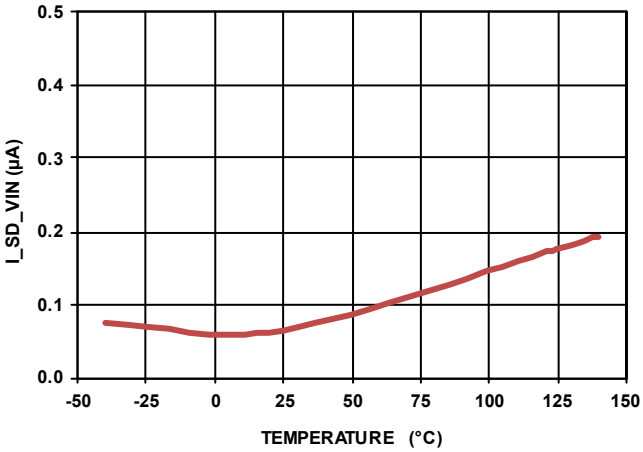


FIGURE 38. SHUTDOWN CURRENT AT THE VIN PIN I_SD vs TEMPERATURE, V_{IN} = 55V

Performance Curves

Unless otherwise specified, operating conditions for the oscilloscope waveforms are V_{IN} = 12V, V_{OUT} = 36V and T_A = +25°C. **(Continued)**

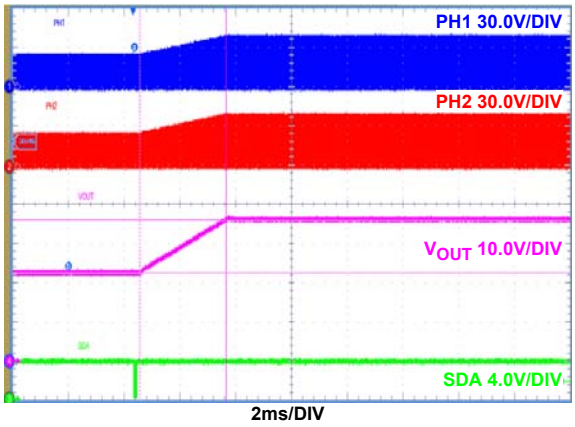


FIGURE 39. PMBus COMMAND VOUT_COMMAND CHANGES VREF_DAC FROM 1V TO 1.6V. VOUT_TRANSITION_RATE SETS VREF_DAC CHANGING SLEW RATE AT 200mV/ms

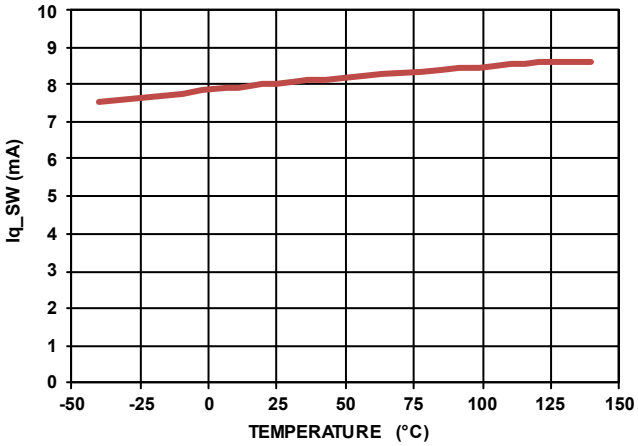


FIGURE 40. IC OPERATIONAL QUIESCENT CURRENT vs TEMPERATURE, IC SWITCHING, NO LOAD ON LGX AND UGX

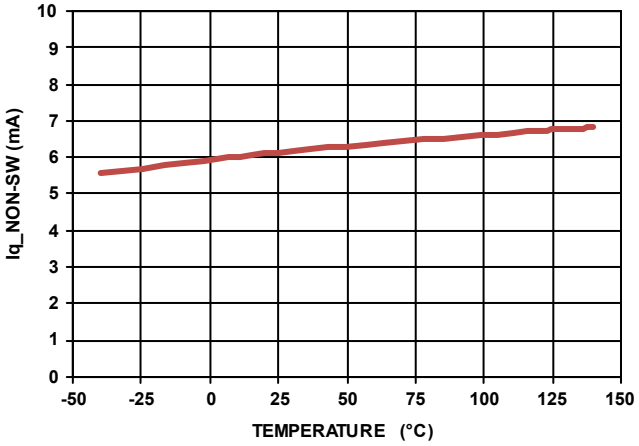


FIGURE 41. IC OPERATIONAL QUIESCENT CURRENT vs TEMPERATURE, IC NOT SWITCHING

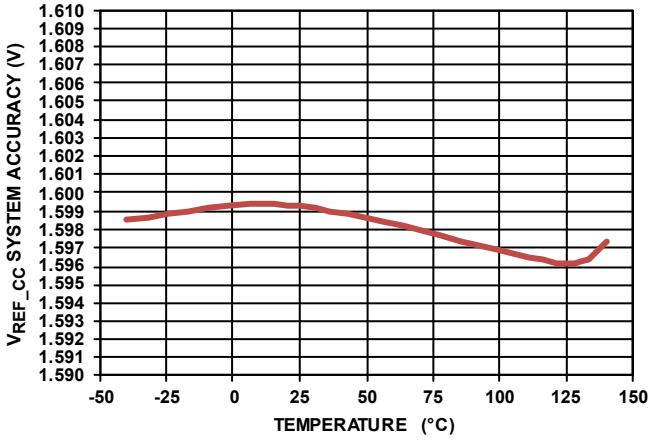


FIGURE 42. V_{REF_CC} SYSTEM ACCURACY vs TEMPERATURE, MEASURED AT THE IMON PIN, VREF_CC = 1.6V (DEFAULT)

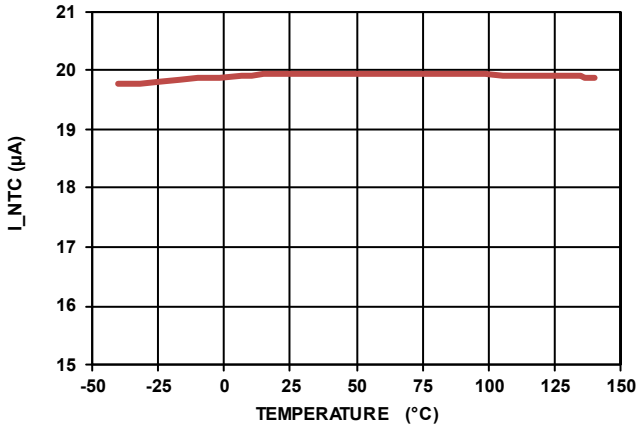


FIGURE 43. NTC PIN OUTPUT CURRENT vs TEMPERATURE, THE NTC PIN SHORTED TO GROUND

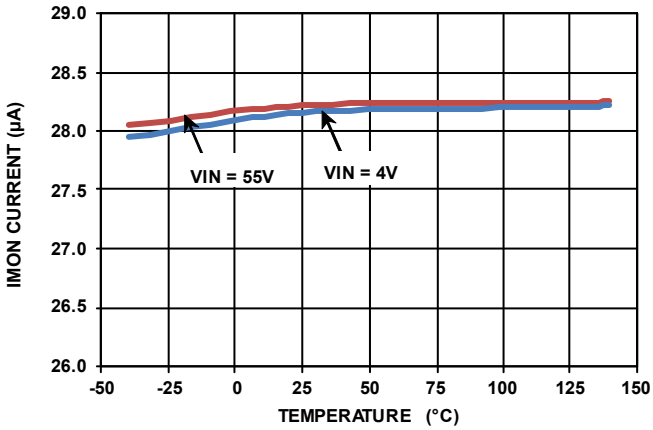


FIGURE 44. IMON OUTPUT CURRENT ACCURACY (CURRENT SENSING SIGNAL OUTPUT) vs TEMPERATURE, V_{RSENx} = 30mV, R_{SETx} = 665Ω (0.1%)

Performance Curves

Unless otherwise specified, operating conditions for the oscilloscope waveforms are V_{IN} = 12V, V_{OUT} = 36V and T_A = +25°C. **(Continued)**

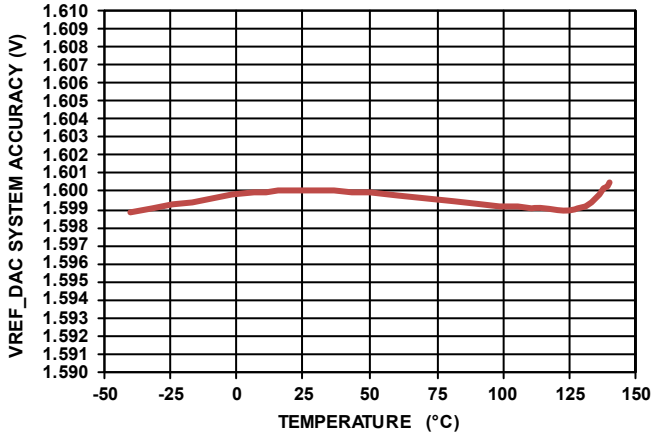


FIGURE 45. VREF_DAC SYSTEM ACCURACY vs TEMPERATURE, MEASURED AT THE FB PIN, VREF_DAC = 1.6V (DEFAULT)

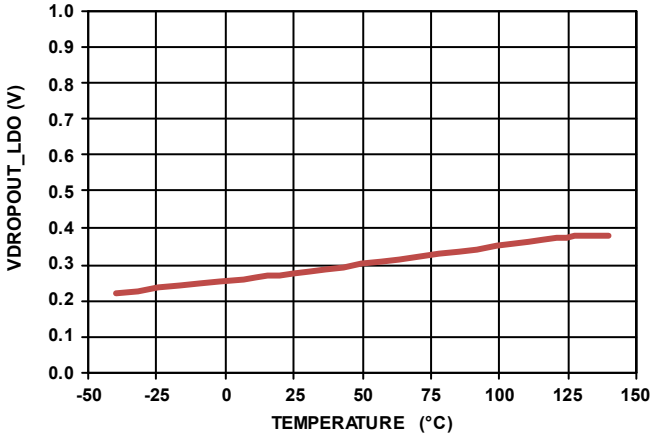


FIGURE 46. INTERNAL LDO DROPOUT VOLTAGE vs TEMPERATURE, 80mA LOAD CURRENT ON LDO OUTPUT (PVCC)

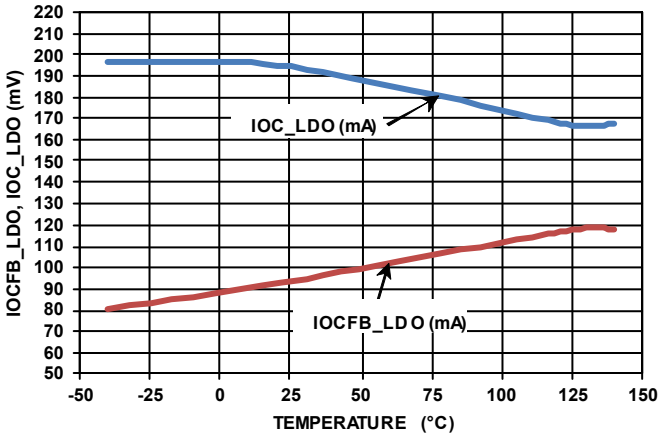


FIGURE 47. INTERNAL LDO OVERCURRENT THRESHOLD AND ITS FOLDBACK OC CURRENT vs TEMPERATURE

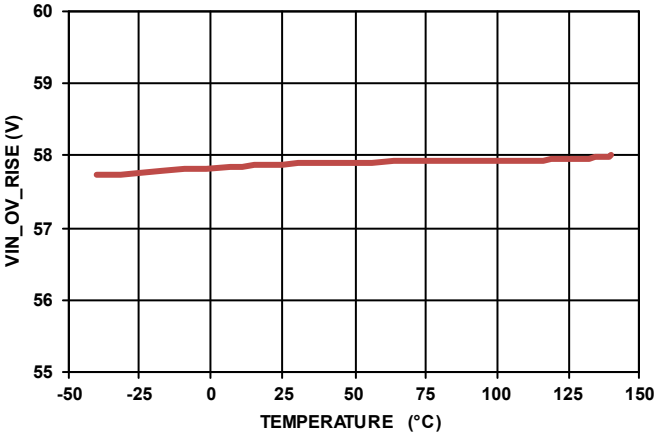


FIGURE 48. V_{IN} OV RISING THRESHOLD vs TEMPERATURE

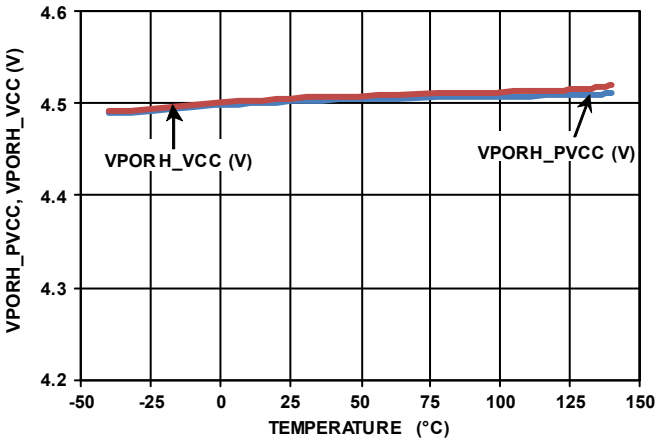


FIGURE 49. PVCC/VCC POR RISING THRESHOLD vs TEMPERATURE

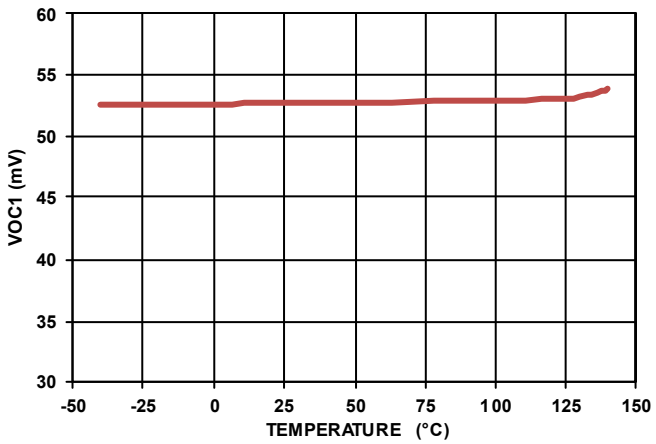


FIGURE 50. OC1 VOLTAGE THRESHOLD (ACROSS RSEN) vs TEMPERATURE

Performance Curves

Unless otherwise specified, operating conditions for the oscilloscope waveforms are V_{IN} = 12V, V_{OUT} = 36V and T_A = +25°C. **(Continued)**

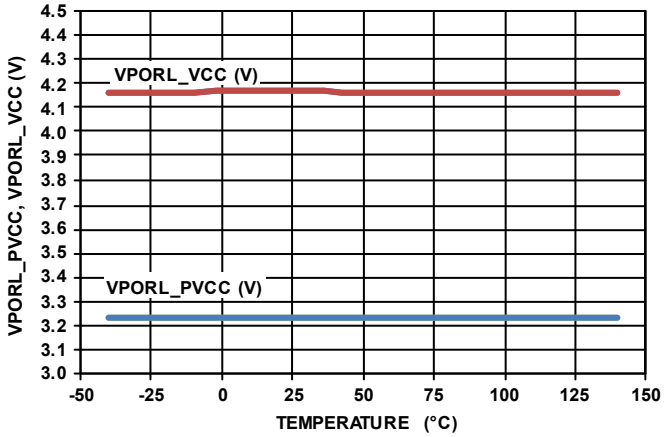


FIGURE 51. PVCC/VCC POR FALLING THRESHOLD vs TEMPERATURE

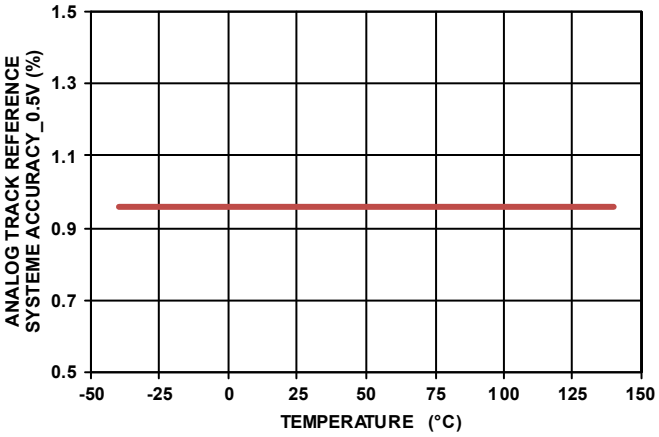


FIGURE 52. ANALOG TRACKING REFERENCE SYSTEM ACCURACY vs TEMPERATURE, MEASURED AT THE FB PIN, V_{TRACK} = 0.5V

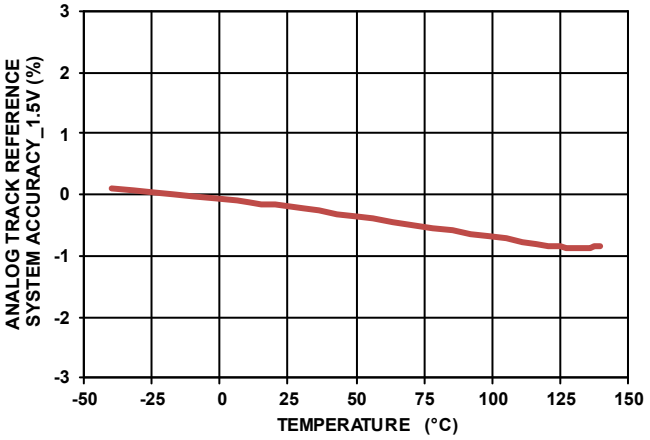


FIGURE 53. ANALOG TRACKING REFERENCE SYSTEM ACCURACY vs TEMPERATURE, MEASURED AT THE FB PIN, V_{TRACK} = 1.5V

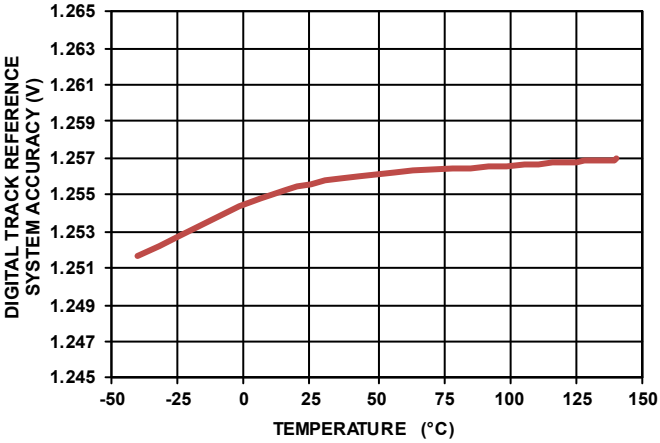


FIGURE 54. DIGITAL TRACKING REFERENCE SYSTEM ACCURACY vs TEMPERATURE, MEASURED AT THE FB PIN, DUTY CYCLE OF TRACK PIN SIGNAL IS 0.5

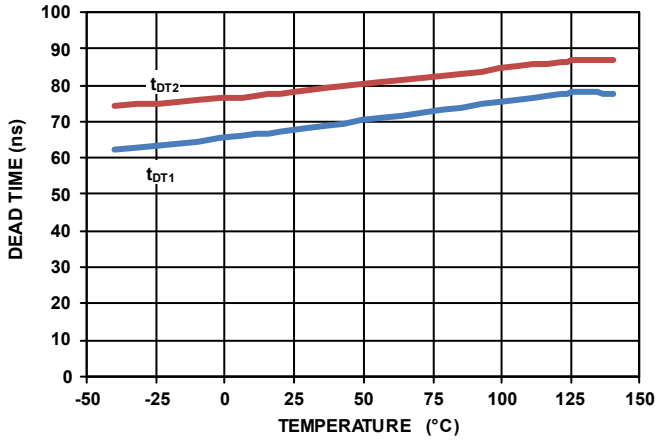


FIGURE 55. GATE DRIVE DEAD TIME vs TEMPERATURE, R_{DT} = 10k, t_{DT1} REFERS TO UG FALLING TO LG RISING, t_{DT2} REFERS TO LG FALLING TO UG RISING

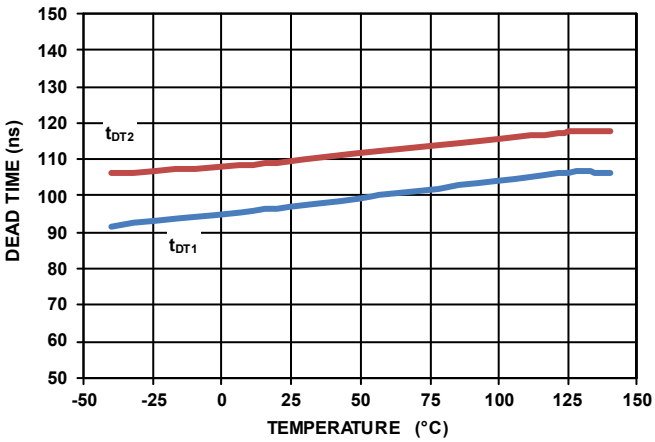


FIGURE 56. GATE DRIVE DEAD TIME vs TEMPERATURE, R_{DT} = 18.2k, t_{DT1} REFERS TO UG FALLING TO LG RISING, t_{DT2} REFERS TO LG FALLING TO UG RISING

Performance Curves

Unless otherwise specified, operating conditions for the oscilloscope waveforms are V_{IN} = 12V, V_{OUT} = 36V and T_A = +25°C. **(Continued)**

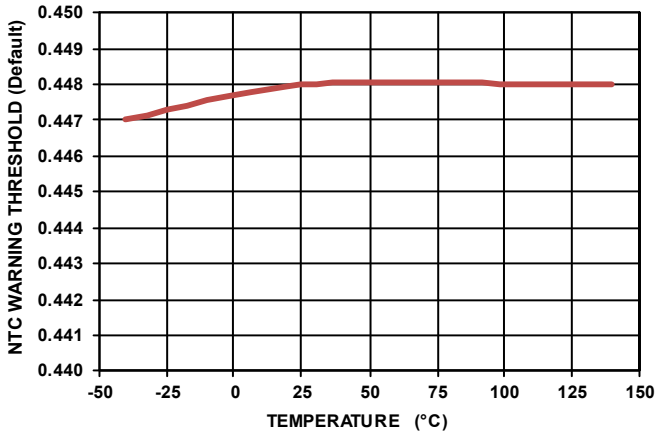


FIGURE 57. NTC WARNING THRESHOLD (DEFAULT) vs TEMPERATURE

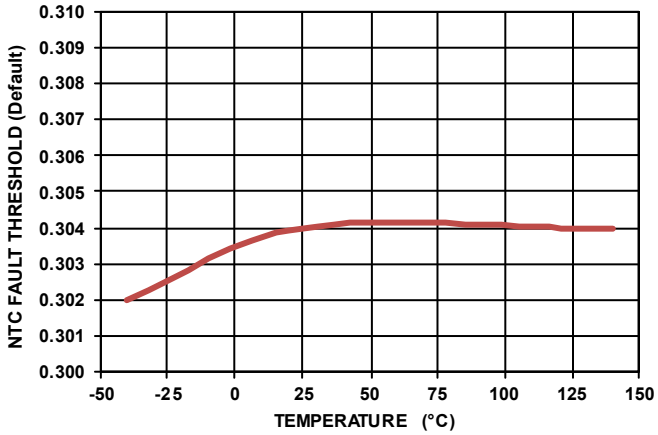


FIGURE 58. NTC FAULT THRESHOLD (DEFAULT) vs TEMPERATURE

Operation Description

The ISL78229 is a 2-phase synchronous boost controller with integrated drivers. It supports wide input and output ranges of 5V to 55V during normal operation and the VIN pin withstands transients up to 60V.

The ISL78229 is integrated with 2A sourcing/3A sinking strong drivers to support high efficiency and high current synchronous boost applications. The drivers have a unique feature of adaptive dead time control of which the dead time can be programmed for different external MOSFETs, achieving both optimized efficiency and reliable MOSFET driving. The ISL78229 has selectable diode emulation and phase dropping functions for enhanced light-load efficiency.

The PWM modulation method is a constant frequency Peak Current Mode Control (PCMC), which has benefits of input voltage feed-forward, a simpler loop to compensate compared to voltage mode control, and inherent current sharing capability.

The ISL78229 offers a track function with unique features of accepting either digital or analog signals for the user to adjust reference voltage externally. The digital signal track function greatly reduces the complexity of the interface circuits between the central control unit and the boost regulator. Equipped with cycle-by-cycle positive and negative current limiting, the track function can be reliably facilitated to achieve an envelope tracking feature in audio amplifier applications, which significantly improves system efficiency.

In addition to the cycle-by-cycle current limiting, the ISL78229 is implemented with a dedicated average Constant Current (CC) loop for input current. For devices having only peak current limiting, the average current under peak current limiting varies significantly because the inductor ripple varies with changes of V_{IN} and V_{OUT} and tolerances of f_{SW} and inductors. The ISL78229's unique CC feature accurately controls the average input current to be constant without shutdown. Under certain constant input voltage, this means constant power limiting, which is especially useful for the boost converter. It helps the user optimize the system with the power devices' capability fully utilized by well controlled constant input power.

With the PMBus compliant digital interface, the ISL78229 provides the designer access to a number of useful system control parameters and diagnostic features.

The following sections describe the function details.

Synchronous Boost

To improve efficiency, the ISL78229 employs synchronous boost architecture as shown in Figure 4 on page 8. The UGx output drives the high-side synchronous MOSFET, which replaces the freewheeling diode and reduces the power losses due to the voltage drop of the freewheeling diode.

While the boost converter is operating in steady state Continuous Conduction Mode (CCM) and each phase's low-side MOSFET is controlled to turn on with duty cycle D, ideally the upper MOSFET is ON for (1-D). Equation 1 shows the input to output voltage DC transfer function for boost is:

$$V_{OUT} = \frac{V_{IN}}{1 - D} \quad \text{(EQ. 1)}$$

DRIVER CONFIGURATION

As shown in Figure 4 on page 8, the upper side UGx drivers are biased by the C_{BOOTx} voltage between BOOTx and PHx **(where "x" indicates the specific phase number and same note applied throughout this document)**. C_{BOOTx} is charged by a charge pump mechanism. PVCC charges BOOTx through the Schottky diode D_{BOOTx} when LGx is high pulling PHx low. BOOTx rises with PHx and maintains the voltage to drive UGx as the D_{BOOTx} is reverse biased.

At start-up, charging to C_{BOOTx} from 0 to ~4.5V causes PVCC to dip slightly. A typical 5.1Ω resistor R_{PVCCBT} is recommended between PVCC and D_{BOOTx} to prevent PVCC from falling below VPORL_PVCC. The typical value for C_{BOOTx} is 0.47µF.

The BOOTx to PHx voltage is monitored by UVLO circuits. When BOOTx-PHx falls below a 3V threshold, the UGx output is disabled.

When BOOTx-PHx rises back above this threshold plus 150mV hysteresis, the high-side driver output is enabled.

For standard boost applications when upper side drivers are not needed, both UG1 and UG2 can be disabled by connecting either BOOT1 or BOOT2 to ground before part start-up initialization. PHx should be connected to ground.

PROGRAMMABLE ADAPTIVE DEAD TIME CONTROL

The UGx and LGx drivers are designed to have an adaptive dead time algorithm that optimizes operation with varying operating conditions. In this algorithm, the device detects the off timing of LGx (UGx) voltages before turning on UGx (LGx).

Furthermore, the dead time between UGx ON and LGx ON can be programmed by the resistor at the RDT pin while the adaptive dead time control is still functioning at the same time. The typical range of programmable dead time is 55ns to 200ns, or larger. This is intended for different external MOSFETs applications to adjust the dead time, maximizing the efficiency while at the same time preventing shoot-through. Refer to Figure 59 for the selection of the RDT resistor and dead time, where t_{DT1} refers to the dead time between UG Falling to LG Rising, and t_{DT2} refers to the dead time between LG Falling to UG Rising. The dead time is smaller with a lower value RDT resistor, and it is clamped to minimum 57ns when RDT is shorted to ground. Because a current as large as 4mA is pulled from the RDT pin if the RDT pin is shorted to ground, it is recommended to use 5kΩ as the smallest value for the RDT resistor where the current drawing from the RDT pin is 0.5V/5kΩ = 100µA.

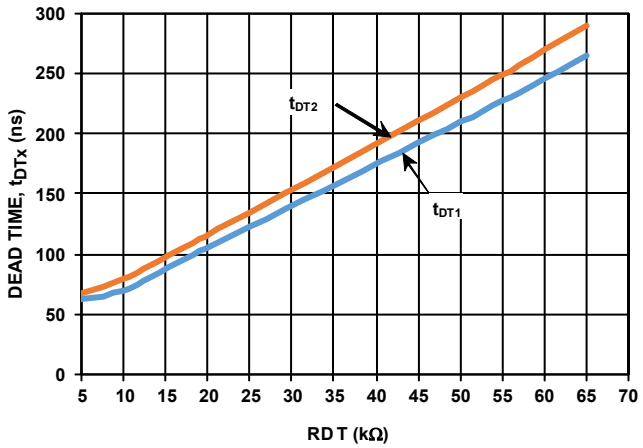


FIGURE 59. DEAD TIME vs RDT, t_{DT1} REFERS TO UG FALLING TO LG RISING, t_{DT2} REFERS TO LG FALLING TO UG RISING

PWM Control

The ISL78229 uses fixed frequency peak current mode control architecture. As shown in Figure 3 on page 7 and the typical schematic diagram, the error amplifier (Gm1) compares the FB pin voltage and reference voltage and generates a voltage loop error signal at the COMP pin. This error signal is compared with the current ramp signal (VRAMP) by the PWM comparator. The PWM comparator output combined with fixed frequency clock signal controls the SR flip-flop to generate the PWM signals (refer to "Peak Current Mode Control" on page 27).

OUTPUT VOLTAGE REGULATION LOOP

The resistor divider R_{FB2} and R_{FB1} from V_{OUT} to FB (Figure 4 on page 8) can be selected to set the desired V_{OUT}. V_{OUT} can be calculated by Equation 2:

$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R_{FB2}}{R_{FB1}}\right) \quad \text{(EQ. 2)}$$

where in normal operation after start-up, V_{REF} can be either VREF_DAC or VREF_TRK, whichever is lower. The VREF_DAC default is 1.6V and can be programmed to a value between 0 and 2.04V via the PMBus command "VOUT_COMMAND (21h)" on page 48.

Gm1 has three inputs for reference voltage: soft-start ramp SS, VREF_TRK, and VREF_DAC. The Gm1 uses the lowest value among SS, VREF_TRK, and VREF_DAC. SS, VREF_TRK, and VREF_DAC are valid for Gm1 during and after soft-start. In general operation, VREF_TRK and VREF_DAC are normally HIGH before soft-start and SS normally ramps up from a voltage lower than VREF_TRK and VREF_DAC, so SS controls the output voltage ramp-up during soft-start. After soft-start is complete, the user can adjust VREF_DAC or VREF_TRK for the desired voltage. Because VREF_TRK is valid before soft-start, setting VREF_TRK lower than SS can make the SS ramp ineffective because Gm1 uses the lower VREF_TRK voltage. In such a case, the VREF_TRK becomes the real soft-start ramp that controls the output voltage ramp-up.

Digital/Analog TRACK Function

The TRACK input provides an external reference voltage to be applied for the output voltage loop to follow, which is useful if the user wants to change the output voltage as required. An example is to employ envelope tracking technology in audio power amplifier applications. The ISL78229 boost stage output is powering the audio power amplifier stage input, where the boost output tracks the music envelope signal applied at the TRACK pin. Ultimately, higher system efficiency can be achieved.

The TRACK pin can accept either a digital signal or an analog signal by configuring the ATRK/DTRK pin to be connected to ground or VCC. Figure 60 on page 28 shows the track function block diagram. VREF_TRK is fed into Gm1 as one of the reference voltages. The Gm1 takes the lowest voltage of SS, VREF_TRK and VREF_DAC as the actual reference. When VREF_TRK is the lowest voltage, it becomes the actual reference voltage for Gm1 and the output voltage can be adjusted with TRACK signal changes. Regarding the effective VREF_TRK range:

- There is no limit for the minimum voltage on the TRACK pin, but note the lower reference voltage and the lower voltage feedback regulation accuracy. Note the SS_DONE signal is checking VREF_TRK ≥0.3V as one of the conditions (refer to the t_8-t_9 description on page 31 and Figure 67 on page 30). Also, for the boost converter, the regulated output minimum voltage is usually the input voltage minus the upper MOSFET's body diode drop, in which case, the corresponding voltage at FB voltage is the minimum effective voltage for the VREF_TRK and VREF_DAC.
- The Gm1 takes the lowest voltage of SS, VREF_TRK and VREF_DAC as the actual reference. The maximum effective range for VREF_TRK is determined by VREF_DAC or SS signal,

whichever is lower. For example, after soft-start, when the SS pin equals to 3.4V (typical) and VREF_DAC = 1.6V (default), the maximum effective voltage for VREF_TRK is 1.6V. If SS = 3.47V and VREF_DAC = 2V, the maximum effective voltage for VREF_TRK is 2V.

When ATRK/DTRK = GND (DTRK mode), the TRACK pin accepts digital signal inputs. VREF_TRK (as one of the reference inputs for the error amplifier Gm1) equals to the average duty cycle value of the PWM signal's at the TRACK pin. As shown in Figure 60 on page 28, the MUX is controlled by the ATRK/DTRK pin configurations. When ATRK/DTRK = GND, the MUX connects the output of the Q1 and Q2 switch bridge to the input of a 2-stage RC filter (R_1, C_1, R_2 and C_2). The PWM signal at the TRACK pin controls Q1 and Q2 to chop the 2.5V internal reference voltage. The phase node of Q1 and Q2 is a PWM signal with accurate 2.5V amplitude and duty cycle D, where D is the input PWM duty cycle on the TRACK input pin. The RC filter smooths out the PWM AC components and the voltage VREF_TRK after the RC filter becomes a DC voltage equaling to 2.5V * D:

$$V_{REFTRK} = 2.5 \cdot D \quad \text{(EQ. 3)}$$

According to Equation 3, the PWM signals' amplitude at the TRACK pin does not affect the VREF_TRK accuracy, and only the duty cycle value changes the VREF_TRK value. In general, the VREF_TRK reference accuracy is as good as the 2.5V reference. The built-in low pass filter (R_1, C_1, R_2 and C_2) converts the PWM signal's duty cycle value to a low noise reference. The low pass filter has a cutoff frequency of 1.75kHz and a gain of -40dB at 400kHz. The 2.5V PWM signal at phase node of Q1 and Q2 has around 25mV at VREF_TRK, which is 1.56% of 1.6V reference. This does not affect the boost output voltage because of the limited bandwidth of the system. 400kHz frequency is recommended for the PWM signal at the TRACK pin. Lower frequency at the TRACK input is possible, but VREF_TRK has higher AC ripple. Bench test evaluation is needed to make sure the output voltage is not affected by this VREF_TRK AC ripple.

When ATRK/DTRK = VCC (ATRK mode), the MUX connects the TRACK pin voltage to the input of the 2-stage RC filter $R_1/C_1/R_2/C_2$. In such a way, the TRACK pin accepts analog signal inputs, with the Gm1's VREF_TRK input equal to the voltage on the TRACK pin. It has the same low pass filter with a cutoff frequency of 1.75kHz.

If not used, the TRACK pin should be left floating or tied to VCC and the internal VREF_DAC working as the reference.

The TRACK function is enabled before the SS pin soft-start. The V_{OUT} reference can be controlled by TRACK inputs at start-up. After the SS pin ramps up to the upper clamp AND the VREF_TRK reaches 0.3V, the upper side FET is controlled to turn on gradually to achieve smooth transitions from DCM mode to CCM mode, of which transition duration is 100ms (when set at CCM mode). After this transition, PGOOD is allowed to be pulled HIGH as long as when output voltage is in regulation (within OV/UV threshold).

The maximum TRACK reference frequency for the boost V_{OUT} to track is limited by the boost converter's loop bandwidth. Generally, the tracking reference signal's frequency should be 10 times lower than the boost loop crossover frequency. Otherwise, the boost output voltage cannot track the tracking reference signal and the output voltage is distorted. For example, for a boost converter with 4kHz loop crossover frequency, the boost can track reference signals up to 400Hz, typically. Figures 23 and 24 on page 19 show performances tracking 100Hz and 300Hz signals.

PEAK CURRENT MODE CONTROL

As shown in the Figure 3 on page 7, each phase's PWM operation is initialized by the fixed clock for this phase from the oscillator (refer to "Oscillator and Synchronization" on page 29). The clocks for Phase 1 and Phase 2 are 180° out of phase. The low-side MOSFET is turned on (LGx) by the clock (after a dead time delay of t_{DT1}) at the beginning of a PWM cycle and the inductor current ramps up. The ISL78229's Current Sense Amplifiers (CSA) sense each phase inductor current and generate the current sense signal I_{SENx}. The I_{SENx} is added with the compensating slope and generates V_{RAMPx}. When V_{RAMPx} reaches the error amplifier (Gm1) output voltage, the PWM comparator is triggered and LGx is turned off to shut down the low-side MOSFET. The low-side MOSFET stays off until the next clock signal comes for the next cycle.

After the low-side MOSFET is turned off, the high-side MOSFET turns on after dead time t_{DT2}. The turn-off time of the high-side MOSFET is determined by either the PWM turn-on time at the next PWM cycle, or when the inductor current become zero if the Diode Emulation mode is selected.

Multiphase Power Conversion

For an n-phase interleaved multiphase boost converter, the PWM switching of each phase is distributed evenly with 360/n phase shift. The total combined current ripples at the input and output are reduced where smaller input and output capacitors can be used. In addition, it is beneficial to have a smaller equivalent inductor for a faster loop design. Also in some applications, especially in a high current case, multiphase makes it possible to use a smaller inductor for each phase rather than one big inductor (single-phase), which is sometimes more costly or unavailable on the market at the high current rating. Smaller size inductors also help to achieve low profile design.

The ISL78229 is a controller for 2-phase interleaved converter where the 2 phases are operating with 180° phase shift, meaning each PWM pulse is triggered 1/2 of a cycle after the start of the PWM pulse of the previous phase. Figure 61 illustrates the interleaving effect on input ripple current. The AC components of the two phase currents (I_{L1} and I_{L2}) interleave each other and the combined AC current ripples (I_{L1} + I_{L2}) at input are reduced. Equivalently, the frequency of the AC inductor ripple at input is two times the switching frequency per phase.

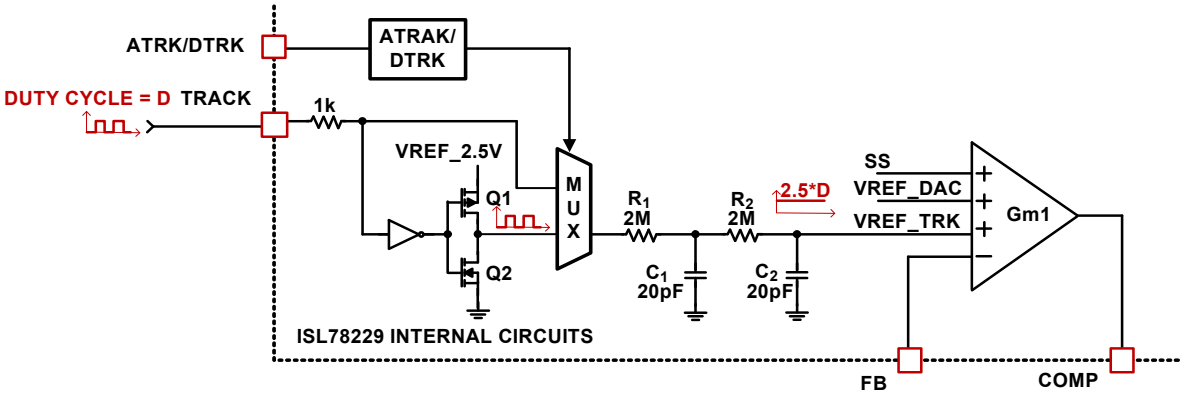


FIGURE 60. TRACK FUNCTION BLOCK DIAGRAM

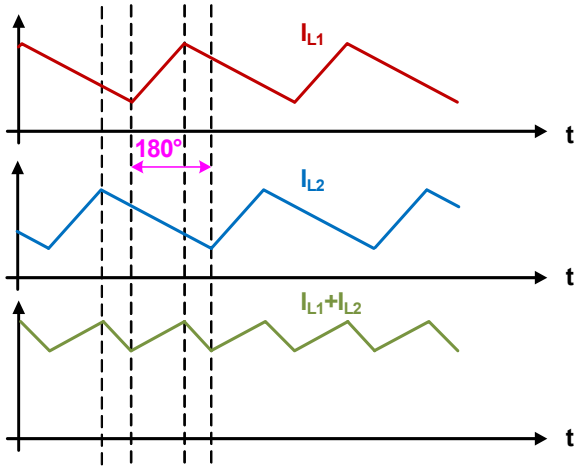


FIGURE 61. PHASE NODE AND INDUCTOR-CURRENT WAVEFORMS FOR 2-PHASE CONVERTER

To understand the reduction of the ripple current amplitude in the multiphase circuit, refer to Equation 4, which represents an individual phase's peak-to-peak inductor current.

In Equation 4, V_{IN} and V_{OUT} are the input and the output voltages respectively, L is the single-phase inductor value, and f_{SW} is the switching frequency.

$$I_{PPCH} = \frac{(V_{OUT} - V_{IN})V_{IN}}{Lf_{SW}V_{OUT}} \quad \text{(EQ. 4)}$$

The input capacitors conduct the ripple component of the inductor current. In the case of a 2-phase boost converters, the capacitor current is the sum of the ripple currents from each of the individual phases. Use Equation 5 to calculate the peak-to-peak ripple of the total input current which goes through the input capacitors, where K_{P-P} can be found in Figure 62 under the specific duty cycle.

$$I_{PPALL} = K_{P-P} \cdot I_{PPCH} \quad \text{(EQ. 5)}$$

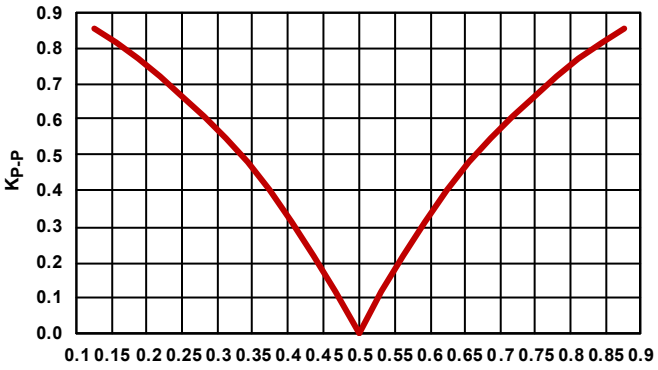


FIGURE 62. K_{P-P} vs DUTY CYCLE

CURRENT SHARING BETWEEN PHASES

The peak current mode control inherently has current sharing capability. As shown in Figure 3 on page 7, the current sense ramp V_{RAMPx} of each phase are compared to the same error amplifier's output at the COMP pin by the PWM comparators to turn off LGx when V_{RAMPx} reaches COMP. Thus, the V_{RAMPx} peaks are controlled to be the same for each phase. V_{RAMPx} is the sum of instantaneous inductor current sense ramp and the compensating slope. Because the compensating slopes are the same for both phases, the inductor peak current of each phase is controlled to be the same.

The same mechanism applies if multiple ISL78229s are configured in parallel for multiphase boost converter. The COMP pins of each ISL78229 are tied together for each phase's current sense ramp peak to be compared with the same COMP voltage (V_{RAMPx} = COMP), meaning the inductor peak currents of all the phases are controlled to be the same. The "4-Phase Operation" section describes how to configure two ISL78229s in parallel for a 4-phase interleaved boost converter.

4-PHASE OPERATION

Two ISL78229s can be used in parallel to achieve interleaved 4-phase operation. Figure 63 on page 29 shows the recommended configuration. The CLKOUT from the master IC drives FSYNC of the slave IC to synchronize the switching frequencies. This achieves a 90° phase shift for the four phases switching, and the respective COMP, FB, SS, EN, and IMON pins of the two ICs are connected.

CLKOUT is 90° out-of-phase with the rising edge of LG1. Therefore, the two phases of the second IC are interleaved with the two phases of the first IC.

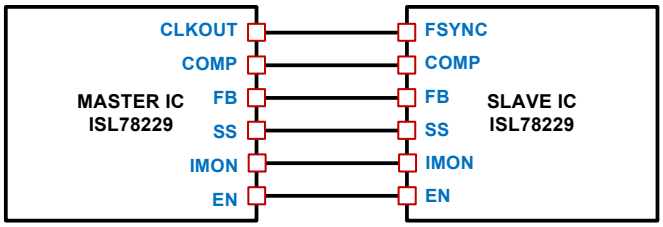


FIGURE 63. CONFIGURATIONS FOR DUAL IC 4-PHASE OPERATION

When using PMBus functions for the two ISL78229s operating in parallel, the telemetry functions as reading register information from the ISL78229 works fine. For example, the host can read from PMBus for the VIN, FB, IMON, NTC voltages, fault status, and all other registers. The host only reads the information and does not change the operating conditions.

However, when using WRITE commands to either control an ISL78229 action (like OPERATION ON/OFF), or configure the fault protection response or thresholds, the designer should carefully evaluate the scenarios of the two ICs operation in parallel. For example, it is recommended to configure both of the ICs to have the same fault thresholds settings. Otherwise, one of the IC's thresholds is not effective. If any fault protection occurs (Latch-off or Hiccup), because the SS pins are connected together, the two ICs' PWM switching is shut off. Generally, it's suggested to set the fault response to Hiccup mode. When the fault condition is gone, the two ICs can always restart to normal operations.

Oscillator and Synchronization

The switching frequency is determined by the selection of the frequency-setting resistor, R_{FSYNC}, connected from the FSYNC pin to GND. Equation 6 is provided to assist in selecting the correct resistor value.

$$R_{FSYNC} = 2.49x(10)^{10}\left(\frac{0.505}{f_{SW}} - 5.5X10^{-8}\right) \quad \text{(EQ. 6)}$$

where f_{SW} is the switching frequency of each phase. Figure 64 shows the relationship between R_{FSYNC} and switching frequency.

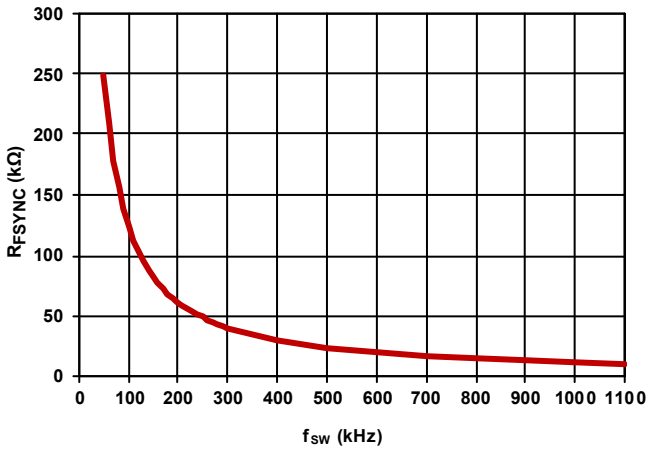


FIGURE 64. f_{SW} vs R_{FS}

The ISL78229 contains a Phase Lock Loop (PLL) circuit. Referring to Figure 4 on page 8, the PLL is compensated with a series resistor-capacitor (R_{PLL} and C_{PLL1}) from the PLLCOMP pin to GND and a capacitor (C_{PLL2}) from PLLCOMP to GND. At a 300kHz switching frequency, typical values are R_{PLL} = 3.24kΩ, C_{PLL1} = 6.8nF, and C_{PLL2} = 1nF. The PLL locking time is around 0.7ms. Generally, the same PLL compensating network can be used in the frequency range of 50kHz to 1.1MHz. With the same PLL compensation network, at a frequency range higher than 500kHz, the PLL loop is overcompensated. However, the PLL loop is stable just with slow frequency response. If a faster frequency response is required at a higher operating frequency, the PLL compensation network can be tuned to have a faster response. An Excel sheet to calculate the PLL compensation is provided on the ISL78229 product page.

The ISL78229's switching frequency can be synchronized to the external clock signals applied at the FSYNC pin. The ISL78229 detects the input clock's rising edge and synchronizes the rising edge of LG1 to the input clock's rising edge with a dead time delay of t_{DT1}. The switching frequency of each phase equals the fundamental frequency of the clock input at FSYNC. Because the ISL78229 detects only the edge of the input clock instead of its pulse width, the input clock's pulse width can be as low as 20ns (as minimum), tens of ns, or hundreds of ns depending on the capability of the specific system to generate the external clock.

The CLKOUT pin outputs a clock signal with the same frequency of per phase switching frequency. Its amplitude is V_{CC} and pulse width is 1/12 of per phase switching period (t_{SW}/12). Figure 65 shows the application example to put two ISL78229s in parallel with the master IC's CLKOUT being connected to the FSYNC pin of the slave IC for 4-phase interleaved operation. The master IC outputs CLKOUT signal with delay of (t_{SW}/4-t_{DT1}) after LG1_master. The slave IC FSYNC pin takes the CLKOUT_master as the input and the slave's IC LG1 is delayed by a time of (35ns + t_{DT1}). Therefore, the LG1_slave is delayed by (t_{SW}/4 + 35ns) to LG1_master, which is approximately a 90° phase shift. With 90° phase shift between LG1 and respective LG2 for each IC, an interleaved 4-phases with 90° phase shift boost is achieved.

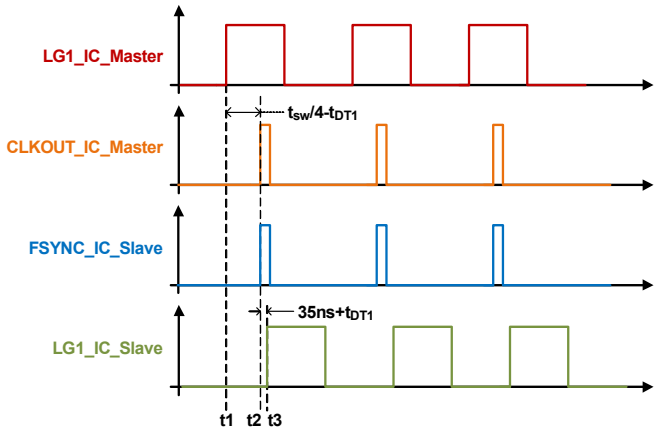


FIGURE 65. TIMING DIAGRAM OF CLKOUT vs LG1 AND FSYNC vs LG1 (CLKOUT_MASTER CONNECTED TO FSYNC_SLAVE)

After the ISL78229 latches to be synchronized with the external clock, if the external clock on the FSYNC pin is removed, the switching frequency oscillator shuts down. Then the part detects a PLL_LOCK fault (refer to Table 4 on page 41), and goes to either Hiccup mode or Latch-off mode as described in "Fault Response Register SET_FAULT_RESPONSE (D2h)" on page 35. If the part is set in Hiccup mode, the part restarts with frequency set by the resistor at the FSYNC pin.

The switching frequency range of the ISL78229 set by R_{FSYNC} or by synchronization is typically 50kHz to 1.1MHz.

The low end 50kHz is determined by PLL_LOCK fault protection, which shuts down the IC when the frequency is lower than 37kHz typical (refer to Table 3 on page 41). The device can operate at frequencies lower than 50kHz by masking the PLL_LOCK fault protection through the PMBus command "FAULT_MASK (D1h)" on page 59.

The phase dropping mode is **not allowed** with external synchronization.

MINIMUM ON-TIME (BLANK TIME) CONSIDERATION

The minimum ON-time (also called BLANK time) of LGx is the minimum ON pulse width as long as LGx is turned ON. It is also intended for the internal circuits to blank out the noise spikes after LGx turns on. The t_{MINON} can be programmed by a resistor at the RBLANK pin.

The selection of the t_{MINON} depends on two considerations.

1. The noise spike durations after LGx turns on, which is normally in a range of tens of ns to 100ns or longer depending on the external MOSFET switching characteristic and noise coupling path to current sensing.
2. Ensure the charging of the boot capacitor during operations of LGx operating at t_{MINON}. One typical case is an operation when the input voltage is close to the output voltage. The duty cycle is smallest at t_{MINON} and C_{BOOTx} is charged by PVCC via D_{BOOTx} with short duration of t_{MINON} minus the delay to pull phase low. If such operation is required, especially when a large MOSFET with large Q_g is used to support heavy load application, larger t_{MINON} can be programmed with the resistor at the RBLANK pin to ensure C_{BOOTx} can be sufficiently charged during minimum duty cycle operation.

Refer to Figure 66 for the selection of R_{BLANK} resistor and t_{MINON} time. A 5kΩ resistor is recommended as the minimum R_{BLANK} resistor.

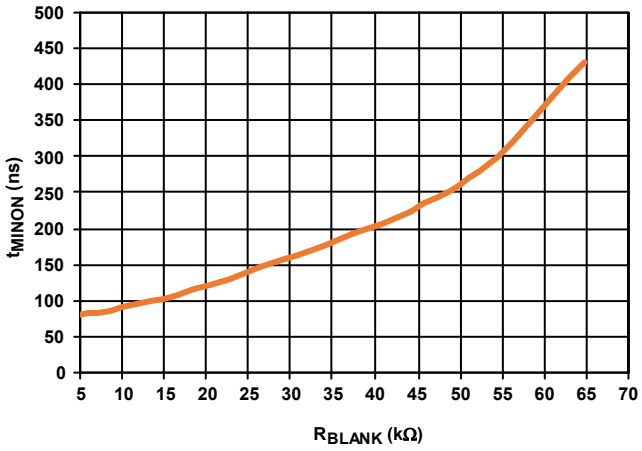


FIGURE 66. t_{MINON} vs R_{BLANK}

Operation Initialization and Soft-Start

Before converter initialization, the EN pin voltage must be higher than its rising threshold and the PVCC/VCC pin must be higher than the rising POR threshold. When these conditions are met, the controller begins initialization and soft-start. Figure 67 shows the ISL78229 internal start-up timing diagram from the power-up to soft-start.

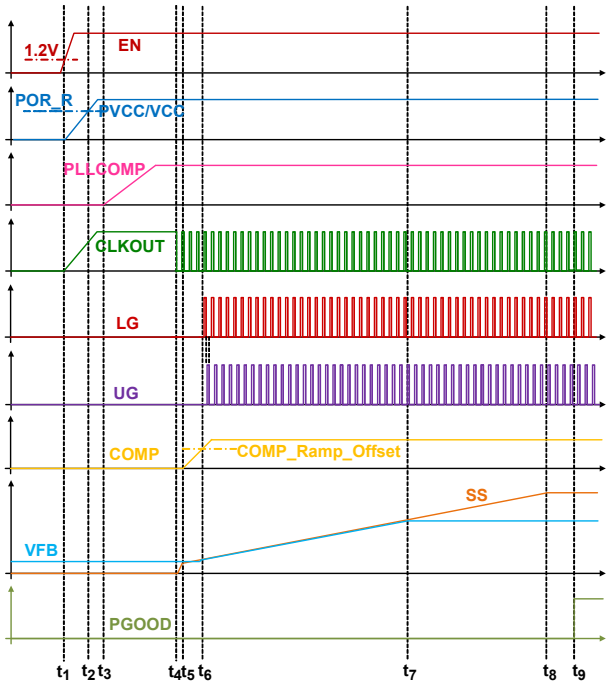


FIGURE 67. CIRCUIT INITIALIZATION AND SOFT-START

Assuming input voltage is applied to the VIN pin before t_1 and VCC is connected to PVCC, as shown on Figure 67, the start-up procedure is described as follows:

t_1 - t_2: The enable comparator holds the ISL78229 in shutdown until the V_{EN} rises above 1.2V (typical) at the time of t_1. During t_1 - t_2, $V_{PVCC/VCC}$ gradually increases and reaches the internal Power-On Reset (POR) rising threshold 4.5V (typical) at t_2.

t_2 - t_3: During t_2 - t_3, the ISL78229 self-calibrates to detect certain pin configurations (HIC/LATCH, DE/PHDRP, ATRK/DTRAK) to latch in the selected operation modes. The time duration for t_2 - t_3 is typically 195µs.

t_3 - t_4: During this period, the ISL78229 waits until the internal PLL circuits are locked to the preset oscillator frequency. When PLL locking is achieved at t_4, the oscillator generates output at the CLK_OUT pin. The time duration for t_3 - t_4 depends on the PLLCOMP pin configuration. The PLL is compensated with a series resistor-capacitor (R_{PLL} and C_{PLL1}) from the PLLCOMP pin to GND and a capacitor (C_{PLL2}) from PLLCOMP to GND. At the 300kHz switching frequency, typical values are R_{PLL} = 3.24kΩ, C_{PLL1} = 6.8nF, and C_{PLL2} = 1nF. With this PLLCOMP compensation, the time duration for t_3 - t_4 is around 0.7ms.

t_4 - t_5: The PLL locks the frequency t_4 and the system prepares to soft-start. The ISL78229 has one unique feature to pre-bias the SS pin voltage to be equal to V_{FB} during t_4 - t_5, which is around 50µs.

t_5 - t_6: At t_5 the soft-start ramps up at the SS pin (V_{SSPIN}) and the COMP voltage starts to ramp up as well. Drivers are enabled but not switching during t_5 - t_6 because the COMP is still below the current sense ramp offset. The device operates in DE mode during soft-start period t_5 - t_8. The slew rate of the SS ramp and the duration of t_5 - t_8 are determined by the capacitor used at the SS pin.

t_6 - t_7: At t_6 COMP is above the current sense ramp offset and the drivers start switching. Output voltage ramps up while FB voltage is following SS ramp during this soft-start period. At t_7, output voltage reaches the regulation level and FB voltage reaches 1.6V (VREF_DAC Default).

t_7 - t_8: SS continues ramping up until it reaches the SS clamp voltage ($V_{SSPCLAMP}$) 3.47V at t_8, indicating the SS pin ramp-up is completed. At t_8, the ISL78229 generates an internal SS_DONE signal, which goes HIGH when both V_{SSPIN} = $V_{SSPCLAMP}$ (3.47V) and VREF_TRK ≥ 0.3V (as shown in Figure 3 on page 7). This indicates the soft-start has completed.

t_8 - t_9: After t_8, a delay time of either 0.5ms or 100ms is inserted before the PGOOD pin is released HIGH at t_9 depending on the selected mode (refer to Table 2 on page 34).

1. If the DE/PHDRP pin = VCC or FLOAT to have DE mode selected, the PGOOD rising delay from V_{SSPIN} = $V_{SSPCLAMP}$ (3.47V) AND VREF_TRK ≥0.3V to PGOOD rising is 0.5ms.
2. If the DE/PHDRP pin = GND to have CCM mode selected, the PGOOD rising delay from V_{SSPIN} = $V_{SSPCLAMP}$ (3.47V) and VREF_TRK ≥0.3V to PGOOD rising is 100ms, during which period the device is transitioning from DE mode to CCM mode. The high-side gate UGx is controlled to gradually increase the ON time to finally merge with CCM ON-time. This synchronous MOSFET "soft-ON" feature is unique and ensures smooth transition from DCM mode to CCM mode after soft-start completes. More importantly, this "SYNC FET soft-ON" function eliminates the large negative current, which usually occurs when starting up to a high prebiased output voltage. This feature makes the system robust for all the challenging start-up conditions and greatly improves the system reliability.

Enable

To enable the device, the EN pin needs to be driven higher than 1.2V (typical) by the external enable signal or resistor divider between VIN and GND. The EN pin has an internal 5MΩ (typical) pull-down resistor. This pin also internally has a 5.2V (typical) clamp circuit with a 5kΩ (typical) resistor in series to prevent excess voltage applied to the internal circuits. When applying the EN signal using resistor divider from VIN, internal pull-down resistance needs to be considered. Also, the resistor divider ratio needs to be adjusted as its EN pin input voltage may not exceed 5.2V.

To disable or reset all fault status, the EN pin needs to be driven lower than 1.1V (typical). When the EN pin is driven low, the ISL78229 turns off all of the blocks to minimize the off-state quiescent current.

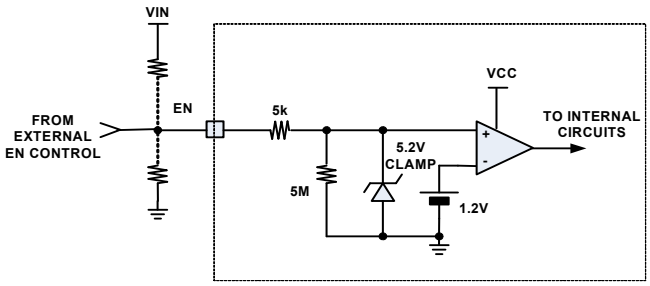


FIGURE 68. ENABLE BLOCK

Soft-Start

Soft-start is implemented by an internal 5µA current source charging the soft-start capacitor (C_{SS}) at SS to ground. The voltage on the SS pin slowly ramps up as the reference voltage for the FB voltage to follow during soft-start.

Typically, for boost converter before soft-start, its output voltage is charged up to be approximately a diode drop below the input voltage through the upper side MOSFETs' body diodes. To more accurately correlate the soft-start ramp time to the output voltage ramp time, the ISL78229 SS pin voltage is prebiased with voltage equal to FB before soft-start begins. The soft-start ramp time for the boost output voltage ramping from V_{IN} to the final regulated voltage V_{OUTreg}, can be calculated by Equation 7, where V_{REF} is typically the VREF_DAC voltage (1.6V default) with the TRACK pin tied HIGH:

$$t_{SS} = V_{REF} \cdot \left(1 - \frac{V_{IN}}{V_{OUTreg}}\right) \cdot \frac{C_{SS}}{5\mu A} \quad \text{(EQ. 7)}$$

PGOOD Signal

The PGOOD pin is an open-drain logic output to indicate that the soft-start period is completed, the input voltage is within safe

operating range, and the output voltage is within the specified range. The PGOOD comparator monitors the FB pin to check if output voltage is within 80% to 120% of reference voltage VREF_DAC (1.6V default).

As described at the t_8 - t_9 duration in "Operation Initialization and Soft-Start" on page 30, the PGOOD pin is pulled low during soft-start and is released HIGH after SS_DONE with a 0.5ms or 100ms delay.

PGOOD is pulled low if any of the comparators for FB_UV, FB_OV or VIN_OV is triggered for a duration longer than 10µs.

In normal operation after start-up, under fault recovery, PGOOD is released high with the same 0.5ms delay time after the fault is removed.

Current Sense

The ISL78229 peak current control architecture senses the inductor current continuously for fast response. A sense resistor is placed in series with the power inductor for each phase, and the ISL78229 Current Sense Amplifiers (CSA) continuously sense the respective inductor current as shown in Figure 69 on page 32 by sensing the voltage signal across the sense resistor R_{SENx} (where "x" indicates the specific phase number and same note applied throughout this document). The sensed current for each active phase is used for peak current mode control loop, phase current balance, individual phase cycle-by-cycle peak current limiting (OC1), individual phase overcurrent fault protection (OC2), input average Constant Current (CC) control and average overcurrent protection (OC_AVG), diode emulation, and phase drop control. The internal circuitry shown in Figure 69 represents a single phase. This circuitry is repeated for each phase.

CURRENT SENSE FOR INDIVIDUAL PHASE - I_{SENX}

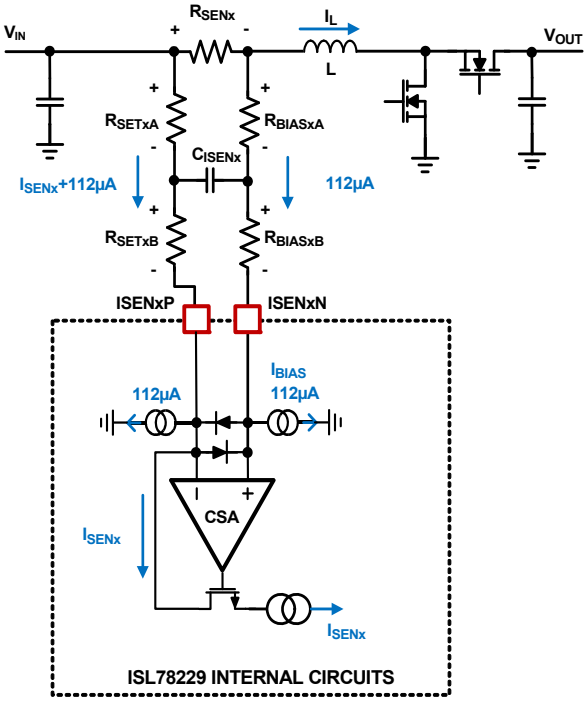


FIGURE 69. CURRENT SENSING BLOCK DIAGRAM

The RC network between R_{SENx} and ISENxP/N pins as shown in Figure 69 is the recommended configuration. The ISENxP pin should be connected to the positive potential of the R_{SEN_CHx} through resistor R_{SETx}, where in Figure 69 R_{SETx} is composed by R_{SETxA} plus R_{SETxB}. R_{SET} is used to set the current sense gain externally.

$$R_{SETx} = R_{SETxA} + R_{SETxB} \quad \text{(EQ. 8)}$$

Because there is a 112µA bias current sinking to each of the ISENxP and ISENxN pins, R_{BIASx} with the same value to R_{SETx} should be placed between the ISENxN pin to the low potential of the R_{SENx}, where in Figure 69 R_{BIASx} is composed by R_{BIASxA} plus R_{BIASxB}.

$$R_{BIASx} = R_{BIASxA} + R_{BIASxB} \quad \text{(EQ. 9)}$$

$$R_{BIASx} = R_{SETx} \quad \text{(EQ. 10)}$$

It is recommended to have $R_{SETxA} = R_{BIASxA}$ and $R_{SETxB} = R_{BIASxB}$, and insert a capacitor (C_{ISENx}) between them as shown in Figure 69. This forms a symmetric noise filter for the small current sense signals. The differential filtering time constant equals to $(R_{SETxA}+R_{BIASxA})*C_{ISENx}$. This time constant is typically selected in range of tens of ns depending on the actual noise levels.

CSA generates the sensed current signal I_{SENx} by forcing ISENxP voltage to be equal to ISENxN voltage. Because R_{SETx} equals to R_{BIASx}, the voltage drop across R_{SETx} and R_{BIASx} incurred by the fixed 112µA bias current cancels each other. Therefore, the resulting current at CSA output I_{SENx} is proportional to each phase inductor current I_{Lx}. I_{SENx} per phase can be derived in Equation 11, where I_{Lx} is the per phase current flowing through R_{SENx}.

$$I_{SENx} = I_{Lx} \cdot \frac{R_{SENx}}{R_{SETx}} \quad \text{(EQ. 11)}$$

R_{SENx} is normally selected with smallest resistance to minimize the power loss on it. With R_{SENx} selected, R_{SETx} is selected by the desired cycle-by-cycle peak current limiting level OC1 (refer to "Peak Current Cycle-by-Cycle Limiting (OC1)" on page 36).

AVERAGE CURRENT SENSE FOR 2 PHASES - IMON

The IMON pin serves to monitor the total average input current of the 2-phase boost. As shown in Figure 3 on page 7, the individual current sense signals (I_{SENx}) are divided by 8 and summed together. A 17µA offset current is added to form a current source output at the IMON pin with the value calculated as in Equation 12.

$$IMON = \left(\frac{I_{L1} \cdot R_{SEN1}}{R_{SET1}} + \frac{I_{L2} \cdot R_{SEN2}}{R_{SET2}}\right) \cdot 0.125 + 17 \cdot 10^{-6} \quad \text{(EQ. 12)}$$

Assume $R_{SEN1} = R_{SEN2}$, $R_{SET1} = R_{SET2}$, and $I_{IN} = I_{L1}+I_{L2}$, which is the total boost input average current:

$$IMON = I_{IN} \cdot \frac{R_{SEN}}{R_{SET}} \cdot 0.125 + 17 \cdot 10^{-6} \quad \text{(EQ. 13)}$$

As shown in Figure 4 on page 8, a resistor R_{IMON} is placed between the IMON pin and ground, which turns the current sense output from the IMON pin to a voltage V_{IMON}. A capacitor C_{IMON} should be used in parallel with R_{IMON} to filter out the ripple such that V_{IMON} represents the total average input current of the 2-phase boost. V_{IMON} can be calculated using Equation 14.

$$V_{IMON} = IMON \cdot R_{IMON} \quad \text{(EQ. 14)}$$

As shown in Figure 3 on page 7, V_{IMON} is fed to inputs of Gm2 and comparators of CMP_PD and CMP_OCAVG for the following functions:

- V_{IMON} is compared with 1.6V (VREF_CC) at error amplifier Gm2 inputs to achieve constant current control function. The CC control threshold for the boost input current is typically set in a way that the per phase average inductor current (when CC control) is lower than the per phase cycle-by-cycle peak current limiting (OC1) threshold. Refer to "Constant Current Control (CC)" on page 37 for detailed descriptions.
- V_{IMON} is compared with phase dropping thresholds (1.1V falling to drop Phase2, 1.15V rising to add Phase2). Refer to "Automatic Phase Dropping/Adding" on page 34 for detailed descriptions.
- V_{IMON} is compared with 2V for OC_AVG fault protections. Refer to "Average Overcurrent Fault (OC_AVG)" on page 38 for detailed descriptions.

The typical scenario when fast overloading is applied is described below. When a large overload is suddenly applied at boost output, the phase inductor peak currents are initially limited by OC1 cycle-by-cycle, during which time the IMON voltage slowly rises up due to the filter delay of R_{IMON} and C_{IMON}. When V_{IMON} reaches 1.6V, the CC loop starts to limit and control the average current to be constant, which lowers the inductor current. As described previously, the CC threshold normally is set lower than the OC1 cycle-by-cycle limiting threshold. Typically tens of nF are used for C_{IMON}. If a longer time delay is needed, a larger C_{IMON} can be used. Refer to "Constant Current Control (CC)" on page 37 for a more detailed description.

Adjustable Slope Compensation

For a boost converter with peak current mode control, slope compensation is needed when the duty cycle is larger than 50%. It is advised to add slope compensation when the duty cycle is approximately 30 to 40% because a transient load step can push the duty cycle higher than the steady state level. When slope compensation is too low, the converter suffers from subharmonic oscillation, which may result in noise emissions at half the switching frequency. On the other hand, overcompensation of the slope may reduce the phase margin. Therefore, proper design of the slope compensation is needed.

The ISL78229 features adjustable slope compensation by setting the resistor value R_{SLOPE} from the SLOPE pin to ground. This function eases the compensation design and provides more flexibility in choosing the external components.

Figure 70 shows the block diagram related to slope compensation. For current mode control, in theory, the compensation slope slew rate m_{SL} needs to be larger than 50% of the inductor current down ramp slope slew rate m_b.

Equation 15 shows the resistor value R_{SLOPE} at the SLOPE pin to create a compensation ramp.

$$R_{SLOPE} = \frac{6.67 \cdot 10^5 \cdot L_x \cdot R_{SETx}}{K_{SLOPE} \cdot (V_{OUT} - V_{IN}) \cdot R_{SENx}} (\Omega) \quad \text{(EQ. 15)}$$

where K_{SLOPE} is the selected gain of compensation slope over inductor down slope. For example, K_{SLOPE} = 1 gives the R_{SLOPE} value generating a compensation slope equal to inductor current down ramp slope. Theoretically, the K_{SLOPE} needs to be larger than 0.5, but practically more than 1.0 is used in the actual application. To cover the operating range, the maximum of V_{OUT} and minimum of V_{IN} should be used in Equation 15 to calculate the R_{SLOPE}.

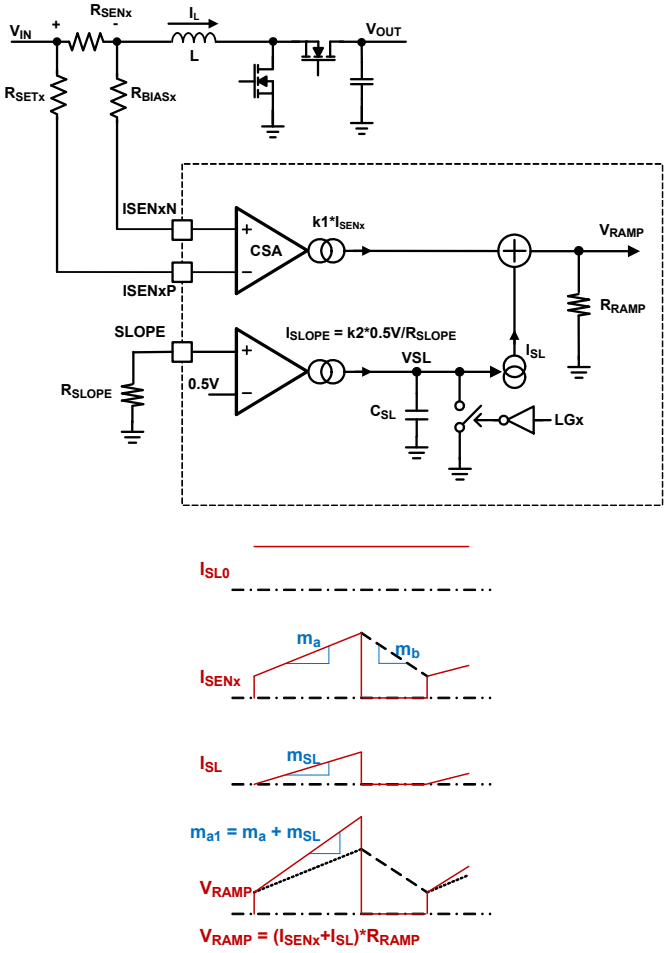


FIGURE 70. SLOPE COMPENSATION BLOCK DIAGRAM

Light-Load Efficiency Enhancement

For switching mode power supplies, the total loss is related to conduction loss and switching loss. At heavy load, the conduction loss dominates, while the switching loss dominates at light-load condition. Therefore, if a multiphase converter is running at a fixed phase number for the entire load range, the efficiency starts to drop significantly below a certain load current. The ISL78229 has selectable automatic phase dropping, cycle-by-cycle diode emulation and pulse skipping features to enhance the light-load efficiency. By observing the total input

current on-the-fly and dropping an active phase, the system can achieve optimized efficiency over the entire load range.

The phase dropping (PH_DROP) and Diode Emulation (DE) functions can be selected to be active or inactive by setting the DE/PHDRP pin. Refer to Table 2 for the 3 configuration modes.

1. When DE/PHDRP = V_{CC}, diode emulation function is enabled, and Phase Drop is disabled.
2. When DE/PHDRP = FLOAT, both diode emulation and phase drop functions are enabled.
3. When DE/PHDRP = GND, both diode emulation and phase drop functions are disabled. The part is set in Continuous Conduction Mode (CCM).

TABLE 2. CCM/DE/PH_DROP MODE SETTING (DE/PHDRP PIN)

MODE NUMBER (NAME)	DE/PHDRP PIN SETTING	DE MODE	PHASE-DROP MODE
1 (DE)	VCC	Enabled	Disabled
2 (DE+PH_DROP)	FLOAT	Enabled	Enabled
3 (CCM)	GND	Disabled	Disabled

AUTOMATIC PHASE DROPPING/ADDING

When the phase drop function is enabled, the ISL78229 automatically drops or adds Phase 2 by comparing the V_{IMON} to the phase dropping/adding thresholds. V_{IMON} is proportional to the average input current indicating the level of the load.

The phase dropping mode is **not allowed** with external synchronization.

Phase Dropping

When load current drops and V_{IMON} falls below 1.1V, Phase 2 is disabled. For better transient response during phase dropping, the ISL78229 gradually reduces the duty cycle of the phase from steady state to zero, typically within 8 to 10 switching cycles. This gradual dropping scheme helps smooth the change of the PWM signal and stabilize the system when phase dropping happens.

From Equations 13 and 14, the phase dropping current threshold level for the total 2-phase boost input current can be calculated by Equation 16.

$$I_{INphDRP} = \frac{\left(\frac{1.1}{R_{IMON}} - 17 \cdot 10^{-6}\right) \cdot 8 \cdot R_{SET}}{R_{SEN}} (A) \quad \text{(EQ. 16)}$$

Phase Adding

The phase adding is decided by two mechanisms listed as follows. Phase 2 is added immediately if either of the two following conditions are met.

1. V_{IMON} >1.15V, the IMON pin voltage is higher than phase adding threshold 1.15V. The phase adding current threshold level for the total 2-phase boost input current can be calculated by Equation 17.

$$I_{INphADD} = \frac{\left(\frac{1.15}{R_{IMON}} - 17 \cdot 10^{-6}\right) \cdot 8 \cdot R_{SET}}{R_{SEN}} (A) \quad \text{(EQ. 17)}$$

2. I_{SENx} >80µA (OC1), individual phase current triggers OC1.

The first is similar to the phase dropping scheme. When the load increases causing V_{IMON} >1.15V, Phase 2 is added back immediately to support the increased load demand. Because the IMON pin normally has large RC filter and V_{IMON} is average current signal, this mechanism has a slow response and is intended for slow load transients.

The second mechanism is intended to handle the case when load increases quickly. If the quick load increase triggers OC1 (I_{SENx} >80µA) in either of the 2 phases, Phase 2 is added back immediately.

After Phase 2 is added, the phase dropping function is disabled for 1.5ms. After this 1.5ms expires, the phase dropping circuit is activated again and Phase 2 can be dropped automatically as usual.

DIODE EMULATION AT LIGHT LOAD CONDITION

When the Diode Emulation mode (DE) is selected to be enabled (Mode 1 and 2 in Table 2), the ISL78229 has cycle-by-cycle diode emulation operation at light load achieving Discontinuous Conduction Mode (DCM) operation. With DE mode operation, negative current is prevented and the conduction loss is reduced, so high efficiency can be achieved at light load conditions.

Diode emulation occurs during t_5-t_8 (on Figure 67 on page 30), regardless of the DE/PHDRP operating modes (Table 2).

PULSE SKIPPING AT DEEP LIGHT-LOAD CONDITION

If the converter enters DE mode and the load is still reducing, eventually pulse skipping occurs to increase the deep light-load efficiency. Either Phase 1 or Phase 2, or both, are pulse skipping at these deep light-load conditions.

Fault Protections/Indications

The ISL78229 is implemented with comprehensive fault protections, the majority of which can be monitored and programmed using PMBus.

FAULTS/WARNINGS MANAGEABLE VIA PMBUS

Table 3 on page 41 summarizes the types of faults and warnings accessible from PMBus and the three related registers to monitor the fault status, enable/disable fault protecting reactions and program the desired type of fault responses (Hiccup or Latch-off). Refer to section "PMBus User Guide" starting on page 40 for more details of the commands related to fault management.

Fault Flag Register FAULT_STATUS (D0h) and SALERT Signal

When any of the faults in Table 3 on page 41 occurs, the corresponding bit of FAULT_STATUS register ("FAULT_STATUS (D0h)" on page 58) is set to 1 and the SALERT pin is pulled low, regardless if that type of fault is masked by the corresponding bit in the FAULT_MASK register.

The bits of the FAULT_STATUS register status are kept unchanged as long as PVCC/VCC and EN are HIGH. Even when the fault conditions are gone, the bit = 1 status is not automatically cleared/reset to 0 by the device itself.

Each individual bit or multiple bits can be cleared/reset to 0, but only by a Write command, a CLEAR_FAULTS command from the PMBus, or EN/POR recycling.

Refer to "FAULT_STATUS (D0h)" on page 58 for more details of this PMBus command, and Table 3 on page 41 for a fault-related registers summary.

SALERT Pin

The SALERT pin is an open-drain logic output and should be connected to VCC through a typical 10k resistor. When any bit of FAULT_STATUS register is set to 1, the SALERT pin is pulled low, regardless if that type of fault is masked by the corresponding bit in the FAULT_MASK register. The host is interrupted by SALERT signal and then inquires the ISL78229 using PMBus for information about the faults/warnings recorded in the FAULT_STATUS register, or any others to diagnose.

After the ISL78229 is enabled, during the part initializing time t_1 - t_4 (refer to Figure 67 on page 30) before soft-start, the SALERT pin is kept pulled low. If no faults (listed in Table 4 on page 41) occur during t_1 - t_4, the SALERT pin open-drain transistor is open at t_4 when soft-start begins and the pin voltage is pulled high by the external pull-up circuits. If any fault in Table 4 on page 41 occurs after the beginning of soft-start, the corresponding bit of the FAULT_STATUS register is set to 1 and the SALERT pin is pulled low.

The SALERT pin can be released to be pulled HIGH only when all the FAULT_STATUS register bits are 0.

Fault Mask Register FAULT_MASK (D1h)

When any of the faults in Table 4 on page 41 are detected, the device responds with either protecting actions (Hiccup or Latch-off) or by ignoring this fault depending on the corresponding bit setting of the FAULT_MASK register ("FAULT_MASK (D1h)" on page 59).

Each bit of this register controls one specific fault condition to be ignored or not (refer to the list in Table 4 on page 41). The bit values are defined as follows:

- Bit = 1 means to ignore, no protection action taken for the triggered fault, and the ISL78229 keeps its normal PWM switching and operations.
- Bit = 0 means to respond with protecting action to enter either Hiccup or Latch-off as the fault response as described in "Fault Response Register SET_FAULT_RESPONSE (D2h)".

The register FAULT_MASK has a default setting and can be programmed using the PMBus command "FAULT_MASK (D1h)" on page 59 to set a specific fault's protection response to be ignored or not. At default, the VOUT_UV fault is ignored with Bit [6] set to 1 as default.

Refer to PMBus command "FAULT_MASK (D1h)" on page 59 for details and Table 3 on page 41 for a fault related registers summary.

Fault Response Register SET_FAULT_RESPONSE (D2h)

The fault response for each type of fault protection (listed in Table 4 on page 41) can be programmed to be either Hiccup or Latch-off by setting the corresponding bit of the register SET_FAULT_RESPONSE (refer to PMBus command "SET_FAULT_RESPONSE (D2h)" on page 60 and Table 3 on page 41).

- When bit = 1, the fault protection response is Hiccup mode
- When bit = 0, the fault protection response is Latch-off mode

The default bit values are determined by the HIC/LATCH pin configuration as listed below. Each bit value can be changed using PMBus to set the respective bit of the fault response register (SET_FAULT_RESPONSE) at default:

- When the HIC/LATCH pin is pulled high (VCC), the fault response is Hiccup mode.
- When the HIC/LATCH pin is pulled low (GND), the fault response is Latch-off mode.

In Hiccup mode, the device stops switching when a fault condition is detected, and restarts from soft-start after 500ms (typical). This operation is repeated until fault conditions are completely removed.

In Latch-off mode, the device stops switching when a fault condition is detected, and PWM switching is kept off even after fault conditions are removed. In Latch-off status, the internal LDO is alive to keep PVCC, and PMBus interface is available for the user to monitor the type of fault triggered or other parameters. Toggle the EN pin or cycle VCC/PVCC below the POR threshold to restart the system.

Refer to the PMBus command "SET_FAULT_RESPONSE (D2h)" on page 60 for details and Table 3 on page 41 for a fault-related registers summary.

INPUT OVERVOLTAGE FAULT

As shown in Figure 3 on page 7, the ISL78229 monitors the VIN pin voltage divided by 48 (VIN/48) as the input voltage information. This fault detection is active at the beginning of soft-start (t_5 as shown in Figure 67 on page 30).

The VIN_OV comparator compares VIN/48 to 1.21V reference to detect if VIN_OV fault is triggered. Equivalently, when V_{IN} >58V (for 5µs), the VIN_OV fault event is triggered. The PGOOD pin is pulled low and the corresponding bit (VIN_OV, Bit [2]) in the FAULT_STATUS register ("Fault Flag Register FAULT_STATUS (D0h) and SALERT Signal" on page 34 and Table 3 on page 41) is set to 1 and the SALERT pin is pulled low.

At the same time the VIN_OV fault condition is triggered, because the VIN_OV fault protection response is enabled by default as the VOIN_OV bit (Bit [2]) is set 0 by default in the FAULT_MASK register (refer to "Fault Mask Register FAULT_MASK (D1h)" on page 35 and Table 3 on page 41), the ISL78229 responds with fault protection actions to shut down the PWM switching and enters either Hiccup or Latch-off mode as described in "Fault Response Register SET_FAULT_RESPONSE (D2h)" on page 35 and Table 3 on page 41.

The VIN_OV fault protection can be disabled by setting the VIN_OV bit (Bit [2]) in "Fault Mask Register FAULT_MASK (D1h)" on page 35 to 1 via PMBus. If disabled, there are no fault protection actions when VIN_OV fault is triggered, and the ISL78229 keeps PWM switching and normal operation.

Under the selection of VIN_OV fault protection activated with Hiccup response, when the output voltage falls down to be lower

than the VIN_OV threshold 58V, the device returns to normal switching through Hiccup soft-start. PGOOD is released to be pulled HIGH after a 0.5ms delay. As described in "Fault Flag Register FAULT_STATUS (D0h) and SALERT Signal" on page 34, the bit = 1 status in the FAULT_STATUS register is not automatically cleared/reset to 0 by the device itself and the SALERT pin is kept low. The bits in the FAULT_STATUS register can only be cleared to 0 by a Write command, or CLEAR_FAULTS command via PMBus, or EN/POR recycling. When all the bits in the FAULT_STATUS register are 0, the SALERT pin is released to be pulled HIGH.

OUTPUT UNDERVOLTAGE FAULT

The ISL78229 monitors the FB pin voltage to detect if an output undervoltage fault (VOUT_UV) occurs.

If the FB pin voltage is lower than 80% (default) of the voltage regulation reference VREF_DAC, the VOUT_UV comparator is triggered to indicate VOUT_UV fault and the PGOOD pin is pulled low. Also, corresponding bit (VOUT_UV, Bit [6]) in the FAULT_STATUS register ("Fault Flag Register FAULT_STATUS (D0h) and SALERT Signal" on page 34 and Table 3 on page 41) is set to 1 and the SALERT pin is pulled low.

When the output voltage rises back to be above the VOUT_UV threshold 80% VREF_DAC plus 4% hysteresis, PGOOD is released to be pulled HIGH after a 0.5ms delay. However, as described in the "Fault Flag Register FAULT_STATUS (D0h) and SALERT Signal" on page 34, the bit = 1 status in the FAULT_STATUS register is not automatically cleared/reset to 0 by the device itself and the SALERT pin is kept low. The bits in the FAULT_STATUS register can only be cleared to 0 by a Write command, a CLEAR_FAULTS command from PMBus, or EN/POR recycling. When all the bits in the FAULT_STATUS register are 0, the SALERT pin is released to be pulled HIGH.

The VOUT_UV fault protection response is disabled (ignored) by default as the VOUT_UV bit (Bit [6]) is set to 1 by default in the FAULT_MASK register (refer to "Fault Mask Register FAULT_MASK (D1h)" on page 35 and Table 3 on page 41), which means the ISL78229 keeps the PWM switching and normal operation when VOUT_UV fault occurs. VOUT_UV fault protection can be enabled by setting set this VOUT_UV bit (Bit [6]) to 0 in the "Fault Mask Register FAULT_MASK (D1h)" on page 35. If enabled, the fault response can be programmed to be either Hiccup or Latch-off as described in "Fault Response Register SET_FAULT_RESPONSE (D2h)" on page 35 and Table 3 on page 41.

The VOUT_UV threshold values can be set to eight options based on percentage of the reference VREF_DAC via PMBus command "VOUT_UV_FAULT_LIMIT (D4h)" on page 62.

OUTPUT OVERVOLTAGE FAULT

The ISL78229 monitors the FB pin voltage to detect if an output overvoltage fault (VOUT_OV) occurs. This fault detection is active at the beginning of soft-start (t_5 as shown in the Figure 67 on page 30).

If the FB pin voltage is higher than 120% (default) of the voltage regulation reference VREF_DAC, the VOUT_OV comparator is triggered to indicate a VOUT_OV fault, and the PGOOD pin is pulled low. The corresponding bit (VOUT_OV, Bit [7]) in the FAULT_STATUS register ("Fault Flag Register FAULT_STATUS (D0h) and SALERT Signal" on page 34 and Table 3 on page 41) is set to 1 and the SALERT pin is pulled low.

At the same time, when a VOUT_OV fault condition is triggered, because the VOUT_OV fault protection response is enabled by default as the VOUT_OV bit (Bit [7]) is set 0 by default in the FAULT_MASK register (refer to "Fault Mask Register FAULT_MASK (D1h)" on page 35 and Table 3 on page 41), the ISL78229 responds with fault protection actions to shut down the PWM switching and enters either Hiccup or Latch-off mode as described in "Fault Response Register SET_FAULT_RESPONSE (D2h)" on page 35 and Table 3 on page 41.

The VOUT_OV fault protection can be disabled by setting the VOUT_OV bit (Bit [7]) in "Fault Mask Register FAULT_MASK (D1h)" on page 35 to 1 via PMBus. If disabled, there are no fault protection actions when VOUT_OV fault is triggered, and the ISL78229 keeps PWM switching and normal operation.

Under the selection of VOUT_OV fault protection activated with Hiccup response, when the output voltage falls down to be lower than the VOUT_OV threshold 120% VREF_DAC minus 4% hysteresis, the device returns to normal switching through Hiccup soft-start. The PGOOD pin is released to be pulled HIGH after 0.5ms delay. However, as described in the "Fault Flag Register FAULT_STATUS (D0h) and SALERT Signal" on page 34, the bit = 1 status in the FAULT_STATUS register is not automatically cleared/reset to 0 by the device itself and the SALERT pin is kept low. The bits in the FAULT_STATUS register can only be cleared to 0 by a Write command, a CLEAR_FAULTS command from PMBus, or EN/POR recycling. When all the bits in the FAULT_STATUS register are 0, the SALERT pin is released to be pulled HIGH.

The VOUT_OV threshold values can be set to eight options based on percentage of the reference VREF_DAC using PMBus command "VOUT_OV_FAULT_LIMIT (D3h)" on page 61.

OVERCURRENT LIMITING AND FAULT PROTECTION

The ISL78229 has multiple levels of overcurrent protection. Each phase is protected from an overcurrent condition by limiting its peak current and the combined total current is protected on an average basis. Also, each phase is implemented with cycle-by-cycle negative current limiting (OC_NEG_TH = -48µA).

Peak Current Cycle-by-Cycle Limiting (OC1)

Each individual phase's inductor peak current is protected with cycle-by-cycle peak current limiting (OC1) **without** triggering Hiccup or Latch-off shutdown of the IC. The controller continuously compares the CSA output current sense signal I_{SENx} (calculated by Equation 11 on page 32) to an overcurrent limiting threshold (OC1_TH = 80µA) in every cycle. When I_{SENx} reaches 80µA, the respective phase's LGx is turned off to stop inductor current further ramping up. In this way, peak current cycle-by-cycle limiting is achieved.

The equivalent cycle-by-cycle peak inductor current limiting for OC1 can be calculated using Equation 18:

$$I_{OC1x} = 80 \cdot 10^{-6} \cdot \frac{R_{SETx}}{R_{SENx}}(A) \quad \text{(EQ. 18)}$$

Negative Current Cycle-by-Cycle Limiting (OC_NEG)

Each individual phase's inductor current is protected with cycle-by-cycle negative current limiting (OC_NEG) **without** triggering Hiccup or Latch-off shutdown of the IC. The controller continuously compares the CSA output current sense signal I_{SENx} (calculated by Equation 11 on page 32) to a negative current limiting threshold (OC_NEG_TH = -48µA) in every cycle. When I_{SENx} falls below -48µA, the respective phase's UGx is turned off to stop the inductor current further ramping down. In this way, negative current cycle-by-cycle limiting is achieved.

The equivalent negative inductor current limiting level can be calculated using Equation 19:

$$I_{OCNEGx} = -48 \cdot 10^{-6} \cdot \frac{R_{SETx}}{R_{SENx}}(A) \quad \text{(EQ. 19)}$$

Peak Overcurrent Fault (OC2_PEAK)

If either of the two individual phase's current sense signal I_{SENx} (calculated by Equation 11 on page 32) reaches 105µA (OC2_TH = 105µA) for three consecutive switching cycles, the Peak Overcurrent fault (OC2_PEAK) event is triggered. This fault protection protects the device by shutdown (Hiccup or Latch-off) from a worst case condition where OC1 cannot limit the inductor peak current.

This fault detection is active at the beginning of soft-start (t_5 as shown in the Figure 67 on page 30).

When an OC2_PEAK fault event is triggered, the corresponding bit (OC2_PEAK, Bit [5]) in the FAULT_STATUS register ("Fault Flag Register FAULT_STATUS (D0h) and SALERT Signal" on page 34 and Table 3 on page 41) is set to 1 and the SALERT pin is pulled low.

At the same time, when an OC2_PEAK fault event is triggered, because the OC2_PEAK fault protection response is enabled by default as the OC2_PEAK bit (Bit [5]) is set 0 by default in the FAULT_MASK register (refer to "Fault Mask Register FAULT_MASK (D1h)" on page 35 and Table 3 on page 41), the ISL78229 responds with fault protection actions to shut down the PWM switching and enters either Hiccup or Latch-off mode as described in "Fault Response Register SET_FAULT_RESPONSE (D2h)" on page 35 and Table 3 on page 41.

The OC2_PEAK fault protection can be disabled by setting the OC2_PEAK bit (Bit [5]) in "Fault Mask Register FAULT_MASK (D1h)" on page 35 to 1 via PMBus. If disabled, there are no fault protection actions when OC2_PEAK fault is triggered, and the ISL78229 keeps PWM switching and normal operation.

Under the selection of OC2_PEAK fault protection activated with Hiccup response, when both phases' peak current sense signal I_{SENx} no longer trip the OC2_PEAK thresholds (105µA), the device returns to normal switching and regulation through Hiccup soft-start. However, as described in the "Fault Flag Register FAULT_STATUS (D0h) and SALERT Signal" on page 34, the bit = 1 status in the FAULT_STATUS register is not automatically cleared/reset to 0 by the device itself and the SALERT pin is kept low. The bits in the FAULT_STATUS register can only be cleared to 0 by a Write command, a CLEAR_FAULTS command using PMBus, or EN/POR recycling. When all the bits in the FAULT_STATUS register are 0, the SALERT pin is released to be pulled HIGH.

The equivalent inductor peak current threshold for the OC2_PEAK fault protection can be calculated by Equation 20:

$$I_{OC2x} = 105 \cdot 10^{-6} \cdot \frac{R_{SETx}}{R_{SENx}}(A) \quad \text{(EQ. 20)}$$

Constant Current Control (CC)

A dedicated constant average Current Control (CC) loop is implemented in the ISL78229 to control the input current to be constant at overload conditions, which means constant input power limiting under a constant input voltage.

As shown in Figure 3 on page 7, the V_{IMON} represents the average input current and is sent to the error amplifier Gm2 input to be compared with the internal CC reference V_{REF_CC} (which is 1.6V as default and can be programmed to different values using the PMBus command "CC_LIMIT (D5h)" on page 63). The Gm2 output drives the COMP voltage through a diode D_{CC}. Thus, the COMP voltage can be controlled by either Gm1 output or Gm2 output through D_{CC}.

At normal operation without overloading, V_{IMON} is lower than the V_{REF_CC} (1.6V at default). Therefore, Gm2 output is HIGH and D_{CC} is blocked and not forward conducting. The COMP voltage is now controlled by the voltage loop error amplifier Gm1's output to have output voltage regulated.

In the input average current overloading case, when V_{IMON} reaches V_{REF_CC} (1.6V at default), the Gm2 output falls and D_{CC} is forward conducting, and the Gm2 output overrides the Gm1 output to drive COMP. In this way, the CC loop overrides the voltage loop, meaning V_{IMON} is controlled to be constant achieving average constant current operation. Under certain input voltages, the input CC makes input power constant for the boost converter. Compared to peak current limiting schemes, the average constant current control is more accurate to control the average current to be constant, which is beneficial for the user to accurately control the maximum average power for the converter to handle.

The CC current threshold should be set lower than the OC1 peak current threshold with margin. Generally, the OC1 peak current threshold (per phase) is set 1.5 to 2 times higher than the CC current threshold (referred to as per-phase average current). This matches with the physics of the power devices that normally have higher transient peak current rating and lower average current ratings. The OC1 provides protection against the transient peak current, which can be higher than the power devices can handle. The CC controls the average current with slower response, but with much more accurate control of the maximum power the system has to handle at overloading conditions.

1. When fast changing overloading occurs, because V_{IMON} has sensing delay of $R_{IMON}*C_{IMON}$, CC does not trip at the initial transient load current until it reaches the CC reference 1.6V (default). OC1 is triggered first to limit the inductor peak current cycle-by-cycle.
2. After the delay of $R_{IMON}*C_{IMON}$, when V_{IMON} reaches the CC reference 1.6V (default), the CC control starts to work and limit duty cycles to reduce the inductor current and keep the sum of the two phases' inductor currents being constant. The time constant of the $R_{IMON}*C_{IMON}$ is typically on the order of 10 times slower than the voltage loop bandwidth so that the two loops do not interfere with each other.

CC loop is active at the beginning of soft-start.

The CC threshold values can be set to eight options using the PMBus command "CC_LIMIT (D5h)" on page 63, which ranges from 1.25V to 1.6V with a default setting of 1.6V.

Average Overcurrent Fault (OC_AVG)

The ISL78229 monitors the IMON pin voltage (which represents the average current signal) to detect if an Average Overcurrent (OC_AVG) fault occurs. As shown in Figure 3 on page 7, the comparator CMP_OCAVG compares V_{IMON} to 2V (as default) threshold. This fault detection is active at the beginning of soft-start (t_5 as shown in Figure 67 on page 30).

When V_{IMON} is higher than 2V, the OC_AVG fault is triggered. The corresponding bit (OC_AVG, Bit [4]) in the FAULT_STATUS register ("Fault Flag Register FAULT_STATUS (D0h) and SALERT Signal" on page 34 and Table 3 on page 41) is set to 1 and the SALERT pin is pulled low.

The fault response at default is either Hiccup or Latch-off (as described in "Fault Response Register SET_FAULT_RESPONSE (D2h)" on page 35).

At the same time an OC_AVG fault condition is triggered, because the OC_AVG fault protection response is enabled by default as the OC_AVG bit (Bit [4]) is set 0 by default in the FAULT_MASK register (refer to "Fault Mask Register FAULT_MASK (D1h)" on page 35 and Table 3 on page 41), the ISL78229 responds with fault protection actions to shut down the PWM switching and enters either Hiccup or Latch-off mode as described in "Fault Response Register SET_FAULT_RESPONSE (D2h)" on page 35 and Table 3 on page 41.

The OC_AVG fault protection can be disabled by setting the OC_AVG bit (Bit [4]) in "Fault Mask Register FAULT_MASK (D1h)" on page 35 to 1 using PMBus. If disabled, there are no fault protection actions when OC_AVG fault is triggered and the device keeps PWM switching and normal operation.

Under the selection of OC_AVG fault protection activated with Hiccup response, when the IMON voltage falls below the 2V (default) threshold, the device returns to normal switching through Hiccup soft-start. As described in the "Fault Flag Register FAULT_STATUS (D0h) and SALERT Signal" on page 34, the bit = 1 status in the FAULT_STATUS register is not automatically cleared/reset to 0 by the device itself and the SALERT pin is kept low. The bits in the FAULT_STATUS register can only be cleared to 0 by a Write command, or CLEAR_FAULTS command via PMBus, or EN/POR recycling. When all the bits in the FAULT_STATUS register are 0, the SALERT pin is released to be pulled HIGH.

The OC_AVG fault threshold can be set to eight options using the PMBus command "OC_AVG_FAULT_LIMIT (D6h)" on page 64.

Because the Constant Current Loop uses the same IMON signal and has a lower threshold (1.6V default), which is lower than the OC_AVG threshold (2V default), the OC_AVG can be tripped. The CC loop limits the IMON signal around 1.6V and below 2V. Generally, OC_AVG functions as worst-case backup protection.

EXTERNAL TEMPERATURE MONITORING AND PROTECTION (NTC PIN)

The NTC pin allows temperature monitoring with a Negative Temperature Coefficient (NTC) thermistor connected from this pin to ground. An accurate 20µA current sourcing out of the NTC pin develops a voltage across the NTC thermistor, which can be converted to temperature in degrees Celsius due to the NTC thermistor characteristic. A precision resistor (100k, 0.1% for example) can be put in parallel with the NTC thermistor to linearize the voltage versus temperature ratio in certain ranges.

As an example, Figure 71 shows the curve of the NTC pin voltage versus the temperature for a 100k resistor in parallel with an NTC thermistor NTCS0805E3474FXT on the NTC pin. The user can read the NTC pin voltage over PMBus and convert the voltage to temperature using the curve in the chart.

In the board layout, the NTC resistor should be placed in the area that needs the temperature to be monitored. Typically the NTC is placed close to the power devices like MOSFETs to monitor the board temperature close to them.

The voltage on the NTC pin is monitored for over-temperature warnings (OT_NTC_WARN) and over-temperature faults (OT_NTC_FAULT), both flagged by SALERT. The default threshold for OT warnings is 450mV and the default threshold for OT faults is 300mV. Both thresholds can be changed to different values using the PMBus commands "OT_NTC_WARN_LIMIT (51h)" on page 51 and "OT_NTC_FAULT_LIMIT (4Fh)" on page 50.

If the NTC function is not used, the NTC pin should be connected to VCC.

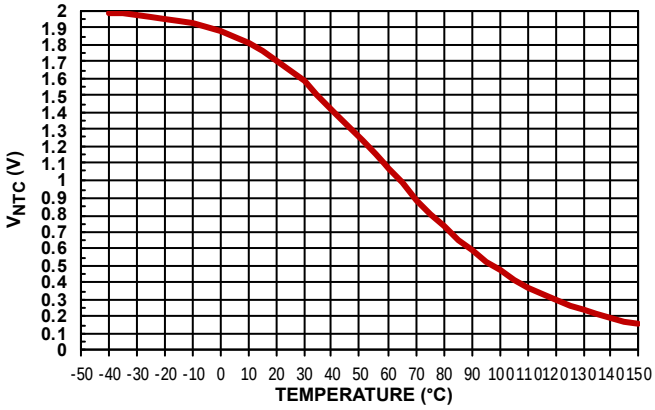


FIGURE 71. NTC VOLTAGE vs TEMPERATURE

External Over-Temperature Warning (OT_NTC_WARN)

If V_{NTC} is lower than 450mV (default as determined by OT_NTC_WARN_LIMIT register), the OT_NTC_WARN warning event is triggered. The corresponding bit (OT_NTC_WARN, Bit [1]) in the FAULT_STATUS register ("Fault Flag Register FAULT_STATUS (D0h) and SALERT Signal" on page 34 and Table 3 on page 41) is set to 1 and the SALERT pin is pulled low to deliver a warning to the host. The ISL78229 continues switching and regulating normally. There is no fault protection response when an OT_NTC_WARN event is triggered.

When the temperature drops and V_{NTC} rises above 450mV (default), the OT_NTC_WARN is no longer tripped. However, as described in the "Fault Flag Register FAULT_STATUS (D0h) and

SALERT Signal" on page 34, the bit = 1 status in the FAULT_STATUS register is not automatically cleared/reset to 0 by the device itself and the SALERT pin is kept low. The bits in the FAULT_STATUS register can only be cleared to 0 by a Write command, a CLEAR_FAULTS command from PMBus, or EN/POR recycling. When all the bits in the FAULT_STATUS register are 0, the SALERT pin is released to be pulled HIGH.

The OT_NTC_WARN threshold OT_NTC_WARN_LIMIT values can be set to different values via PMBus command "OT_NTC_WARN_LIMIT (51h)" on page 51.

This warning detection is active at the beginning of soft-start (t_5 as shown in Figure 67 on page 30).

External Over-Temperature Fault (OT_NTC_FAULT)

If V_{NTC} is lower than 300mV (default as determined by OT_NTC_FAULT_LIMIT register), the OT_NTC_FAULT fault event is triggered. The corresponding bit (OC_NTC_FAULT, Bit [3]) in the FAULT_STATUS register ("Fault Flag Register FAULT_STATUS (D0h) and SALERT Signal" on page 34 and Table 3 on page 41) is set to 1 and the SALERT pin is pulled low to deliver a warning to the host.

When the OT_NTC_FAULT fault condition is triggered, because the OT_NTC_FAULT fault protection response is disabled by default as the OT_NTC_FAULT bit (Bit [3]) is set to 1 by default in the FAULT_MASK register (refer to "Fault Mask Register FAULT_MASK (D1h)" on page 35 and Table 3 on page 41), the ISL78229 does not respond with fault protection actions and continues switching and regulating normally.

The OT_NTC_FAULT fault protection can be enabled by setting the OT_NTC_FAULT bit (Bit [3]) in "Fault Mask Register FAULT_MASK (D1h)" on page 35 to 0 via PMBus. If enabled, the ISL78229 responds with fault protection actions to shut down the PWM switching and enters either Hiccup or Latch-off mode as described in "Fault Response Register SET_FAULT_RESPONSE (D2h)" on page 35 and Table 3 on page 41.

Under the selection of OT_NTC_FAULT fault protection activated with a Hiccup response, when the temperature drops and V_{NTC} rises back to be above 300mV (default), the OT_NTC_FAULT is no longer tripped, and the device returns to normal switching through Hiccup soft-start. However, as described in the "Fault Flag Register FAULT_STATUS (D0h) and SALERT Signal" on page 34, the bit = 1 status in the FAULT_STATUS register is not automatically cleared/reset to 0 by the device itself and the SALERT pin is kept low. The bits in the FAULT_STATUS register can only be cleared to 0 by a Write command, a CLEAR_FAULTS command using PMBus, or EN/POR recycling. When all the bits in the FAULT_STATUS register are 0, the SALERT pin is released to be pulled HIGH.

The OT_NTC_FAULT threshold values can be set to different values using the PMBus command "OT_NTC_FAULT_LIMIT (4Fh)" on page 50.

This warning detection is active at the beginning of soft-start (t_5 as shown in the Figure 67 on page 30).

INTERNAL DIE OVER-TEMPERATURE PROTECTION

The ISL78229 PWM is disabled if the junction temperature reaches +160°C (typical) while the internal LDO is alive to keep PVCC/VCC biased (VCC connected to PVCC). A +15°C hysteresis ensures that the device restarts with soft-start when the junction temperature falls below +145°C (typical).

Internal 5.2V LDO

The ISL78229 has an internal LDO with an input at VIN and a fixed 5.2V/100mA output at PVCC. The internal LDO tolerates an input supply range of VIN up to 55V (60V absolute maximum). A 10µF, 10V or higher X7R type of ceramic capacitor is recommended between PVCC to GND. At low VIN operation when the internal LDO is saturated, the dropout voltage from the VIN pin to the PVCC pin is typically 0.3V under 80mA load at PVCC as shown in the "Electrical Specifications" table on page 9. This is one of the constraints to estimate the required minimum VIN voltage.

The output of this LDO is mainly used as the bias supply for the gate drivers. With VCC connected to PVCC as in the typical application, PVCC also supplies other internal circuitry. To provide a quiet power rail to the internal analog circuitry, it is recommended to place an RC filter between PVCC and VCC. A minimum of 1µF ceramic capacitor from VCC to ground should be used for noise decoupling purpose. Because PVCC provides noisy drive current, a small resistor (10Ω or smaller) between the PVCC and VCC helps to prevent the noises interfering from PVCC to VCC.

Figure 72 shows the internal LDO's output voltage (PVCC) regulation versus its output current. The PVCC drops to 4.5V (typical) when the load is 195mA (typical) because of the LDO current limiting circuits. When the load current further increases, the voltage drops further and finally enters current foldback mode where the output current is clamped to 100mA (typical). At the worst case when LDO output is shorted to ground, the LDO output is clamped to 100mA.

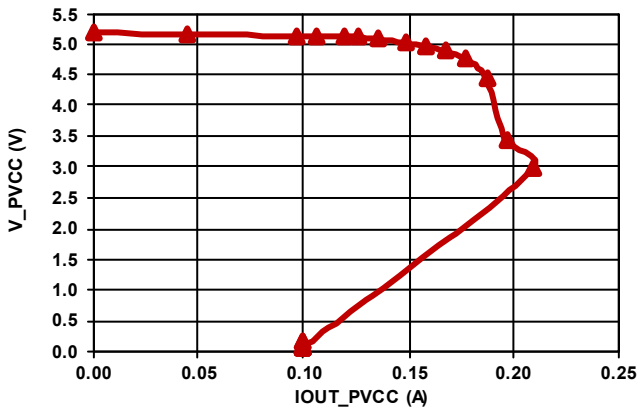


FIGURE 72. INTERNAL LDO OUTPUT VOLTAGE vs LOAD

Based on the junction to ambient thermal resistance R_{JA} of the package, the maximum junction temperature should be kept below +125°C. However, the power losses at the LDO need to be considered, especially when the gate drivers are driving external MOSFETs with large gate charges. At high V_{IN}, the LDO has significant power dissipation that may raise the junction temperature where the thermal shutdown occurs.

With an external PNP transistor as shown in Figure 73 on page 40, the power dissipation of the internal LDO can be moved from the ISL78229 to the external transistor. Choose R_S to be

68Ω so that the LDO delivers about 10mA when the external transistor begins to turn on. The external circuit increases the minimum input voltage to approximately 6.5V.

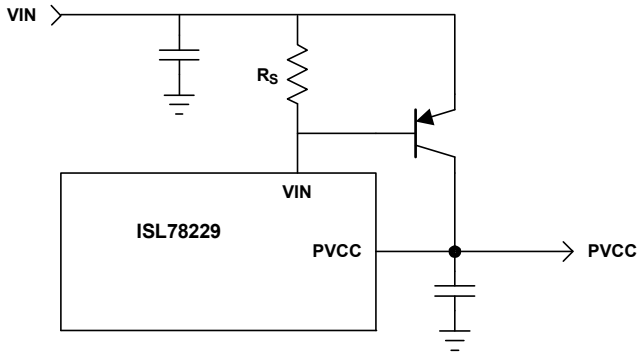


FIGURE 73. SUPPLEMENTING LDO CURRENT

PMBus User Guide

The ISL78229 is implemented with a PMBus digital interface for the user to monitor and change a few operating parameters, allowing smart control of the regulator.

The Power Management Bus (PMBus) is an open-standard digital power management protocol. It uses SMBus as its physical communication layer and includes support for the SMBus Alert (SALERT). In much the same way as SMBus defines the general means to manage portable power, PMBus defines the means to manage power subsystems.

PMBus and SMBus are I^2C derived bus standards that are generally electrically compatible with I^2C. They are more robust (Timeouts Force Bus Reset) and offer more features than I^2C, like SMBALERT(SALERT) line for interrupts, Packet Error Checking (PEC), and Host Notify Protocol.

The ISL78229 is compliant with the PMBus Power System Management Protocol Specification Part I and II version 1.2. These specification documents may be obtained from the website http://PMBus.org. These are required reading for complete understanding of the PMBus implementation.

- Specification Part I – General Requirements Transport and Electrical Interface - Includes the general requirements, as well as defines the transport and electrical interface and timing requirements of hardwired signals.
- Specification Part II – Command Language - Describes the operation of commands, data formats, and fault management, as well as defines the command language used with the PMBus.

Monitor Operating Parameters Through PMBus

A system controller can monitor several ISL78229 operating parameters through the PMBus interface including:

- Input voltage (monitors the VIN Pin)
- Output voltage (monitors the FB Pin)
- Input current (monitors the IMON Pin)
- External temperature (monitors the NTC Pin)

Monitor Faults and Configure Fault Responses

When any of the 10 fault conditions in Table 4 on page 41 occur, the corresponding bit of the FAULT_STATUS register is set to 1 and the SALERT pin is pulled low, regardless whether that type of fault is masked by the FAULT_MASK register. The PMBus host controller is interrupted by monitoring the SALERT pin and responds as follows:

- ISL78229 device pulls SALERT low.
- PMBus Host detects that SALERT is low, then performs transmission with Alert Response Address to find which device is pulling SALERT low.
- PMBus Host communicates with the device that is pulling SALERT low. The actions that the host performs next are up to the system designer.

Each individual bit of the FAULT_STATUS register can only be cleared to 0 by writing to that register using PMBus, by a CLEAR_FAULTS command, or POR recycle. When all the bits of FAULT_STATUS register are reset to 0, the SALERT pin is released to be pulled HIGH. Table 4 on page 41 lists the 10 types of faults that can be accessed through PMBus to:

- Monitor or reset/clear each individual bit of the FAULT_STATUS Register (D0h) for its corresponding fault's status.
- Configure the FAULT_MASK Register (D1h) to ignore or respond to each individual fault's protection.
- Configure the SET_FAULT_RESPONSE Register (D2h) to set each individual fault response to Hiccup or Latch-off.

Refer to "PMBus Command Detail" starting on page 46 for details on each specific PMBus command.

Set Operation/Fault Thresholds via PMBus

A system controller can change the ISL78229 operating parameters through the PMBus interface. Some of the commands include, but are not limited to:

- Enable or disable the PWM operation and regulation
- Set output voltage
- Set output voltage changing slew rate
- Set output overvoltage thresholds
- Set output undervoltage thresholds
- Set input constant current control thresholds

Accessible Timing for PMBus Registers Status

All PMBus command registers are set to default values during the part initialization period during t_2 - t_3 in Figure 67 on page 30. All the PMBus registers (commands) are ready to be accessed after this part initialization period.

After part start-up, as long as EN and PVCC/VCC is kept HIGH, all the PMBus registers values are accessible via the PMBus.

When the part is in Latch-off status or Hiccup mode triggered by any fault in Table 4 on page 41, the internal LDO is still enabled and keeps PVCC/VCC HIGH. All the PMBus register values are accessible using PMBus, and the FAULT_STATUS register values are accessible for the host to diagnose the type of fault.

Either EN low or PVCC/VCC falling below POR disables the ISL78229. All the registers are reset and are not accessible from PMBus.

TABLE 3. REGISTERS TO MONITOR FAULT STATUS AND CONFIGURE FAULT RESPONSE

COMMAND CODE	REGISTER NAME	FORMAT	ACCESS	DESCRIPTIONS	DEFAULT VALUE	REFER TO PAGE
D0h	FAULT_STATUS	Bit Field	R/W	0: No fault 1: Fault occurred	See Table 4	Page 58
D1h	FAULT_MASK	Bit Field	R/W	0: Hiccup or Latch-off fault response 1: Ignore fault with no protection response	See Table 4	Page 59
D2h	SET_FAULT_RESPONSE	Bit Field	R/W	0: Latch-off 1: Hiccup	See Table 4	Page 60

TABLE 4. FAULT NAMES LIST FOR THE REGISTERS (WITH DEFAULT VALUES) IN Table 3

FAULT NAME	BIT NUMBER	D0h DEFAULT VALUE	D1h DEFAULT VALUE	D2h DEFAULT VALUE SET BY HIC/LATCH PIN HIC/LATCH = GND: BITS [9:0] = 00000000 HIC/LATCH = VCC: BITS [9:0] = 11111111	RELATED FAULT TO BE MONITORED/CONTROLLED
CML	0	0	1	Set by the HIC/LATCH pin	Communications warning (for unsupported command, PEC error)
OT_NTC_WARN	1	0	0	Set by the HIC/LATCH pin	External over-temperature warning (NTC_PIN<450mV as default, threshold programmable)
VIN_OV	2	0	0	Set by the HIC/LATCH pin	Input overvoltage fault (VIN_PIN>58V)
OT_NTC_FAULT	3	0	1	Set by the HIC/LATCH pin	External over-temperature fault (NTC_PIN <300mV as default, threshold programmable)
OC_AVG	4	0	0	Set by the HIC/LATCH pin	Input average overcurrent fault (IMON_PIN >2V)
OC2_PEAK	5	0	0	Set by the HIC/LATCH pin	Peak overcurrent fault (I_{SENx} >105µA)
VOUT_UV	6	0	1	Set by the HIC/LATCH pin	Output undervoltage fault (FB_PIN <80% VREF_DAC as default, threshold programmable)
VOUT_OV	7	0	0	Set by the HIC/LATCH pin	Output overvoltage fault (FB_PIN >120% VREF_DAC as default, threshold programmable)
PLLCOMP_SHORT	8	0	0	Set by the HIC/LATCH pin	PLLCOMP PIN shorted to high potential voltages (PLLCOMP_PIN >1.7V)
PLL_LOCK	9	0	0	Set by the HIC/LATCH pin	PLL fault due to reaching minimum frequency (Detect the minimum frequency of 37kHz as typical)

Device Identification Address and Read/Write

The ISL78229 serves as a slave device on the PMBus. The 7-bit physical slave address can be set by the ADDR1 and ADDR2 pin configurations to have four address options. Table 5 defines the four available 7-bit addresses for the ISL78229 where Bits [7:3] are fixed and Bits [2:1] are determined by the ADDR1 and ADDR2 pin configurations. Bit [0] is a R/W bit to define the command to perform Read (Bit = 1) or Write (Bit = 0).

TABLE 5. SLAVE ADDRESS SET BY THE ADDR1 AND ADDR2 PIN CONFIGURATIONS

ADDR1/ADDR2 SETTING		DEVICE IDENTIFICATION -SLAVE ADDRESS BITS 7-1							R/W BIT BIT 0
ADDR1	ADDR2	BIT FIELD							
		7	6	5	4	3	2	1	0
GND	GND	1	0	0	1	1	0	0	Write: 0 Read: 1
GND	VCC	1	0	0	1	1	1	0	Write: 0 Read: 1
VCC	GND	1	0	0	1	1	0	1	Write: 0 Read: 1
VCC	VCC	1	0	0	1	1	1	1	Write: 0 Read: 1

PMBus Data Formats Used in ISL78229

The data formats used in the ISL78229 are listed below.

16-BIT LINEAR UNSIGNED (16LU)

16-bit Linear Unsigned (16Lu) data format is a two byte (16-bit) unsigned binary integer. For the ISL78229, the 16Lu data format performs the following actions:

Read the 16Lu Data to Report the 10-Bit ADC Input Voltage

The 16Lu data format is used in some commands to report the binary unsigned integer data at the 10-bit ADC output, where Bits [15:10] are not used. Bits [9:0] are used as equals to the 10-bit ADC output unsigned binary integer value. The input of the ADC is alternatively connected to voltages of NTC, FB, VIN/48, and IMON pins for monitoring.

The ADC has 2mV for 1 LSB, so the 16Lu data can report voltage ranges of 0V to 2.046V ($2mV*(2^{10-1})$).

Equation 21 can be used to convert the 16Lu data reported by the commands to ADC input voltage, where COMMAND is the 10-bit [9:0] unsigned binary integer value:

$$V_{ADCIN} = 0.002 \cdot COMMAND \quad \text{(EQ. 21)}$$

The 10-bit ADC accuracy from output to input has typical tolerances of -15mV to +25mV over the ADC input range of 0V to 2.046V.

Write/Read the 16Lu Data as the 8-Bit DAC Input

The 16Lu data format is used in the command "VOUT_COMMAND (21h)" on page 48 to set or read the 8-bit DAC input binary unsigned integer data which changes the DAC output voltage. The DAC output voltage is VREF_DAC, which is the reference to the output voltage regulation. In this command, the 8-bit [7:0] unsigned binary integer value are used and equal to the 8-bit DAC output binary integer value.

The DAC has 8mV for 1 LSB. So the 16Lu data can set VREF_DAC voltage range of 0V to 2.04V ($8mV*(2^{8-1})$).

Use Equation 22 to convert the 16Lu data written/read by the VOUT_COMMAND to DAC output voltage, where COMMAND is the 8-bit [7:0] unsigned binary integer value in the command:

$$V_{DACOUT} = 0.008 \cdot COMMAND = V_{REFDAC} \quad \text{(EQ. 22)}$$

Write/Read the 16Lu Data to Set NTC Threshold

The 16Lu data format is used in command "OT_NTC_FAULT_LIMIT (4Fh)" on page 50 and "OT_NTC_WARN_LIMIT (51h)" on page 51 to set the OT_NTC_WARN and OT_NTC_FAULT thresholds. The 10-bit [9:0] unsigned binary integer values are used and the 1 LSB represents 2mV.

Use Equation 23 to convert the 16Lu data in the OT_NTC_FAULT_LIMIT and OT_NTC_WARN_LIMIT commands to the voltage thresholds for the NTC pin, where COMMAND is the 10-bit [9:0] unsigned binary integer value in the command:

$$V_{OTNTC} = 0.002 \cdot COMMAND \quad \text{(EQ. 23)}$$

BIT FIELD (BIT)

The Bit Field is explained in "PMBus Command Detail" starting on page 46.

CUSTOM (CUS)

The Custom data format is explained in "PMBus Command Detail" starting on page 46. A combination of Bit Field and integer are common types of Custom data formats.

PMBus Command Summary

Table 6 lists all the command sets available for the ISL78229. Refer to "PMBus Command Detail" starting on page 46 for details about each specific PMBus command.

TABLE 6. PMBus COMMAND SUMMARY

COMMAND CODE	COMMAND NAME	ACCESS	NUMBER OF DATA BYTES	DATA FORMAT	DEFAULT SETTING	DESCRIPTIONS	REFER TO PAGE
01h	OPERATION	Read/Write Byte	1	BIT	80h	Enable/disable	page 46
03h	CLEAR_FAULTS	Send Byte	0	N/A	N/A	Clears any fault bits in the Fault_Status register that have been set	page 46
10h	WRITE_PROTECT	Read/Write Byte	1	BIT	00h	Protects against accidental changes	page 47
19h	CAPABILITY	Read Byte	1	BIT	B0h	Provides the way for a host system to determine some key capabilities of the ISL78229 as a PMBus device	page 47
21h	VOUT_COMMAND	Read/Write Word	2	16Lu	00C8h	Sets the nominal reference voltage for the V_{OUT} set-point, VREF_DAC = 1.6V as default	page 48
27h	VOUT_TRANSITION_RATE	Read/Write Word	2	BIT	0004h	Sets the V_{OUT} transition rate during VOUT_COMMAND commands to change V_{OUT}	page 49
4Fh	OT_NTC_FAULT_LIMIT	Read/Write Word	2	16Lu	0096h	Sets the over-temperature fault limit, NTC_PIN <300mV as default	page 50
51h	OT_NTC_WARN_LIMIT	Read/Write Word	2	16Lu	00E1h	Sets the over-temperature warning limit, NTC_PIN <450mV as default	page 51
88h	READ_VIN	Read Word	2	16Lu	N/A	Reports the input voltage measurement (VIN_PIN/48)	page 52
89h	READ_VOUT	Read Word	2	16Lu	N/A	Reports the FB pin voltage measurement, which is proportional to the output voltage	page 53
8Ch	READ_IIN	Read Word	2	16Lu	N/A	Renesas defined register. Reports the IMON pin voltage measurement which represents the total two phases' inductor average current which is the boost input current.	page 54
8Dh	READ_TEMPERATURE	Read Word	2	16Lu	N/A	Reports the NTC pin voltage measurement, which represents the temperature	page 55
98h	PMBUS_REVISION	Read Byte	1	BIT	22h	Reports the PMBus revision to which the ISL78229 is compliant. (PMBus Part I revision 1.2, Part II revision 1.2)	page 56
ADh	IC_DEVICE_ID	Read Word	2	CUS	8229h	Reports device identification information	page 56
AEh	IC_DEVICE_REV	Read Word	2	CUS	0C01h	Reports device revision information	page 57

TABLE 6. PMBus COMMAND SUMMARY (Continued)

COMMAND CODE	COMMAND NAME	ACCESS	NUMBER OF DATA BYTES	DATA FORMAT	DEFAULT SETTING	DESCRIPTIONS	REFER TO PAGE
D0h	FAULT_STATUS	Read/Write Word	2	BIT	0000h	Renesas defined register. Each bit's value records one specific fault or warning event (as listed below) being triggered or not. Bits [15:10]: Unused Bit [9]: PLL_LOCK fault Bit [8]: PLLCOMP_SHORT fault Bit [7]: VOUT_OV fault Bit [6]: VOUT_UV fault Bit [5]: OC2_IPEAK fault Bit [4]: OC_AVG fault Bit [3]: OT_NTC_FAULT fault Bit [2]: VIN_OV fault Bit [1]: OT_NTC_WARN warning Bit [0] CML warning FAULT_STATUS Bit = 1 stays unchanged until using a Write command to set Bit = 0, Write CLEAR FAULT command or POR cycle. FAULT_STATUS is not masked by FAULT_MASK register.	page 58
D1h	FAULT_MASK	Read/Write Word	2	BIT	0049h	Renesas defined register. Each bit controls one specific fault condition listed below to be masked (ignored) or not. Bits [15:10]: Not used Bit [9]: ignore PLL_LOCK fault Bit [8]: ignore PLLCOMP_SHORT fault Bit [7]: ignore VOUT_OV fault Bit [6]: ignore VOUT_UV fault Bit [5]: ignore OC2_IPEAK fault Bit [4]: ignore OC_AVG fault Bit [3]: ignore OT_NTC_FAULT fault Bit [2]: ignore VIN_OV fault Bit [1]: Not used Bit [0]: Not used Bit = 1 means to ignore, no protecting action taken by the device for the triggered fault, and the ISL78229 keeps its normal PWM switching and operations. Bit = 0 means to respond with protecting action to enter either Hiccup or Latch-off as fault response as described in "Fault Response Register SET_FAULT_RESPONSE (D2h)" on page 35.	page 59

TABLE 6. PMBus COMMAND SUMMARY (Continued)

COMMAND CODE	COMMAND NAME	ACCESS	NUMBER OF DATA BYTES	DATA FORMAT	DEFAULT SETTING	DESCRIPTIONS	REFER TO PAGE
D2h	SET_FAULT_RESPONSE	Read/Write Word	2	BIT	Set by the HIC/LATCH pin	Renesas defined register. Each bit [9:2] controls the respective type of the eight fault condition's responses as listed below. Bit = 1 sets the fault protection response to Hiccup mode. Bit = 0 sets the fault protection response to Latch-off mode. Bits [15:10]: Not used Bit [9]: PLL_LOCK fault Bit [8]: PLLCOMP_SHORT fault Bit [7]: VOUT_OV fault Bit [6]: VOUT_UV fault Bit [5]: OC2_IPEAK fault Bit [4]: OC_AVG fault Bit [3]: OT_NTC_FAULT fault Bit [2]: VIN_OV fault Bit [1]: Not used Bit [0]: Not used Bit = 1 means Hiccup mode Bit = 0 means Latch-off mode	page 60
D3h	VOUT_OV_FAULT_LIMIT	Read/Write Byte	1	BIT	06h	Renesas defined register. Set the output overvoltage fault threshold for the output voltage measured at the FB pin. Bits [7:3]: Not used Bits [2:0]: Valid bits	page 61
D4h	VOUT_UV_FAULT_LIMIT	Read/Write Byte	1	BIT	01h	Renesas defined register. Set the output undervoltage fault threshold for the output voltage measured at the FB pin. [7:3]: Not used; [2:0] Valid bits	page 62
D5h	CC_LIMIT	Read/Write Byte	1	BIT	07h	Renesas defined register. Set the constant current control threshold for the boost input current measured at the IMON pin. Bits [7:3]: Not used Bits [2:0]: Valid bits	page 63
D6h	OC_AVG_FAULT_LIMIT	Read/Write Byte	1	BIT	07h	Renesas defined register. Set the average overcurrent fault threshold for the boost input average current measured at the IMON pin. Bits [7:3]: Not used Bits [2:0]: Valid bits	page 64

PMBus Command Detail

OPERATION (01h)

Definition: Enables and disables the PWM regulating operation. Only Bits [7:6] are used for ISL78229. If Bits [7:6] are written to be 00b, the device turns off PWM regulation immediately. This command can also be monitored to read the operating state of the device on Bits [7:6]. The value read reflects the current state of the device.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 80h (Immediate off)

Units: N/A

COMMAND	OPERATION (01h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table							
Default Value	1	0	0	0	0	0	0	0

BITS 7:6	BITS 5:0 (NOT USED)	UNIT ON OR OFF
00	XXXXXX	Immediate off
10	XXXXXX	On, normal operation

CLEAR_FAULTS (03h)

Definition: Clears all fault bits that are set in the Fault_Status register and releases the SALERT pin (if asserted) simultaneously. If a fault condition still exists when the bit is cleared, the fault bit is set again immediately and the host notified by the SALERT pin. This command does not restart the ISL78229 that has latched off or been in Hiccup mode for a fault condition. It only clears the fault bits in the Fault_Status register and releases the SALERT pin.

This command is write only. There is no data byte for this command.

Data Length in Bytes: 0 Byte

Data Format: N/A

Type: Send Byte

Protectable: Yes

Default Value: N/A

Units: N/A

WRITE_PROTECT (10h)

Definition: Controls writing to the ISL78229. The intent of this command is to provide protection against accidental changes. This command is not intended to provide protection against deliberate changes to a device's configuration or operation. All supported commands may have their parameters read, regardless of the WRITE_PROTECT settings.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W Byte

Protectable: Yes

Default Value: 00h

Units: N/A

COMMAND	WRITE_PROTECT (10h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table							
Default Value	0	0	0	0	0	0	0	0

VALUE	DESCRIPTION
10000000	Disable all writes except to the WRITE_PROTECT command
01000000	Disable all writes except to the WRITE_PROTECT and OPERATION commands
00100000	Disable all writes except to the WRITE_PROTECT, OPERATION and VOUT_COMMAND commands
00000000	Enable writes to all commands

CAPABILITY (19h)

Definition: Provides the way for a host system to determine some key capabilities of the ISL78229.

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Protectable: N/A

Default Value: B0h

Units: N/A

COMMAND	CAPABILITY (19h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See following table							
Default Value	1	0	1	1	0	0	0	0

BIT NUMBER	DESCRIPTION	BIT VALUE	MEANING
7	Packet Error Checking	1	Packet Error Checking is supported
6:5	Maximum Bus Speed	01	Maximum supported bus speed is 400kHz
4	SMBALERT#	1	The device does have a SALERT# pin and does support the SMBus Alert Response protocol
3:0	Reserved	0000	Reserved

VOUT_COMMAND (21h)

Definition: Sets or reports VREF_DAC, which is the reference for the output voltage regulation as described in "Output Voltage Regulation Loop" on page 26.

The VOUT_COMMAND has two data bytes formatted as 16Lu ("Write/Read the 16Lu Data as the 8-Bit DAC Input" on page 42). Bits [15:8] are not used. The Bits [7:0] unsigned binary integer represents VREF_DAC value with 8mV LSB. Use Equation 22 on page 42 to convert the 16Lu data's 8-bit [7:0] unsigned binary integer to VREF_DAC, and use Equation 2 on page 26 to convert VREF_DAC to V_{OUT}.

Data Length in Bytes: 2

Data Format: 16Lu

Type: R/W

Protectable: Yes

Default Value: 00C8h. With 00C8h = 200(decimal) and 8mV/LSB, meaning V_{REFDAC} = 0.008 * 200 = 1.6V

Units: Volts

Equation: V_{REFDAC} = 0.008*VOUT_COMMAND as Equation 22 on page 42. Then use Equation 2 on page 26 to calculate V_{OUT}.

Range: 0V to 2.04V

Example: VOUT_COMMAND = 00C8h = 200(decimal), use Equation 22 on page 42, VREF_DAC = 0.008 * 200 = 1.6V

With R_{FB1} = 4.53kΩ and R_{FB2} = 97.6kΩ (Figure 4 on page 8), use Equation 2 on page 26 to get V_{OUT} = 36.07V

COMMAND	VOUT_COMMAND (21h)															
Format	16Lu															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table															
Default Value	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0

BIT NUMBER	MEANING
7:0	Sets/reads the VREF_DAC voltage
15:8	Not used

VOUT_TRANSITION_RATE (27h)

Definition: When the ISL78229 receives the VOUT_COMMAND that causes the VREF_DAC and eventually output voltage to change, this command sets the rate in mV/ms at which the VREF_DAC changes, and correspondingly sets the rate at which the output voltage changes. This commanded rate of change does not apply when the unit is commanded to turn on or to turn off.

The VOUT_TRANSITION_RATE command has two data bytes formatted in bit field as shown in the table below. Bits [15:3] are not used. Bits [2:0] define the transition rate of the VREF_DAC with default value of 0004h, meaning 200mV/ms for VREF_DAC transition rate (per table below), and eight options ranging from 12.5mV/ms to 1600mV/ms.

According to Equation 2 on page 26, Equation 24 below can be used to convert the V_{REFDAC} transition rate ($V_{REFDACTR}$) to the V_{OUT} transition rate (V_{OUTTR}), where R_{FB2} and R_{FB1} are resistor dividers from V_{OUT} to FB as shown in Figure 3 on page 7.

$$V_{OUTTR} = V_{REFDACTR} \cdot \left(1 + \frac{R_{FB2}}{R_{FB1}}\right) \quad \text{(EQ. 24)}$$

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 0004h, which equals to 0000_0100b, meaning 200mV/ms as for transition rate of VREF_DAC

Units: mV/ms (referred for V_{REFDAC} transition rate)

Equation: Use Equation 24 to convert the V_{REFDAC} transition rate ($V_{REFDACTR}$) to the V_{OUT} transition rate (V_{OUTTR}).

Range: 12.5mV/ms to 1600mV/ms for V_{REFDAC} transition rate

Example: VOUT_TRANSITION_RATE = 0003h = 0000_0000_0000_0011b sets the V_{REFDAC} transition rate to be 100mV/ms. Using Equation 24 with R_{FB1} = 4.53kΩ and R_{FB2} = 97.6kΩ (Figure 4 on page 8), the V_{OUT} transition rate (V_{OUTTR}) is calculated to be 2.25V/ms.

COMMAND	VOUT_TRANSITION_RATE (27h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

BITS 15:3 (NOT USED)	BITS 2:0	TRANSITION RATE OF VREF_DAC (mV/ms)
Not Used	000	12.5
Not Used	001	25
Not Used	010	50
Not Used	011	100
Not Used	100	200
Not Used	101	400
Not Used	110	800
Not Used	111	1600

OT_NTC_FAULT_LIMIT (4Fh)

Definition: Sets/reads the voltage threshold for the external over-temperature fault (OT_NTC_FAULT). As described in "External Temperature Monitoring and Protection (NTC Pin)" on page 38, the NTC pin voltage represents the temperature of the board (Figure 71 on page 38). The ISL78229 compares the NTC pin voltage V_{NTC} to a voltage threshold which is set by this OT_NTC_FAULT_LIMIT command to detect if the OT_NTC_FAULT occurs.

The OT_NTC_FAULT_LIMIT command has two data bytes formatted as 16Lu ("Write/Read the 16Lu Data to Set NTC Threshold" on page 42). Bits [15:10] are not used. Bits [9:0] are an unsigned binary integer value representing the voltage threshold for V_{NTC} with 2mV/LSB. The OT_NTC_FAULT_LIMIT has a default setting of 0096h, meaning 300mV threshold for V_{NTC}.

When V_{NTC} is lower than 300mV (default), the OT_NTC_FAULT event is triggered. For detailed descriptions of this fault, refer to "External Over-Temperature Fault (OT_NTC_FAULT)" on page 39, Table 3 on page 41 and the "PMBus Command Summary" on page 43 to deactivate this fault and configure the fault response.

To convert the voltage threshold to temperature threshold, refer to the specific V_{NTC} versus temperature characteristic curve (example Figure 71 on page 38) for each specific application setup.

Data Length in Bytes: 2

Data Format: 16Lu

Type: R/W

Protectable: Yes

Default Value: 0096h. With 0096h = 150(decimal) and 2mV/LSB, the OT_NTC_FAULT default threshold for V_{NTC} is 150 * 2mV = 300mV.

Units: mV (referred for voltage threshold for V_{NTC} with 2mV/LSB)

Equation: $V_{OT\_NTC\_FAULT\_LIMIT}$ = 0.002 * OT_NTC_FAULT_LIMIT as Equation 23 on page 42, where OT_NTC_FAULT_LIMIT is the 16Lu data in this command, and $V_{OT\_NTC\_FAULT\_LIMIT}$ refers to the OT_NTC_FAULT threshold for V_{NTC}

Range: 0V to 2.046V

COMMAND	OT_NTC_FAULT_LIMIT (4Fh)															
Format	16Lu															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table															
Default Value	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0

BIT NUMBER	MEANING
9:0	Sets/reads the voltage threshold for V_{NTC} as OT_NTC_FAULT fault detection with 2mV/LSB
15:10	Not used

OT_NTC_WARN_LIMIT (51h)

Definition: Sets/reads the voltage threshold for the external over-temperature warning (OT_NTC_WARN). As described in "External Temperature Monitoring and Protection (NTC Pin)" on page 38, the NTC pin voltage represents the temperature of the board (Figure 71 on page 38). The ISL78229 compares the NTC pin voltage V_{NTC} to a voltage threshold which is set by this OT_NTC_WARN_LIMIT command to detect if OT_NTC_WARN occurs.

The OT_NTC_WARN_LIMIT command has two data bytes formatted as 16Lu ("Write/Read the 16Lu Data to Set NTC Threshold" on page 42). Bits [15:10] are not used. Bits [9:0] are an unsigned binary integer value representing the voltage threshold for V_{NTC} with 2mV/LSB. The OT_NTC_WARN_LIMIT has default setting of 00E1h meaning 450mV threshold for V_{NTC}.

When V_{NTC} is lower than 450mV (default), the OT_NTC_WARN warning event is triggered. For detailed descriptions of this warning, refer to "External Over-Temperature Warning (OT_NTC_WARN)" on page 38.

To convert the voltage threshold for to temperature threshold, refer to the specific V_{NTC} versus temperature characteristic curve (example Figure 71 on page 38) for each specific application setup.

Data Length in Bytes: 2

Data Format: 16Lu

Type: R/W

Protectable: Yes

Default Value: 00E1h. With 00E1h = 225 (decimal) and 2mV/LSB, the OT_NTC_WARN default threshold for V_{NTC} is 225 * 2mV = 450mV.

Units: mV (referred for voltage threshold for V_{NTC} with 2mV/LSB)

Equation: $V_{OT\_NTC\_WARN\_LIMIT}$ = 0.002 * OT_NTC_WARN_LIMIT as Equation 23 on page 42, where OT_NTC_WARN_LIMIT is the 16Lu data in this command, and $V_{OT\_NTC\_WARN\_LIMIT}$ refers to the OT_NTC_WARN threshold for V_{NTC}

Range: 0V to 2.046V (referred for voltage threshold for V_{NTC} with 2mV/LSB)

COMMAND	OT_NTC_WARN_LIMIT (51h)															
Format	16Lu															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table															
Default Value	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	1

BIT NUMBER	MEANING
9:0	Sets/reads the voltage threshold for V_{NTC} as OT_NTC_WARN warning detection with 2mV/LSB
15:10	Not used

READ_VIN (88h)

Definition: Returns a voltage reading with the VIN/48 values (VIN pin voltage divided by 48).

The READ_VIN command has two data bytes formatted as 16Lu (refer to "Read the 16Lu Data to Report the 10-Bit ADC Input Voltage" on page 42), where Bits [15:10] are not used and Bits [9:0] are used. The Bits [9:0] unsigned binary integer value represents the VIN/48 voltage value with 2mV/LSB. According to Equation 21 on page 42, Equation 25 can be used to convert the 16Lu data (Bits [9:0] unsigned binary integer value, termed as COMMAND) in this command to input voltage at the VIN pin:

$$V_{IN} = 48 \cdot 0.002 \cdot COMMAND \quad \text{(EQ. 25)}$$

Data Length in Bytes: 2

Data Format: 16Lu

Type: Read Only

Protectable: N/A

Default Value: N/A

Units: Volts (referred for VIN/48 with 2mV/LSB, use Equation 25 get V_{OUT})

Equation: Equation 25

Range: 0V to 2.046V (referred for VIN/48 with 2mV/LSB)

Example: READ_VIN = 007Dh = 125(decimal), with 2mV/LSB and Equation 25, V_{IN} = 48 * 0.002 * 125 = 12V

COMMAND	READ_VIN (88h)															
Format	16Lu															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table															
Default Value	N/A															

BIT NUMBER	MEANING
9:0	Reports input voltage with value of VIN/48 with 2mV/LSB. Use Equation 25 to calculate the V_{IN}.
15:10	Not used

READ_VOUT (89h)

Definition: Returns the output voltage reading with the FB pin voltage values.

The READ_VIN command has two data bytes formatted as 16Lu (refer to "Read the 16Lu Data to Report the 10-Bit ADC Input Voltage" on page 42), where Bits [15:10] are not used and Bits [9:0] are used. The Bits [9:0] unsigned binary integer value represents the FB voltage value with 2mV/LSB.

Equation 26 can be used to convert the 16Lu data (Bits [9:0] unsigned binary integer value, termed as COMMAND) reported in this command to output voltage V_{FB}:

$$V_{FB} = 0.002 \cdot COMMAND \quad \text{(EQ. 26)}$$

According to Equation 2 on page 26, Equation 27 can be used to convert the 16Lu data (Bits [9:0] unsigned binary integer value, termed as COMMAND) reported in this command to output voltage V_{OUT}, where R_{FB2} and R_{FB1} are resistor dividers from V_{OUT} to FB as shown in Figure 4 on page 8:

$$V_{OUT} = \left(1 + \frac{R_{FB2}}{R_{FB1}}\right) \cdot 0.002 \cdot COMMAND \quad \text{(EQ. 27)}$$

Data Length in Bytes: 2

Data Format: 16Lu

Type: Read Only

Protectable: N/A

Default Value: N/A

Units: Volts (referred for V_{FB} with 2mV/LSB, use Equation 27 get V_{OUT})

Equation: Equation 26 to calculate V_{FB} and Equation 27 to calculate V_{OUT}

Range: 0V to 2.046V (referred for V_{FB} with 2mV/LSB)

Example: READ_VOUT = 0800h = 800(decimal).

Use Equation 26 to get V_{FB} = 0.002 * 800 = 1.6V.

With R_{FB1} = 4.53kΩ and R_{FB2} = 97.6kΩ, use Equation 27 to get V_{OUT} = (1 + 97.6/4.53) * 0.002 * 800 = 36.072V.

COMMAND	READ_VOUT (89h)															
Format	16Lu															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table															
Default Value	N/A															

BIT NUMBER	MEANING
9:0	Reports the output voltage with value of the FB pin voltage with 2mV/LSB. Use Equation 26 to calculate V_{FB}, and Equation 27 to calculate the corresponding V_{OUT}.
15:10	Not used

READ_IIN (8Ch)

Definition: Returns input current information with the IMON pin voltage value (V_{IMON}), which represents the 2-phase boost total input average current I_{IN} as described in "Average Current Sense for 2 Phases - IMON" on page 32.

The READ_IIN command has two data bytes formatted as 16Lu (refer to "Read the 16Lu Data to Report the 10-Bit ADC Input Voltage" on page 42), where Bits [15:10] are not used and Bits [9:0] are used. The Bits [9:0] unsigned binary integer value represents the IMON voltage value with 2mV/LSB.

Equation 28 can be used to convert the 16Lu data (Bits [9:0] unsigned binary integer value, termed as COMMAND) reported in this command to V_{IMON}:

$$V_{IMON} = 0.002 \cdot COMMAND \quad \text{(EQ. 28)}$$

According to Equations 13 and 14, Equation 29 can be used to convert the 16Lu data (Bits [9:0] unsigned binary integer value, termed as COMMAND) reported in this command to the total 2-phase current value as the boost input current I_{IN}, where R_{SEN}, R_{SET} and R_{IMON} are described in "Current Sense" on page 32:

$$I_{IN} = \frac{\left(\frac{COMMAND \cdot 0.002}{R_{IMON}} - 17 \cdot 10^{-6}\right) \cdot 8 \cdot R_{SET}}{R_{SEN}} \quad \text{(EQ. 29)}$$

Data Length in Bytes: 2

Data Format: 16Lu

Type: Read Only

Protectable: N/A

Default Value: N/A

Units: Volts (referred for V_{IMON} with 2mV/LSB. Use Equation 29 get I_{IN}, which has unit "A")

Equation: Equation 28 to calculate V_{IMON} and Equation 29 to calculate I_{IN}

Range: 0V to 2.046V (referred for V_{IMON} with 2mV/LSB)

Example: READ_IIN = 0800h = 800(decimal).

Use Equation 28 to get V_{IMON} = 0.002 * 800 = 1.6V.

With R_{SEN} = 1mΩ, R_{SET} = 483.1Ω and R_{IMON} = 57.6kΩ, use Equation 29 to get I_{IN} = 41.65A.

COMMAND	READ_IIN (8Ch)															
Format	16Lu															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table															
Default Value	N/A															

BIT NUMBER	MEANING
9:0	Reports the total 2-phase boost input average current information with value of the IMON pin voltage with 2mV/LSB. Use Equation 28 to calculate V_{IMON}, and Equation 29 to calculate the total 2-phase boost input average current I_{IN}.
15:10	Not used

READ_TEMPERATURE (8Dh)

Definition: Returns temperature information with the NTC pin voltage value (V_{NTC}), which represents the temperature of the board spot where the NTC resistor is placed (refer to "External Temperature Monitoring and Protection (NTC Pin)" on page 38).

The READ_TEMPERATURE command has two data bytes formatted as 16Lu (refer to "Read the 16Lu Data to Report the 10-Bit ADC Input Voltage" on page 42), where Bits [15:10] are not used and Bits [9:0] are used. The Bits [9:0] unsigned binary integer value represents the VNTC voltage value with 2mV/LSB.

Equation 30 can be used to convert the 16Lu data (Bits [9:0] unsigned binary integer value, termed as COMMAND) reported in this command to V_{NTC}:

$$V_{NTC} = 0.002 \cdot COMMAND \quad \text{(EQ. 30)}$$

To convert the V_{NTC} voltage to temperature, refer to the specific V_{NTC} versus temperature characteristic curve (example Figure 71 on page 38) for each specific application setup.

Data Length in Bytes: 2

Data Format: 16Lu

Type: Read Only

Protectable: N/A

Default Value: N/A

Units: Volts (referred for V_{NTC} with 2mV/LSB)

Equation: Equation 30 to calculate V_{NTC}. Use the specific V_{NTC} versus temperature characteristic curve such as Figure 71 on page 38 for the specific setup to convert $_{NTC}$ to temperature.

Range: 0V to 2.046V (referred for V_{NTC} with 2mV/LSB)

Example: READ_TEMPERATURE = 00E1h = 225(decimal), with 2mV/LSB, use Equation 30 to get V_{NTC} = 225 * 2mV = 450mV.

If V_{NTC} versus temperature characteristic curve is Figure 71 on page 38, the temperature is around 102°C reading from the figure.

COMMAND	READ_TEMPERATURE (8Dh)															
Format	16Lu															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table															
Default Value	N/A															

BIT NUMBER	MEANING
9:0	Reports the temperature information with value of the NTC pin voltage and with 2mV/LSB. Use Equation 30 to calculate the NTC pin voltage V_{NTC}. Use the specific V_{NTC} versus temperature characteristic curve to convert V_{NTC} to temperature.
15:10	Not used

PMBUS_REVISION (98h)

Definition: Returns the revision of the PMBus Specification to which the device is compliant.

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Protectable: N/A

Default Value: 22h (Part 1 Revision 1.2, Part 2 Revision 1.2)

Units: N/A

COMMAND	PMBUS_REVISION (98h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See following table							
Default Value	0	0	1	0	0	0	1	0

BITS 7:4	PART 1 REVISION	BITS 3:0	PART 2 REVISION
0000	1.0	0000	1.0
0001	1.1	0001	1.1
0010	1.2	0010	1.2

IC_DEVICE_ID (ADh)

Definition: Reports device identification information. For the ISL78229, this command is normal Read, and it returns the binary unsigned integer data with values correlating to the ISL78229 part number.

Data Length in Bytes: 2

Data Format: CUS

Type: Read Only

Protectable: N/A

Default Value: 8229h, which correlates to the ISL78229 part number

Units: N/A

COMMAND	IC_DEVICE_ID (ADh)															
Format	CUS															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Returns IC ID as part number “8229h”															
Default Value	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	1

IC_DEVICE_REV (AEh)

Definition: Reports device revision information. For the ISL78229, this command is normal Read, and it returns the binary unsigned integer data with values correlating to the revision 0C01h.

Data Length in Bytes: 2

Data Format: CUS

Type: Read Only

Protectable: No

Default Value: 0C01h (Initial Release)

Units: N/A

COMMAND	IC_DEVICE_REV (AEh)															
Format	CUS															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Returns IC Revision information as “0C01h”															
Default Value	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1

FAULT_STATUS (D0h)

Definition: Renesas defined register. Reports if a specific fault condition has ever been triggered. Each bit represents one specific fault condition (listed in the table below).

The bit value meanings are defined as follows:

- Bit = 1 means this fault occurred
- Bit = 0 means this fault did not occur.

Bits [9:2] control a total of eight fault conditions. Bits [15:10] and Bits [1:0] are not used.

For more descriptions about this command and related commands, refer to "Fault Flag Register FAULT_STATUS (D0h) and SALERT Signal" on page 34 and Table 3 on page 41.

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 0000h

Units: N/A

COMMAND	FAULT_STATUS (D0h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	FAULT NAME	DEFAULT VALUE	MEANING
0	CML	0	Communications warning (for unsupported command, PEC error)
1	OT_NTC_WARN	0	External over-temperature warning (NTC_PIN <450mV as default, threshold programmable)
2	VIN_OV	0	Input overvoltage fault (VIN_PIN >58V)
3	OT_NTC_FAULT	0	External over-temperature fault (NTC_PIN <300mV as default, threshold programmable)
4	OC_AVG	0	Input average overcurrent fault (IMON_PIN >2V as default, threshold programmable)
5	OC2_PEAK	0	Per phase peak overcurrent fault (I_{SENx} >105µA)
6	VOUT_UV	0	Output undervoltage fault (FB_PIN <80% VREF_DAC as default, threshold programmable)
7	VOUT_OV	0	Output overvoltage fault (FB_PIN >120% VREF_DAC as default, threshold programmable)
8	PLLCOMP_SHORT	0	PLLCOMP pin shorted to high potential voltages (PLLCOMP_PIN >1.7V)
9	PLL_LOCK	0	PLL fault due to reaching the minimum frequency (detects the minimum frequency of 37kHz as typical)
15:10	Not used	000000	Not used

FAULT_MASK (D1h)

Definition: Renesas defined register. Sets any specific fault protection to be masked (ignored) or not. Each bit controls one specific fault condition (listed in the table below) to be ignored or not. With any bit's value setting to 1, the corresponding fault is masked (ignored), which means there is no fault protecting action taken by the device when that fault is triggered, and the ISL78229 keeps its normal PWM switching and operations.

The bit values meanings are defined as follows:

- Bit = 1 means to ignore, no action taken as fault response.
- Bit = 0 means to respond with protecting action, with part enter either hiccup or latch-off as fault response as described in the "Fault Response Register SET_FAULT_RESPONSE (D2h)" on page 35.

Bits [9:2] control total of eight fault conditions. Bits [15:10] and Bits [1:0] are not used.

At default, the VOUT_UV fault is ignored with Bit [6] setting to 1 as default.

Also, refer to Table 3 on page 41 for fault related registers summary.

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 0049h

Units: N/A

COMMAND	FAULT_MASK (D1h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table															
Default Value	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1

BIT NUMBER	FAULT NAME	DEFAULT VALUE	MEANING
0	N/A	1	Reserved
1	N/A	0	Reserved
2	VIN_OV	0	Ignore input overvoltage fault (VIN_PIN >58V)
3	OT_NTC_FAULT	1	Ignore external over-temperature fault (NTC_PIN <300mV as default, threshold programmable)
4	OC_AVG	0	Ignore input average overcurrent fault (IMON_PIN >2V)
5	OC2_PEAK	0	Ignore peak overcurrent fault (I_{SENx} >105µA)
6	VOUT_UV	1	Ignore output undervoltage fault (FB_PIN <80% VREF_DAC as default, threshold programmable)
7	VOUT_OV	0	Ignore output overvoltage fault (FB_PIN >120% VREF_DAC as default, threshold programmable)
8	PLLCOMP_SHORT	0	Ignore PLLCOMP pin shorted to high potential voltages (PLLCOMP_PIN >1.7V)
9	PLL_LOCK	0	Ignore PLL fault due to reaching the minimum frequency (detects the minimum frequency of 37kHz as typical)
15:10	Not used	000000	Not used

SET_FAULT_RESPONSE (D2h)

Definition: Sets/reads the fault protection response which is either Hiccup or Latch-off determined by the corresponding bit of SET_FAULT_RESPONSE register. The default value of the SET_FAULT_RESPONSE register is determined by the HIC/LATCH pin configurations.

- When HIC/LATCH pin is pulled high (VCC), each of Bits [9:0] is set to 1 as default
- When the HIC/LATCH pin is pulled low (GND), each of Bits [9:0] is set to 0 as default
- When bit = 1, the fault protection response is Hiccup mode
- When bit = 0, the fault protection response is Latch-off mode

In Hiccup mode, the device stops switching when a fault condition is detected, and restarts from soft-start after 500ms (typical). This operation is repeated until fault conditions are completely removed.

In Latch-off mode, the device stops switching when a fault condition is detected and PWM switching disabled even after fault conditions are removed. In Latch-off status, the internal LDO is active to maintain PVCC voltage, and PMBus interface is accessible for user to monitor the type of fault triggered or other parameters. By either toggling the EN pin or cycling VCC/PVCC below the POR threshold restarts the system.

For related descriptions, refer to "Fault Response Register SET_FAULT_RESPONSE (D2h)" on page 35, and Table 3 on page 41 for some fault related registers summary.

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: Set by the HIC/LATCH pin. 03FFh when HIC/LATCH = VCC; 0000h when HIC/LATCH = GND.

Units: N/A

COMMAND	SET_FAULT_RESPOSE (D2h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table															
Default Value (HIC/LATCH = VCC)	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
Default Value (HIC/LATCH = GND)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	FAULT NAME	DEFAULT VALUE	MEANING
0	Not used	Set by the HIC/LATCH pin	Not used
1	Not used	Set by the HIC/LATCH pin	Not used
2	VIN_OV	Set by the HIC/LATCH pin	Input overvoltage fault (VIN_PIN >58V) protection response is Hiccup when bit = 1, and Latch-off when bit = 0
3	OT_NTC_FAULT	Set by the HIC/LATCH pin	NTC over-temperature fault (NTC_PIN <300mV as default, threshold programmable) protection response is Hiccup when bit = 1, and Latch-off when bit = 0
4	OC_AVG	Set by the HIC/LATCH pin	Input average overcurrent fault (IMON_PIN >2V) protection response is Hiccup when bit = 1, and Latch-off when bit = 0
5	OC2_PEAK	Set by the HIC/LATCH pin	Peak overcurrent fault (I_{SENx} >105µA) protection response is Hiccup when bit = 1, and Latch-off when bit = 0
6	VOUT_UV	Set by the HIC/LATCH pin	Output undervoltage fault (FB_PIN <80% VREF_DAC as default, threshold programmable) protection response is Hiccup when bit = 1, and Latch-off when bit = 0
7	VOUT_OV	Set by the HIC/LATCH pin	Output overvoltage fault (FB_PIN >120% VREF_DAC as default, threshold programmable) protection response is Hiccup when bit = 1, and Latch-off when bit = 0

BIT NUMBER	FAULT NAME	DEFAULT VALUE	MEANING
8	PLLCOMP_SHORT	Set by the HIC/LATCH pin	PLLCOMP_SHORT fault (PLLCOMP_PIN >1.7V) protection response is Hiccup when bit = 1, and Latch-off when bit = 0
9	PLL_LOCK	Set by the HIC/LATCH pin	PLL loop fault (detect the minimum frequency of 37kHz as typical) protection response is Hiccup when bit = 1, and Latch-off when bit = 0
15:10	Not used	000000	Not used

VOUT_OV_FAULT_LIMIT (D3h)

Definition: Sets/reads the output overvoltage fault threshold. The output overvoltage fault is generated by a comparator comparing the FB pin voltage with VOUT_OV threshold which has setting options based on percentage of the VREF_DAC reference voltage. This command set OV threshold with eight options ranging from 105% to 125% of the reference voltage VREF_DAC. The default is set at 120% of VREF_DAC.

Equivalently the V_{OUT} overvoltage threshold is set at the same percentage of V_{OUT} target voltage (set by VREF_DAC) because the device uses the same FB voltage to regulate the output voltage with the same resistor divider between V_{OUT} and the FB pin. For example, at default, the V_{OUT} overvoltage threshold is set at 120% of V_{OUT_TARGET}. According to Equation 2 on page 26, the default V_{OUT} overvoltage threshold can be calculated using Equation 31. Other threshold options can be calculated using Equation 31 with 1.2 replaced with other percentage options.

$$VOUT_{OVdefault} = 1.2 \cdot V_{REFDAC} \cdot \left(1 + \frac{R_{FB2}}{R_{FB1}}\right) \quad \text{(EQ. 31)}$$

This fault detection is active at the beginning of soft-start (t_5 as shown in Figure 67 on page 30).

When an OV fault occurs, the corresponding bit in the FAULT_STATUS register is set to 1 and the SALERT pin is pulled low. The OV fault protection response is by default active and the fault response is either Hiccup or Latch-off determined by the corresponding bit of FAULT_RESPONSE register of which default value is determined by the HIC/LATCH pin.

For related description, refer to "Output Overvoltage Fault" on page 36, Table 3 on page 41 and the "PMBus Command Summary" on page 43 to deactivate this fault and configure the fault response.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 06h, which equals to 0000_0110b, meaning 120% of VREF_DAC

Units: %

COMMAND	OVP_SET (D3h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table							
Default Value	0	0	0	0	0	1	1	0

BITS 7:3 (NOT USED)	BITS 2:0	PERCENTAGE OF VREF_DAC (%)
Not Used	000	105
Not Used	001	107.5
Not Used	010	110
Not Used	011	112.5
Not Used	100	115
Not Used	101	117.5
Not Used	110	120
Not Used	111	125

VOUT_UV_FAULT_LIMIT (D4h)

Definition: Sets/reads the output undervoltage fault threshold. The output undervoltage fault is generated by a comparator comparing the FB pin voltage with VOUT_UV threshold which has setting options based on percentage of the VREF_DAC reference voltage. This command sets the UV threshold with eight options ranging from 75% to 95% of the reference voltage VREF_DAC. The default is set at 80% of VREF_DAC.

Equivalently, the V_{OUT} undervoltage threshold is set at the same percentage of V_{OUT} target voltage (set by VREF_DAC) because the device uses the same FB voltage to regulate the output voltage with the same resistor divider between V_{OUT} and the FB pin. For example, at default, the V_{OUT} undervoltage threshold is set at 80% of V_{OUT_TARGET}. According to Equation 2 on page 26, the default V_{OUT} undervoltage threshold can be calculated using Equation 32. Other threshold options can be calculated using Equation 32 with 0.8 replaced with other percentage options.

$$VOUT_{UV} = COMMAND \cdot V_{REFDAC} \cdot \left(1 + \frac{R_{FB2}}{R_{FB1}}\right) \quad \text{(EQ. 32)}$$

This fault is masked before soft-start completes (t_9 as shown in Figure 67 on page 30), or when the device is disabled.

During normal operation after soft-start completes and part is enabled, when a UV fault occurs, the corresponding bit in FAULT_STATUS register is set to 1 and the SALERT pin is pulled low. However, this UV fault protection response is masked by the FAULT_MASK register by default.

For related descriptions and command details, refer to "Output Undervoltage Fault" on page 36, Table 3 on page 41 and "PMBus Command Summary" on page 43.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 01h, which equals to 0000_0001b, meaning 80% of VREF_DAC

Units: V (referred for the VOUT_UV threshold V_{OUT_UV} calculated by Equation 32)

COMMAND	UVP_SET (D4h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table							
Default Value	0	0	0	0	0	0	0	1

BITS 7:3 (NOT USED)	BITS 2:0	PERCENTAGE OF VREF_DAC (%)
Not Used	000	75
Not Used	001	80
Not Used	010	82.5
Not Used	011	85
Not Used	100	87.5
Not Used	101	90
Not Used	110	92.5
Not Used	111	95

CC_LIMIT (D5h)

Definition: Sets/reads the reference voltage V_{REF_CC} for constant current control loop described in "Constant Current Control (CC)" on page 37. At overloading condition when constant current control loop is working, the V_{IMON} is controlled to be equal to the 1.6V reference (V_{REF_CC}) by default. Because V_{IMON} represents the boost total input average current I_{IN} as described in "Average Current Sense for 2 Phases - IMON" on page 32, the I_{IN} is controlled to be constant by the CC loop.

This command can set CC reference to 8 options ranging from 1.25V to 1.6V with default setting of 1.6V.

From Equations 13 and 14, Equation 33 can be derived to convert the eight CC reference options in below table (as V_{IMON} in the equation) to the actual total boost input current thresholds for CC, where COMMAND in the equation is the voltage options (CC_LIMIT Reference Voltage) in the command table shown in following.

$$I_{IN} = \left(\frac{COMMAND}{R_{IMON}} - 17 \cdot 10^{-6}\right) \cdot \frac{R_{SET}}{R_{SEN}} \cdot 8 \qquad \text{(EQ. 33)}$$

For related descriptions, refer to "Constant Current Control (CC)" on page 37.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 07h, which equals to 0000_0111b, meaning V_{REF_CC} = 1.6V (per table) for V_{IMON} to follow at CC control.

Units:

V (referred for the reference voltage V_{REF_CC} for V_{IMON} to follow);

A (referred for the boost average input current converted by Equation 33)

COMMAND	CC_LIMIT (D5h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table							
Default Value	0	0	0	0	0	1	1	1

BITS 7:3 (NOT USED)	BITS 2:0	CC REFERENCE VOLTAGE V_{REF_CC} (V)
Not Used	000	1.25
Not Used	001	1.3
Not Used	010	1.35
Not Used	011	1.4
Not Used	100	1.45
Not Used	101	1.5
Not Used	110	1.55
Not Used	111	1.6

OC_AVG_FAULT_LIMIT (D6h)

Definition: Sets/reads the input average overcurrent fault threshold. The input average overcurrent fault is generated by a comparator comparing the IMON pin voltage with 2V threshold as default. This command sets the OC_AVG fault threshold with eight options ranging from 1V to 2V. The default is set at 07h meaning 2V for V_{IMON}.

Use Equation 33 to convert the OC_AVG fault thresholds in following table to the actual total boost input average current protection thresholds.

This fault detection is active at the beginning of soft-start (t_5 as shown in Figure 67 on page 30).

When an OC_AVG fault occurs, the corresponding bit in the FAULT_STATUS register is set to 1 and the SALERT pin is pulled low. The OC_AVG fault protection is by default active and the fault response is either Hiccup or Latch-off determined by the corresponding bit of FAULT_RESPONSE register of which default value is determined by the HIC/LATCH pin.

For related description, refer to "Average Overcurrent Fault (OC_AVG)" on page 38, Table 3 on page 41, and the related commands in "PMBus Command Summary" on page 43 to deactivate this fault and configure the fault response.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 07h, which equals to 0000_0111b, meaning 2V threshold for the IMON pin voltage (V_{IMON}) to detect OC_AVG fault.

Units: V

COMMAND	OC_AVG_FAULT_LIMIT (D6h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table							
Default Value	0	0	0	0	0	1	1	1

BITS 7:3 (NOT USED)	BITS 2:0	OC_AVG THRESHOLD FOR V_{IMON} (V)
Not Used	000	1
Not Used	001	1.15
Not Used	010	1.25
Not Used	011	1.4
Not Used	100	1.55
Not Used	101	1.7
Not Used	110	1.85
Not Used	111	2

Application Information

External components and boost regulators can be defined several ways. This section shows one example of how to decide the parameters of the external components based on the typical application schematics as shown in Figure 4 on page 8. In the actual application, the parameters may need to be adjusted and additional components may be needed for the specific applications regarding noise, physical sizes, thermal, testing, and/or other requirements.

Output Voltage Setting

The output voltage (V_{OUT}) of the regulator can be programmed by an external resistor divider connecting from V_{OUT} to FB and FB to GND as shown in Figure 4 on page 8. Use Equation 2 on page 26 to calculate the desired V_{OUT}, where V_{REF} can be either VREF_DAC or VREF_TRK, whichever is lower. VREF_DAC default is 1.6V and can be programmed to a value between 0V to 2.04V using the PMBus command "VOUT_COMMAND (21h)" on page 48. In the actual application, the resistor value should be decided by considering the quiescent current requirement and loop response. Typically, between 4.7kΩ to 20kΩ is used for the R_{FB1}.

Switching Frequency

Switching frequency is determined by requirements for transient response time, solution size, EMC/EMI, power dissipation, efficiency, ripple noise level, and input/output voltage range. Higher frequency may improve the transient response and help to reduce the solution size. However, this may increase the switching losses and EMC/EMI concerns. Thus, a balance of these parameters is needed when deciding the switching frequency.

When the switching frequency f_{SW} is decided, the frequency setting resistor (R_{FSYNC}) can be determined by Equation 6 on page 29.

Input Inductor Selection

While the boost converter is operating in steady state Continuous Conduction Mode (CCM), the output voltage is determined by Equation 1 on page 25. With the required input and output voltage, duty cycle D can be calculated by Equation 34:

$$D = 1 - \frac{V_{IN}}{V_{OUT}} \quad \text{(EQ. 34)}$$

where D is the on-duty of the boost low-side power transistor.

Under this CCM condition, the inductor peak-to-peak ripple current of each phase can be calculated as Equation 35:

$$I_{L(P-P)} = D \cdot T \cdot \frac{VIN}{L} \quad \text{(EQ. 35)}$$

where T is the switching cycle $1/f_{SW}$ and L is each phase inductor's inductance.

From the previous equations, the inductor value is determined by Equation 36:

$$L = \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \cdot \frac{V_{IN}}{I_{L(P-P)} \cdot f_{SW}} \quad \text{(EQ. 36)}$$

Use Equation 36 to calculate L, where values of V_{IN}, V_{OUT} and I_{Lpp} are based on the considerations described in the following:

- One method is to select the minimum input voltage and the maximum output voltage under long term operation as the conditions to select the inductor. In this case, the inductor DC current is the largest.
- The general rule for selecting the inductor is to have its ripple current $I_{L(P-P)}$ around 30% to 50% of maximum DC current. The individual maximum DC inductor current for the 2-phase boost converter can be calculated by Equation 37, where P_{OUTmax} is the maximum DC output power, EFF is the estimated efficiency:

$$I_{Lmax} = \frac{P_{OUTmax}}{V_{INmin} \cdot EFF \cdot 2} \quad \text{(EQ. 37)}$$

Using Equation 36 with the two conditions listed above, a reasonable starting point for the minimum inductor value can be estimated from Equation 38, where K is typically selected as 30%.

$$L_{min} = \left(1 - \frac{V_{INmin}}{V_{OUTmax}}\right) \cdot \frac{V_{INmin}^2 \cdot EFF \cdot 2}{P_{OUTmax} \cdot K \cdot f_{SW}} \quad \text{(EQ. 38)}$$

Increasing the value of the inductor reduces the ripple current and therefore the ripple voltage. However, the large inductance value may reduce the converter's response time to a load transient. Also, this reduces the ramp signal and may cause a noise sensitivity issue.

The peak current at maximum load condition must be lower than the saturation current rating of the inductor with enough margin. In the actual design, the largest peak current may be observed at some transient conditions like the start-up or heavy load transient. Therefore, the inductor's size needs to be determined with the consideration of these conditions. To avoid exceeding the inductor's saturation rating, OC1 peak current limiting (refer to "Peak Current Cycle-by-Cycle Limiting (OC1)" on page 36) should be selected below the inductor's saturation current rating.

Output Capacitor

To filter the inductor current ripples and to have sufficient transient response, output capacitors are required. A combination of electrolytic and ceramic capacitors is normally used.

The ceramic capacitors filter the high frequency spikes of the main switching devices. In layout, these output ceramic capacitors must be placed as close as possible to the main switching devices to maintain the smallest switching loop. To maintain capacitance over the biased voltage and temperature range, high quality capacitors such as X7R or X5R are recommended.

The electrolytic capacitors are normally used to handle the load transient and output ripples. The boost output ripples are mainly dominated by the load current and output capacitance volume.

For the boost converter, the maximum output voltage ripple can be estimated using Equation 39, where I_{OUTmax} is the load current at output, C is the total capacitance at output, and D_{MIN} is the minimum duty cycle at VIN_{max} and $VOUT_{min}$.

$$V_{OUTripple} = \frac{I_{OUTmax} \cdot (1 - D_{MIN})}{C \cdot 2 \cdot f_{SW}} \quad \text{(EQ. 39)}$$

For a 2-phase boost converter, the RMS current going through the output current can be calculated by Equation 39 for D > 0.5, where I_L is per phase inductor DC current. For D < 0.5, time domain simulation is recommended to get the accurate calculation of the input capacitor RMS current.

$$I_{CoutRMS} = I_L \cdot \sqrt{(1 - D) \cdot (2D - 1)} \quad \text{(EQ. 40)}$$

It is recommended to use multiple capacitors in parallel to handle this output RMS current.

Input Capacitor

Depending upon the system input power rail conditions, the aluminum electrolytic type capacitors are normally used to provide a stable input voltage. The input capacitor should be able to handle the RMS current from the switching power devices. Refer to Equation 5 and Figure 62 on page 28 to estimate the RMS current the input capacitors need to handle.

Ceramic capacitors must be placed near the VIN and PGND pin of the IC. Multiple ceramic capacitors including 1µF and 0.1µF are recommended. Place these capacitors as close as possible to the IC.

Power MOSFET

The external MOSFETs driven by the ISL78229 controller must be carefully selected to optimize the design of the synchronous boost regulator.

The MOSFET's BV_{DSS} rating must have enough voltage margin against the maximum boost output voltage plus the phase node voltage transient during switching.

As the UG and LG gate drivers are 5V output, the MOSFET V_{GS} need to be in this range.

The MOSFET should have low Total Gate Charge (Q_g), low ON-resistance ($r_{DS(ON)}$) at V_{GS} = 4.5V and small gate resistance (R_g <1.5Ω is recommended). It is recommended that the minimum V_{GS} threshold is higher than 1.2V but does not exceed 2.5V, in order to prevent false turn-on by noise spikes due to high dv/dt during phase node switching and maintain low $r_{DS(ON)}$ under limitation of maximum gate drive voltage, which is 5.2V (typical) for low-side MOSFET and 4.5V (typical) due to diode drop of boot diode for high-side MOSFET.

Bootstrap Capacitor

The power required for high-side MOSFET drive is provided by the boot capacitor connected between BOOT and PH pins. The bootstrap capacitor can be chosen using Equation 41:

$$C_{BOOT} > \frac{Q_{gate}}{dV_{BOOT}} \quad \text{(EQ. 41)}$$

Where Q_{gate} is the total gate charge of the high-side MOSFET and dV_{BOOT} is the maximum droop voltage across the bootstrap capacitor while turning on the high-side MOSFET.

Though the maximum charging voltage across the bootstrap capacitor is PVCC minus the bootstrap diode drop (~4.5V), large excursions below GND by PH node requires at least 10V rating for this ceramic capacitor. To keep enough capacitance over the biased voltage and temperature range, a high quality capacitor such as X7R or X5R is recommended.

RESISTOR ON BOOTSTRAP CIRCUIT

In the actual application, sometimes a large ringing noise at the PH node and the BOOT node occurs. This noise is caused by high dv/dt phase node switching and parasitic PH node capacitance due to PCB routing and the parasitic inductance. To reduce this noise, a resistor can be added between the BOOT pin and the bootstrap capacitor. A large resistor value reduces the ringing noise at PH node but limits the charging of the bootstrap capacitor during the low-side MOSFET on-time, especially when the controller is operating at very low duty cycle. Also, large resistance causes a voltage dip at BOOT each time the high-side driver turns on the high-side MOSFET. Make sure this voltage dip does not trigger the high-side BOOT to PH UVLO threshold 3V (typical), especially when a MOSFET with large Q_g is used.

Loop Compensation Design

The ISL78229 uses constant frequency peak current mode control architecture with a Gm amp as the error amplifier. Figures 74 and 75 show the conceptual schematics and control block diagram, respectively.

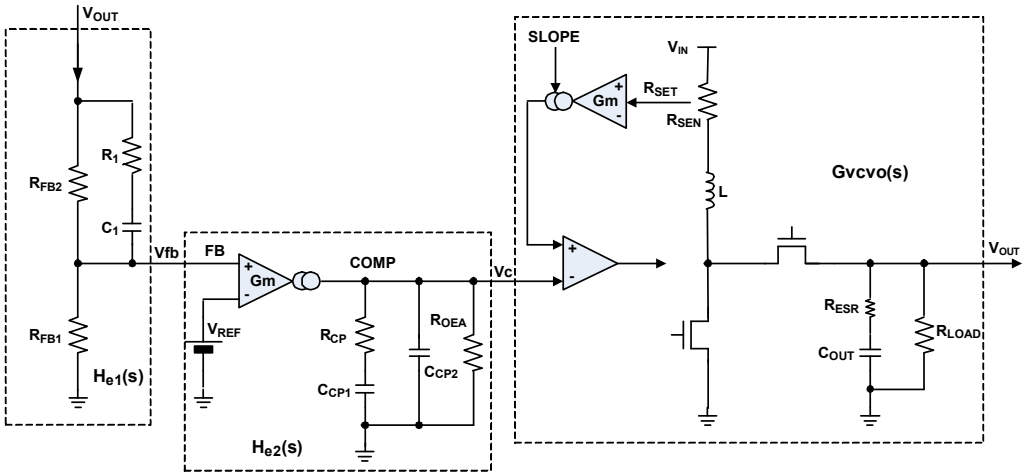


FIGURE 74. CONCEPTUAL BLOCK DIAGRAM OF PEAK CURRENT MODE CONTROLLED BOOST REGULATOR

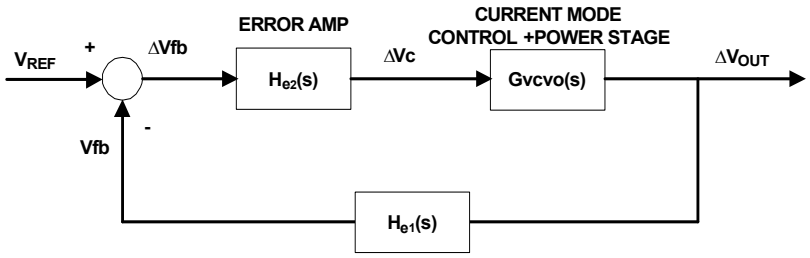


FIGURE 75. CONCEPTUAL CONTROL BLOCK DIAGRAM

TRANSFER FUNCTION FROM V_C TO V_{OUT}

Transfer function from error amplifier output V_C to output voltage V_{OUT} $G_{vcvo}(s)$ can be expressed as Equation 42.

$$G_{vcvo}(s) = K_{DC} \cdot \frac{\left(1+\frac{s}{\omega_{esr}}\right)\cdot\left(1-\frac{s}{\omega_{RHZ}}\right)}{\left(1+\frac{s}{\omega_p PS}\right)\cdot\left(1+\frac{s}{Q_p\cdot\omega_n}+\left(\frac{s}{\omega_n}\right)^2\right)} \quad \text{(EQ. 42)}$$

The expressions of the poles and zeros are listed below:

$$K_{DC} = \frac{R_{LOAD}\cdot(1-D)}{2\cdot K_{ISEN}}$$

$$\omega_{RHZ} = \frac{R_{LOAD}\cdot(1-D)^2}{L_{eq}}$$

$$\omega_{esr} = \frac{1}{C_{OUT}\cdot R_{esr}}$$

$$\omega_p PS = \frac{2}{C_{OUT}\cdot R_{LOAD}}$$

$$Q_p = \frac{1}{\pi\cdot\left[(1-D)\cdot\frac{S_e}{S_n}+0.5-D\right]}$$

$$\omega_n = \pi\cdot f_{sw}$$

where:

- N is the number of phases, R_{ESR} is the output capacitor's Equivalent Series Resistance (ESR) of the total capacitors, R_{LOAD} is the load resistance, L_{eq} is the equivalent inductance for multiphase boost with N number of phases and L is the inductance on each phase.

  $$L_{eq} = \frac{L}{N}$$

- K_{ISEN} is the current sense gain as shown in Equation 43, where R_{SENx} and R_{SETx} are per phase current sense resistor and setting resistors described in "Current Sense for Individual Phase - ISENX" on page 32.

  $$K_{ISEN} = \frac{R_{SENx}\cdot 6500}{N\cdot R_{SETx}} \quad \text{(EQ. 43)}$$

- Se/Sn is gain of the selected compensating slope over the sensed inductor current up-ramp. It can be calculated in Equation 44, where K_{SLOPE} is the gain of selected compensating slope over the sensed I_L down slope (refer to Equation 15 on page 33).

  $$\frac{S_e}{S_n} = K_{SLOPE}\cdot\left(\frac{V_{OUT}}{V_{IN}}-1\right) \quad \text{(EQ. 44)}$$

Equation 42 shows that the system is mainly a single order system plus a Right Half Zero (RHZ), which commonly exists for boost converters. The main pole ω_{pPS} is determined by load and output capacitance and the ESR zero ω_{ESR} is the same as buck converter.

Because the ω_{RHZ} changes with load, typically the boost converter crossover frequency is set 1/5 to 1/3 of the ω_{RHZ} frequency.

The double pole ω_n is at half of the f_{SW} and has minimum effects at crossover frequency for most of the cases when the crossover frequency is fairly low.

COMPENSATOR DESIGN

Generally a simple Type-2 compensator can be used to stabilize the system. In the actual application, however, an extra phase margin is provided by a Type-3 compensator.

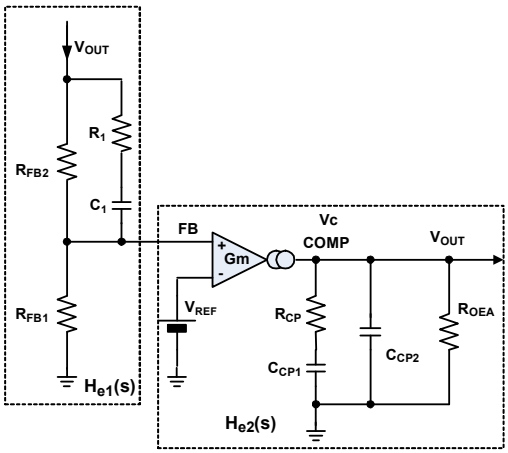


FIGURE 76. TYPE-3 COMPENSATOR

The transfer function at the error amplifier and its compensation network is expressed as Equation 45.

$$H_{e2}(s) = \frac{V_C}{V_{FB}} = g_m \cdot Z_{COMP} = \frac{g_m \frac{(1+sR_{CP}C_{CP1})R_{OEA}}{1+s[R_{CP}C_{CP1}+R_{OEA}(C_{CP1}+C_{CP2})]+C_{CP2}C_{CP1}R_{CP}R_{OEA}s^2}}{} \quad \text{(EQ. 45)}$$

If $R_{OEA}>>R_{CP}$, $C_{CP1}>>C_{CP2}$, and R_{OEA} = infinite, the equation can be simplified as shown in Equation 46:

$$H_{e2}(s) = g_m \cdot \frac{1+s \cdot R_{CP} \cdot C_{CP1}}{s \cdot C_{CP1} \cdot (1+s \cdot R_{CP} \cdot C_{CP2})} = \frac{\omega_1}{s} \cdot \frac{1+\frac{s}{\omega_{z2}}}{1+\frac{s}{\omega_{p2}}} \quad \text{(EQ. 46)}$$

where:

$$\omega_{p2} = \frac{g_m}{C_{CP1}}$$

$$\omega_{z2} = \frac{1}{R_{CP} \cdot C_{CP1}}$$

$$\omega_{p3} = \frac{1}{R_{CP} \cdot C_{CP2}}$$

If Type-3 compensation is needed, the transfer function at the feedback resistor network is:

$$H_{e1}(S) = \frac{R_{FB1}}{R_{FB1}+R_{FB2}} \cdot \frac{1+\frac{s}{\omega_{z1}}}{1+\frac{s}{\omega_{p1}}} \quad \text{(EQ. 47)}$$

where:

$$\omega_{z1} = \frac{1}{C_1 \cdot (R_{FB2}+R_1)}$$

$$\omega_{p1} = \frac{1}{C_1 \cdot \frac{R_{FB2} \cdot R_{FB1}+R_{FB2} \cdot R_1+R_{FB1} \cdot R_1}{R_{FB2}+R_{FB1}}}$$

The total transfer function with compensation network and gain stage is expressed:

$$G_{open}(s) = G_{vcvo}(s) \cdot H_{e1}(s) \cdot H_{e2}(s) \quad \text{(EQ. 48)}$$

Use f = ω/2π to convert the pole and zero expressions to frequency domain, and from Equations 42, 47 and 48, select the compensator's pole and zero locations.

In general, as described earlier, a Type-2 compensation is enough. Typically the crossover frequency is set 1/5 to 1/3 of the ω_{RHZ} frequency. For the compensator, as general rule, set $\omega_{p2}/2\pi$ at very low end frequency; set $\omega_{z2}/2\pi$ at 1/5 of the crossover frequency; set $\omega_{p3}/2\pi$ at the ESR zero or the RHZ frequency $\omega_{RHZ}/2\pi$, whichever is lower.

VCC Input Filter

To provide a quiet power rail to the internal analog circuitry, it is recommended to place an RC filter between PVCC and VCC. A 10Ω resistor between PVCC and VCC and at least 1µF ceramic capacitor from VCC to GND are recommended.

Current Sense Circuit

To set the current sense resistor, the voltage across the current sense resistor should be limited to within ±0.3V. In a typical application, it is recommended to set the voltage across the current sense resistor between 30mV to 100mV for the typical load current condition.

Configuration to Support Single Phase Boost

The IC can be configured to support single phase operation using either phase 1 or phase 2. The configurations needed to use phase 1 for single phase operation are listed below (use phase 2 for single phase operation by changing corresponding phase number to the other phase number):

- BOOT2 = GND (UG2 disabled)
- ISEN2P = ISEN2N = GND
- PH2 = GND

The extra notes are listed below with upper single phase configurations:

- LG2 can be left floating. LG2 has PWM signals which is fine with no external MOSFET to drive.
- IMON pin output current signal has only phase 1's inductor current sensed signal. Equation 12, for calculating the IMON output current, is turned to into Equation 49.

$$IMON = \frac{I_{L1} \cdot R_{SEN1}}{R_{SET1}} \cdot 0.125 + 17 \cdot 10^{-6} \quad \text{(EQ. 49)}$$

The Constant Current Loop works on the same principle.

Layout Considerations

The PCB layout is very important to ensure the desired performance for the DC/DC converter.

1. Place input ceramic capacitors as close as possible to the IC's VIN and PGND/SGND pins.
2. Place the output ceramic capacitors as close as possible to the power MOSFET. Keep this loop (output ceramic capacitor and MOSFETs for each phase) as small as possible to reduce voltage spikes induced by the trace parasitic inductances when MOSFETs switching ON and OFF.
3. Place the output aluminum capacitors close to power MOSFETs too.
4. Keep the phase node copper area small but large enough to handle the load current.
5. Place the input aluminum and some ceramic capacitors close to the input inductors and power MOSFETs.
6. Place multiple vias under the thermal pad of the IC. Connect the thermal pad to the ground copper plane with as large an area as possible in multiple layers to effectively reduce the thermal impedance. Figure 77 shows the layout example for vias in the IC bottom pad.

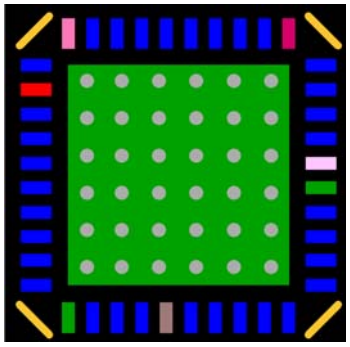


FIGURE 77. RECOMMENDED LAYOUT PATTERN FOR VIAS IN THE IC BOTTOM PAD

7. Place the 10µF decoupling ceramic capacitor at the PVCC pin and as close as possible to the IC. Put multiple vias close to the ground pad of this capacitor.
8. Place the 1µF decoupling ceramic capacitor at the VCC pin and as close as possible to the IC. Put multiple vias close to the ground pad of this capacitor.
9. Keep the bootstrap capacitor as close as possible to the IC.
10. Keep the driver traces as short as possible and with relatively large width (25 mil to 40 mil is recommended), and avoid using vias or a minimal number of vias in the driver path to achieve the lowest impedance.
11. Place the current sense setting resistors and the filter capacitor (shown as R_{SETxB}, R_{BIASxB} and C_{ISENx} in Figure 69 on page 32) as close as possible to the IC. Keep each pair of the traces close to each other to avoid undesired switching noise injections.
12. The current sensing traces must be laid out very carefully because they carry tiny signals with only tens of mV. For the current sensing traces close to the power sense resistor (R_{SENx}), the layout pattern shown in Figure 78 is recommended. Assuming the R_{SENx} is placed in the top layer (red), route one current sense connection from the middle of one R_{SENx} pad in the top layer under the resistor (red trace). For the other current-sensing trace, from the middle of the other pad on R_{SENx} in top layer, after a short distance, via down to the second layer and route this trace right under the top layer current sense trace.
13. Keep the current sensing traces far from the noisy traces like gate driving traces (LGx, UGx, and PHx), phase nodes in power stage, BOOTx signals, output switching pulse currents, driving bias traces, and input inductor ripple current signals, etc.

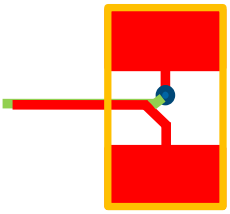


FIGURE 78. RECOMMENDED LAYOUT PATTERN FOR CURRENT SENSE TRACES REGULATOR

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Jul 13, 2018	FN8656.6	Updated the ordering information table by adding tape and reel column, adding T&R FGs to table, and updating Note 1. Added two lines to the “Absolute Maximum Ratings” on page 9. Changed “If the DE/PHDRP pin = GND” to “If the DE/PHDRP pin = VCC” in “Operation Initialization and Soft-Start” on page 30. Removed the About Intersil section and updated disclaimer.
Sep 18, 2017	FN8656.5	Added Related Literature section Updated Equation 7 on page 31. Applied new header/footer.
Feb 6, 2017	FN8656.4	- Added third sentence in the VIN pin description on page 5. - Figures 26 and 28 on page 19, changed "D" to "D_TRACK" in the title to avoid confusion. - Figure 51 on page 24, swapped VPORL_PVCC and VPORL_VCC data labels for the 2 curves. - Added “while the adaptive dead time control is still functioning at the same time” to the first sentence in “Programmable Adaptive Dead Time Control” on page 26. - Added “for three consecutive switching cycles” to the first sentence in “Peak Overcurrent Fault (OC2_PEAK)” on page 37. - Added the last paragraph in “Average Overcurrent Fault (OC_AVG)” on page 38. - Updated Figures 74, 75, and 76. - Updated Equation 42 on page 67, and expressions K_{DC}, wpPS, Q_p, and w_n. - Updated Equation 43 on page 67. - Added section “Configuration to Support Single Phase Boost” on page 68.
Feb 12, 2016	FN8656.3	Table 4 on page 41 updated D2h descriptions PMBus command summary Table 6 on page 43, simplified D2h descriptions. SET_FAULT_RESPONSE (D2h) on page 60 changes as follow: Changed 0000h to 03FFh, 00FFh to 0000h. Changed from “Not used” to “set by the HIC/LATCH pin” (2 places) Changed from “all the bits are set to 1 as default” to “each of bits[9:0] is set to 1 as default” Changed from “all the bits are set to 0 as default” to “each of bits[9:0] is set to 0 as default”
Feb 4, 2016	FN8656.2	Changed in Figure 16 on page 18 label “IL1” to IL2” and in title “Phase 1” to “Phase 2”.
Jan 4, 2016	FN8656.1	Updated 2nd and 3rd paragraph in section “External Over-Temperature Fault (OT_NTC_FAULT)” on page 39 for clarity and changed in 4th paragraph “450mV” to “300mV”. Changed in “IC_DEVICE_REV (AEh)”, “0B01h” and “010Ch” to “0C01h” and changed default value in table starting with the 6th number from “...011...” to “...100...” on page 43 and page 57. Changed Default Value for “FAULT_MASK FROM “0043h” to “0049h” on page 41 and page 59 Updated the table bit value: From: 0000-0000-0100-0011; To: 0000-0000-0100-1001 Updated D1h default value column in Table 4 on page 41. Updated expression Qp and Equation 44 on page 67 Removed text after Equation 44 on page 67 and before paragraph that begins with “Equation 42”.
Nov 23, 2015	FN8656.0	Initial Release

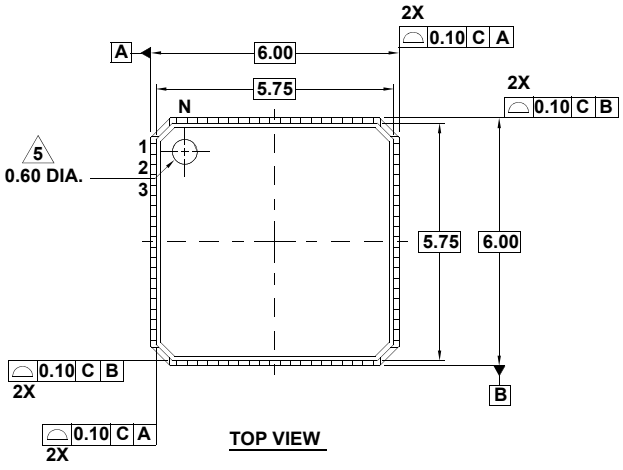
Package Outline Drawing

For the most recent package outline drawing, see L40.6x6C.

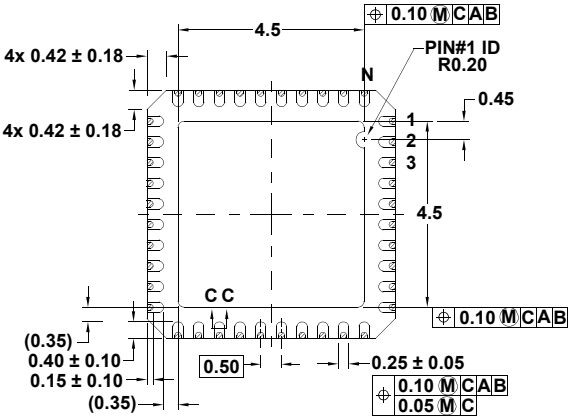
L40.6x6C

40 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (PUNCH QFN WITH WETTABLE FLANK)

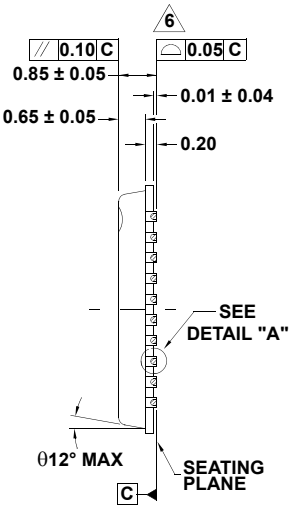
Rev 1, 1/14



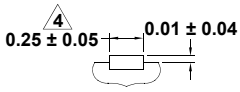
TOP VIEW



BOTTOM VIEW



SIDE VIEW



SECTION "C-C"

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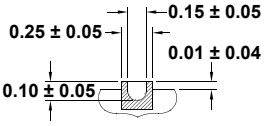

DETAIL "A"

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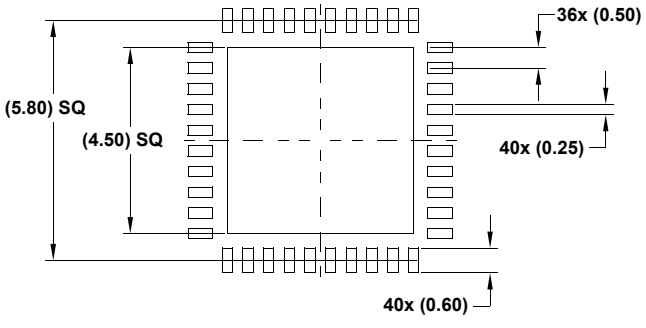

TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension applies to the plated terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
6. Reference document: JEDEC MO220

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