



**THE DATASHEET OF  
J309**



# J309, J310

Preferred Device

## JFET VHF/UHF Amplifiers

### N-Channel — Depletion

#### Features

- Pb-Free Packages are Available\*

#### MAXIMUM RATINGS

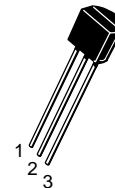
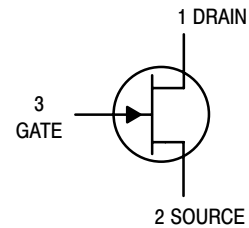
Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	25	Vdc
Gate-Source Voltage	$V_{GS}$	25	Vdc
Forward Gate Current	$I_{GF}$	10	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above = $25^\circ\text{C}$	$P_D$	350 2.8	mW mW/ $^\circ\text{C}$
Junction Temperature Range	$T_J$	-65 to +125	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-65 to +150	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.



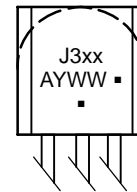
ON Semiconductor®

<http://onsemi.com>



TO-92  
CASE 29-11  
STYLE 5

#### MARKING DIAGRAM



J3xx = Device Code

xx = 09 or 10

A = Assembly Location

Y = Year

WW = Work Week

▪ = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

**Preferred** devices are recommended choices for future use and best overall value.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# J309, J310

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Gate–Source Breakdown Voltage (I <sub>G</sub> = –1.0 μAdc, V <sub>DS</sub> = 0)	V <sub>(BR)GSS</sub>	–25	–	–	Vdc
Gate Reverse Current (V <sub>GS</sub> = –15 Vdc, V <sub>DS</sub> = 0, T <sub>A</sub> = 25°C) (V <sub>GS</sub> = –15 Vdc, V <sub>DS</sub> = 0, T <sub>A</sub> = +125°C)	I <sub>GSS</sub>	– –	– –	–1.0 –1.0	nAdc μAdc
Gate Source Cutoff Voltage (V <sub>DS</sub> = 10 Vdc, I <sub>D</sub> = 1.0 nAdc)	V <sub>GS(off)</sub>	–1.0 –2.0	– –	–4.0 –6.5	Vdc
<b>ON CHARACTERISTICS</b>					
Zero–Gate–Voltage Drain Current <sup>(1)</sup> (V <sub>DS</sub> = 10 Vdc, V <sub>GS</sub> = 0)	I <sub>DSS</sub>	12 24	– –	30 60	mAdc
Gate–Source Forward Voltage (V <sub>DS</sub> = 0, I <sub>G</sub> = 1.0 mAdc)	V <sub>GS(f)</sub>	–	–	1.0	Vdc
<b>SMALL–SIGNAL CHARACTERISTICS</b>					
Common–Source Input Conductance (V <sub>DS</sub> = 10 Vdc, I <sub>D</sub> = 10 mAdc, f = 100 MHz)	Re(y <sub>is</sub> )	– –	0.7 0.5	– –	mmhos
Common–Source Output Conductance (V <sub>DS</sub> = 10 Vdc, I <sub>D</sub> = 10 mAdc, f = 100 MHz)	Re(y <sub>os</sub> )	–	0.25	–	mmhos
Common–Gate Power Gain (V <sub>DS</sub> = 10 Vdc, I <sub>D</sub> = 10 mAdc, f = 100 MHz)	G <sub>pg</sub>	–	16	–	dB
Common–Source Forward Transconductance (V <sub>DS</sub> = 10 Vdc, I <sub>D</sub> = 10 mAdc, f = 100 MHz)	Re(y <sub>fs</sub> )	–	12	–	mmhos
Common–Gate Input Conductance (V <sub>DS</sub> = 10 Vdc, I <sub>D</sub> = 10 mAdc, f = 100 MHz)	Re(y <sub>ig</sub> )	–	12	–	mmhos
Common–Source Forward Transconductance (V <sub>DS</sub> = 10 Vdc, I <sub>D</sub> = 10 mAdc, f = 1.0 kHz)	g <sub>fs</sub>	10000 8000	– –	20000 18000	μmhos
Common–Source Output Conductance (V <sub>DS</sub> = 10 Vdc, I <sub>D</sub> = 10 mAdc, f = 1.0 kHz)	g <sub>os</sub>	–	–	250	μmhos
Common–Gate Forward Transconductance (V <sub>DS</sub> = 10 Vdc, I <sub>D</sub> = 10 mAdc, f = 1.0 kHz)	g <sub>fg</sub>	– –	13000 12000	– –	μmhos
Common–Gate Output Conductance (V <sub>DS</sub> = 10 Vdc, I <sub>D</sub> = 10 mAdc, f = 1.0 kHz)	g <sub>og</sub>	– –	100 150	– –	μmhos
Gate–Drain Capacitance (V <sub>DS</sub> = 0, V <sub>GS</sub> = –10 Vdc, f = 1.0 MHz)	C <sub>gd</sub>	–	1.8	2.5	pF
Gate–Source Capacitance (V <sub>DS</sub> = 0, V <sub>GS</sub> = –10 Vdc, f = 1.0 MHz)	C <sub>gs</sub>	–	4.3	5.0	pF
<b>FUNCTIONAL CHARACTERISTICS</b>					
Equivalent Short–Circuit Input Noise Voltage (V <sub>DS</sub> = 10 Vdc, I <sub>D</sub> = 10 mAdc, f = 100 Hz)	$\bar{e}_n$	–	10	–	nV/√Hz

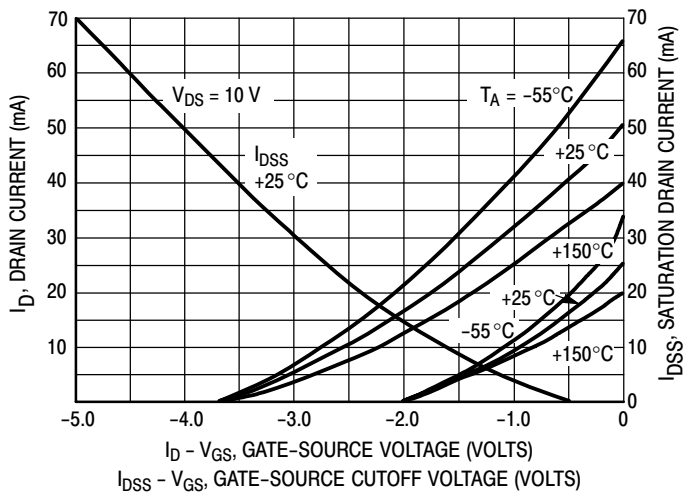
1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 3.0%.

# J309, J310

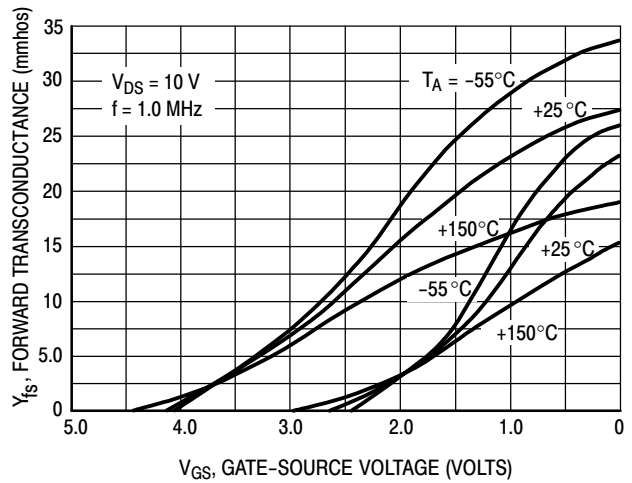
## ORDERING INFORMATION

Device	Package	Shipping†
J309	TO-92	1000 Units / Bulk
J309G	TO-92 (Pb-Free)	
J310	TO-92	1000 Units / Bulk
J310G	TO-92 (Pb-Free)	
J310RLRP	TO-92	2000 Units / Tape & Ammo Box
J310RLRPG	TO-92 (Pb-Free)	
J310ZL1	TO-92	2000 Units / Tape & Ammo Box
J310ZL1G	TO-92 (Pb-Free)	

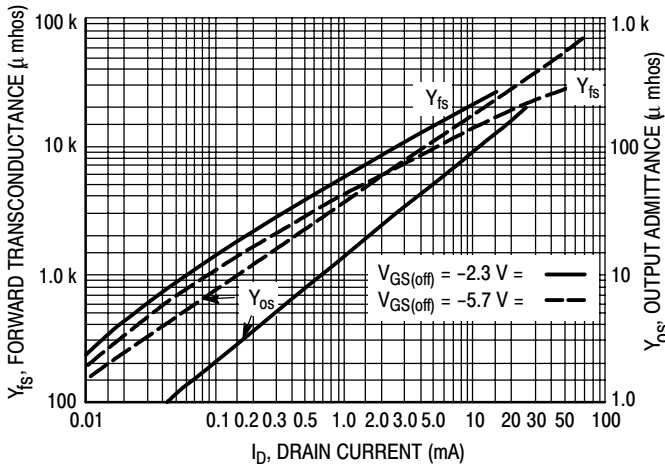
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



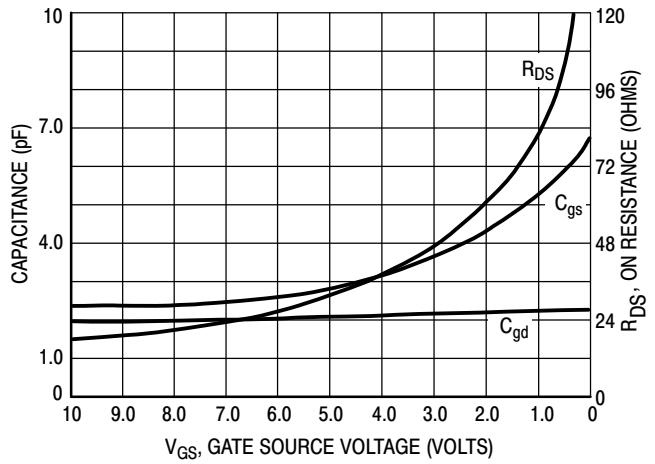
**Figure 1. Drain Current and Transfer Characteristics versus Gate-Source Voltage**



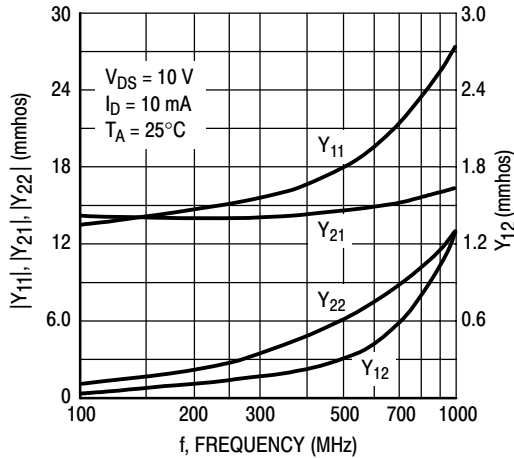
**Figure 2. Forward Transconductance versus Gate-Source Voltage**



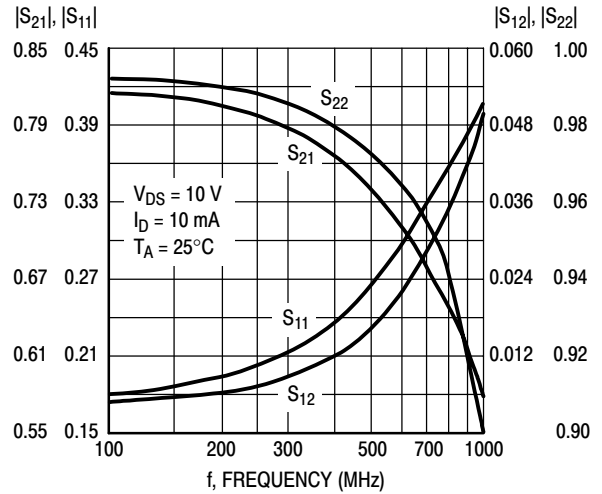
**Figure 3. Common-Source Output Admittance and Forward Transconductance versus Drain Current**



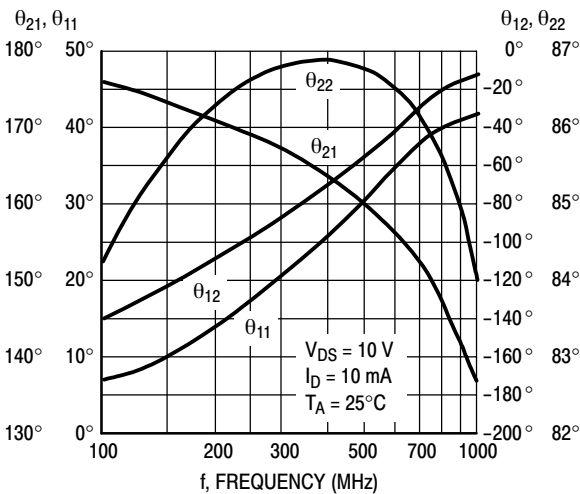
**Figure 4. On Resistance and Junction Capacitance versus Gate-Source Voltage**



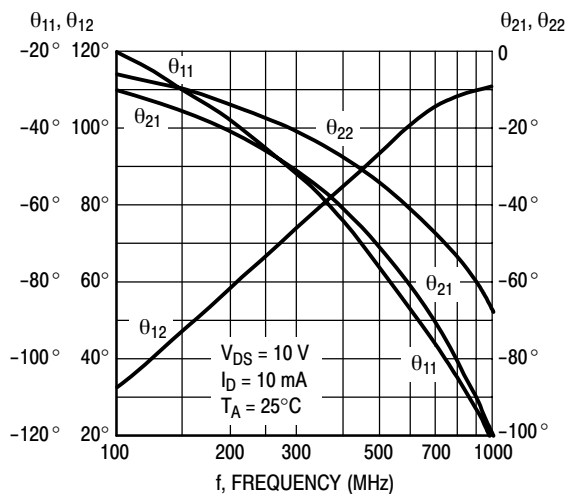
**Figure 5. Common-Gate Y Parameter Magnitude versus Frequency**



**Figure 6. Common-Gate S Parameter Magnitude versus Frequency**



**Figure 7. Common-Gate Y Parameter Phase-Angle versus Frequency**



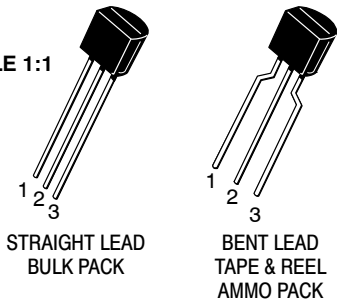
**Figure 8. S Parameter Phase-Angle versus Frequency**

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®

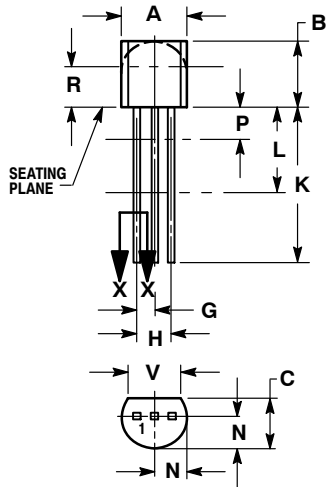


SCALE 1:1

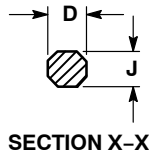


TO-92 (TO-226)  
CASE 29-11  
ISSUE AM

DATE 09 MAR 2007



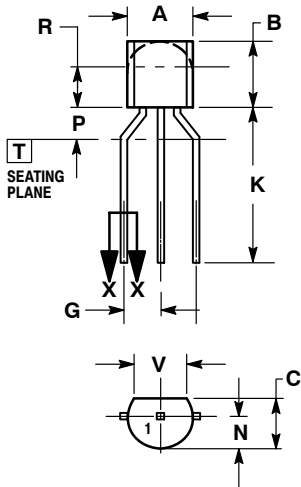
STRAIGHT LEAD  
BULK PACK



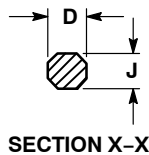
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---



BENT LEAD  
TAPE & REEL  
AMMO PACK



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	MILLIMETERS	
	MIN	MAX
A	4.45	5.20
B	4.32	5.33
C	3.18	4.19
D	0.40	0.54
G	2.40	2.80
J	0.39	0.50
K	12.70	---
N	2.04	2.66
P	1.50	4.00
R	2.93	---
V	3.43	---

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42022B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:		
DESCRIPTION:	TO-92 (TO-226)	PAGE 1 OF 3

**TO-92 (TO-226)**  
**CASE 29-11**  
**ISSUE AM**

DATE 09 MAR 2007

STYLE 1:  
 PIN 1. EMITTER  
 2. BASE  
 3. COLLECTOR

STYLE 2:  
 PIN 1. BASE  
 2. EMITTER  
 3. COLLECTOR

STYLE 3:  
 PIN 1. ANODE  
 2. ANODE  
 3. CATHODE

STYLE 4:  
 PIN 1. CATHODE  
 2. CATHODE  
 3. ANODE

STYLE 5:  
 PIN 1. DRAIN  
 2. SOURCE  
 3. GATE

STYLE 6:  
 PIN 1. GATE  
 2. SOURCE & SUBSTRATE  
 3. DRAIN

STYLE 7:  
 PIN 1. SOURCE  
 2. DRAIN  
 3. GATE

STYLE 8:  
 PIN 1. DRAIN  
 2. GATE  
 3. SOURCE & SUBSTRATE

STYLE 9:  
 PIN 1. BASE 1  
 2. EMITTER  
 3. BASE 2

STYLE 10:  
 PIN 1. CATHODE  
 2. GATE  
 3. ANODE

STYLE 11:  
 PIN 1. ANODE  
 2. CATHODE & ANODE  
 3. CATHODE

STYLE 12:  
 PIN 1. MAIN TERMINAL 1  
 2. GATE  
 3. MAIN TERMINAL 2

STYLE 13:  
 PIN 1. ANODE 1  
 2. GATE  
 3. CATHODE 2

STYLE 14:  
 PIN 1. EMITTER  
 2. COLLECTOR  
 3. BASE

STYLE 15:  
 PIN 1. ANODE 1  
 2. CATHODE  
 3. ANODE 2

STYLE 16:  
 PIN 1. ANODE  
 2. GATE  
 3. CATHODE

STYLE 17:  
 PIN 1. COLLECTOR  
 2. BASE  
 3. EMITTER

STYLE 18:  
 PIN 1. ANODE  
 2. CATHODE  
 3. NOT CONNECTED

STYLE 19:  
 PIN 1. GATE  
 2. ANODE  
 3. CATHODE

STYLE 20:  
 PIN 1. NOT CONNECTED  
 2. CATHODE  
 3. ANODE

STYLE 21:  
 PIN 1. COLLECTOR  
 2. EMITTER  
 3. BASE

STYLE 22:  
 PIN 1. SOURCE  
 2. GATE  
 3. DRAIN

STYLE 23:  
 PIN 1. GATE  
 2. SOURCE  
 3. DRAIN

STYLE 24:  
 PIN 1. EMITTER  
 2. COLLECTOR/ANODE  
 3. CATHODE

STYLE 25:  
 PIN 1. MT 1  
 2. GATE  
 3. MT 2

STYLE 26:  
 PIN 1. V<sub>CC</sub>  
 2. GROUND 2  
 3. OUTPUT

STYLE 27:  
 PIN 1. MT  
 2. SUBSTRATE  
 3. MT

STYLE 28:  
 PIN 1. CATHODE  
 2. ANODE  
 3. GATE

STYLE 29:  
 PIN 1. NOT CONNECTED  
 2. ANODE  
 3. CATHODE

STYLE 30:  
 PIN 1. DRAIN  
 2. GATE  
 3. SOURCE

STYLE 31:  
 PIN 1. GATE  
 2. DRAIN  
 3. SOURCE

STYLE 32:  
 PIN 1. BASE  
 2. COLLECTOR  
 3. EMITTER

STYLE 33:  
 PIN 1. RETURN  
 2. INPUT  
 3. OUTPUT

STYLE 34:  
 PIN 1. INPUT  
 2. GROUND  
 3. LOGIC

STYLE 35:  
 PIN 1. GATE  
 2. COLLECTOR  
 3. EMITTER

<b>DOCUMENT NUMBER:</b>	<b>98ASB42022B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>STATUS:</b>	<b>ON SEMICONDUCTOR STANDARD</b>	
<b>NEW STANDARD:</b>		
<b>DESCRIPTION:</b>	<b>TO-92 (TO-226)</b>	<b>PAGE 2 OF 3</b>



**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:



Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View J309](#) on WIN SOURCE
-  [ON Semiconductor](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management