



**THE DATASHEET OF
LT1793CS8#TRPBF**



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage	±20V	Specified Temperature Range	
Differential Input Voltage	±40V	Commercial (Note 8)	–40°C to 85°C
Input Voltage (Equal to Supply Voltage)	±20V	Industrial	–40°C to 85°C
Output Short-Circuit Duration	Indefinite	Storage Temperature Range	–65°C to 150°C
Operating Temperature Range	–40°C to 85°C	Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION

TOP VIEW	ORDER PART NUMBER	TOP VIEW	ORDER PART NUMBER
<p>N8 PACKAGE 8-LEAD PDIP $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 80^{\circ}\text{C/W}$</p>	LT1793ACN8 LT1793CN8 LT1793AIN8 LT1793IN8	<p>S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 160^{\circ}\text{C}$, $\theta_{JA} = 190^{\circ}\text{C/W}$</p>	LT1793ACS8 LT1793CS8 LT1793AIS8 LT1793IS8
		S8 PART MARKING	
		1793A	1793AI
		1793	1793I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS $T_A = 25^{\circ}\text{C}$, $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 2)	LT1793AC/LT1793AI			LT1793C/LT1793I			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$V_S = \pm 5\text{V}$		0.25	0.8		0.25	0.9	mV
				0.45	1.4		0.45	1.6	mV
I_{OS}	Input Offset Current	Warmed Up (Note 3) $T_J = 25^{\circ}\text{C}$ (Note 6)		1.5	7		2.5	15	μA
				0.5	2		0.7	4	μA
I_B	Input Bias Current	Warmed Up (Note 3) $T_J = 25^{\circ}\text{C}$ (Note 6)		3	10		4.0	20	μA
				1	3		1.5	5	μA
e_n	Input Noise Voltage	0.1Hz to 10Hz		2.4			2.4		μV_{P-P}
	Input Noise Voltage Density	$f_0 = 10\text{Hz}$ $f_0 = 1000\text{Hz}$		11.5			11.5		$\text{nV}/\sqrt{\text{Hz}}$
				6	8		6	8	$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f_0 = 10\text{Hz}$, $f_0 = 1\text{kHz}$ (Note 4)		0.8			1		$\text{fA}/\sqrt{\text{Hz}}$
R_{IN}	Input Resistance			10^{14}			10^{14}		Ω
	Differential Mode			10^{13}			10^{13}		Ω
	Common Mode	$V_{CM} = -10\text{V}$ to 13V							
C_{IN}	Input Capacitance	$V_S = \pm 5\text{V}$		1.5			1.5		pF
				2.0			2.0		pF
V_{CM}	Input Voltage Range (Note 5)		13.0	13.5		13.0	13.5		V
			–10.5	–11.0		–10.5	–11.0		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = -10\text{V}$ to 13V	83	102		81	96		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5\text{V}$ to $\pm 20\text{V}$	85	98		83	95		dB

ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 2)	LT1793AC/LT1793AI			LT1793C/LT1793I			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 12\text{V}$, $R_L = 10\text{k}$ $V_O = \pm 10\text{V}$, $R_L = 1\text{k}$	1000 500	4500 3500		900 400	4400 3000		V/mV V/mV
V_{OUT}	Output Voltage Swing	$R_L = 10\text{k}$ $R_L = 1\text{k}$	± 13.0 ± 12.0	± 13.2 ± 12.3		± 13.0 ± 12.0	± 13.2 ± 12.3		V V
SR	Slew Rate	$R_L \geq 2\text{k}$ (Note 7)	2.3	3.4		2.3	3.4		V/ μs
GBW	Gain-Bandwidth Product	$f_0 = 100\text{kHz}$	2.5	4.2		2.5	4.2		MHz
I_S	Supply Current	$V_S = \pm 5\text{V}$		4.2 4.2	5.20 5.15		4.2 4.2	5.20 5.15	mA mA
	Offset Voltage Adjustment Range	R_{POT} (to V_{EE}) = 10k		13			13		mV

The ● denotes specifications which apply over the temperature range $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$, unless otherwise noted. (Note 9)

SYMBOL	PARAMETER	CONDITIONS (Note 2)	LT1793AC			LT1793C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$V_S = \pm 5\text{V}$	●	0.50	1.0	●	1.0	3.5	mV
			●	0.75	1.6		1.6	4.2	mV
$\frac{\Delta V_{OS}}{\Delta \text{Temp}}$	Average Input Offset Voltage Drift	(Note 6)	●	5	13		8	50	$\mu\text{V}/^\circ\text{C}$
I_{OS}	Input Offset Current		●	15	100		20	130	pA
I_B	Input Bias Current		●	130	400		150	500	pA
V_{CM}	Input Voltage Range (Note 5)		●	12.9	13.4	●	12.9	13.4	V
			●	-10.0	-10.8		-10.0	-10.8	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = -10\text{V}$ to 12.9V	●	79	100		77	95	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5\text{V}$ to $\pm 20\text{V}$	●	83	97		81	94	dB
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 12\text{V}$, $R_L = 10\text{k}$ $V_O = \pm 10\text{V}$, $R_L = 1\text{k}$	●	900	3600	●	800	3400	V/mV
			●	500	2600		400	2400	V/mV
V_{OUT}	Output Voltage Swing	$R_L = 10\text{k}$ $R_L = 1\text{k}$	●	± 12.9	± 13.2	●	± 12.9	± 13.2	V
			●	± 11.9	± 12.15		± 11.9	± 12.15	V
SR	Slew Rate	$R_L \geq 2\text{k}$ (Note 7)	●	2.2	3.3		2.2	3.3	V/ μs
GBW	Gain-Bandwidth Product	$f_0 = 100\text{kHz}$	●	2.2	3.3		2.2	3.3	MHz
I_S	Supply Current	$V_S = \pm 5\text{V}$	●	4.2	5.30	●	4.2	5.30	mA
			●	4.2	5.25		4.2	5.25	mA

ELECTRICAL CHARACTERISTICS The ● denotes specifications which apply over the temperature range $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$. $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$, unless otherwise noted. (Notes 8, 9)

SYMBOL	PARAMETER	CONDITIONS (Note 2)		LT1793AC/LT1793AI			LT1793C/LT1793I			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$V_S = \pm 5\text{V}$	●	0.65	1.3		1.6	4.8	mV	
			●	1.00	1.9		2.0	5.5	mV	
$\frac{\Delta V_{OS}}{\Delta \text{Temp}}$	Average Input Offset Voltage Drift	(Note 6)	●	5	13		9	50	$\mu\text{V}/^{\circ}\text{C}$	
I_{OS}	Input Offset Current		●	80	300		100	400	μA	
I_B	Input Bias Current		●	700	2400		800	3000	μA	
V_{CM}	Input Voltage Range (Note 5)		●	12.6	13.0		12.6	13.0	V	
			●	-10.0	-10.5		-10.0	-10.5	V	
CMRR	Common Mode Rejection Ratio	$V_{CM} = -10\text{V}$ to 12.6V	●	78	99		76	94	dB	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5\text{V}$ to $\pm 20\text{V}$	●	81	96		79	93	dB	
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 12\text{V}$, $R_L = 10\text{k}$ $V_O = \pm 10\text{V}$, $R_L = 1\text{k}$	●	850	3300		750	3000	V/mV	
			●	400	2200		300	2000	V/mV	
V_{OUT}	Output Voltage Swing	$R_L = 10\text{k}$ $R_L = 1\text{k}$	●	± 12.8	± 13.1		± 12.8	± 13.1	V	
			●	± 11.8	± 12.1		± 11.8	± 12.1	V	
SR	Slew Rate	$R_L \geq 2\text{k}$	●	2.1	3.2		2.1	3.2	$\text{V}/\mu\text{s}$	
GBW	Gain-Bandwidth Product	$f_0 = 100\text{kHz}$	●	2	3.1		2	3.1	MHz	
I_S	Supply Current	$V_S = \pm 5\text{V}$	●	4.2	5.40		4.2	5.40	mA	
			●	4.2	5.35		4.2	5.35	mA	

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Typical parameters are defined as the 60% yield of parameter distributions of individual amplifiers.

Note 3: I_B and I_{OS} readings are extrapolated to a warmed-up temperature from 25°C measurements and 32°C characterization data.

Note 4: Current noise is calculated from the formula:

$$i_n = (2qI_B)^{1/2}$$

where $q = 1.6 \cdot 10^{-19}$ coulomb. The noise of source resistors up to 200M swamps the contribution of current noise.

Note 5: Input voltage range functionality is assured by testing offset voltage at the input voltage range limits to a maximum of 2.3mV (A grade) to 2.8mV (C grade).

Note 6: This parameter is not 100% tested.

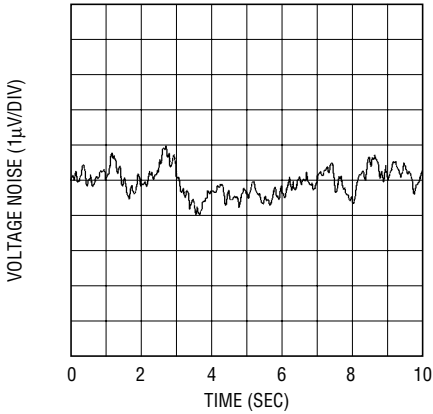
Note 7: Slew rate is measured in $A_V = -1$; input signal is $\pm 7.5\text{V}$, output measured at $\pm 2.5\text{V}$.

Note 8: The LT1793AC and LT1793C are guaranteed to meet specified performance from 0°C to 70°C and are designed, characterized and expected to meet these extended temperature limits, but are not tested at -40°C and 85°C . The LT1793I is guaranteed to meet the extended temperature limits. The LT1793AC and LT1793AI grade are 100% temperature tested for the specified temperature range.

Note 9: The LT1793 is measured in an automated tester in less than one second after application of power. Depending on the package used, power dissipation, heat sinking, and air flow conditions, the fully warmed-up chip temperature can be 10°C to 50°C higher than the ambient temperature.

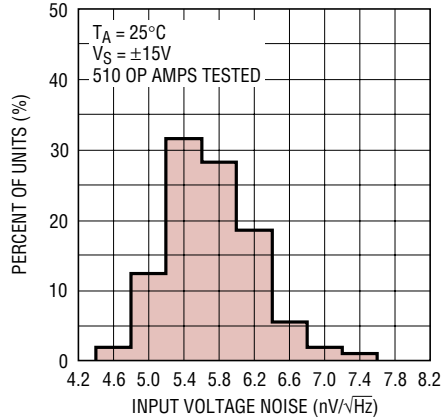
TYPICAL PERFORMANCE CHARACTERISTICS

0.1Hz to 10Hz Voltage Noise



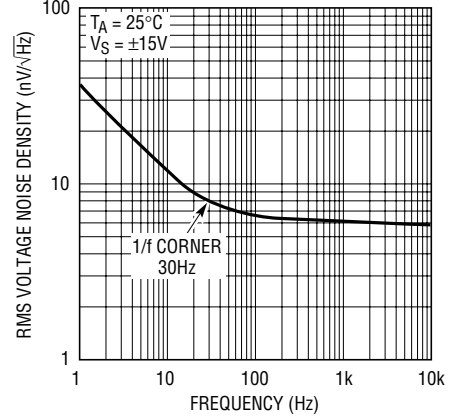
1793 G01

1kHz Input Noise Voltage Distribution



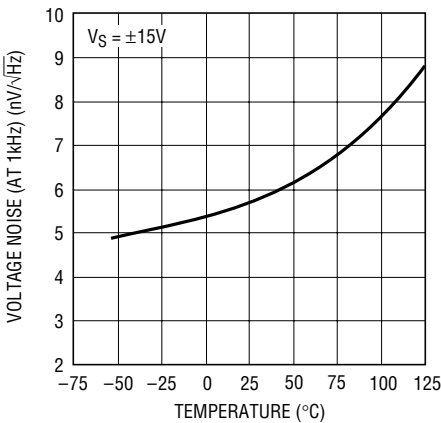
1793 G02

Voltage Noise vs Frequency



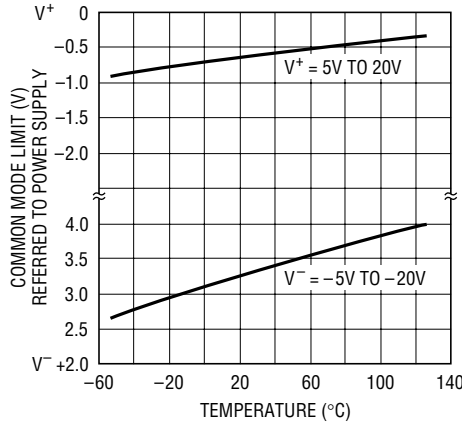
1793 G03

Voltage Noise vs Chip Temperature



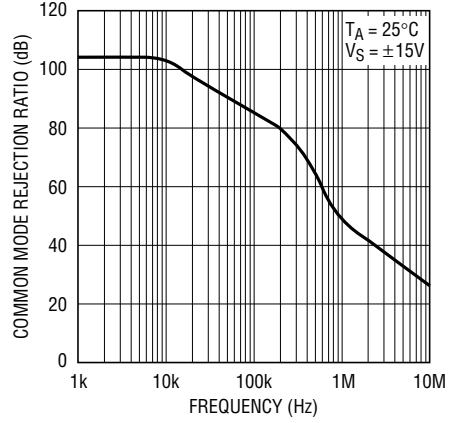
1793 G04

Common Mode Limit vs Temperature



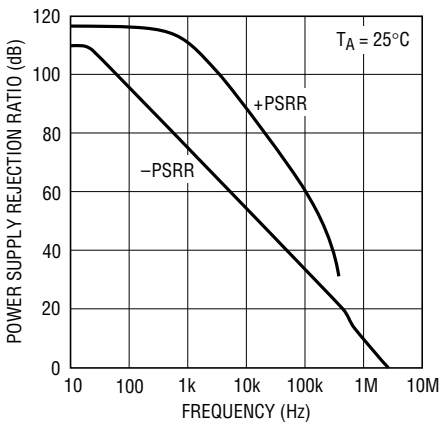
1793 G05

Common Mode Rejection Ratio vs Frequency



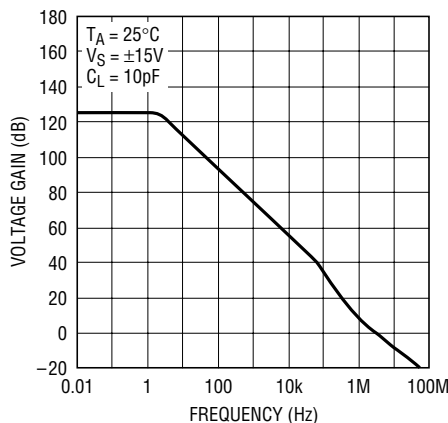
1793 G06

Power Supply Rejection Ratio vs Frequency



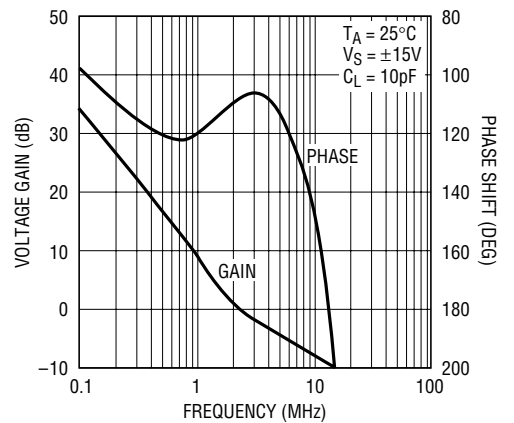
1793 G07

Voltage Gain vs Frequency



1793 G08

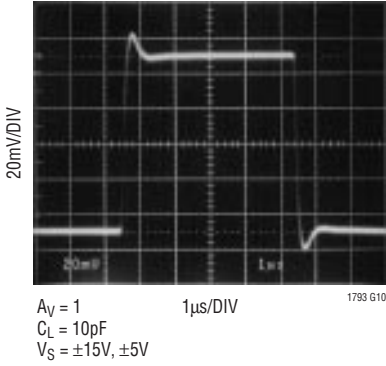
Gain and Phase Shift vs Frequency



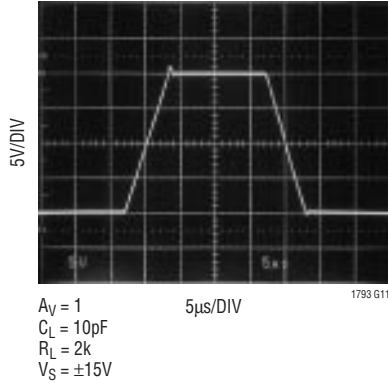
1793 G09

TYPICAL PERFORMANCE CHARACTERISTICS

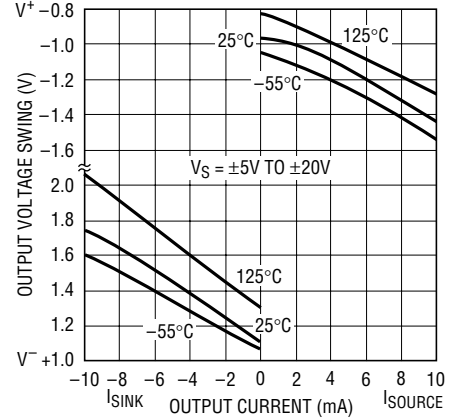
Small-Signal Transient Response



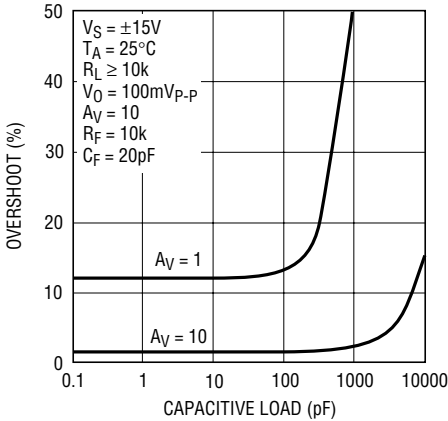
Large-Signal Transient Response



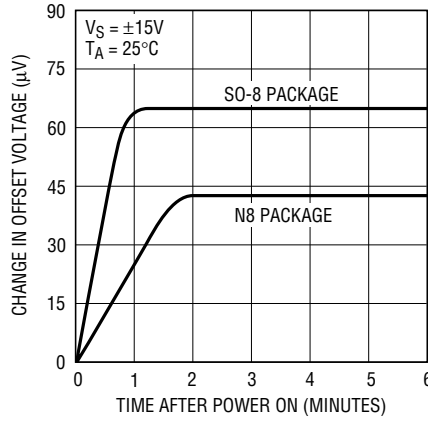
Output Voltage Swing vs Load Current



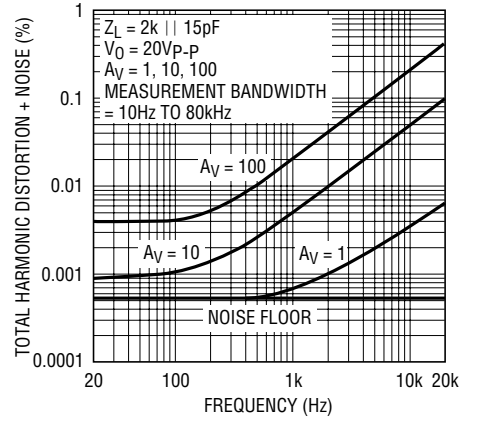
Capacitive Load Handling



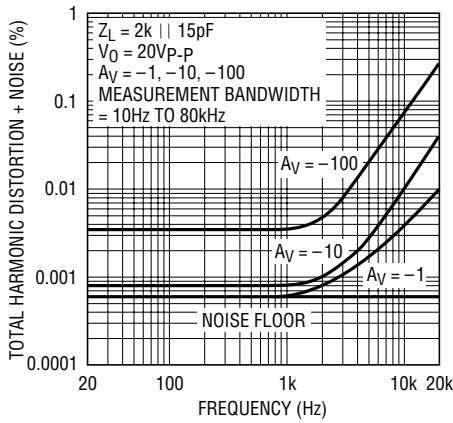
Warm-Up Drift



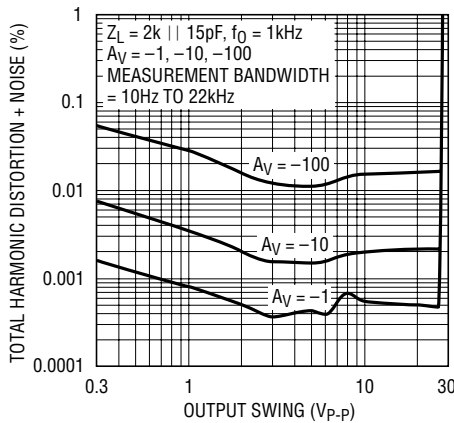
THD and Noise Frequency for Noninverting Gain



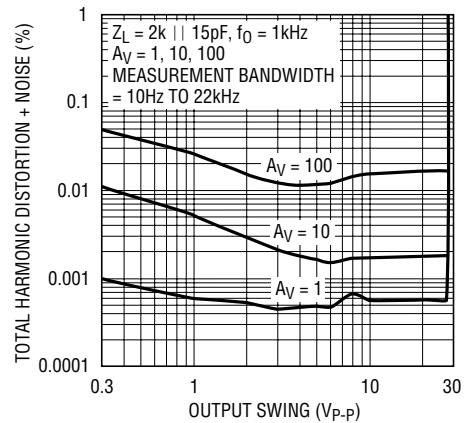
THD and Noise vs Frequency for Inverting Gain



THD and Noise vs Output Amplitude for Inverting Gain

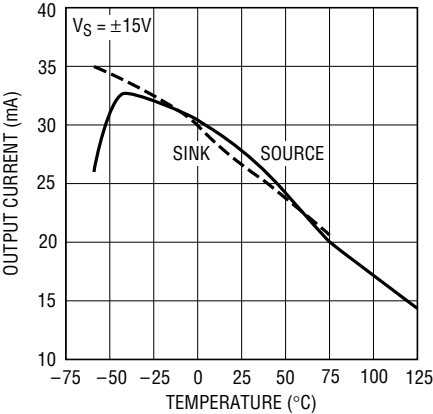


THD and Noise vs Output Amplitude for Noninverting Gain



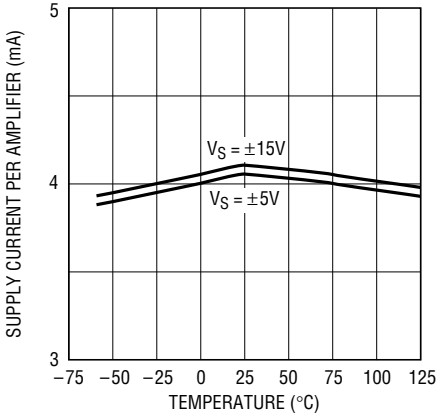
TYPICAL PERFORMANCE CHARACTERISTICS

Short-Circuit Output Current vs Temperature



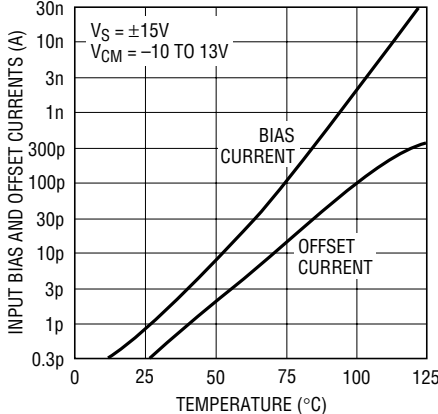
1793 G19

Supply Current vs Temperature



1793 G20

Input Bias and Offset Currents vs Chip Temperature



1793 G21

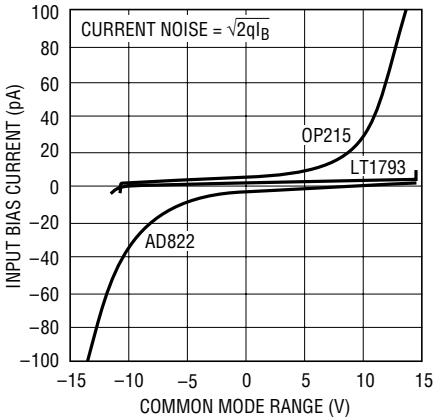
APPLICATIONS INFORMATION

LT1793 vs the Competition

With improved noise performance, the LT1793 in the PDIP directly replaces such JFET op amps as the OPA111 and the AD645. The combination of low current and voltage noise of the LT1793 allows it to surpass most dual and single JFET op amps. The LT1793 can replace many of the lowest noise bipolar amps that are used in amplifying low level signals from high impedance transducers. The best bipolar op amps (with higher current noise) will eventually lose out to the LT1793 when transducer impedance increases.

The extremely high input impedance ($10^{13}\Omega$) assures that the input bias current is almost constant over the entire common mode range. Figure 1 shows how the LT1793 stands up to the competition. Unlike the competition, as the input voltage is swept across the entire common mode range the input bias current of the LT1793 hardly changes. As a result the current noise does not degrade. This makes the LT1793 the best choice in applications where an amplifier has to buffer signals from a high impedance transducer.

Offset nulling will be compatible with these devices with the wiper of the potentiometer tied to the negative supply (Figure 2a). No appreciable change in offset voltage drift



1793 F01

Figure 1. Comparison of LT1793, OP215, and AD822 Input Bias Current vs Common Mode Range

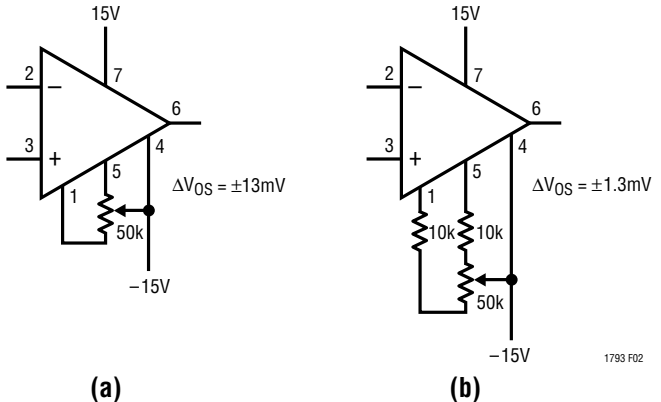


Figure 2

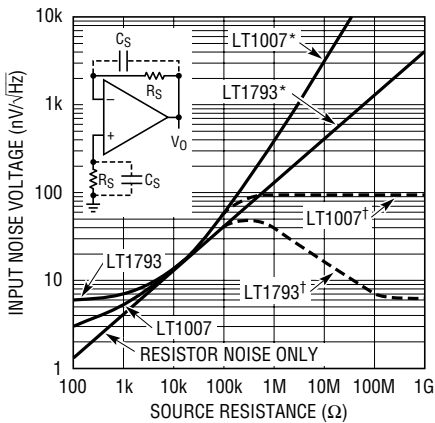
APPLICATIONS INFORMATION

with temperature will occur when the device is nulled with a potentiometer ranging from 10k to 200k. Finer adjustments can be made with resistors in series with the potentiometer (Figure 2b).

Amplifying Signals from High Impedance Transducers

The low voltage and current noise offered by the LT1793 makes it useful in a wide range of applications, especially where high impedance, capacitive transducers are used such as hydrophones, precision accelerometers and photodiodes. The total output noise in such a system is the gain times the RMS sum of the op amp's input referred

voltage noise, the thermal noise of the transducer, and the op amp's input bias current noise times the transducer impedance. Figure 3 shows total input voltage noise versus source resistance. In a low source resistance (<5k) application the op amp voltage noise will dominate the total noise. This means the LT1793 is superior to most JFET op amps. Only the lowest noise bipolar op amps have the advantage at low source resistances. As the source resistance increases from 5k to 50k, the LT1793 will match the best bipolar op amps for noise performance, since the thermal noise of the transducer (4kTR) begins to dominate the total noise. A further increase in source resistance, above 50k, is where the op amp's current noise component (2qI_BR²) will eventually dominate the total noise. At these high source resistances, the LT1793 will out perform the lowest noise bipolar op amps due to the inherently low current noise of FET input op amps. Clearly, the LT1793 will extend the range of high impedance transducers that can be used for high signal-to-noise ratios. This makes the LT1793 the best choice for high impedance, capacitive transducers.



SOURCE RESISTANCE = 2R_S = R
 * PLUS RESISTOR
 † PLUS RESISTOR || 1000pF CAPACITOR
 $V_n = A_V \sqrt{V_n^2(\text{OP AMP}) + 4kTR + 2qI_B R^2}$

Figure 3. Comparison of LT1793 and LT1007 Total Output 1kHz Voltage Noise vs Source Resistance

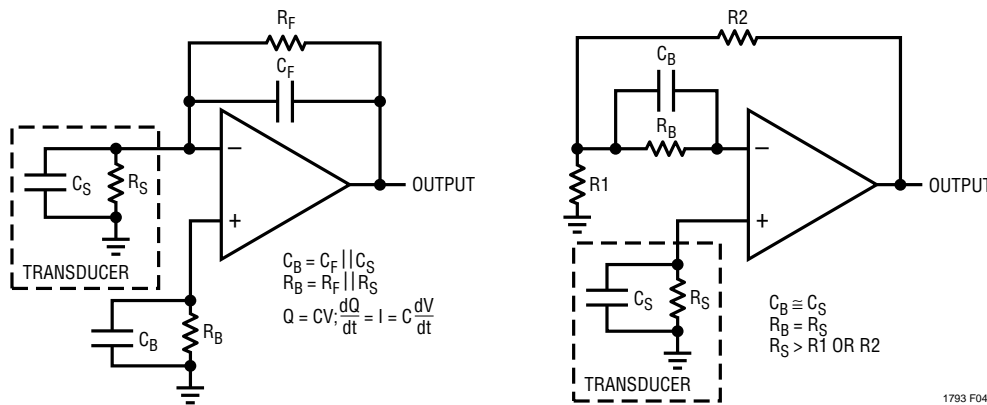


Figure 4. Inverting and Noninverting Gain Configurations

APPLICATIONS INFORMATION

resulting in a change in voltage dV , which is equal to dQ/C_F . The gain therefore is C_F/C_S . For unity-gain, the C_F should equal the transducer capacitance plus the input capacitance of the LT1793 and R_F should equal R_S .

In the noninverting mode example, the transducer current is converted to a change in voltage by the transducer capacitance, C_S . This voltage is then buffered by the LT1793 with a gain of $1 + R1/R2$. A DC path is provided by R_S , which is either the transducer impedance or an external resistor. Since R_S is usually several orders of magnitude greater than the parallel combination of $R1$ and $R2$, R_B is added to balance the DC offset caused by the noninverting input bias current and R_S . The input bias currents, although small at room temperature, can create significant errors at higher temperature, especially with transducer resistances of up to 1000M or more. The optimum value

for R_B is determined by equating the thermal noise ($4kTR_S$) to the current noise ($2qI_B$) times R_S^2 . Solving for R_S results in $R_B = R_S = 2V_T/I_B$ ($V_T = 26mV$ at $25^\circ C$). A parallel capacitor C_B , is used to cancel the phase shift caused by the op amp input capacitance and R_B .

Reduced Power Supply Operation

To take full advantage of a wide input common mode range, the LT1793 was designed to eliminate phase reversal. Referring to the photographs in Figure 5, the LT1793 is shown operating in the follower mode ($A_V = 1$) at $\pm 5V$ supplies with the input swinging $\pm 5.2V$. The output of the LT1793 clips cleanly and recovers with no phase reversal. This has the benefit of preventing lockup in servo systems and minimizing distortion components.

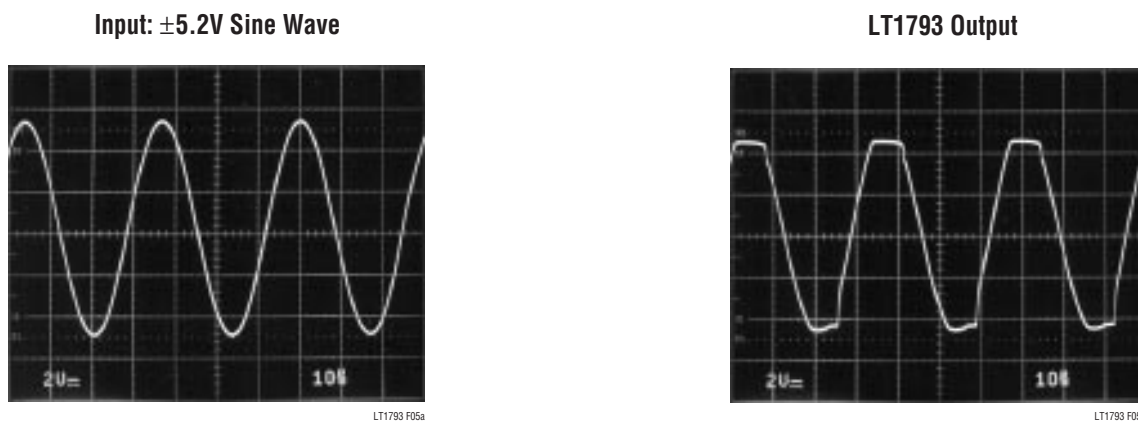
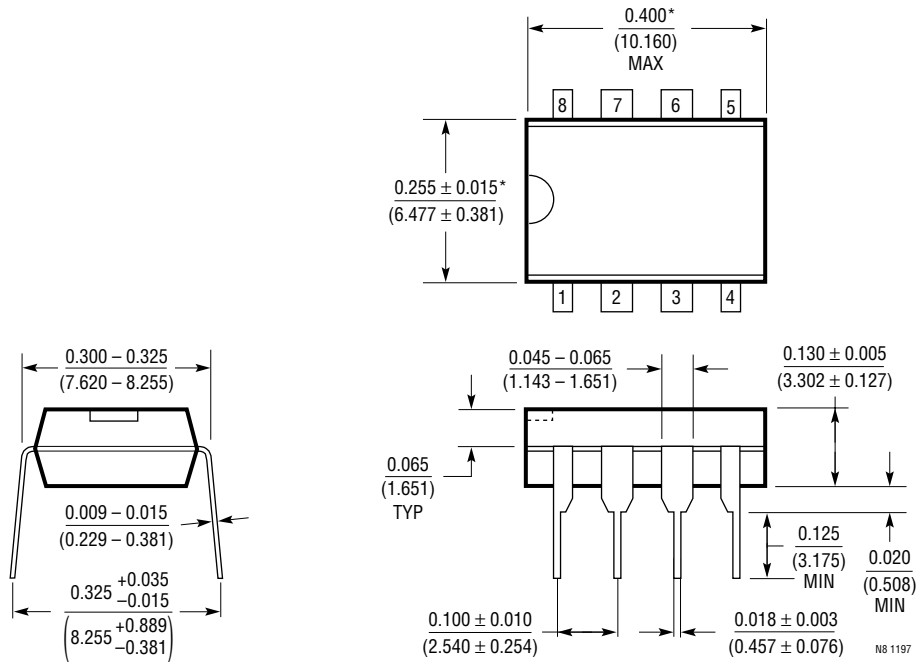


Figure 5. Voltage Follower with Input Exceeding the Common Mode Range ($V_S = \pm 5V$)

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

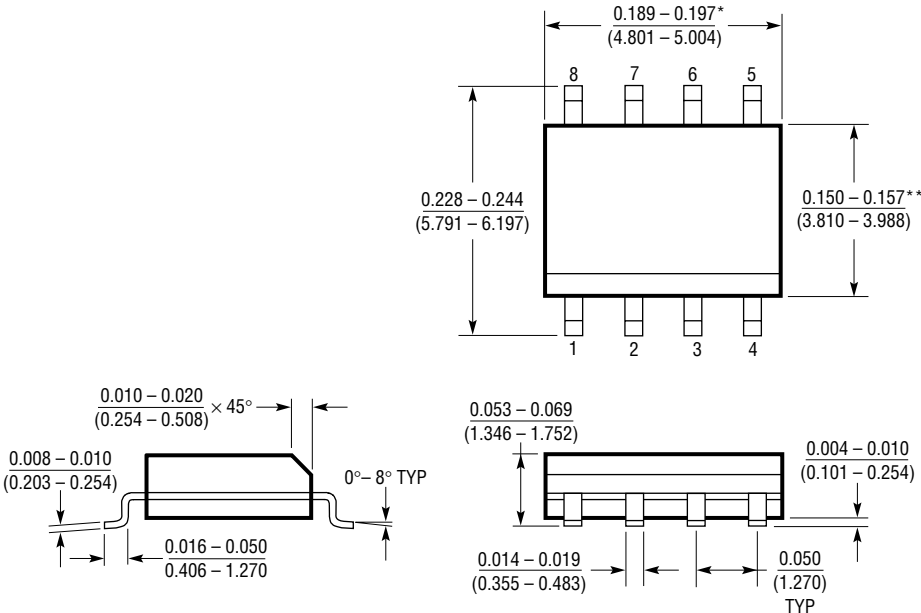
N8 Package
8-Lead PDIP (Narrow 0.300)
 (LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
 MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
 (LTC DWG # 05-08-1610)

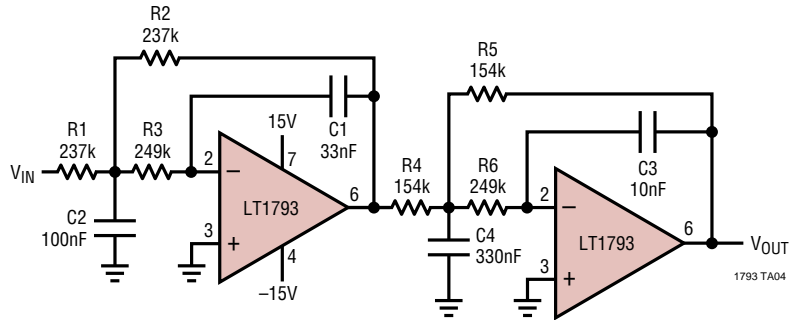


*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
 **DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S08 0996

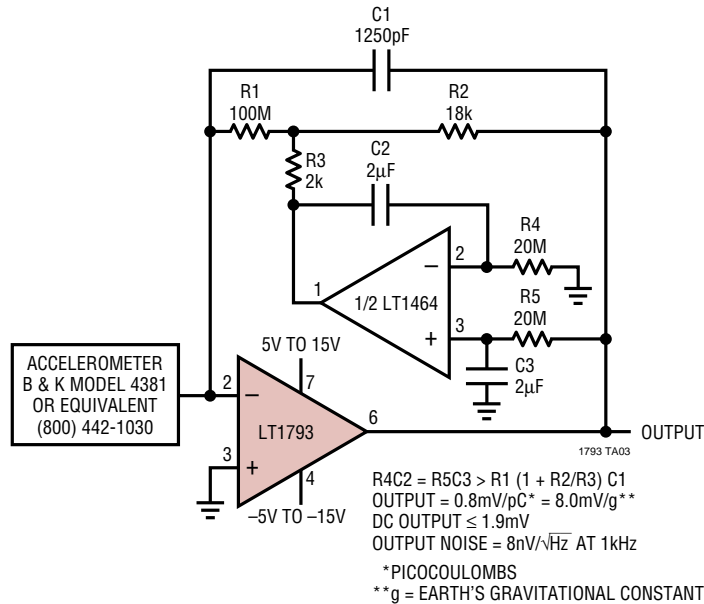
TYPICAL APPLICATIONS

10Hz Fourth Order Chebyshev Lowpass Filter (0.01dB Ripple)



TYPICAL OFFSET \approx 0.8mV
 1% TOLERANCES
 FOR $V_{IN} = 10V_{P-P}$, $V_{OUT} = -121dB$ AT $f > 330Hz$
 $= -6dB$ AT $f = 16.3Hz$
 LOWER RESISTOR VALUES WILL RESULT IN LOWER THERMAL NOISE AND LARGER CAPACITORS

Accelerometer Amplifier with DC Servo



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1113	Low Noise, Dual JFET Op Amp	Dual Version of LT1792, $V_{NOISE} = 4.5nV/\sqrt{Hz}$
LT1169	Low Noise, Dual JFET Op Amp	Dual Version of LT1793, $V_{NOISE} = 6nV/\sqrt{Hz}$, $I_B = 10pA$
LT1467	Micropower Dual JFET Op Amp	1MHz, 2pA Max I_B , 200uA Max I_S
LT1792	Low Noise, Single JFET Op Amp	Lower V_{NOISE} Version of LT1793, $V_{NOISE} = 4.2nV/\sqrt{Hz}$

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