THE DATASHEET OF

LT3641IUFD#TRPBF

Dual Monolithic Buck Regulator with Power-On Reset and Watchdog Timer

FEATURES

- **High Voltage Buck Regulator:**
  4V to 42V Operating Range
  1.3A Output Current
- **Input Transient Protection to 55V**
- **Low Voltage Synchronous Buck Regulator:**
  2.5V to 5.5V Input Voltage Range
  1.1A Output Current
- **Synchronizable, Adjustable 350kHz to 2.5MHz Switching Frequency**
- **Programmable Power-On Reset Timer**
- **Programmable Window Mode Watchdog Timer**
- Typical Quiescent Current: 290µA
- Short-Circuit Robust
- Programmable Soft-Start
- Low Shutdown Current: I_Q < 1µA
- Thermal Shutdown
- Available in Thermally Enhanced 28-Lead (4mm × 5mm) QFN and 28-Lead TSSOP Packages

APPLICATIONS

- Industrial Power Supplies
- Automotive Electronic Control Units

DESCRIPTION

The LT®3641 is a dual channel, current mode monolithic buck switching regulator with a power-on reset and a watchdog timer. Both regulators are synchronized to a single oscillator with an adjustable frequency (350kHz to 2.5MHz). At light loads, both regulators operate in low ripple Burst Mode® to maintain high efficiency and low output ripple.

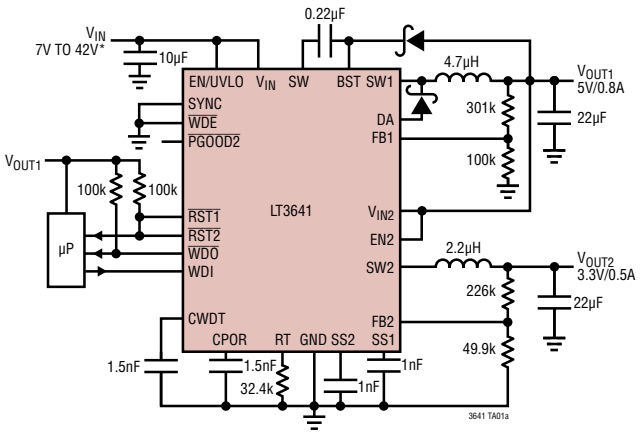
The high voltage channel is a nonsynchronous buck with an internal 2.4A top switch that operates from an input of 4V to 42V and input transient protection to 55V. The low voltage channel operates from an input of 2.5V to 5.5V. Internal synchronous power switches provide high efficiency without the need of external Schottky diode. Both channels have cycle-by-cycle current limit, providing protection against shorted outputs.

The power-on reset and watchdog timeout periods are both adjustable using external capacitors. The window mode watchdog timer flags when the µP pulses group too close together or too far apart.

The LT3641 is available in a 28-pin 4mm × 5mm QFN package and 28-pin TSSOP package. Both packages have an exposed pad for low thermal resistance.

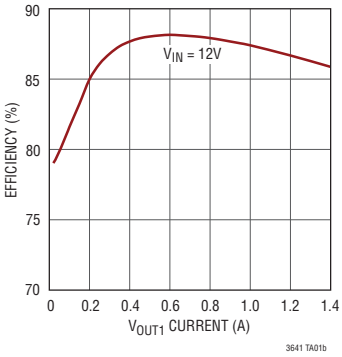
TYPICAL APPLICATION

2MHz 5V/0.8A and 3.3V/0.5A Step Down Regulators

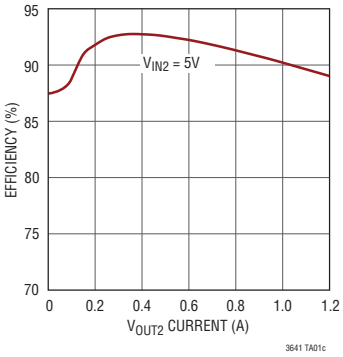


* FOR INPUT VOLTAGES ABOVE 42V RESTRICTIONS APPLY

HV Channel Efficiency, 2MHz, V_{OUT1} = 5V



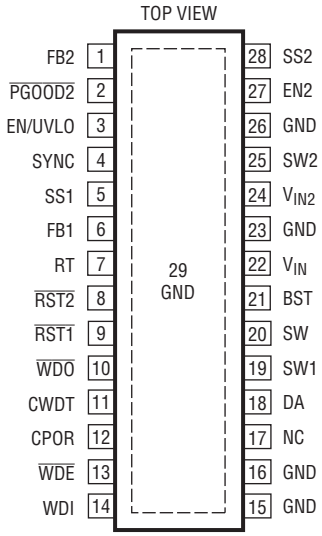
LV Channel Efficiency, 2MHz, V_{OUT2} = 3.3V



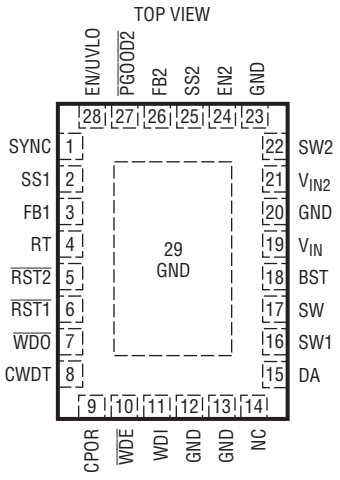
ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{IN}, EN/UVLO Voltage (Note 7) 55V
$\overline{WDE}$ Voltage 30V
BST Above SW, SW1 Voltage ..... –0.3V to 6V
SW1 Above SW Voltage ..... –0.3V to 6V
V_{IN2}, SYNC, EN2, $\overline{PGOOD2}$, WDI, $\overline{WDO}$, $\overline{RST1}$, $\overline{RST2}$, Voltages ..... –0.3V to 6V
SS1, SS2, FB1, FB2, RT, CWDT, CPOR Voltages ..... –0.3V to 2.5V
SW2 Voltage ..... –0.3V to (V_{IN2} + 0.3V)
Operating Junction Temperature Range (Note 2)
LT3641E ..... –40°C to 125°C
LT3641I ..... –40°C to 125°C
LT3641H ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature, FE Only (Soldering, 10 sec) .... 300°C

PIN CONFIGURATION



FE PACKAGE
28-LEAD PLASTIC TSSOP
θ_{JA} = 30°C/W, θ_{JC} = 8°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN
θ_{JA} = 43°C/W, θ_{JC} = 3.4°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3641EFE#PBF	LT3641EFE#TRPBF	LT3641FE	28-Lead Plastic TSSOP	–40°C to 125°C
LT3641IFE#PBF	LT3641IFE#TRPBF	LT3641FE	28-Lead Plastic TSSOP	–40°C to 125°C
LT3641HFE#PBF	LT3641HFE#TRPBF	LT3641FE	28-Lead Plastic TSSOP	–40°C to 150°C
LT3641EUFD#PBF	LT3641EUFD#TRPBF	3641	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LT3641IUFD#PBF	LT3641IUFD#TRPBF	3641	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, V_{IN2} = 3.3V, EN/UVLO = 12V, EN2 = 3.3V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Undervoltage Lockout Threshold		●		3.6	4	V
V_{IN} Undervoltage Release Threshold		●		3.8	4.2	V
Quiescent Current from V_{IN}	EN/UVLO = 0.3V Not Switching			0.1 275	1 375	µA µA
EN/UVLO Threshold Voltage			1.2	1.26	1.3	V
EN/UVLO High Bias Current	EN/UVLO = Threshold + 60mV			2		µA
EN/UVLO Low Bias Current	EN/UVLO = Threshold – 60mV			0.1		µA
SYNC Input Frequency			0.35		2.5	MHz
SYNC Threshold Voltage			0.4	0.8	1	V
Switching Frequency	RT = 32.4k RT = 182k	● ●	1.75 450	2 500	2.35 550	MHz kHz
FB1 Voltage		●	1.24	1.265	1.29	V
FB1 Bias Current	FB1 = 1.265V			30	100	nA
FB1 Line Regulation	5V < V_{IN} < 30V			0.001		%/V
SW1 Minimum Off-Time				70	100	ns
SW1 V_{CESAT}	I_{SW1} = 800mA			400		mV
SW1 Leakage Current				0.1	1	µA
SW1 Current Limit	FB1 = 1V (Note 3) FB1 = 0.1V	●	2.2	2.8 1.8	3.4	A A
DA Current limit	FB1 = 1V (Note 4) FB1 = 0.1V	●	1.35	1.7 1	2.2	A A
BST Pin Current	I_{SW1} = 800mA			30	50	mA
Minimum BST-SW Voltage				2	2.7	V
V_{IN2} Minimum Operating Voltage		●		2.3	2.5	V
V_{IN2} Maximum Operating Voltage		●			5.5	V
EN2 Threshold	Rising	●	1.13	1.18	1.23	V
EN2 Hysteresis			50	80	110	mV
EN2 Bias Current	EN2 = EN2 Threshold			50	500	nA
FB2 Voltage		●	585	600	615	mV
FB2 Bias Current	FB2 = 0.6V			0	100	nA
FB2 Line Regulation	2.5V < V_{IN2} < 5.5V			0.01		%/V
SW2 PMOS Current Limit	(Note 5)	●	1.5	1.9	2.2	A
SW2 NMOS Current Limit	(Note 5)	●	1.2	1.6	2	A
SW2 PMOS $R_{DS(ON)}$	I_{SW2} = 0.5A (Note 6)			275		mΩ
SW2 NMOS $R_{DS(ON)}$	I_{SW2} = 0.5A (Note 6)			200		mΩ
ΔFB2 to Enable $\overline{PGOOD2}$			20	40	80	mV
ΔFB2 Hysteresis to Disable $\overline{PGOOD2}$			20	40	80	mV
$\overline{PGOOD2}$ Voltage	FB2 = 0.6V, $I_{\overline{PGOOD2}}$ = 1mA			200	320	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, V_{IN2} = 3.3V, EN/UVLO = 12V, EN2 = 3.3V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SS1, SS2 Charge Current	SS1 = 0.5V, SS2 = 0.5V		1.3	2.0	2.7	µA
SS1 to FB1 Offset Voltage	SS1 = 0.6V			5	30	mV
SS2 to FB2 Offset Voltage	SS2 = 0.3V			5	30	mV
$\overline{RST1}$ Threshold as Percentage of V_{FB1}		●	90	92	94	%
$\overline{RST2}$ Threshold as Percentage of V_{FB1}		●	88	91	94	%
Undervoltage to $\overline{RST}$ Assert Time				20		µs
$\overline{RST1}$, $\overline{RST2}$, $\overline{WDO}$ Pull-Up Current	$\overline{RST1}$, $\overline{RST2}$, $\overline{WDO}$ = 0V		5	15	30	µA
$\overline{RST1}$, $\overline{RST2}$, $\overline{WDO}$ Output Voltage	$I_{\overline{RST1}}$, $I_{\overline{RST2}}$, $I_{\overline{WDO}}$ = 2mA			150	250	mV
$\overline{RST1}$, $\overline{RST2}$ Timeout Period (t_{RST})	CPOR = 220pF	●	8	9.5	11	ms
Watchdog Start Delay Time (t_{DLY})	CWDT = 820pF		14	16	18	ms
Watchdog Upper Boundary (t_{WDU})	CWDT = 820pF	●	27	32	35	ms
Watchdog Lower Boundary (t_{WDL})	CWDT = 820pF	●	1.68	2	2.2	ms
WDI Pull-Up Current	WDI = 1.2V			4		µA
WDI Voltage Threshold			0.55	0.85	1.15	V
WDI Low Minimum Pulse Width			300			ns
WDI High Minimum Pulse Width			300			ns
$\overline{WDE}$ Pull-Down Current	$\overline{WDE}$ = 2V			1		µA
$\overline{WDE}$ Threshold		●	0.5	0.7	0.9	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3641E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3641I is guaranteed and tested over the full –40°C to 125°C operating junction temperature range. The LT3641H is guaranteed and tested over the full –40°C to 150°C operating junction temperature range.

Note 3: SW1, SW2 current limit is guaranteed by design and/or correlation to static test. Slope compensation reduces current limit at higher duty cycle.

Note 4: The oscillator cycle is extended when DA current exceeds its limit. DA current limit is flat over duty cycle.

Note 5: If the SW2 NMOS current exceeds its limit at the start of an oscillator cycle, the PMOS will not be turned on in the cycle.

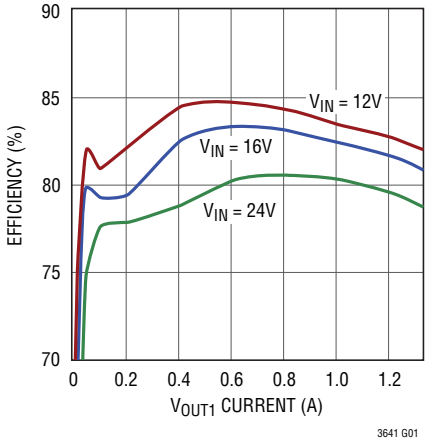
Note 6: The QFN switch $R_{DS(ON)}$ is guaranteed by correlation to wafer level measurement.

Note 7: Absolute Maximum Voltage at V_{IN} and EN/UVLO pins is 55V for nonrepetitive 1 second transients, and 42V for continuous operation.

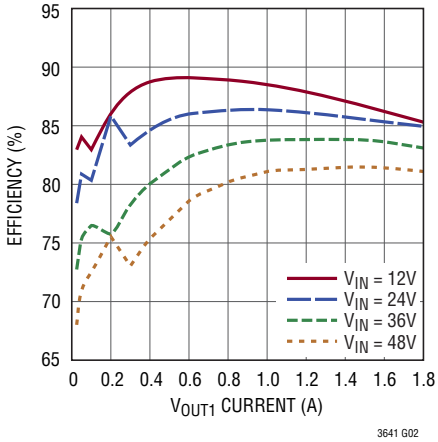
Note 8: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

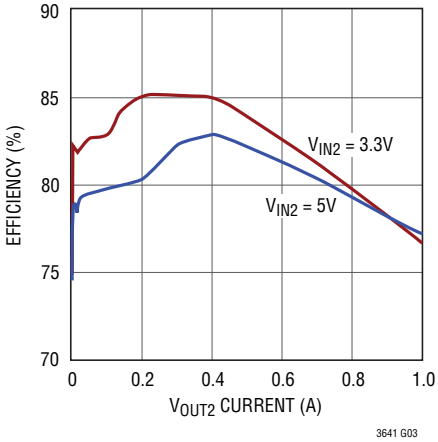
HV Channel Efficiency (2MHz, V_{OUT1} = 3.3V)



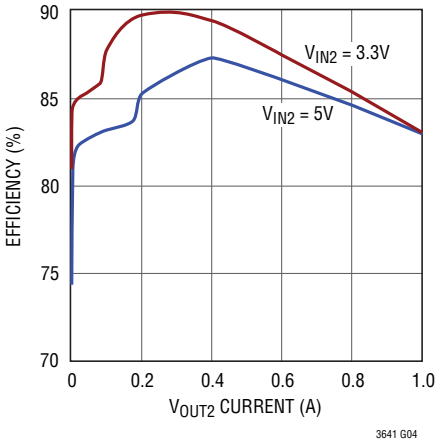
HV Channel Efficiency (2MHz, V_{OUT1} = 5V)



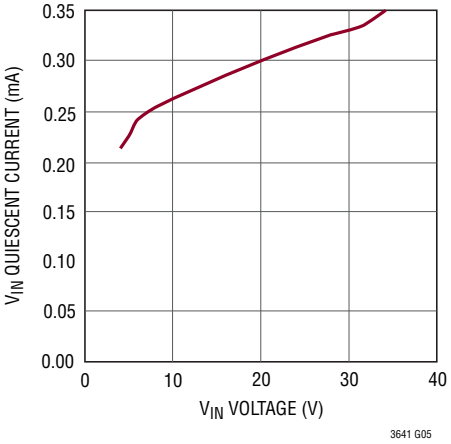
LV Channel Efficiency (2MHz, V_{OUT2} = 1.2V)



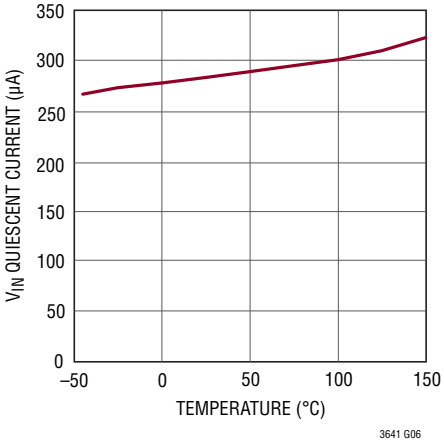
LV Channel Efficiency (2MHz, V_{OUT2} = 1.8V)



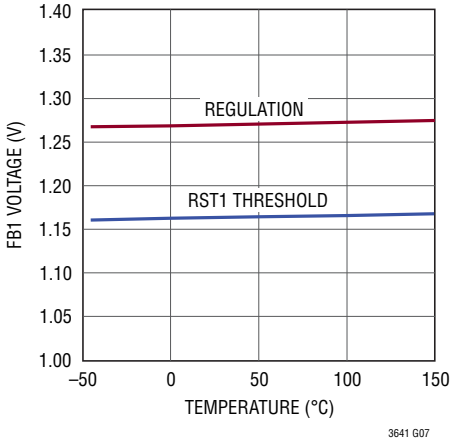
Quiescent Current vs V_{IN}



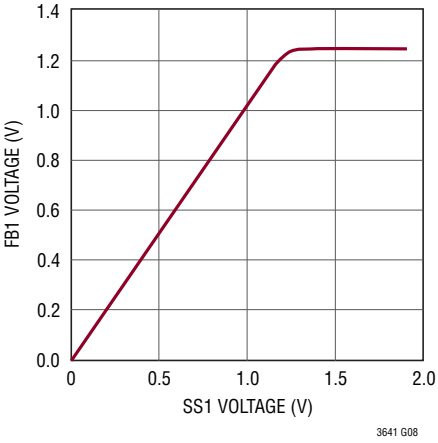
Quiescent Current vs Temperature



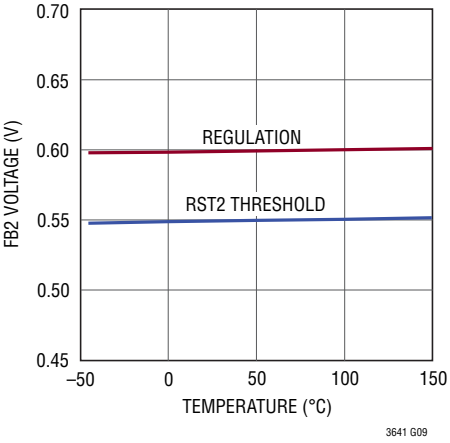
FB1 Voltage vs Temperature



FB1 Voltage vs SS1

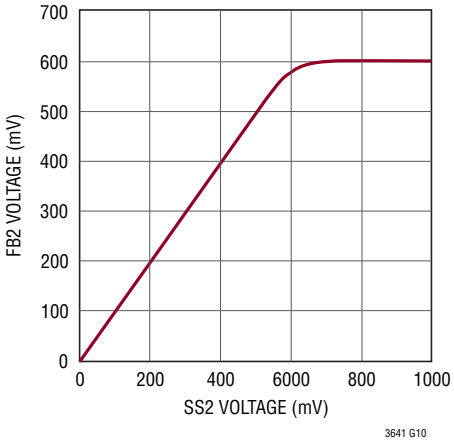


FB2 Voltage vs Temperature

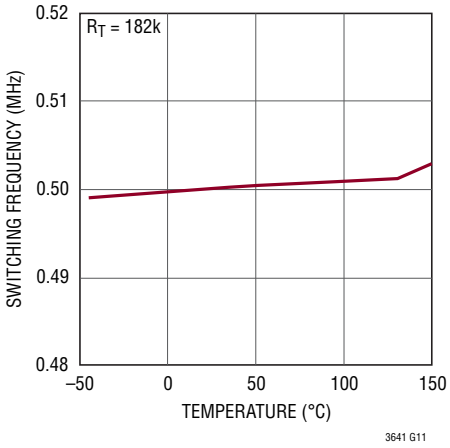


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

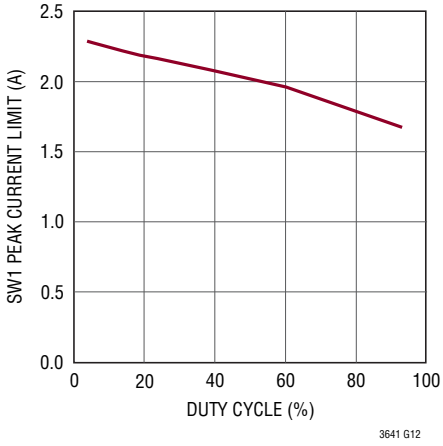
FB2 Voltage vs SS2



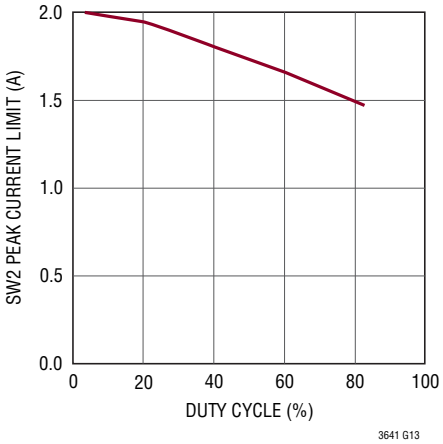
Switching Frequency vs Temperature



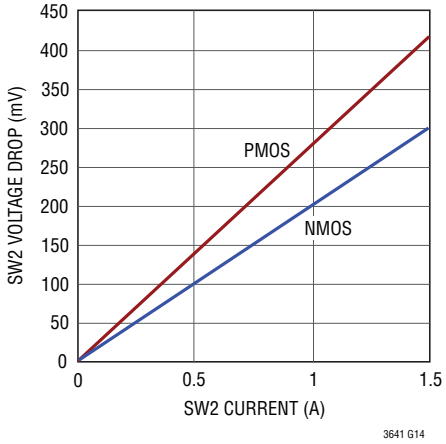
HV Channel Current Limit vs Duty Cycle



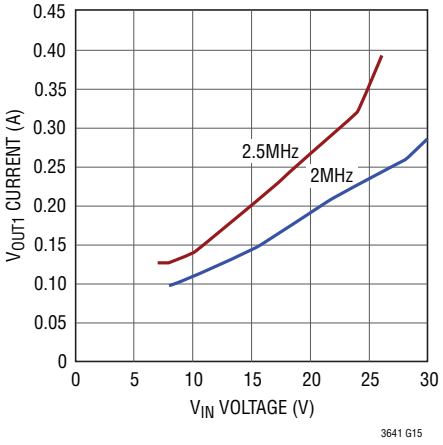
LV Channel Peak Current Limit vs Duty Cycle



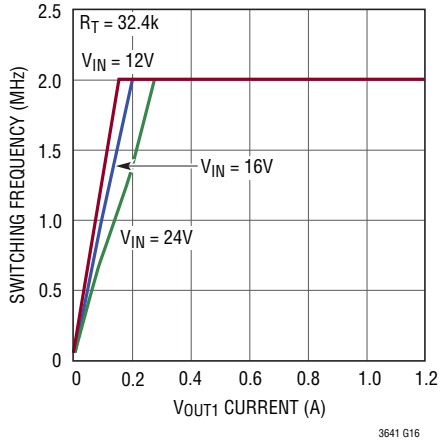
LV Channel Switch Voltage Drop vs Current (V_{IN2} = 3.3V)



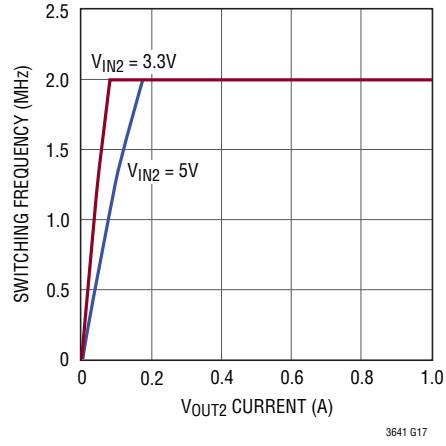
V_{OUT1} Minimum Load to Run at Full Frequency (V_{OUT1} = 3.3V)



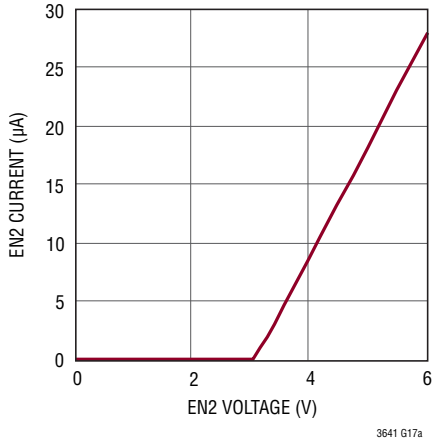
HV Channel Switching Frequency (V_{OUT1} = 3.3V)



LV Channel Switching Frequency (V_{OUT2} = 1.8V)

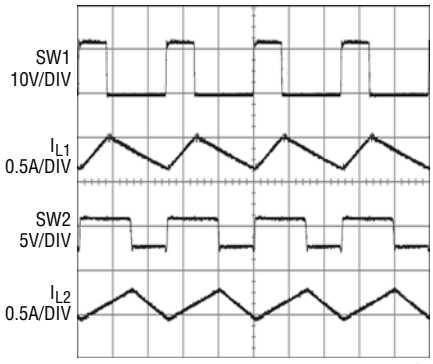


EN2 Current vs Voltage



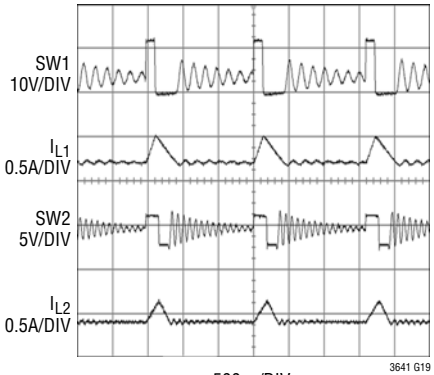
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Full Frequency Waveforms



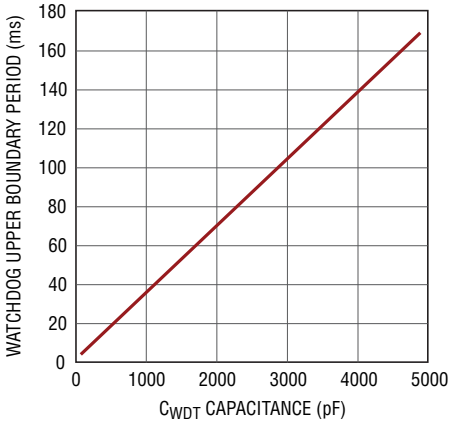
V_{IN1} = 12V $V_{IN2} = V_{OUT1}$
V_{OUT1} = 3.3V/0.5A V_{OUT2} = 1.8V/0.5A

Light Load Operation Waveforms

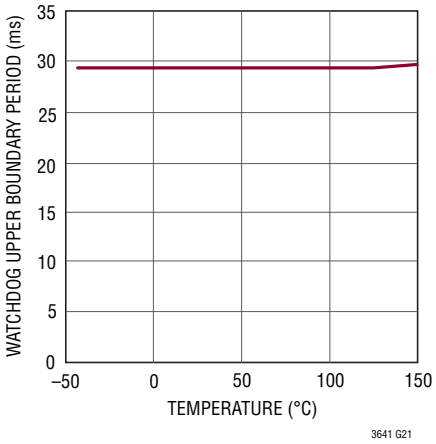


V_{IN1} = 12V $V_{IN2} = V_{OUT1}$
V_{OUT1} = 3.3V/25mA V_{OUT2} = 1.8V/30mA

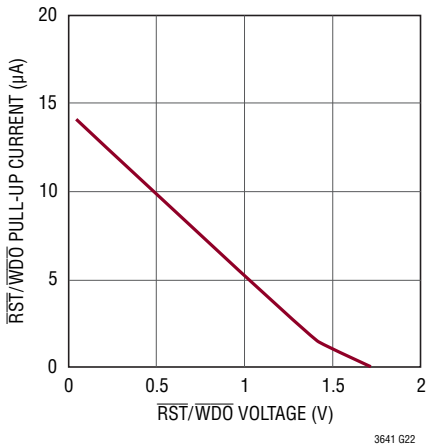
Watchdog Upper Boundary Period vs C_{WDT}



Watchdog Upper Boundary Period vs Temperature



$\overline{RST}/\overline{WDO}$ Pull-Up Current



PIN FUNCTIONS (FE/QFN)

FB2 (Pin 1/Pin 26): The low voltage converter regulates the FB2 pin to 600mV. Connect the feedback resistor divider tap to this pin to set output voltage.

$\overline{\text{PGOOD2}}$ (Pin 2/Pin 27): Open-drain logic output that starts to sink current when FB2 is in regulation.

EN/UVLO (Pin 3/Pin 28): Pull this pin below 0.3V to shut down the LT3641. The 1.26V threshold can function as an accurate undervoltage lockout, preventing the LT3641 from operating until V_{IN} voltage has reached the programmed level.

SYNC (Pin 4/Pin 1): Driving the SYNC pin with an external clock signal synchronizes both converters to the applied frequency. The lowest external clock frequency should be 20% higher than the internal oscillator frequency.

SS1 (Pin 5/Pin 2): The SS1 pin sets the FB1 voltage externally between 0V and 1.265V, providing soft-start and tracking. Tie this pin 1.5V or higher to use the internal 1.265V reference. A capacitor to ground at this pin sets the ramp time to regulated output voltage for the high voltage converter. Use a resistor divider to track another supply.

FB1 (Pin 6/Pin 3): The high voltage converter regulates the FB1 pin to 1.265V. Connect the feedback resistor divider tap to this pin to set output voltage.

RT (Pin 7/Pin 4): Oscillator Resistor Input. Connecting a resistor to ground from this pin sets the internal oscillator frequency.

$\overline{\text{RST2}}$ (Pin 8/Pin 5): Open-drain logic output that remains asserted for the period set by the CPOR pin capacitor after FB2 goes above 550mV.

$\overline{\text{RST1}}$ (Pin 9/Pin 6): Open-drain logic output that remains asserted for the period set by the CPOR pin capacitor after FB1 goes above 1.165V.

$\overline{\text{WDO}}$ (Pin 10/Pin 7): Open-drain logic output that remains asserted for the period set by the CPOR pin capacitor if $\overline{\text{WDE}}$ is enabled and WDI pin is not driven by an appropriate signal.

CWDT (Pin 11/Pin 8): Connect a capacitor to ground at this pin to set watchdog timer.

CPOR (Pin 12/Pin 9): Connect a capacitor to ground at this pin to set the power-on reset timer and $\overline{\text{WDO}}$ output timer.

$\overline{\text{WDE}}$ (Pin 13/Pin 10): Watchdog Enable Pin.

WDI (Pin 14/Pin 11): The WDI pin receives watchdog signals from a microprocessor.

GND (Pins 15, 16, 23, 26, Exposed Pad Pin 29/Pins 12, 13, 20, 23, Exposed Pad Pin 29): Ground. These pins must be soldered to PCB ground.

NC (Pin 17/Pin 14): Not Connected. This pin can be connected to ground.

DA (Pin 18/Pin 15): The DA pin is used to sense the catch diode current for current limit and protection. Connect this pin to catch diode anode.

SW1 (Pin 19/Pin 16): Output of the High Voltage Internal Power Switch. Connect this pin to the inductor and catch diode cathode.

SW (Pin 20/Pin 17): The SW pin is used to charge the boost capacitor. Connect this pin to the boost capacitor.

BST (Pin 21/Pin 18): The BST pin is used to provide a drive voltage, higher than V_{IN} pin voltage, to the high voltage channel internal power switch. Connect an external boost diode to this pin.

V_{IN} (Pin 22/Pin 19): The V_{IN} pin supplies current to the LT3641's internal circuitry and to the high voltage channel internal power switch. This pin must be locally bypassed.

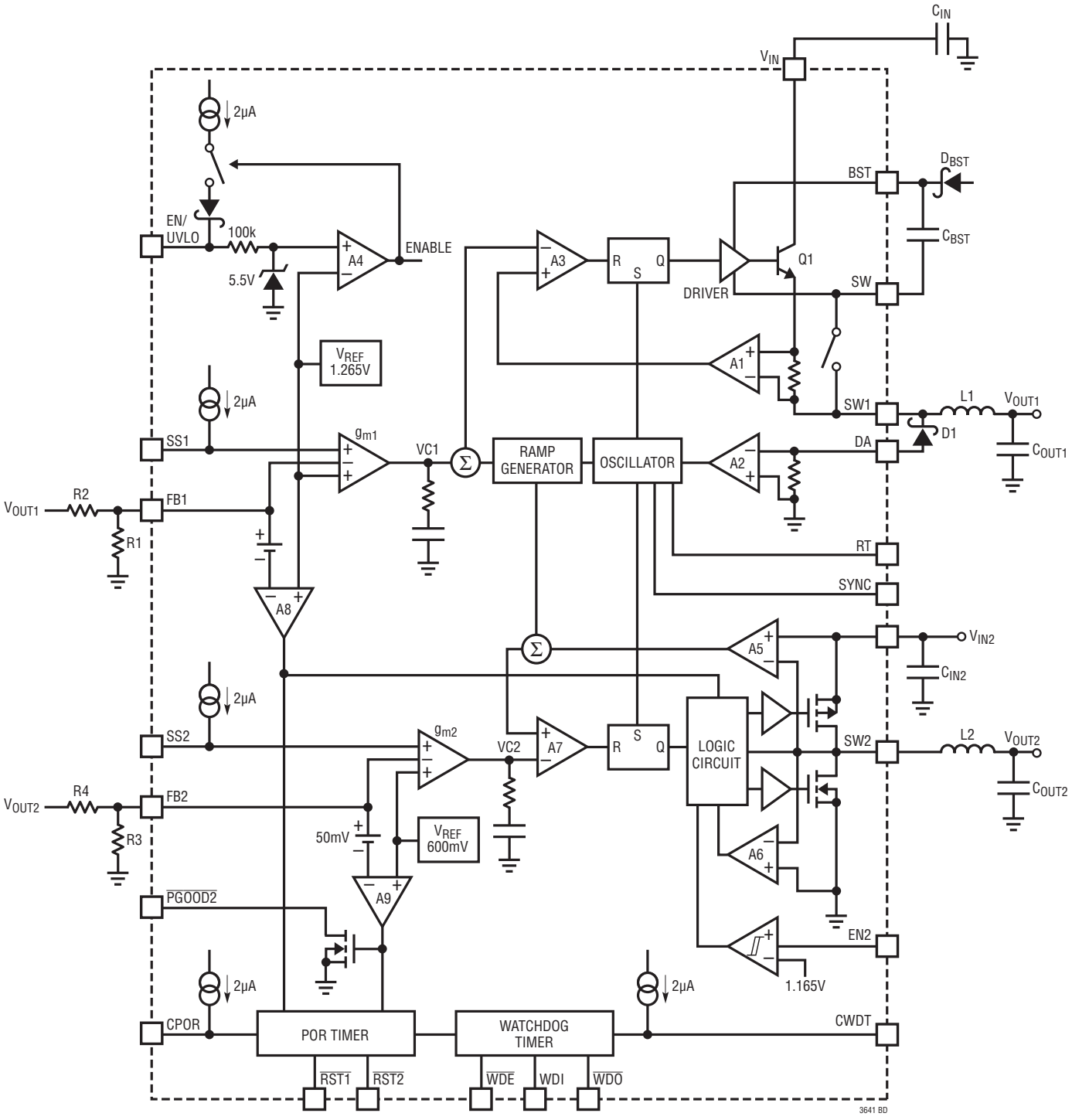
V_{IN2} (Pin 24/Pin 21): The V_{IN2} pin supplies current to the internal power MOSFET of the low voltage converter and to the LT3641's internal circuitry when V_{IN2} is above 3V.

SW2 (Pin 25/Pin 22): Switch Node of the Low Voltage Converter. Connect this pin to an inductor.

EN2 (Pin 27/Pin 24): Low Voltage Converter Enable Pin. The enable threshold is 100mV below FB1 target voltage. The disable threshold has 50mV hysteresis. The accurate threshold can function as an accurate undervoltage lockout.

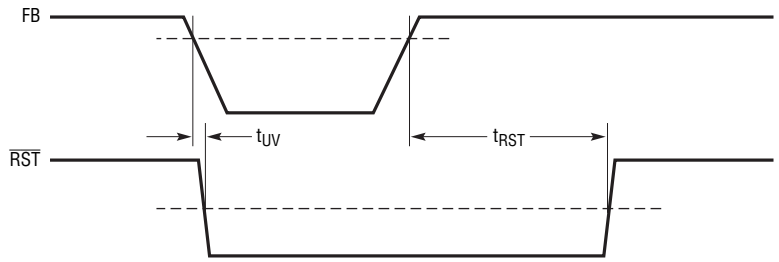
SS2 (Pin 28/Pin 25): The SS2 pin sets the FB2 voltage externally between 0V and 0.6V, providing soft-start and tracking. Tie this pin 0.8V or higher to use the internal 0.6V reference. A capacitor to ground at this pin sets the ramp time to regulated output voltage for the low voltage converter. Use a resistor divider to track another supply.

BLOCK DIAGRAM

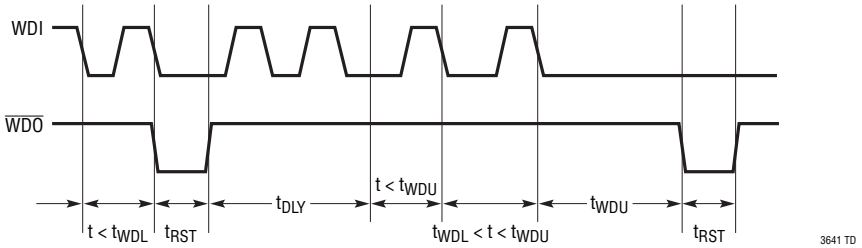


TIMING DIAGRAMS

Power-On Reset Timing



Watchdog Timing



OPERATION

The LT3641 is a dual channel, constant-frequency, current mode monolithic buck switching regulator with power-on reset and watchdog timer. Both channels are synchronized to a single oscillator with frequency set by RT. Operation can be best understood by referring to the Block Diagram.

Buck Regulators

The high voltage channel is a nonsynchronous buck regulator that operates from the V_{IN} pin. The start of each oscillator cycle sets an SR latch and turns on the internal NPN power switch. An amplifier and comparator monitor the current flowing between the V_{IN} and SW1 pins, turning the switch off when this current reaches a level determined by the voltage at VC1 node. An error amplifier measures the output voltage through an external resistor divider tied to the FB1 pin and servos the VC1 node. The reference of the error amplifier is determined by the lower of the internal reference and the voltage at the SS1 pin. If the error amplifier's output increases, more current is delivered to the output; if it decreases, less current is delivered.

An active clamp (not shown) on the VC1 node provides peak current limit. A DA pin current comparator extends the oscillator cycle until the catch diode current is below the valley current limit. Both the peak and valley current limits help to control the inductor current in fault conditions such as shorted output with high V_{IN}. Both current limits are reduced when the voltage at the FB1 pin is below 0.2V. This current foldback helps to control the inductor current during start-up and overload.

The NPN power switch driver operates from either the V_{IN} pin or the BST pin. An external capacitor and diode are used to generate a voltage between the BST and SW pins. During the power-up of the LT3641, an internal 5mA current source charges the external BST capacitor. The regulator starts switching when the (BST-SW) voltage reaches the 2V threshold. The internal NPN power switch can be fully saturated for efficient operation when the (BST-SW) voltage is between 2.3V and 5.5V.

The low voltage channel is a synchronous buck regulator that operates from the V_{IN2} pin. It starts switching only

OPERATION

when the V_{IN2} pin voltage is above 2.3V, and the EN2 pin is above its threshold. The internal top power MOSFET is turned on each cycle at the beginning of each oscillator cycle, and turned off when the current flowing through the top MOSFET reaches a level determined by the voltage at the VC2 node. An error amplifier measures the output voltage through an external resistor divider tied to the FB2 pin and servos the VC2 node. The reference of the error amplifier is determined by the lower of the internal 600mV reference and the voltage at the SS2 pin.

While the top MOSFET is off, the bottom MOSFET is turned on in an oscillator cycle until the inductor current starts to reverse. If the inductor current is higher than the valley current limit at the beginning of an oscillator cycle, the bottom MOSFET will remain on and prevent the top MOSFET from turning on until the overcurrent situation clears, limiting inductor current in shorted output fault.

An internal regulator provides power to the control circuitry. The regulator draws most power from the V_{IN2} pin and a small portion of power from the V_{IN} pin when the V_{IN2} pin voltage is higher than 3V. If the voltage at V_{IN2} pin is lower than 3V, the regulator draws all power from the V_{IN} pin.

The EN/UVLO pin is used to put the LT3641 in shutdown, reducing the input current to less than 1µA. The accurate 1.26V threshold of the EN/UVLO pin provides a programmable V_{IN} undervoltage lockout through an external resistor divider tied to the EN/UVLO pin. A 2µA hysteresis current on the EN/UVLO pin prevents switching noise from shutting down the LT3641.

The LT3641 has an overtemperature protection feature which disables switching in both channels when the junction temperature exceeds the overtemperature threshold. Junction temperature will exceed the maximum operating junction when overtemperature protection is active.

Internal 2µA current sources charge the SS1 pin and the SS2 pin up to about 2V. Soft-start or output voltage tracking of the two channels can be independently implemented with capacitors from the SS1 pin and the SS2 pin to ground. Any undervoltage condition on the V_{IN} pin triggers an internal latch that discharges the SS1 pin to below 100mV before it is released. If the EN2 pin goes below its threshold, or the V_{IN2} voltage falls below 2.2V, the SS2 pin will be discharged to below 100mV before it is released.

To optimize efficiency, the LT3641 switches to low ripple Burst Mode operation in light load situations. Between switching pulses, control-circuitry current is minimized.

A power good comparator with 40mV of hysteresis trips when the low voltage channel is enabled and the FB2 pin is above 550mV. The $\overline{PGOOD2}$ pin is an open-drain output that is pulled low when both the outputs are in regulation.

Power-On Reset and Watchdog Timer

The LT3641 includes one power-on reset timer for each buck regulator and one common watchdog timer. Power-on reset and watchdog timers are both adjustable using external capacitors. Operation can be best understood by referring to the Timing Diagram.

The $\overline{RST1}$, $\overline{RST2}$ and $\overline{WDO}$ pins are all open-drain outputs with weak internal pull-ups to about 2V. The $\overline{RST1}$ and $\overline{RST2}$ pins are pulled low when the LT3641 is enabled and V_{IN} is above 3.6V. Once the FB1 pin rises above 1.165V, the high voltage channel reset timer is started and $\overline{RST1}$ is released after the reset timeout period. The low voltage channel reset timer is started once the FB2 pin rises above 550mV, and releases $\overline{RST2}$ after the reset timeout period.

The watchdog circuit monitors a µP's activity. As soon as $\overline{RST2}$ is released, a delay timer is started. The watchdog timer is started after the delay timer times out. The LT3641 implements windowed watchdog function for higher system reliability. The watchdog timer detects falling edges on the WDI pin. If the falling edges are grouped too close together or too far apart, the $\overline{WDO}$ pin is pulled down and the reset timer is started. When the reset timer times out, $\overline{WDO}$ is released and the watchdog timer is again started after the delay period.

APPLICATIONS INFORMATION

Setting the Output Voltages

The internal reference voltage is 1.265V for the high voltage channel, and 600mV for the low voltage channel. The output voltages are set by resistor dividers according to the following formulas:

$$R2 = R1 \bullet \left(\frac{V_{OUT1}}{1.265V} - 1 \right)$$

$$R4 = R3 \bullet \left(\frac{V_{OUT2}}{0.6V} - 1 \right)$$

Use 1% resistors in the resistor dividers. To avoid noise problems, R1 should be 100k or less, and R3 should be 50k or less. Reference designators refer to the Block Diagram.

Switching Frequency

The LT3641 uses a constant-frequency PWM architecture that can be programmed to switch from 350kHz to 2.2MHz by using a resistor tied from the RT pin to ground. Table 1 shows the necessary R_T value for a desired switching frequency.

Table 1. Switching Frequency vs R_T Value

SWITCHING FREQUENCY (MHz)	R_T (k)
0.35	267
0.5	182
1	82.5
2	32.4
2.2	27.4

Selection of the operating frequency is mainly a trade-off between efficiency and component size. The advantage of high frequency operation is that smaller inductor and capacitor values may be used. The disadvantage is lower efficiency.

The high switching frequency also decreases the duty cycle range. The reason is that the LT3641 switches have finite minimum on- and off-times independent of the switching frequency. The top switch in the high voltage channel can turn on for a minimum of ~60ns and turn off for a minimum of ~70ns. The top switch in the low voltage channel can turn on for a minimum of ~110ns and turn off for a minimum of ~70ns. The minimum and maximum duty cycles are:

$$DC_{MIN} = f_S \bullet t_{ON(MIN)}$$

$$DC_{MAX} = 1 - f_S \bullet t_{OFF(MIN)}$$

where f_S is the switching frequency, $t_{ON(MIN)}$ is the minimum switch on-time, and $t_{OFF(MIN)}$ is the minimum switch off-time. These equations illustrate how duty cycle range increases when switching frequency decreases.

The internal oscillator of the LT3641 can be synchronized to an external 350kHz to 2.5MHz positive clock signal on the SYNC pin. The R_T value should be chosen such that the internal oscillator's frequency is 20% lower than the lowest SYNC clock frequency (refer to Table 1). To avoid erratic operation, the LT3641 ignores the SYNC signal until the FB1 pin voltage is above 1.165V. When applying a SYNC signal, the rising edges reset the LT3641's internal clock and initiate a switch cycle. The amplitude of the SYNC signal must be at least 2V. The SYNC pulse width must be at least 40ns.

V_{IN} Voltage Range

The LT3641's minimum operating voltage is 3.6V typical. A higher minimum operating voltage can be accurately programmed with a resistor divider between the V_{IN} pin and the EN/UVLO pin. The EN/UVLO threshold is 1.26V. When the LT3641 is enabled, a 2µA current flows out of the EN/UVLO pin generating hysteresis to prevent the switching action from falsely disabling the LT3641. Choose the divider resistances for appropriate hysteresis voltage.

APPLICATIONS INFORMATION

The high voltage nonsynchronous channel operates from the V_{IN} pin. The minimum V_{IN} voltage to regulate output voltage is:

$$V_{IN(MIN)} = \left(\frac{V_{OUT1} + V_D}{DC_{MAX}}\right) - V_D + V_{CE}$$

Where V_D is the forward voltage drop of the catch diode, V_{CE} is the voltage drop of the internal NPN power switch, and DC_{MAX} is the maximum duty cycle (refer to the Switching Frequency section). If V_{IN} is below the calculated minimum voltage, output will lose regulation.

The maximum V_{IN} should not exceed the absolute maximum rating. For fixed frequency operation, the maximum V_{IN} is:

$$V_{IN(MAX)} = \left(\frac{V_{OUT1} + V_D}{DC_{MIN}}\right) - V_D + V_{CE}$$

Note that the high voltage buck will still regulate at an input voltage that exceeds $V_{IN(MAX)}$ (up to 42V). It will continue to regulate through transients up to 55V for one second. Note that the switching frequency will be reduced once the on-time required to satisfy the above equation is below 50ns (Figure 1).

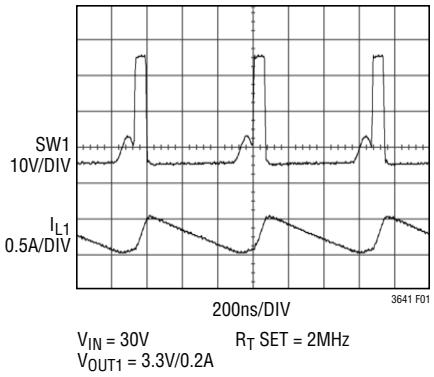


Figure 1. Lower Switching Frequency Occurs in High Voltage Channel When Required On-Time Is Below 50ns

V_{IN2} Voltage Range

The low voltage synchronous channel operates from the V_{IN2} pin. The V_{IN2} pin can be connected to either an independent voltage supply or the high voltage channel output for a two-stage power regulator. The V_{IN2} voltage range is 2.3V ~ 5.5V

The minimum V_{IN2} voltage to regulate output voltage at full frequency is:

$$V_{IN2(MIN)} \approx \frac{V_{OUT2}}{DC_{MAX}}$$

Where DC_{MAX} is the maximum duty cycle (refer to Switching Frequency section). If V_{IN2} is below the calculated minimum voltage, the low voltage channel starts to skip oscillator clock. In this case, the low voltage channel switching frequency will no longer be the programmed frequency. As the V_{IN2} voltage further decreases, the top MOSFET will remain on 100% duty cycle. In the case, the output starts to fall out of regulation.

The maximum V_{IN2} for fixed frequency operation is:

$$V_{IN2(MAX)} \approx \frac{V_{OUT2}}{DC_{MIN}}$$

Where DC_{MIN} is the minimum duty cycle (refer to the Switching Frequency section). For voltage that exceeds $V_{IN2(MAX)}$ (up to 5.5V), the low voltage channel exhibits pulse-skipping behavior, and the output ripple will increase.

Inductor Selection

Inductor selection involves inductance, saturation current, series resistance (DCR) and magnetic loss.

The inductance for the high voltage channel is:

$$L1 = 1.7 \bullet \frac{V_{OUT1} + V_D}{f_S}$$

APPLICATIONS INFORMATION

where V_{OUT1} is high voltage channel output voltage, V_D is the forward voltage drop of the catch diode, and f_S is the switching frequency. For example, 3.3µH is a reasonable inductance for a 3.3V output with 2MHz switching frequency.

Once the inductance is selected, the inductor current ripple and peak current can be calculated:

$$\Delta I_{L1} = \frac{(V_{OUT1} + V_D)}{L1 \bullet f_S} \bullet \left(1 - \frac{V_{OUT1} + V_D}{V_{IN}}\right)$$

$$I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

To guarantee sufficient output current, peak inductor current must be lower than the switch current limit (I_{LIM}). The largest inductor current ripple occurs at the highest V_{IN}. To guarantee current capacity, use $V_{IN(MAX)}$ in the above formula.

The inductance for the low voltage channel is:

$$L2 = 1.5\frac{V_{OUT2}}{f_S}$$

For a selected inductance, the inductor current ripple can be calculated:

$$\Delta I_{L2} = \frac{V_{OUT2}}{L2 \bullet f_S} \bullet \left(1 - \frac{V_{OUT2}}{V_{IN2}}\right)$$

For robust operation in fault conditions, the inductor saturation current should be higher than the upper limit of the corresponding top switch current limit.

To keep the efficiency high, the inductor series resistance (DCR) should be as small as possible (must be < 0.1Ω), and the core material should be intended for the chosen operation frequency. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores; instead use ferrite, molypermalloy or Kool Mµ cores. Table 2 lists several vendors and suitable inductor series.

Table 2. Inductor Vendors

VENDOR	WEBSITE
Murata	www.murata.com
TDK	www.tdk.com
TOKO	www.toko.com
Sumida	www.sumida.com
Cooper/Coiltronics	www.cooperindustries.com
Coilcraft	www.coilcraft.com
Vishay	www.vishay.com
NIC	www.niccomp.com
Würth Elektronik	www.we-online.com

Of course, such a simple design guide will not always result in the optimum inductors for the applications. A larger value inductor provides a slightly higher maximum load current and will reduce the output voltage ripple. A larger value inductor also results in higher efficiency in the condition of same DCR and same magnetic loss. However, for a same series of inductors, a larger value inductor has higher DCR. The trade-off between inductance and DCR is not always obvious. Use experiments to find optimum inductors.

Low inductance may result in discontinuous mode operation, which is okay, but reduces maximum load current. For details of maximum output current and discontinuous mode operation, see the Linear Technology Application Note 44. For duty cycles greater than 50%, there is a minimum inductance required to avoid subharmonic oscillations. See the Linear Technology Application Note 19.

Input Capacitor

Bypass the V_{IN} pin of the LT3641 with a ceramic capacitor of X7R (–55°C to 125°C) or X5R (–55°C to 85°C) type.

Buck converters draw pulse current from the input supply. The input capacitor is required to reduce the resulting voltage ripple. Use a ceramic capacitor with:

$$C_{IN} \geq \frac{10\mu F}{f_S}$$

where f_S in the switching frequency in MHz.

APPLICATIONS INFORMATION

A second precaution regarding the ceramic input capacitor concerns the maximum input voltage rating of the LT3641. A ceramic input capacitor combined with trace or cable inductance forms a under damped tank circuit. If the LT3641 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT3641's voltage rating. This situation can be easily avoided (see the Linear Technology Application Note 80).

Output Capacitors and Output Ripple

The output capacitor has two essential functions. In steady state, it determines the output voltage ripple. In transient, it stores energy in order to satisfy transient loads and stabilize the control loop. Ceramic capacitors have low equivalent series resistance (ESR) and provide the best ripple performance. A good starting value is:

$$C_{OUT1} = \frac{150}{V_{OUT} \bullet f_S}$$

where f_S is in MHz, and C_{OUT} is the recommended output capacitance in µF. Use X5R or X7R types. This choice will provide low output ripple and good transient response.

A good starting value for the low voltage channel output capacitor is:

$$C_{OUT2} = \frac{100}{V_{OUT2} \bullet f_S}$$

In the case where V_{IN2} is connected to the high voltage channel output, the high voltage channel output capacitor can be used as the low voltage channel input capacitor. The required V_{IN2} input capacitor value is usually smaller than the high voltage output capacitor.

Low ESR ceramic capacitors for V_{IN2} input and high voltage channel output could form resonant tank and cause jitter in certain operating area. Avoid V_{IN2} input capacitor if possible.

When choosing a capacitor, look carefully through the data sheet to find out what the actual capacitance is under operating conditions (applied voltage and temperature). A physically larger capacitor or one with a higher voltage rating may be required. High performance tantalum or electrolytic capacitors can be used for the output capacitor. Low ESR is important, so choose one that is intended for use in switching regulators. Table 3 lists several capacitor vendors.

Table 3. Capacitor Vendors

PART SERIES	VENDOR
Ceramic, Polymer, Tantalum	Panasonic/Sanyo www.panasonic.com
Ceramic, Tantalum	Kemet www.kemet.com
Ceramic	Murata www.murata.com
Ceramic, Tantalum	AVX www.avxcorp.com
Ceramic	Taiyo Yuden www.taiyo-yuden.com

Catch Diode

The high voltage channel requires an external catch diode to conduct current during switch off-time. Average forward current in normal operation can be calculated from:

$$I_{D(AVG)} = \frac{I_{OUT}\,(V_{IN} - V_{OUT})}{V_{IN}}$$

where I_{OUT} is the output load current. Use a 1A or 2A rated Schottky diode. Peak reverse voltage is equal to the regulator input voltage. Use a diode with a reverse voltage rating greater than the input voltage. Table 4 lists several Schottky diodes and their manufacturers. Diodes Inc. PDS360 is recommended for high current, H-grade applications. Diodes Inc. DFLS260 can be used for smaller circuit footprint in non-H-grade applications.

APPLICATIONS INFORMATION

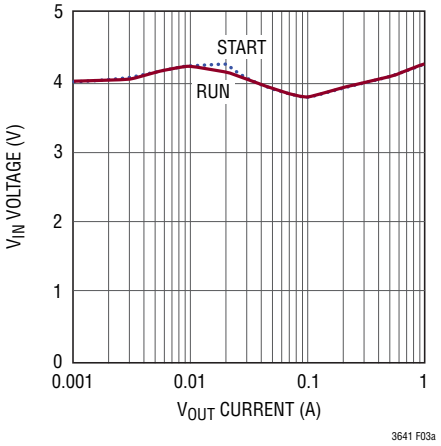
Table 4. Diode Vendors

PART NUMBER	V_R (V)	I_{AVE} (A)	V_F AT 1A (MV)	V_F AT 2A (MV)	V_F AT 3A (MV)
On Semiconductor					
MBRM120E	20	1	530	595	
MBRM140	40	1			
Diodes Inc.					
B120	20	1	500		
B130	30	1	500		
B220	20	2		500	
B230	30	2		500	
DFLS240L	40	2		500	650
DFLS260	60	2		620	
PDS360	60	3			620
PDS3100	100	3			760
International Rectifier					
10BQ030	30	1	420	470	
20BQ030	30	2		470	

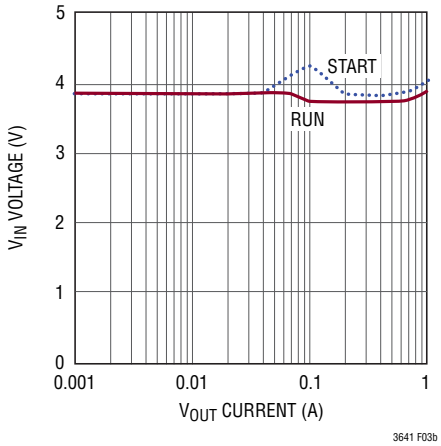
BST and SW Pin Considerations

The high voltage channel requires an external capacitor between the BST and SW pins and an external boost diode from a voltage source to the BST pin. In most cases, a 0.22µF capacitor will work well. Use a Schottky with fast reverse recovery for BST diode. The (BST-SW) voltage cannot exceed 5.5V, and must be more than 2.3V for best efficiency. Connect the boost diode to any voltage between 2.7V and 5.5V. The V_{IN2} pin is the best choice if the low voltage channel is used.

The high voltage channel will not start until the (BST-SW) voltage is 2V or above. When the LT3641 is enabled, an internal ~5mA current source from V_{IN} flows out of the BST pin. The SW pin is disconnected from the SW1 pin, and is pulled down by an internal current source to ground. The external boost capacitor can be charged up regardless of the output. When the (BST-SW) voltage reaches 2V, the SW pin is connected to the SW1 pin, and the high voltage channel starts switching. However, the internal bipolar power switch cannot be fully saturated until the (BST-SW) voltage is further charged to above 2.3V. To start up a traditional nonsynchronous buck regulator with very light load, the input voltage needs to be a couple of volts higher than the minimum running input voltage if the input voltage is ramping up slowly. The LT3641's unique boost capacitor charging scheme solves this start-up issue. Figure 2 shows that the minimum input voltage to start the high voltage channel nonsynchronous buck regulator of the LT3641 is very close to the minimum input voltage to regulate the output voltage for most of the load range.



(2a) F_S = 2MHz



(2b) F_S = 500kHz

Figure 2. High Voltage Channel Minimum Input Voltage for V_{OUT1} = 3.3V

APPLICATIONS INFORMATION

Soft-Start

The LT3641 has a soft-start pin for each channel. The feedback pin voltage is regulated to the lower of the corresponding SS pin and the internal references, which is 1.265V for the high voltage channel, and 600mV for the low voltage channel. A capacitor from the SS pin to ground is charged by an internal 2µA current source resulting in an output ramping linearly from 0V to the regulated voltage. The duration of the ramp is:

$$t_{SS1} = C_{SS1} \bullet \frac{1.265V}{2\mu A}$$

$$t_{SS2} = C_{SS2} \bullet \frac{600mV}{2\mu A}$$

where t_{SS1} is the ramping time for the SS1 pin, t_{SS2} is the ramping time for the SS2 pin, C_{SS1} is the capacitance from the SS1 pin to ground, and C_{SS2} is the capacitance from the SS2 pin to ground.

At power-up, a latch is set to discharge the SS1 pin. After the SS1 pin is discharged to below 100mV, the latch is reset. The internal 2µA current source starts to charge the SS1 pin when the (BST-SW) voltage is charged to above 2V.

In the event of V_{IN} undervoltage lockout, or the EN/UVLO pin being driven below 1.26V, the soft-start latch is set, triggering a start-up sequence.

A latch is set to discharge the SS2 pin at power-up. After EN/UVLO is enabled, the V_{IN2} voltage is above 2.3V, the EN2 pin is enabled, and the SS2 pin is below 100mV, the latch is reset. The internal 2µA current source starts to charge the SS2 pin.

In the event of the V_{IN2} pin falling below 2.2V, or the EN2 pin going below its threshold, the SS2 discharging latch is set, triggering a start-up sequence.

The SS pins can also be pulled up by external current sources or resistors for output tracking. The external pull-up current should not exceed 100µA for either SS pin.

Figure 3 shows the soft-start for a 3.3V and 1.8V application.

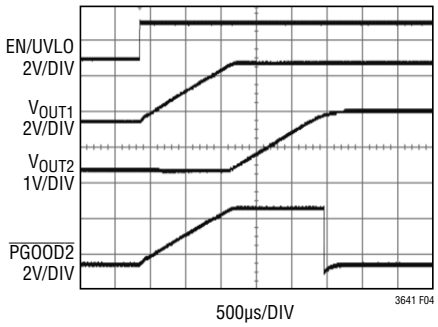


Figure 3. Soft-Start of LT3641

Shorted-Output Protection

If an inductor is chosen that will not saturate excessively, the LT3641 will tolerate a shorted output. For the high voltage channel, the DA current comparator extends the internal oscillator period until the catch diode current is below its limit. Both the top switch and the DA comparator have current foldback to help limit load current when the output is shorted to ground. The DA current limit is 1.7A when the FB1 voltage is above 0.2V, and is 1A when the FB1 voltage is below 0.2V. Figure 4 shows the high voltage channel operation under shorted output.

Because of the low V_{IN2} voltage, the low voltage channel does not have current foldback. The low voltage channel does not extend the internal oscillator in shorted output condition allowing the high voltage channel to operate in constant frequency. If the bottom MOSFET current exceeds the NMOS current limit at the start of a clock cycle, the top MOSFET is kept off until the overcurrent situation clears. The inductor valley current is kept below the NMOS current limit to ensure robustness in shorted output condition (Figure 5).

APPLICATIONS INFORMATION

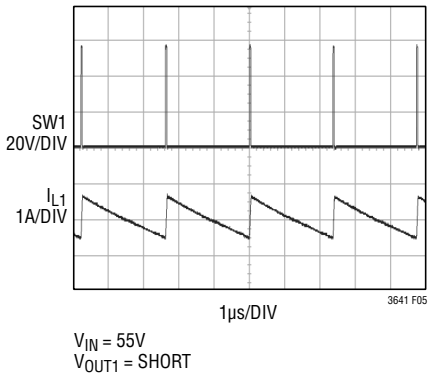


Figure 4. The High Voltage Channel Reduces Frequency to Protect Against Shorted Output with 55V Input

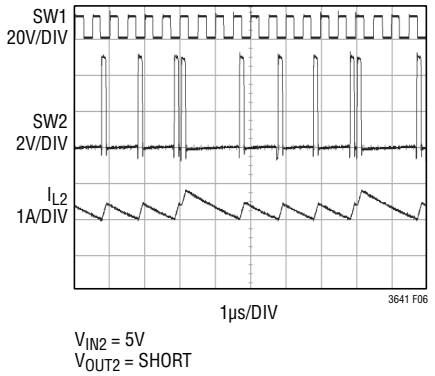


Figure 5. The Low Voltage Channel Operates in Valley Current Limit Mode to Protect Against Shorted Output

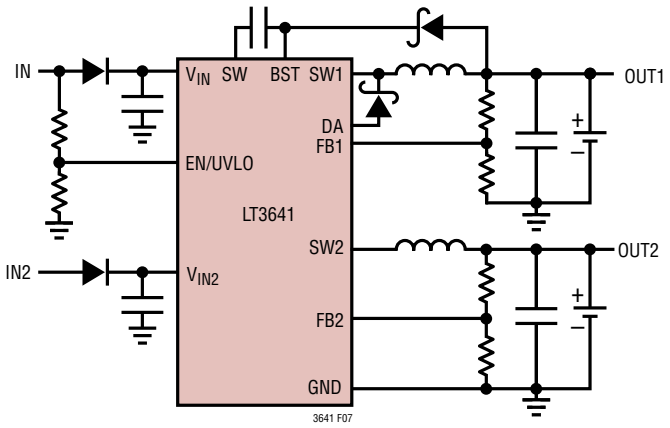


Figure 6. Diodes Prevent Shorted Inputs from Discharging a Battery Tied to the Outputs

Reverse Protection

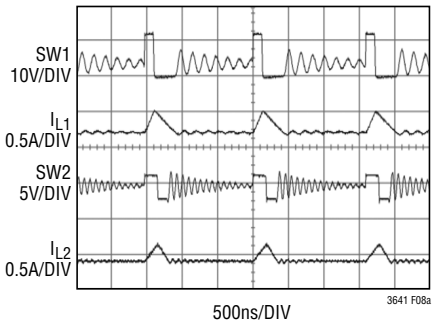
In battery charging applications or in battery back-up systems, the output will be held high when the input to the LT3641 is absent. If the V_{IN} pin is floated and the LT3641 is enabled, the LT3641's internal circuitry will pull its quiescent current through the SW1 pin or the SW2 pin. This is fine if the system can tolerate a few mA in this state. If the LT3641 is disabled, the SW1 pin and the SW2 pin current will drop to essentially zero. However, if the V_{IN} pin is grounded while the high voltage channel output is held high, an external diode is required at the V_{IN} pin to prevent current being pulled out of the V_{IN} pin. If the V_{IN2} pin is grounded while the low voltage channel output is held high, an external diode is required at the V_{IN2} pin to prevent current being pulled out of the V_{IN2} pin (Figure 6).

PFM Operation

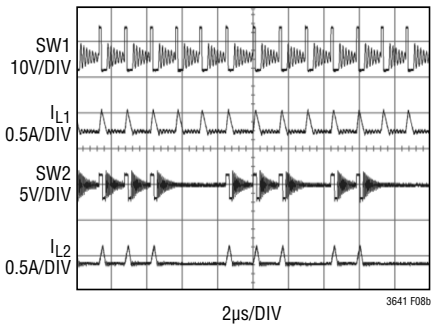
To improve efficiency at light loads, the LT3641 automatically switches to pulse frequency modulation (PFM) operation which minimizes the switching loss and keeps the output voltage ripples small.

Because the two channels of the LT3641 may have different loads, the two channels can have different switching frequency (Figure 7).

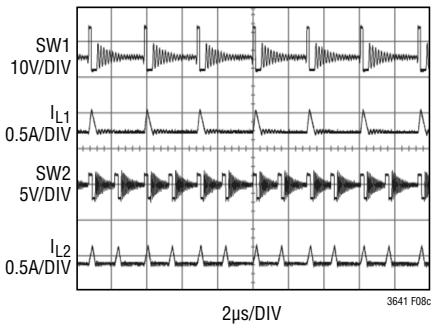
APPLICATIONS INFORMATION



(7a)



(7b)



(7c)

Figure 7. PFM Operation

Power-On Reset Timer

Each channel of the LT3641 has a power-on comparator. Both comparators are enabled when the LT3641 is powered up and starts monitoring their corresponding feedback voltages. The threshold of power-on comparator is 1.15V for the high voltage channel, and 550mV for the low voltage channel.

Both $\overline{RST1}$ and $\overline{RST2}$ are open-drain outputs with weak internal pull-ups (100k to ~2V). The DC characteristics of the $\overline{RST1}$ and $\overline{RST2}$ pull-down strength are shown in the Typical Performance Characteristics section. The weak pull-ups eliminate the need for external pull-ups when the rise time of these pins is not critical. The open-drain configuration allows wired-OR connections.

The two power-on reset timers share one oscillator. The power-on reset timeout period, t_{RST} (64 cycles on the CPOR pin), which is the same for the two channels, can be programmed by connecting a capacitor, C_{POR}, between the CPOR pin and ground:

$$t_{RST} = C_{POR} \bullet 37 \bullet 10^6 \left(\frac{s}{F}\right)$$

For example, using a capacitor value of 8.2nF gives a 303ms reset timeout period. The accuracy of t_{RST} will be limited by the accuracy and temperature coefficient of the capacitor CPOR. Extra parasitic capacitance on the CPOR pin, such as probe capacitance, can affect t_{RST}.

Watchdog

The $\overline{WDE}$ pin is the enable pin for the watchdog. As soon as $\overline{RST2}$ is released, the watchdog starts a delay period, t_{DLY}, during which the input signal at the WDI pin is ignored for higher reliability. After the delay period, the watchdog starts detecting falling edges on the WDI pin. If the time between any two WDI falling edges is shorter than the watchdog lower boundary, t_{WDL}, or longer than the watchdog upper boundary, t_{WDU}, the $\overline{WDO}$ pin is pulled down for a period of t_{RST}, which is the same as the power-on reset timeout period. When the $\overline{WDO}$ pin is released, the watchdog again starts the delay period.

APPLICATIONS INFORMATION

The $\overline{WDO}$ is open-drain output with weak internal pull-up, similar to the $\overline{RST}$ pins.

The delay period corresponding to 33 cycles on CWDT, the watchdog lower boundary (4 cycles on CWDT), and the watchdog upper boundary (64 cycles on CWDT) are all related and set by a capacitor, C_{WDT}, between the CWDT pin and ground:

$$t_{DLY} = t_{WDU} \bullet \left(\frac{33}{64}\right)$$

$$t_{WDL} = \frac{t_{WDU}}{16}$$

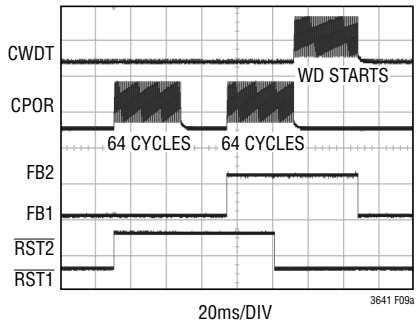
$$t_{WDU} = C_{WDT} \bullet 37 \bullet 10^6 \left(\frac{s}{F}\right)$$

The accuracy of the watchdog timer will be limited by the accuracy and temperature coefficient of the capacitor C_{WDT}. Extra parasitic capacitance on the CWDT pin, such as probe capacitance, can affect the watchdog timer.

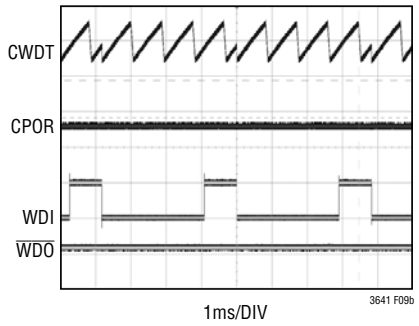
Figure 8a shows the power-on reset timing. Having FB1 or FB2 high starts the CPOR oscillator. After t_{RST}, the corresponding $\overline{RST}$ is released. When both $\overline{RST1}$ and $\overline{RST2}$ are released, the CWDT oscillator starts. Figure 8b shows the watchdog waveform with the WDI period between t_{WDL} and t_{WDU}. The WDI falling edge resets the CWDT oscillator. The CPOR oscillator is disabled and $\overline{WDO}$ remains high. Figure 8c shows the watchdog waveform with the WDI period longer than t_{WDU}. $\overline{WDO}$ is asserted for a period of t_{RST} when the watchdog upper boundary, t_{WDU}, expires.

The watchdog function can be disabled by tying $\overline{WDE}$ above its threshold. In this case, the CWDT pin can be left floating. If neither the watchdog function nor the power-on reset function is used, both the CWDT and CPOR pin can be left floating.

The accuracy of the CPOR and CWDT capacitors determine the accuracy of the power-on reset timer and watchdog timer. The COG or NPO type of ceramic capacitors have zero temperature coefficient and good aging characteristics. Use COG or NPO type of capacitors with flat DC bias characteristic up to 1.5V on the CPOR and CWDT pins.



(8a)



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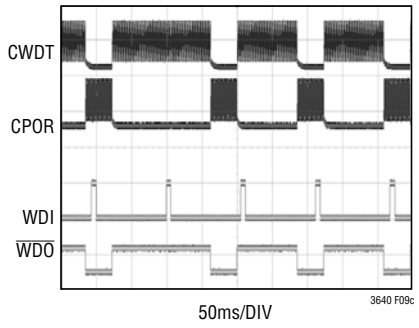


(8c)

Figure 8. Power-On Reset and Watchdog Timing

APPLICATIONS INFORMATION

PCB Layout

For proper operation and minimum EMI, care must be taken during the printed circuit board (PCB) layout. Figure 9 shows the recommended component placement with trace, ground plane and via locations. The input loop of the high voltage channel, which is formed by the V_{IN} and SW1 pins, the external catch diode (D1), the input capacitor (C_{IN}) and the ground, should be as small as possible. These external components should be placed on the same side of the circuit board as the LT3641, and their connections should be made on that layer. Place a local, unbroken ground plane below these components. The BST and SW nodes should be as small as possible. The boost capacitor (C_{BST}) should be as close to the BST and SW pins as possible.

The input loop of the low voltage channel is formed by the V_{IN2} pin, the input capacitor (C_{IN2}) and the ground. Place C_{IN2} close to the V_{IN2} and the GND pin to minimize this loop. Place a local, unbroken ground plane below this input loop.

Keep the FB1 and FB2 nodes small so that the ground traces will shield them from the switching nodes. The Exposed Pad on the bottom of the package must be soldered to the ground so that the pad acts as a heat sink. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the LT3641 to additional ground planes within the circuit board and on the bottom side.

Sequencing Options

In most LT3641 applications, the low voltage regulator generating OUT2 will operate from the output of the high voltage regulator generating OUT1. In this cascade circuit, channel 1 must start before channel 2. However, the LT3641 provides additional flexibility in programming the sequencing of the outputs. Figure 10 shows several possibilities.

Figure 10a shows the easiest option. With EN2 tied to FB1, channel 2 will start when OUT1 is within 10% of its regulation point.

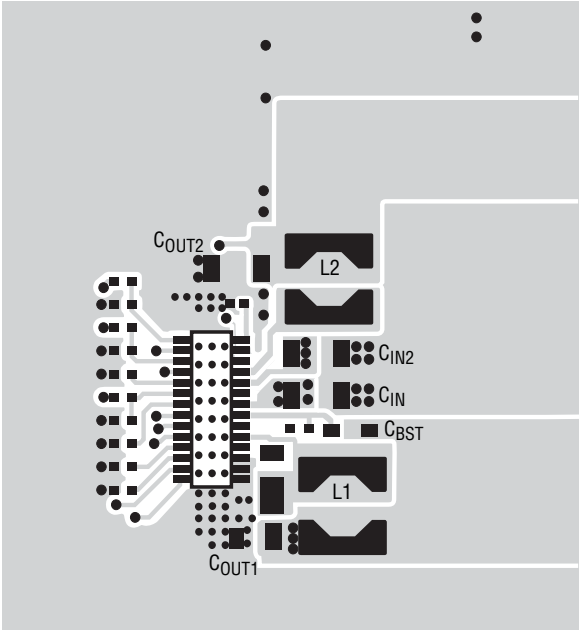


Figure 9. Recommended PCB Layout, FE28 Package

Figure 10b shows a simple alternative. By tying EN2 to V_{IN2}, channel 2 starts as soon as its input reaches its minimum operating voltage of 2.3V.

Figure 10c shows a circuit that handles two other common requirements. If the system requires the low voltage output to be in regulation before the higher voltage output (for example core voltage must appear before the I/O supply), then add a PMOS switch and drive its gate with the $\overline{PGOOD2}$ pin, which will go low when both channels are in regulation. This provides a third output OUT3, which is present only when both OUT1 and OUT2 are in regulation.

Figure 10c also takes care of a potential problem in cascaded power supply circuits. Because channel 2 is a switching regulator, it appears as negative impedance load to channel 1; as OUT1 decreases, the load required to supply the input of channel 2 increases. Since the channel 1 is current limited, you must be certain that it can supply both its own load and the power required by channel 2. The EN2 has an accurate threshold of 1.165V, and is used to program an undervoltage lockout for channel 2, allowing channel 1 to supply adequate power.

APPLICATIONS INFORMATION

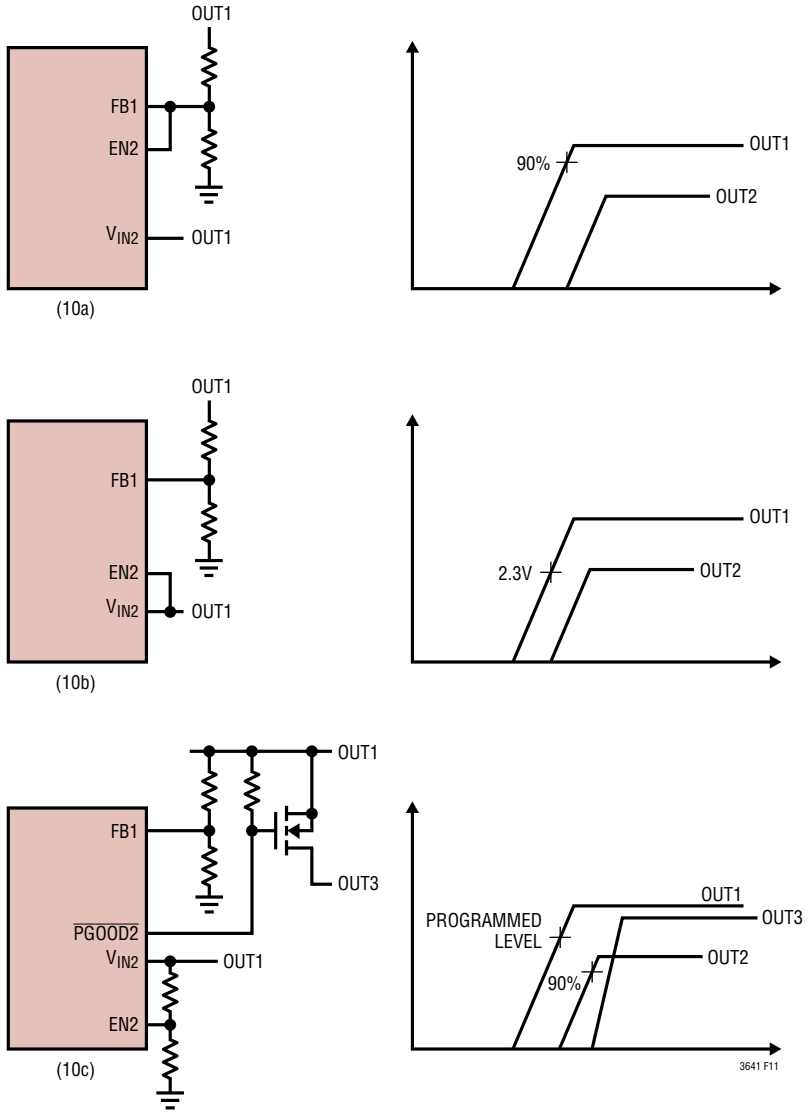
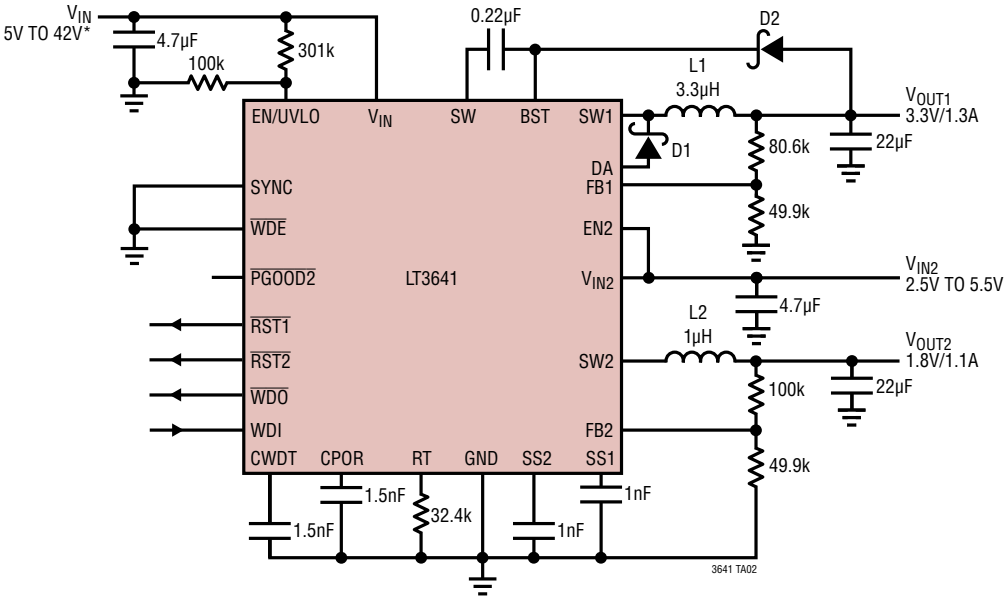


Figure 10. The EN2 and $\overline{\text{PGOOD2}}$ Pins Allow Serial Sequencing Options

TYPICAL APPLICATIONS

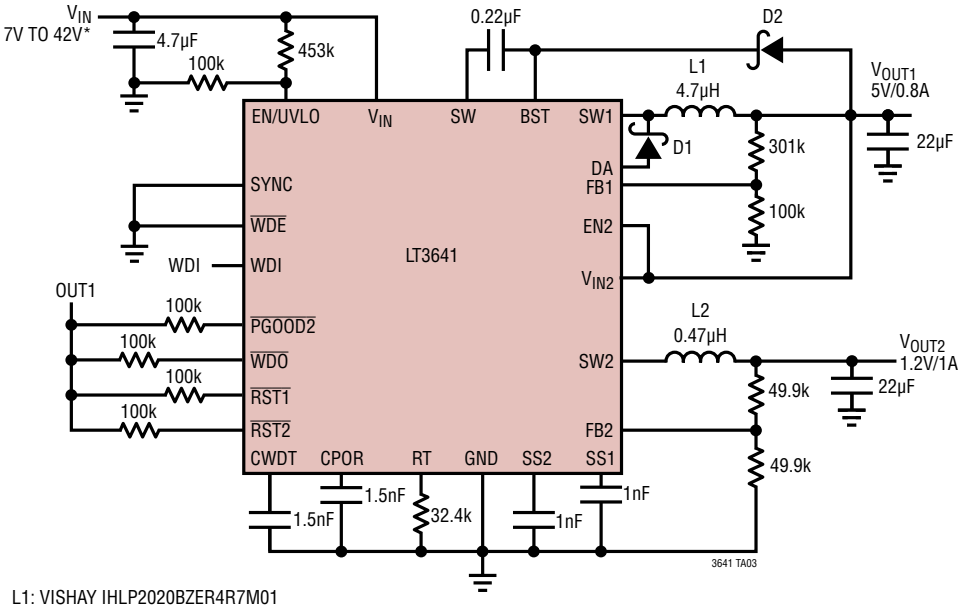
2MHz 3.3V/1.3A and 1.8V/1A Buck Regulators



L1: VISHAY IHLP2020BZER3R3M01
L2: VISHAY IHLP1616ABER1R0M01
D1: DIODES PDS360
D2: CENTRAL SEMI CMDSH-4E

* RESTRICTIONS APPLY FOR INPUT VOLTAGES ABOVE 42V

2MHz 5V/0.8A and 1.2V/1A Buck Regulators

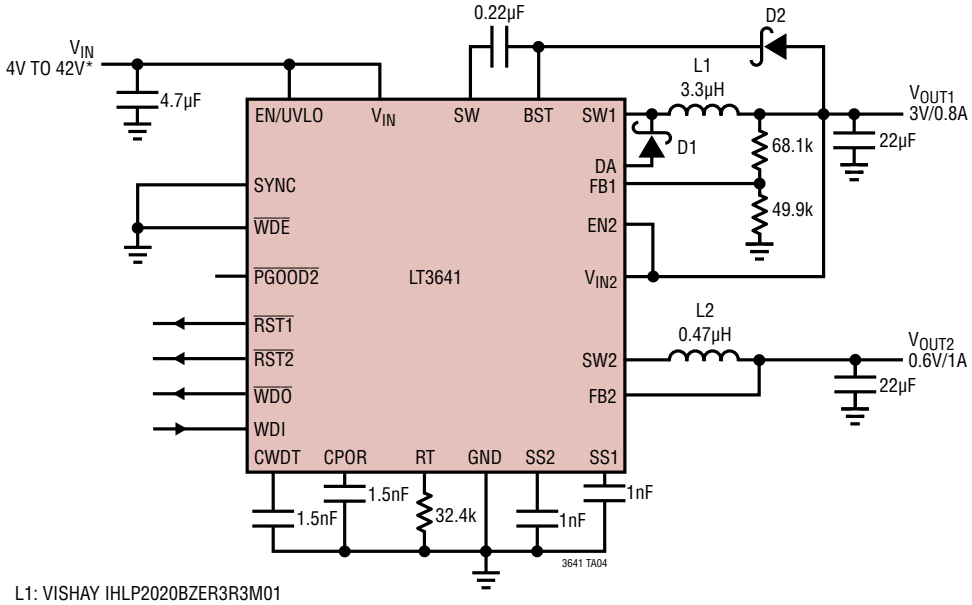


L1: VISHAY IHLP2020BZER4R7M01
L2: VISHAY IHLP1616ABERR47M01
D1: DIODES DFLS260
D2: CENTRAL SEMI CMDD6263

* RESTRICTIONS APPLY FOR INPUT VOLTAGES ABOVE 42V

TYPICAL APPLICATIONS

2MHz 3V/0.8A and 0.6V/1A Buck Regulators



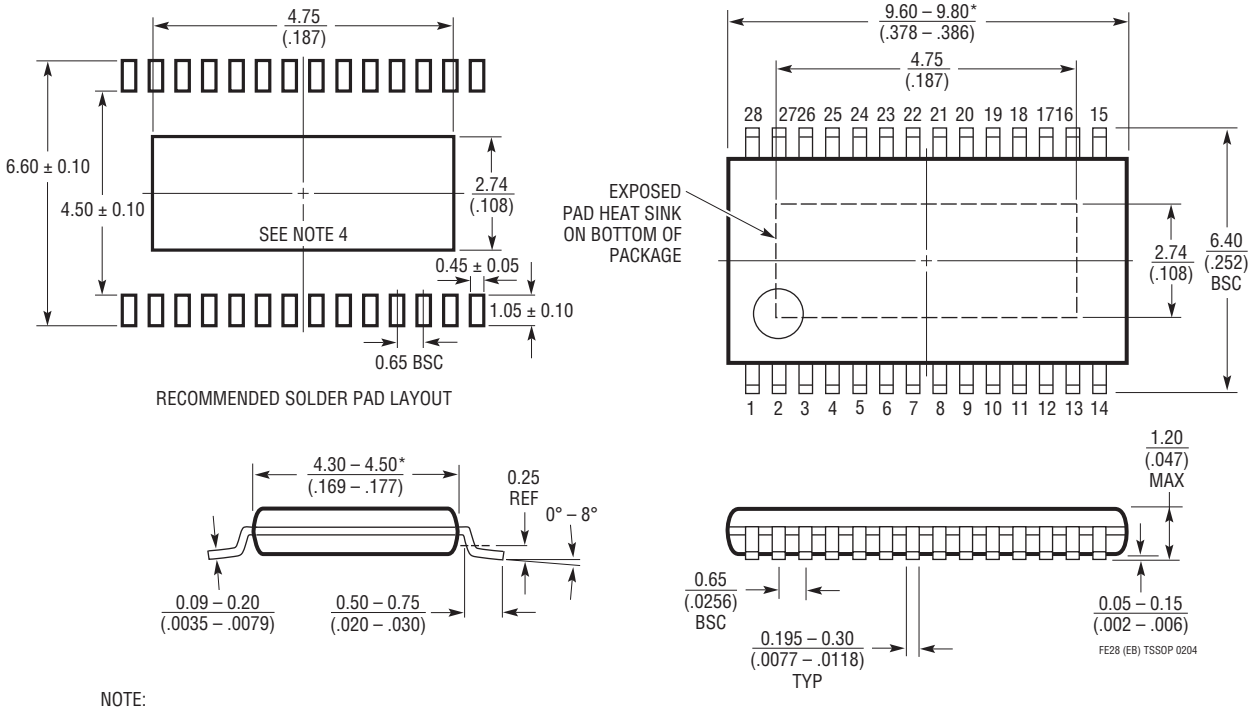
L1: VISHAY IHLP2020BZER3R3M01
L2: VISHAY IHLP1616ABERR47M01
D1: DIODES PDS360
D2: CENTRAL SEMI CMDSH2-3

* RESTRICTIONS APPLY FOR INPUT VOLTAGES ABOVE 42V

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

FE Package
28-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663)
Exposed Pad Variation EB

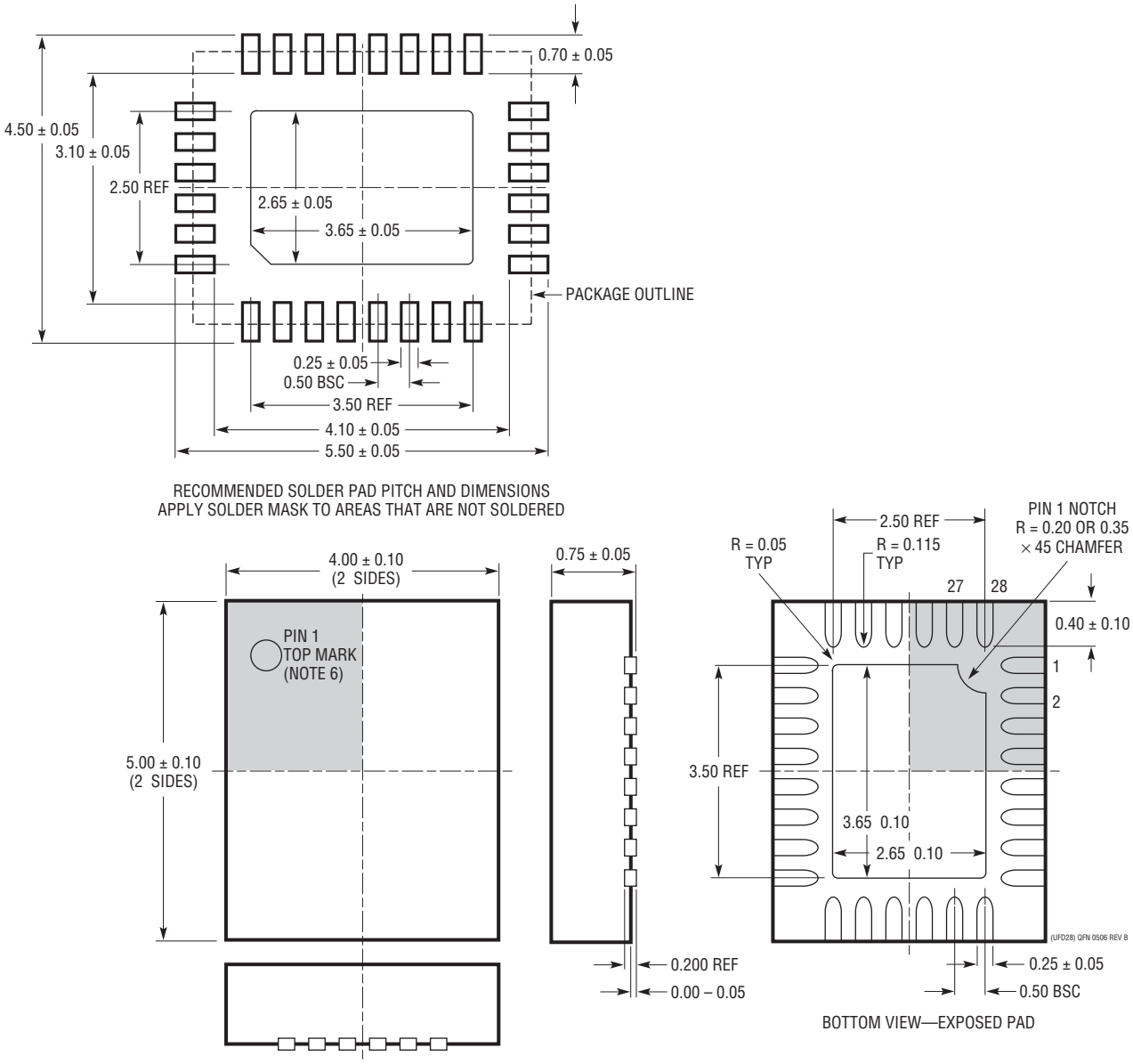


NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev B)



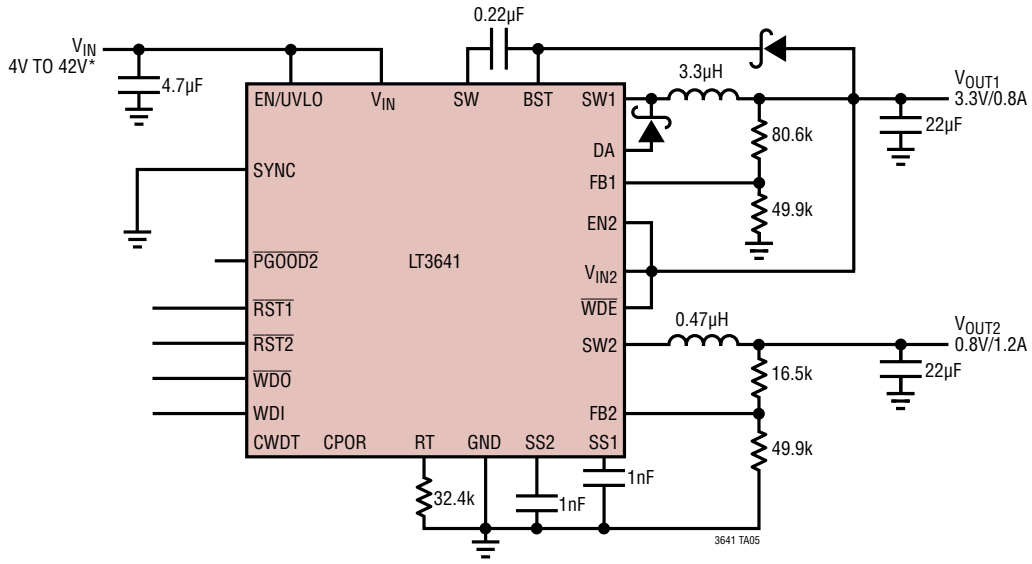
NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	11/11	Added H-grade to Absolute Maximum Ratings, Order Information, and Note 2	2, 4

TYPICAL APPLICATION

2MHz 3.3V/0.8A and 0.8V/1.2A Buck Regulators



* RESTRICTIONS APPLY FOR INPUT VOLTAGES ABOVE 42V

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3640	35V, 55V Transient Protection, 1.3A High Voltage Channel and 1.1A Low Volume Channel	V_{IN}: 4V to 35V, Transient to 55V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 290mA, 1µA, 4mm × 5mm QFN-28, TSSOP-28E Packages
LT3689	36V, 60V Transient Protection, 800mA, 2.2MHz High Efficiency MicroPower Step-Down DC/DC Converter with POR Reset and Watchdog Timer	V_{IN}: 3.6V to 36V, Transient to 60V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 75µA, I_{SD} < 1µA, 3mm × 3mm QFN-16 Package
LT3686/LT3686A	37V, 55V_{MAX}, 1.2A, 2.5MHz High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.6V to 37V, Transient to 55V, $V_{OUT(MIN)}$ = 1.21V, I_Q = 1.1mA, I_{SD} < 1µA, 3mm × 3mm DFN-10 Package
LT3682	36V, 60V_{MAX}, 1A, 2.2MHz High Efficiency Micropower Step-Down DC/DC Converter	V_{IN}: 3.6V to 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 75µA, I_{SD} < 1µA, 3mm × 3mm DFN-12 Package
LT3971	38V, 1.2A (I_{OUT}), 2MHz, High Efficiency Step-Down DC/DC Converter with Only 2.8µA of Quiescent Current	V_{IN}: 4.2V to 38V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 2.8µA, I_{SD} < 1µA, 3mm × 3mm DFN-10, MSOP-10E Packages
LT3991	55V, 1.2A (I_{OUT}), 2MHz, High Efficiency Step-Down DC/DC Converter with Only 2.8µA of Quiescent Current	V_{IN}: 4.2V to 55V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 2.8µA, I_{SD} < 1µA, 3mm × 3mm DFN-10, MSOP-10E Packages

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