THE DATASHEET OF

LTC2412CGN#TRPBF

2-Channel Differential Input 24-Bit No Latency ΔΣ ADC

FEATURES

- **2-Channel Differential Input with Automatic Channel Selection (Ping-Pong)**
- **Low Supply Current: 200µA, 4µA in Autosleep**
- **Differential Input and Differential Reference with GND to V_{CC} Common Mode Range**
- **2ppm INL, No Missing Codes**
- **2.5ppm Full-Scale Error and 0.1ppm Offset**
- **0.16ppm Noise, 22.5 Effective Number of Bits**
- No Latency: Digital Filter Settles in a Single Cycle and Each Channel Conversion is Accurate
- Internal Oscillator—No External Components Required
- 110dB Min, 50Hz or 60Hz Notch Filter
- Narrow SSOP-16 Package
- Single Supply 2.7V to 5.5V Operation

APPLICATIONS

- Direct Sensor Digitizer
- Weight Scales
- Direct Temperature Measurement
- Gas Analyzers
- Strain-Gage Transducers
- Instrumentation
- Data Acquisition
- Industrial Process Control
- 6-Digit DVMs

DESCRIPTION

The LTC®2412 is a 2-channel differential input micropower 24-bit No Latency ΔΣ™ analog-to-digital converter with an integrated oscillator. It provides 2ppm INL and 0.16ppm RMS noise over the entire supply range. The two differential channels are converted alternately with channel ID included in the conversion results. It uses delta-sigma technology and provides single conversion settling of the digital filter. Through a single pin, the LTC2412 can be configured for better than 110dB input differential mode rejection at 50Hz or 60Hz ±2%, or it can be driven by an external oscillator for a user defined rejection frequency. The internal oscillator requires no external frequency setting components.

The converter accepts any external differential reference voltage from 0.1V to V_{CC} for flexible ratiometric and remote sensing measurement configurations. The full-scale differential input range is from $–0.5V_{REF}$ to $0.5V_{REF}$. The reference common mode voltage, V_{REFCM}, and the input common mode voltage, V_{INCM}, may be independently set anywhere within the GND to V_{CC}. The DC common mode input rejection is better than 140dB.

The LTC2412 communicates through a flexible 3-wire digital interface which is compatible with SPI and MICROWIRE protocols.

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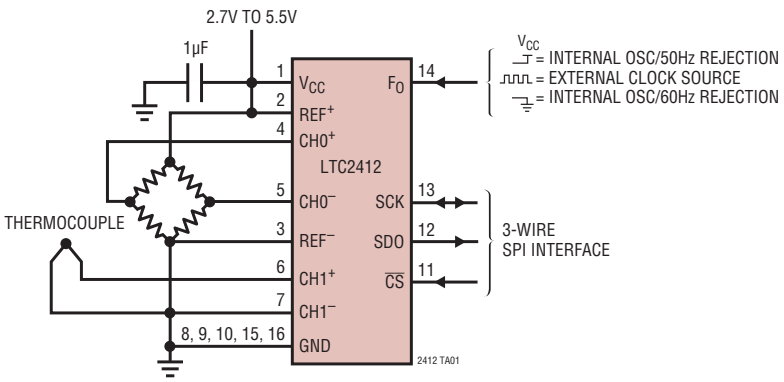
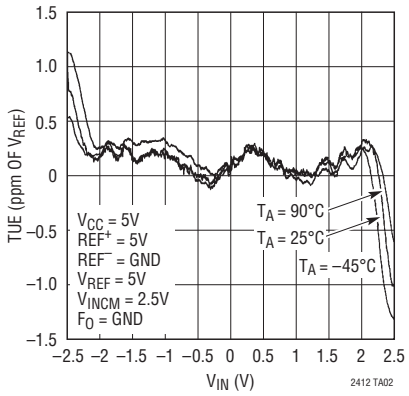
TYPICAL APPLICATION



Total Unadjusted Error vs Input

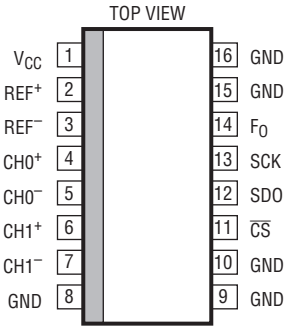


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) to GND ..... –0.3V to 7V
Analog Input Voltage
to GND ..... –0.3V to (V_{CC} + 0.3V)
Reference Input Voltage
to GND ..... –0.3V to (V_{CC} + 0.3V)
Digital Input Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Digital Output Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Operating Temperature Range
LTC2412C ..... 0°C to 70°C
LTC2412I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



GN PACKAGE
16-LEAD PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2412CGN#PBF	LTC2412CGN#TRPBF	2412	16-Lead Plastic SSOP	0°C to 70°C
LTC2412IGN#PBF	LTC2412IGN#TRPBF	2412I	16-Lead Plastic SSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)	0.1V ≤ V_{REF} ≤ V_{CC}, –0.5 • V_{REF} ≤ V_{IN} ≤ 0.5 • V_{REF}, (Note 5)	●	24			Bits
Integral Nonlinearity	5V ≤ V_{CC} ≤ 5.5V, REF^+ = 2.5V, $REF^–$ = GND, V_{INCM} = 1.25V, (Note 6) 5V ≤ V_{CC} ≤ 5.5V, REF^+ = 5V, $REF^–$ = GND, V_{INCM} = 2.5V, (Note 6) REF^+ = 2.5V, $REF^–$ = GND, V_{INCM} = 1.25V, (Note 6)	 ● 		1 2 5	 14 	ppm of V_{REF} ppm of V_{REF} ppm of V_{REF}
Offset Error	2.5V ≤ REF^+ ≤ V_{CC}, $REF^–$ = GND, GND ≤ IN^+ = $IN^–$ ≤ V_{CC}, (Note 14)	●		0.5	2.5	µV
Offset Error Drift	2.5V ≤ REF^+ ≤ V_{CC}, $REF^–$ = GND, GND ≤ IN^+ = $IN^–$ ≤ V_{CC}			10		nV/°C
Positive Full-Scale Error	2.5V ≤ REF^+ ≤ V_{CC}, $REF^–$ = GND, IN^+ = 0.75REF^+, $IN^–$ = 0.25 • REF^+	●		2.5	12	ppm of V_{REF}
Positive Full-Scale Error Drift	2.5V ≤ REF^+ ≤ V_{CC}, $REF^–$ = GND, IN^+ = 0.75REF^+, $IN^–$ = 0.25 • REF^+			0.03		ppm of V_{REF}/°C
Negative Full-Scale Error	2.5V ≤ REF^+ ≤ V_{CC}, $REF^–$ = GND, IN^+ = 0.25 • REF^+, $IN^–$ = 0.75 • REF^+	●		2.5	12	ppm of V_{REF}
Negative Full-Scale Error Drift	2.5V ≤ REF^+ ≤ V_{CC}, $REF^–$ = GND, IN^+ = 0.25 • REF^+, $IN^–$ = 0.75 • REF^+			0.03		ppm of V_{REF}/°C
Total Unadjusted Error	5V ≤ V_{CC} ≤ 5.5V, REF^+ = 2.5V, $REF^–$ = GND, V_{INCM} = 1.25V 5V ≤ V_{CC} ≤ 5.5V, REF^+ = 5V, $REF^–$ = GND, V_{INCM} = 2.5V REF^+ = 2.5V, $REF^–$ = GND, V_{INCM} = 1.25V, (Note 6)			3 3 4		ppm of V_{REF} ppm of V_{REF} ppm of V_{REF}
Output Noise	5V ≤ V_{CC} ≤ 5.5V, REF^+ = 5V, $REF^–$ = GND, GND ≤ $IN^–$ = IN^+ ≤ V_{CC}, (Note 13)			0.8		μV_{RMS}

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Common Mode Rejection DC	2.5V ≤ REF^+ ≤ V_{CC}, REF^- = GND, GND ≤ IN^- = IN^+ ≤ V_{CC} (Note 5)	●	130	140		dB
Input Common Mode Rejection 60Hz ±2%	2.5V ≤ REF^+ ≤ V_{CC}, REF^- = GND, GND ≤ IN^- = IN^+ ≤ V_{CC}, (Notes 5, 7)	●	140			dB
Input Common Mode Rejection 50Hz ±2%	2.5V ≤ REF^+ ≤ V_{CC}, REF^- = GND, GND ≤ IN^- = IN^+ ≤ V_{CC}, (Notes 5, 8)	●	140			dB
Input Normal Mode Rejection 60Hz ±2%	(Notes 5, 7)	●	110	140		dB
Input Normal Mode Rejection 50Hz ±2%	(Note 5, 8)	●	110	140		dB
Reference Common Mode Rejection DC	2.5V ≤ REF^+ ≤ V_{CC}, GND ≤ REF^- ≤ 2.5V, V_{REF} = 2.5V, IN^- = IN^+ = GND (Note 5)	●	130	140		dB
Power Supply Rejection, DC	REF^+ = 2.5V, REF^- = GND, IN^- = IN^+ = GND			120		dB
Power Supply Rejection, 60Hz ±2%	REF^+ = 2.5V, REF^- = GND, IN^- = IN^+ = GND, (Note 7)			120		dB
Power Supply Rejection, 50Hz ±2%	REF^+ = 2.5V, REF^- = GND, IN^- = IN^+ = GND, (Note 8)			120		dB

ANALOG INPUT AND REFERENCE

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN^+	Absolute/Common Mode IN^+ Voltage		●	GND – 0.3		V_{CC} + 0.3	V
IN^-	Absolute/Common Mode IN^- Voltage		●	GND – 0.3		V_{CC} + 0.3	V
V_{IN}	Input Differential Voltage Range (IN^+ – IN^-)		●	$-V_{REF}/2$		$V_{REF}/2$	V
REF^+	Absolute/Common Mode REF^+ Voltage		●	0.1		V_{CC}	V
REF^-	Absolute/Common Mode REF^- Voltage		●	GND		V_{CC} – 0.1	V
V_{REF}	Reference Differential Voltage Range (REF^+ – REF^-)		●	0.1		V_{CC}	V
C_S (IN^+)	IN^+ Sampling Capacitance				18		pF
C_S (IN^-)	IN^- Sampling Capacitance				18		pF
C_S (REF^+)	REF^+ Sampling Capacitance				18		pF
C_S (REF^-)	REF^- Sampling Capacitance				18		pF
I_{DC_LEAK} (IN^+)	IN^+ DC Leakage Current	$\overline{CS}$ = V_{CC} = 5.5V, IN^+ = GND	●	–10	1	10	nA
I_{DC_LEAK} (IN^-)	IN^- DC Leakage Current	$\overline{CS}$ = V_{CC} = 5.5V, IN^- = 5.5V	●	–10	1	10	nA
I_{DC_LEAK} (REF^+)	REF^+ DC Leakage Current	$\overline{CS}$ = V_{CC} = 5.5V, REF^+ = 5.5V	●	–10	1	10	nA
I_{DC_LEAK} (REF^-)	REF^- DC Leakage Current	$\overline{CS}$ = V_{CC} = 5.5V, REF^- = GND	●	–10	1	10	nA

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage $\overline{CS}$, F_O	2.7V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 3.3V	● ●	2.5 2.0			V V
V_{IL}	Low Level Input Voltage $\overline{CS}$, F_O	4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V	● ●			0.8 0.6	V V
V_{IH}	High Level Input Voltage SCK	2.7V ≤ V_{CC} ≤ 5.5V (Note 9) 2.7V ≤ V_{CC} ≤ 3.3V (Note 9)	● ●	2.5 2.0			V V
V_{IL}	Low Level Input Voltage SCK	4.5V ≤ V_{CC} ≤ 5.5V (Note 9) 2.7V ≤ V_{CC} ≤ 5.5V (Note 9)	● ●			0.8 0.6	V V
I_{IN}	Digital Input Current $\overline{CS}$, F_O	0V ≤ V_{IN} ≤ V_{CC}	●	–10		10	µA
I_{IN}	Digital Input Current SCK	0V ≤ V_{IN} ≤ V_{CC} (Note 9)	●	–10		10	µA
C_{IN}	Digital Input Capacitance $\overline{CS}$, F_O				10		pF
C_{IN}	Digital Input Capacitance SCK	(Note 9)			10		pF
V_{OH}	High Level Output Voltage SDO	I_O = –800µA	●	V_{CC} – 0.5			V
V_{OL}	Low Level Output Voltage SDO	I_O = 1.6mA	●			0.4	V
V_{OH}	High Level Output Voltage SCK	I_O = –800µA (Note 10)	●	V_{CC} – 0.5			V
V_{OL}	Low Level Output Voltage SCK	I_O = 1.6mA (Note 10)	●			0.4	V
I_{OZ}	Hi-Z Output Leakage SDO		●	–10		10	µA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	2.7		5.5	V
I_{CC}	Supply Current Conversion Mode Sleep Mode Sleep Mode	 $\overline{CS}$ = 0V $\overline{CS}$ = V_{CC} (Note 12) $\overline{CS}$ = V_{CC}, 2.7V ≤ V_{CC} ≤ 3.3V (Note 12)	 ● ● 		 200 4 2	 300 13 	 µA µA µA

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range		●	2.56		500	kHz
t_{HEO}	External Oscillator High Period		●	0.25		390	µs
t_{LEO}	External Oscillator Low Period		●	0.25		390	µs
t_{CONV}	Conversion Time	F_O = 0V F_O = V_{CC} External Oscillator (Note 11)	● ● ●	130.86 157.03 20510/f_{EOSC} (in kHz)	133.53 160.23	136.20 163.44	ms ms ms
f_{ISCK}	Internal SCK Frequency	Internal Oscillator (Note 10) External Oscillator (Notes 10, 11)		19.2 f_{EOSC}/8			kHz kHz
D_{ISCK}	Internal SCK Duty Cycle	(Note 10)	●	45		55	%
f_{ESCK}	External SCK Frequency Range	(Note 9)	●			2000	kHz
t_{LESCK}	External SCK Low Period	(Note 9)	●	250			ns
t_{HESCK}	External SCK High Period	(Note 9)	●	250			ns
t_{DOUT_ISCK}	Internal SCK 32-Bit Data Output Time	Internal Oscillator (Notes 10, 12) External Oscillator (Notes 10, 11)	● ●	1.64 256/f_{EOSC} (in kHz)	1.67	1.70	ms ms
t_{DOUT_ESCK}	External SCK 32-Bit Data Output Time	(Note 9)	●	32/f_{ESCK} (in kHz)			ms
t_1	$\overline{CS}$ ↓ to SDO Low Z		●	0		200	ns
t_2	$\overline{CS}$ ↑ to SDO High Z		●	0		200	ns
t_3	$\overline{CS}$ ↓ to SCK ↓	(Note 10)	●	0		200	ns
t_4	$\overline{CS}$ ↓ to SCK ↑	(Note 9)	●	50			ns
t_{KQMAX}	SCK ↓ to SDO Valid		●			220	ns
t_{KQMIN}	SDO Hold After SCK ↓	(Note 5)	●	15			ns
t_5	SCK Set-Up Before $\overline{CS}$ ↓		●	50			ns
t_6	SCK Hold After $\overline{CS}$ ↓		●			50	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

Note 3: V_{CC} = 2.7V to 5.5V unless otherwise specified.
V_{REF} = $REF^+ – REF^–$, V_{REFCM} = $(REF^+ + REF^–)/2$; V_{IN} = $IN^+ – IN^–$, V_{INCM} = $(IN^+ + IN^–)/2$, IN^+ and $IN^–$ are defined as the selected positive ($CH0^+$ or $CH1^+$) and negative ($CH0^–$ or $CH1^–$) input respectively.

Note 4: F_O pin tied to GND or to V_{CC} or to external conversion clock source with f_{EOSC} = 153600Hz unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: F_O = 0V (internal oscillator) or f_{EOSC} = 153600Hz ±2% (external oscillator).

Note 8: F_O = V_{CC} (internal oscillator) or f_{EOSC} = 128000Hz ±2% (external oscillator).

Note 9: The converter is in external SCK mode of operation such that the SCK pin is used as digital input. The frequency of the clock signal driving SCK during the data output is f_{ESCK} and is expressed in kHz.

Note 10: The converter is in internal SCK mode of operation such that the SCK pin is used as digital output. In this mode of operation the SCK pin has a total equivalent load capacitance C_{LOAD} = 20pF.

Note 11: The external oscillator is connected to the F_O pin. The external oscillator frequency, f_{EOSC}, is expressed in kHz.

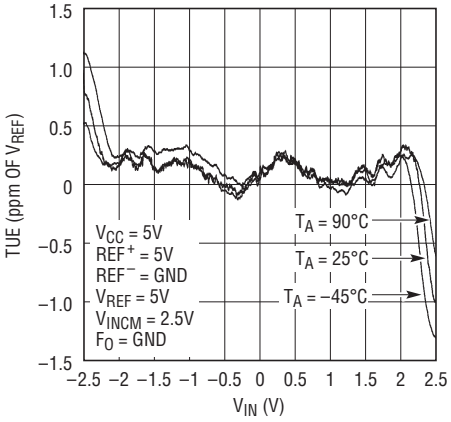
Note 12: The converter uses the internal oscillator.
F_O = 0V or F_O = V_{CC}.

Note 13: The output noise includes the contribution of the internal calibration operations.

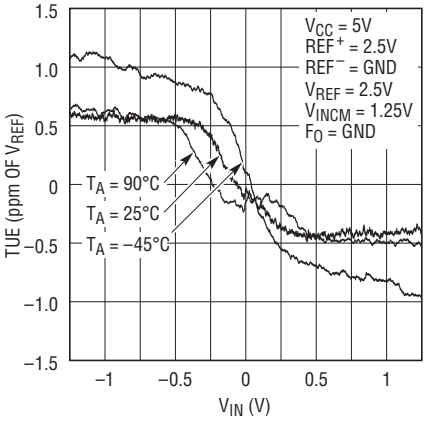
Note 14: Guaranteed by design and test correlation.

TYPICAL PERFORMANCE CHARACTERISTICS

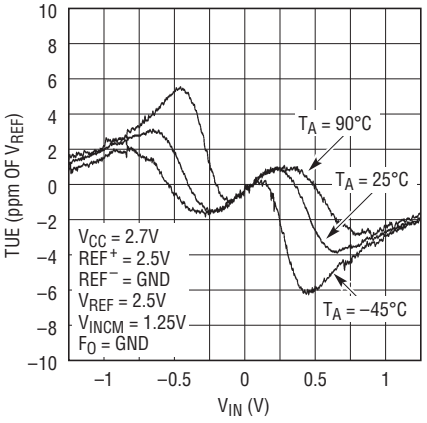
Total Unadjusted Error vs Temperature (V_{CC} = 5V, V_{REF} = 5V)



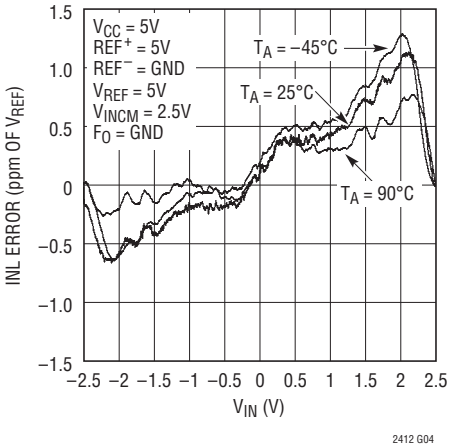
Total Unadjusted Error vs Temperature (V_{CC} = 5V, V_{REF} = 2.5V)



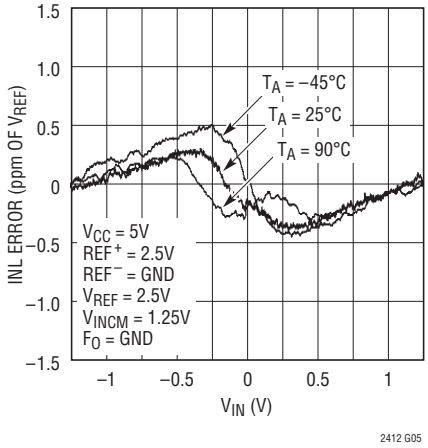
Total Unadjusted Error vs Temperature (V_{CC} = 2.7V, V_{REF} = 2.5V)



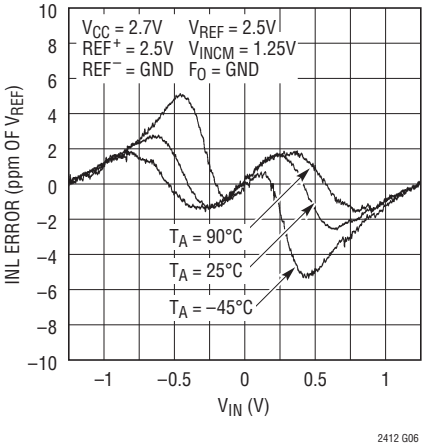
Integral Nonlinearity vs Temperature (V_{CC} = 5V, V_{REF} = 5V)



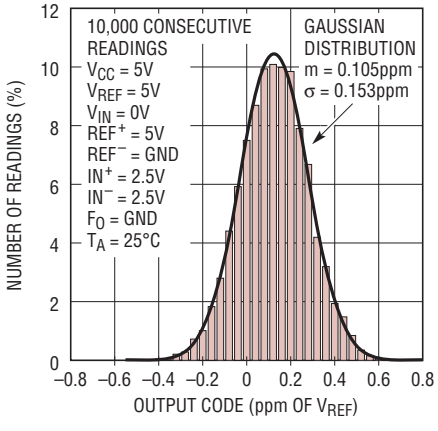
Integral Nonlinearity vs Temperature (V_{CC} = 5V, V_{REF} = 2.5V)



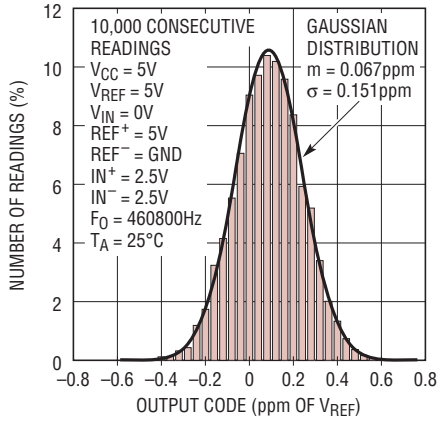
Integral Nonlinearity vs Temperature (V_{CC} = 2.7V, V_{REF} = 2.5V)



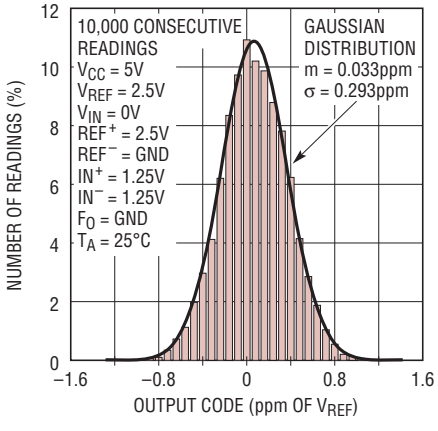
Noise Histogram (Output Rate = 7.5Hz, V_{CC} = 5V, V_{REF} = 5V)



Noise Histogram (Output Rate = 22.5Hz, V_{CC} = 5V, V_{REF} = 5V)

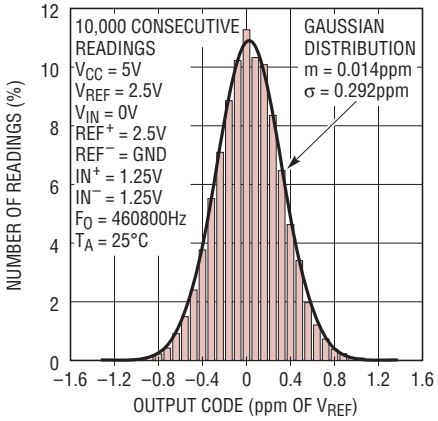


Noise Histogram (Output Rate = 7.5Hz, V_{CC} = 5V, V_{REF} = 2.5V)

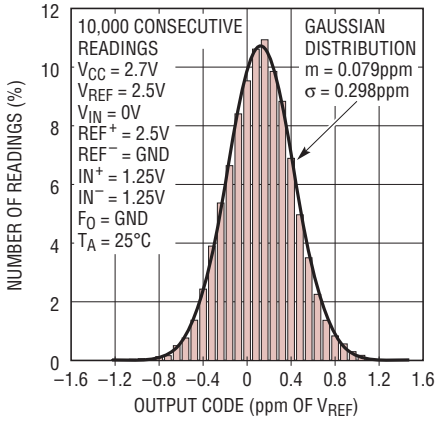


TYPICAL PERFORMANCE CHARACTERISTICS

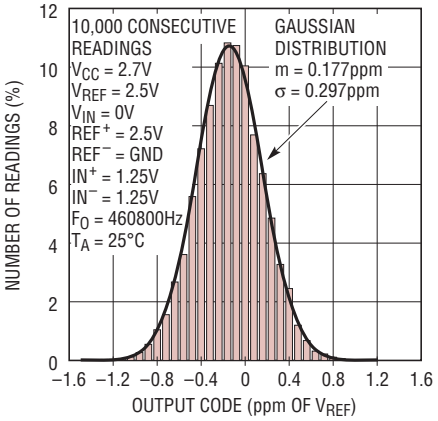
Noise Histogram (Output Rate = 22.5Hz, V_{CC} = 5V, V_{REF} = 2.5V)



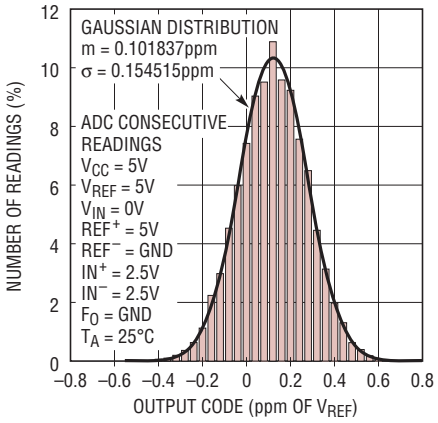
Noise Histogram (Output Rate = 7.5Hz, V_{CC} = 2.7V, V_{REF} = 2.5V)



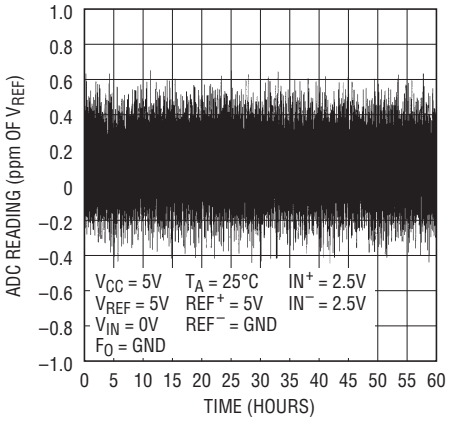
Noise Histogram (Output Rate = 22.5Hz, V_{CC} = 2.7V, V_{REF} = 2.5V)



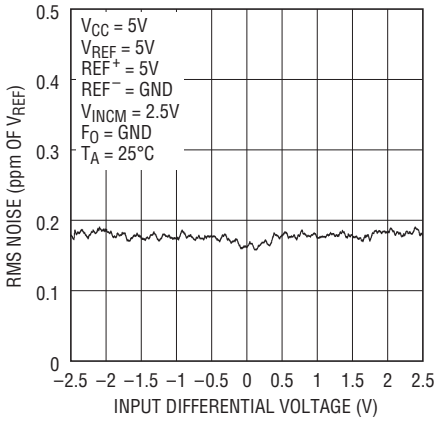
Long-Term Noise Histogram (Time = 60 Hrs, V_{CC} = 5V, V_{REF} = 5V)



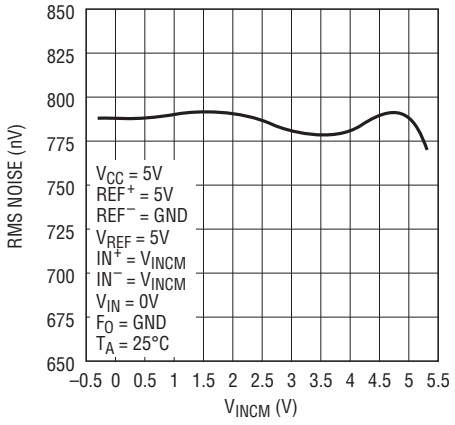
Consecutive ADC Readings vs Time



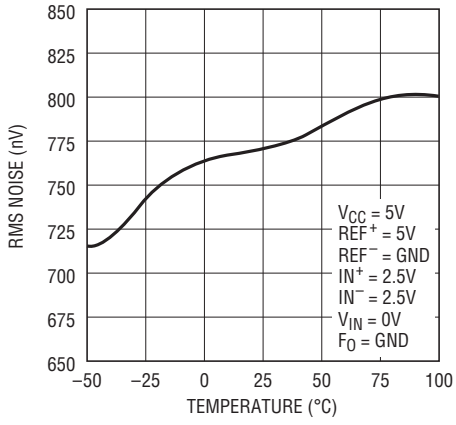
RMS Noise vs Input Differential Voltage



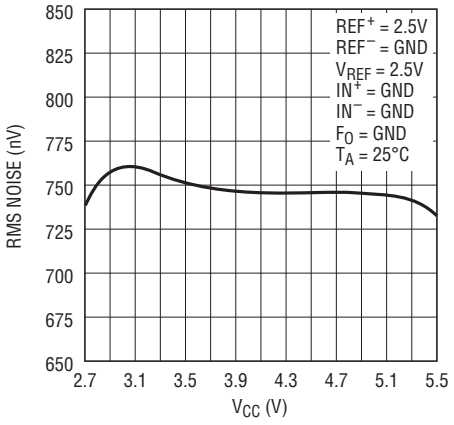
RMS Noise vs V_{INCM}



RMS Noise vs Temperature (T_A)

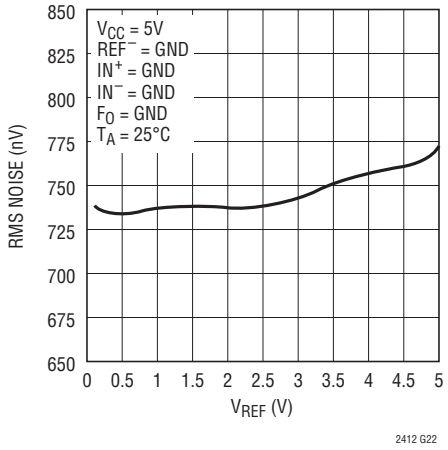


RMS Noise vs V_{CC}

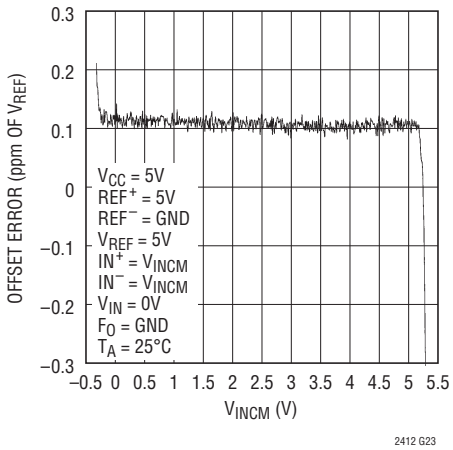


TYPICAL PERFORMANCE CHARACTERISTICS

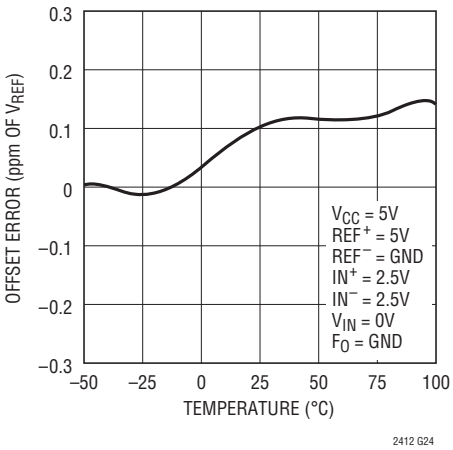
RMS Noise vs V_{REF}



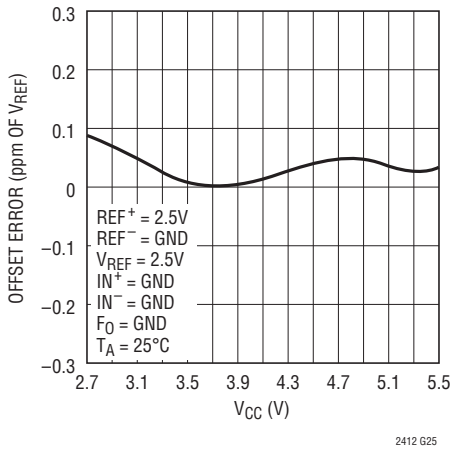
Offset Error vs V_{INCM}



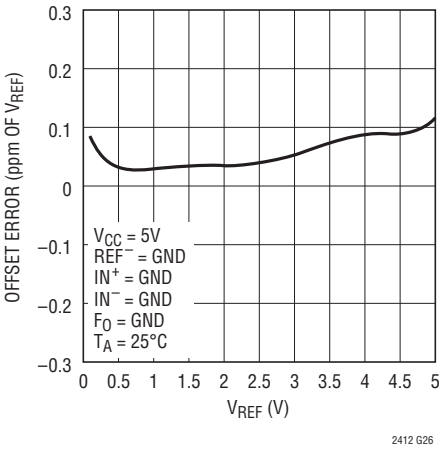
Offset Error vs Temperature (T_A)



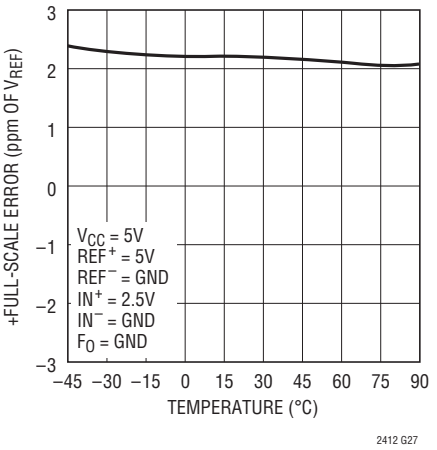
Offset Error vs V_{CC}



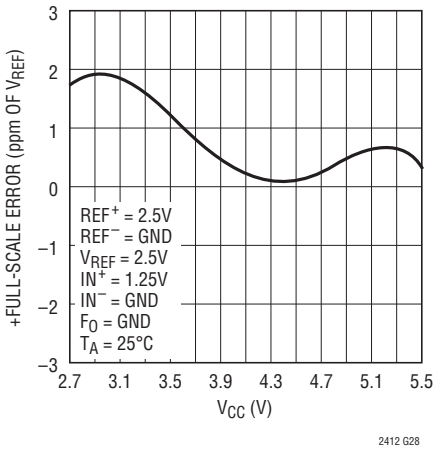
Offset Error vs V_{REF}



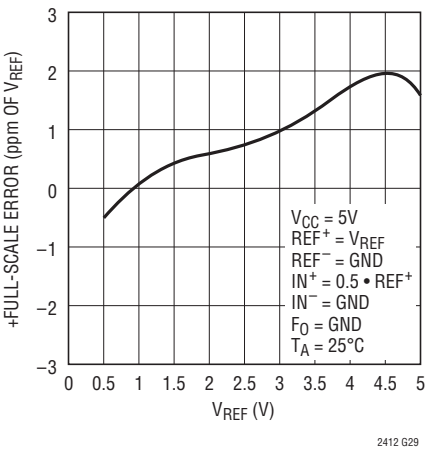
+Full-Scale Error vs Temperature (T_A)



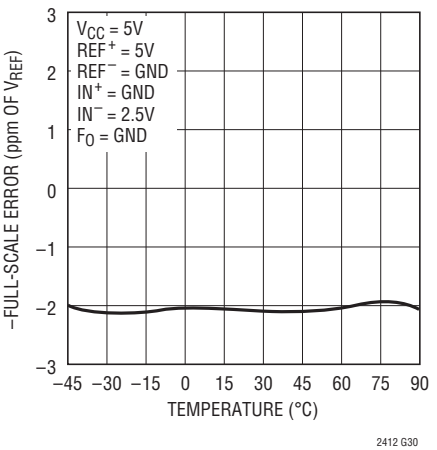
+Full-Scale Error vs V_{CC}



+Full-Scale Error vs V_{REF}

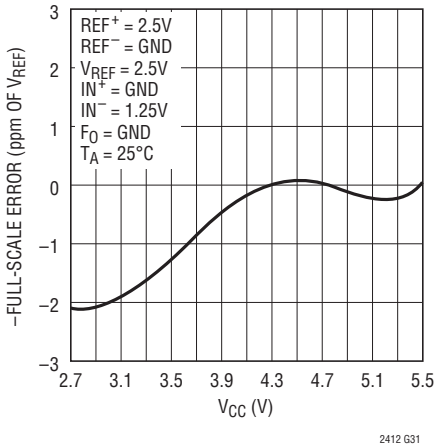


–Full-Scale Error vs Temperature (T_A)

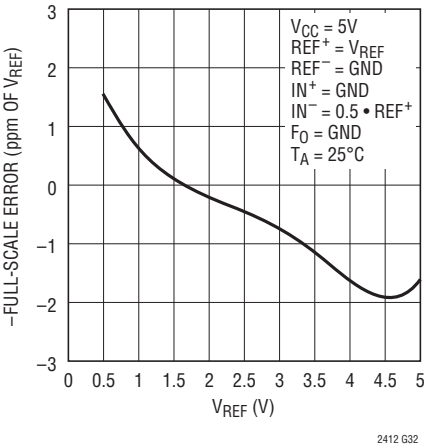


TYPICAL PERFORMANCE CHARACTERISTICS

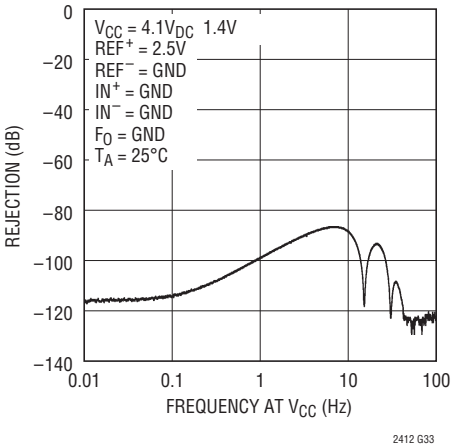
–Full-Scale Error vs V_{CC}



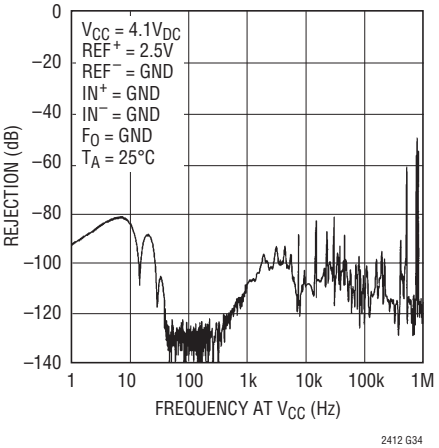
–Full-Scale Error vs V_{REF}



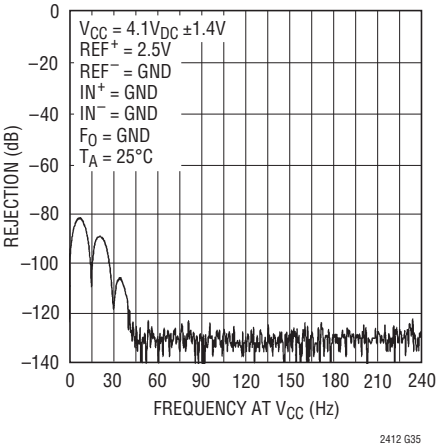
PSRR vs Frequency at V_{CC}



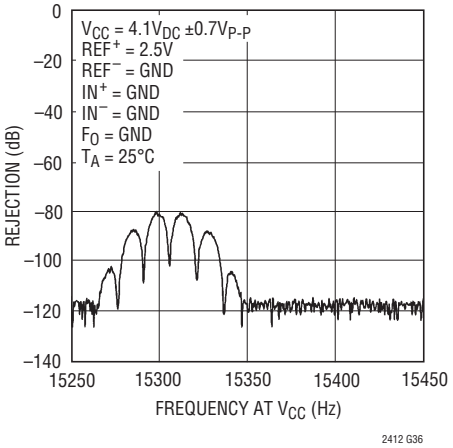
PSRR vs Frequency at V_{CC}



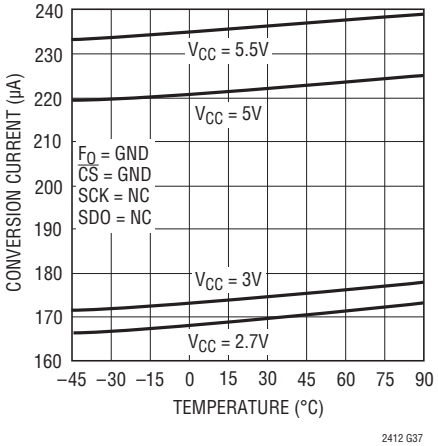
PSRR vs Frequency at V_{CC}



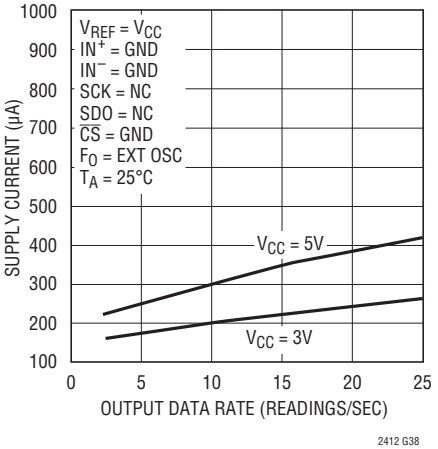
PSRR vs Frequency at V_{CC}



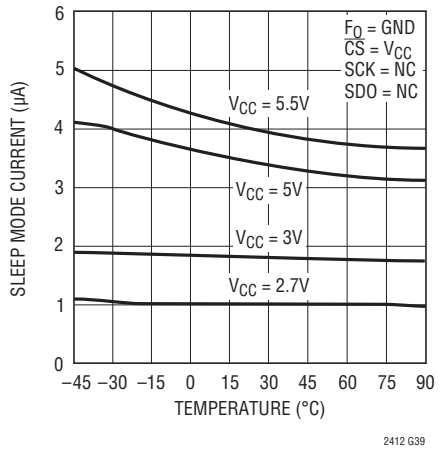
Conversion Current vs Temperature



Conversion Current vs Output Data Rate



Sleep Mode Current vs Temperature



PIN FUNCTIONS

V_{CC} (Pin 1): Positive Supply Voltage. Bypass to GND with a 10µF tantalum capacitor in parallel with 0.1µF ceramic capacitor as close to the part as possible.

REF^+ (Pin 2), REF^- (Pin 3): Differential Reference Input. The voltage on these pins can have any value between GND and V_{CC} as long as the reference positive input, REF^+, is maintained more positive than the reference negative input, REF^-, by at least 0.1V.

$CH0^+$ (Pin 4): Positive Input for Differential Channel 0.

$CH0^-$ (Pin 5): Negative Input for Differential Channel 0.

$CH1^+$ (Pin 6): Positive Input for Differential Channel 1.

$CH1^-$ (Pin 7): Negative Input for Differential Channel 1. The voltage on these four analog inputs (Pins 4 to 7) can have any value between GND and V_{CC}. Within these limits the converter bipolar input range ($V_{IN} = IN^+ – IN^-$) extends from $–0.5 • (V_{REF})$ to $0.5 • (V_{REF})$. Outside this input range the converter produces unique overrange and underrange output codes.

GND (Pins 8, 9, 10, 15, 16): Ground. Multiple ground pins internally connected for optimum ground current flow and V_{CC} decoupling. Connect each one of these pins to a ground plane through a low impedance connection. All five pins must be connected to ground for proper operation.

$\overline{CS}$ (Pin 11): Active LOW Digital Input. A LOW on this pin enables the SDO digital output and wakes up the ADC. Following each conversion the ADC automatically enters the Sleep mode and remains in this low power state as long as $\overline{CS}$ is HIGH. A LOW-to-HIGH transition on $\overline{CS}$ during the Data Output transfer aborts the data transfer and starts a new conversion.

SDO (Pin 12): Three-State Digital Output. During the Data Output period, this pin is used as serial data output. When the chip select $\overline{CS}$ is HIGH ($\overline{CS} = V_{CC}$) the SDO pin is in a high impedance state. During the Conversion and Sleep periods, this pin is used as the conversion status output. The conversion status can be observed by pulling $\overline{CS}$ LOW.

SCK (Pin 13): Bidirectional Digital Clock Pin. In Internal Serial Clock Operation mode, SCK is used as digital output for the internal serial interface clock during the Data Output period. In External Serial Clock Operation mode, SCK is used as digital input for the external serial interface clock during the Data Output period. A weak internal pull-up is automatically activated in Internal Serial Clock Operation mode. The Serial Clock Operation mode is determined by the logic level applied to the SCK pin at power up or during the most recent falling edge of $\overline{CS}$.

F_O (Pin 14): Frequency Control Pin. Digital input that controls the ADC's notch frequencies and conversion time. When the F_O pin is connected to V_{CC} ($F_O = V_{CC}$), the converter uses its internal oscillator and the digital filter first null is located at 50Hz. When the F_O pin is connected to GND ($F_O = 0V$), the converter uses its internal oscillator and the digital filter first null is located at 60Hz. When F_O is driven by an external clock signal with a frequency f_{EOSC}, the converter uses this signal as its system clock and the digital filter first null is located at a frequency $f_{EOSC}/2560$.

FUNCTIONAL BLOCK DIAGRAM

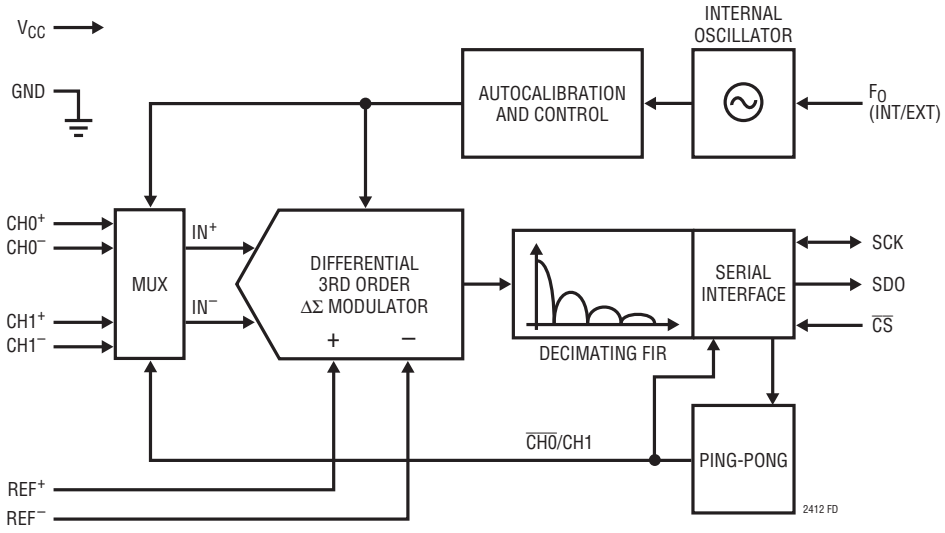
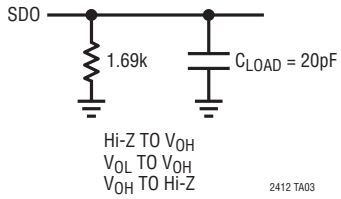
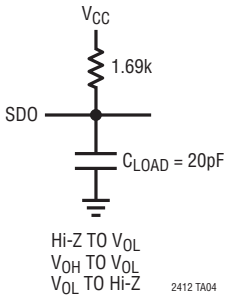


Figure 1. Functional Block Diagram

TEST CIRCUIT





APPLICATIONS INFORMATION

CONVERTER OPERATION

Converter Operation Cycle

The LTC2412 is a low power, ΔΣ ADC with automatic alternate channel selection between the two differential channels and an easy-to-use 3-wire serial interface (see Figure 1). Channel 0 is selected automatically at power up and the two channels are selected alternately afterwards (ping-pong). Its operation is made up of three states. The converter operating cycle begins with the conversion, followed by the low power sleep state and ends with the data output (see Figure 2). The 3-wire interface consists of serial data output (SDO), serial clock (SCK) and chip select ($\overline{CS}$).

Initially, the LTC2412 performs a conversion. Once the conversion is complete, the device enters the sleep state. The part remains in the sleep state as long as $\overline{CS}$ is HIGH. While in this sleep state, power consumption is reduced by nearly two orders of magnitude. The conversion result is held indefinitely in a static shift register while the converter is in the sleep state.

Once $\overline{CS}$ is pulled LOW, the device exits the low power mode and enters the data output state. If $\overline{CS}$ is pulled HIGH before the first rising edge of SCK, the device returns to the low power sleep mode and the conversion result is still held in the internal static shift register. If $\overline{CS}$ remains LOW after the first rising edge of SCK, the device begins outputting the conversion result. Taking $\overline{CS}$ high at this point will terminate the data output state and start a new conversion. There is no latency in the conversion result. The data output corresponds to the conversion just performed. This result is shifted out on the serial data out pin (SDO) under the control of the serial clock (SCK). Data is updated on the falling edge of SCK allowing the user to reliably latch data on the rising edge of SCK (see Figure 3). The data output state is concluded once 32 bits are read out of the ADC or when $\overline{CS}$ is brought HIGH. The device automatically initiates a new conversion and the cycle repeats.

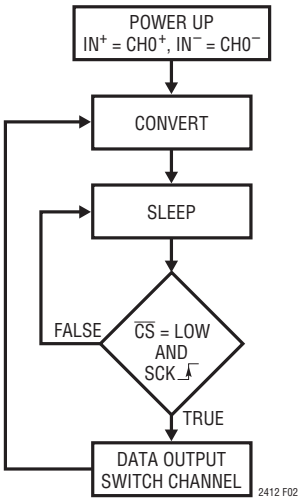


Figure 2. LTC2412 State Transition Diagram

Through timing control of the $\overline{CS}$ and SCK pins, the LTC2412 offers several flexible modes of operation (internal or external SCK and free-running conversion modes). These various modes do not require programming configuration registers; moreover, they do not disturb the cyclic operation described above. These modes of operation are described in detail in the Serial Interface Timing Modes section.

Conversion Clock

A major advantage the delta-sigma converter offers over conventional type converters is an on-chip digital filter (commonly implemented as a Sinc or Comb filter). For high resolution, low frequency applications, this filter is typically designed to reject line frequencies of 50Hz or 60Hz plus their harmonics. The filter rejection performance is directly related to the accuracy of the converter system clock. The LTC2412 incorporates a highly accurate on-chip oscillator. This eliminates the need for external frequency setting components such as crystals or oscillators. Clocked by the on-chip oscillator, the LTC2412 achieves a minimum of 110dB rejection at the line frequency (50Hz or 60Hz ±2%).

Ease of Use

The LTC2412 data output has no latency, filter settling delay or redundant data associated with the conversion cycle. There is a one-to-one correspondence between the conversion and the output data. Therefore, multiplexing multiple analog voltages is easy.

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The LTC2412 performs offset and full-scale calibrations every conversion cycle. This calibration is transparent to the user and has no effect on the cyclic operation described above. The advantage of continuous calibration is extreme stability of offset and full-scale readings with respect to time, supply voltage change and temperature drift.

Power-Up Sequence

The LTC2412 automatically enters an internal reset state when the power supply voltage V_{CC} drops below approximately 2V. This feature guarantees the integrity of the conversion result and of the serial interface mode selection. (See the 2-wire I/O sections in the Serial Interface Timing Modes section.)

When the V_{CC} voltage rises above this critical threshold, the converter creates an internal power-on-reset (POR) signal with a typical duration of 1ms. The POR signal clears all internal registers and selects channel 0. Following the POR signal, the LTC2412 starts a normal conversion cycle and follows the succession of states described above. The first conversion result following POR is accurate within the specifications of the device if the power supply voltage is restored within the operating range (2.7V to 5.5V) before the end of the POR time interval.

Reference Voltage Range

This converter accepts a truly differential external reference voltage. The absolute/common mode voltage specification for the REF^+ and REF^- pins covers the entire range from GND to V_{CC}. For correct converter operation, the REF^+ pin must always be more positive than the REF^- pin.

The LTC2412 can accept a differential reference voltage from 0.1V to V_{CC}. The converter output noise is determined by the thermal noise of the front-end circuits, and as such, its value in nanovolts is nearly constant with reference voltage. A decrease in reference voltage will not significantly improve the converter's effective resolution. On the other hand, a reduced reference voltage will improve the converter's overall INL performance. A reduced reference voltage will also improve the converter performance when operated with an external conversion clock (external F_O signal) at substantially higher output data rates (see the Output Data Rate section).

Input Voltage Range

The analog input is truly differential with an absolute/common mode range for the $CH0^+/CH0^-$ or $CH1^+/CH1^-$ input pins extending from GND – 0.3V to V_{CC} + 0.3V. Outside these limits, the ESD protection devices begin to turn on and the errors due to input leakage current increase rapidly. Within these limits, the LTC2412 converts the bipolar differential input signal, $V_{IN} = IN^+ – IN^-$, from –FS = –0.5 • V_{REF} to +FS = 0.5 • V_{REF} where $V_{REF} = REF^+ – REF^-$, with the selected channel referred as IN^+ and IN^-. Outside this range, the converter indicates the overrange or the underrange condition using distinct output codes.

Input signals applied to the analog input pins may extend by 300mV below ground and above V_{CC}. In order to limit any fault current, resistors of up to 5k may be added in series with the pins without affecting the performance of the device. In the physical layout, it is important to maintain the parasitic capacitance of the connection between these series resistors and the corresponding pins as low as possible; therefore, the resistors should be located as close as practical to the pins. The effect of the series resistance on the converter accuracy can be evaluated from the curves presented in the Input Current/Reference Current sections. In addition, series resistors will introduce a temperature dependent offset error due to the input leakage current. A 1nA input leakage current will develop a 1ppm offset error on a 5k resistor if V_{REF} = 5V. This error has a very strong temperature dependency.

Output Data Format

The LTC2412 serial output data stream is 32 bits long. The first 3 bits represent status information indicating the conversion state, selected channel and sign. The next 24 bits are the conversion result, MSB first. The remaining 5 bits are sub LSBs beyond the 24-bit level that may be included in averaging or discarded without loss of resolution. The third and fourth bit together are also used to indicate an underrange condition (the differential input voltage is below –FS) or an overrange condition (the differential input voltage is above +FS).

APPLICATIONS INFORMATION

Bit 31 (first output bit) is the end of conversion ($\overline{EOC}$) indicator. This bit is available at the SDO pin during the conversion and sleep states whenever the $\overline{CS}$ pin is LOW. This bit is HIGH during the conversion and goes LOW when the conversion is complete.

Bit 30 (second output bit) is the selected channel indicator. The bit is LOW for channel 0 and HIGH for channel 1 selected.

Bit 29 (third output bit) is the conversion result sign indicator (SIG). If V_{IN} is >0, this bit is HIGH. If V_{IN} is <0, this bit is LOW.

Bit 28 (fourth output bit) is the most significant bit (MSB) of the result. This bit in conjunction with Bit 29 also provides the underrange or overrange indication. If both Bit 29 and Bit 28 are HIGH, the differential input voltage is above +FS. If both Bit 29 and Bit 28 are LOW, the differential input voltage is below –FS.

The function of these bits is summarized in Table 1.

Table 1. LTC2412 Status Bits

Input Range	Bit 31 $\overline{EOC}$	Bit 30 $\overline{CH0}$/CH1	Bit 29 SIG	Bit 28 MSB
$V_{IN} \geq 0.5 \cdot V_{REF}$	0	0 or 1	1	1
$0V \leq V_{IN} < 0.5 \cdot V_{REF}$	0	0 or 1	1	0
$-0.5 \cdot V_{REF} \leq V_{IN} < 0V$	0	0 or 1	0	1
$V_{IN} < -0.5 \cdot V_{REF}$	0	0 or 1	0	0

Bits 28-5 are the 24-bit conversion result MSB first.

Bit 5 is the least significant bit (LSB).

Bits 4-0 are sub LSBs below the 24-bit level. Bits 4-0 may be included in averaging or discarded without loss of resolution.

Data is shifted out of the SDO pin under control of the serial clock (SCK), see Figure 3. Whenever $\overline{CS}$ is HIGH, SDO remains high impedance and any externally generated SCK clock pulses are ignored by the internal data out shift register.

In order to shift the conversion result out of the device, $\overline{CS}$ must first be driven LOW. $\overline{EOC}$ is seen at the SDO pin of the device once $\overline{CS}$ is pulled LOW. $\overline{EOC}$ changes real time from HIGH to LOW at the completion of a conversion. This signal may be used as an interrupt for an external microcontroller. Bit 31 ($\overline{EOC}$) can be captured on the first rising edge of SCK. Bit 30 is shifted out of the device on the first falling edge of SCK. The final data bit (Bit 0) is shifted out on the falling edge of the 31st SCK and may be latched on the rising edge of the 32nd SCK pulse. On the falling edge of the 32nd SCK pulse, SDO goes HIGH indicating the initiation of a new conversion cycle. This bit serves as $\overline{EOC}$ (Bit 31) for the next conversion cycle. Table 2 summarizes the output data format.

As long as the voltage on the analog input pins is maintained within the –0.3V to (V_{CC} + 0.3V) absolute maximum operating range, a conversion result is generated for any differential input voltage V_{IN} from –FS = $-0.5 \cdot V_{REF}$ to +FS = $0.5 \cdot V_{REF}$. For differential input voltages greater than +FS, the conversion result is clamped to the value corresponding to the +FS + 1LSB. For differential input voltages below –FS, the conversion result is clamped to the value corresponding to –FS – 1LSB.

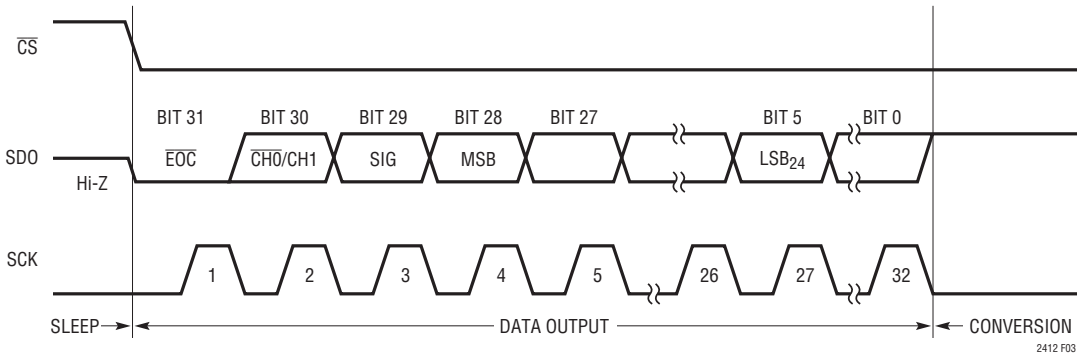

Figure 3. Output Data Timing

APPLICATIONS INFORMATION

Table 2. LTC2412 Output Data Format

Differential Input Voltage V_{IN}*	Bit 31 $\overline{EOC}$	Bit 30 $\overline{CH0}$/CH1	Bit 29 SIG	Bit 28 MSB	Bit 27	Bit 26	Bit 25	…	Bit 0
V_{IN}* ≥ 0.5 • V_{REF}**	0	0/1	1	1	0	0	0	…	0
0.5 • V_{REF}** – 1LSB	0	0/1	1	0	1	1	1	…	1
0.25 • V_{REF}**	0	0/1	1	0	1	0	0	…	0
0.25 • V_{REF}** – 1LSB	0	0/1	1	0	0	1	1	…	1
0	0	0/1	1	0	0	0	0	…	0
–1LSB	0	0/1	0	1	1	1	1	…	1
–0.25 • V_{REF}**	0	0/1	0	1	1	0	0	…	0
–0.25 • V_{REF}** – 1LSB	0	0/1	0	1	0	1	1	…	1
–0.5 • V_{REF}**	0	0/1	0	1	0	0	0	…	0
V_{IN}* < –0.5 • V_{REF}**	0	0/1	0	0	1	1	1	…	1

*The differential input voltage $V_{IN} = IN^+ – IN^–$.
**The differential reference voltage $V_{REF} = REF^+ – REF^–$.

Frequency Rejection Selection (F_O)

The LTC2412 internal oscillator provides better than 110dB normal mode rejection at the line frequency and all its harmonics for 50Hz ±2% or 60Hz ±2%. For 60Hz rejection, F_O should be connected to GND while for 50Hz rejection the F_O pin should be connected to V_{CC}.

The selection of 50Hz or 60Hz rejection can also be made by driving F_O to an appropriate logic level. A selection change during the sleep or data output states will not disturb the converter operation. If the selection is made during the conversion state, the result of the conversion in progress may be outside specifications but the following conversions will not be affected.

When a fundamental rejection frequency different from 50Hz or 60Hz is required or when the converter must be synchronized with an outside source, the LTC2412 can operate with an external conversion clock. The converter automatically detects the presence of an external clock signal at the F_O pin and turns off the internal oscillator. The frequency f_{EOSC} of the external signal must be at least 2560Hz (1Hz notch frequency) to be detected. The external clock signal duty cycle is not significant as long as the minimum and maximum specifications for the high and low periods t_{HEO} and t_{LEO} are observed.

While operating with an external conversion clock of a frequency f_{EOSC}, the LTC2412 provides better than 110dB normal mode rejection in a frequency range $f_{EOSC}/2560$ ±4% and its harmonics. The normal mode rejection as a function of the input frequency deviation from $f_{EOSC}/2560$ is shown in Figure 4.

Whenever an external clock is not present at the F_O pin, the converter automatically activates its internal oscillator and enters the Internal Conversion Clock mode. The LTC2412 operation will not be disturbed if the change of conversion clock source occurs during the sleep state or during the data output state while the converter uses an external serial clock. If the change occurs during the conversion state, the result of the conversion in progress

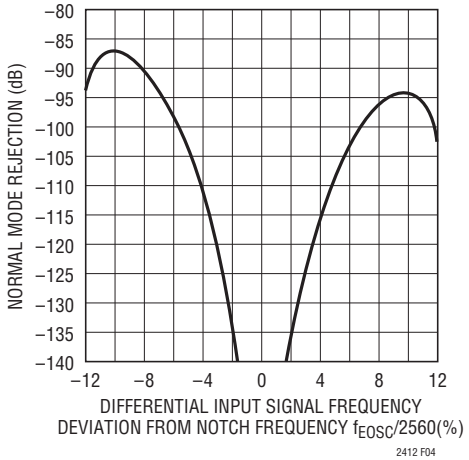

Figure 4. LTC2412 Normal Mode Rejection When Using an External Oscillator of Frequency f_{EOSC}

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may be outside specifications but the following conversions will not be affected. If the change occurs during the data output state and the converter is in the Internal SCK mode, the serial clock duty cycle may be affected but the serial data stream will remain valid.

Table 3 summarizes the duration of each state and the achievable output data rate as a function of F_O.

SERIAL INTERFACE PINS

The LTC2412 transmits the conversion results and receives the start of conversion command through a synchronous 3-wire interface. During the conversion and sleep states, this interface can be used to assess the converter status and during the data output state it is used to read the conversion result.

Serial Clock Input/Output (SCK)

The serial clock signal present on SCK (Pin 13) is used to synchronize the data transfer. Each bit of data is shifted out the SDO pin on the falling edge of the serial clock.

In the Internal SCK mode of operation, the SCK pin is an output and the LTC2412 creates its own serial clock by dividing the internal conversion clock by 8. In the External SCK mode of operation, the SCK pin is used as input. The internal or external SCK mode is selected on power-up and then reselected every time a HIGH-to-LOW transition is detected at the $\overline{CS}$ pin. If SCK is HIGH or floating at power-up or during this transition, the converter enters the internal SCK mode. If SCK is LOW at power-up or during this transition, the converter enters the external SCK mode.

Serial Data Output (SDO)

The serial data output pin, SDO (Pin 12), provides the result of the last conversion as a serial bit stream (MSB first) during the data output state. In addition, the SDO pin is used as an end of conversion indicator during the conversion and sleep states.

When $\overline{CS}$ (Pin 11) is HIGH, the SDO driver is switched to a high impedance state. This allows sharing the serial interface with other devices. If $\overline{CS}$ is LOW during the convert or sleep state, SDO will output EOC. If $\overline{CS}$ is LOW during the conversion phase, the $\overline{EOC}$ bit appears HIGH on the SDO pin. Once the conversion is complete, $\overline{EOC}$ goes LOW.

Chip Select Input ($\overline{CS}$)

The active LOW chip select, $\overline{CS}$ (Pin 11), is used to test the conversion status and to enable the data output transfer as described in the previous sections.

In addition, the $\overline{CS}$ signal can be used to trigger a new conversion cycle before the entire serial data transfer has been completed. The LTC2412 will abort any serial data transfer in progress and start a new conversion cycle any-

Table 3. LTC2412 State Duration

State	Operating Mode		Duration
CONVERT	Internal Oscillator	F_O = LOW (60Hz Rejection)	133ms, Output Data Rate ≤ 7.5 Readings/s
		F_O = HIGH (50Hz Rejection)	160ms, Output Data Rate ≤ 6.2 Readings/s
	External Oscillator	F_O = External Oscillator with Frequency f_{EOSC} kHz (f_{EOSC}/2560 Rejection)	20510/f_{EOSC}s, Output Data Rate ≤ f_{EOSC}/20510 Readings/s
SLEEP			As Long As $\overline{CS}$ = HIGH
DATA OUTPUT	Internal Serial Clock	F_O = LOW/HIGH (Internal Oscillator)	As Long As $\overline{CS}$ = LOW But Not Longer Than 1.67ms (32 SCK cycles)
		F_O = External Oscillator with Frequency f_{EOSC} kHz	As Long As $\overline{CS}$ = LOW But Not Longer Than 256/f_{EOSC}ms (32 SCK cycles)
	External Serial Clock with Frequency f_{SCK} kHz		As Long As $\overline{CS}$ = LOW But Not Longer Than 32/f_{SCK}ms (32 SCK cycles)

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time a LOW-to-HIGH transition is detected at the $\overline{CS}$ pin after the converter has entered the data output state (i.e., after the first rising edge of SCK occurs with $\overline{CS}$ = LOW).

Finally, $\overline{CS}$ can be used to control the free-running modes of operation, see Serial Interface Timing Modes section. Grounding $\overline{CS}$ will force the ADC to continuously convert at the maximum output rate selected by F_O.

SERIAL INTERFACE TIMING MODES

The LTC2412's 3-wire interface is SPI and MICROWIRE compatible. This interface offers several flexible modes of operation. These include internal/external serial clock, 2- or 3-wire I/O, single cycle conversion and auto-start. The following sections describe each of these serial interface timing modes in detail. In all these cases, the converter can use the internal oscillator (F_O = LOW or F_O = HIGH) or an external oscillator connected to the F_O pin. Refer to Table 4 for a summary.

External Serial Clock, Single Cycle Operation (SPI/MICROWIRE Compatible)

This timing mode uses an external serial clock to shift out the conversion result and a $\overline{CS}$ signal to monitor and control the state of the conversion cycle, see Figure 5.

The serial clock mode is selected on the falling edge of $\overline{CS}$. To select the external serial clock mode, the serial clock pin (SCK) must be LOW during each $\overline{CS}$ falling edge.

Table 4. LTC2412 Interface Timing Modes

Configuration	SCK Source	Conversion Cycle Control	Data Output Control	Connection and Waveforms
External SCK, Single Cycle Conversion	External	$\overline{CS}$ and SCK	$\overline{CS}$ and SCK	Figures 5, 6
External SCK, 2-Wire I/O	External	SCK	SCK	Figure 7
Internal SCK, Single Cycle Conversion	Internal	$\overline{CS}$ ↓	$\overline{CS}$ ↓	Figures 8, 9
Internal SCK, 2-Wire I/O, Continuous Conversion	Internal	Continuous	Internal	Figure 10

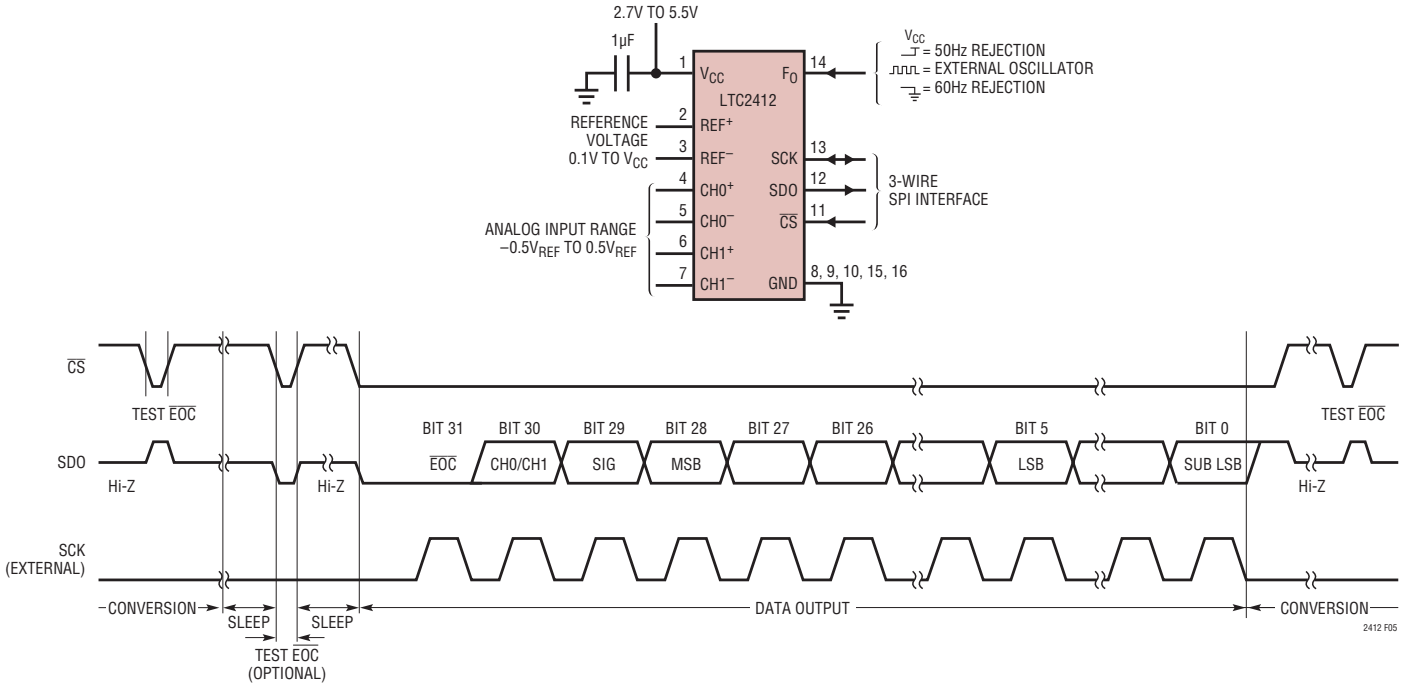

Figure 5. External Serial Clock, Single Cycle Operation

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The serial data output pin (SDO) is Hi-Z as long as $\overline{CS}$ is HIGH. At any time during the conversion cycle, $\overline{CS}$ may be pulled LOW in order to monitor the state of the converter. While $\overline{CS}$ is pulled LOW, $\overline{EOC}$ is output to the SDO pin. $\overline{EOC}$ = 1 while a conversion is in progress and $\overline{EOC}$ = 0 if the device is in the sleep state. With $\overline{CS}$ high, the device automatically enters the low power sleep state once the conversion is complete.

When the device is in the sleep state ($\overline{EOC}$ = 0), its conversion result is held in an internal static shift register. Data is shifted out the SDO pin on each falling edge of SCK. This enables external circuitry to latch the output on the rising edge of SCK. $\overline{EOC}$ can be latched on the first rising edge of SCK and the last bit of the conversion result can be latched on the 32nd rising edge of SCK. On the 32nd falling edge of SCK, the device begins a new conversion. SDO goes HIGH ($\overline{EOC}$ = 1) indicating a conversion is in progress.

At the conclusion of the data cycle, $\overline{CS}$ may remain LOW and $\overline{EOC}$ monitored as an end-of-conversion interrupt. Alternatively, $\overline{CS}$ may be driven HIGH setting SDO to Hi-Z.

As described above, $\overline{CS}$ may be pulled LOW at any time in order to monitor the conversion status.

Typically, $\overline{CS}$ remains LOW during the data output state. However, the data output state may be aborted by pulling $\overline{CS}$ HIGH anytime between the first rising edge and the 32nd falling edge of SCK, see Figure 6. On the rising edge of $\overline{CS}$, the device aborts the data output state and immediately initiates a new conversion. This is useful for systems not requiring all 32 bits of output data, aborting an invalid conversion cycle or synchronizing the start of a conversion.

External Serial Clock, 2-Wire I/O

This timing mode utilizes a 2-wire serial I/O interface. The conversion result is shifted out of the device by an externally generated serial clock (SCK) signal, see Figure 7. $\overline{CS}$ may be permanently tied to ground, simplifying the user interface or isolation barrier.

The external serial clock mode is selected at the end of the power-on reset (POR) cycle. The POR cycle is concluded

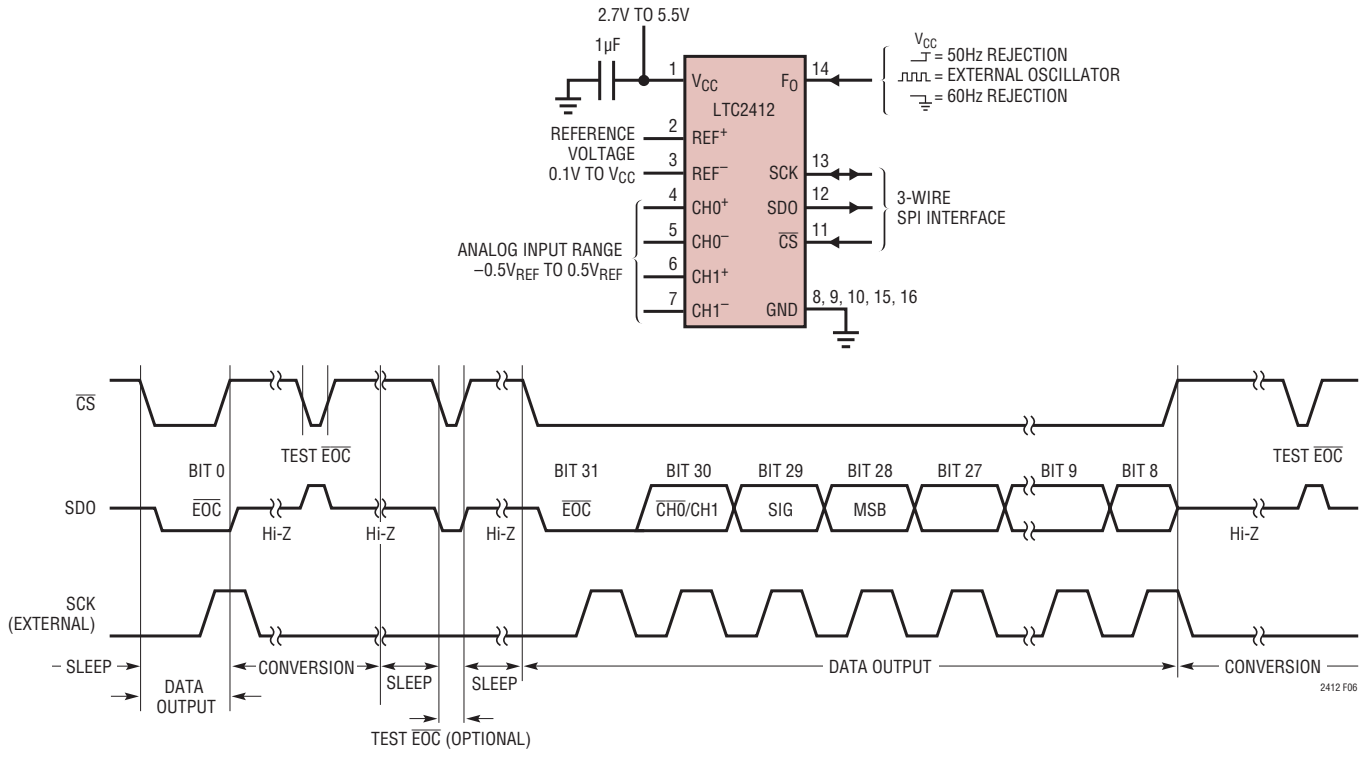

Figure 6. External Serial Clock, Reduced Data Output Length

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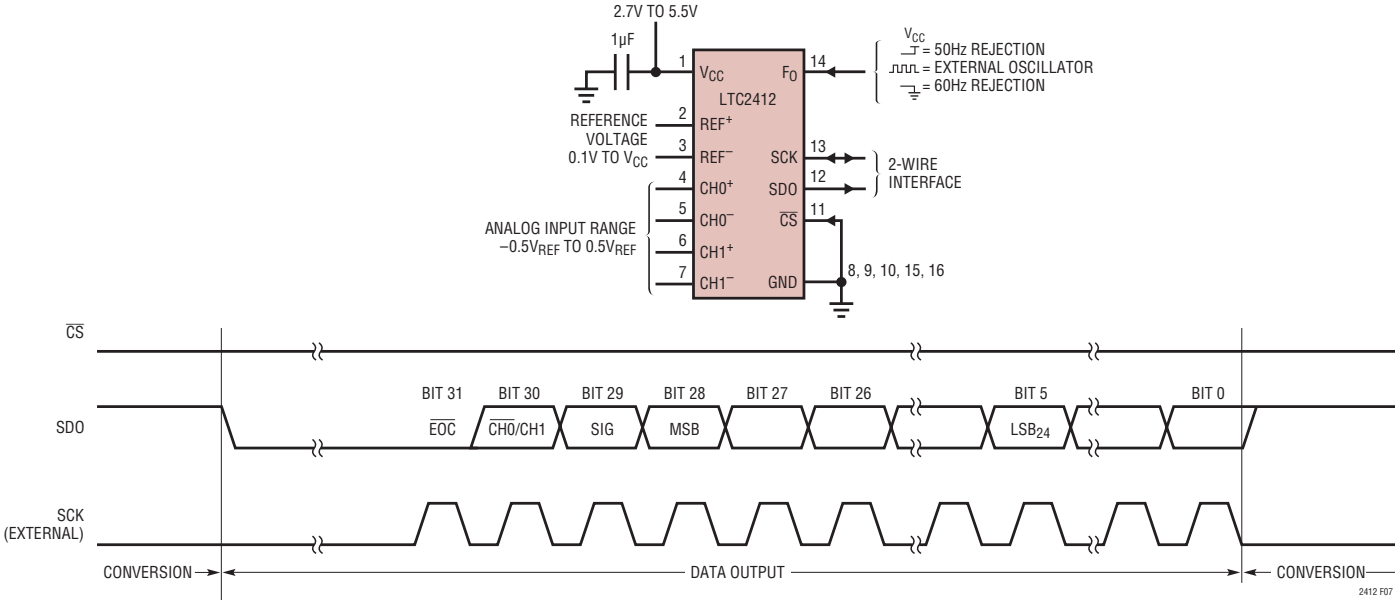

Figure 7. External Serial Clock, $\overline{CS}$ = 0 Operation (2-Wire)

typically 1ms after V_{CC} exceeds 2V. The level applied to SCK at this time determines if SCK is internal or external. SCK must be driven LOW prior to the end of POR in order to enter the external serial clock timing mode.

Since $\overline{CS}$ is tied LOW, the end-of-conversion ($\overline{EOC}$) can be continuously monitored at the SDO pin during the convert and sleep states. $\overline{EOC}$ may be used as an interrupt to an external controller indicating the conversion result is ready. $\overline{EOC}$ = 1 while the conversion is in progress and $\overline{EOC}$ = 0 once the conversion ends. On the falling edge of $\overline{EOC}$, the conversion result is loaded into an internal static shift register. Data is shifted out the SDO pin on each falling edge of SCK enabling external circuitry to latch data on the rising edge of SCK. $\overline{EOC}$ can be latched on the first rising edge of SCK. On the 32nd falling edge of SCK, SDO goes HIGH ($\overline{EOC}$ = 1) indicating a new conversion has begun.

Internal Serial Clock, Single Cycle Operation

This timing mode uses an internal serial clock to shift out the conversion result and a $\overline{CS}$ signal to monitor and control the state of the conversion cycle, see Figure 8.

In order to select the internal serial clock timing mode, the serial clock pin (SCK) must be floating (Hi-Z) or pulled HIGH prior to the falling edge of $\overline{CS}$. The device will not enter the internal serial clock mode if SCK is driven LOW on the falling edge of $\overline{CS}$. An internal weak pull-up resistor is active on the SCK pin during the falling edge of $\overline{CS}$; therefore, the internal serial clock timing mode is automatically selected if SCK is not externally driven.

The serial data output pin (SDO) is Hi-Z as long as $\overline{CS}$ is HIGH. At any time during the conversion cycle, $\overline{CS}$ may be pulled LOW in order to monitor the state of the converter. Once $\overline{CS}$ is pulled LOW, SCK goes LOW and $\overline{EOC}$ is output to the SDO pin. $\overline{EOC}$ = 1 while a conversion is in progress and $\overline{EOC}$ = 0 if the device is in the sleep state.

When testing $\overline{EOC}$, if the conversion is complete ($\overline{EOC}$ = 0), the device will exit the sleep state during the $\overline{EOC}$ test. In order to allow the device to return to the low power sleep state, $\overline{CS}$ must be pulled HIGH before the first rising edge of SCK. In the internal SCK timing mode, SCK goes HIGH and the device begins outputting data at time $t_{EOCtest}$ after the falling edge of $\overline{CS}$ (if $\overline{EOC}$ = 0) or $t_{EOCtest}$ after $\overline{EOC}$ goes LOW (if $\overline{CS}$ is LOW during the falling edge of $\overline{EOC}$). The value of $t_{EOCtest}$ is 23µs if the device is using its internal oscillator (F_O = logic LOW or HIGH). If F_O is driven by an external oscillator of frequency fEOSC, then $t_{EOCtest}$ is 3.6/fEOSC. If $\overline{CS}$ is pulled HIGH before time $t_{EOCtest}$, the device

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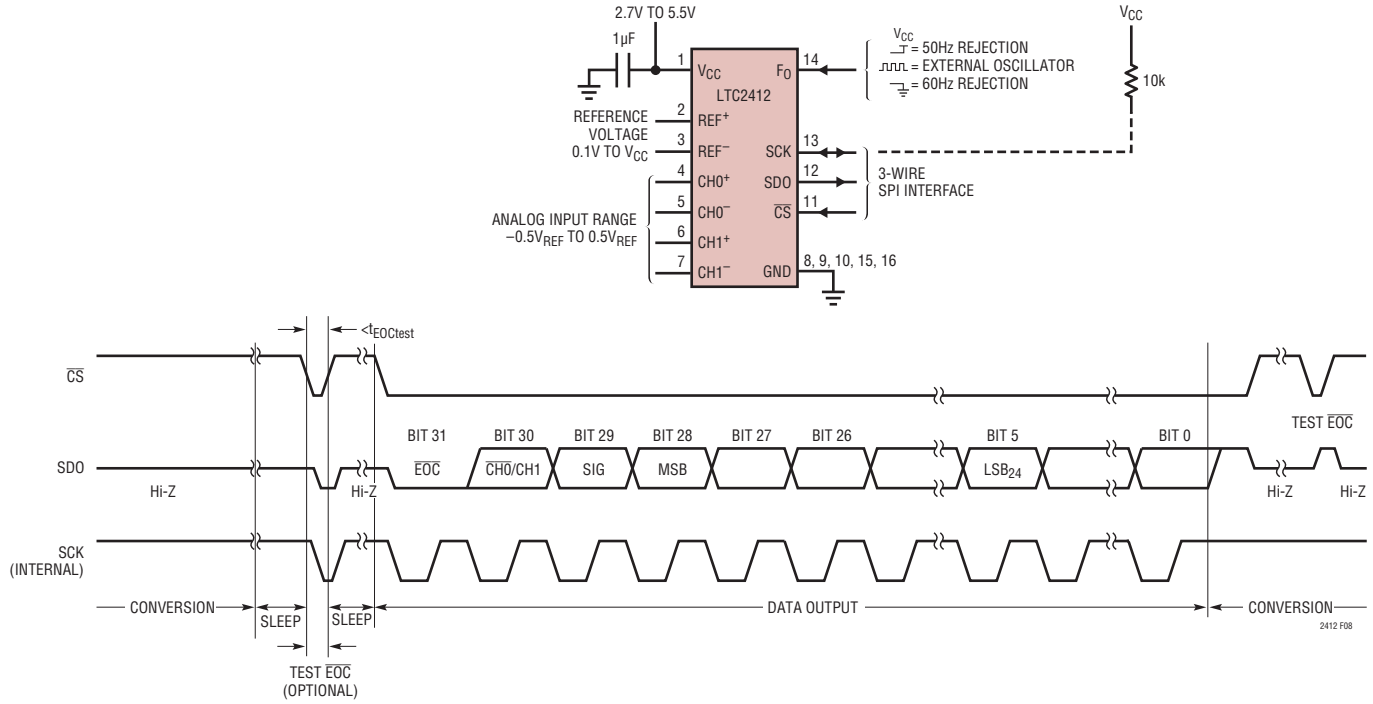

Figure 8. Internal Serial Clock, Single Cycle Operation

returns to the sleep state and the conversion result is held in the internal static shift register.

If $\overline{CS}$ remains LOW longer than $t_{EOCtest}$, the first rising edge of SCK will occur and the conversion result is serially shifted out of the SDO pin. The data output cycle concludes after the 32nd rising edge. Data is shifted out the SDO pin on each falling edge of SCK. The internally generated serial clock is output to the SCK pin. This signal may be used to shift the conversion result into external circuitry. $\overline{EOC}$ can be latched on the first rising edge of SCK and the last bit of the conversion result on the 32nd rising edge of SCK. After the 32nd rising edge, SDO goes HIGH ($\overline{EOC}$ = 1), SCK stays HIGH and a new conversion starts.

Typically, $\overline{CS}$ remains LOW during the data output state. However, the data output state may be aborted by pulling $\overline{CS}$ HIGH anytime between the first and 32nd rising edge of SCK, see Figure 9. On the rising edge of $\overline{CS}$, the device aborts the data output state and immediately initiates a new conversion. This is useful for systems not requiring all 32 bits of output data, aborting an invalid conversion cycle, or synchronizing the start of a conversion. If $\overline{CS}$ is pulled HIGH while the converter is driving SCK LOW, the internal pull-up is not available to restore SCK to a logic HIGH state. This will cause the device to exit the internal serial clock mode on the next falling edge of $\overline{CS}$. This can be avoided by adding an external 10k pull-up resistor to the SCK pin or by never pulling $\overline{CS}$ HIGH when SCK is LOW.

Whenever SCK is LOW, the LTC2412's internal pull-up at pin SCK is disabled. Normally, SCK is not externally driven if the device is in the internal SCK timing mode. However, certain applications may require an external driver on SCK. If this driver goes Hi-Z after outputting a LOW signal, the LTC2412's internal pull-up remains disabled. Hence, SCK remains LOW. On the next falling edge of $\overline{CS}$, the device is switched to the external SCK timing mode. By adding an external 10k pull-up resistor to SCK, this pin goes HIGH once the external driver goes Hi-Z. On the next $\overline{CS}$ falling edge, the device will remain in the internal SCK timing mode.

A similar situation may occur during the sleep state when $\overline{CS}$ is pulsed HIGH-LOW-HIGH in order to test the conversion status. If the device is in the sleep state ($\overline{EOC}$ = 0), SCK will go LOW. Once $\overline{CS}$ goes HIGH (within the time period defined above as $t_{EOCtest}$), the internal pull-up is activated. For a heavy capacitive load on the SCK pin, the internal pull-up may not be adequate to return SCK

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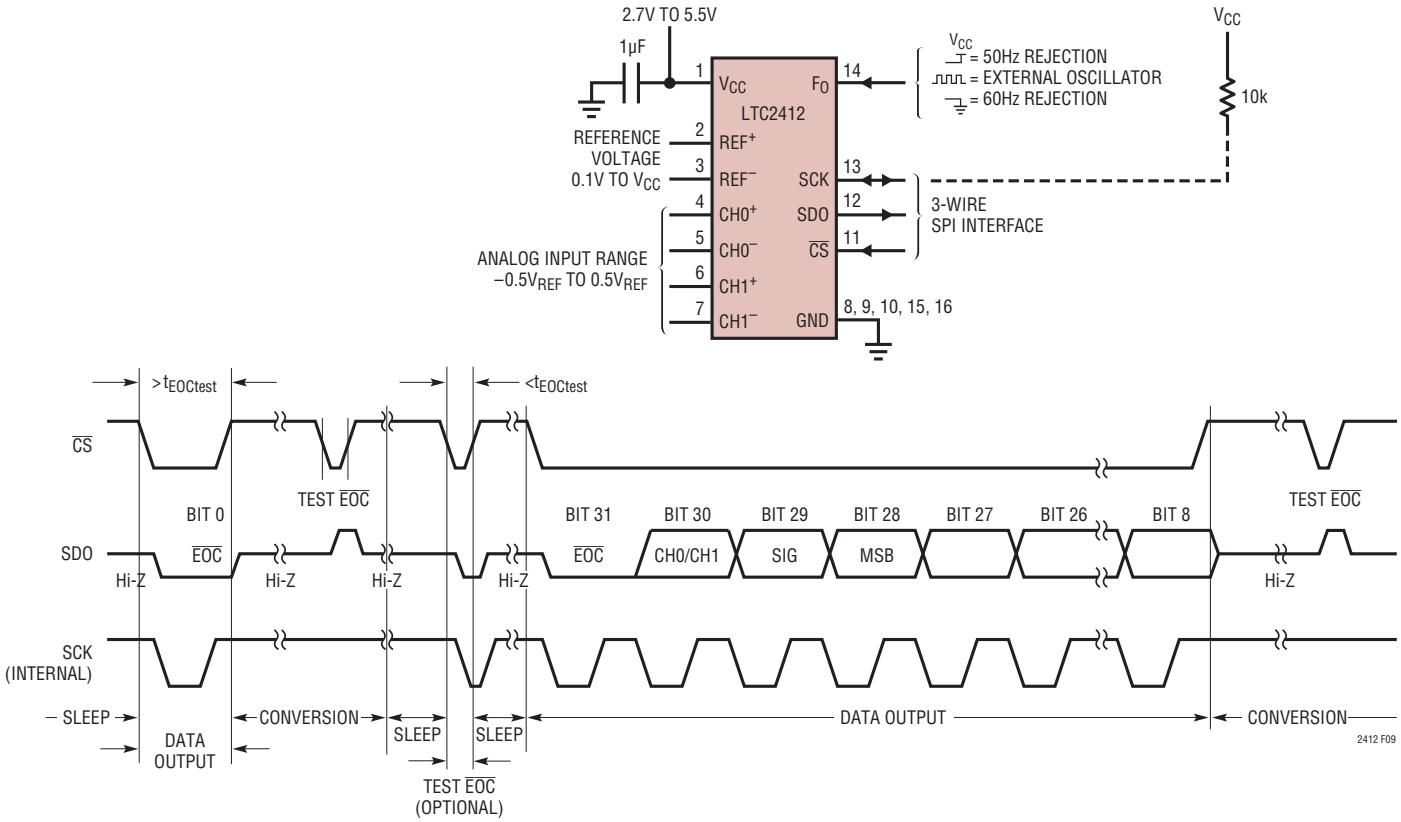

Figure 9. Internal Serial Clock, Reduced Data Output Length

to a HIGH level before $\overline{CS}$ goes low again. This is not a concern under normal conditions where $\overline{CS}$ remains LOW after detecting $\overline{EOC}$ = 0. This situation is easily overcome by adding an external 10k pull-up resistor to the SCK pin.

Internal Serial Clock, 2-Wire I/O, Continuous Conversion

This timing mode uses a 2-wire, all output (SCK and SDO) interface. The conversion result is shifted out of the device by an internally generated serial clock (SCK) signal, see Figure 10. $\overline{CS}$ may be permanently tied to ground, simplifying the user interface or isolation barrier.

The internal serial clock mode is selected at the end of the power-on reset (POR) cycle. The POR cycle is concluded approximately 1ms after V_{CC} exceeds 2V. An internal weak pull-up is active during the POR cycle; therefore, the internal serial clock timing mode is automatically selected if SCK is not externally driven LOW (if SCK is loaded such that the internal pull-up cannot pull the pin HIGH, the external SCK mode will be selected).

During the conversion, the SCK and the serial data output pin (SDO) are HIGH ($\overline{EOC}$ = 1). Once the conversion is complete, SCK and SDO go LOW ($\overline{EOC}$ = 0) indicating the conversion has finished and the device has entered the data output state. The data output cycle begins on the first rising edge of SCK and ends after the 32nd rising edge. Data is shifted out the SDO pin on each falling edge of SCK. The internally generated serial clock is output to the SCK pin. This signal may be used to shift the conversion result into external circuitry. $\overline{EOC}$ can be latched on the first rising edge of SCK and the last bit of the conversion result can be latched on the 32nd rising edge of SCK. After the 32nd rising edge, SDO goes HIGH ($\overline{EOC}$ = 1) indicating a new conversion is in progress. SCK remains HIGH during the conversion.

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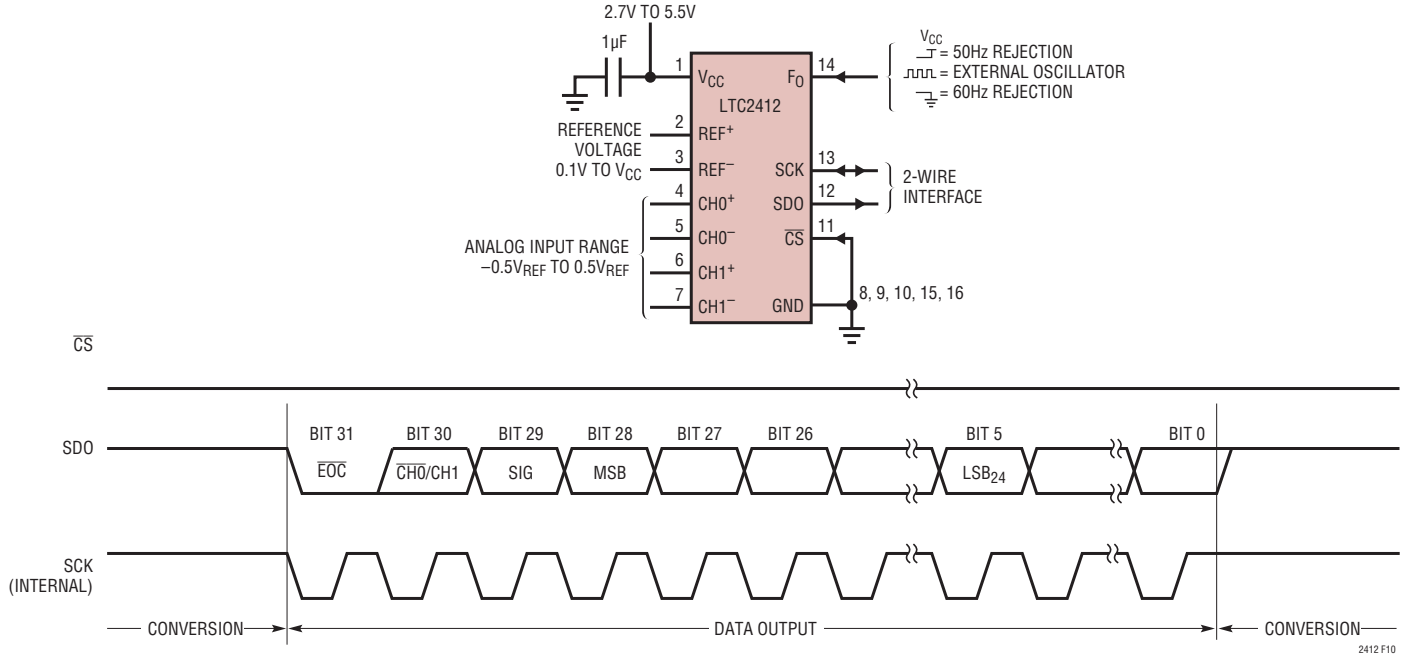

Figure 10. Internal Serial Clock, Continuous Operation

PRESERVING THE CONVERTER ACCURACY

The LTC2412 is designed to reduce as much as possible the conversion result sensitivity to device decoupling, PCB layout, anti-aliasing circuits, line frequency perturbations and so on. Nevertheless, in order to preserve the extreme accuracy capability of this part, some simple precautions are desirable.

Digital Signal Levels

The LTC2412's digital interface is easy to use. Its digital inputs (F_O, $\overline{CS}$ and SCK in External SCK mode of operation) accept standard TTL/CMOS logic levels and the internal hysteresis receivers can tolerate edge rates as slow as 100µs. However, some considerations are required to take advantage of the exceptional accuracy and low supply current of this converter.

The digital output signals (SDO and SCK in Internal SCK mode of operation) are less of a concern because they are not generally active during the conversion state.

While a digital input signal is in the range 0.5V to (V_{CC} – 0.5V), the CMOS input receiver draws additional current from the power supply. It should be noted that, when any one of the digital input signals (F_O, $\overline{CS}$ and SCK in External SCK mode of operation) is within this range, the LTC2412 power supply current may increase even if the signal in question is at a valid logic level. For micropower operation, it is recommended to drive all digital input signals to full CMOS levels [V_{IL} < 0.4V and V_{OH} > (V_{CC} – 0.4V)].

During the conversion period, the undershoot and/or overshoot of a fast digital signal connected to the LTC2412 pins may severely disturb the analog to digital conversion process. Undershoot and overshoot can occur because of the impedance mismatch at the converter pin when the transition time of an external control signal is less than twice the propagation delay from the driver to LTC2412. For reference, on a regular FR-4 board, signal propagation velocity is approximately 183ps/inch for internal traces and 170ps/inch for surface traces. Thus, a driver generating a control signal with a minimum transition time of 1ns must be connected to the converter pin through a trace shorter than 2.5 inches. This problem becomes particularly difficult when shared control lines are used and multiple reflections may occur. The solution is to carefully terminate all transmission lines close to their characteristic impedance.

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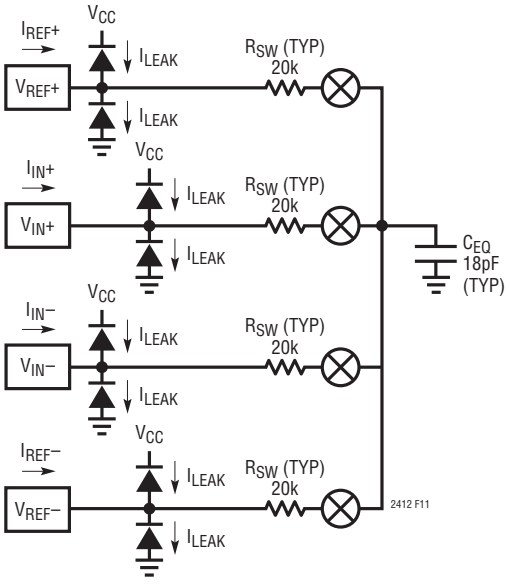
Parallel termination near the LTC2412 pin will eliminate this problem but will increase the driver power dissipation. A series resistor between 27Ω and 56Ω placed near the driver or near the LTC2412 pin will also eliminate this problem without additional power dissipation. The actual resistor value depends upon the trace impedance and connection topology.

An alternate solution is to reduce the edge rate of the control signals. It should be noted that using very slow edges will increase the converter power supply current during the transition time. The multiple ground pins used in this package configuration, as well as the differential input and reference architecture, reduce substantially the converter's sensitivity to ground currents.

Particular attention must be given to the connection of the F_O signal when the LTC2412 is used with an external conversion clock. This clock is active during the conversion time and the normal mode rejection provided by the internal digital filter is not very high at this frequency. A normal mode signal of this frequency at the converter reference terminals may result into DC gain and INL errors. A normal mode signal of this frequency at the converter input terminals may result into a DC offset error. Such perturbations may occur due to asymmetric capacitive coupling between the F_O signal trace and the converter input and/or reference connection traces. An immediate solution is to maintain maximum possible separation between the F_O signal trace and the input/reference signals. When the F_O signal is parallel terminated near the converter, substantial AC current is flowing in the loop formed by the F_O connection trace, the termination and the ground return path. Thus, perturbation signals may be inductively coupled into the converter input and/or reference. In this situation, the user must reduce to a minimum the loop area for the F_O signal as well as the loop area for the differential input and reference connections.

Driving the Input and Reference

The input and reference pins of the LTC2412 converter are directly connected to a network of sampling capacitors. Depending upon the relation between the differential input voltage and the differential reference voltage, these capacitors are switching between these four pins transferring small amounts of charge in the process. A simplified equivalent circuit is shown in Figure 11, where IN^+ and IN^- refer to the selected differential channel and the unselected channel is omitted for simplicity.



SWITCHING FREQUENCY
f_{SW} = 76800Hz INTERNAL OSCILLATOR (F_O = LOW OR HIGH)
$f_{SW} = 0.5 \bullet f_{EOSC}$ EXTERNAL OSCILLATOR

$$I(IN^+)_{AVG} = \frac{V_{IN} + V_{INCM} - V_{REFCM}}{0.5 \bullet R_{EQ}}$$

$$I(IN^-)_{AVG} = \frac{-V_{IN} + V_{INCM} - V_{REFCM}}{0.5 \bullet R_{EQ}}$$

$$I(REF^+)_{AVG} = \frac{1.5 \bullet V_{REF} - V_{INCM} + V_{REFCM}}{0.5 \bullet R_{EQ}} - \frac{V_{IN}^2}{V_{REF} \bullet R_{EQ}}$$

$$I(REF^-)_{AVG} = \frac{-1.5 \bullet V_{REF} - V_{INCM} + V_{REFCM}}{0.5 \bullet R_{EQ}} + \frac{V_{IN}^2}{V_{REF} \bullet R_{EQ}}$$

where:

$$V_{REF} = REF^+ - REF^-$$

$$V_{REFCM} = \left(\frac{REF^+ + REF^-}{2}\right)$$

$$V_{IN} = IN^+ - IN^-$$

$$V_{INCM} = \left(\frac{IN^+ - IN^-}{2}\right)$$

R_{EQ} = 3.61MΩ INTERNAL OSCILLATOR 60Hz Notch (F_O = LOW)
R_{EQ} = 4.32MΩ INTERNAL OSCILLATOR 50Hz Notch (F_O = HIGH)
$R_{EQ} = \left(0.555 \bullet 10^{12}\right) / f_{EOSC}$ EXTERNAL OSCILLATOR

Figure 11. LTC2412 Equivalent Analog Input Circuit

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For a simple approximation, the source impedance RS driving an analog input pin (IN^+, IN^-, REF^+ or REF^-) can be considered to form, together with R_{SW} and C_{EQ} (see Figure 11), a first order passive network with a time constant $\tau = (R_S + R_{SW}) \bullet C_{EQ}$. The converter is able to sample the input signal with better than 1ppm accuracy if the sampling period is at least 14 times greater than the input circuit time constant τ. The sampling process on the four input analog pins is quasi-independent so each time constant should be considered by itself and, under worst-case circumstances, the errors may add.

When using the internal oscillator (F_O = LOW or HIGH), the LTC2412's front-end switched-capacitor network is clocked at 76800Hz corresponding to a 13µs sampling period. Thus, for settling errors of less than 1ppm, the driving source impedance should be chosen such that $\tau \leq 13\mu s/14 = 920ns$. When an external oscillator of frequency f_{EOSC} is used, the sampling period is $2/f_{EOSC}$ and, for a settling error of less than 1ppm, $\tau \leq 0.14/f_{EOSC}$.

Input Current

If complete settling occurs on the input, conversion results will be unaffected by the dynamic input current. An incomplete settling of the input signal sampling process may result in gain and offset errors, but it will not degrade the INL performance of the converter. Figure 11 shows the mathematical expressions for the average bias currents flowing through the IN^+ and IN^- pins as a result of the sampling charge transfers when integrated over a substantial time period (longer than 64 internal clock cycles).

The effect of this input dynamic current can be analyzed using the test circuit of Figure 12. The C_{PAR} capacitor includes the LTC2412 pin capacitance (5pF typical) plus the capacitance of the test fixture used to obtain the results shown in Figures 13 and 14. A careful implementation can bring the total input capacitance ($C_{IN} + C_{PAR}$) closer to 5pF thus achieving better performance than the one predicted by Figures 13 and 14. For simplicity, two distinct situations can be considered.

For relatively small values of input capacitance (C_{IN} < 0.01µF), the voltage on the sampling capacitor settles almost completely and relatively large values for the source impedance result in only small errors. Such values for C_{IN} will deteriorate the converter offset and gain performance without significant benefits of signal filtering and the user is advised to avoid them. Nevertheless, when small values of C_{IN} are unavoidably present as parasitics of input

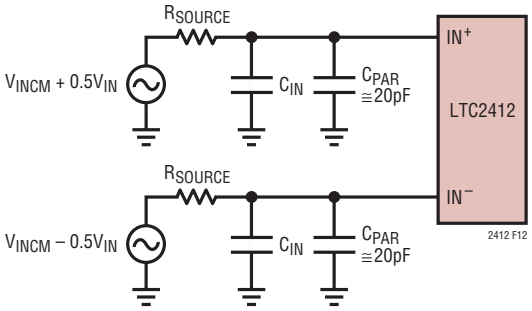

Figure 12. An RC Network at IN^+ and IN^-

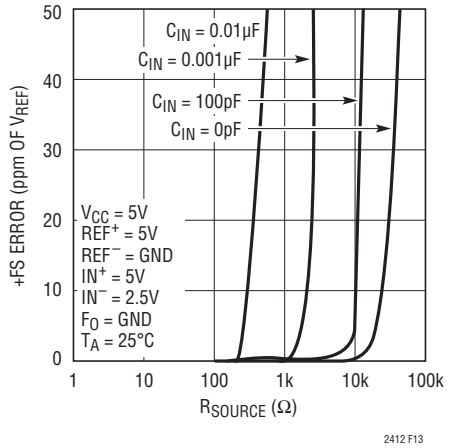

Figure 13. +FS Error vs R_{SOURCE} at IN^+ or IN (Small C_{IN})

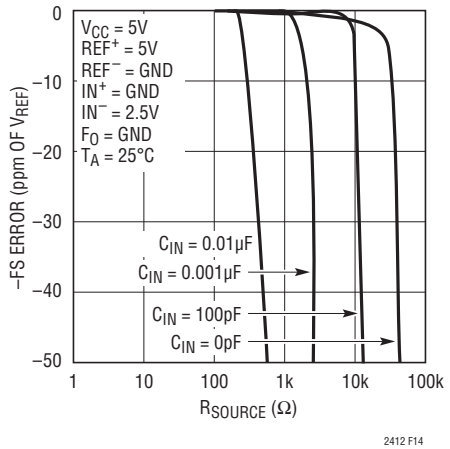

Figure 14. –FS Error vs R_{SOURCE} at IN^+ or IN^- (Small C_{IN})

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multiplexers, wires, connectors or sensors, the LTC2412 can maintain its exceptional accuracy while operating with relative large values of source resistance as shown in Figures 13 and 14. These measured results may be slightly different from the first order approximation suggested earlier because they include the effect of the actual second order input network together with the nonlinear settling process of the input amplifiers. For small C_{IN} values, the settling on IN^+ and IN^- occurs almost independently and there is little benefit in trying to match the source impedance for the two pins.

Larger values of input capacitors (C_{IN} > 0.01µF) may be required in certain configurations for anti-aliasing or general input signal filtering. Such capacitors will average the input sampling charge and the external source resistance will see a quasi constant input differential impedance. When F_O = LOW (internal oscillator and 60Hz notch), the typical differential input resistance is 1.8MΩ which will generate a gain error of approximately 0.28ppm at full-scale for each ohm of source resistance driving IN^+ or IN. When F_O = HIGH (internal oscillator and 50Hz notch), the typical differential input resistance is 2.16MΩ which will generate a gain error of approximately 0.23ppm at full-scale for each ohm of source resistance driving IN^+ or IN. When F_O is driven by an external oscillator with a frequency f_{EOSC} (external conversion clock operation), the typical differential input resistance is $0.28 \bullet 10^{12}/f_{EOSC}\Omega$ and each ohm of source resistance driving IN^+ or IN^- will result in $1.78 \bullet 10^{-6} \bullet f_{EOSC}$ppm gain error at full-scale. The effect of the source resistance on the two input pins is additive with respect to this gain error. The typical +FS and –FS errors as a function of the sum of the source resistance seen by IN^+ and IN^- for large values of C_{IN} are shown in Figures 15 and 16.

In addition to this gain error, an offset error term may also appear. The offset error is proportional with the mismatch between the source impedance driving the two input pins IN^+ and IN^- and with the difference between the input and reference common mode voltages. While the input drive circuit nonzero source impedance combined with the converter average input current will not degrade the INL performance, indirect distortion may result from the modulation of the offset error by the common mode component of the input signal. Thus, when using large

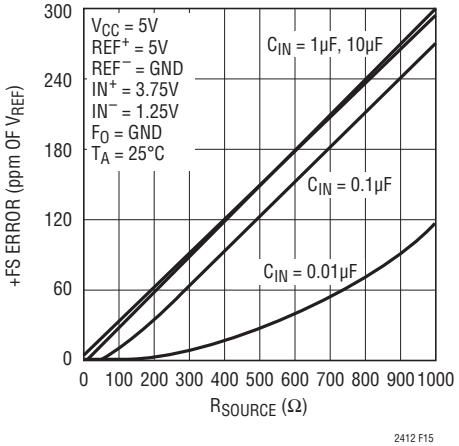

Figure 15. +FS Error vs R_{SOURCE} at IN^+ or IN^- (Large C_{IN})

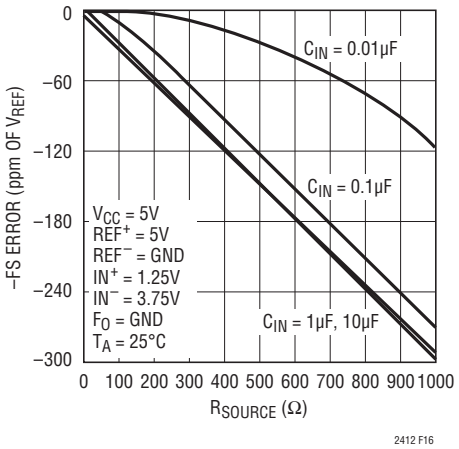

Figure 16. –FS Error vs R_{SOURCE} at IN^+ or IN^- (Large C_{IN})

C_{IN} capacitor values, it is advisable to carefully match the source impedance seen by the IN^+ and IN^- pins. When F_O = LOW (internal oscillator and 60Hz notch), every 1Ω mismatch in source impedance transforms a full-scale common mode input signal into a differential mode input signal of 0.28ppm. When F_O = HIGH (internal oscillator and 50Hz notch), every 1Ω mismatch in source impedance transforms a full-scale common mode input signal into a differential mode input signal of 0.23ppm. When F_O is driven by an external oscillator with a frequency f_{EOSC}, every 1Ω mismatch in source impedance transforms a full-scale common mode input signal into a differential mode input signal of 1.78 • 10–6 • f_{EOSC}ppm. Figure 17 shows the typical offset error due to input common mode voltage for

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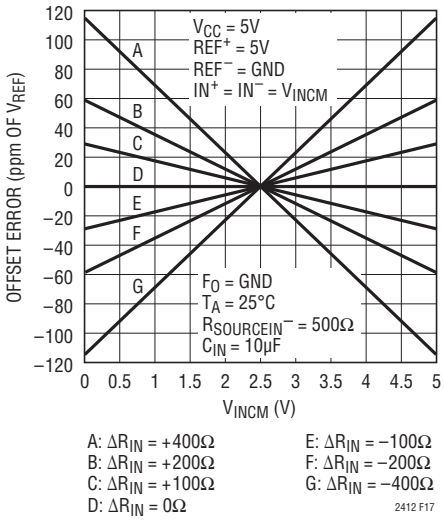

Figure 17. Offset Error vs Common Mode Voltage (V_{INCM} = IN^+ = IN^-) and Input Source Resistance Imbalance (ΔR_{IN} = $R_{SOURCEIN}^+$ – $R_{SOURCEIN}^-$) for Large C_{IN} Values (C_{IN} ≥ 1µF)

various values of source resistance imbalance between the IN^+ and IN^- pins when large C_{IN} values are used.

If possible, it is desirable to operate with the input signal common mode voltage very close to the reference signal common mode voltage as is the case in the ratiometric measurement of a symmetric bridge. This configuration eliminates the offset error caused by mismatched source impedances.

The magnitude of the dynamic input current depends upon the size of the very stable internal sampling capacitors and upon the accuracy of the converter sampling clock. The accuracy of the internal clock over the entire temperature and power supply range is typical better than 0.5%. Such a specification can also be easily achieved by an external clock. When relatively stable resistors (50ppm/°C) are used for the external source impedance seen by IN^+ and IN^-, the expected drift of the dynamic current, offset and gain errors will be insignificant (about 1% of their respective values over the entire temperature and voltage range). Even for the most stringent applications, a one-time calibration operation may be sufficient.

In addition to the input sampling charge, the input ESD protection diodes have a temperature dependent leakage current. This current, nominally 1nA (±10nA max), results in a small offset shift. A 100Ω source resistance will create a 0.1µV typical and 1µV maximum offset voltage.

Reference Current

In a similar fashion, the LTC2412 samples the differential reference pins REF^+ and REF^- transferring small amount of charge to and from the external driving circuits thus producing a dynamic reference current. This current does not change the converter offset, but it may degrade the gain and INL performance. The effect of this current can be analyzed in the same two distinct situations.

For relatively small values of the external reference capacitors (C_{REF} < 0.01µF), the voltage on the sampling capacitor settles almost completely and relatively large values for the source impedance result in only small errors. Such values for C_{REF} will deteriorate the converter offset and gain performance without significant benefits of reference filtering and the user is advised to avoid them.

Larger values of reference capacitors (C_{REF} > 0.01µF) may be required as reference filters in certain configurations. Such capacitors will average the reference sampling charge and the external source resistance will see a quasi constant reference differential impedance. When F_O = LOW (internal oscillator and 60Hz notch), the typical differential reference resistance is 1.3MΩ which will generate a gain error of approximately 0.38ppm at full-scale for each ohm of source resistance driving REF^+ or REF^-. When F_O = HIGH (internal oscillator and 50Hz notch), the typical differential reference resistance is 1.56MΩ which will generate a gain error of approximately 0.32ppm at full-scale for each ohm of source resistance driving REF^+ or REF^-. When F_O is driven by an external oscillator with a frequency f_{EOSC} (external conversion clock operation), the typical differential reference resistance is $0.20 \cdot 10^{12}/f_{EOSC}\Omega$ and each ohm of source resistance driving REF^+ or REF^- will result in $2.47 \cdot 10^{-6} \cdot f_{EOSC}$ppm gain error at full-scale. The effect of the source resistance on the two reference pins is additive with respect to this gain error. The typical $^+$FS and $^-$FS errors for various combinations of source resistance seen by the REF^+ and REF^- pins and external capacitance C_{REF} connected to these pins are shown in Figures 18, 19, 20 and 21.

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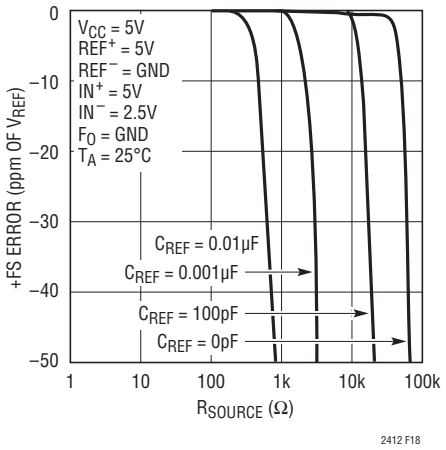

Figure 18. +FS Error vs R_{SOURCE} at REF^+ or REF^- (Small C_{IN})

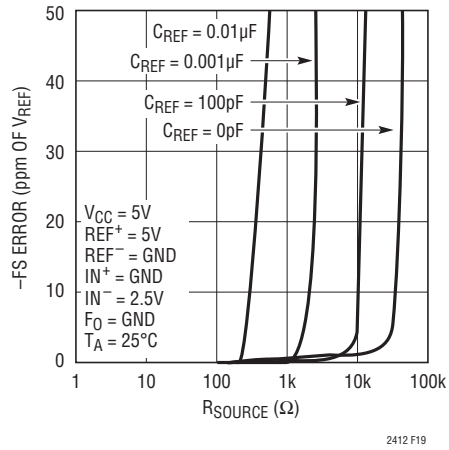

Figure 19. –FS Error vs R_{SOURCE} at REF^+ or REF^- (Small C_{IN})

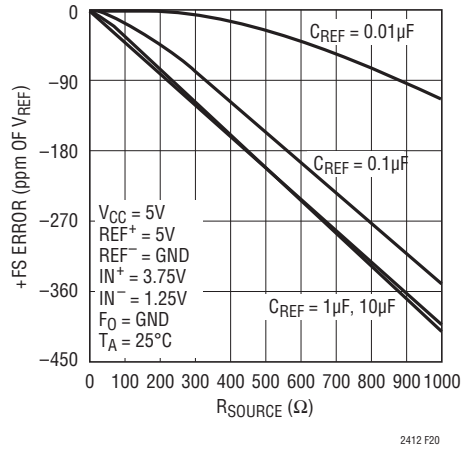

Figure 20. +FS Error vs R_{SOURCE} at REF^+ and REF^- (Large C_{REF})

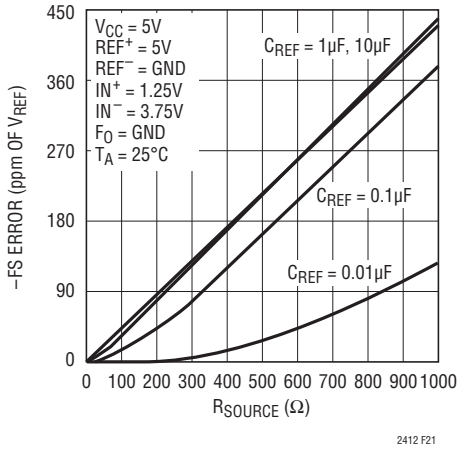

Figure 21. –FS Error vs R_{SOURCE} at REF^+ and REF^- (Large C_{REF})

In addition to this gain error, the converter INL performance is degraded by the reference source impedance. When F_O = LOW (internal oscillator and 60Hz notch), every 100Ω of source resistance driving REF^+ or REF^- translates into about 1.34ppm additional INL error. When F_O = HIGH (internal oscillator and 50Hz notch), every 100Ω of source resistance driving REF^+ or REF^- translates into about 1.1ppm additional INL error. When F_O is driven by an external oscillator with a frequency f_{EOSC}, every 100Ω of source resistance driving REF^+ or REF^- translates into about $8.73 \cdot 10^{-6} \cdot f_{EOSC}$ppm additional INL error. Figure 22 shows the typical INL error due to the source resistance driving the REF^+ or REF^- pins when large C_{REF} values are used. The effect of the source resistance on the two reference pins is additive with respect to this INL error. In general, matching of source impedance for the REF^+ and REF^- pins does not help the gain or the INL error. The user is thus advised to minimize the combined source impedance driving the REF^+ and REF^- pins rather than to try to match it.

The magnitude of the dynamic reference current depends upon the size of the very stable internal sampling capacitors and upon the accuracy of the converter sampling clock. The accuracy of the internal clock over the entire temperature and power supply range is typical better than 0.5%. Such a specification can also be easily achieved by an external clock. When relatively stable resistors (50ppm/°C) are

APPLICATIONS INFORMATION

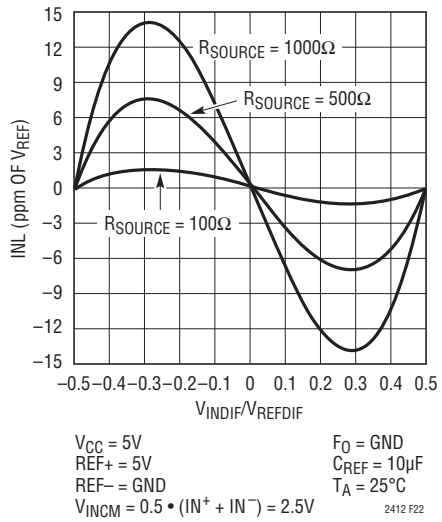

Figure 22. INL vs Differential Input Voltage (V_{IN} = IN^+ – IN^-) and Reference Source Resistance (R_{SOURCE} at REF^+ and REF^- for Large C_{REF} Values (C_{REF} ≥ 1µF)

used for the external source impedance seen by REF^+ and REF^-, the expected drift of the dynamic current gain error will be insignificant (about 1% of its value over the entire temperature and voltage range). Even for the most stringent applications a one-time calibration operation may be sufficient.

In addition to the reference sampling charge, the reference pins ESD protection diodes have a temperature dependent leakage current. This leakage current, nominally 1nA (±10nA max), results in a small gain error. A 100Ω source resistance will create a 0.05µV typical and 0.5µV maximum full-scale error.

Output Data Rate

When using its internal oscillator, the LTC2412 can produce up to 7.5 readings per second with a notch frequency of 60Hz (F_O = LOW) and 6.25 readings per second with a notch frequency of 50Hz (F_O = HIGH). The actual output data rate will depend upon the length of the sleep and data output phases which are controlled by the user and which can be made insignificantly short. When operated with an external conversion clock (F_O connected to an external oscillator), the LTC2412 output data rate can be increased as desired. The duration of the conversion phase is 20510/f_{EOSC}. If f_{EOSC} = 153600Hz, the converter behaves as if the internal oscillator is used and the notch is set at 60Hz. There is no significant difference in the LTC2412 performance between these two operation modes.

An increase in f_{EOSC} over the nominal 153600Hz will translate into a proportional increase in the maximum output data rate. This substantial advantage is nevertheless accompanied by three potential effects, which must be carefully considered.

First, a change in f_{EOSC} will result in a proportional change in the internal notch position and in a reduction of the converter differential mode rejection at the power line frequency. In many applications, the subsequent performance degradation can be substantially reduced by relying upon the LTC2412's exceptional common mode rejection and by carefully eliminating common mode to differential mode conversion sources in the input circuit. The user should avoid single-ended input filters and should maintain a very high degree of matching and symmetry in the circuits driving the IN^+ and IN^- pins.

Second, the increase in clock frequency will increase proportionally the amount of sampling charge transferred through the input and the reference pins. If large external input and/or reference capacitors (C_{IN}, C_{REF}) are used, the previous section provides formulae for evaluating the effect of the source resistance upon the converter performance for any value of f_{EOSC}. If small external input and/or reference capacitors (C_{IN}, C_{REF}) are used, the effect of the external source resistance upon the LTC2412 typical performance can be inferred from Figures 13, 14, 18 and 19 in which the horizontal axis is scaled by 153600/f_{EOSC}.

Third, an increase in the frequency of the external oscillator above 460800Hz (a more than 3× increase in the output data rate) will start to decrease the effectiveness of the internal auto-calibration circuits. This will result in a progressive degradation in the converter accuracy and linearity. Typical measured performance curves for output data rates up to 25 readings per second are shown in Figures 23, 24, 25, 26, 27, 28, 29 and 30. In order to obtain the highest possible level of accuracy from this converter at output data rates above 7.5 readings per second, the user is advised to maximize the power supply voltage used and to limit the maximum ambient operating temperature. In certain circumstances, a reduction of the differential reference voltage may be beneficial.

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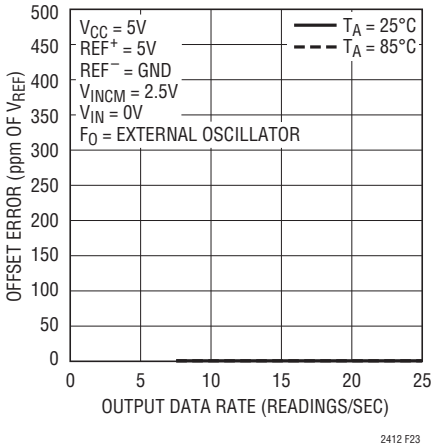

Figure 23. Offset Error vs Output Data Rate and Temperature

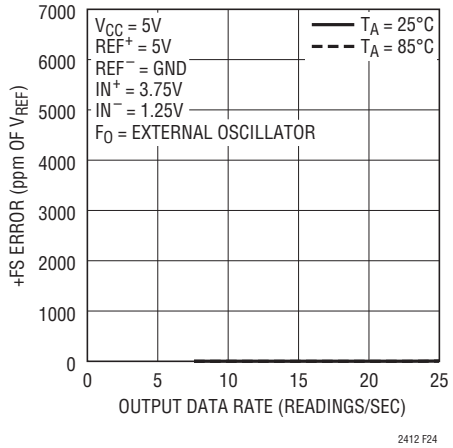

Figure 24. +FS Error vs Output Data Rate and Temperature

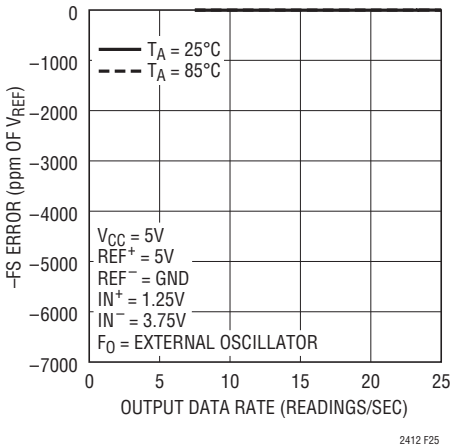

Figure 25. –FS Error vs Output Data Rate and Temperature

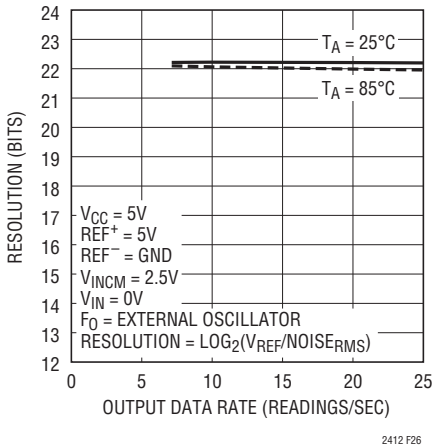

Figure 26. Resolution ($Noise_{RMS}$ ≤ 1LSB) vs Output Data Rate and Temperature

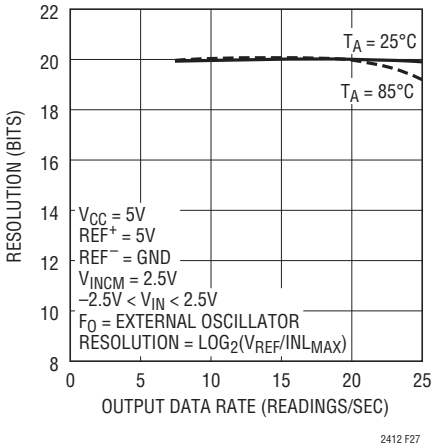

Figure 27. Resolution (INL_{MAX} ≤ 1LSB) vs Output Data Rate and Temperature

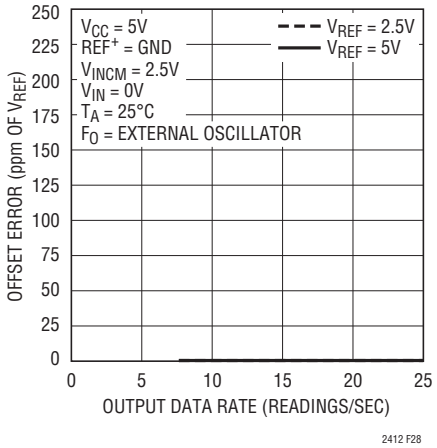

Figure 28. Offset Error vs Output Data Rate and Reference Voltage

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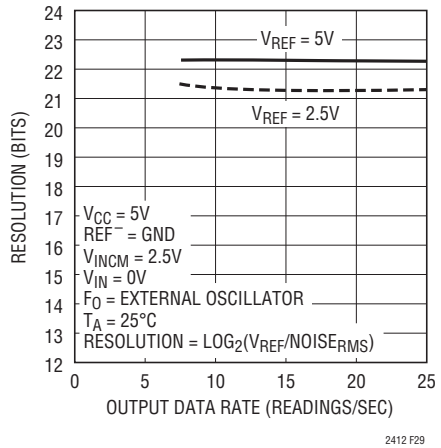

Figure 29. Resolution ($Noise_{RMS}$ ≤ 1LSB) vs Output Data Rate and Reference Voltage

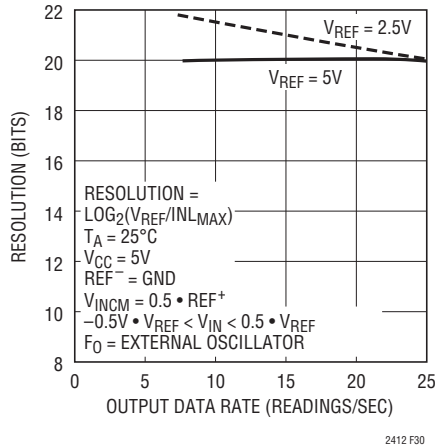

Figure 30. Resolution (INL_{MAX} ≤ 1LSB) vs Output Data Rate and Reference Voltage

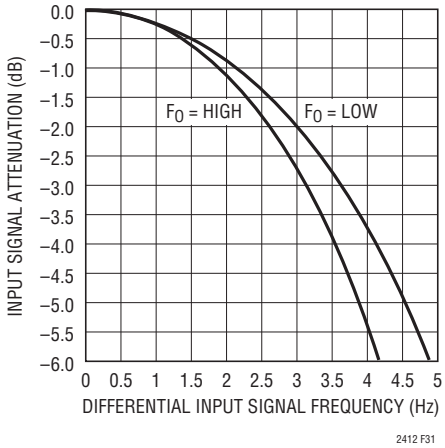

Figure 31. Input Signal Bandwidth Using the Internal Oscillator

Input Bandwidth

The combined effect of the internal Sinc^4 digital filter and of the analog and digital auto-calibration circuits determines the LTC2412 input bandwidth. When the internal oscillator is used with the notch set at 60Hz (F_O = LOW), the 3dB input bandwidth is 3.63Hz. When the internal oscillator is used with the notch set at 50Hz (F_O = HIGH), the 3dB input bandwidth is 3.02Hz. If an external conversion clock generator of frequency f_{EOSC} is connected to the F_O pin, the 3dB input bandwidth is $0.236 \cdot 10^{-6} \cdot f_{EOSC}$.

Due to the complex filtering and calibration algorithms utilized, the converter input bandwidth is not modeled very accurately by a first order filter with the pole located at the 3dB frequency. When the internal oscillator is used, the shape of the LTC2412 input bandwidth is shown in Figure 31 for F_O = LOW and F_O = HIGH. When an external oscillator of frequency f_{EOSC} is used, the shape of the LTC2412 input bandwidth can be derived from Figure 31, F_O = LOW curve in which the horizontal axis is scaled by $f_{EOSC}/153600$.

The conversion noise (800nV$_{RMS}$ typical for V_{REF} = 5V) can be modeled by a white noise source connected to a noise free converter. The noise spectral density is 62.75nV/$\sqrt{Hz}$ for an infinite bandwidth source and 86.1nV/$\sqrt{Hz}$ for a single 0.5MHz pole source. From these numbers, it is clear that particular attention must be given to the design of external amplification circuits. Such circuits face the simultaneous requirements of very low bandwidth (just a few Hz) in order to reduce the output referred noise and relatively high bandwidth (at least 500kHz) necessary to drive the input switched-capacitor network. A possible solution is a high gain, low bandwidth amplifier stage followed by a high bandwidth unity-gain buffer.

When external amplifiers are driving the LTC2412, the ADC input referred system noise calculation can be simplified by Figure 32. The noise of an amplifier driving the LTC2412 input pin can be modeled as a band limited white noise source. Its bandwidth can be approximated by the bandwidth of a single pole lowpass filter with a corner frequency f_i. The amplifier noise spectral density is n_i. From Figure 32, using f_i as the x-axis selector, we can find on the y-axis the noise equivalent bandwidth $freq_i$

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of the input driving amplifier. This bandwidth includes the band limiting effects of the ADC internal calibration and filtering. The noise of the driving amplifier referred to the converter input and including all these effects can be calculated as $N = n_i \bullet \sqrt{freq_i}$. The total system noise (referred to the LTC2412 input) can now be obtained by summing as square root of sum of squares the three ADC input referred noise sources: the LTC2412 internal noise (800nV), the noise of the IN^+ driving amplifier and the noise of the IN^- driving amplifier.

If the F_O pin is driven by an external oscillator of frequency f_{EOSC}, Figure 32 can still be used for noise calculation if the x-axis is scaled by $f_{EOSC}/153600$. For large values of the ratio $f_{EOSC}/153600$, the Figure 32 plot accuracy begins to decrease, but in the same time the LTC2412 noise floor rises and the noise contribution of the driving amplifiers lose significance.

Normal Mode Rejection and Anti-Aliasing

One of the advantages delta-sigma ADCs offer over conventional ADCs is on-chip digital filtering. Combined with a large oversampling ratio, the LTC2412 significantly simplifies anti-aliasing filter requirements.

The $Sinc^4$ digital filter provides greater than 120dB normal mode rejection at all frequencies except DC and integer multiples of the modulator sampling frequency (f_S). The LTC2412's auto-calibration circuits further simplify the anti-aliasing requirements by additional normal mode signal filtering both in the analog and digital domain. Independent of the operating mode, $f_S = 256 \bullet f_N = 2048 \bullet f_{OUTMAX}$ where f_N in the notch frequency and f_{OUTMAX} is the maximum output data rate. In the internal oscillator mode with a 50Hz notch setting, f_S = 12800Hz and with a 60Hz notch setting f_S = 15360Hz. In the external oscillator mode, $f_S = f_{EOSC}/10$.

The combined normal mode rejection performance is shown in Figure 33 for the internal oscillator with 50Hz notch setting (F_O = HIGH) and in Figure 34 for the internal oscillator with 60Hz notch setting (F_O = LOW) and for the external oscillator mode. The regions of low rejection occurring at integer multiples of f_S have a very narrow bandwidth. Magnified details of the normal mode rejection curves are shown in Figure 35 (rejection near DC) and

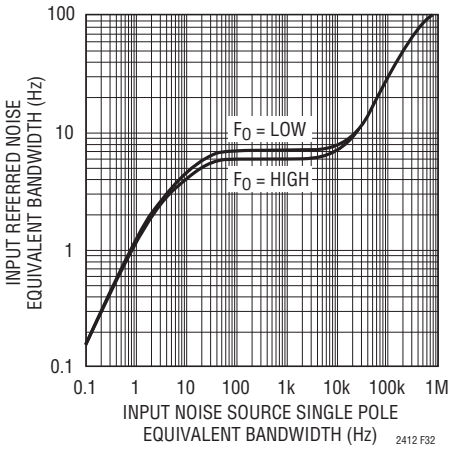

Figure 32. Input Referred Noise Equivalent Bandwidth of an Input Connected White Noise Source

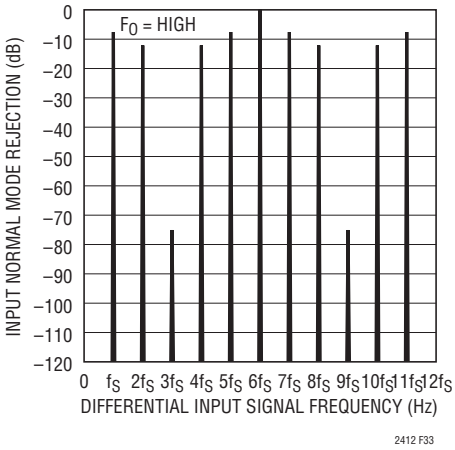

Figure 33. Input Normal Mode Rejection, Internal Oscillator and 50Hz Notch

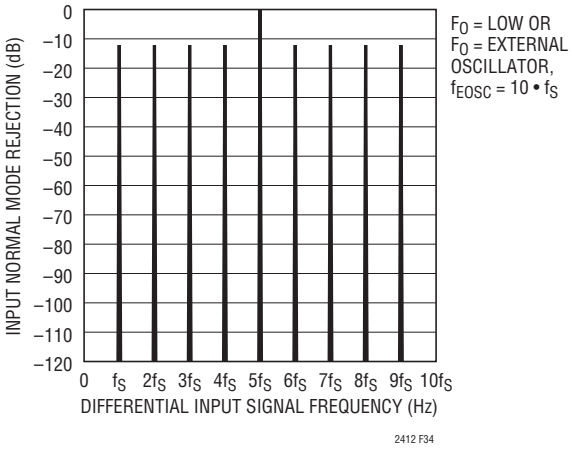

Figure 34. Input Normal Mode Rejection, Internal Oscillator and 60Hz Notch or External Oscillator

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Figure 36 (rejection at $f_S = 256f_N$) where f_N represents the notch frequency. These curves have been derived for the external oscillator mode but they can be used in all operating modes by appropriately selecting the f_N value.

The user can expect to achieve in practice this level of performance using the internal oscillator as it is demonstrated by Figures 37 and 38. Typical measured values of the normal mode rejection of the LTC2412 operating with an internal oscillator and a 60Hz notch setting are shown in Figure 37 superimposed over the theoretical calculated curve. Similarly, typical measured values of the normal mode rejection of the LTC2412 operating with an internal oscillator and a 50Hz notch setting are shown in Figure 38 superimposed over the theoretical calculated curve.

As a result of these remarkable normal mode specifications, minimal (if any) anti-alias filtering is required in front of the LTC2412. If passive RC components are placed in front of the LTC2412, the input dynamic current should be considered (see Input Current section). In cases where large effective RC time constants are used, an external buffer amplifier may be required to minimize the effects of dynamic input current.

Traditional high order delta-sigma modulators, while providing very good linearity and resolution, suffer from potential instabilities at large input signal levels. The proprietary architecture used for the LTC2412 third order modulator resolves this problem and guarantees a predictable stable behavior at input signal levels of up to 150% of full-scale.

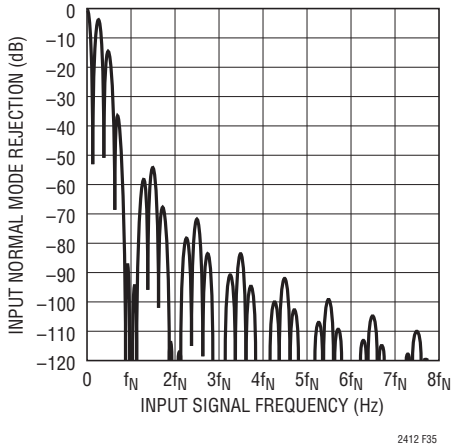


Figure 35. Input Normal Mode Rejection

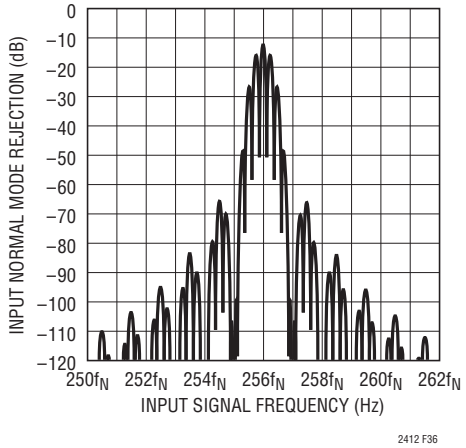


Figure 36. Input Normal Mode Rejection

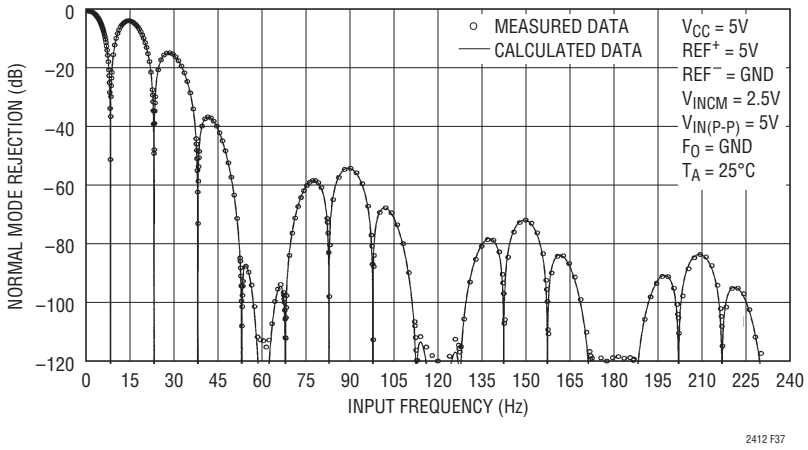


Figure 37. Input Normal Mode Rejection vs Input Frequency with Input Perturbation of 100% Full-Scale (60Hz Notch)

APPLICATIONS INFORMATION

In many industrial applications, it is not uncommon to have to measure microvolt level signals superimposed over volt level perturbations and LTC2412 is eminently suited for such tasks. When the perturbation is differential, the specification of interest is the normal mode rejection for large input signal levels. With a reference voltage V_{REF} = 5V, the LTC2412 has a full-scale differential input range of 5V peak-to-peak. Figures 39 and 40 show measurement results for the LTC2412 normal mode rejection ratio with a 7.5V peak-to-peak (150% of full-scale) input signal superimposed over the more traditional normal mode rejection ratio results obtained with a 5V peak-to-peak (full-scale) input signal. In Figure 39, the LTC2412 uses the internal oscillator with the notch set at 60Hz (F_O = LOW) and in Figure 40 it uses the internal oscillator with the notch set at 50Hz (F_O = HIGH). It is clear that the LTC2412 rejection performance is maintained with no compromises in this extreme situation. When operating with large input signal levels, the user must observe that such signals do not violate the device absolute maximum ratings.

Measuring Barometric Pressure and Temperature with a Single Sensor

Figure 41 shows the LTC2412 measuring both temperature and pressure from an Intersema model MS5401-BM absolute pressure sensor. The bridge has a nominal impedance of 3.4kΩ, a temperature coefficient of resistance of 2900ppm/°C and a temperature coefficient of span of –1900ppm/°C. R1 provides first order temperature compensation of the output span by causing the bridge voltage to increase by 1900ppm/°C, offsetting the –1900ppm/°C TC of span. R1 should have a much smaller TC than that of the bridge resistance; 50ppm/°C or less is satisfactory.

In addition to compensating the bridge output span, this circuit also provides a convenient way to measure ambient temperature. Channel 1 of the LTC2412 measures the bridge excitation voltage, which has a slope of approximately 3.2mV/°C. Channel 0 measures the bridge output, which has a slope of 50mV/bar. The temperature reading can also be used for second order compensation of the pressure reading.

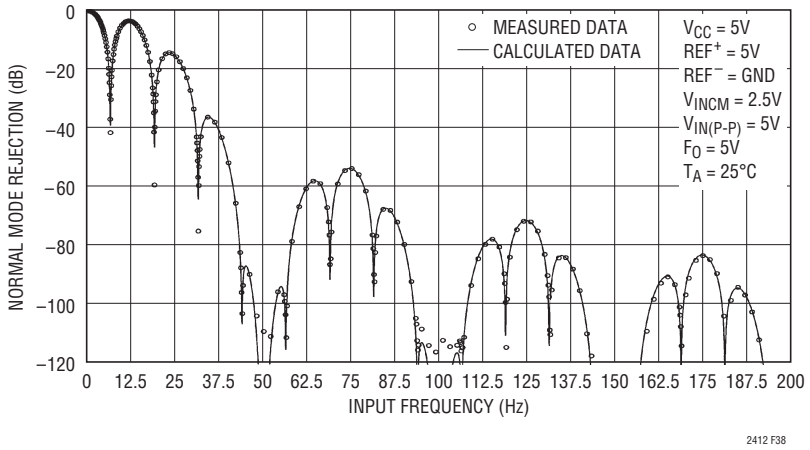


Figure 38. Input Normal Mode Rejection vs Input Frequency with Input Perturbation of 100% Full-Scale (50Hz Notch)

APPLICATIONS INFORMATION

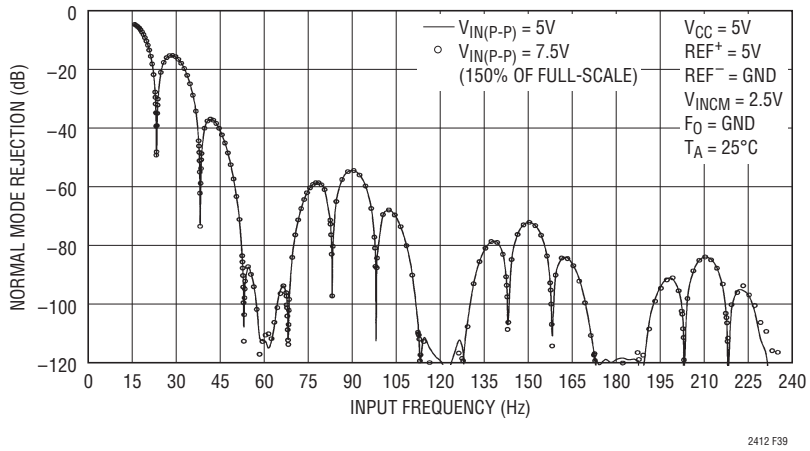


Figure 39. Measured Input Normal Mode Rejection vs Input Frequency with Input Perturbation of 150% Full-Scale (60Hz Notch)

APPLICATIONS INFORMATION

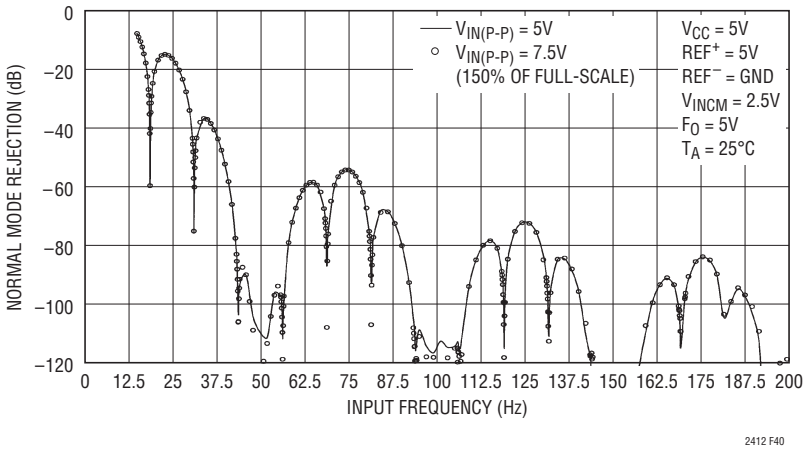
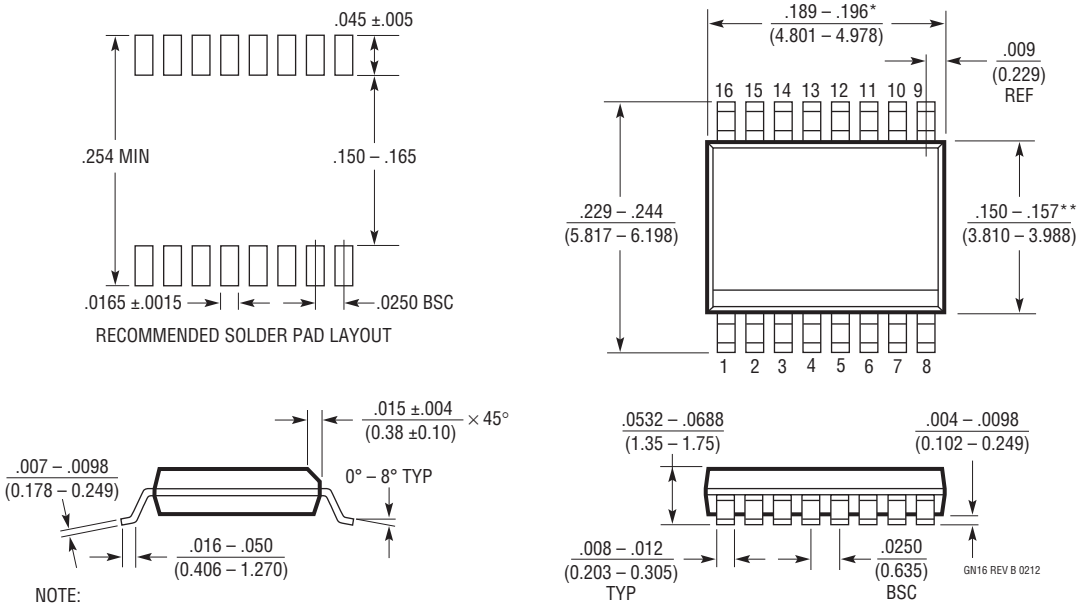


Figure 40. Measured Input Normal Mode Rejection vs Input Frequency with Input Perturbation of 150% Full-Scale (50Hz Notch)

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641 Rev B)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	08/15	Updated f_{EOSC} maximum to 500kHz and all associated information	5, 6, 7, 9, 28, 29, 30

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

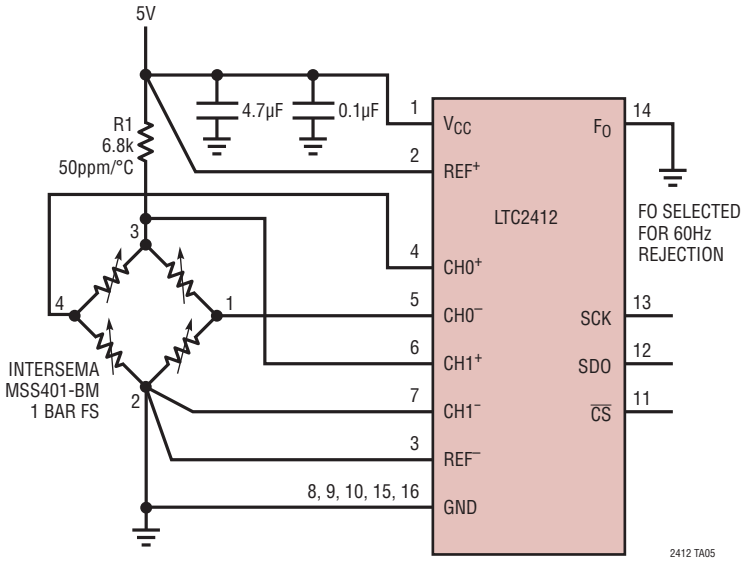


Figure 41. Measure Barometric Pressure and Temperature with a Single Sensor

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1019	Precision Bandgap Reference, 2.5V, 5V	3ppm/°C Drift, 0.05% Max
LTC1043	Dual Precision Instrumentation Switched Capacitor Building Block	Precise Charge, Balanced Switching, Low Power
LTC1050	Precision Chopper Stabilized Op Amp	No External Components 5µV Offset, 1.6µV_{P-P} Noise
LT1236A-5	Precision Bandgap Reference, 5V	0.05% Max, 5ppm/°C Drift
LT1461	Micropower Precision LDO Reference	High Accuracy 0.04% Max, 3ppm/°C Max Drift
LTC2400	24-Bit, No Latency ΔΣ ADC in SO-8	0.3ppm Noise, 4ppm INL, 10ppm Total Unadjusted Error, 200µA
LTC2401/LTC2402	1-/2-Channel, 24-Bit, No Latency ΔΣ ADC in MSOP	0.6ppm Noise, 4ppm INL, 10ppm Total Unadjusted Error, 200µA
LTC2404/LTC2408	4-/8-Channel, 24-Bit, No Latency ΔΣ ADC	0.3ppm Noise, 4ppm INL, 10ppm Total Unadjusted Error, 200µA
LTC2410	24-Bit, Fully Differential, No Latency ΔΣ ADC	0.16ppm Noise, 2ppm INL, 3ppm Total Unadjusted Error, 200µA
LTC2411	24-Bit, No Latency ΔΣ ADC in MSOP	1.45µV_{RMS} Noise, 2ppm INL
LTC2411-1	24-Bit, Simultaneous 50Hz/60Hz Rejection ΔΣ ADC	0.3ppm Noise, 2ppm INL, Pin Compatible with LTC2411
LTC2413	24-Bit, No Latency ΔΣ ADC	Simultaneous 50Hz/60Hz Rejection, 800nV_{RMS} Noise
LTC2414/LTC2418	8-/16-Channel, 24-Bit No Latency ΔΣ ADC	0.2ppm Noise, 2ppm INL, 3ppm Total Unadjusted Error, 200µA
LTC2415	24-Bit, No Latency ΔΣ ADC with 15Hz Output Rate	Pin Compatible with the LTC2410
LTC2420	20-Bit, No Latency ΔΣ ADC in SO-8	1.2ppm Noise, 8ppm INL, Pin Compatible with LTC2400
LTC2424/LTC2428	4-/8-Channel, 20-Bit, No Latency ΔΣ ADCs	1.2ppm Noise, 8ppm INL, Pin Compatible with LTC2404/LTC2408
LTC2440	High Speed, Low Noise 24-Bit ADC	4kHz Output Rate, 200nV Noise, 24.6 ENOBs

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