



**THE DATASHEET OF  
LTC2453CTS8#TRPBF**




# Ultra-Tiny, Differential, 16-Bit $\Delta\Sigma$ ADC With I<sup>2</sup>C Interface

## FEATURES

- $\pm V_{CC}$  Differential Input Range
- 16-Bit Resolution (Including Sign), No Missing Codes
- 2LSB Offset Error
- 4LSB Full-Scale Error
- 60 Conversions Per Second
- Single Conversion Settling Time for Multiplexed Applications
- Single-Cycle Operation with Auto Shutdown
- 800 $\mu$ A Supply Current
- 0.2 $\mu$ A Sleep Current
- Internal Oscillator—No External Components Required
- 2-Wire I<sup>2</sup>C Interface
- Ultra-Tiny 8-Pin 3mm  $\times$  2mm DFN and TSOT23 Packages

## APPLICATIONS

- System Monitoring
- Environmental Monitoring
- Direct Temperature Measurements
- Instrumentation
- Industrial Process Control
- Data Acquisition
- Embedded ADC Upgrades

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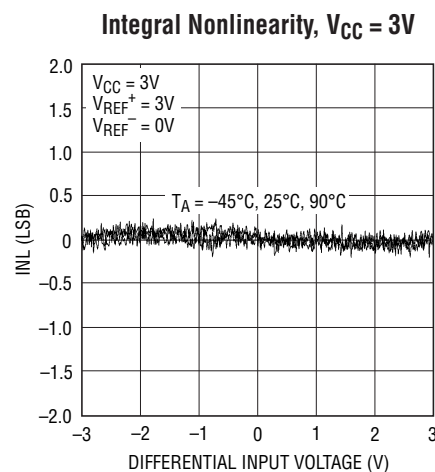
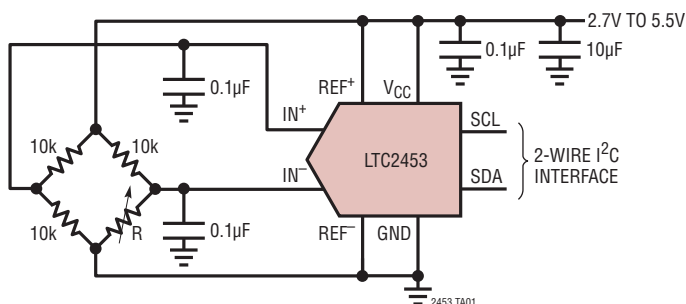
## DESCRIPTION

The LTC<sup>®</sup>2453 is an ultra-tiny, fully differential, 16-bit, analog-to-digital converter. The LTC2453 uses a single 2.7V to 5.5V supply and communicates through an I<sup>2</sup>C interface. The ADC is available in an 8-pin, 3mm  $\times$  2mm DFN package or 8-pin, 3mm  $\times$  3mm TSOT package. It includes an integrated oscillator that does not require any external components. It uses a delta-sigma modulator as a converter core and has no latency for multiplexed applications. The LTC2453 includes a proprietary input sampling scheme that reduces the average input sampling current several orders of magnitude lower than conventional delta-sigma converters. Additionally, due to its architecture, there is negligible current leakage between the input pins.

The LTC2453 can sample at 60 conversions per second, and due to the very large oversampling ratio, has extremely relaxed antialiasing requirements. The LTC2453 includes continuous internal offset and full-scale calibration algorithms which are transparent to the user, ensuring accuracy over time and over the operating temperature range. The converter has external REF<sup>+</sup> and REF<sup>-</sup> pins and the differential input voltage range can extend up to  $\pm(V_{REF}^+ - V_{REF}^-)$ .

Following a single conversion, the LTC2453 can automatically enter a sleep mode and reduce its power to less than 0.2 $\mu$ A. If the user reads the ADC once a second, the LTC2453 consumes an average of less than 50 $\mu$ W from a 2.7V supply.

## TYPICAL APPLICATION



# LTC2453

## ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage ( $V_{CC}$ ) .....  $-0.3V$  to  $6V$   
 Analog Input Voltage ( $V_{IN}^+$ ,  $V_{IN}^-$ )...  $-0.3V$  to  $(V_{CC} + 0.3V)$   
 Reference Voltage ( $V_{REF}^+$ ,  $V_{REF}^-$ )...  $-0.3V$  to  $(V_{CC} + 0.3V)$   
 Digital Voltage (SDA, SCL).....  $-0.3V$  to  $(V_{CC} + 0.3V)$

Storage Temperature Range.....  $-65^{\circ}C$  to  $150^{\circ}C$   
 Operating Temperature Range  
 LTC2453C .....  $0^{\circ}C$  to  $70^{\circ}C$   
 LTC2453I.....  $-40^{\circ}C$  to  $85^{\circ}C$

## PIN CONFIGURATION



## ORDER INFORMATION

### Lead Free Finish

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2453CDDB#TRMPBF	LTC2453CDDB#TRPBF	LDBQ	8-Lead Plastic (3mm × 2mm) DFN	$0^{\circ}C$ to $70^{\circ}C$
LTC2453IDDB#TRMPBF	LTC2453IDDB#TRPBF	LDBQ	8-Lead Plastic (3mm × 2mm) DFN	$-40^{\circ}C$ to $85^{\circ}C$
LTC2453CTS8#TRMPBF	LTC2453CTS8#TRPBF	LTDCG	8-Lead Plastic TSOT-23	$0^{\circ}C$ to $70^{\circ}C$
LTC2453ITS8#TRMPBF	LTC2453ITS8#TRPBF	LTDCG	8-Lead Plastic TSOT-23	$-40^{\circ}C$ to $85^{\circ}C$

TRM = 500 pieces. \*Temperature grades are identified by a label on the shipping container.

Consult LTC Marketing for parts specified with wider operating temperature ranges.

Consult LTC Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^{\circ}C$ . (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)	(Note 3)	●	16		Bits
Integral Nonlinearity	(Note 4)	●	2	10	LSB
Offset Error		●	2	10	LSB
Offset Error Drift			0.02		LSB/ $^{\circ}C$
Gain Error		●	0.01	0.02	% of FS
Gain Error Drift			0.02		LSB/ $^{\circ}C$
Transition Noise			1.4		$\mu V_{RMS}$
Power Supply Rejection DC			80		dB

2453fc

## ANALOG INPUTS AND REFERENCES

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
$V_{IN}^+$	Positive Input Voltage Range	●	0		$V_{CC}$	V	
$V_{IN}^-$	Negative Input Voltage Range	●	0		$V_{CC}$	V	
$V_{REF}^+$	Positive Reference Voltage Range	$V_{REF}^+ - V_{REF}^- \geq 2.5V$	●	$V_{CC} - 2.5$	$V_{CC}$	V	
$V_{REF}^-$	Negative Reference Voltage Range	$V_{REF}^+ - V_{REF}^- \geq 2.5V$	●	0	$V_{CC} - 2.5$	V	
$V_{OR}^+ + V_{UR}^+$	Overrange + Underrange Voltage, $IN^+$	$V_{REF} = 5V, V_{IN}^- = 2.5V$ (See Figure 2)		31		LSB	
$V_{OR}^- + V_{UR}^-$	Overrange + Underrange Voltage, $IN^-$	$V_{REF} = 5V, V_{IN}^+ = 2.5V$ (See Figure 2)		31		LSB	
$C_{IN}$	$IN^+, IN^-$ Sampling Capacitance			0.35		pF	
$I_{DC\_LEAK}(IN^+)$	$IN^+$ DC Leakage Current	$V_{IN} = GND$ (Note 8) $V_{IN} = V_{CC}$ (Note 8)	● ●	-10 -10	1 1	10 10	nA nA
$I_{DC\_LEAK}(IN^-)$	$IN^-$ DC Leakage Current	$V_{IN} = GND$ (Note 8) $V_{IN} = V_{CC}$ (Note 8)	● ●	-10 -10	1 1	10 10	nA nA
$I_{DC\_LEAK}(REF^+, REF^-)$	$REF^+, REF^-$ DC Leakage Current	$V_{REF} = 3V$ (Note 8)	●	-10	1	10	nA
$I_{CONV}$	Input Sampling Current (Note 5)			50		nA	

## POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{CC}$	Supply Voltage	●	2.7		5.5	V
$I_{CC}$	Supply Current Conversion Sleep	● ●		800 0.2	1200 0.6	$\mu\text{A}$ $\mu\text{A}$

## I<sup>2</sup>C INPUTS AND OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Notes 2, 7)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IH}$	High Level Input Voltage	●	$0.7V_{CC}$			V
$V_{IL}$	Low Level Input Voltage	●			$0.3V_{CC}$	V
$I_I$	Digital Input Current	●	-10		10	$\mu\text{A}$
$V_{HYS}$	Hysteresis of Schmidt Trigger Inputs	(Note 3)	●	$0.05V_{CC}$		V
$V_{OL}$	Low Level Output Voltage (SDA)	$I = 3\text{mA}$	●		0.4	V
$I_{IN}$	Input Leakage	$0.1V_{CC} \leq V_{IN} \leq 0.9V_{CC}$	●		1	$\mu\text{A}$
$C_I$	Capacitance for Each I/O Pin	●	10			pF
$C_B$	Capacitance Load for Each Bus Line	●			400	pF

## I<sup>2</sup>C TIMING CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T<sub>A</sub> = 25°C. (Notes 2, 7)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t <sub>CONV</sub>	Conversion Time	●	13	16.6	23	ms
f <sub>SCL</sub>	SCL Clock Frequency	●	0		400	kHz
t <sub>HD(SDA)</sub>	Hold Time (Repeated) START Condition	●	0.6			μs
t <sub>LOW</sub>	LOW Period of the SCL Pin	●	1.3			μs
t <sub>HIGH</sub>	HIGH Period of the SCL Pin	●	0.6			μs
t <sub>SU(STA)</sub>	Set-Up Time for a Repeated START Condition	●	0.6			μs
t <sub>HD(DAT)</sub>	Data Hold Time	●			0.9	μs
t <sub>SU(DAT)</sub>	Data Set-Up Time	●	100			ns
t <sub>r</sub>	Rise Time for SDA, SCL Signals	(Note 6) ●	20 + 0.1C <sub>B</sub>		300	ns
t <sub>f</sub>	Fall Time for SDA, SCL Signals	(Note 6) ●	20 + 0.1C <sub>B</sub>		300	ns
t <sub>SU(STO)</sub>	Set-Up Time for STOP Condition	●	0.6			μs
t <sub>BUF</sub>	Bus Free Time Between a Stop and Start Condition	●	1.3			μs
t <sub>OF</sub>	Output Fall Time V <sub>IHMIN</sub> to V <sub>ILMAX</sub>	Bus Load C <sub>B</sub> 10pF to 400pF (Note 6) ●	20 + 0.1C <sub>B</sub>		250	ns
t <sub>SP</sub>	Input Spike Suppression	●			50	ns

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All voltage values are with respect to GND. V<sub>CC</sub> = 2.7V to 5.5V unless otherwise specified.

$$V_{REF} = V_{REF^+} - V_{REF^-}, V_{REFCM} = (V_{REF^+} + V_{REF^-})/2, FS = V_{REF^+} - V_{REF^-};$$

$$V_{IN} = V_{IN^+} - V_{IN^-}, -V_{REF} \leq V_{IN} \leq V_{REF}; V_{INCM} = (V_{IN^+} + V_{IN^-})/2.$$

**Note 3:** Guaranteed by design, not subject to test.

**Note 4:** Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. Guaranteed by design and test correlation.

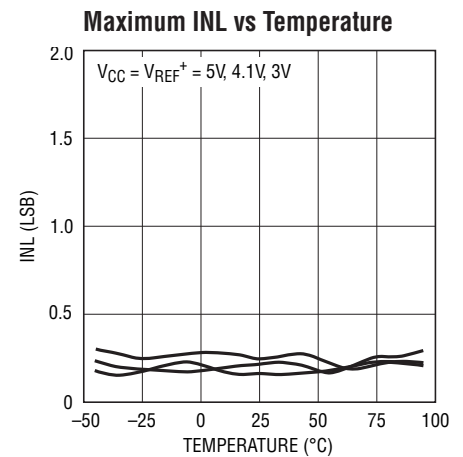
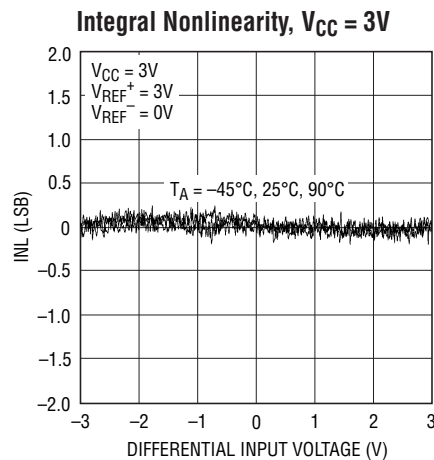
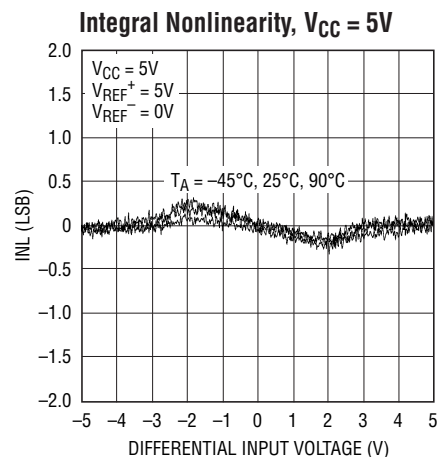
**Note 5:** Input sampling current is the average input current drawn from the input sampling network while the LTC2453 is converting.

**Note 6:** C<sub>B</sub> = capacitance of one bus line in pF.

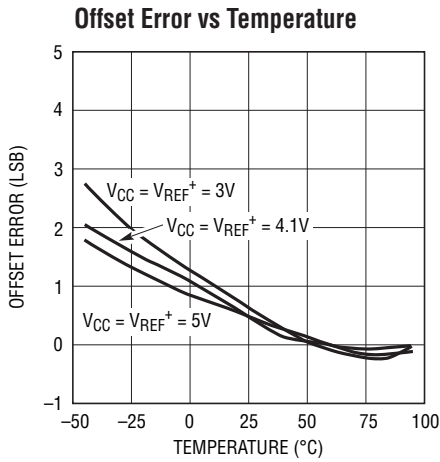
**Note 7:** All values refer to V<sub>IH(MIN)</sub> and V<sub>IL(MAX)</sub> levels.

**Note 8:** A positive current is flowing into the DUT pin.

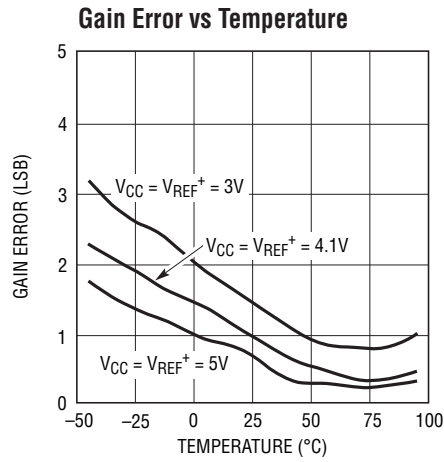
## TYPICAL PERFORMANCE CHARACTERISTICS (T<sub>A</sub> = 25°C, unless otherwise noted)



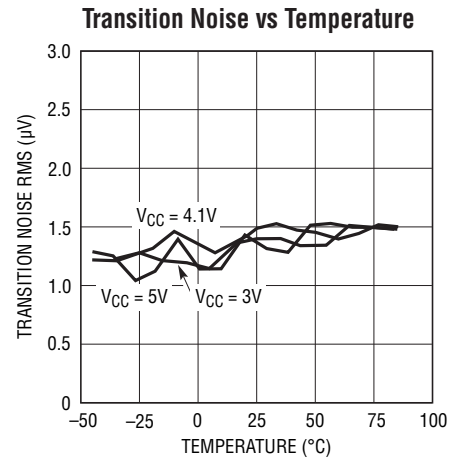
**TYPICAL PERFORMANCE CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)



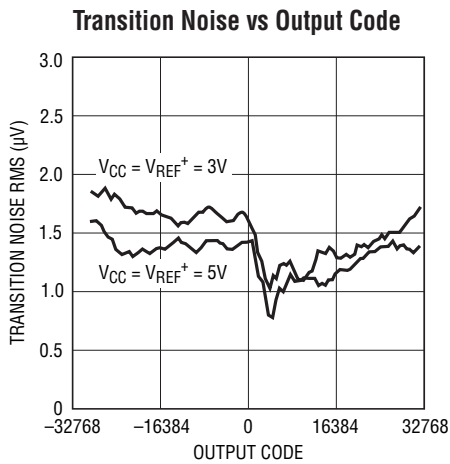
2453 G04



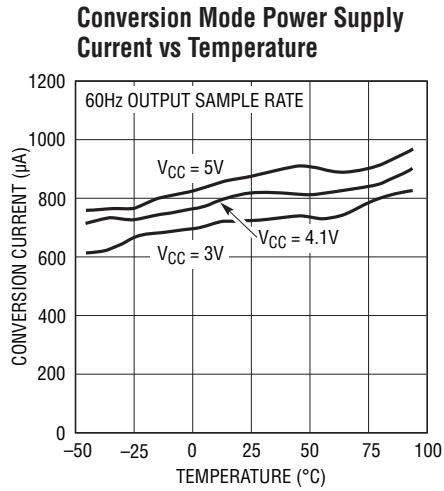
2453 G05



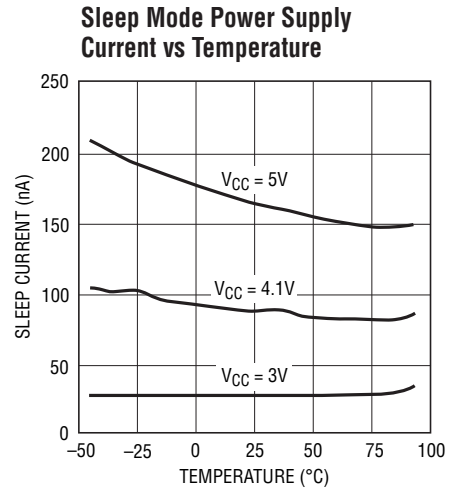
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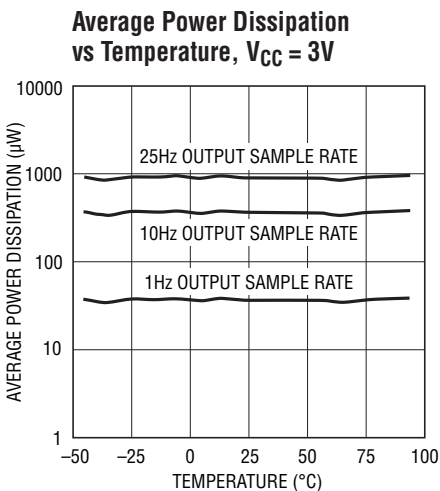
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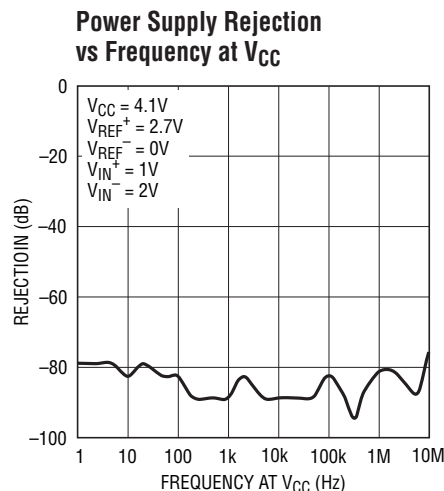
2453 G08



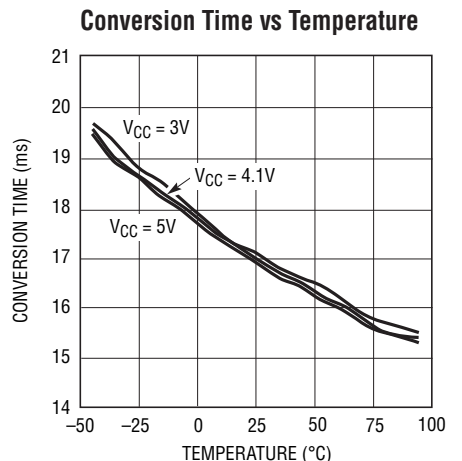
2453 G09



2453 G10



2453 G11



2453 G12

## PIN FUNCTIONS

**GND (Pin 1):** Ground. Connect to a ground plane through a low impedance connection.

**REF<sup>-</sup> (Pin 2), REF<sup>+</sup> (Pin 3):** Differential Reference Input. The voltage on these pins can have any value between GND and V<sub>CC</sub> as long as the reference positive input, REF<sup>+</sup>, remains more positive than the negative reference input, REF<sup>-</sup>, by at least 2.5V. The differential reference voltage (V<sub>REF</sub> = REF<sup>+</sup> to REF<sup>-</sup>) sets the full-scale range.

**V<sub>CC</sub> (Pin 4):** Positive Supply Voltage. Bypass to GND (Pin 1) with a 10μF capacitor in parallel with a low-series-inductance 0.1μF capacitor located as close to the part as possible.

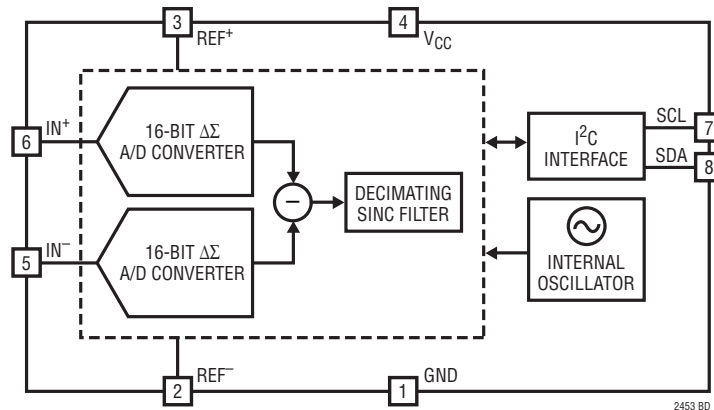
**IN<sup>-</sup> (Pin 5), IN<sup>+</sup> (Pin 6):** Differential Analog Input.

**SCL (Pin 7):** Serial Clock Input of the I<sup>2</sup>C Interface. The LTC2453 can only act as a slave and the SCL pin only accepts external serial clock. Data is shifted into the SDA pin on the rising edges of SCL and output through the SDA pin on the falling edges of SCL.

**SDA (Pin 8):** Bidirectional Serial Data Line of the I<sup>2</sup>C Interface. The conversion result is output through the SDA pin. The pin is high impedance unless the LTC2453 is in the data output mode. While the LTC2453 is in the data output mode, SDA is an open drain pull down (which requires an external 1.7k pull-up resistor to V<sub>CC</sub>).

**Exposed Pad (Pin 9, DFN Only):** Ground. Must be soldered to PCB ground.

## BLOCK DIAGRAM



## APPLICATIONS INFORMATION

### CONVERTER OPERATION

#### Converter Operation Cycle

The LTC2453 is a low-power, fully differential, delta-sigma analog-to-digital converter with an I<sup>2</sup>C interface. Its operation, as shown in Figure 1, is composed of three successive states: CONVERSION, SLEEP and DATA OUTPUT.

Initially, at power up, the LTC2453 performs a conversion. Once the conversion is complete, the device enters the sleep state. While in this sleep state, power consumption is reduced by several orders of magnitude. The part remains in the sleep state as long as it is not addressed for a read operation. The conversion result is held indefinitely in a static shift register while the part is in the sleep state.

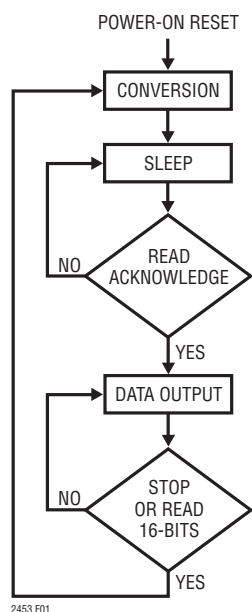


Figure 1. LTC2453 State Diagram

The device will not acknowledge an external request during the conversion state. After a conversion is finished, the device is ready to accept a read request. The LTC2453's address is hard-wired at 0010100. Once the LTC2453 is addressed for a read operation, the device begins outputting the conversion result under the control of the serial clock (SCL). There is no latency in the conversion result. The data output is 16 bits long and contains a 15-bit plus sign conversion result. Data is updated on the falling

edges of SCL, allowing the user to reliably latch data on the rising edge of SCL. A new conversion is initiated by a stop condition following a valid read operation, or by the conclusion of a complete read cycle (all 16 bits read out of the device).

#### Power-Up Sequence

When the power supply voltage ( $V_{CC}$ ) applied to the converter is below approximately 2.1V, the ADC performs a power-on reset. This feature guarantees the integrity of the conversion result.

When  $V_{CC}$  rises above this threshold, the converter generates an internal power-on reset (POR) signal for approximately 0.5ms. The POR signal clears all internal registers. Following the POR signal, the LTC2453 starts a conversion cycle and follows the succession of states described in Figure 1. The first conversion result following POR is accurate within the specifications of the device if the power supply voltage  $V_{CC}$  is restored within the operating range (2.7V to 5.5V) before the end of the POR time interval.

#### Ease of Use

The LTC2453 data output has no latency, filter settling delay or redundant results associated with the conversion cycle. There is a one-to-one correspondence between the conversion and the output data. Therefore, multiplexing multiple analog input voltages requires no special actions.

The LTC2453 performs offset calibrations every conversion. This calibration is transparent to the user and has no effect upon the cyclic operation described previously. The advantage of continuous calibration is extreme stability of the ADC performance with respect to time and temperature.

The LTC2453 includes a proprietary input sampling scheme that reduces the average input current by several orders of magnitude when compared to traditional delta-sigma architectures. This allows external filter networks to interface directly to the LTC2453. Since the average input sampling current is 50nA, an external RC lowpass filter using a 1k $\Omega$  and 0.1 $\mu$ F results in <1LSB additional error. Additionally, there is negligible leakage current between  $IN^+$  and  $IN^-$ .

## APPLICATIONS INFORMATION

### Reference Voltage Range

This converter accepts a truly differential external reference voltage. The absolute/common mode voltage range for REF<sup>+</sup> and REF<sup>-</sup> pins covers the entire operating range of the device (GND to V<sub>CC</sub>). For correct converter operation, V<sub>REF<sup>+</sup></sub> must be >(2.5V + V<sub>REF<sup>-</sup></sub>).

The LTC2453 differential reference input range is 2.5V to V<sub>CC</sub>. For the simplest operation, REF<sup>+</sup> can be shorted to V<sub>CC</sub> and REF<sup>-</sup> can be shorted to GND.

### Input Voltage Range

For most applications, V<sub>REF<sup>-</sup></sub> ≤ (V<sub>IN<sup>+</sup></sub>, V<sub>IN<sup>-</sup></sub>) ≤ V<sub>REF<sup>+</sup></sub>. Under these conditions the output code is given (see Data Format section) as 32768 • (V<sub>IN<sup>+</sup></sub> - V<sub>IN<sup>-</sup></sub>) / (V<sub>REF<sup>+</sup></sub> - V<sub>REF<sup>-</sup></sub>) + 32768. The output of the LTC2453 is clamped at a minimum value of 0 and clamped at a maximum value of 65535.

The LTC2453 includes a proprietary system that can, typically, correctly digitize each input 8LSB above V<sub>REF<sup>+</sup></sub> and below V<sub>REF<sup>-</sup></sub>, if the LTC2453's output is not clamped. As an example (Figure 2), if the user desires to measure a signal slightly below ground, the user could set V<sub>IN<sup>-</sup></sub> = V<sub>REF<sup>-</sup></sub> = GND, and V<sub>REF<sup>+</sup></sub> = 5V. If V<sub>IN<sup>+</sup></sub> = GND, the output code would be approximately 32768. If V<sub>IN<sup>+</sup></sub> = GND - 8LSB = -1.22 mV, the output code would be approximately 32760.

The total amount of overrange and underrange capability is typically 31LSB for a given device. The 31LSB total is distributed between the overrange and underrange

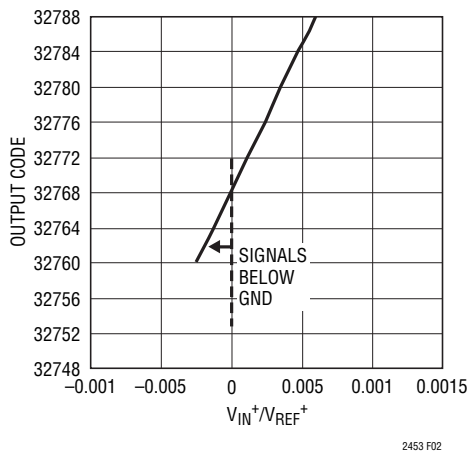


Figure 2. Output Code vs V<sub>IN<sup>+</sup></sub> with V<sub>IN<sup>-</sup></sub> = 0 and V<sub>REF<sup>-</sup></sub> = 0

capability. For example, if the underrange capability is 8LSB, the overrange capability is typically 31 - 8 = 23LSB.

### I<sup>2</sup>C INTERFACE

The LTC2453 communicates through an I<sup>2</sup>C interface. The I<sup>2</sup>C interface is a 2-wire open-drain interface supporting multiple devices and masters on a single bus. The connected devices can only pull the data line (SDA) LOW and never drive it HIGH. SDA must be externally connected to the supply through a pull-up resistor. When the data line is free, it is HIGH. Data on the I<sup>2</sup>C bus can be transferred at rates up to 100kbits/s in the Standard-Mode and up to 400kbits/s in the Fast-Mode. The V<sub>CC</sub> power should not be removed from the device when the I<sup>2</sup>C bus is active to avoid loading the I<sup>2</sup>C bus lines through the internal ESD protection diodes.

Each device on the I<sup>2</sup>C bus is recognized by a unique address stored in that device and can operate either as a transmitter or receiver, depending on the function of the device. In addition to transmitters and receivers, devices can also be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. Devices addressed by the master are considered a slave. The address of the LTC2453 is 0010100.

The LTC2453 can only be addressed as a slave. It can only transmit the last conversion result. The serial clock line, SCL, is always an input to the LTC2453 and the serial data line SDA is bidirectional. Figure 3 shows the definition of the I<sup>2</sup>C timing.

### The START and STOP Conditions

A START (S) condition is generated by transitioning SDA from HIGH to LOW while SCL is HIGH. The bus is considered to be busy after the START condition. When the data transfer is finished, a STOP (P) condition is generated by transitioning SDA from LOW to HIGH while SCL is HIGH. The bus is free after a STOP is generated. START and STOP conditions are always generated by the master.

When the bus is in use, it stays busy if a repeated START (Sr) is generated instead of a STOP condition. The repeated

## APPLICATIONS INFORMATION

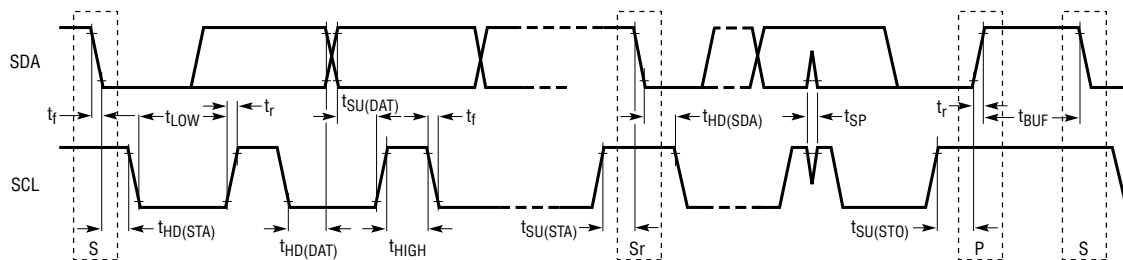


Figure 3. Definition of Timing for Fast/Standard Mode Devices on the I<sup>2</sup>C Bus

START timing is functionally identical to the START and is used for reading from the device before the initiation of a new conversion.

### Data Transferring

After the START condition, the I<sup>2</sup>C bus is busy and data transfer can begin between the master and the addressed slave. Data is transferred over the bus in groups of nine bits, one byte followed by one acknowledge (ACK) bit. The master releases the SDA line during the ninth SCL clock cycle. The slave device can issue an ACK by pulling SDA LOW or issue a Not Acknowledge (NAK) by leaving the SDA line HIGH impedance (the external pull-up resistor will hold the line HIGH). Change of data only occurs while the clock line (SCL) is LOW.

### Data Format

After a START condition, the master sends a 7-bit address followed by a read request (R) bit. The bit R is 1 for a Read Request. If the 7-bit address matches the LTC2453's address (hard-wired at 0010100) the ADC is selected. When the device is addressed during the conversion state, it does not accept the request and issues a NAK by leaving the SDA line HIGH. If the conversion is complete, the LTC2453 issues an ACK by pulling the SDA line LOW.

Following the ACK, the LTC2453 can output data. The data output stream is 16 bits long and is shifted out on the falling edges of SCL (see Figure 4). The first bit output by the LTC2453, the MSB, is the sign, which is 1 for  $V_{IN}^+ \geq V_{IN}^-$  and 0 for  $V_{IN}^+ < V_{IN}^-$  (see Table 1). The MSB (D15) is followed by successively less significant bits (D14, D13...) until the LSB is output by the LTC2453. This sequence is shown in Figure 5.

## OPERATION SEQUENCE

### Continuous Read

Conversions from the LTC2453 can be continuously read, see Figure 6. At the end of a read operation, a new conversion automatically begins. At the conclusion of the conversion cycle, the next result may be read using the method described above. If the conversion cycle is not complete and a valid address selects the device, the LTC2453 generates a NAK signal indicating the conversion cycle is in progress.

### Discarding a Conversion Result and Initiating a New Conversion

It is possible to start a new conversion without reading the old result, as shown in Figure 7. Following a valid 7-bit address, a read request (R) bit, and a valid ACK, a STOP command will start a new conversion.

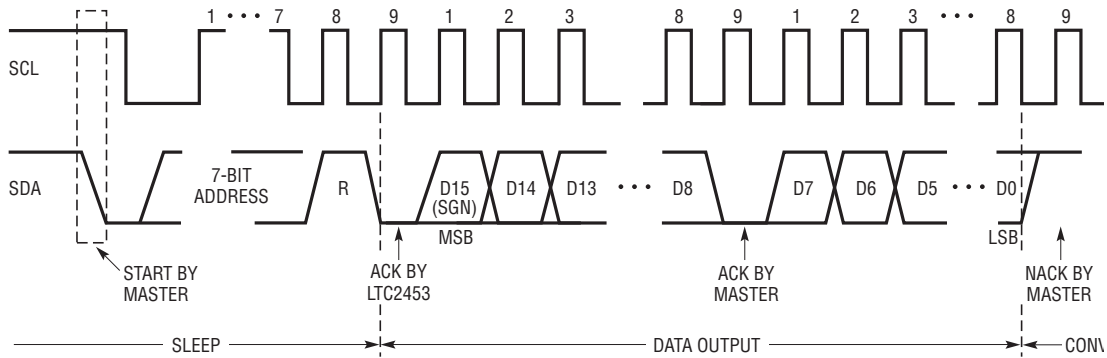
## PRESERVING THE CONVERTER ACCURACY

The LTC2453 is designed to dramatically reduce the conversion result's sensitivity to device decoupling, PCB layout, antialiasing circuits, line and frequency perturbations. Nevertheless, in order to preserve the high accuracy capability of this part, some simple precautions are desirable.

### Digital Signal Levels

Due to the nature of CMOS logic, it is advisable to keep input digital signals near GND or  $V_{CC}$ . Voltages in the range of 0.5V to  $V_{CC} - 0.5V$  may result in additional current leakage from the part.

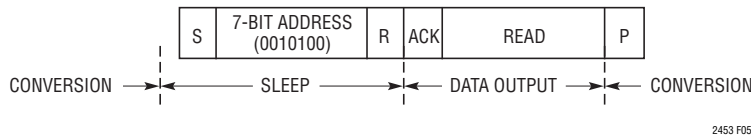
## APPLICATIONS INFORMATION



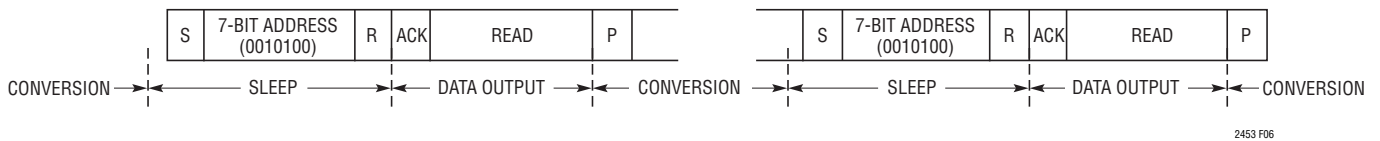
**Figure 4. Read Sequence Timing Diagram**

**Table 1. LTC2453 Output Data Format.  $FS = V_{REF+} - V_{REF-}$ .**

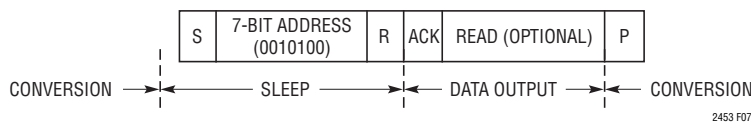
DIFFERENTIAL INPUT VOLTAGE $V_{IN+} - V_{IN-}$	D15 (MSB)	D14	D13	D12 ... D2	D1	D0 (LSB)	CORRESPONDING DECIMAL VALUE
$\geq FS$	1	1	1	1	1	1	65535
$FS - 1LSB$	1	1	1	1	1	0	65534
$0.5 \cdot FS$	1	1	0	0	0	0	49152
$0.5 \cdot FS - 1LSB$	1	0	1	1	1	1	49151
0	1	0	0	0	0	0	32768
-1LSB	0	1	1	1	1	1	32767
$-0.5 \cdot FS$	0	1	0	0	0	0	16384
$-0.5 \cdot FS - 1LSB$	0	0	1	1	1	1	16383
$\leq -FS$	0	0	0	0	0	0	0



**Figure 5. The LTC2453 Conversion Sequence**



**Figure 6. Consecutive Reading at the Same Configuration**



**Figure 7. Start a New Conversion without Reading Old Conversion Result**

## APPLICATIONS INFORMATION

### Driving $V_{CC}$ and GND

In relation to the  $V_{CC}$  and GND pins, the LTC2453 combines internal high frequency decoupling with damping elements, which reduce the ADC performance sensitivity to PCB layout and external components. Nevertheless, the very high accuracy of this converter is best preserved by careful low and high frequency power supply decoupling.

A 0.1 $\mu$ F, high quality, ceramic capacitor in parallel with a 10 $\mu$ F ceramic capacitor should be connected between the  $V_{CC}$  and GND pins, as close as possible to the package. The 0.1 $\mu$ F capacitor should be placed closest to the ADC package. It is also desirable to avoid any via in the circuit path, starting from the converter  $V_{CC}$  pin, passing through these two decoupling capacitors, and returning to the converter GND pin. The area encompassed by this circuit path, as well as the path length, should be minimized.

Very low impedance ground and power planes, and star connections at both  $V_{CC}$  and GND pins, are preferable. The  $V_{CC}$  pin should have three distinct connections: the first to

the decoupling capacitors described above, the second to the ground return for the input signal source, and the third to the ground return for the power supply voltage source.

### Driving $REF^+$ and $REF^-$

A simplified equivalent circuit for  $REF^+$  and  $REF^-$  is shown in Figure 8. Like all other A/D converters, the LTC2453 is only as accurate as the reference it is using. Therefore, it is important to keep the reference line quiet by careful low and high frequency power supply decoupling.

The LT6660 reference is an ideal match for driving the LTC2453's  $REF^+$  pin. The LT6660 is available in a 2mm  $\times$  2mm DFN package with 2.5V, 3V, 3.3V and 5V options.

A 0.1 $\mu$ F, high quality, ceramic capacitor in parallel with a 10 $\mu$ F ceramic capacitor should be connected between the  $REF^+/REF^-$  and GND pins, as close as possible to the package. The 0.1 $\mu$ F capacitor should be placed closest to the ADC.

### Driving $V_{IN}^+$ and $V_{IN}^-$

The input drive requirements can best be analyzed using the equivalent circuit of Figure 9. The input signal  $V_{SIG}$  is connected to the ADC input pins ( $IN^+$  and  $IN^-$ ) through an equivalent source resistance  $R_S$ . This resistor includes both the actual generator source resistance and any additional optional resistors connected to the input pins. Optional input capacitors  $C_{IN}$  are also connected to the

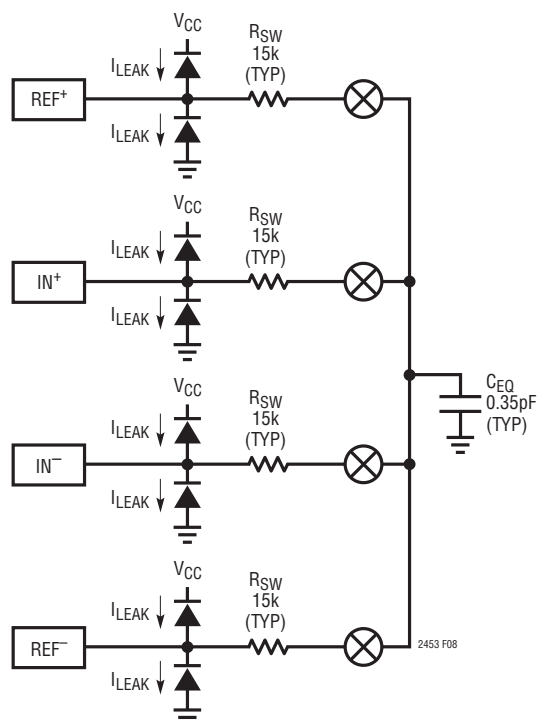


Figure 8. LTC2453 Analog Input/Reference Equivalent Circuit

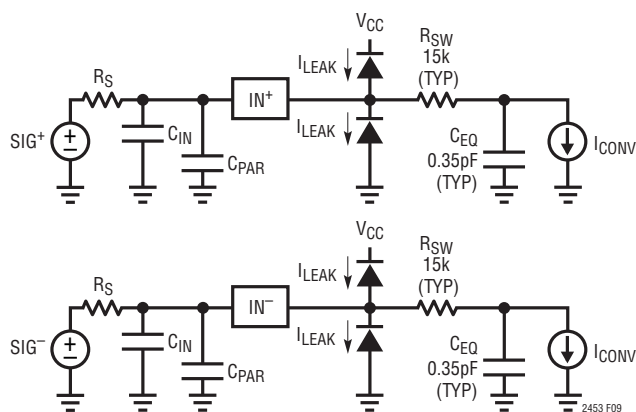


Figure 9. LTC2453 Input Drive Equivalent Circuit

## APPLICATIONS INFORMATION

ADC input pins. This capacitor is placed in parallel with the ADC input parasitic capacitance  $C_{PAR}$ . Depending on the PCB layout,  $C_{PAR}$  has typical values between 2pF and 15pF. In addition, the equivalent circuit of Figure 9 includes the converter equivalent internal resistor  $R_{SW}$  and sampling capacitor  $C_{EQ}$ .

There are some immediate trade-offs in  $R_S$  and  $C_{IN}$  without needing a full circuit analysis. Increasing  $R_S$  and  $C_{IN}$  can give the following benefits:

- 1) Due to the LTC2453's input sampling algorithm, the input current drawn by either  $V_{IN}^+$  or  $V_{IN}^-$  over a conversion cycle is 50nA. A high  $R_S \cdot C_{IN}$  attenuates the high frequency components of the input current, and  $R_S$  values up to 1k result in <1LSB error.
- 2) The bandwidth from  $V_{SIG}$  is reduced at the input pins ( $IN^+$ ,  $IN^-$ ). This bandwidth reduction isolates the ADC from high frequency signals, and as such provides simple antialiasing and input noise reduction.
- 3) Switching transients generated by the ADC are attenuated before they go back to the signal source.
- 4) A large  $C_{IN}$  gives a better AC ground at the input pins, helping reduce reflections back to the signal source.
- 5) Increasing  $R_S$  protects the ADC by limiting the current during an outside-the-rails fault condition.

There is a limit to how large  $R_S \cdot C_{IN}$  should be for a given application. Increasing  $R_S$  beyond a given point increases

the voltage drop across  $R_S$  due to the input current, to the point that significant measurement errors exist. Additionally, for some applications, increasing the  $R_S \cdot C_{IN}$  product too much may unacceptably attenuate the signal at frequencies of interest.

For most applications, it is desirable to implement  $C_{IN}$  as a high-quality 0.1 $\mu$ F ceramic capacitor and  $R_S \leq 1k$ . This capacitor should be located as close as possible to the actual  $V_{IN}$  package pin. Furthermore, the area encompassed by this circuit path, as well as the path length, should be minimized.

In the case of a 2-wire sensor that is not remotely grounded, it is desirable to split  $R_S$  and place series resistors in the ADC input line as well as in the sensor ground return line, which should be tied to the ADC GND pin using a star connection topology.

Figure 10 shows the measured LTC2453 INL vs Input Voltage as a function of  $R_S$  value with an input capacitor  $C_{IN} = 0.1\mu$ F.

In some cases,  $R_S$  can be increased above these guidelines. The input current is zero when the ADC is either in sleep or I/O modes. Thus, if the time constant of the input RC circuit  $\tau = R_S \cdot C_{IN}$ , is of the same order of magnitude or longer than the time periods between actual conversions, then one can consider the input current to be reduced correspondingly.

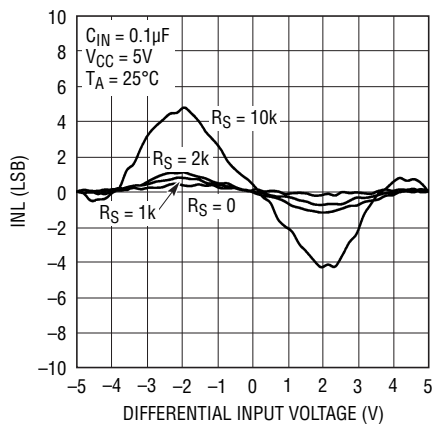


Figure 10. Measured INL vs Input Voltage,  $C_{IN} = 0.1\mu$ F,  $V_{CC} = 5V$ ,  $T_A = 25^\circ$ C

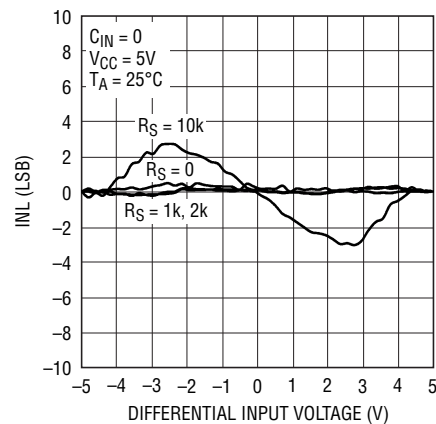


Figure 11. Measured INL vs Input Voltage,  $C_{IN} = 0$ ,  $V_{CC} = 5V$ ,  $T_A = 25^\circ$ C

## APPLICATIONS INFORMATION

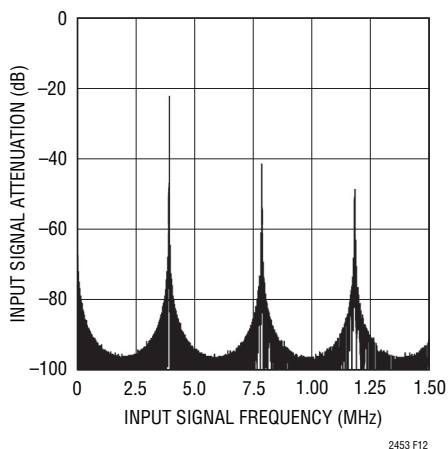


Figure 12. LTC2453 Input Signal Attenuation vs Frequency

These considerations need to be balanced out by the input signal bandwidth. The 3dB bandwidth  $\approx 1/(2\pi R_S C_{IN})$ .

Finally, if the recommended choice for  $C_{IN}$  is unacceptable for the user's specific application, an alternate strategy is to eliminate  $C_{IN}$  and minimize  $C_{PAR}$  and  $R_S$ . In practical terms, this configuration corresponds to a low impedance sensor directly connected to the ADC through minimum length traces. Actual applications include current measurements through low value sense resistors, temperature measurements, low impedance voltage source monitoring, and so on. The resultant INL vs  $V_{IN}$  is shown in Figure 11. The measurements of Figure 11 include a capacitor  $C_{PAR}$  corresponding to a minimum sized layout pad and a minimum width input trace of about 1 inch length.

### Signal Bandwidth, Transition Noise and Noise Equivalent Input Bandwidth

The LTC2453 includes a  $\text{sinc}^1$  type digital filter with the first notch located at  $f_0 = 60\text{Hz}$ . As such, the 3dB input signal bandwidth is 26.54Hz. The calculated LTC2453 input signal attenuation vs frequency over a wide frequency range is shown in Figure 12. The calculated LTC2453 input signal attenuation vs frequency at low frequencies is shown in Figure 13. The converter noise level is about  $1.4\mu\text{V}_{\text{RMS}}$  and can be modeled by a white noise source connected at the input of a noise-free converter.

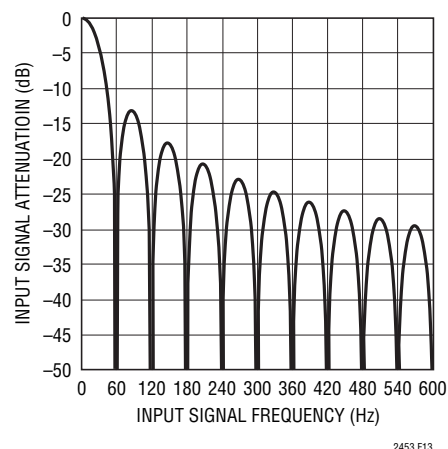


Figure 13. LTC2453 Input Signal Attenuation vs Frequency (Low Frequencies)

On a related note, the LTC2453 uses two separate A/D converters to digitize the positive and negative inputs. Each of these A/D converters has  $1.4\mu\text{V}_{\text{RMS}}$  transition noise. If one of the input voltages is within this small transition noise band, then the output will fluctuate one bit, regardless of the value of the other input voltage. If both of the input voltages are within their transition noise bands, the output can fluctuate 2 bits.

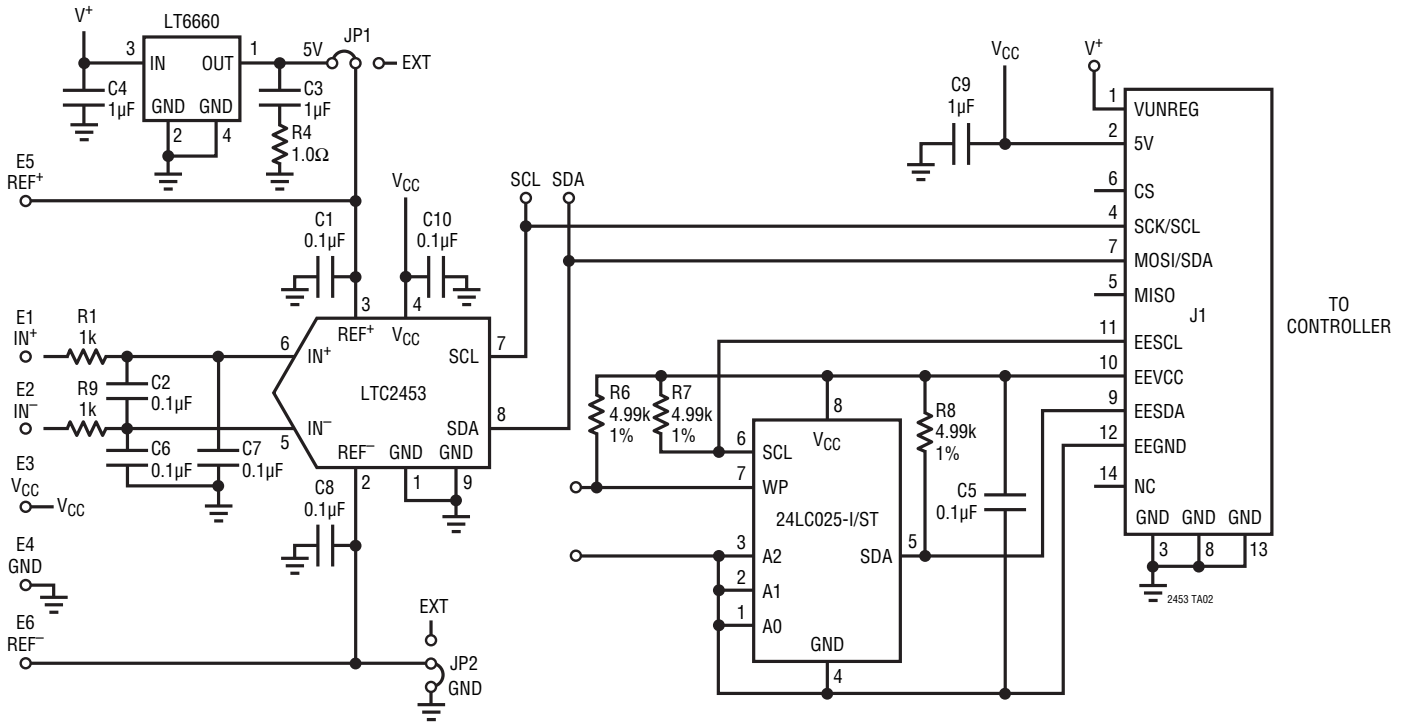
For a simple system noise analysis, the  $V_{IN}$  drive circuit can be modeled as a single-pole equivalent circuit characterized by a pole location  $f_i$  and a noise spectral density  $n_i$ . If the converter has an unlimited bandwidth, or at least a bandwidth substantially larger than  $f_i$ , then the total noise contribution of the external drive circuit would be:

$$V_n = n_i \sqrt{\pi / 2 \cdot f_i}$$

Then, the total system noise level can be estimated as the square root of the sum of  $(V_n^2)$  and the square of the LTC2453 noise floor ( $\sim 1.4\mu\text{V}^2$ ).

## TYPICAL APPLICATION

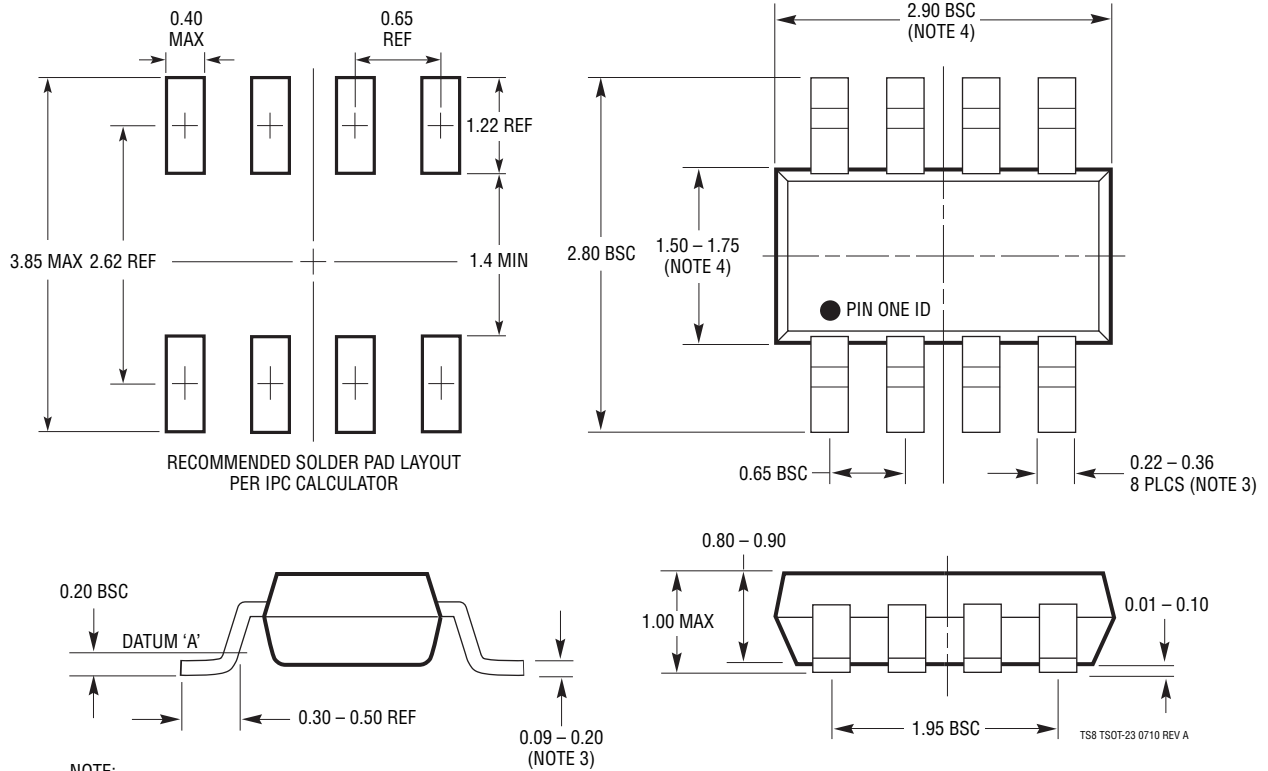
DC1266A Demo Board Schematic





## PACKAGE DESCRIPTION

**TSOT Package**  
**8-Lead Plastic TSOT**  
 (Reference LTC TS8 # 05-08-1637)



- NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
  2. DRAWING NOT TO SCALE
  3. DIMENSIONS ARE INCLUSIVE OF PLATING
  4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
  5. MOLD FLASH SHALL NOT EXCEED 0.254mm
  6. JEDEC PACKAGE REFERENCE IS MO-193

**REVISION HISTORY** (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	6/10	Added text to I <sup>2</sup> C Interface section	8
C	3/11	Updated Analog Inputs and References section Add text to Input Voltage Range section	3 8

## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1236A-5	Precision Bandgap Reference, 5V	0.05% Max, 5ppm/°C Drift
LT1461	Micropower Series Reference, 2.5V	0.04% Max, 3ppm/°C Drift
LT1790	Micropower Precision Reference in TSOT-23-6 Package	60μA Max Supply Current, 10ppm/°C Max Drift, 1.25V, 2.048V, 2.5V, 3V, 3.3V, 4.096V and 5V Options
LTC1860/LTC1861	12-Bit, 5V, 1-/2-Channel 250ksps SAR ADC in MSOP	850μA at 250ksps, 2μA at 1ksps, SO-8 and MSOP Packages
LTC1860L/LTC1861L	12-Bit, 3V, 1-/2-Channel 150ksps SAR ADC	450μA at 150ksps, 10μA at 1ksps, SO-8 and MSOP Packages
LTC1864/LTC1865	16-Bit, 5V, 1-/2-Channel 250ksps SAR ADC in MSOP	850μA at 250ksps, 2μA at 1ksps, SO-8 and MSOP Packages
LTC1864L/LTC1865L	16-bit, 3V, 1-/2-Channel 150ksps SAR ADC	450μA at 150ksps, 10μA at 1ksps, SO-8 and MSOP Packages
LTC2440	24-Bit No Latency $\Delta\Sigma^{\text{TM}}$ ADC	200nV <sub>RMS</sub> Noise, 8kHz Output Rate, 15ppm INL
LTC2480	16-Bit, Differential Input, No Latency $\Delta\Sigma$ ADC, with PGA, Temp. Sensor, SPI	Easy-Drive Input Current Cancellation, 600nV <sub>RMS</sub> Noise, Tiny 10-Lead DFN Package
LTC2481	16-Bit, Differential Input, No Latency $\Delta\Sigma$ ADC, with PGA, Temp. Sensor, I <sup>2</sup> C	Easy-Drive Input Current Cancellation, 600nV <sub>RMS</sub> Noise, Tiny 10-Lead DFN Package
LTC2482	16-Bit, Differential Input, No Latency $\Delta\Sigma$ ADC, SPI	Easy-Drive Input Current Cancellation, 600nV <sub>RMS</sub> Noise, Tiny 10-Lead DFN Package
LTC2483	16-Bit, Differential Input, No Latency $\Delta\Sigma$ ADC, I <sup>2</sup> C	Easy-Drive Input Current Cancellation, 600nV <sub>RMS</sub> Noise, Tiny 10-Lead DFN Package
LTC2484	24-Bit, Differential Input, No Latency $\Delta\Sigma$ ADC, SPI	Easy-Drive Input Current Cancellation, 600nV <sub>RMS</sub> Noise, Tiny 10-Lead DFN Package
LTC2485	24-Bit, Differential Input, No Latency $\Delta\Sigma$ ADC, I <sup>2</sup> C	Easy-Drive Input Current Cancellation, 600nV <sub>RMS</sub> Noise, Tiny 10-Lead DFN Package
LTC6241	Dual, 18MHz, Low Noise, Rail-to-Rail Op Amp	550nV <sub>P-P</sub> Noise, 125μV Offset Max
LT6660	Micropower References in 2mm × 2mm DFN Package, 2.5V, 3V, 3.3V, 5V	20ppm/°C max drift, 0.2% Max
LTC2450	Easy-to-Use, Ultra-Tiny 16-Bit ADC	2 LSB INL, 50nA Sleep current, Tiny 2mm × 2mm DFN-6 Package, 30Hz Output Rate
LTC2450-1	Easy-to-Use, Ultra-Tiny 16-Bit ADC	2 LSB INL, 50nA Sleep Current, Tiny 2mm × 2mm DFN-6 Package, 60Hz Output Rate

## Looking for pricing, stock, or lifecycle information?

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- ⊖ [Analog Devices Inc. Information](#)

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