THE DATASHEET OF

LTC2662IUH-12#TRPBF

www.win-source.net 0086-755-83957316

Data Sheet

LTC2662

Five-Channel, 300 mA Current-Source-Output 16-/12-Bit SoftSpan DACs

FEATURES

- Per-Channel Programmable Output Ranges: 300 mA, 200 mA, 100 mA, 50 mA, 25 mA, 12.5 mA, 6.25 mA and 3.125 mA
- Flexible 2.85 V to 33 V Supply Voltage
- 1 V Dropout Guaranteed
- Separate Voltage Supply per Output Channel
- Internal Switches to Optional Negative Supply
- Full 16-/12-Bit Resolution at All Ranges
- Guaranteed Operation –40°C to +125°C
- Precision (10 ppm/°C Max) Internal Reference or External Reference Input
- Analog Mux Monitors Voltages and Currents
- A/B Toggle via SPI or Dedicated Pin
- 1.8 V to 5 V SPI Serial Interface
- 5 mm × 5 mm 32-Lead QFN Package

APPLICATIONS

- Tunable Lasers
- Semiconductor Optical Amplifiers
- Resistive Heaters
- Current Mode Biasing
- Proportional Solenoid Drive

GENERAL DESCRIPTION

The LTC2662 is a family of five-channel, 16-/12-bit current-source digital-to-analog converters, providing five high-compliance current source outputs with guaranteed 1 V dropout at 200 mA. The part supports load voltages of up to 32 V. There are eight current ranges, programmable per channel, with full-scale outputs of up to 300 mA; and the channels can be paralleled to allow for ultrafine adjustments of large currents, or for combined outputs of up to 1.5 A.

A dedicated supply pin is provided for every output channel. Each can be operated from 2.85 V to 33 V, and internal switches allow any output to be pulled to the optional negative supply.

The LTC2662 includes a precision integrated 1.25 V reference (10 ppm/°C maximum), with the option to use an external reference.

The SPI/Microwire-compatible 3-wire serial interface operates on logic levels as low as 1.71 V at clock rates up to 50 MHz.

FUNCTIONAL BLOCK DIAGRAM

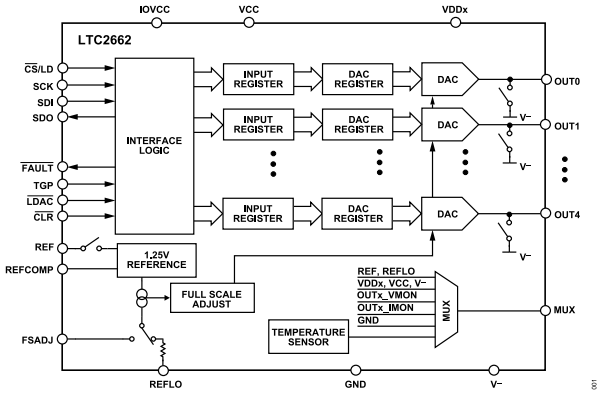

Figure 1. Functional Block Diagram

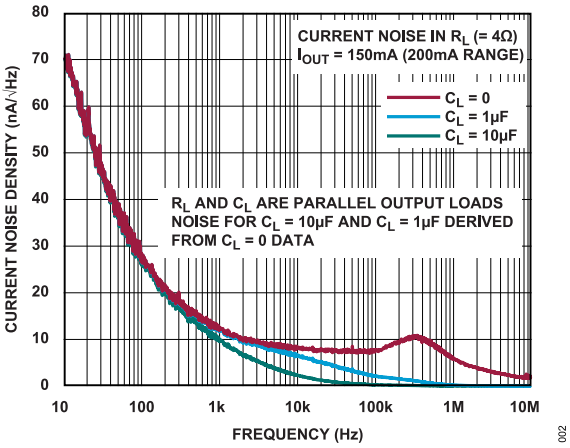

Figure 2. Current Noise Density vs. Frequency

DOCUMENT FEEDBACK
TECHNICAL SUPPORT

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4/2024—Rev. A to Rev. B

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SPECIFICATIONS

DAC CHARACTERISTICS

All specifications which apply over the full operating T_J range, otherwise specifications are at T_J = 25°C. V_{CC} = IOV_{CC} = 5 V; V^- = –5 V; $V_{DD0/1/2/3/4}$ = 5 V, V^+ = 5 V, FSADJ = V_{CC}, $V_{(REF)}$ = 1.25 V external, unless otherwise specified.

Table 1.

			LTC2662-12			LTC2662-16			
Parameter	**Symbol**	**Test Conditions/Comments**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
DC PERFORMANCE ALL RANGES[1]									
Resolution			12			16			Bits
Monotonicity		All current ranges[2]	12			16			Bits
Differential Non-linearity	DNL	All current ranges[2]	−0.5		+0.5	−1	±0.2	+1	LSB
Integral Non-linearity	INL	All current ranges[2]	−4		+4	−64	±12	+64	LSB
Current Offset Error	I_{OS}	All current ranges[2]	−0.4		+0.4	−0.4	±0.1	+0.4	%FSR
I_{OS} Temperature Coefficient		All current ranges[2], T_J = 25°C		10			±10		ppm/°C
Gain Error[1]	GE	300 mA and 200 mA output current ranges	−0.9		+0.9	−0.9	±0.3	+0.9	%FSR
		100 mA, 50 mA, and 25 mA output current ranges	−1.2		+1.2	−1.2	±0.4	+1.2	%FSR
		12.5 mA, 6.25 mA, and 3.125 mA output current ranges	−1.5		+1.5	−1.5	±0.7	+1.5	%FSR
Gain Temperature Coefficient		FSADJ = V_{CC}, T_J = 25°C		±30			30		ppm/°C
Total Unadjusted Error[1]	TUE	300 mA and 200 mA output current ranges	−1.4		+1.4	−1.4	±0.4	+1.4	%FSR
		100 mA, 50 mA, and 25 mA output current ranges	−1.7		+1.7	−1.7	±0.5	+1.7	%FSR
		12.5 mA, 6.25 mA, and 3.125 mA output current ranges	−2		+2	−2	±0.8	+2	%FSR
Power Supply Rejection Ratio	PSRR	Range = 100 mA, OUTx current (I_{OUTx}) = 50 mA							
		V_{CC} = 4.75 V to 5.25 V, T_J = 25°C		±0.15			±2.2		LSB
		V_{DDx} = 2.85 V to 3.15 V, T_J = 25°C		±0.05			±0.6		LSB
		V_{DDx} = 4.75 V to 5.25 V, T_J = 25°C		±0.25			±3.7		LSB
		V^+ = 4.75 V to 5.25 V, T_J = 25°C		±0.01			±0.09		LSB
		V^- = −5.25 V to −4.75 V, T_J = 25°C		±0.001			±0.01		LSB
DC Crosstalk[3]		Result of a 200 mW change in dissipated power, T_J = 25°C		±1			±14		LSB

[1] For the full-scale current (I_{FS}) = 300 mA, R_{LOAD} = 10 Ω. For I_{FS} = 200 mA, R_{LOAD} = 15 Ω. For I_{FS} = 100 mA, R_{LOAD} = 30 Ω. For I_{FS} = 50 mA, R_{LOAD} = 50 Ω. For I_{FS} = 25 mA, R_{LOAD} = 100 Ω. For I_{FS} = 12.5 mA, R_{LOAD} = 200 Ω. For I_{FS} = 6.25 mA, R_{LOAD} = 400 Ω. For I_{FS} = 3.125 mA, R_{LOAD} = 800 Ω.

[2] Current Offset Error is measured at Code 384 for the LTC2662-16, and at code 24 for the LTC2662-12. Linearity is defined from Code 384 to Code 65535 for the LTC2662-16 and from Code 24 to Code 4095 for the LTC2662-12.

[3] I_{FS} = 200 mA and R_{LOAD} = 15 Ω. DC crosstalk is measured with a 100 mA to 200 mA current step on all four aggressor channels. Total power dissipation change is 4 × 50 mW = 200 mW. The monitor channel is held at 3/4 × I_{FS} or 150 mA.

SPECIFICATIONS

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DC PERFORMANCE						
Dropout Voltage (V_{DDx} – V_{OUTx}[1])	$V_{DROPOUT}$	200 mA range, (V_{DDx} – V^-) = 4.75 V		0.72	1	V
		200 mA range, (V_{DDx} – V^-) = 2.85 V, T_J = 25°C		0.85		V
		200 mA range, (V_{DDx} – V^-) = 33 V		0.76	1.1	V
		300 mA range, (V_{DDx} – V^-) = 4.75 V, T_J = 25°C		1.13		V
		300 mA range, (V_{DDx} – V^-) = 2.85 V, valid for LTC2662C and LTC2662I		1.15	1.75	V
		300 mA range, (V_{DDx} – V^-) = 2.85 V, valid for LTC2662H		1.35	1.95	V
Hi-Z Output Leakage Current[2]		I_{OUTX} = Hi-Z, 2.85 V ≤ (V_{DDX} – V^-) ≤ 33 V	−1	+0.1	+1	µA
OUTx Switch to V^- Resistance to V^- supply	$R_{PULLDOWN}$	Span code = 1000 b, sinking 80 mA		8	12	Ω
OUTx Switch to V^- Current	$I_{PULLDOWN}$	Maximum allowable DC current, T_J = 25°C			80	mA
AC PERFORMANCE		T_A = 25°C for all ac performance specifications				
Settling Time[3, 4]	t_{SETTLE}					
Full-Scale Step 3.125 mA Range		±0.0015% (±1 LSB at 16b), T_J = 25°C		19.2		µs
		±0.024% (±1 LSB at 12b), T_J = 25°C		6.1		µs
145 mA to 155 mA Step 200 mA Range		±0.0015% (±1 LSB at 16b), T_J = 25°C		7.7		µs
		±0.024% (±1 LSB at 12b), T_J = 25°C		3.5		µs
Full-Scale Step 200 mA Range		±0.0015% (±1 LSB at 16b), T_J = 25°C		8.7		ms
		±0.024% (±1 LSB at 12b), T_J = 25°C		4.5		µs
Glitch Impulse		At midscale transition, 200 mA range, resistive load that connects the DAC output to GND (R_{LOAD}) = 4 Ω, T_J = 25°C		180		pA × s
DAC to DAC Crosstalk[5]		100 mA to 200 mA step, R_{LOAD} = 15 Ω, T_J = 25°C		150		pA × s
Output Current Noise Density	i_{NOISE}	Internal reference, I_{OUTx} = 150 mA, R_{LOAD} = 4 Ω, load capacitance (C_{LOAD}) = 10 µF				
		Frequency (f) = 1 kHz, T_J = 25°C		12		nA/√Hz
		f = 10 kHz, T_J = 25°C		5		nA/√Hz
		f = 100 kHz, T_J = 25°C		0.5		nA/√Hz
		f = 1 MHz, T_J = 25°C		0.05		nA/√Hz

[1] V_{OUTx} is the channel output (OUTx) voltage.

[2] The loads attached to the OUTx pins must be terminated to GND.

[3] V_{DDx} = 5 V (3.125 mA range), V_{DDx} = 4 V (200 mA range), and V^- = −5 V for all ranges. For large current output steps, internal thermal effects result in a final settling tail. In most cases, the tail is too small to affect settling to ±0.024%, but several milliseconds can be needed for full settling to the ±0.0015% level. For optimal results, solder/via all GND and REFLO pins as well as the exposed pad (LFCSP package only) to a solid GND plane and set VDDx as low as practicable for each channel to reduce power dissipation in the device.

[4] Internal reference mode. The load is 15 Ω (200 mA range) or 800 Ω (3.125 mA range) in parallel with 100 pF terminated to GND.

[5] DAC to DAC crosstalk is the glitch that appears at the output of one DAC because of a 100 mA to 200 mA step change in an adjacent DAC channel. The measured DAC is at midscale (100 mA output current) in the 200 mA span range, with the internal reference, V_{DDx} = 5 V, V^- = −3.3 V.

SPECIFICATIONS

REFERENCE CHARACTERISTICS

All specifications which apply over the full operating T_J range, otherwise specifications are at T_J = 25°C. V_{CC} = IOV_{CC} = 5 V; V^- = –5 V; $V_{DD0/1/2/3/4}$ = 5 V, V^+ = 5 V, FSADJ = V_{CC}, unless otherwise specified.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INTERNAL REFERENCE MODE						
Reference Output Voltage	V_{REF}	T_J = 25°C	1.248	1.250	1.252	V
V_{REF} Temperature Coefficient[1]		T_J = 25°C	−10	±3	+10	ppm/°C
V_{REF} Line Regulation		V_{CC} = 5 V ± 10%, T_J = 25°C		50		µV/V
V_{REF} Short-Circuit Current		V_{CC} = 5.5 V, forcing output to GND, T_J = 25°C		2.5		mA
REFCOMP Pin Short-Circuit Current		V_{CC} = 5.5 V, forcing output to GND, T_J = 25°C		65		µA
V_{REF} Load Regulation		V_{CC} = 5 V, reference current (I_{REF}) = 100 µA sourcing, T_J = 25°C		140		mV/mA
V_{REF} Output Voltage Noise Density		REFCOMP pin current ($C_{REFCOMP}$) = REFCOMP pin capacitance (C_{REF}) = 0.1 µF, at f = 10 kHz, T_J = 25°C		32		nV/√Hz
EXTERNAL REFEERENCE MODE						
External Reference Input Voltage		REFCOMP pin is tied to GND	1.225		1.275	V
External Reference Input Current				0.001	1	µA
External Reference Input Capacitance[2]		T_J = 25°C		40		pF
External Full-Scale Adjust Gain Resistor	R_{FSADJ}	R_{FSADJ} to GND	19	20	50	kΩ

[1] The temperature coefficient is calculated by first computing the ratio of the maximum change in the output voltage to the nominal output voltage, and then dividing the ratio by the specified temperature range.

[2] Guaranteed by design and not production tested.

DIGITAL INPUTS AND DIGITAL OUTPUTS

All specifications which apply over the full operating T_J range, otherwise specifications are at T_J = 25°C. V_{CC} = IOV_{CC} = 5 V; V^- = –5 V; $V_{DD0/1/2/3/4}$ = 5 V, V^+ = 5 V, FSADJ = V_{CC}, unless otherwise specified.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL INPUT/OUPUT						
Digital Output High Voltage	V_{OH}	SDO pin, load current = −100 µA	IOV_{CC} − 0.2			V
Digital Output Low Voltage	V_{OL}	SDO pin, load current = 100 µA			0.2	V
		$\overline{FAULT}$ pin, load current = 100 µA			0.2	V
Digital High-Z Output Leakage Current		SDO pin leakage current ($\overline{CS}$/LD high)	−1		+1	µA
		$\overline{FAULT}$ pin leakage current (not asserted)			1	µA
Digital Input Current		Input voltage (V_{IN}) = GND to IOV_{CC}	−1		+1	µA
Digital Input Capacitance[1]	C_{IN}				8	pF
High Level Input Voltage	V_{IH}	2.85 V ≤ IOV_{CC} ≤ V_{CC}	0.8 × IOV_{CC}			V
		1.71 V ≤ IOV_{CC} ≤ 2.85 V	0.8 × IOV_{CC}			V
Low Level Input Voltage	V_{IL}	2.85 V ≤ IOV_{CC} ≤ V_{CC}			0.5	V
		1.71 V ≤ IOV_{CC} ≤ 2.85 V			0.3	V

[1] Guaranteed by design and not production tested.

SPECIFICATIONS

POWER REQUIREMENTS

All specifications which apply over the full operating T_J range, otherwise specifications are at T_J = 25°C. V_{CC} = IOV_{CC} = 5 V; V^- = –5 V; $V_{DD0/1/2/3/4}$ = 5 V, V^+ = 5 V, FSADJ = V_{CC}, $V_{(REF)}$ = 1.25 V external, unless otherwise specified.

Table 5.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY						
Analog Supply Voltage	V_{CC}	V_{CC} Must Not Exceed V^+	2.85		5.5	V
Digital Input and Output Supply Voltage	IOV_{CC}		1.71		V_{CC}	V
Negative Supply	V^-		−15.75		0	V
Positive Supply	V^+		2.85		V^- + 33	V
Output Supply Voltages	V_{DDx}		2.85		V^+	V
V_{CC} Supply Current		All ranges (code = 0, all channels)		2.6	3.8	mA
IOV_{CC} Supply Current		All ranges (code = 0, all channels)		0.01	1	µA
V^+ Supply Current		All ranges (code = 0, all channels)		385	500	µA
V^- Supply Current		All ranges (code = 0, all channels)		2.3	3.2	mA
V_{DDX} Supply Current		All ranges (code = 0, per channel)		0.7	1.2	mA
		25 mA range (code = full-scale, per channel)[1]		26.5	27.6	mA
		200 mA range (code = full-scale, per channel)[1]		204	207	mA
V_{CC} Shutdown Current[2, 3]	I_{SLEEP}			1	10	µA
IOV_{CC} Shutdown Current				0.01	1	µA
V^+ Shutdown Current				20	36	µA
V^- Shutdown Current				30	59	µA
V_{DDX} Shutdown Current		Per channel		4.2	8.1	µA
MONITOR MULTIPLEXER						
MUX Pin DC Output Impedance		T_J = 25°C		15		kΩ
MUX Pin Leakage Current		Monitor multiplexer disabled (high impedance)	−1	+0.1	+1	µA
MUX Pin Output Voltage Range		Monitor multiplexer selected to OUT0 pin voltage to OUT4 pin voltage	V^-		V^+	V
MUX Pin Continuous Current[4]		T_A = 25°C (do not exceed)	−1		+1	mA

1 Single channel at a specified output.

2 V_{CC} = IOV_{CC} = 5 V, V_{DDx} = 5 V, V^- = −5 V.

3 Digital inputs are at 0 V or IOV_{CC}.

4 Guaranteed by design and not production tested.

TIMING CHARACTERISTICS

All specifications apply over the full operating T_J range, otherwise specifications are at T_J = 25°C. Digital input low and high voltages are 0 V and IOV_{CC}, respectively.

Table 6.

Parameter	Symbol	Test Conditions/ Comments	V^+ = V_{DDX} = V_{CC} = 2.85 V to 5.5 V, IOV_{CC} = 2.85 V to V_{CC}			V^+ = V_{DDX} = V_{CC} = 2.85 V to 5.5 V, 1.71 V ≤ IOV_{CC} < 2.85 V			Unit
			Min	Typ	Max	Min	Typ	Max	
SDI Valid to SCK Setup	t_1		6			7			ns
SDI Valid to SCK Hold	t_2		6			7			ns
SCK HIGH Time	t_3		9			30			ns
SCK LOW Time	t_4		9			30			ns
$\overline{CS}$/LD Pulse Width	t_5		10			15			ns
LSB SCK High to $\overline{CS}$/LD High	t_6		19			19			ns

SPECIFICATIONS

Table 6. (Continued)

Parameter	Symbol	Test Conditions/ Comments	$V^+ = V_{DDX} = V_{CC}$ = 2.85 V to 5.5 V, IOV_{CC} = 2.85 V to V_{CC}			$V^+ = V_{DDX} = V_{CC}$ = 2.85 V to 5.5 V, 1.71 V ≤ IOV_{CC} < 2.85 V			Unit
			Min	Typ	Max	Min	Typ	Max	
$\overline{CS}$/LD Low to SCK High	t_7		7			7			ns
Propagation Delay from SCK Falling Edge, C_{LOAD} = 10 pF	t_8	4.5 V ≤ IOV_{CC} ≤ V_{CC}			20				ns
		2.85 V ≤ IOV_{CC} < 4.5 V			30				ns
		1.71 V ≤ IOV_{CC} < 2.85 V						60	ns
$\overline{CLR}$ Pulse Width	t_9		20			30			ns
$\overline{CS}$/LD High to SCK Positive Edge	t_{10}		7			7			ns
$\overline{LDAC}$ Pulse Width	t_{12}		15			15			ns
$\overline{CS}$/LD High to $\overline{LDAC}$ High or Low Transition	t_{13}		15			15			ns
SCK Frequency		50% Duty Cycle			50			15	MHz
TGP High Time[1]	t_{14}		1			1			µs
TGP Low Time[1]	t_{15}		1			1			µs

[1] Guaranteed by design and not production tested.

Timing Diagrams

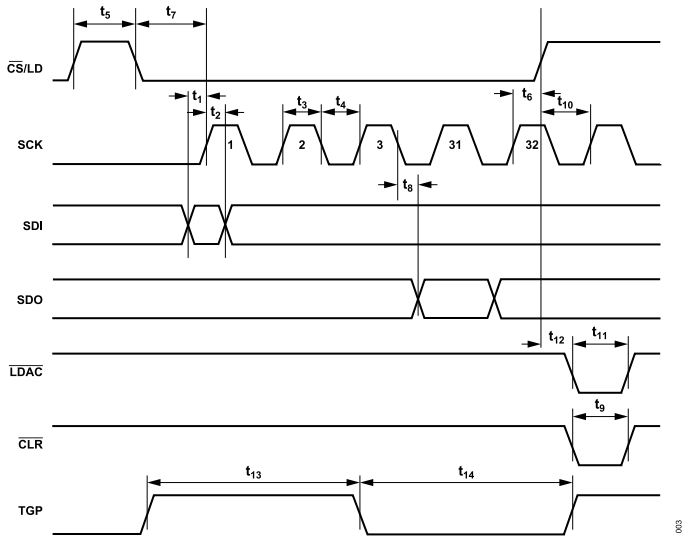


Figure 3. Serial Interface Timing

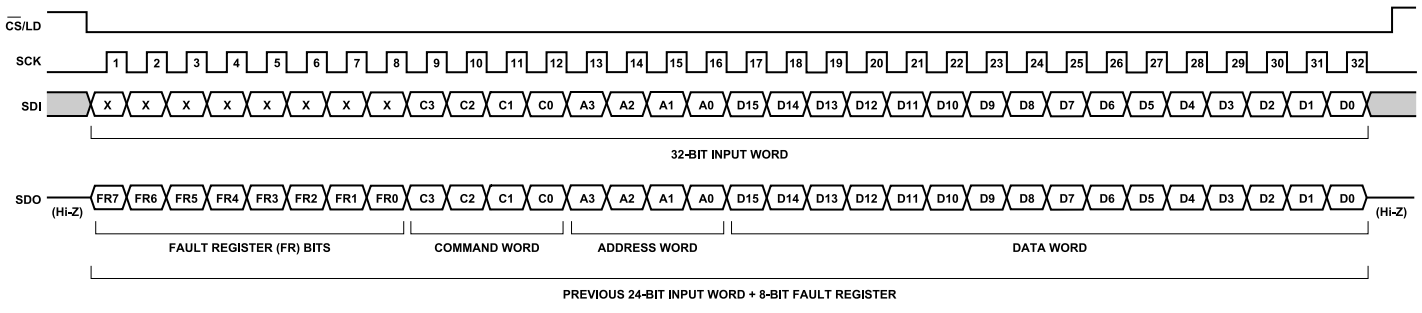


Figure 4. LTC2662-16 32-Bit Load Sequence

SPECIFICATIONS

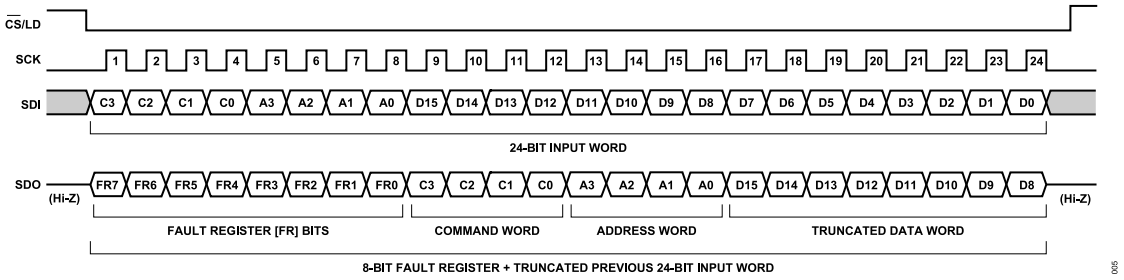


Figure 5. LTC2662-16 24-Bit Load Sequence

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
Analog Supply Voltage (V_{CC})	–0.3 V to 6 V
Digital I/O Voltage (IOV_{CC})	–0.3 V to 6 V
Negative Supply Voltage (V^-)	–16.5 V to 0.3 V
Positive Supply Voltage (V^+)	–0.3 V to (V^- + 36 V)
Output Supply Voltages (VDD0, VDD1, VDD2, VDD3, VDD4)	–0.3 V to (V^+ + 0.3 V)
OUT0, OUT1, OUT2, OUT3, OUT4	(V^- – 0.3 V) to (V_{DDX} + 0.3 V)
MUX	(V^- – 0.3 V) to (V^+ + 0.3 V)
REF, REFCOMP, FSADJ	–0.3 V to Min (V_{CC} + 0.3 V, 6 V)
$\overline{CS}$/LD, SCK, SDI, $\overline{LDAC}$, $\overline{CLR}$, TGP	–0.3 V to 6 V
$\overline{FAULT}$	–0.3 V to 6 V
SDO	–0.3 V to Min (IOV_{CC} + 0.3 V, 6 V)
Operating Junction Temperature (T_J) Range	
LTC2662C	0°C to 70°C
LTC2662I	–40°C to 85°C
LTC2662H	–40°C to 125°C
Maximum Junction Temperature	150°C
Storage Temperature Range	–65°C to 150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Thermal characteristics are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. Thermal resistance values specified in Table 8 are simulated based on JEDEC specifications using a 2S2P thermal test board (see JEDEC JESD51), except for θ_{JC-TOP}, which uses a JEDEC 1S test board.

θ_{JA} is the junction to ambient thermal resistance, measured in a JEDEC natural convection environment.

θ_{JC} is the junction to case thermal resistance, measured at the center of the package top surface, with an infinite heat sink attached to the package surface.

θ_{JB} is the junction to board thermal resistance, measured at a point on the board 1 mm from the package edge, along the package center line, measured in a JEDEC θ_{JB} environment.

Ψ_{JB} is the junction to board thermal characterization parameter, measured in a JEDEC natural convection environment.

Ψ_{JT} is the junction to package top thermal characterization parameter, measured in a JEDEC natural convection environment.

Do not use θ_{JA}, θ_{JC}, and θ_{JB} thermal resistances to perform direct calculation/measurement of the die temperature because doing so results in incorrect values. The thermal resistances assume 100% of the power that is dissipated along the specified path between the measurement points. The thermal resistances are directly dependent on the PCB design and environment.

If direct measurement of the package is required, the Ψ_{JT} and Ψ_{JB} values must be used because they more accurately reflect the true thermal dissipation paths.

θ_{JC} must only be used where an external heat sink is attached directly to the package.

System level thermal simulation is highly recommended.

For more details about the thermal resistances, refer to *JEDEC51-12: Guidelines for Reporting and Using Electronic Package Thermal Information*.

Table 8. Thermal Resistance

Package Type	θ_{JA}	θ_{JB}	θ_{JC-TOP}	Ψ_{JT}	Ψ_{JB}	Unit
05-08-1693[1]	28.34	9.27	17.33	0.11	9.20	°C/W

[1] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with no bias. See JEDEC JESD-51.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for the LTC2662

Table 9. LTC2662, 32-lead LFCSP

ESD Model	Withstand Voltage (V)	Class
HBM	2000	2
FICDM	1500	C3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

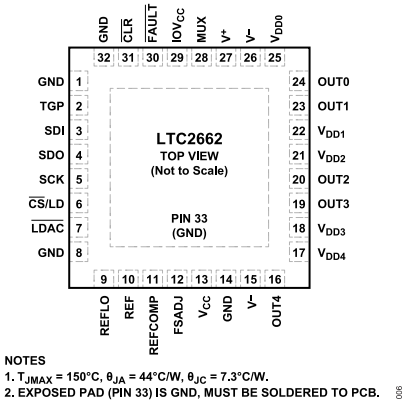


Figure 6. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 8, 14, 32	GND	Ground. These pins and the exposed pad (Pin 33) must be tied directly to a solid ground plane.
2	TGP	Asynchronous Toggle Pin. A falling edge updates the DAC register with data from input register A. A rising edge updates the DAC register with data from input register B. Toggle operations only affect those DAC channels with their toggle select bit (Tx) set to 1. Tie the TGP pin to IOV_{CC} if toggle operations are to be done through software. Tie the TGP pin to GND if not using toggle operations. Logic levels are determined by IOV_{CC}.
3	SDI	Serial Data Input. Data on SDI is clocked into the DAC on the rising edge of SCK. The LTC2662 accepts input word lengths of 24, 32, or multiples of 32 bits. Logic levels are determined by IOV_{CC}.
4	SDO	Serial Data Output. The serial output of the 32-bit shift register appears at the SDO pin. The data transferred to the device via the SDI pin is delayed 32 SCK rising edges before being output at the next falling edge. Can be used for data echo readback or daisy-chain operation. The SDO pin becomes high impedance when $\overline{CS}$/LD is high. Logic levels are determined by IOV_{CC}.
5	SCK	Serial Clock Input. Logic levels are determined by IOV_{CC}.
6	$\overline{CS}$/LD	Serial Interface Chip Select/Load Input. When $\overline{CS}$/LD is low, SCK is enabled for shifting SDI data into the register. In addition, SDO is enabled when $\overline{CS}$/LD is low. When $\overline{CS}$/LD is taken high, SDO and SCK are disabled and the specified command (see Table 11) is executed. Logic levels are determined by IOV_{CC}.
7	$\overline{LDAC}$	Active Low Asynchronous DAC Update Pin. This pin allows updates independent of SPI timing. If $\overline{CS}$/LD is high, a falling edge on $\overline{LDAC}$ updates all DAC registers with the contents of the input registers. $\overline{LDAC}$ is gated by $\overline{CS}$/LD and has no effect if $\overline{CS}$/LD is low. Logic levels are determined by IOV_{CC}. If not used, tie $\overline{LDAC}$ to IOV_{CC}.
9	REFLO	Reference Low. Signal ground for the reference. Tie directly to GND.
10	REF	Reference Input/Output. The voltage at the REF pin proportionally scales the full-scale output current of each DAC output channel. By default, the internal 1.25 V reference is routed to this pin. This pin must be buffered when driving external DC load currents. If the reference is disabled (see the Reference Modes section in the Theory of Operation section), its output is disconnected and the REF pin becomes a high impedance input which will accept a precision external reference. For low noise and reference stability, tie a capacitor from this pin to GND. The value must be less than $C_{REFCOMP}$, where $C_{REFCOMP}$ is the capacitance tied to the REFCOMP pin. The allowable external reference input range is 1.225 V to 1.275 V.
11	REFCOMP	Internal Reference Compensation Pin. For low noise and reference stability, tie a 0.1 µF capacitor from this pin to GND. Tying REFCOMP to GND causes the part to power up with the internal reference disabled, allowing the use of an external reference at start-up.
12	FSADJ	Full-Scale Current Adjust Pin. This pin can be used in one of two ways to produce either nominal, internally-calibrated output ranges, or incrementally-tunable ranges. In either case, the reference voltage V_{REF} is forced across a resistor R_{FSADJ} to define a reference current that scales the outputs for all ranges and channels. Full-scale currents are proportional to the voltage at REF (Pin 10) and inversely proportional to R_{FSADJ}. If FSADJ is tied to V_{CC}, an internal R_{FSADJ} (20 kΩ) is selected, resulting in nominal output ranges. An external resistor of 19 kΩ to 41 kΩ can be used instead by simply connecting the resistor between FSADJ and GND. In this case the external resistor controls the scaling of ranges, and the internal resistor is automatically disconnected. See Table 13 for details. When using an external resistor, FSADJ is sensitive to stray capacitance; the pin should be compensated with a snubber network consisting of a series combination of 1 kΩ and 1 µF, connected in parallel to R_{FSADJ}. With the recommended compensation, the pin is stable driving stray capacitance of up to 50 pF.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 10. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
13	V_{CC}	Analog Supply Voltage. 2.85 V ≤ V_{CC} ≤ 5.5 V. Bypass to GND with a 1 µF capacitor.
15, 26	V^-	Negative Supply Voltage. –15.75 V ≤ V^- ≤ GND. Bypass to GND with a 1 µF capacitor unless V^- is connected to GND.
24, 23, 20, 19, 16	OUT0 to OUT4	DAC Analog Current Outputs. Each current output pin has a dedicated analog supply pin V_{DD0} to V_{DD4}. The operational voltage level range at these pins is V^- ≤ V_{OUTX} ≤ V_{DDX}.
25, 22, 21, 18, 17	V_{DD0} to V_{DD4}	Output Supply Voltages. 2.85 V ≤ $V_{DD0/1/2/3/4}$ ≤ V^+. These five positive supply inputs provide independent supplies for each of the five DAC current output pins OUT0 to OUT4 respectively. Bypass each supply input to GND separately with a 1 µF capacitor.
27	V^+	Positive Supply Voltage. 2.85 V ≤ V^+ ≤ V^- + 33 V. V^+ must always be greater than or equal to the largest of the five DAC positive supply voltages V_{DD0} to V_{DD4} and V_{CC}. The supply voltage difference (V^+ – V^-) cannot exceed 33 V maximum. Bypass to GND with a 1 µF capacitor.
28	MUX	Analog Multiplexer Output. Pin voltages and currents can be monitored by measuring the voltage at the MUX pin. When the mux is disabled, this pin becomes high impedance. The available mux selections are given in Table 14.
29	IOV_{CC}	Digital Input/Output Supply Voltage. 1.71 V ≤ IOV_{CC} ≤ V_{CC} + 0.3 V. Bypass to GND with a 0.1 µF capacitor.
30	$\overline{FAULT}$	Active-Low Fault Detection Pin. This open-drain N-channel output pulls low when any valid fault condition is detected. This pin is released on the next $\overline{CS}$/LD rising edge. A pull-up resistor is required.
31	$\overline{CLR}$	Active-Low Asynchronous Clear Input. A logic low at this level-triggered input clears the part to the default reset code and output range which is zero-scale and high impedance (Hi-Z) outputs. The control registers are cleared to zero. Logic levels are determined by IOV_{CC}.
33	Exposed Pad	Ground. Solder this pad directly to the analog ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

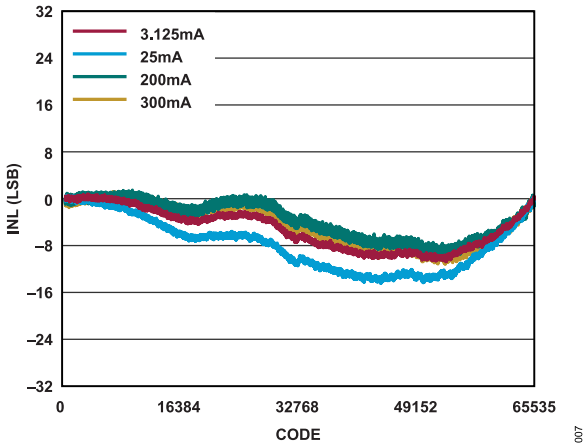


Figure 7. LTC2662-16 Integral Nonlinearity (INL)

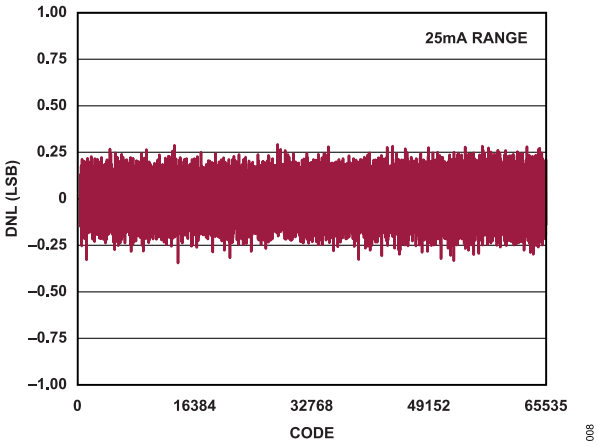


Figure 8. LTC2662-16 Differential Nonlinearity (DNL)

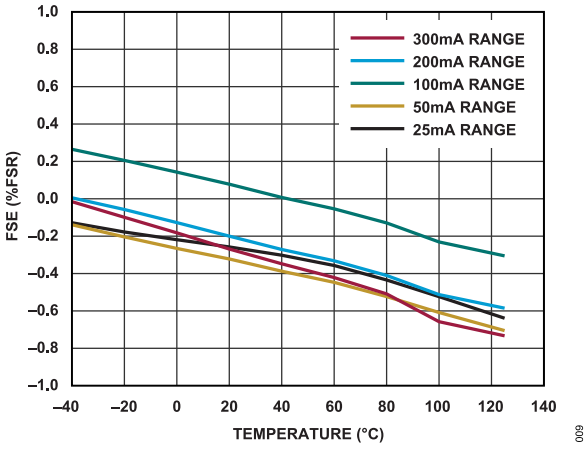


Figure 9. Full–Scale Current Error vs. Temperature

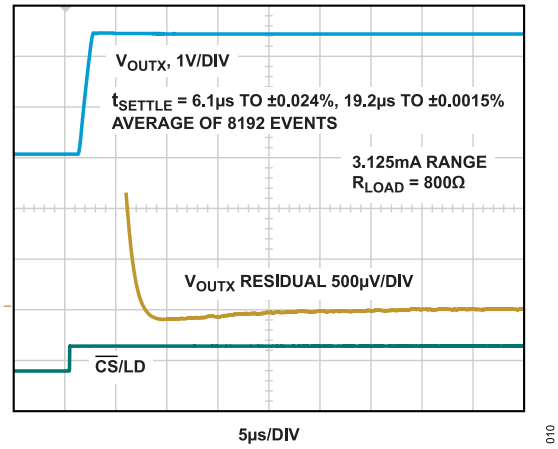


Figure 10. Settling 0 to 3.125 mA Step

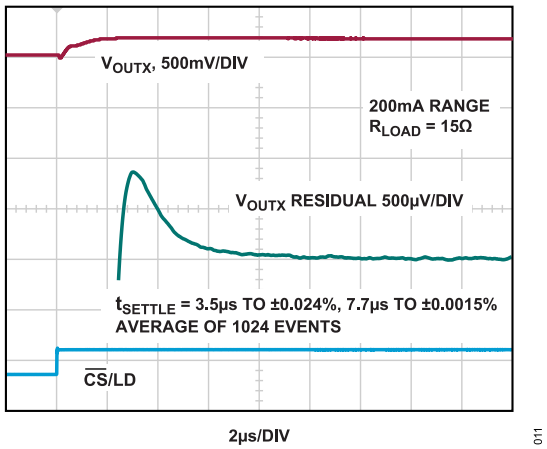


Figure 11. Settling 145 mA to 155 mA Step

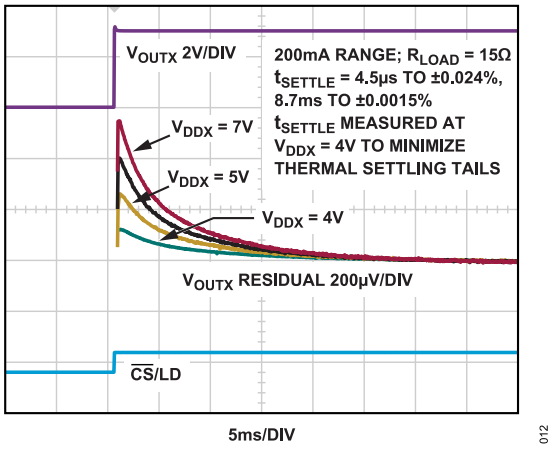


Figure 12. Settling 0 to 200 mA Step

TYPICAL PERFORMANCE CHARACTERISTICS

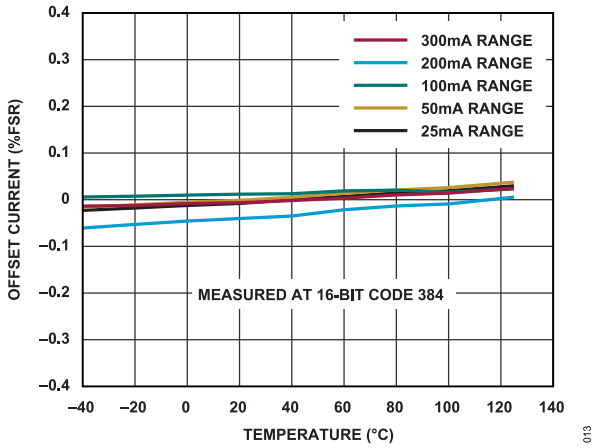


Figure 13. Offset Current Error vs. Temperature

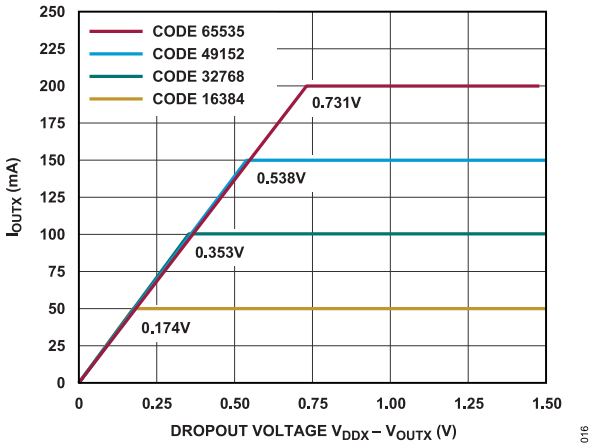


Figure 16. Dropout Voltage vs. Code, 200 mA Range

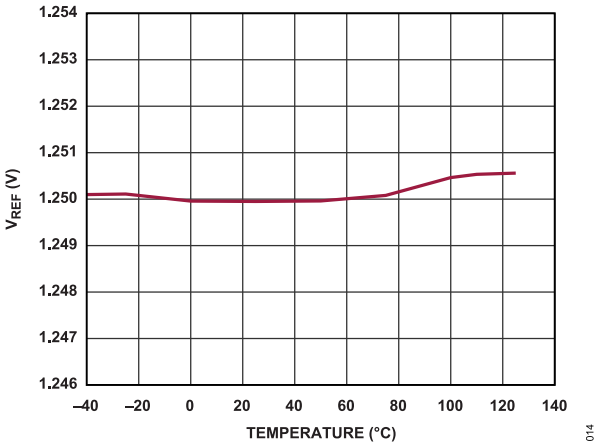


Figure 14. Reference Output vs. Temperature

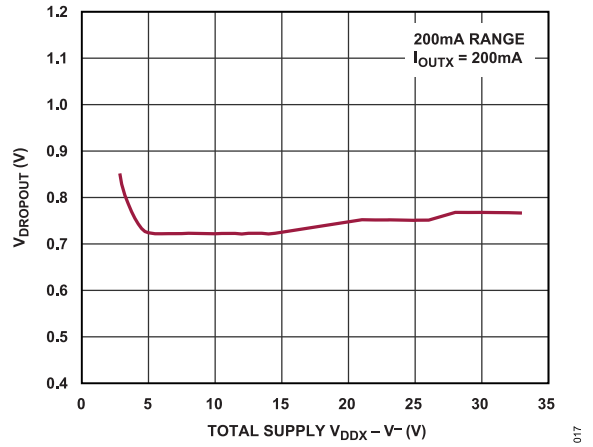


Figure 17. Dropout vs. Total Supply Voltage

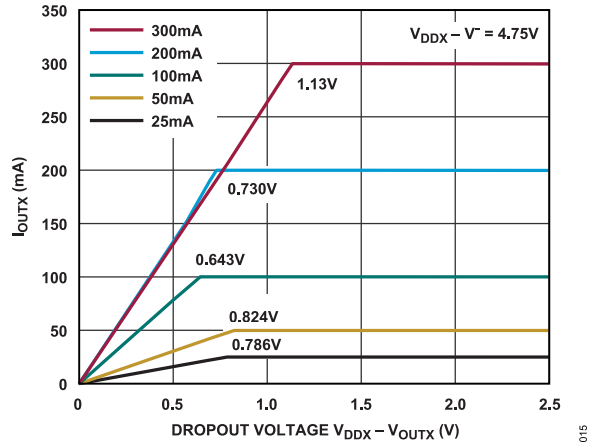


Figure 15. Dropout Voltage vs. Current Range

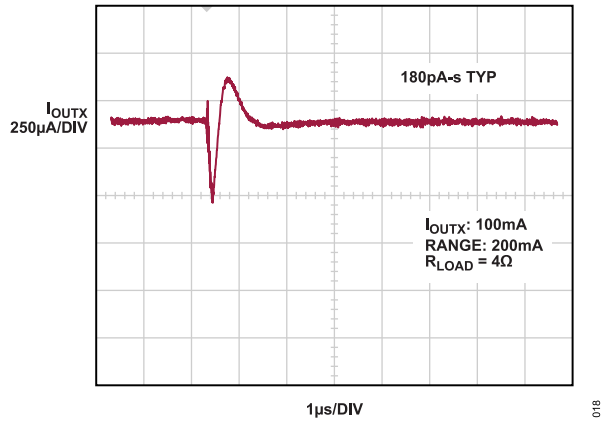


Figure 18. Mid-Scale Glitch

TYPICAL PERFORMANCE CHARACTERISTICS

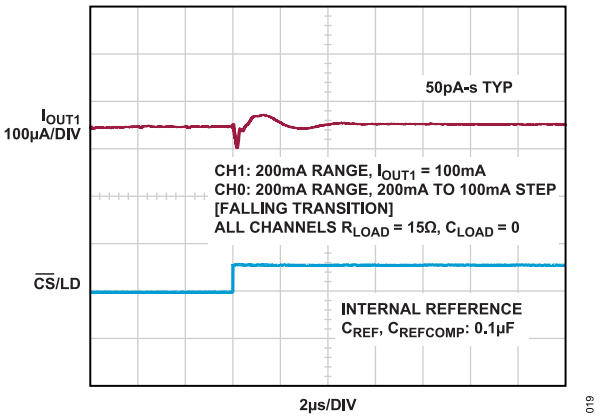


Figure 19. DAC-to-DAC Crosstalk (Falling)

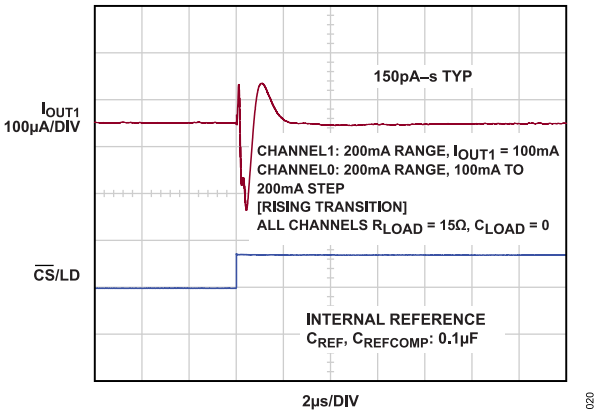


Figure 20. DAC-to-DAC Crosstalk (Rising)

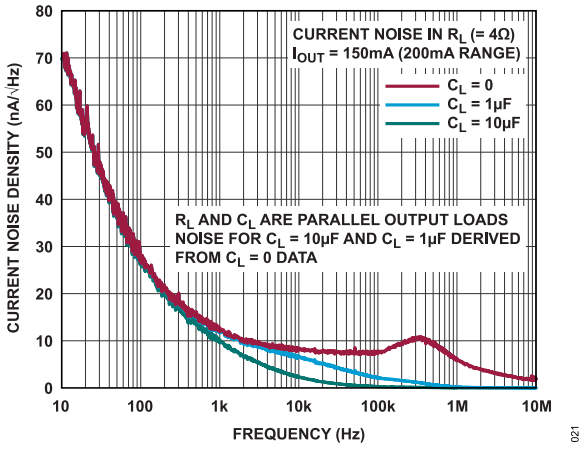


Figure 21. Current Noise Density vs. Frequency

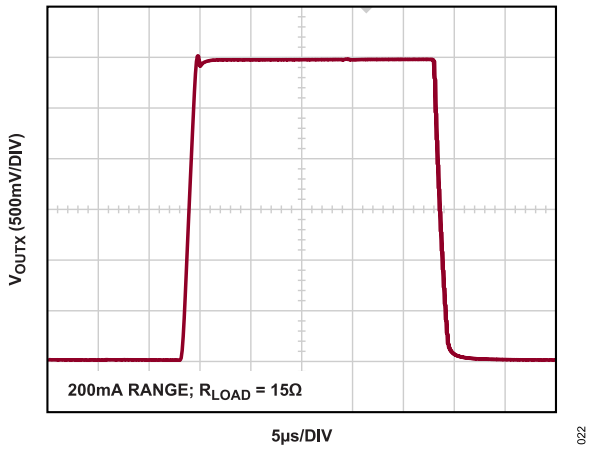


Figure 22. Large Signal Response

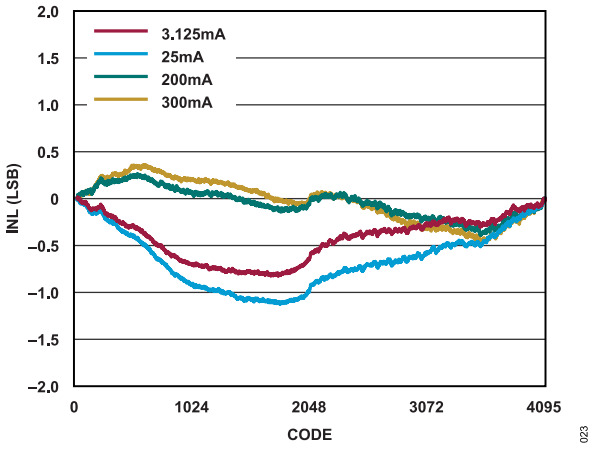


Figure 23. LTC2662-12 Integral Nonlinearity (INL)

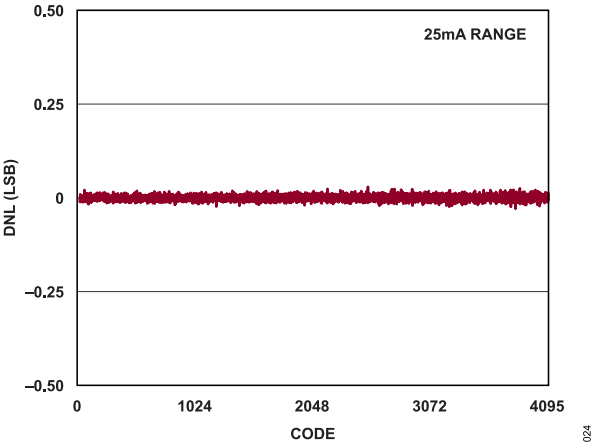


Figure 24. LTC2662-12 Differential Nonlinearity (DNL)

TYPICAL PERFORMANCE CHARACTERISTICS

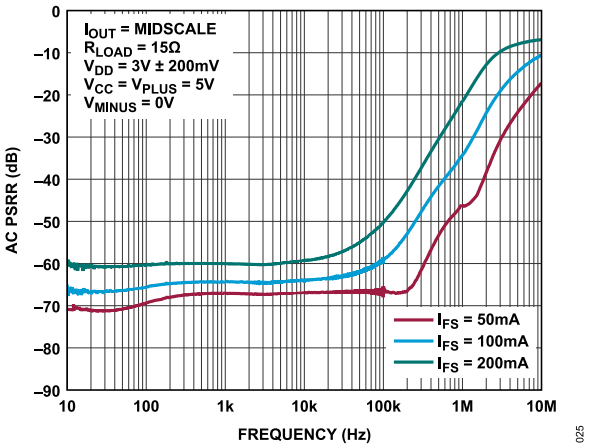


Figure 25. AC PSRR vs. Frequency

THEORY OF OPERATION

The LTC2662 is a family of five-channel, current source output digital-to-analog converters (DACs) with selectable output ranges, precision reference and a high-voltage multiplexer (MUX) for surveying the channel output voltages and currents. Each output draws its current from a separate dedicated positive supply pin that accepts voltages of 2.85 V to 33 V, allowing optimization of power dissipation and headroom for a wide range of loads. Internal 12 Ω switches allow any output pin to be connected to an optional negative V^- supply voltage and sink up to 80 mA.

POWER-ON-RESET

The outputs reset to a high-impedance state on power up, making system initialization consistent and repeatable. After power-on initialization, select the output range via SPI bus using Table 11, Table 12, and Table 13.

POWER SUPPLY SEQUENCING AND START-UP

The supplies (V_{CC}, IOV_{CC}, V^+, V^-, and V_{DD0} to V_{DD4}) may be powered up in any convenient order. If an external reference is used, do not allow the input voltage at REF to rise above V_{CC} + 0.3 V during supply turn-on and turn-off sequences (see the Absolute Maximum Ratings section).

After start-up, IOV_{CC} should be within V_{CC}; and no supply should exceed V^+. DC reference voltages of 1.225 V to 1.275 V are acceptable.

Supply bypassing is critical to achieving the best possible performance. Use at least 1 µF of low-ESR capacitance to ground on all supply pins and locate as close to the device as possible. A 0.1 µF capacitor may be used for IOV_{CC}.

DATA TRANSFER FUNCTIONS

The DAC input-to-output transfer functions for all resolutions and output ranges greater than or equal to 25 mA are shown in Figure 26 and Figure 27. The input code is in straight binary format for all ranges.

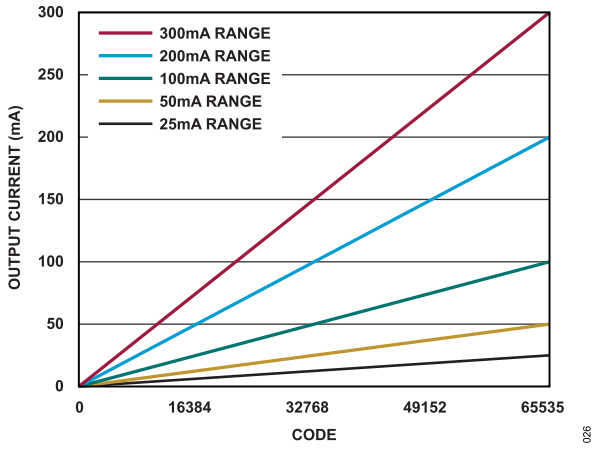


Figure 26. LTC2662-16 Transfer Function

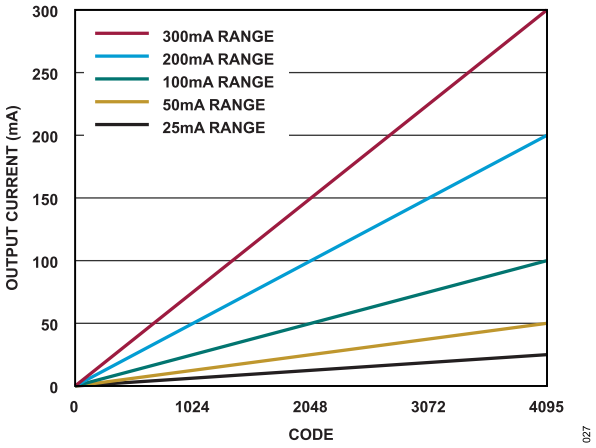


Figure 27. LTC2662-12 Transfer Function

SERIAL INTERFACE

When the $\overline{CS}$/LD pin is taken low, the data on the SDI pin is loaded into the shift register on the rising edge of the clock (SCK pin). The 4-bit command, C3-C0, is loaded first, followed by the 4-bit DAC address, A3-A0, and finally the 16-bit data word in straight binary format. For the LTC2662-16, the data word comprises the 16-bit input code, ordered MSB-to-LSB. For the LTC2662-12, the data word comprises the 12-bit input code, ordered MSB-to-LSB, followed by four don't-care bits. Data can only be transferred to the LTC2662 when the $\overline{CS}$/LD signal is low. The rising edge of $\overline{CS}$/LD ends the data transfer and causes the device to carry out the action specified in the 24-bit input word.

Table 11. Command Codes

Command				
C3	C2	C1	C0	
0	0	0	0	Write Code to n
1	0	0	0	Write Code to All
0	1	1	0	Write Span to n
1	1	1	0	Write Span to All
0	0	0	1	Update n (Power Up)
1	0	0	1	Update All (Power Up)
0	0	1	1	Write Code to n, Update n (Power Up)
0	0	1	0	Write Code to n, Update All (Power Up)
1	0	1	0	Write Code to All, Update All (Power Up)
0	1	0	0	Power Down n
0	1	0	1	Power Down Chip
1	0	1	1	Monitor Mux
1	1	0	0	Toggle Select
1	1	0	1	Global Toggle
0	1	1	1	Config Command
1	1	1	1	No Operation

THEORY OF OPERATION

Table 12. DAC Addresses, n

Address[1]				
A3	A2	A1	A0	
0	0	0	0	DAC 0
0	0	0	1	DAC 1
0	0	1	0	DAC 2
0	0	1	1	DAC 3
0	1	0	0	DAC 4

[1] Any DAC address code used other than the codes given above in Table 12 will cause the command to be ignored.

While the minimum input word is 24 bits, it may optionally be extended to 32 bits. To use the 32-bit word width, 8 don't-care bits must be transferred to the device first, followed by the 24-bit word, as just described. The 32-bit word is required for daisy-chain operation. It also provides accommodation for processors that have a minimum word width of 16 or more bits. The complete 24-bit and 32-bit sequences are shown in Figure 4 and Figure 5. Note that the Fault Register outputs appear on the SDO pin for either word width.

INPUT AND DAC REGISTERS

The LTC2662 has five internal registers for each DAC, in addition to the main shift register. Each DAC channel has two sets of double-buffered registers: one set for the code data, and one set for the span (output range) of the DAC. Double buffering provides the capability to simultaneously update the span and code, which allows smooth current transitions when changing output ranges. It also permits the simultaneous updating of multiple DACs.

Each set of double-buffered registers comprises an input register and a DAC register:

- Input Register: The write operation shifts data from the SDI pin into a chosen register. The input registers are holding buffers; write operations do not affect the DAC outputs.

  In the code data path, there are two input registers, A and B, for each DAC register. Register B is an alternate register used only in the toggle operation, while register A is the default input register.
- DAC Register: The update operation copies the contents of an input register to its associated DAC register. The content of a DAC register directly controls the DAC output current or range. The update operation also powers up the selected DAC if it had been in power-down mode.

Note that updates always refresh both code and span data, but the values held in the DAC registers remain unchanged unless the associated input register values have been changed via a write operation. For example, if a new code is written and the channel is updated, the code is updated while the span is refreshed unchanged. A channel update can come from a serial update command, an $\overline{\text{LDAC}}$ negative pulse or a toggle operation.

OUTPUT RANGES AND SOFTSPAN OPERATION

The LTC2662 is a five-channel current DAC with selectable output ranges. The full set of current output ranges is only available through SPI programming.

Figure 29 shows a simplified diagram of a single channel of the LTC2662. The full-scale current range of the LTC2662 is selected via four control bits S(3:0) on a per channel basis. Also provided is the ability to provide an external reference or to use a precision external resistor at pin FSADJ to reduce the overall gain drift over temperature of the LTC2662.

The LTC2662 initializes at power-on with all channel outputs (OUT0 to OUT4) at Hi-Z. The range and code of each channel are then fully programmable through SoftSpan as given in Table 13.

Each channel has a set of double-buffered registers for range information. Program the span input register using the **write span n** or **write span all** commands (0110b and 1110b, respectively). Figure 28 shows the syntax, and Table 13 shows the span codes and ranges.

As with the double-buffered code registers, update operations copy the span input registers to the associated span DAC registers.

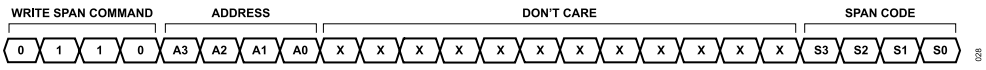


Figure 28. Write Span Syntax

THEORY OF OPERATION

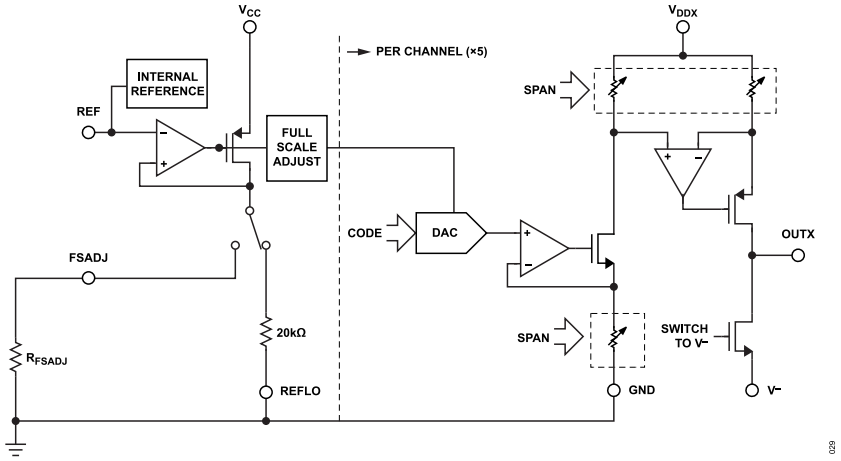


Figure 29. LTC2662 Single Channel Simplified Diagram

Table 13. Span Codes

				Output Range	
S3	S2	S1	S0	External R_{FSADJ}	FSADJ = V_{CC}
0	0	0	0	(Hi-Z)	
0	0	0	1	50 × V_{REF}/R_{FSADJ}	3.125 mA
0	0	1	0	100 × V_{REF}/R_{FSADJ}	6.25 mA
0	0	1	1	200 × V_{REF}/R_{FSADJ}	12.5 mA
0	1	0	0	400 × V_{REF}/R_{FSADJ}	25 mA
0	1	0	1	800 × V_{REF}/R_{FSADJ}	50 mA
0	1	1	0	1600 × V_{REF}/R_{FSADJ}	100 mA
0	1	1	1	3200 × V_{REF}/R_{FSADJ}	200 mA
1	1	1	1	4800 × V_{REF}/R_{FSADJ}	300 mA
1	0	0	0	(Switch to V^-)	

As shown in Table 13, there are two additional selections (code 0000 and code 1000) which place the output(s) in a high impedance (Hi-Z) mode or in a mode where a low on-resistance (≤ 12 Ω) NMOS device shunts the DAC output to the negative supply V^-. When the NMOS device is enabled, the OUTX pin driver is disabled for that channel(s). Span codes not listed in Table 13 default to the Hi-Z output range.

MONITOR MUX

The LTC2662 includes a high voltage multiplexer (mux) for monitoring both the voltages and currents at the five current output pins (OUT0 to OUT4). Additionally, the output supply voltages (V_{DD0} to V_{DD4}), the positive/negative supplies V^+/V^-, core supply V_{CC}, reference voltage V_{REF} and die temperature can all be monitored.

The MUX pin is intended for use with high impedance inputs only; the impedance at the pin is typically 15 kΩ. Continuous DC output current at the MUX pin must be limited to ±1 mA to avoid damaging internal circuitry.

The operating range of the mux extends rail-to-rail from V^- to V^+; its output is disabled (high impedance) at power-up.

The syntax and codes for the **mux** command are shown in Figure 30 and Table 14.

THEORY OF OPERATION

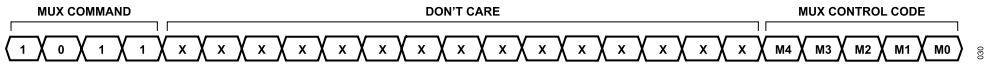


Figure 30. Mux Command

Table 14. Monitor Mux Control Codes

M4	M3	M2	M1	M0	MUux Pin Output	Notes
0	0	0	0	0	Disabled (Hi-Z)	
0	0	0	0	1	OUT0 Current Measurement	$I_{OUT0} = I_{FS} \times V_{MUX}/V_{REF}$
0	0	0	1	0	OUT1 Current Measurement	$I_{OUT1} = I_{FS} \times V_{MUX}/V_{REF}$
0	0	0	1	1	OUT2 Current Measurement	$I_{OUT2} = I_{FS} \times V_{MUX}/V_{REF}$
0	0	1	0	0	OUT3 Current Measurement	$I_{OUT3} = I_{FS} \times V_{MUX}/V_{REF}$
0	0	1	0	1	OUT4 Current Measurement	$I_{OUT4} = I_{FS} \times V_{MUX}/V_{REF}$
0	0	1	1	0	V_{CC}	
0	1	0	0	0	V_{REF}	
0	1	0	0	1	V_{REFLO}	DAC Reference GND
0	1	0	1	0	Die Temperature, T_J	$T_J = 25°C + (1.4\ V - V_{MUX})/(0.0037\ V/°C)$
1	0	0	0	0	V_{DD0}	
1	0	0	0	1	V_{DD1}	
1	0	0	1	0	V_{DD2}	
1	0	0	1	1	V_{DD3}	
1	0	1	0	0	V_{DD4}	
1	0	1	0	1	V^+	
1	0	1	1	0	V^-	
1	0	1	1	1	GND	
1	1	0	0	0	OUT0 Pin Voltage	
1	1	0	0	1	OUT1 Pin Voltage	
1	1	0	1	0	OUT2 Pin Voltage	
1	1	0	1	1	OUT3 Pin Voltage	
1	1	1	0	0	OUT4 Pin Voltage	

Current Measurement Using the Mux

Measure the current of any output pin by using the **mux** command (1011b) along with one of the mux current measurement codes from Table 14. The mux responds by outputting a voltage proportional to the actual output current. The proportionality factor is given by the following equation:

$$I_{OUTX} = I_{FS} \times V_{MUX}/V_{REF} \quad (1)$$

The V_{MUX} pin voltage has the same excellent linearity as the current outputs, but calibrating for slope error (±15% FSR) is necessary for accurate results. ±1% FSR accuracy is easily achievable with a one- or two-point calibration.

Note that for a given V_{REF} and DAC code, V_{MUX} is constant and does not vary by range; but full-scale current I_{FS} has a different value for each output range. If the channel's range is set to Hi-Z or Short-to-V^-, or if it is in dropout (flagged by fault register bits FR0 to FR4), the voltage is not representative of the pin current.

Die Temperature Measurement Using the Mux

Measure the die temperature by using the **mux** command along with mux control code 01010b. The V_{MUX} pin voltage in this case is linearly related to the die temperature by a temperature coefficient of –3.7 mV/°C. The measured junction temperature T_J is then

$$T_J = 25°C + (1.4\ V - V_{MUX})/(3.7\ mV/°C) \quad (2)$$

If needed, the temp monitor can be calibrated by measuring the initial temperature and voltage, and then substituting these values for 25°C and 1.4 V, respectively, in the equation.

Monitor Mux Pre-Charge Considerations

The analog multiplexer in the LTC2662 is unbuffered. This obviates error terms from amplifier offsets; but without buffers, the high-impedance current outputs could be disturbed due to charge transfer at the moment when the MUX pin is connected. The LTC2662 contains circuitry that suppresses charging glitches on the output pins (OUT0 to OUT4) by pre-charging the MUX pin before connecting it to the output.

THEORY OF OPERATION

Due to the pre-charge behavior, the mux output becomes valid approximately 7 µs after the **mux** command is given ($\overline{CS}$/LD rising). Residual charging transients can be further reduced by adding capacitance to the output pins if needed. Do not add capacitance to the MUX pin, as this potentially increases the disturbance to the outputs during mux switching. Up to 100 pF on the MUX pin is allowable.

TOGGLE OPERATIONS

Some systems require that the DAC outputs switch repetitively between two output levels (i.e. switching between an on and off state). The LTC2662 toggle function facilitates these kinds of operations by providing two input registers (A and B) per DAC channel.

Toggling between A and B is controlled by three signals. The first of these is the **toggle select** command, which acts on the data field of 5 bits, each of which controls a single channel (see Figure 31). The second is the **global toggle** command, which controls all selected channels using the global toggle bit TGB (see Figure 32). Finally, the TGP pin allows the use of an external clock or logic signal to toggle the DAC outputs between A and B. The signals from these controls are combined as shown in Figure 33.

If the toggle function is not needed, tie TGP (Pin 2) to ground and leave the toggle select register in its power-on reset state (cleared to zero). Input registers A then function as the sole input registers, and registers B are not used.

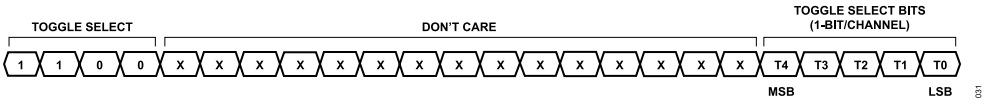


Figure 31. Toggle Select Syntax

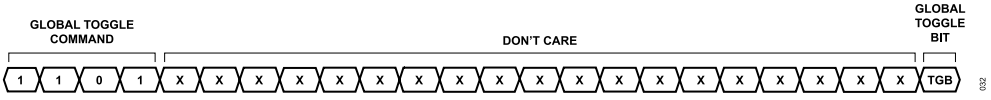


Figure 32. Global Toggle Syntax

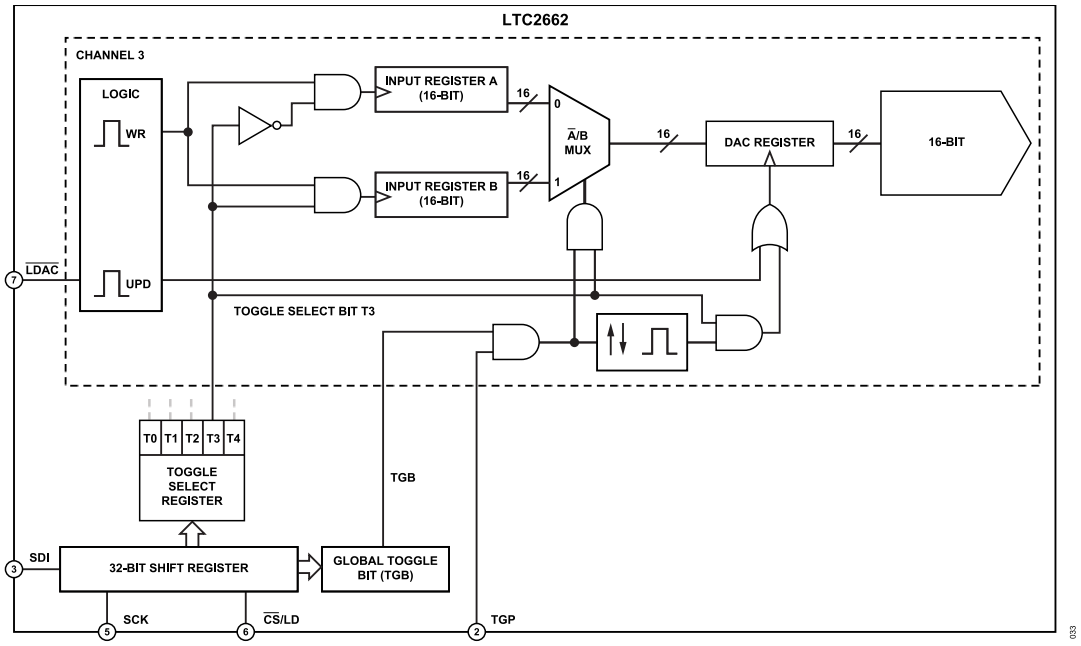


Figure 33. Conceptual Block Diagram—Toggle Functionality

THEORY OF OPERATION

Toggle Select Register (TSR)

The **toggle select** command (1100b) syntax is shown in Figure 31. Each bit in the 5-bit TSR data field controls the DAC channel of the same name: T0 controls channel 0, T1 channel 1… and T4 controls channel 4.

The toggle select bits (T0, T1… T4) have a dual function. First, each toggle select bit controls which input register (A or B) receives data from a write-code operation. When the toggle select bit of a given channel is high, write-code operations are directed to input register B of the addressed channel. When the bit is low, write-code operations are directed to input register A. Secondly, each toggle select bit enables the corresponding channel for a toggle operation.

Writing to Input Registers A and B

Having chosen channels to toggle, write the desired codes to input registers A for the chosen channels; then set the channels toggle select bits using the **toggle select** command; and finally, write the desired codes to input registers B. Once these steps are completed, the channels are ready to toggle. For example, to set up channel 3 to toggle between codes 4096 and 4200:

1. Write code channel 3 (code = 4096) to register A

   00000011 00010000 00000000
2. Toggle select (set bit T3)

   11000000 00000000 00001000
3. Write code channel 3 (code = 4200) to register B

   00000011 00010000 01101000

The write code of step (3) is directed to register B because in step (2), bit T3 was set to 1. Channel 3 now has input registers A and B holding the two desired codes, and is prepared for the toggle operation.

Note: After writing to register B, the code for register A can still be changed. The state of the Toggle Select bit determines to which register (A or B) a write is directed.

First, toggle select bit T3 has to be reset to 0:

11000000 00000000 00000000

Then write the new register A code. Let's say the new code is 4300, so the instruction would be:

00000011 00010000 11001100

After that, set toggle select bit T3 to 1 again [step 2 above]. It is not necessary to write to register B again; channel 3 is ready for the toggle operation.

Toggling Between Registers A and B

Once input registers A and B have been written to for all desired channels and the corresponding toggle-select bits are set high, as in the previous example, the channels are ready for toggling.

The LTC2662 supports three types of toggle operations: a first in which all selected channels are toggled together using the SPI port; a second in which all selected channels are toggled together using an external clock or logic signal; and a third in which any combination of channels can be instructed to update from either input register A or B.

The internal toggle-update circuit is edge triggered, so only transitions (of TGB or TGP) trigger an update from the respective input register.

To toggle all selected channels together using the SPI port, ensure the TGP pin is high and that the bits in the toggle select register corresponding to the desired channels are also high. Use the global command (1101b) to alternate codes, sequentially changing the global toggle bit TGB (see Figure 32). Changing TGB from 1 to 0 updates the DAC registers from their respective input registers A. Changing TGB from 0 to 1 updates the DAC registers from their respective input registers B. Note that in this way up to 5 channels may be toggled with just one serial command.

To toggle all selected channels using an external logic signal, ensure that the TGB bit in the global toggle register is high and that in the toggle select register, the bits corresponding to the desired channels are also high. Apply a clock or logic signal to the TGP pin to alternate codes. TGP falling edges update the DAC registers from their associated input registers A. TGP rising edges update the DAC registers from their associated input registers B. Note that once the input registers are set up, all toggling is triggered by the signal applied to the TGP pin, with no further SPI instructions needed.

To cause any combination of channels to update from either input register A or B, ensure the TGP pin is high and that the TGB bit in the global toggle register is also high. Using the **toggle select** command set the toggle select bits as needed to select the input register (A or B) with which each channel is to be updated. Then update all channels, either by using the serial command (1001b) or by applying a negative pulse to the $\overline{\text{LDAC}}$ pin. Any channels whose toggle select bits are 0 update from input register A, while channels whose toggle select bits are 1 update from input register B (see Figure 33). By alternating toggle select and update operations, up to 5 channels can be simultaneously switched to A or B as needed.

THEORY OF OPERATION

DAISY-CHAIN OPERATION

The serial output of the shift register appears at the SDO pin. Data transferred to the device from the SDI input is delayed 32 SCK rising edges before being output at the next SCK falling edge, suitable for clocking into the microprocessor on the next 32 SCK rising edges.

The SDO output can be used to facilitate control of multiple serial devices from a single 3-wire serial port (i.e. SCK, SDI and $\overline{CS}$/LD). Such a daisy-chain series is configured by connecting the SDO of each upstream device to the SDI of the next device in the chain. The shift registers of the devices are thus connected in series, effectively forming a single input shift register which extends through the entire chain. Because of this, the devices can be addressed and controlled individually by simply concatenating their input words; the first instruction addresses the last device in the chain and so forth. The SCK and $\overline{CS}$/LD signals are common to all devices in the series.

In use, $\overline{CS}$/LD is first taken low. Then, the concatenated input data is transferred to the chain, using the SDI of the first device as the data input. When the data transfer is complete, $\overline{CS}$/LD is taken high, completing the instruction sequence for all devices simultaneously. A single device can be controlled by using the **no-operation** command (1111b) for all other devices in the chain. When $\overline{CS}$/LD is taken high, the SDO pin presents a high impedance out-put, so a pull-up resistor is required at the SDO of each device (except the last) for daisy-chain operation.

ECHO READBACK

The SDO pin can be used to verify data transfer to the device. During each 32-bit instruction cycle, SDO outputs the previous 32-bit instruction for verification. The 8-bit don't-care prefix is replaced by 8 Fault Register status bits, followed by the 4-bit command and address words and the full 16-bit data word (see Figure 4). The SDO sequence for a 24-bit instruction cycle is the same, except that the data word is truncated to 8 bits (see Figure 5). When $\overline{CS}$/LD is high, SDO presents a high impedance output, releasing the bus for use by other SPI devices.

FAULT REGISTER (FR)

The LTC2662 provides notifications of operational fault conditions. The fault register (FR) status bits comprise the first data byte (8 bits) of each 24- or 32-bit SDO word, outputted to the SDO pin during every SPI transaction. See Figure 4 and Figure 5 for sequences.

An FR bit is set when its trigger condition is detected, and clocked to SDO during the next SPI transaction. FR information is updated with each SPI transaction. Note that if a fault condition is corrected by the action of an SPI instruction, the cleared FR flag for that condition is observable at SDO on the next SPI transaction.

Table 15 lists the FR bits and their associated trigger conditions.

Table 15. Fault Register (FR)

FR Bit	Fault Condition
FR0	Open-Circuit condition detected on OUT0
FR1	Open-Circuit condition detected on OUT1
FR2	Open-Circuit condition detected on OUT2
FR3	Open-Circuit condition detected on OUT3
FR4	Open-Circuit condition detected on OUT4
FR5	Overtemperature. If die temperature T_J > 175°C, FR5 is set and thermal protection is activated. Can be disabled using the **Config** command (0111b).
FR6	Power Limit. If $V_{DDX} - V_{OUTX}$ > 10 V and the current range is ≥ 200 mA, FR6 is set and the range for that channel is reduced to 100 mA. Can be disabled using the **Config** command (0111b).
FR7	Invalid SPI sequence length. Valid sequence lengths are 24, 32, and multiples of 32 bits. For all other lengths, FR7 is set and the SPI instruction is ignored.

Fault Indicator Pin ($\overline{FAULT}$)

The $\overline{FAULT}$ pin is an open-drain N-channel output that pulls low when a fault condition is detected. It is released on the next rising $\overline{CS}$/LD edge. The pin is an open-drain output suitable for wired-OR connection to an interrupt bus; a pull-up resistor on the bus is required.

Fault Conditions and Thermal Overload Protection

There are four types of fault conditions that cause the $\overline{FAULT}$ pin to pull low. First, FR0 to FR4 flag an open-circuit (OC) condition on any of the output pins (OUT0 to OUT4, respectively) when an output channel enters dropout due to insufficient voltage from V_{DDx} to OUTx. Independent open-circuit detection is provided for each of the five DAC current output pins.

FR5 provides a detection flag which is set when the die temperature exceeds 175°C. The overtemperature condition also forces all five DAC channels to power down and the open-drain $\overline{FAULT}$ pin to pull low. FR5 remains set and the device stays in shutdown until the die cools. Below approximately 150°C the DAC channels can be returned to normal operation. Note that a $\overline{CS}$/LD rising edge releases the $\overline{FAULT}$ pin regardless of the die temperature.

Since any DAC channel can source up to 300 mA, die heating potential of the system design should be evaluated carefully. FR6, a power-limit protection flag, is provided to help prevent accidental damage to the current output device(s). The power-limit fault condition is triggered for the 200 mA and 300 mA full-scale current spans when the voltage difference between an output supply pin (V_{DDX}) and its current output pin (OUTX) is ≥10 V.

Finally, FR7 is provided to flag invalid SPI word lengths. Valid word lengths are 24 bits, 32 bits, and integer multiples of 32 bits; any other length causes FR7 to set, the $\overline{FAULT}$ pin to assert, and the instruction itself to be ignored.

THEORY OF OPERATION

CONFIG COMMAND

The Config command has four arguments—OC, PL, TS, and RD (see Figure 34).

Setting the OC bit disables open-circuit detection (FR0 to FR4). Likewise, the PL bit disables power-limit protection (FR6); and the TS bit disables thermal protection (FR5). Use these options with caution, particularly PL and TS.

The RD bit is used to select external-reference operation. The REFCOMP pin must be grounded for external reference use whether the RD bit is set or not.

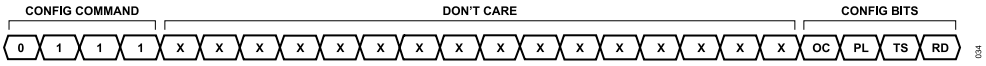


Figure 34. Config Command Syntax: Open-Circuit Detection Disable (OC), Power Limit Protection Disable (PL), Thermal Shutdown Disable (TS), and Reference Disable (RD)

THEORY OF OPERATION

POWER-DOWN MODE

For power-constrained applications, power-down mode can be used to reduce the supply current whenever less than five DAC outputs are needed. When in power-down, the voltage-to-current output drivers and reference buffers are disabled. The current DAC outputs are put into a high impedance state. Register contents are not disturbed during power-down.

Any channel or combination of channels can be put into power-down mode by using command 0100b in combination with the appropriate DAC address. In addition, all the DAC channels and the integrated reference together can be put into power-down using the **power-down chip** command, 0101b. The 16-bit data word is ignored for all power-down commands.

Normal operation resumes by executing any command which includes a DAC update—either in software, as shown in Table 11 or by toggling (see the Toggle Operations section). The selected DAC channel is powered up as it is updated with the new code value. When updating a powered-down DAC, add wait time to accommodate the extra power-up delay. If the channels have been powered down (command 0100b) prior to the update command, the power-up delay time is 30 µs. If, alternatively the chip has been powered down (command 0101b), the power-up delay time is 35 µs.

VALID SUPPLY RANGES

The valid supply ranges for the LTC2662 have several restrictions as described in the Table 5 and the Pin Functions section. The voltage at V^+ (Pin 27) must be greater than or equal to all other supply voltages. V^+ is allowed to be up to 33 V above V^-. The five output supplies (V_{DD0} to V_{DD4}) may be independently set between 2.85 V and V^+. The negative supply, V^-, may be any voltage between –15.75 V and GND, but note again that V^+ must be no more than 33 V above V^-.

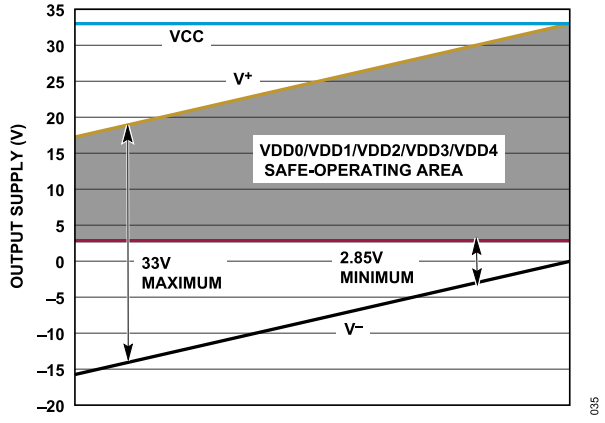


Figure 35. Output Supply Safe Operating Area

CURRENT OUTPUTS

The LTC2662 incorporates a high-gain voltage-to-current converter at each current output pin. INL and DNL are guaranteed for all ranges from 3.125 mA to 300 mA if the minimum dropout voltage ($V_{DDX} – V_{OUTX}$) is met for all DAC codes.

If sufficient dropout voltage is maintained, the DC output impedances of the current outputs (OUT0 to OUT4) are very high. Each current output has a dedicated positive supply pin, V_{DD0} to V_{DD4}, to allow the tailoring of each channel's current compliance and power dissipation.

SWITCH-TO-V^- MODE

Span code 1000b can be used to pull outputs below GND. In Switch-to-V^- mode, the output current is turned off for the addressed channel(s), and the channel voltage V_{OUTX} pulls to V^-. The pulldown switch can sink up to 80 mA at an effective resistance of 12 Ω max.

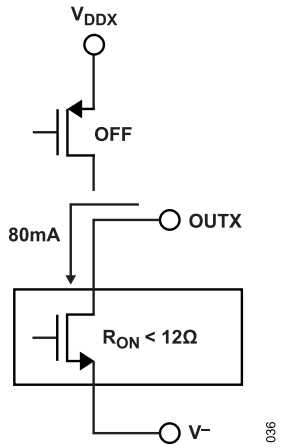


Figure 36. Switch-to-V^- Mode

Switch-to-V^- mode can be invoked with the **write span to all** or **write span to n** command and the desired address. Span codes are shown in Table 13; a diagram of an output in Switch-to-V^- mode is shown in Figure 36.

GAIN ADJUSTMENT USING THE FSADJ PIN

The full-scale output currents are proportional to the reference voltage, and inversely proportional to the resistance associated with FSADJ. That is:

$$I_{OUTFS} \sim V_{REF}/R_{FSADJ} \quad (3)$$

If the FSADJ pin is tied to V_{CC}, the LTC2662 uses an internal R_{FSADJ} = 20 kΩ. Optionally, FSADJ can instead be connected to a grounded external resistor to tune the default current ranges to the application, or for the best possible temperature coefficient using an appropriately-specified precision resistor. Values from 19 kΩ to 41 kΩ are supported. The new current ranges can easily be calculated using the External R_{FSADJ} column of Table 13. The internal resistor is automatically disconnected when using an external resistor.

THEORY OF OPERATION

When using an external resistor, FSADJ is sensitive to stray capacitance; the pin should be compensated with a snubber network consisting of a series combination of 1 kΩ and 1 µF, connected in parallel to R_{FSADJ}. With the recommended compensation, the pin is stable driving stray capacitance of up to 50 pF.

OFFSET CURRENT AND CODE ZERO

The offset current error of the LTC2662 is guaranteed ±0.4%FSR maximum. If the offset of a given channel is positive, some non-zero current flows at code zero; if negative, the current is zero (leakage only) for a range of codes close to zero. Offset and linearity endpoints are measured at code 384 (LTC2662-16) or 24 (LTC2662-12), guaranteeing that the DAC is operating with a measurable output current at the point of measurement.

A channel with a positive offset error may not completely turn off, even at code zero. To turn an output completely off, set the range to Hi-Z (span code 0000b from Table 13), and update the channel.

REFERENCE MODES

The LTC2662 can be used with either an internal or external reference. As with voltage DACs, the reference voltage scales the outputs, so that the outputs reflect any errors in the reference. Full scale output currents are limited to 300 mA maximum per channel regardless of reference voltage.

The internal 1.25 V reference has a typical temperature drift of ±2 ppm/°C and an initial output tolerance of ±2 mV max. It is trimmed, tested and characterized independent of the DACs; and the DACs are tested and characterized with an ideal external reference.

To use the internal reference, the REFCOMP pin should be left floating, with no DC path to GND. In addition, the RD bit in the Config register must have a value of 0. This value is reset to 0 at power-up, or it can be reset using the **config** command, 0111b. Figure 34 shows the command syntax.

For reference stability and low noise, a 0.1 µF capacitor should be tied between REFCOMP and GND. In this configuration, the internal reference can drive up to 0.1 µF with excellent stability. To ensure stable operation, the capacitive load on the REF pin should not exceed that on the REFCOMP pin. A buffer is needed if the internal reference is to drive external circuitry.

To use an external reference, tie the REFCOMP pin to GND. This disables the output of the internal reference at start-up, so that the REF pin becomes a high-impedance input. Apply the reference voltage at the REF pin after powering up. Set the RD bit to 1 using the **config** command, 0111b. The REF input voltage range is 1.225 V to 1.275 V.

BOARD LAYOUT

The excellent load regulation and DC crosstalk performance of these devices is achieved in part by minimizing common-mode resistance of signal and power grounds.

As with any high resolution converter, clean board grounding is important. A low impedance analog ground plane is necessary, as are star-grounding techniques. Keep the board layer used for star-ground continuous to minimize ground resistances; that is, use the star-ground concept without using separate star traces. Resistance from the REFLO pin to the star point should be as low as possible. The exposed pad is recommended as the star ground point.

For best performance, stitch the ground plane with arrays of vias on 150 mil to 200 mil centers connecting it with the ground pours from the other board layers. This reduces the overall ground resistance and minimizes ground loop area.

TYPICAL APPLICATION

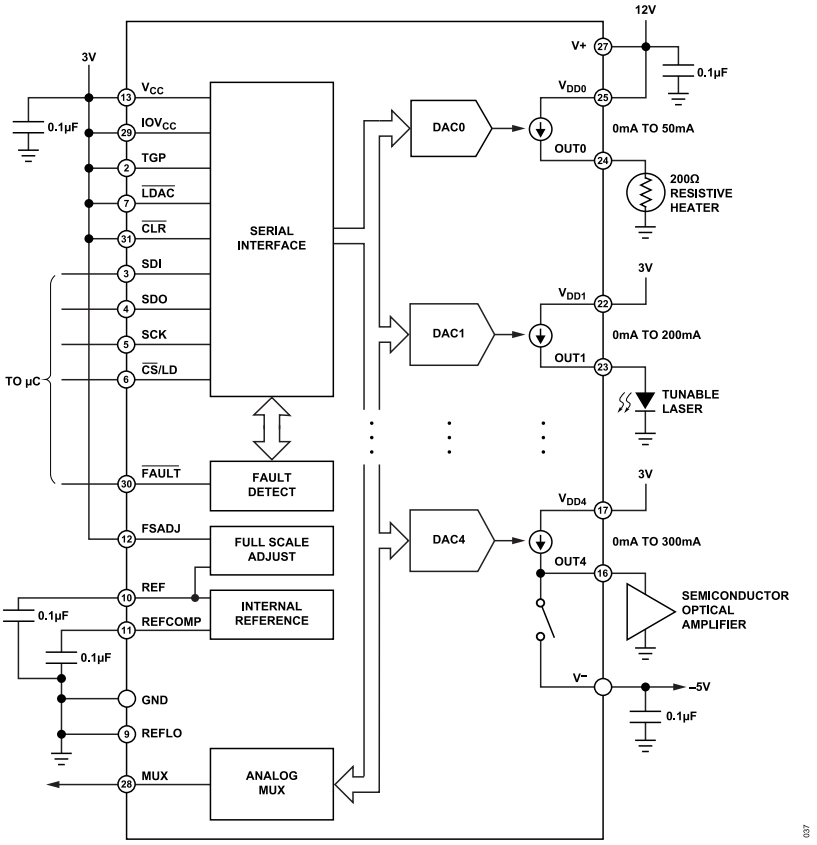


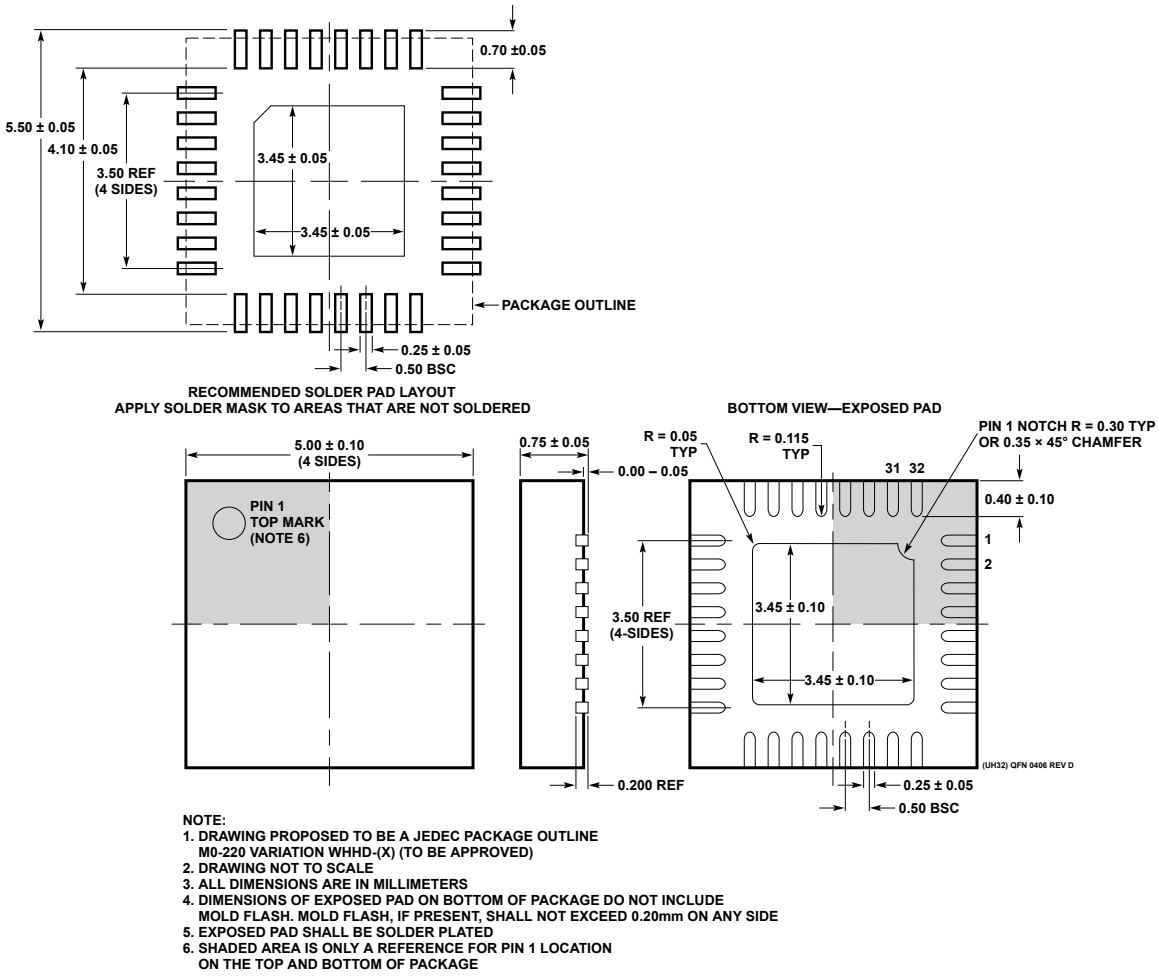
Figure 37. Typical Application Example

RELATED PARTS

Table 16.

Part Number	Description	Comments
LTC2672	Five-Channel, Low Dropout, 300 mA, Current Source Output, 12-/16-Bit SoftSpan DAC	Software-Programmable Current Output Ranges from 3.125 mA to 300 mA with Flexible 2.1 V to 5.5 V Supply Voltage per Channel, 3.5 mm × 3.6 mm WLCSP and 5 mm × 5 mm QFN packages
AD5770R	Six-Channel, 14-Bit, Current Output DAC with On-Chip Reference, SPI Interface	Software-Programmable Output Ranges from −60 mA to +300 mA with Flexible 0.8 V to 5.1 V per Channel, 4 mm × 4 mm QFN package
LTC2668	16-Channel Serial 16-/12-Bit V_{OUT} SoftSpan DACs with ±10 ppm/°C Reference	Software-Programmable Output Ranges Up to ±10 V, 6 mm × 6 mm QFN Package
LTC2666	Octal Serial 16-/12-Bit V_{OUT} SoftSpan DACs with ±10 ppm/°C Reference	Software-Programmable Output Ranges Up to ±10 V, 5 mm × 5 mm QFN Package
LTC2664	Quad Serial 16-/12-Bit V_{OUT} SoftSpan DACs with ±10 ppm/°C Reference	Software-Programmable Output Ranges Up to ±10 V, 5 mm × 5 mm QFN Package
References		
LTC6655	Low Drift Precision Buffered Reference	0.025% Max Tolerance 2 ppm/°C Max, 0.25 ppm_{P-P} 0.1 Hz to 10 Hz Noise
LT6654	Low Drift Precision Buffered Reference	0.05% Maximum Tolerance 10 ppm/°C Maximum, 1.6 ppm_{P-P}, 0.1 Hz to 10Hz Noise

OUTLINE DIMENSIONS



NOTE:
1. DRAWING PROPOSED TO BE A JEDEC PACKAGE OUTLINE
   M0-220 VARIATION WHHD-(X) (TO BE APPROVED)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

Figure 38. 32-Lead Plastic QFN (5 mm × 5 mm)
(Reference LTC DWG # 05-08-1693 Rev D)

Updated: April 15, 2024

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
LTC2662CUH-12#PBF	0°C to +70°C	32-Lead QFN (5mm x 5mm x 0.75mm w/ EP)		05-08-1693
LTC2662CUH-12#TRPBF	0°C to +70°C	32-Lead QFN (5mm x 5mm x 0.75mm w/ EP)	Reel, 2500	05-08-1693
LTC2662CUH-16#PBF	0°C to +70°C	32-Lead QFN (5mm x 5mm x 0.75mm w/ EP)		05-08-1693
LTC2662CUH-16#TRPBF	0°C to +70°C	32-Lead QFN (5mm x 5mm x 0.75mm w/ EP)	Reel, 2500	05-08-1693
LTC2662HUH-12#PBF	-40°C to +125°C	32-Lead QFN (5mm x 5mm x 0.75mm w/ EP)		05-08-1693
LTC2662HUH-12#TRPBF	-40°C to +125°C	32-Lead QFN (5mm x 5mm x 0.75mm w/ EP)	Reel, 2500	05-08-1693
LTC2662HUH-16#PBF	-40°C to +125°C	32-Lead QFN (5mm x 5mm x 0.75mm w/ EP)		05-08-1693
LTC2662HUH-16#TRPBF	-40°C to +125°C	32-Lead QFN (5mm x 5mm x 0.75mm w/ EP)	Reel, 2500	05-08-1693
LTC2662IUH-12#PBF	-40°C to +85°C	32-Lead QFN (5mm x 5mm x 0.75mm w/ EP)		05-08-1693
LTC2662IUH-12#TRPBF	-40°C to +85°C	32-Lead QFN (5mm x 5mm x 0.75mm w/ EP)	Reel, 2500	05-08-1693
LTC2662IUH-16#PBF	-40°C to +85°C	32-Lead QFN (5mm x 5mm x 0.75mm w/ EP)		05-08-1693
LTC2662IUH-16#TRPBF	-40°C to +85°C	32-Lead QFN (5mm x 5mm x 0.75mm w/ EP)	Reel, 2500	05-08-1693

[1] Z = RoHS Compliant Part.

OUTLINE DIMENSIONS

EVALUATION BOARDS

Model[1]	Description
DC2692A-A	Evaluation Board

[1] The DC2692A-A is RoHS compliant.

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