THE DATASHEET OF

LTC3124IDHC#PBF

15V, 5A 2-Phase Synchronous Step-Up DC/DC Converter with Output Disconnect

FEATURES

- **V_{IN} Range: 1.8V to 5.5V, 500mV After Start-Up**
- **Adjustable Output Voltage: 2.5V to 15V**
- **1.5A Output Current for V_{IN} = 5V and V_{OUT} = 12V**
- **Dual-Phase Control Reduces Output Voltage Ripple**
- **Output Disconnects from Input When Shut Down**
- **Synchronous Rectification: Up to 95% Efficiency**
- **Inrush Current Limit**
- Up to 3MHz Programmable Switching Frequency Synchronizable to External Clock
- Selectable Burst Mode® Operation: 25µA I_Q
- Output Overvoltage Protection
- Internal Soft-Start
- <1µA I_Q in Shutdown
- 16-Lead, Thermally- Enhanced 3mm × 5mm × 0.75mm DFN and TSSOP Packages

APPLICATIONS

- RF, Microwave Power Amplifiers
- Piezo Actuators
- Small DC Motors, Thermal Printers
- 12V Analog Rail from Battery, 5V, or Backup Capacitor

DESCRIPTION

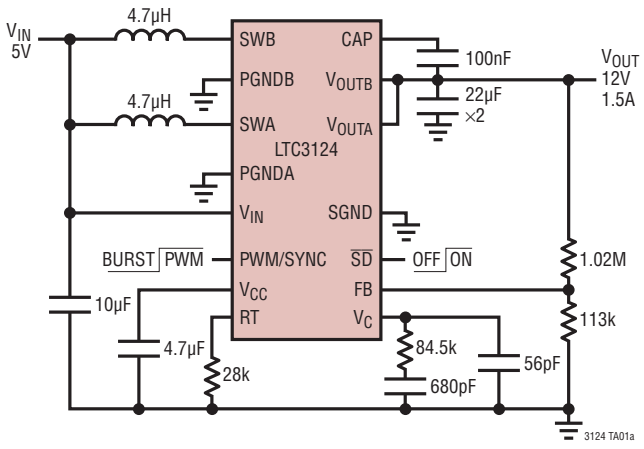
The LTC®3124 is a dual-phase, synchronous step-up DC/DC converter with true output disconnect and inrush current limiting capable of providing output voltages up to 15V. Dual-phase operation significantly reduces peak inductor and capacitor ripple currents, minimizing inductor and capacitor size. The 2.5A per phase current limit, along with the ability to program output voltages up to 15V make the LTC3124 well suited for a variety of demanding applications. Once started, operation will continue with inputs down to 500mV.

The LTC3124 switching frequency can be programmed from 100kHz to 3MHz to optimize applications for highest efficiency or smallest solution footprint. The oscillator can be synchronized to an external clock for noise sensitive applications. Selectable Burst Mode operation reduces quiescent current to 25µA, ensuring high efficiency across the entire load range. An internal soft-start limits inrush current during start-up.

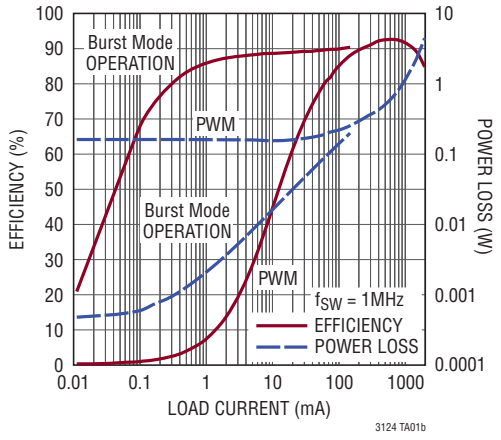
Other features include a <1µA shutdown current and robust protection under short-circuit, thermal overload, and output overvoltage conditions. The LTC3124 is offered in both 16-lead DFN and thermally-enhanced TSSOP packages.

TYPICAL APPLICATION

5V to 12V Synchronous Boost Converter



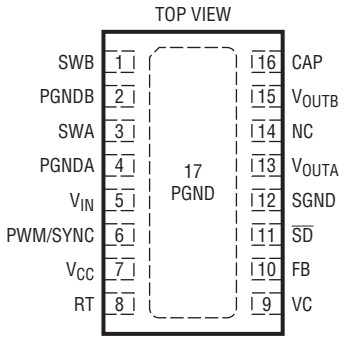
Efficiency Curve



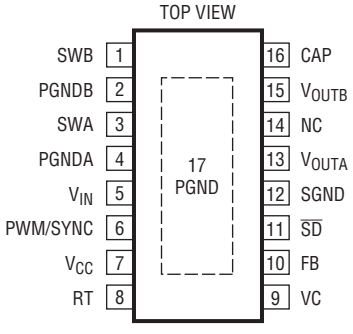
ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{IN} Voltage ..... –0.3V to 6V
V_{OUTA}, V_{OUTB} Voltages ..... –0.3V to 18V
SWA, SWB Voltages (Note 2) ..... –0.3V to 18V
SWA, SWB (Pulsed < 100ns) (Note 2) ..... –0.3V to 19V
VC Voltage ..... –0.3V to V_{CC}
RT Voltage ..... –0.3V to V_{CC}
CAP Voltage
V_{OUT} < 5.7V ..... –0.3V to (V_{OUT} + 0.3V)
5.7V ≤ V_{OUT} ≤ 11.7V ..... (V_{OUT} – 6V) to (V_{OUT} + 0.3V)
V_{OUT} > 11.7V ..... (V_{OUT} – 6V) to 12V
All Other Pins ..... –0.3V to 6V
Operating Junction Temperature Range (Notes 3, 4)
LTC3124E/LTC3124I ..... –40°C to 125°C
LTC3124H ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
FE Package Only ..... 300°C

PIN CONFIGURATION



DHC PACKAGE
16-LEAD (5mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W (NOTE 5), θ_{JC} = 5°C/W
EXPOSED PAD (PIN 17) IS PGND AND MUST BE SOLDERED TO PCB
FOR RATED THERMAL PERFORMANCE



FE PACKAGE
16-LEAD PLASTIC TSSOP
T_{JMAX} = 150°C, θ_{JA} = 40°C/W (NOTE 5), θ_{JC} = 10°C/W
EXPOSED PAD (PIN 17) IS PGND AND MUST BE SOLDERED TO PCB
FOR RATED THERMAL PERFORMANCE

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3124EDHC#PBF	LTC3124EDHC#TRPBF	3124	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3124IDHC#PBF	LTC3124IDHC#TRPBF	3124	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3124EFE#PBF	LTC3124EFE#TRPBF	3124FE	16-Lead Plastic TSSOP	–40°C to 125°C
LTC3124IFE#PBF	LTC3124IFE#TRPBF	3124FE	16-Lead Plastic TSSOP	–40°C to 125°C
LTC3124HFE#PBF	LTC3124HFE#TRPBF	3124FE	16-Lead Plastic TSSOP	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 3). V_{IN} = 3.6V, V_{OUTA} = V_{OUTB} = 12V, R_T = 28k unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Start-Up Voltage	V_{OUT} = 0V	●		1.6	1.8	V
Input Voltage Range	V_{OUT} ≥ 2.5V	●	0.5		5.5	V
Output Voltage Adjust Range		●	2.5		15	V
Feedback Voltage		●	1.176	1.200	1.224	V
Feedback Input Current	FB = 1.4V			1	50	nA
Quiescent Current, Shutdown	$\overline{SD}$ = 0V, V_{OUT} = 0V, Not Including Switch Leakage			0.2	1	µA
Quiescent Current, Active	FB = 1.4V, Measured on V_{IN}, Non-Switching			600	840	µA
Quiescent Current, Burst	Measured on V_{IN}, FB = 1.4V Measured on V_{OUT}, FB = 1.4V			25 10	40 20	µA µA
N-Channel MOSFET Switch Leakage Current	SW = 15V, V_{OUT} = 15V, Per Phase	●		0.1	40	µA
P-Channel MOSFET Switch Leakage Current	SW = 0V, V_{OUT} = 15V, $\overline{SD}$ = 0V, Per Phase	●		0.1	70	µA
N-Channel MOSFET Switch On-Resistance	Per Phase			0.130		Ω
P-Channel MOSFET Switch On-Resistance	Per Phase			0.200		Ω
N-Channel MOSFET Peak Current Limit	Per Phase	●	2.5	3.5	4.5	A
Maximum Duty Cycle	FB = 1.0V	●	90	94		%
Minimum Duty Cycle	FB = 1.4V	●			0	%
Switching Frequency	Per Phase	●	0.83	1	1.17	MHz
SYNC Frequency Range		●	0.2		6.0	MHz
PWM/SYNC Input High Voltage		●	0.9 • V_{CC}			V
PWM/SYNC Input Low Voltage		●			0.1 • V_{CC}	V
PWM/SYNC Input Current	$V_{PWM/SYNC}$ = 5.5V			0.01	1	µA
CAP Clamp Voltage	V_{OUT} > 6.2V, Referenced to V_{OUT}		–5.0	–5.4	–5.8	V
V_{CC} Regulation Voltage	V_{IN} < 2.8V, V_{OUT} > 5V		3.9	4.25	4.6	V
Error Amplifier Transconductance		●	60	100	130	µS
Error Amplifier Sink Current	FB = 1.6V, VC = 1.15V			25		µA
Error Amplifier Source Current	FB = 800mV, VC = 1.15V			–25		µA
Soft-Start Time				10		ms
$\overline{SD}$ Input High Voltage		●	1.6			V
$\overline{SD}$ Input Low Voltage		●			0.25	V
$\overline{SD}$ Input Current	$\overline{SD}$ = 5.5V			1	2	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Voltage transients on the SW pin beyond the DC limit specified in the Absolute Maximum Ratings are non-disruptive to normal operations when using good layout practices, as shown on the demo board or described in the data sheet or application notes.

Note 3: The LTC3124 is tested under pulsed load conditions such that $T_A \approx T_J$. The LTC3124E is guaranteed to meet performance specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3124I is guaranteed to meet specifications over the –40°C to 125°C operating junction temperature range. The LTC3124H is guaranteed to meet specifications over the full –40°C to 150°C operating junction range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C.

Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} is the thermal impedance of the package.

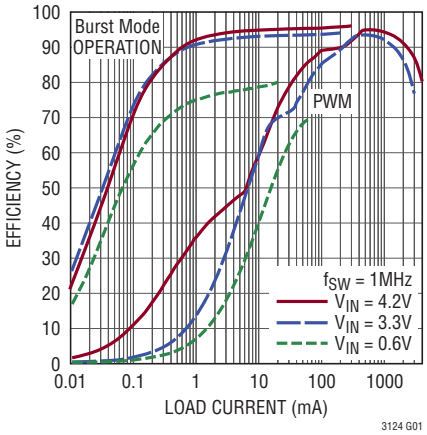
Note 4: The LTC3124 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature shutdown is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

Note 5: Failure to solder the exposed backside of the package to the PC board ground plane will result in a thermal impedance much higher than the rated package specifications.

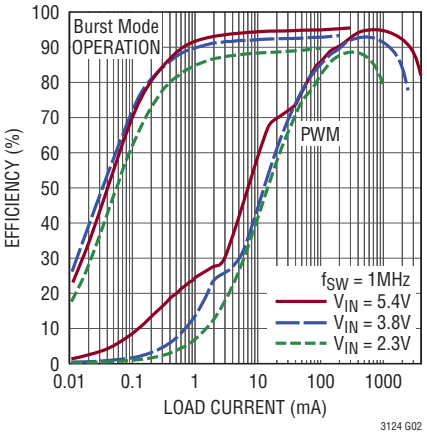
TYPICAL PERFORMANCE CHARACTERISTICS

Configured as front page application at T_A = 25°C, unless otherwise specified.

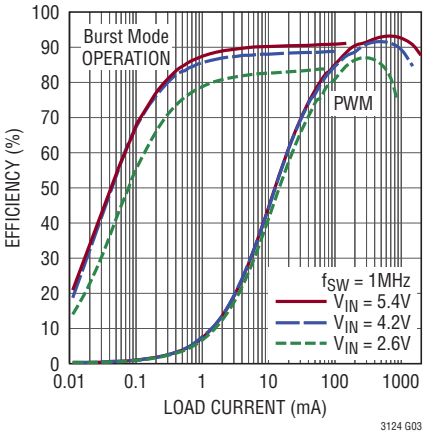
Efficiency vs Load Current, V_{OUT} = 5V



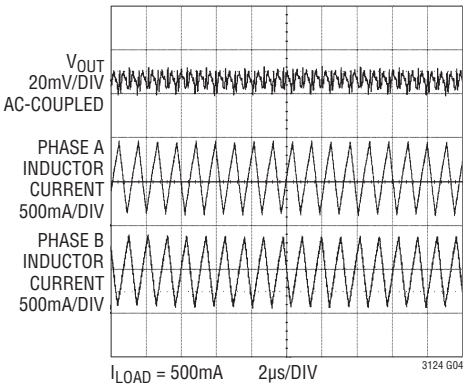
Efficiency vs Load Current, V_{OUT} = 7.5V



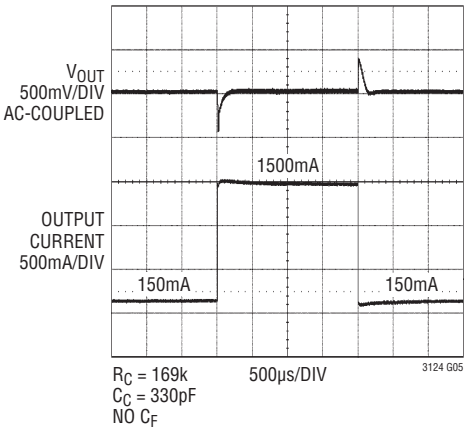
Efficiency vs Load Current, V_{OUT} = 12V



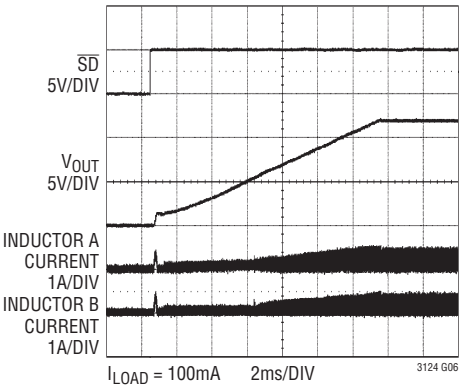
PWM Mode Operation



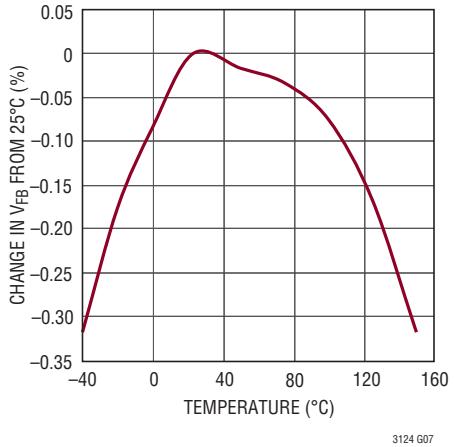
Load Transient Response



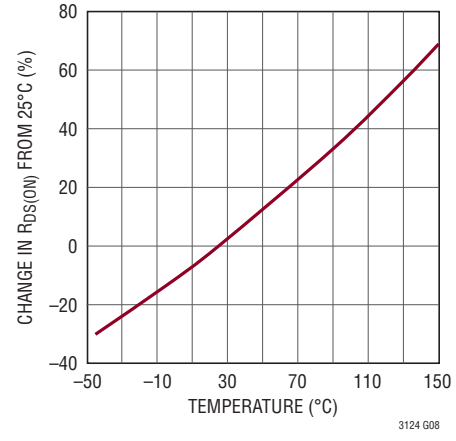
Inrush Current Control



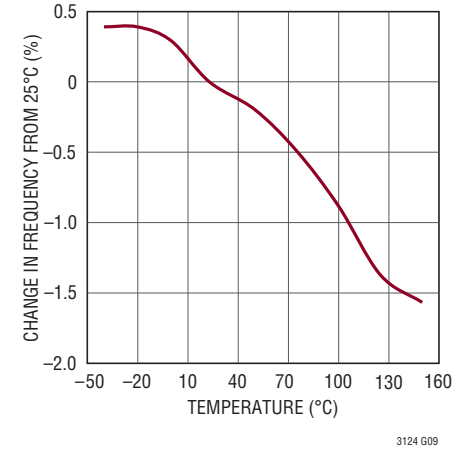
Feedback vs Temperature



$R_{DS(ON)}$ vs Temperature, Both NMOS and PMOS



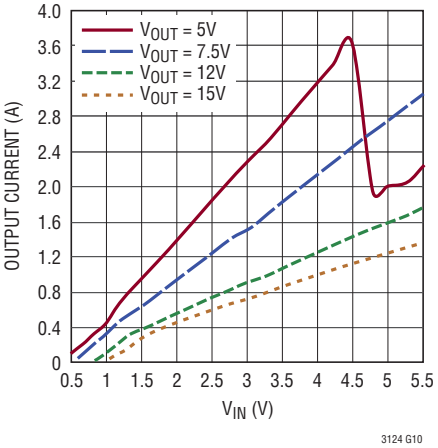
Switching Frequency vs Temperature



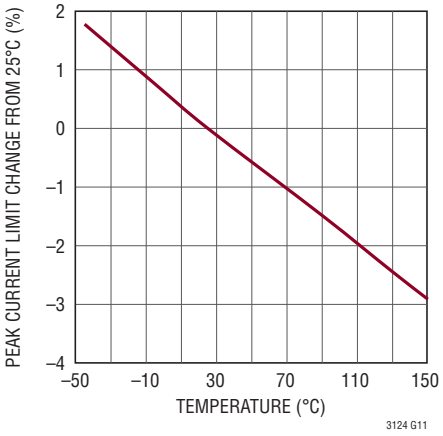
TYPICAL PERFORMANCE CHARACTERISTICS

Configured as front page application at T_A = 25°C, unless otherwise specified.

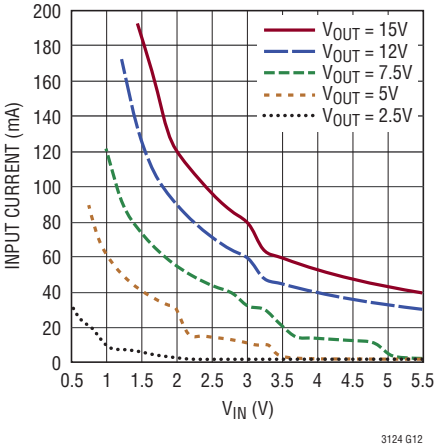
PWM Mode Maximum Output Current vs V_{IN}



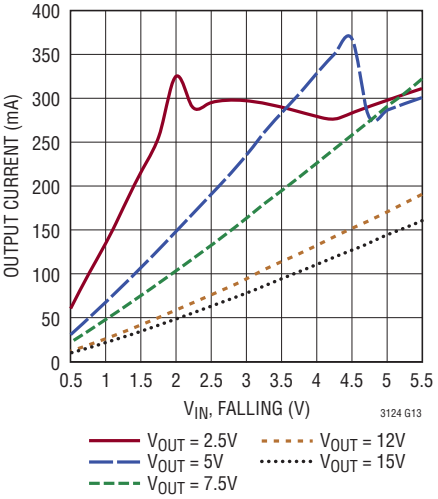
Peak Current Limit Change vs Temperature



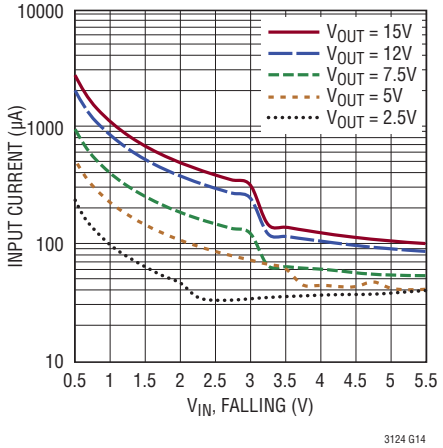
PWM Operation No-Load Input Current vs V_{IN}



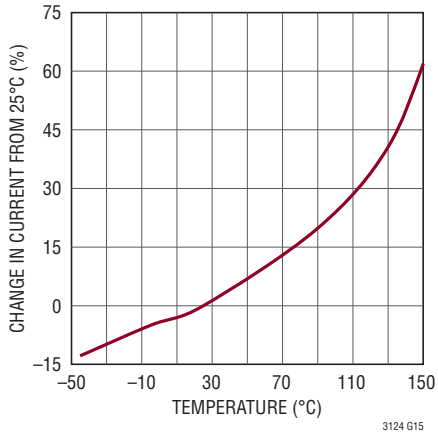
Burst Mode Output Current vs V_{IN}



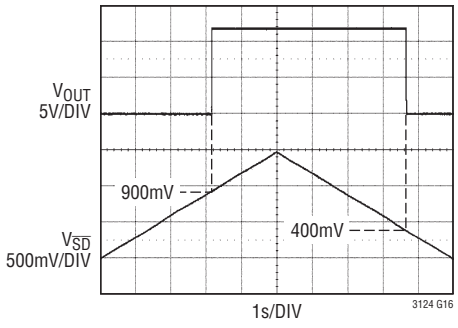
Burst Mode No-Load Input Current vs V_{IN}



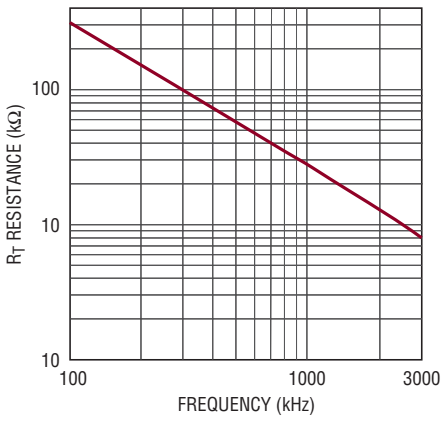
Burst Mode Quiescent Current Change vs Temperature



$\overline{SD}$ Pin Threshold



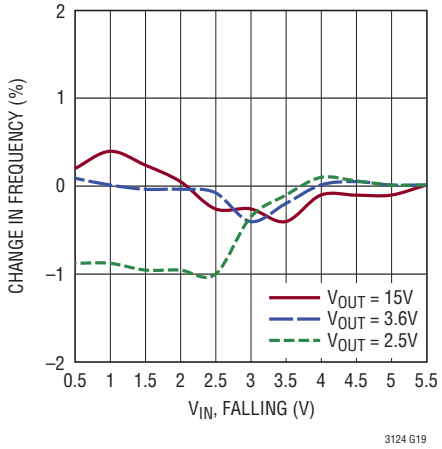
RT vs Frequency



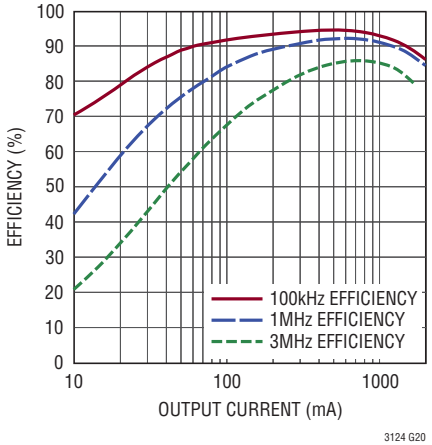
TYPICAL PERFORMANCE CHARACTERISTICS

Configured as front page application at T_A = 25°C, unless otherwise specified.

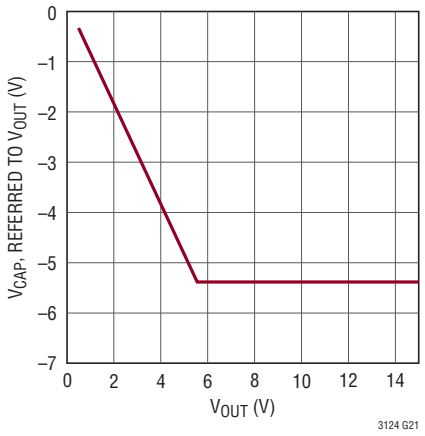
Frequency Accuracy



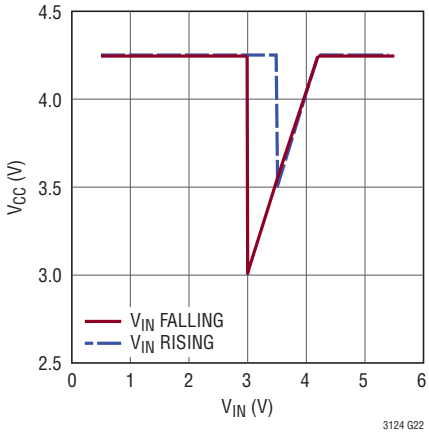
Efficiency vs Frequency



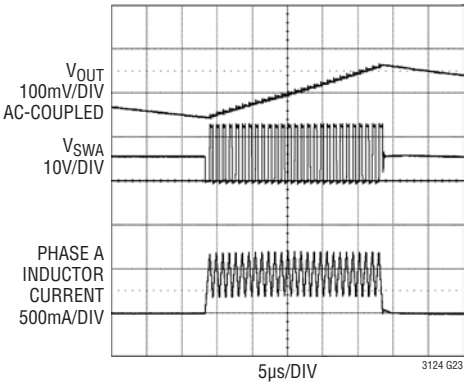
CAP Pin Voltage vs V_{OUT}



V_{CC} vs V_{IN}

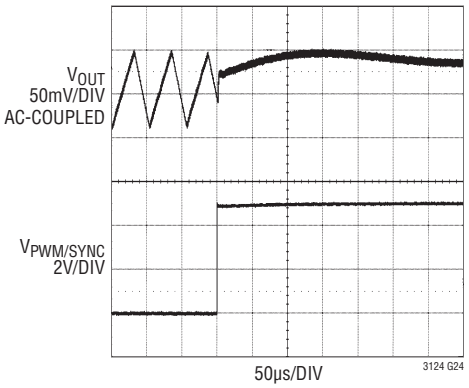


Burst Mode Operation



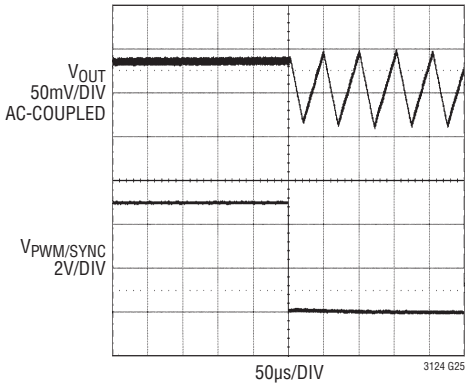
OUTPUT CURRENT = 50mA

Burst Mode Operation to PWM Mode



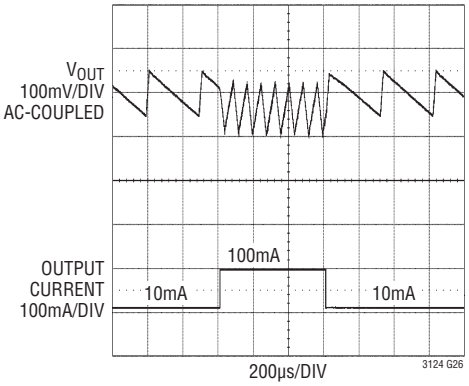
OUTPUT CURRENT = 100mA
TYPE III COMPENSATION—SEE FIGURE 10 FOR COMPONENT VALUES

PWM Mode to Burst Mode Operation

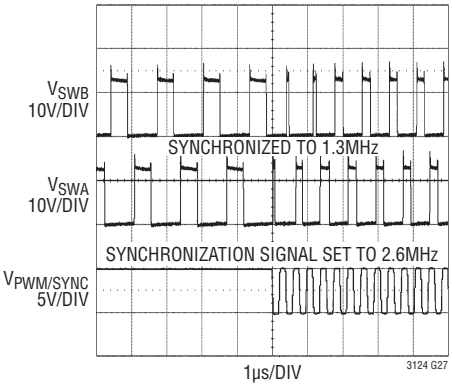


OUTPUT CURRENT = 100mA
TYPE III COMPENSATION—SEE FIGURE 10 FOR COMPONENT VALUES

Burst Mode Transient



Synchronized Operation

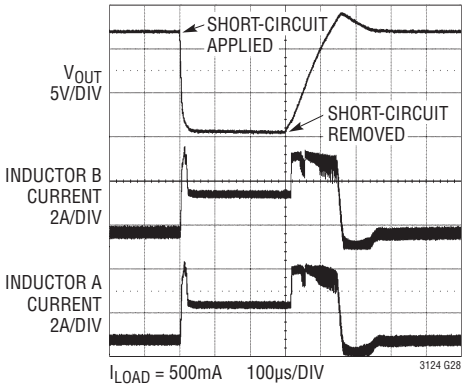


OUTPUT CURRENT = 1A

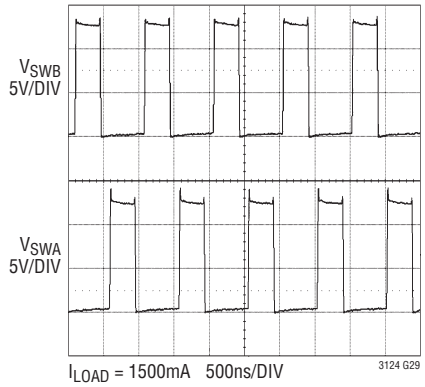
TYPICAL PERFORMANCE CHARACTERISTICS

Configured as front page application at T_A = 25°C, unless otherwise specified.

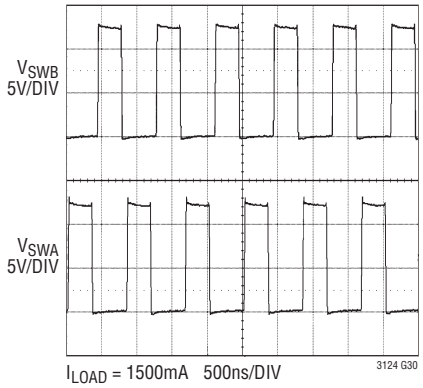
Short-Circuit Response



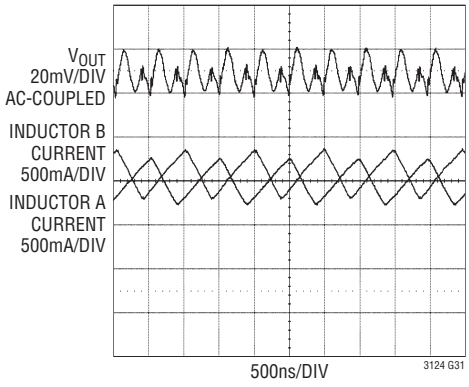
SWA and SWB at 1MHz/Phase



SW Pins while Synchronizing to 1.2MHz



Output Voltage Ripple at 1.5A Load with Two 10µF Ceramic Capacitors



PIN FUNCTIONS

SWB, SWA (Pin 1, Pin 3): Phase B and Phase A Switch Pins. Connect inductors from these pins to the input supply. Keep PCB trace lengths as short and wide as possible to reduce EMI and voltage overshoot. When $V_{OUT} \geq V_{IN}$ + 2V, internal anti-ringing resistors are connected between V_{IN} and both SWA and SWB after their respective inductor currents have dropped to near zero, to minimize EMI. These anti-ringing resistors are also activated in shutdown and during the sleep periods of Burst Mode operation.

PGNDB, PGNDA, PGND (Pin 2, Pin 4, Exposed Pad Pin 17): Power Ground. When laying out your PCB, provide a short, direct path between PGND and the output capacitors and tie directly to the ground plane. ***The exposed pad is ground and must be soldered to the PCB ground plane for rated thermal and electrical performance.***

V_{IN} (Pin 5): Input Supply Pin. The device is powered from V_{IN} if V_{IN} is initially greater than approximately 3.5V, with V_{IN} continuing to supply the device down to approximately 3V; otherwise the greater of V_{IN} and V_{OUT} supplies the

PIN FUNCTIONS

device. Place a low ESR ceramic bypass capacitor of at least 10µF from V_{IN} to PGND. X5R and X7R dielectrics are preferred for their superior voltage and temperature characteristics.

PWM/SYNC (Pin 6): Burst Mode Operation Select and Oscillator Synchronization. ***Do not leave this pin floating.***

- PWM/SYNC = High. Disable Burst Mode operation and maintain low noise, constant frequency operation.
- PWM/SYNC = Low. The converter operates in Burst Mode, independent of load current.
- PWM/SYNC = External CLK. The internal oscillator is synchronized to the external CLK signal. Burst Mode operation is disabled. A clock pulse width of 100ns minimum is required to synchronize the oscillator. An external resistor MUST BE connected between R_T and SGND to program the oscillator slightly below the desired synchronization frequency.

In non-synchronized applications, repeated clocking of the PWM/SYNC pin to affect an operating mode change is supported with these restrictions:

- Boost Mode ($V_{OUT} > V_{IN}$): $I_{OUT} < 3mA$: $f_{PWM/SYNC} \leq 10Hz$, $I_{OUT} \geq 3mA$: $f_{PWM/SYNC} \leq 5kHz$.
- Buck Mode ($V_{OUT} < V_{IN}$): $I_{OUT} < 5mA$: $f_{PWM/SYNC} \leq 2.5Hz$, $I_{OUT} \geq 5mA$: $f_{PWM/SYNC} \leq 5kHz$.

V_{CC} (Pin 7): V_{CC} Regulator Output. Connect a low ESR filter capacitor of at least 4.7µF from this pin to SGND to provide a regulated rail approximately equal to the lower of V_{IN} and 4.25V. When V_{OUT} is higher than V_{IN}, and V_{IN} falls below 3V, V_{CC} will regulate to the lower of approximately V_{OUT} and 4.25V. A UVLO event occurs if V_{CC} drops below 1.5V, typical. Switching is inhibited, and a soft-start is initiated when V_{CC} returns above 1.6V, typical.

RT (Pin 8): Frequency Adjust Pin. Connect to SGND through an external resistor (R_T) to program the oscillator frequency according to the formula:

$$f_{OSC} \cong \frac{56}{R_T}$$

$$f_{SWITCH} = \frac{f_{OSC}}{2} \cong \frac{28}{R_T}$$

where f_{OSC} is in MHz and R_T is in kΩ.

VC (Pin 9): Error Amplifier Output. A frequency compensation network is connected from this pin to SGND to compensate the control loop. See Compensating the Feedback Loop section for guidelines.

FB (Pin 10): Feedback Input to the Error Amplifier. Connect the resistor divider tap to this pin. Connect the top of the divider to V_{OUT} and the bottom of the divider to SGND. The output voltage can be adjusted from 2.5V to 15V according to the formula:

$$V_{OUT} = 1.2V \bullet \left(1 + \frac{R1}{R2}\right)$$

$\overline{SD}$ (Pin 11): Logic Controlled Shutdown Input. Pulling this pin above 1.6V enables normal, free-running operation. Forcing this pin below 0.25V shuts the LTC3124 off, with quiescent current below 1µA. ***Do not leave this pin floating.***

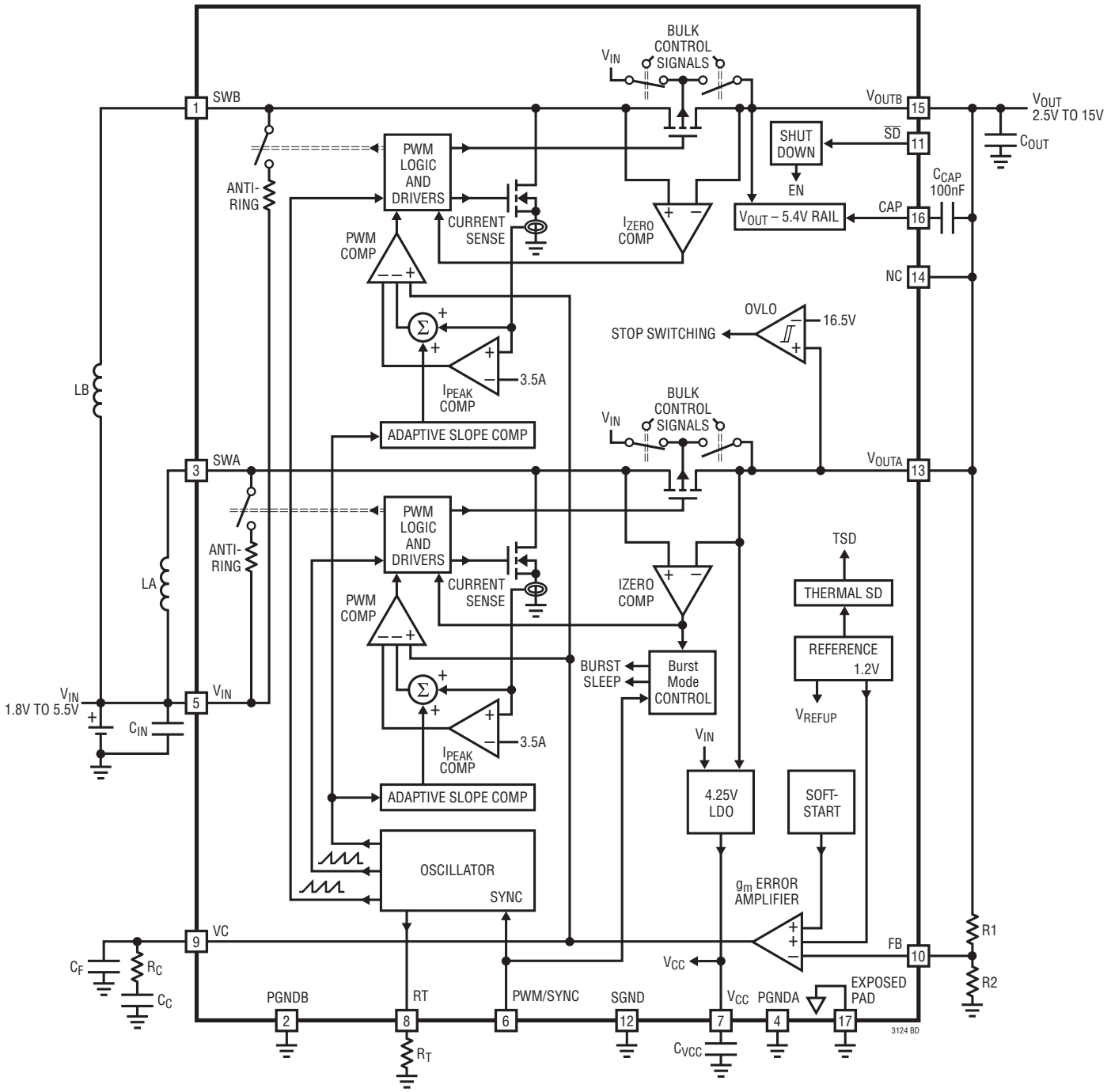
SGND (Pin 12): Signal Ground. When laying out your PC board, provide a short, direct path between SGND and the ground referenced sides of all the appropriate components connecting to pins RT, VC, and FB.

V_{OUTA}, V_{OUTB} (Pin 13, Pin 15): Output Voltage Senses and the Source of the Internal Synchronous Rectifier MOSFETs. Driver bias is derived from V_{OUT}. Connect the output filter capacitor from V_{OUT} to PGND, close to the IC. A minimum value of 10µF ceramic per phase is recommended. V_{OUT} is disconnected from V_{IN} when $\overline{SD}$ is low. ***V_{OUTA} and V_{OUTB} must be tied together.***

NC (Pin 14): No Connect. Not connected internally. Connect this pin to V_{OUTA}/V_{OUTB} to provide a wider V_{OUT} copper plane on the printed circuit board.

CAP (Pin 16): Serves as the Low Reference for the Synchronous Rectifiers Gate Drives. Connect a low ESR filter capacitor (typically 100nF) from this pin to V_{OUT} to provide an elevated ground rail, approximately 5.4V below V_{OUT}, used to drive the synchronous rectifiers.

BLOCK DIAGRAM



OPERATION

The LTC3124 is a dual-phase, adjustable frequency (100kHz to 3MHz) synchronous boost converter housed in either a 16-lead 5mm × 3mm DFN or a thermally-enhanced TSSOP package. The LTC3124 offers the unique ability to start up from inputs as low as 1.8V and continue to operate from inputs as low as 0.5V, for output voltages greater than 2.5V. The device also features fixed frequency, current mode PWM control for exceptional line and load regulation. The current mode architecture with adaptive slope compensation provides excellent load transient response and requires minimal output filtering. An internal 10ms soft-start limits inrush current during start-up and simplifies the design process while minimizing the number of external components.

With its low $R_{DS(ON)}$ and low gate charge internal N-channel MOSFET switches and P-channel MOSFET synchronous rectifiers, the LTC3124 achieves high efficiency over a wide range of load current. High efficiency is achieved at light loads by utilizing Burst Mode operation. Operation can be best understood by referring to the Block Diagram.

MULTIPHASE OPERATION

The LTC3124 uses a dual-phase architecture, rather than the conventional single phase of other boost converters. By having two phases equally spaced 180° apart, not only is the output ripple frequency increased by a factor of two, but the output capacitor ripple current is significantly reduced. Although this architecture requires two inductors, rather than a single inductor, there are a number of important advantages.

- Substantially lower peak inductor current allows the use of smaller, lower cost inductors.
- Significantly reduced output ripple current minimizes output capacitance requirement.
- Higher frequency output ripple is easier to filter for low noise applications.
- Input ripple current is also reduced for lower noise on V_{IN}.

The peak inductor current, reduced nearly by a factor of 2 when compared to a single phase step-up converter, is given by:

$$I_{LPEAK} \cong \frac{1}{2} \bullet \frac{I_O}{(1-D)} + \frac{\Delta I_L}{2}$$

where I_O is the average load current, D is the PWM duty cycle, and ΔI_L is the inductor ripple current. This relationship is shown graphically in Figure 1.

With 2-phase operation, one of the phases is always delivering current to the load whenever V_{IN} is greater than one-half V_{OUT} (duty cycles less than 50%). As the duty cycle decreases further, load current delivery between the two phases begins to overlap, occurring simultaneously for a growing portion of each phase as the duty cycle approaches zero. This significantly reduces both the output ripple current and the peak current in each inductor, when compared with a single-phase converter. This is illustrated in the waveforms of Figures 2 and 3.

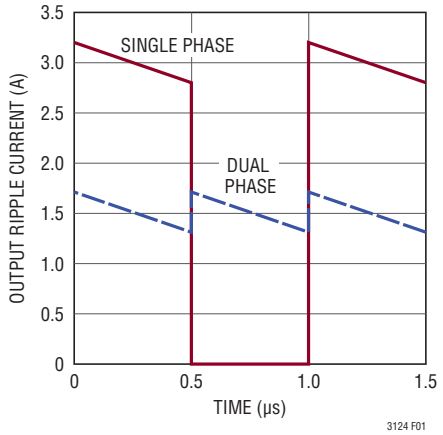


Figure 1. Comparison of Output Ripple Current with Single Phase and Dual Phase Boost Converter in a 1.5A Load Application Operating at 50% Duty Cycle

OPERATION

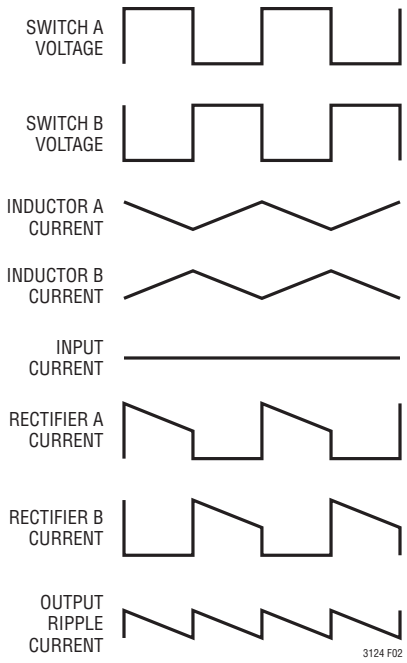


Figure 2. Simplified Voltage and Current Waveforms for 2-Phase Operation at 50% Duty Cycle

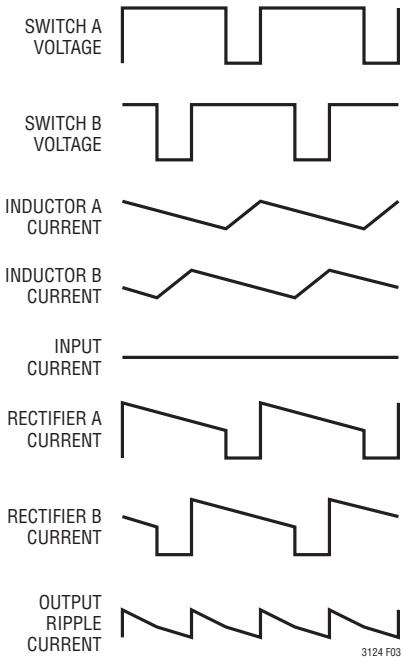


Figure 3. Simplified Voltage and Current Waveforms for 2-Phase Operation at 25% Duty Cycle

LOW VOLTAGE OPERATION

The LTC3124 is designed to allow start-up from input voltages as low as 1.8V. When V_{OUT} exceeds 2.5V, the LTC3124 continues to regulate its output, even when V_{IN} falls as low as 0.5V. This feature extends operating times by maximizing the amount of energy that can be extracted from the input source. The limiting factors for the application become the availability of the power source to supply sufficient power to the output at the low input voltage, and the maximum duty cycle, which is clamped at 94%. Note that at low input voltages, small voltage drops due to series resistance become critical and greatly limit the power delivery capability of the converter.

LOW NOISE FIXED FREQUENCY OPERATION

Soft-Start

The LTC3124 contains internal circuitry to provide soft-start operation. The soft-start utilizes a linearly increasing ramp of the error amplifier reference voltage from zero to its nominal value of 1.2V in approximately 10ms, with the internal control loop driving V_{OUT} from zero to its final programmed value. This limits the inrush current drawn from the input source. As a result, the duration of the soft-start is largely unaffected by the size of the output capacitor or the output regulation voltage. The closed-loop nature of the soft-start allows the converter to respond to load transients that might occur during the soft-start interval. The soft-start period is reset by a shutdown command on $\overline{SD}$, a UVLO event on V_{CC} (V_{CC} < 1.5V), an overvoltage event on V_{OUT} ($V_{OUT} \geq 16.5V$), or an overtemperature event (TSD is invoked when the die temperature exceeds 170°C). Upon removal of these fault conditions, the LTC3124 will soft-start the output voltage.

Error Amplifier

The noninverting input of the transconductance error amplifier is internally connected to the 1.2V reference and the inverting input is connected to FB. An external resistive voltage divider from V_{OUT} to SGND programs the output voltage from 2.5V to 15V via FB as shown in Figure 4.

$$V_{OUT} = 1.2V\left(1+\frac{R1}{R2}\right)$$

OPERATION

Selecting an R2 value of 113k to have approximately 10µA of bias current in the V_{OUT} resistor divider yields the formula:

$R1 = 94 \bullet (V_{OUT} – 1.2V)$; V_{OUT} in Volts and R1 in kΩ.

Power converter control loop compensation is set with a simple RC network connected between VC and SGND.

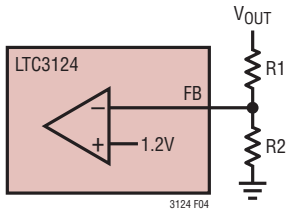


Figure 4. Programming the Output Voltage

Internal Current Limit

Current limit comparators shut off the N-channel MOSFET switches once their respective peak current is reached. Peak switch current per phase is limited to 3.5A, independent of input or output voltage, unless V_{OUT} is below approximately 1.5V, resulting in the current limit being approximately half of the nominal peak values.

Lossless current sensing converts the peak current signals of the N-channel MOSFET switches into voltages that are summed with their respective internal slope compensation. The summed signals are compared to the error amplifier outputs to provide a peak current control command for the PWMs.

Zero Current Comparator

The zero current comparators monitor the inductor currents being delivered to the output and shut off the synchronous rectifiers when the current is approximately 50mA. This prevents the inductor currents from reversing in polarity, improving efficiency at light loads.

Oscillator

The internal oscillator is programmed to *twice* the desired switching frequency with an external resistor from the RT pin to SGND according to the following formula:

$$f_{OSC}\,(MHz) \cong \left(\frac{56}{R_T(k\Omega)}\right) = 2 \bullet f\,(MHz)$$

where f = switching frequency of one phase.

Thus $R_T\,(k\Omega) \cong 28/f\,(MHz)$. See Table 1 for various switching frequencies and their corresponding R_T values.

Table 1. Switching Frequency and Their Respective R_T

SWITCHING FREQUENCY (kHz)	R_T (kΩ)
100	316
200	154
300	100
500	57.6
800	34.8
1000	28
1200	22.6
2000	13
2200	11.5
3000	8.06

For desired switching frequencies not included in Table 1, please refer to the Resistance vs Frequency curve in the Typical Performance Characteristics section.

The oscillator can be synchronized to an external frequency by applying a pulse train of *twice* the desired switching frequency to the PWM/SYNC pin. An external resistor must be connected between RT and SGND to program the oscillator to a frequency approximately 25% below that of the externally applied pulse train used for synchronization. R_T is selected in this case according to this formula:

$$R_{T(SYNC)}\,(k\Omega) \geq 1.25 \bullet R_{T(SWITCH)}\,(k\Omega)$$

where $R_{T(SWITCH)}$ is the value of R_T at the desired switching frequency, which is half of the synchronization frequency.

Shutdown

The boost converter is disabled by pulling $\overline{SD}$ below 0.25V and enabled by pulling $\overline{SD}$ above 1.6V. Note that $\overline{SD}$ can be driven above V_{IN} or V_{OUT}, as long as it is limited to less than its absolute maximum rating.

Thermal Shutdown

If the die temperature exceeds 170°C typical, the LTC3124 will go into thermal shutdown (TSD). All switches will be shut off until the die temperature drops by approximately 7°C, when the device re-initiates a soft-start and switching is re-enabled.

OPERATION

Boost Anti-Ringing Control

When $V_{OUT} \geq V_{IN} + 2V$, the anti-ringing circuitry connects a resistor across each inductor to V_{IN} to damp high frequency ringing on the SW pins during discontinuous current mode operation. Although the ringing of the resonant circuits formed by the inductors and $C_{SW(A/B)}$ (capacitance on the respective SW pins) is low energy, it can cause EMI radiation if not damped.

V_{CC} Regulator

An internal low dropout regulator generates the 4.25V (nominal) V_{CC} rail from V_{IN} or V_{OUT}, depending upon operating conditions. V_{CC} is supplied from V_{IN} if V_{IN} is initially greater than approximately 3.5V, with V_{IN} continuing to supply V_{CC} down to approximately 3V; otherwise the greater of V_{IN} and V_{OUT} supplies V_{CC}. The V_{CC} rail powers the internal control circuitry and power MOSFET gate drivers of the LTC3124. The V_{CC} regulator is disabled in shutdown to reduce quiescent current and is enabled by forcing the $\overline{SD}$ pin above its input high threshold. A 4.7µF or larger capacitor must be connected between V_{CC} and SGND.

Overvoltage Lockout

An overvoltage condition occurs when V_{OUT} exceeds approximately 16.5V. Switching is disabled and the internal soft-start ramp is reset. Once V_{OUT} drops below approximately 16V a soft-start is initiated and switching is allowed to resume. If the boost converter output is lightly loaded such that the time constant of the output capacitance, C_{OUT}, and the output load resistance, R_{OUT} is near or greater than the soft-start time of approximately 10ms, the soft-start ramp may end before or soon after switching resumes, defeating the inrush current limiting of the closed-loop soft-start following an overvoltage event.

Short-Circuit Protection

The LTC3124 output disconnect feature allows output short-circuit protection while maintaining a maximum set current limit. To reduce power dissipation under overload and short-circuit conditions, the peak switch current limits are reduced to approximately 2A. Once V_{OUT} exceeds approximately 1.5V, the current limits are reset to their nominal values of 3.5A per phase.

Output Disconnect

The LTC3124's output disconnect feature eliminates body diode conduction of the internal P-channel MOSFET rectifiers. This feature allows for V_{OUT} to discharge to 0V during shutdown, and draw no current from the input source. Inrush current will also be limited at turn-on, minimizing surge currents seen by the input supply. Note that to obtain the advantages of output disconnect, there must not be an external Schottky diode connected between SWA, SWB and V_{OUT}. The output disconnect feature also allows V_{OUT} to be pulled high, without backfeeding the power source connected to V_{IN}.

$V_{IN} > V_{OUT}$ Operation

The LTC3124 step-up converter will maintain voltage regulation even when the input voltage is above the desired output voltage. Note that operating in this mode will exhibit lower efficiency and a reduced output current capability. Refer to the Typical Performance Characteristics for details.

Burst Mode OPERATION

When the PWM/SYNC pin is held low, the boost converter operates in Burst Mode, independent of load current. This mode of operation is typically commanded to improve efficiency at light loads and reduce standby current at no load. The output current (I_{OUT}) capability in Burst Mode operation is significantly less than in PWM mode and varies with V_{IN} and V_{OUT}, as shown in Figure 5. The logic input thresholds for this pin are determined relative to V_{CC} with a low being less than 10% of V_{CC} and a high being greater than 90% of V_{CC}. The LTC3124 will operate in fixed frequency PWM mode even if Burst Mode operation is commanded during soft-start.

In Burst Mode operation, only Phase A of the LTC3124 is operational, while Phase B is disabled. The Phase A inductor current is initially charged to approximately 700mA by turning on the N-channel MOSFET switch, at which point the N-channel switch is turned off and the P-channel synchronous switch is turned on, delivering current to the output. When the inductor current discharges to approximately zero, the cycle repeats. In Burst Mode operation, energy is delivered to the output until the nominal

OPERATION

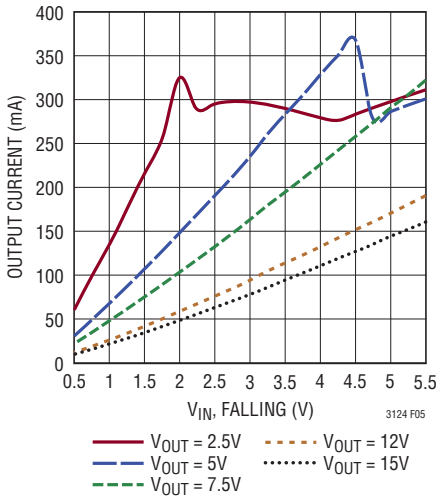


Figure 5. Burst Mode Output Current vs V_{IN}

regulation value is reached, then the LTC3124 transitions into a very low quiescent current sleep state. In sleep, the output switches are turned off and the LTC3124 consumes only 25µA of quiescent current. When the output voltage droops approximately 1%, switching resumes. This maximizes efficiency at very light loads by minimizing switching and quiescent losses. Output voltage ripple in Burst Mode operation is typically 1% to 2% peak-to-peak. Additional output capacitance (22µF or greater), or the addition of a small feedforward capacitor (10pF to 50pF) connected between V_{OUT} and FB can help further reduce the output ripple.

APPLICATIONS INFORMATION

PCB LAYOUT CONSIDERATIONS

The LTC3124 switches currents as high as 4.5A at high frequencies. Special attention should be paid to the PCB layout to ensure a stable, noise-free and efficient application circuit. Figure 6 presents the LTC3124's 4-layer PCB demo board layout (the schematic of which may be obtained from the Quick Start Guide) to outline some of the primary considerations. A few key guidelines are outlined below:

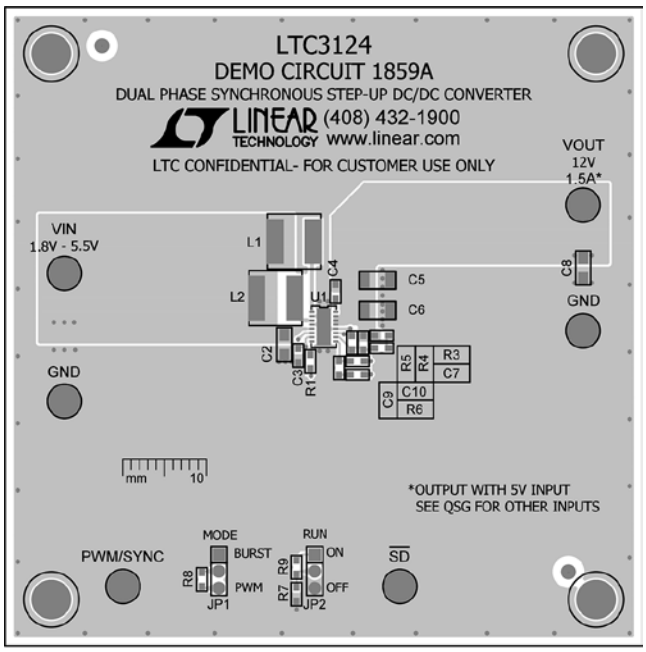
1. A 4-layer board is highly recommended for the LTC3124 to ensure stable performance over the full operating voltage and current range. A dedicated/solid ground plane should be placed directly under the V_{IN}, V_{OUTA}, V_{OUTB}, SWA, and SWB traces to provide a mirror plane to minimize noise loops from high dI/dt and dV/dt edges (see Figure 6, 2nd layer).
2. All circulating high current paths should be kept as short as possible. Capacitor ground connections should via down to the ground plane in the shortest route possible. The bypass capacitors on V_{IN} should be placed as close to the IC as possible and should have the shortest possible paths to ground (see Figure 6, top layer).
3. PGNDA pin, PGNDB pin, and the exposed pad are the power ground connections for the LTC3124. Multiple vias should connect the back pad directly to the ground plane. In addition, maximization of the metallization connected to the back pad will improve the thermal environment and improve the power handling capabilities of the IC.
4. The high current components and their connections should all be placed over a complete ground plane to minimize loop cross-sectional areas. This minimizes EMI and reduces inductive drops.
5. Connections to all of the high current components should be made as wide as possible to reduce the series resistance. This will improve efficiency and maximize the output current capability of the boost converter.
6. To prevent large circulating currents from disrupting the converters' output voltage sensing, compensation, and programmed switching frequency, the ground for the resistor divider, compensation components, and RT should be returned to the ground plane using a via placed close to the IC and away from the power connections.

APPLICATIONS INFORMATION

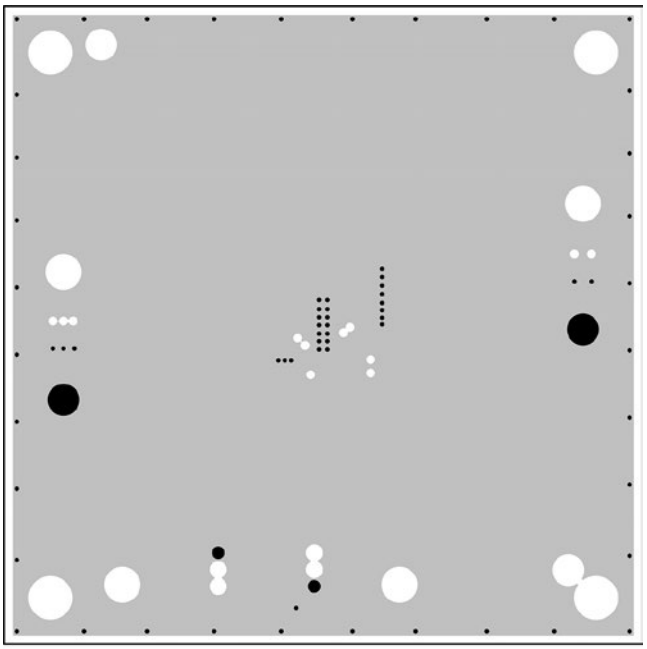
7. Keep the connections from the resistor divider to the FB pin and from the compensation components to the VC pin as short as possible and away from the switch pin connections.

8. Crossover connections should be made on inner copper layers if available. If it is necessary to place these on the ground plane, make the trace on the ground plane as short as possible to minimize the disruption to the ground plane (see Figure 6, 3rd layer).

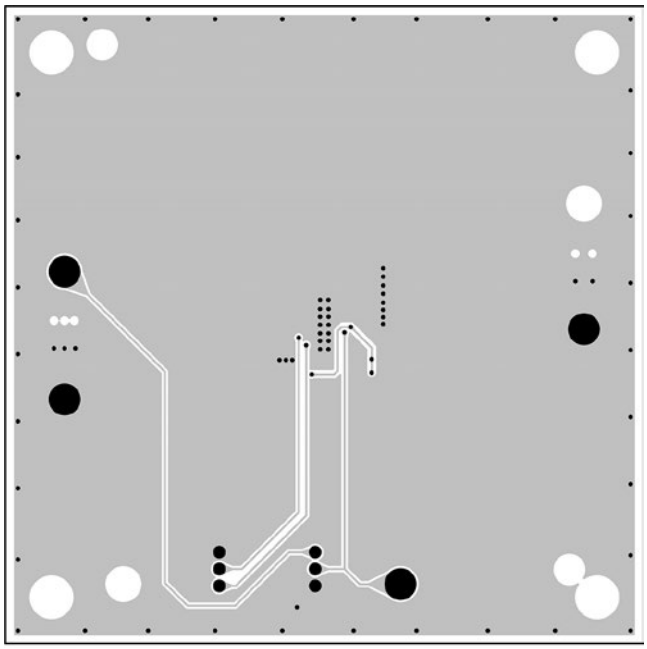
Top Layer



2nd Layer



3rd Layer



Bottom Layer (Top View)

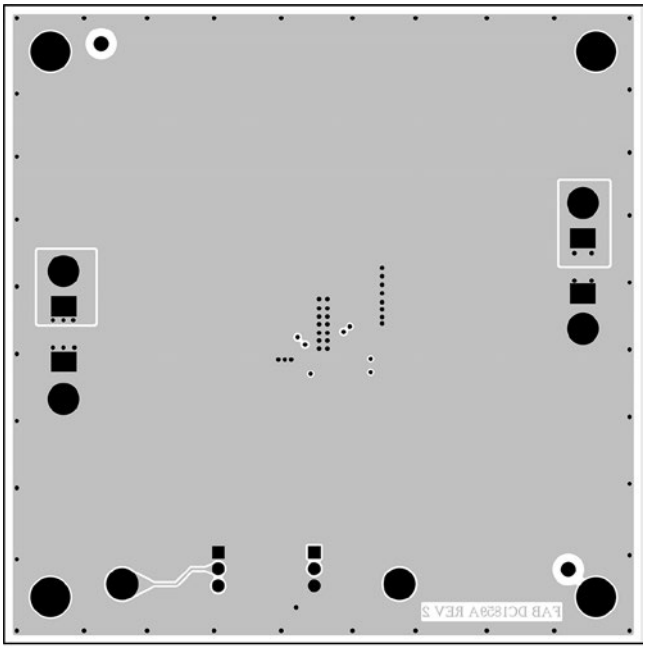


Figure 6. Example PCB Layout

APPLICATIONS INFORMATION

SCHOTTKY DIODE

Although it is not required, adding a Schottky diode from both SW pins to V_{OUT} can improve the converter efficiency by up to 4%. Note that this defeats the output disconnect and short-circuit protection features of the LTC3124.

COMPONENT SELECTION

Inductor Selection

The LTC3124 can utilize small inductors due to its capability of setting a fast (up to 3MHz) switching frequency. Larger values of inductance will allow slightly greater output current capability by reducing the inductor ripple current. To design a stable converter the range of inductance values is bounded by the targeted magnitude of the internal slope compensation and is inversely proportional to the switching frequency. The Inductor selection for the LTC3124 has the following bounds:

$$\frac{10}{f}\mu H > L > \frac{3}{f}\mu H$$

The inductor peak-to-peak ripple current is given by the following equation:

$$Ripple(A) = \frac{V_{IN} \bullet (V_{OUT} - V_{IN})}{f \bullet L \bullet V_{OUT}}$$

where:

L = Inductor Value in µH

f = Switching Frequency in MHz of One Phase

The inductor ripple current is a maximum at the minimum inductor value. Substituting 3/f for the inductor value in the above equation yields the following:

$$Ripple_{MAX}(A) = \frac{V_{IN} \bullet (V_{OUT} - V_{IN})}{3 \bullet V_{OUT}}$$

A reasonable operating range for the inductor ripple current is typically 10% to 40% of the maximum inductor current. High frequency ferrite core inductor materials reduce frequency dependent power losses compared to cheaper powdered iron types, improving efficiency. The inductor should have low DCR (series resistance of the windings) to reduce the I^2R power losses, and must be able to support the peak inductor current without saturating. Molded chokes and most chip inductors usually do not have enough core area to support the peak inductor currents of 3A to 4A seen on the LTC3124. To minimize radiated noise, use a shielded inductor.

See Table 2 for suggested components and suppliers.

Table 2. Recommended Inductors

PART NUMBER	VALUE (µH)	DCR (mΩ)	I_{SAT} (A)	SIZE (mm) W×L×H
Coilcraft XFL4020-102ME	1	12	5.4	4.3×4.3×2.1
Coilcraft MSS7341T-332NL	3.3	18	3.7	7.3×7.3×4.1
Coilcraft XAL5030-332ME	3.3	23	8.7	5.3×5.3×3.1
Coilcraft XAL5030-472ME	4.7	36	6.7	5.3×5.3×3.1
Coilcraft XAL5050-562ME	5.6	26	6.3	5.3×5.3×5.1
Coilcraft XAL6060-223ME	22	61	5.6	6.3×6.3×6.1
Coilcraft MSS1260T-333ML	33	57	4.34	12.3×12.3×6.2
Coiltronics SD53-1R1-R	1.1	20	4.8	5.2×5.2×3
Coiltronics DR74-4R7-R	4.7	25	4.37	7.6×7.6×4.35
Coiltronics DR125-330-R	33	51	3.84	12.5×12.5×6
Coiltronics DR127-470-R	47	72	5.28	12.5×12.5×8
Sumida CDR7D28MNNP-1R2NC	1.2	21	5.9	7.6×7.6×3
Sumida CDMC6D28NP-3R3MC	3.3	31	5	7.25×6.7×3
Taiyo-Yuden NR5040T3R3N	3.3	35	3.8	5×5×4
TDK LTF5022T-1R2N4R2-LC	1.2	25	4.3	5×5.2×2.2
TDK SPM6530T-3R3M	3.3	30	6.8	7.1×6.5×3
TDK VLP8040T-4R7M	4.7	25	4.4	8×7.7×4
Würth WE-LHMI 74437324010	1	27	9	4.45×4.06×1.8
Würth WE-PD 7447789002	2.2	20	4.8	7.3×7.3×3.2
Würth WE-PD 7447779002	2.2	20	6	7.3×7.3×4.5
Würth WE-PD 7447789003	3.3	30	4.2	7.3×7.3×3.2
Würth WE-PD 7447789004	4.7	35	3.9	7.3×7.3×3.2
Würth WE-HCI 7443251000	10	16	8.5	10×10×5
Würth WE-PD 744770122	22	43	5	12×12×8
Würth WE-PD 744770133	33	64	3.6	12×12×8
Würth WE-PD 7447709470	47	60	4.5	12×12×10

Output and Input Capacitor Selection

Low ESR (equivalent series resistance) capacitors should be used to minimize the output voltage ripple. Multilayer ceramic capacitors are an excellent choice as they have extremely low ESR and are available in small footprints. X5R and X7R dielectric materials are preferred for their ability to maintain capacitance over wide voltage and temperature ranges. Y5V types should not be used. Although ceramic capacitors are recommended, low ESR tantalum capacitors may be used as well.

APPLICATIONS INFORMATION

When selecting output capacitors, the magnitude of the peak inductor current, together with the ripple voltage specification, determine the choice of the capacitor. Both the ESR (equivalent series resistance) of the capacitor and the charge stored in the capacitor each cycle contribute to the output voltage ripple.

The peak-to-peak ripple due to the charge is approximately:

$$V_{RIPPLE(CHARGE)}(V) \approx \frac{I_P \bullet V_{IN}}{C_{OUT} \bullet V_{OUT} \bullet f \bullet 2}$$

where:

I_P = Peak inductor current

f = Switching frequency of one phase

The ESR of C_{OUT} is usually the most dominant factor for ripple in most power converters. The peak-to-peak ripple due to the capacitor ESR is:

$$V_{RIPPLE(ESR)}(V) = I_{LOAD} \bullet R_{ESR} \bullet \frac{V_{OUT}}{V_{IN}}$$

where R_{ESR} = capacitor equivalent series resistance.

The input filter capacitor reduces peak currents drawn from the input source and reduces input switching noise. A low ESR bypass capacitor with a minimum value of 10µF should be located as close to V_{IN} as possible.

Low ESR and high capacitance are critical to maintain low output ripple. Capacitors can be used in parallel for even larger capacitance values and lower effective ESR. Ceramic capacitors are often utilized in switching converter applications due to their small size, low ESR and low leakage currents. However, many ceramic capacitors experience significant loss in capacitance from their rated value with increased DC bias voltage. It is not uncommon for a small surface mount capacitor to lose more than 50% of its rated capacitance when operated near its rated voltage. As a result it is sometimes necessary to use a larger capacitor value or a capacitor with a larger value and case size, such as 1812 rather than 1206, in order to actually realize the intended capacitance at the full operating voltage. Be sure to consult the vendor's curve of capacitance versus DC bias voltage. Table 3 shows a sampling of capacitors suited for the LTC3124 applications.

Table 3: Representative Output Capacitors

Manufacturer, Part Number	Value (µF)	Voltage (V)	SIZE L × W × H (mm) Type, ESR (mΩ)
AVX, 1206YD226KAT2A	22	16	3.2 × 1.6 × 1.78, X5R Ceramic
AVX, 1210YC226KAT2A	22	16	3.2 × 2.5 × 2.79, X7R Ceramic
Murata, GRM31CR61C226ME15L	22	16	3.2 × 1.6 × 1.8, X5R Ceramic
Murata, GRM32ER71C226KE18K	22	16	3.2 × 2.5 × 2.7, X7R Ceramic
Murata, GRM43ER61C226KE01L	22	16	4.5 × 3.2 × 2.7, X5R Ceramic
Murata, GRM32EB31C476ME15K	47	16	3.2 × 2.5 × 2.5, X5R Ceramic
Panasonic, ECJ-4YB1C226M	22	16	3.2 × 2.5 × 2.7, X5R Ceramic
Taiyo Yuden, EMK316BJ226ML-T	22	16	3.2 × 1.6 × 1.8, X5R Ceramic
Taiyo Yuden, EMK325B7226MM-TR	22	16	3.2 × 2.5 × 2.7, X7R Ceramic
Taiyo Yuden, EMK432BJ226KM-T	22	16	4.5 × 3.2 × 2.7, X5R Ceramic
TDK, C5750X7R1C476M	47	16	5.7 × 5 × 2.5, X7R Ceramic
TDK, C4532X5R0J107M	100	6.3	4.5 × 3.2 × 2.8, X5R Ceramic
Nichicon, UBC1C101MNS1GS	100	16	8.3 × 8.3 × 11.5, Aluminum Polymer
Sanyo, 25TQC22MV	22	25	7.3 x 4.3 x 1.9, POSCAP, 45mΩ
Sanyo, 16TQC47MW	47	16	7.3 × 4.3 × 3.1, POSCAP, 40mΩ
Sanyo, 16TQC100M	100	16	7.3 × 4.3 × 3.1, POSCAP, 50mΩ
Sanyo, 25SVPF47M	47	25	6.6 × 6.6 × 5.9, OS-CON, 30mΩ
AVX, BestCap Series BZ125A105ZLB	1F	5.5	48 × 30 × 6.1, 35mΩ, 4 Lead
Cap-XX GS230F	1.2F	4.5	39 × 17 × 3.8, 28mΩ
Tecate Powerburst TPL-100/22X45	100F	2.7	D = 22, H = 45 15mΩ
Cooper KR-5R5C155-R	1.5F	5.5	D = 21.5, H = 7.5 30mΩ
Cooper HB1860-2R5117-R	110F	2.5	D = 18.5, H = 60 20mΩ
Maxwell BCAP0050-P270	50F	2.5	D = 18, H = 40 20 mΩ

APPLICATIONS INFORMATION

For applications requiring a very low profile and very large capacitance, the GS, GS2 and GW series from Cap-XX, the BestCap series from AVX and PowerStor KR series capacitors from Cooper all offer very high capacitance and low ESR in various low profile packages.

OPERATING FREQUENCY SELECTION

There are several considerations in selecting the operating frequency of the converter. Typically, the first consideration is to stay clear of sensitive frequency bands, which cannot tolerate any spectral noise. For example, in products incorporating RF communications, the 455kHz IF frequency can be sensitive to any noise, therefore switching above 600kHz is desired. Some communications have sensitivity to 1.1MHz and in that case a 1.5MHz switching converter frequency may be employed. A second consideration is the physical size of the converter. As the operating frequency is increased, the inductor and filter capacitors typically can be reduced in value, leading to smaller sized external components. The smaller solution size is typically traded for efficiency, since the switching losses due to gate charge increase with frequency.

Another consideration is whether the application can allow pulse-skipping. When the boost converter pulse-skips, the minimum on-time of the converter is unable to support the duty cycle. This results in a low frequency component to the output ripple. In many applications where physical size is the main criterion, running the converter in this mode is acceptable. In applications where it is preferred not to enter this mode, the maximum operating frequency is given by:

$$f_{MAX\_NOSKIP} <\cong \frac{V_{OUT} - V_{IN}}{V_{OUT} \bullet t_{ON(MIN)}} Hz$$

where $t_{ON(MIN)}$ = minimum on-time, which is typically around 100ns.

Thermal Considerations

For the LTC3124 to deliver its full power, it is imperative that a good thermal path be provided to dissipate the heat generated within the package. This can be accomplished by taking advantage of the large thermal pad on the underside of the IC. It is recommended that multiple vias in the printed circuit board be used to conduct heat away from the IC and into a copper plane with as much area as possible. If the junction temperature rises above ~170°C, the part will trip an internal thermal shutdown, and all switching will stop until the junction temperature drops ~7°C.

Compensating the Feedback Loop

The LTC3124 uses current mode control, with internal adaptive slope compensation. Current mode control eliminates the second order filter due to the inductor and output capacitor exhibited in voltage mode control, and simplifies the power loop to a single pole filter response. Because of this fast current control loop, the power stage of the IC combined with the external inductor can be modeled by a transconductance amplifier g_{mp} and a current controlled current source. Figure 7 shows the key equivalent small signal elements of a boost converter.

The DC small-signal loop gain of the system shown in Figure 7 is given by the following equation:

$$G_{BOOST} = G_{EA} \bullet G_{MP} \bullet G_{POWER} \bullet \frac{R2}{R1+R2}$$

where G_{EA} is the DC gain of the error amplifier, G_{MP} is the modulator gain, and G_{POWER} is the inductor current to V_{OUT} gain.

$G_{EA} = g_{ma} \bullet R_O \approx 1000V/V$

(Not Adjustable; $g_{ma} \approx 100\mu S$, $R_O \approx 10M\Omega$)

$$G_{MP} = 2 \bullet g_{mp};\ g_{mp} = \frac{\Delta I_L}{\Delta V_C} \approx 3.4S\ (\text{Not Adjustable})$$

$$G_{POWER} = \frac{\Delta V_{OUT}}{\Delta I_L} = \frac{\eta \bullet V_{IN}}{2 \bullet I_{OUT}} = \frac{\eta \bullet V_{IN} \bullet R_L}{2 \bullet V_{OUT}}$$

APPLICATIONS INFORMATION

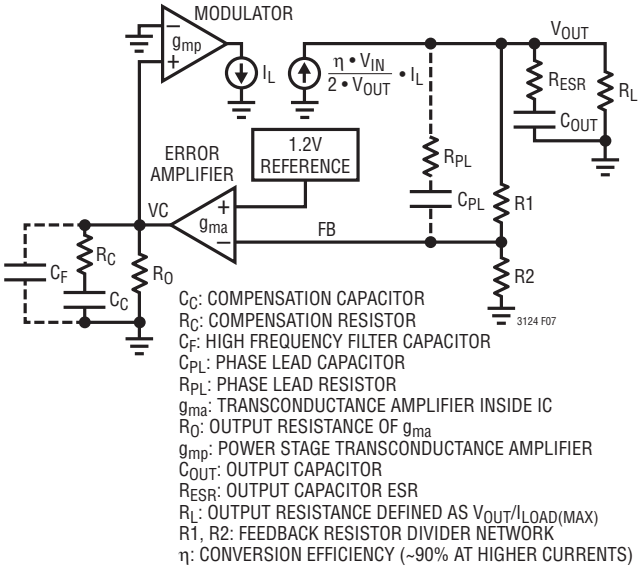


Figure 7. Boost Converter Equivalent Model

Combining the two equations above yields:

$$G_{DC} = G_{MP} \bullet G_{POWER} \approx \frac{3.4 \bullet \eta \bullet V_{IN} \bullet R_L}{V_{OUT}} \text{ V/V}$$

Converter efficiency η will vary with I_{OUT} and switching frequency f_{SWITCH} as shown in the typical performance characteristics curves.

$$\text{Output Pole: P1} = \frac{2}{2\pi \bullet R_L \bullet C_{OUT}} \text{Hz}$$

Error Amplifier Pole:

$$\text{P2} = \frac{1}{2\pi \bullet R_O \bullet (C_C + C_F)} \text{Hz; } C_F < \frac{C_C}{10}$$

$$\approx \frac{1}{2\pi \bullet R_O \bullet C_C} \text{Hz; Extremely Close to DC}$$

$$\text{Error Amplifier Zero: Z1} = \frac{1}{2\pi \bullet R_C \bullet C_C} \text{Hz}$$

$$\text{ESR Zero: Z2} = \frac{1}{2\pi \bullet R_{ESR} \bullet C_{OUT}} \text{Hz}$$

$$\text{RHP Zero: Z3} = \frac{V_{IN}^2 \bullet 2R_L}{2\pi \bullet V_{OUT}^2 \bullet L} \text{Hz}$$

$$\text{High Frequency Pole: P3} > \frac{f_{OSC}}{3} \text{Hz}$$

$$\text{Phase Lead Zero: Z4} = \frac{1}{2\pi \bullet (R1 + R_{PL}) \bullet C_{PL}} \text{Hz}$$

$$\text{Phase Lead Pole: P4} = \frac{1}{2\pi \bullet \left(\frac{R1 \bullet R2}{R1 + R2} + R_{PL}\right) \bullet C_{PL}} \text{Hz}$$

Error Amplifier Filter Pole:

$$\text{P5} = \frac{1}{2\pi \bullet R_C \bullet \frac{C_C \bullet C_F}{C_C + C_F}} \text{Hz, } C_F < \frac{C_C}{10}$$

$$\approx \frac{1}{2\pi \bullet R_C \bullet C_F} \text{Hz}$$

The current mode zero (Z3) is a right-half plane zero which can be an issue in feedback control design, but is manageable with proper external component selection. Also note that the RHP zero is a minimum at minimum input voltage and maximum output current for a given output voltage. As a general rule, the frequency at which the open-loop gain of the converter is reduced to unity, known as the crossover frequency f_C , should be set to less than one-sixth of the right-half plane zero (Z3), and under one-eighth of the switching frequency f_{SWITCH}. Once f_C is selected, the compensation component values can be calculated using a Bode plot of the power stage or two generally valid assumptions: P1 dominates the gain of the power stage for frequencies lower than f_C and f_C is much higher than P2. First calculate the power stage gain at f_C, G_{fC} in V/V. Assuming the output pole P1 dominates G_{fC} for this range, it is expressed by:

$$G_{fC} \approx \frac{G_{DC}}{\sqrt{1 + \left(\frac{f_C}{P1}\right)^2}} \text{ V/V}$$

APPLICATIONS INFORMATION

Decide how much phase margin (Φ_m) is desired. Greater phase margin can offer more stability while lower phase margin can yield faster transient response. Typically, $\Phi_m \approx 60°$ is optimal for minimizing transient response time while allowing sufficient margin to account for component variability. Φ_1 is the phase boost of Z1, P2, and P5 while Φ_2 is the phase boost of Z4 and P4. Select Φ_1 and Φ_2 such that:

$$\Phi_1 + \Phi_2 = \Phi_m + \tan^{-1}\left(\frac{f_C}{Z3}\right) \text{ and}$$

$$\Phi_1 \le 74°;\ \Phi_2 \le \left(2 \bullet \tan^{-1}\sqrt{\frac{V_{OUT}}{1.2V}}\right) - 90°$$

where V_{OUT} is in V and f_C and Z3 are in kHz.

Setting Z1, P5, Z4, and P4 such that

$$Z1 = \frac{f_C}{\sqrt{a_1}},\ P5 = f_C\sqrt{a_1},\ Z4 = \frac{f_C}{\sqrt{a_2}},\ P4 = f_C\sqrt{a_2}$$

allows a_1 and a_2 to be determined using Φ_1 and Φ_2

$$a_1 = \tan^2\left(\frac{\Phi_1 + 90°}{2}\right),\ a_2 = \tan^2\left(\frac{\Phi_2 + 90°}{2}\right)$$

The compensation will force the converter gain G_{BOOST} to unity at f_C by using the following expression for C_C:

$$C_C = \frac{10^3 \bullet g_{ma} \bullet R2 \bullet G_{fC}(a_1 - 1)\sqrt{a_2}}{2\pi \bullet f_C \bullet (R1+R2)\sqrt{a_1}} pF$$

(g_{ma} in µS, f_C in kHz, G_{fC} in V/V)

Once C_C is calculated, R_C and C_F are determined by:

$$R_C = \frac{10^6 \bullet \sqrt{a_1}}{2\pi \bullet f_C \bullet C_C} k\Omega \ (f_C \text{ in kHz, } C_C \text{ in pF})$$

$$C_F = \frac{C_C}{a_1 - 1}$$

A method for improving the converter's transient response uses a small feedforward series network of a capacitor and a resistor across the top resistor of the feedback divider (from V_{OUT} to FB). This adds a phase-lead zero and pole to the transfer function of the converter. The values of these phase lead components are given by the expressions:

$$R_{PL} = \frac{R1 - a_2 \bullet \left(\frac{R1 \bullet R2}{R1+R2}\right)}{a_2 - 1} k\Omega \text{ and}$$

$$C_{PL} = \frac{10^6 (a_2 - 1)(R1+R2)}{2\pi \bullet f_C \bullet R1^2 \sqrt{a_2}} pF$$

where R1, R2, and R_{PL} are in kΩ and f_C is in kHz.

Note that selecting Φ_2 = 0° forces a_2 = 1, and so the converter will have Type II compensation and therefore no feedforward: R_{PL} is open (infinite impedance) and C_{PL} = 0pF. If $a_2 = 0.833 \bullet V_{OUT}$ (its maximum), feedforward is maximized; R_{PL} = 0 and C_{PL} is maximized for this compensation method.

Once the compensation values have been calculated, obtaining a converter bode plot is strongly recommended to verify calculations and adjust values as required.

Using the circuit in Figure 8 as an example, Table 4 shows the parameters used to generate the Bode plot shown in Figure 9.

Table 4. Bode Plot Parameters

PARAMETER	VALUE	UNITS	COMMENT
V_{IN}	5	V	App Specific
V_{OUT}	12	V	App Specific
R_L	8	Ω	App Specific
C_{OUT} at No Bias C_{OUT} at 12V Bias	22 × 2 14 × 2	µF µF	App Specific App Specific
R_{ESR}	2.5	mΩ	App Specific
LA, LB	4.7	µH	App Specific
f_{SWITCH}	1	MHz	Adjustable
R1	1020	kΩ	Adjustable
R2	113	kΩ	Adjustable
g_{ma}	100	µS	Fixed
R_O	10	MΩ	Fixed
g_{mp}	3.4	S	Fixed
η	90	%	App Specific
R_C	84.5	kΩ	Adjustable
C_C	680	pF	Adjustable
C_F	56	pF	Adjustable
R_{PL}	Open	kΩ	Optional
C_{PL}	0	pF	Optional

APPLICATIONS INFORMATION

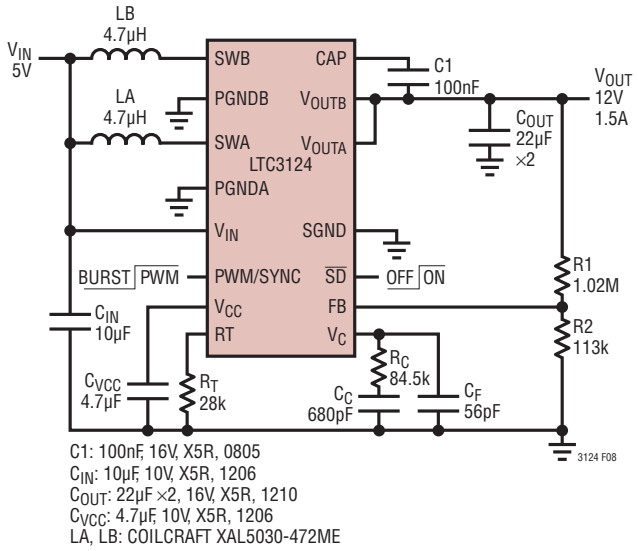
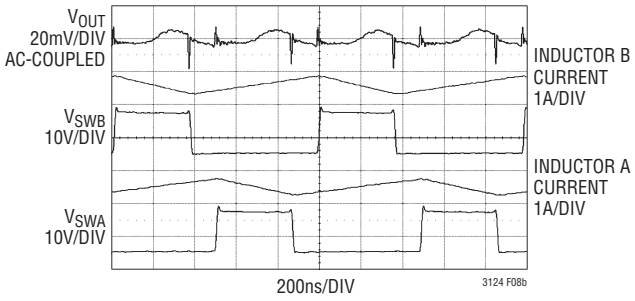
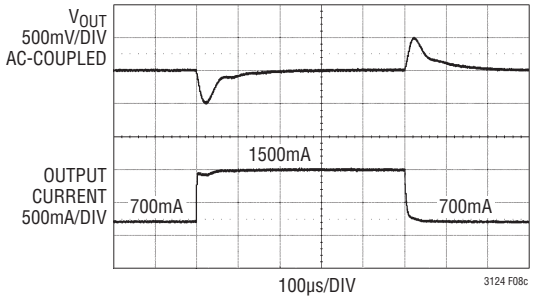


Figure 8. 1MHz, 5V to 12V, 1.5A Boost Converter

Switching Waveforms with 1.5A Load



Transient Response with 700mA to 1.5A Load Step



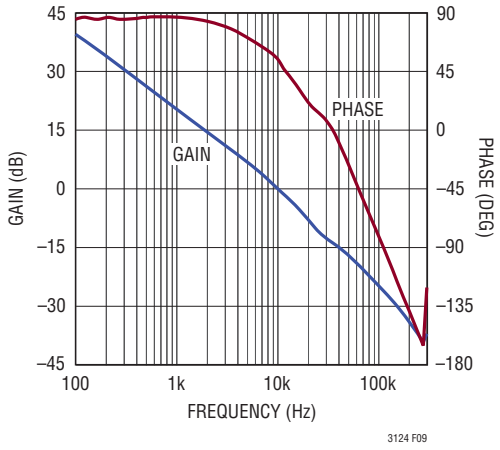


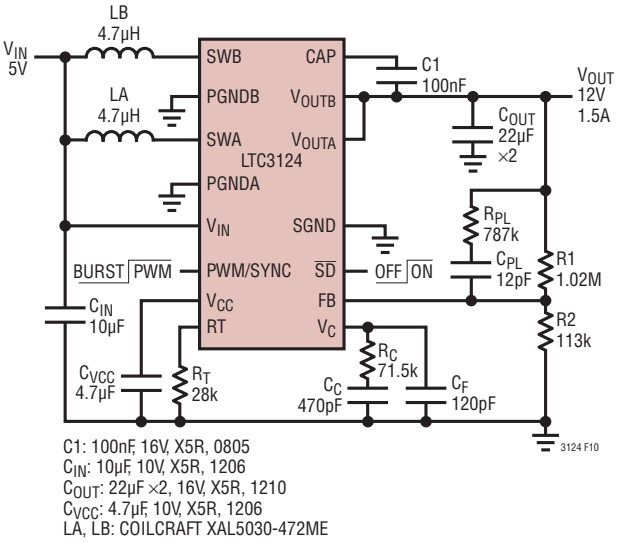
Figure 9. Bode Plot for Example Converter

APPLICATIONS INFORMATION

From Figure 9, the phase is ~60° when the gain reaches 0dB, so the phase margin of the converter is ~60°. The crossover frequency is ~10kHz, which is more than six times lower than the 94kHz frequency of the RHP zero to achieve adequate phase margin.

The circuit in Figure 10 shows the same application as that in Figure 8 with Type III compensation. This is accomplished by adding C_{PL} and R_{PL} and adjusting C_C, C_F, and R_C accordingly. Table 5 shows the parameters used to generate the bode plot shown in Figure 11.

From Figure 11, the phase margin is still optimized at ~60° and the crossover frequency remains ~10kHz. Adding CPL and RPL provides some feedforward signal in Burst Mode operation, leading to lower output voltage ripple.



C1: 100nF, 16V, X5R, 0805
C_{IN}: 10µF, 10V, X5R, 1206
C_{OUT}: 22µF ×2, 16V, X5R, 1210
C_{VCC}: 4.7µF, 10V, X5R, 1206
LA, LB: COILCRAFT XAL5030-472ME

Figure 10. Boost Converter with Phase Lead

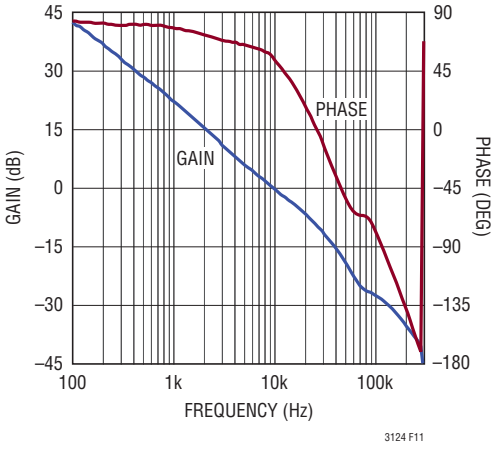


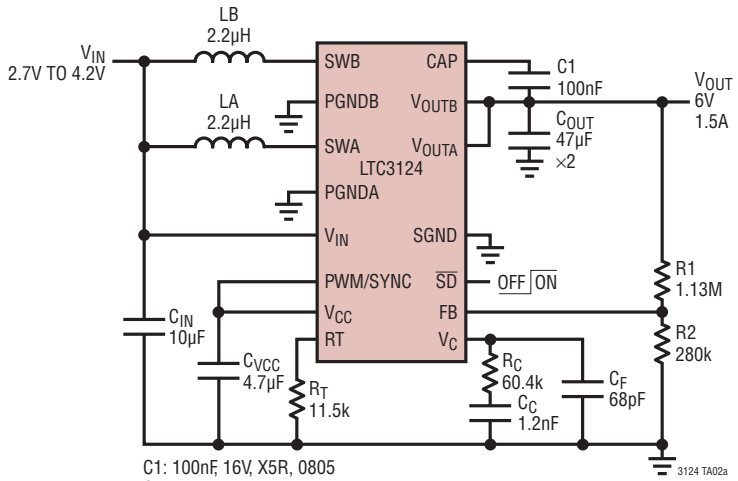
Figure 11. Bode Plot Showing Phase Lead

Table 5. Bode Plot Parameters

PARAMETER	VALUE	UNITS	COMMENT
V_{IN}	5	V	App Specific
V_{OUT}	12	V	App Specific
R_L	8	Ω	App Specific
C_{OUT} at No Bias C_{OUT} at 12V Bias	22 × 2 14 × 2	µF µF	App Specific App Specific
R_{ESR}	2.5	mΩ	App Specific
LA, LB	4.7	µH	App Specific
f_{SWITCH}	1	MHz	Adjustable
R1	113	kΩ	Adjustable
R2	1020	kΩ	Adjustable
g_{ma}	100	µS	Fixed
R_O	10	MΩ	Fixed
g_{mp}	3.4	S	Fixed
η	90	%	App Specific
R_C	71.5	kΩ	Adjustable
C_C	470	pF	Adjustable
C_F	120	pF	Adjustable
R_{PL}	787	kΩ	Adjustable
C_{PL}	12	pF	Adjustable

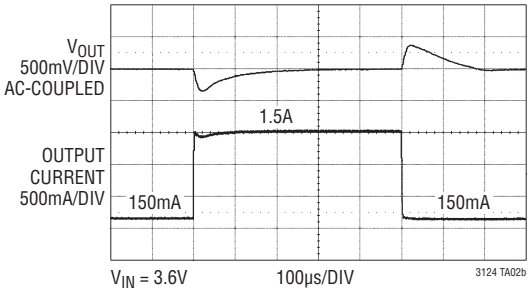
TYPICAL APPLICATIONS

Single Li Cell to 6V, 9W, 2.2MHz Synchronous Boost Converter for RF Transmitter

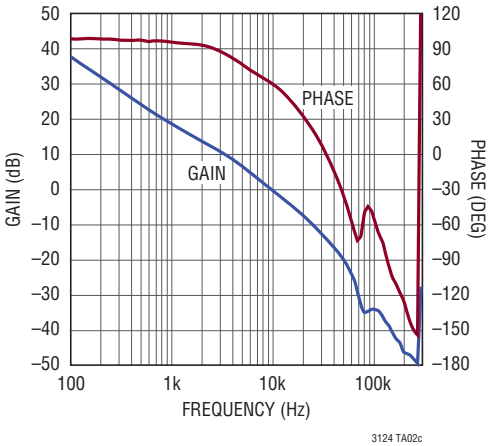


C1: 100nF, 16V, X5R, 0805
C_{IN}: 10µF, 10V, X5R, 1206
C_{OUT}: 47µF ×2, 16V, X5R, 1210
C_{VCC}: 4.7µF, 10V, X5R, 1206
LA, LB: WÜRTH WE-PD 7447779002

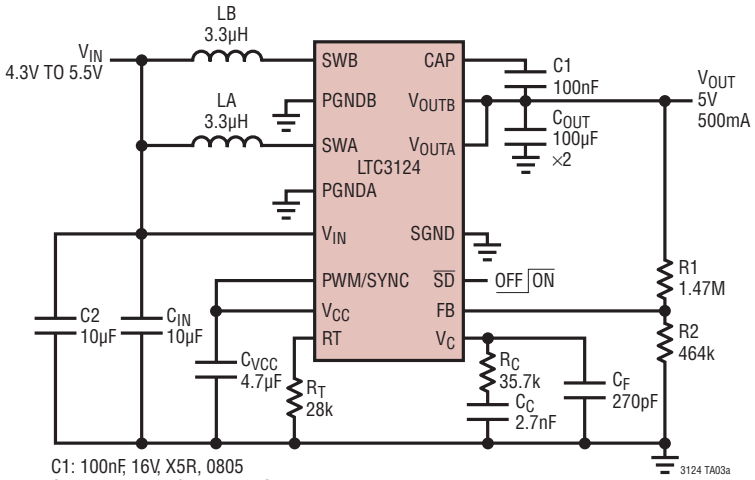
Load Step



Bode Plot

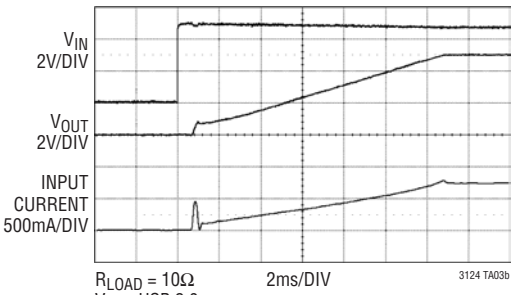


2-Port USB-Powered 1MHz Synchronous Boost Converter to 5V, 500mA



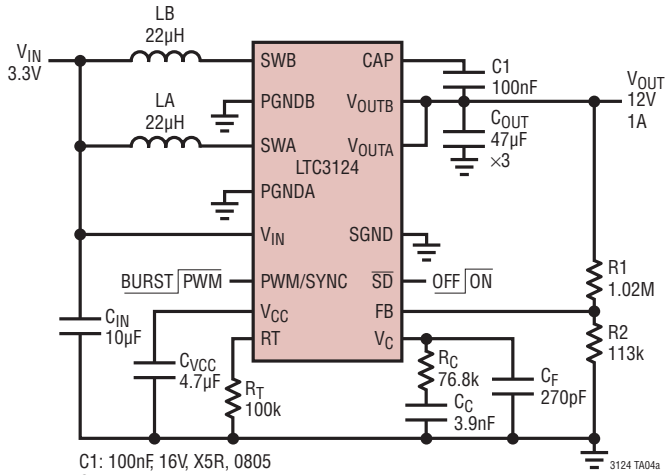
C1: 100nF, 16V, X5R, 0805
C2: KEMET T491C106K025AS
C_{IN}: 10µF, 10V, X5R, 1206
C_{OUT}: 100µF ×2, 6.3V, X5R, 1812
C_{VCC}: 4.7µF, 10V, X5R, 1206
LA, LB: COILCRAFT XAL5030-332ME

2-Port USB 2.0 Hot Plugged



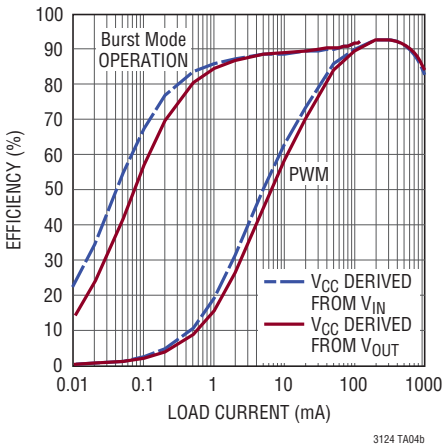
TYPICAL APPLICATIONS

3.3V to 12V, 300kHz Synchronous Boost Converter with Output Disconnect, 1A

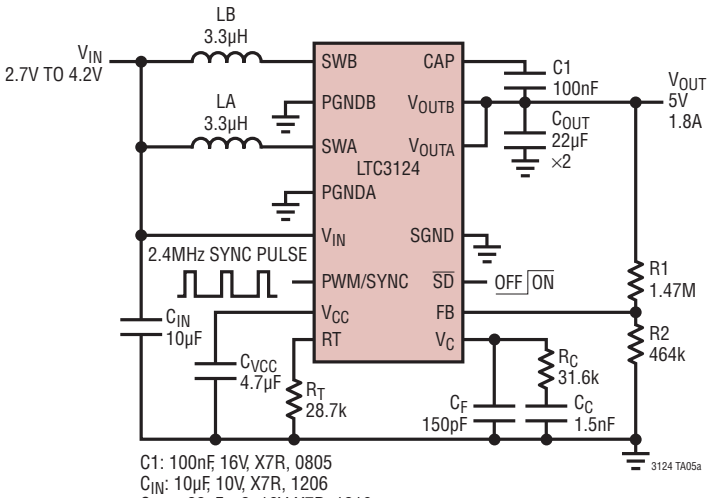


C1: 100nF, 16V, X5R, 0805
C_{IN}: 10µF, 10V, X5R, 1206
C_{OUT}: 47µF ×3, 16V, X5R, 1210
C_{VCC}: 4.7µF, 10V, X5R, 1206
LA, LB: WÜRTH WE-PDF 7447998221

Efficiency

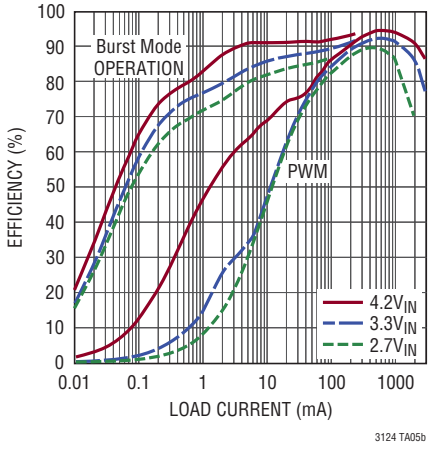


Single Li Cell to 5V, 1.8A Synchronized 1.2MHz Switching Boost Converter for RFPA Power Supply



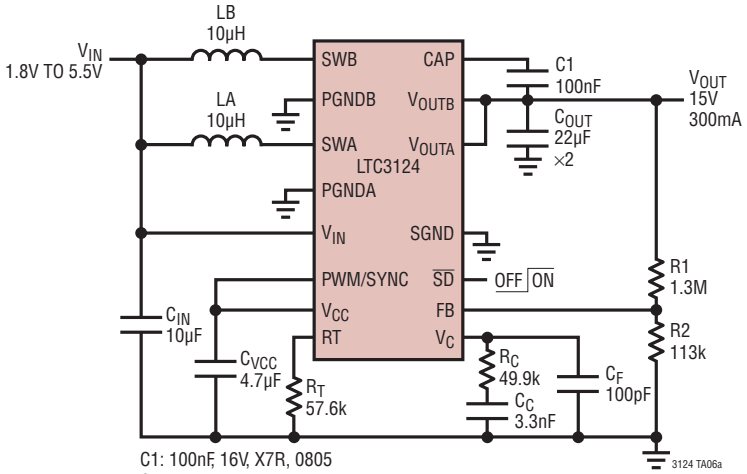
C1: 100nF, 16V, X7R, 0805
C_{IN}: 10µF, 10V, X7R, 1206
C_{OUT}: 22µF ×2, 16V, X7R, 1210
C_{VCC}: 4.7µF, 10V, X7R, 1206
LA, LB: COILCRAFT MSS7341T-332NL

Efficiency



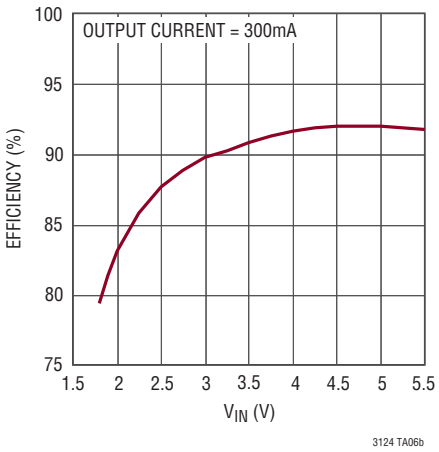
TYPICAL APPLICATIONS

1.8V to 5.5V Input to 15V Output, 500kHz Synchronous Boost Converter with Output Disconnect, 300mA

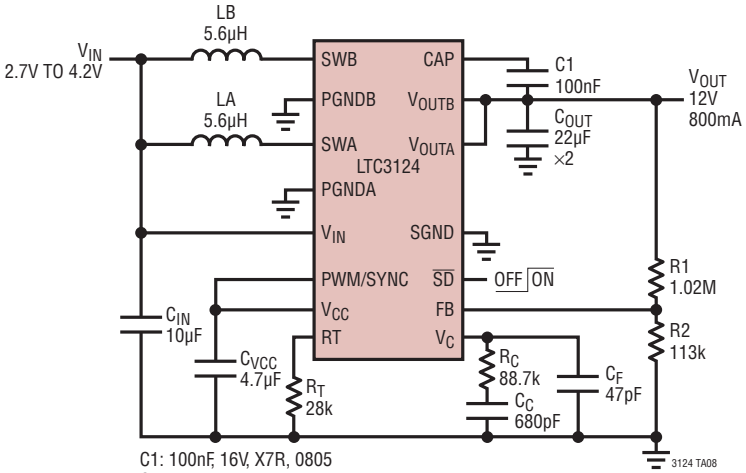


C1: 100nF, 16V, X7R, 0805
C_{IN}: 10µF, 10V, X7R, 1206
C_{OUT}: 22µF ×2, 16V, X7R, 1210
C_{VCC}: 4.7µF, 10V, X7R, 1206
LA, LB: WÜRTH WE-HCI 7443251000

Efficiency



Single Li Cell to 12V, 1MHz Synchronous Boost Converter with Output Disconnect, 800mA

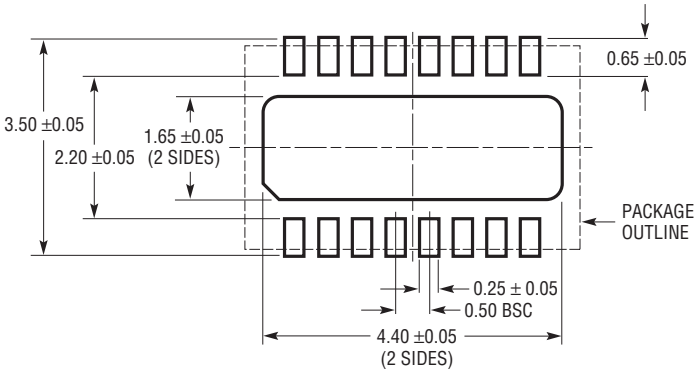


C1: 100nF, 16V, X7R, 0805
C_{IN}: 10µF, 10V, X7R, 1206
C_{OUT}: 22µF ×2, 16V, X7R, 1210
C_{VCC}: 4.7µF, 10V, X7R, 1206
LA, LB: COILCRAFT XAL5050-562ME

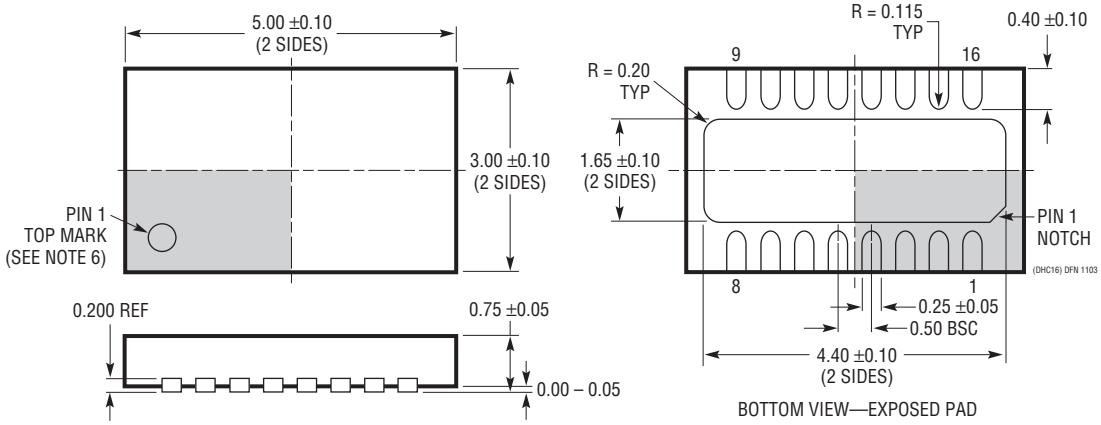
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DHC Package
16-Lead Plastic DFN (5mm × 3mm)
(Reference LTC DWG # 05-08-1706 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



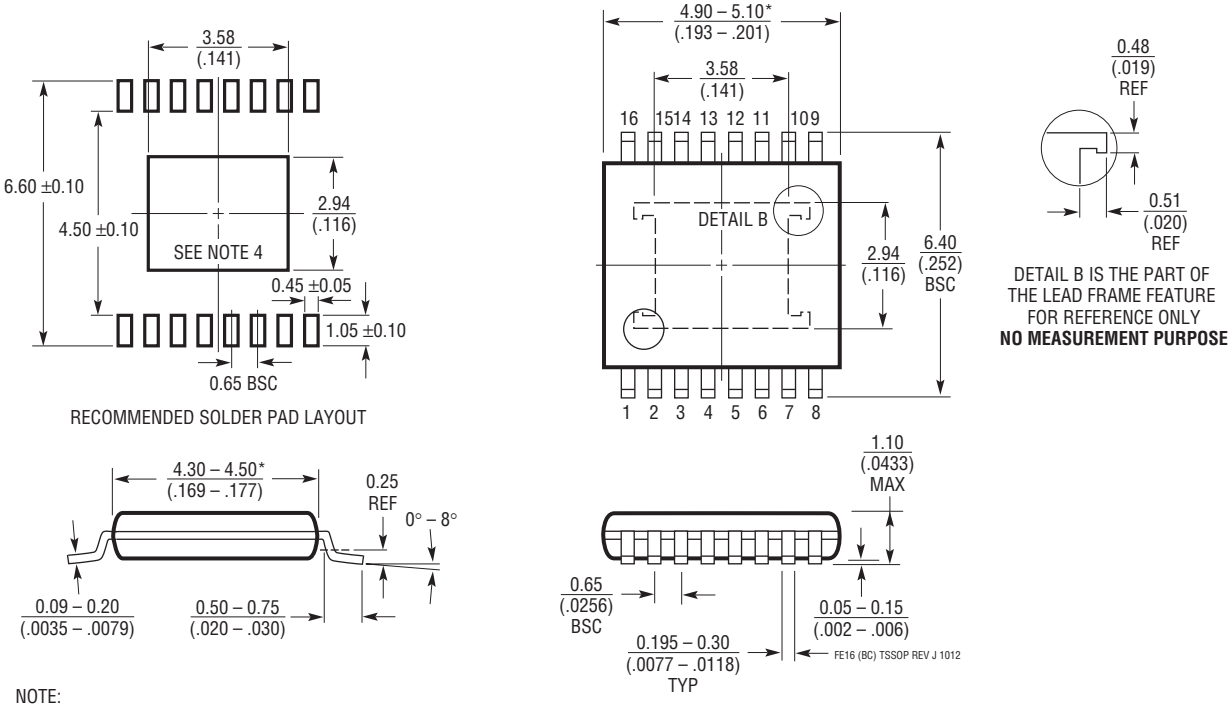
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJED-1) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

FE Package
16-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev J)
Exposed Pad Variation BC

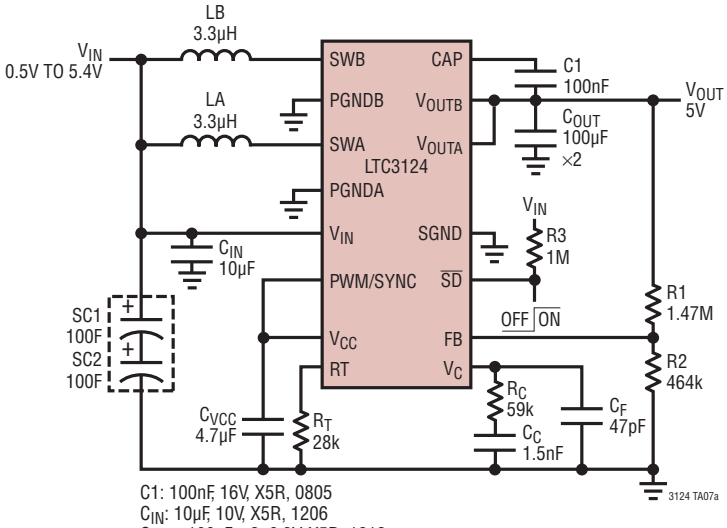


NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

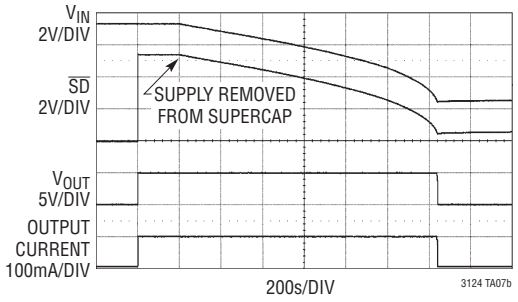
TYPICAL APPLICATION

Dual Supercapacitor Backup Power Supply, 0.5V to 5.4V

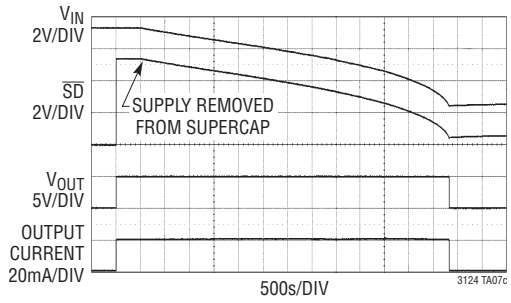


C1: 100nF, 16V, X5R, 0805
C_{IN}: 10µF, 10V, X5R, 1206
C_{OUT}: 100µF ×2, 6.3V, X5R, 1812
C_{VCC}: 4.7µF, 10V, X5R, 1206
LA, LB: COILCRAFT XAL5030-332ME
SC1, SC2: TECATE POWERBURST TPL-100/22X45

PWM Rundown Curve



Burst Mode Rundown Curve



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3459	70mA I_{SW}, 10V Micropower Synchronous Boost Converter with Output Disconnect, Burst Mode Operation	V_{IN}: 1.5V to 5.5V, $V_{OUT(MAX)}$ = 10V, I_Q = 10µA, I_{SD} < 1µA, ThinSOT Package
LTC3528	1A I_{SW}, 1MHz, Synchronous Step-Up DC/DC Converter with Output Disconnect, Burst Mode Operation	94% Efficiency V_{IN}: 700mV to 5.25V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 12µA, I_{SD} < 1µA, 2mm × 3mm DFN Package
LTC3539	2A I_{SW}, 1MHz/2MHz, Synchronous Step-Up DC/DC Converters with Output Disconnect, Burst Mode Operation	94% Efficiency V_{IN}: 700mV to 5.25V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 10uA, I_{SD} < 1µA, 2mm × 3mm DFN Package
LTC3421	3A I_{SW}, 3MHz, Synchronous Step-Up DC/DC Converter with Output Disconnect	95% Efficiency V_{IN}: 0.5V to 4.5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 12µA, I_{SD} < 1µA, QFN24 Package
LTC3428	4A I_{SW}, 2MHz (1MHz Switching), Dual Phase Step-Up DC/DC Converter	92% Efficiency V_{IN}: 1.6V to 4.5V, $V_{OUT(MAX)}$ = 5.25V, I_{SD} < 1µA, 3mm × 3mm DFN Package
LTC3425	5A I_{SW}, 8MHz, Low Ripple, 4-Phase Synchronous Step-Up DC/DC Converter with Output Disconnect	95% Efficiency V_{IN}: 0.5V to 4.5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 12µA, I_{SD} < 1µA, QFN32
LTC3122	2.5A I_{SW}, 3MHz, Synchronous Step-Up DC/DC Converter with Output Disconnect, Burst Mode Operation	95% Efficiency V_{IN}: 1.8V to 5.5V [500mV After Start-Up], $V_{OUT(MAX)}$ = 15V, I_Q = 25µA, I_{SD} < 1µA, 3mm × 4mm DFN and MSOP Packages
LTC3112	15V, 2.5A, 750kHz, Synchronous Buck-Boost DC/DC Converter with Output Disconnect, Burst Mode Operation	95% Efficiency V_{IN}: 2.7V to 15V, $V_{OUT(MAX)}$ = 14V, I_Q = 50µA, I_{SD} < 1µA, 4mm × 5mm DFN and TSSOP Packages
LTC3114-1	40V, 1A, 2MHz, Synchronous Buck-Boost DC/DC Converter with Output Disconnect, Output Current Limit, Burst Mode Operation	95% Efficiency V_{IN}: 2.2V to 40V, $V_{OUT(MAX)}$ = 40V, I_Q = 30µA, I_{SD} = 3µA, 3mm × 5mm DFN and TSSOP Packages
LTC3115-1	40V, 2A, 2MHz, Synchronous Buck-Boost DC/DC Converter with Output Disconnect, Burst Mode Operation	95% Efficiency V_{IN}: 2.7V to 40V, $V_{OUT(MAX)}$ = 40V, I_Q = 30µA, I_{SD} = 3µA, 4mm × 5mm DFN and TSSOP Packages

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