THE DATASHEET OF

LTC3811EUHF#TRPBF

High Speed Dual, Multiphase Step-Down DC/DC Controller

FEATURES

- **Fixed Frequency, Peak Current Mode Control**
- **±0.5% Output Accuracy Over Temperature**
- **Optimized for Low V_{OUT} Applications (Up to 3.3V)**
- **Dual or Single Output, Multiphase Operation**
- **Wide V_{IN} Range: 4.5V to 30V Operation**
- **High Speed Differential Remote Sense Amplifier**
- **Inductor DCR or Sense Resistor Capable**
- **Adjustable Peak Current Sense Voltage: 24mV to 85mV**
- **Very Low Duty Cycle Operation: $t_{ON(MIN)}$ = 65ns (Typ)**
- Powerful Internal Gate Drivers
- Output Voltage Soft-Start, Tracking and Sequencing
- Programmable Load Line for Reduced C_{OUT}
- Clock Input and Output for Up to 12-Phase Operation
- Fixed Frequency Operation from 250kHz to 750kHz
- PLL Synchronization from 150kHz Up to 900kHz
- Selectable CCM or DCM Operation
- Available in 5mm × 7mm QFN and G36 Packages

APPLICATIONS

- Network Servers
- High Current ASIC Supplies
- Low Voltage Power Distribution

DESCRIPTION

The LTC®3811 is a dual, PolyPhase® synchronous step-down switching regulator controller optimized for output voltages up to 3.3V. The LTC3811 includes high bandwidth error amplifiers as well as a high speed differential remote sense amplifier. The sense voltage range is programmable from 24mV to 85mV, allowing the use of either the inductor DCR or a discrete sense resistor. Multiphase operation is made possible using the MODE/SYNC input, the CLKOUT output and the PHASEMODE control pin, allowing 1-, 2-, 3-, 4-, 6- or 12-phase operation.

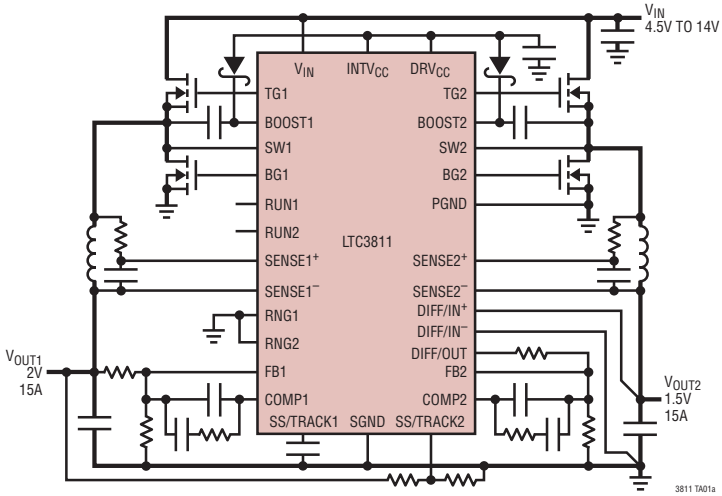
Large internal gate drivers minimize switching losses and allow the use of multiple power MOSFETs connected in parallel for high current applications.

The operating frequency of the LTC3811 can be programmed from 250kHz to 750kHz and can also be synchronized to an external clock using the internal PLL.

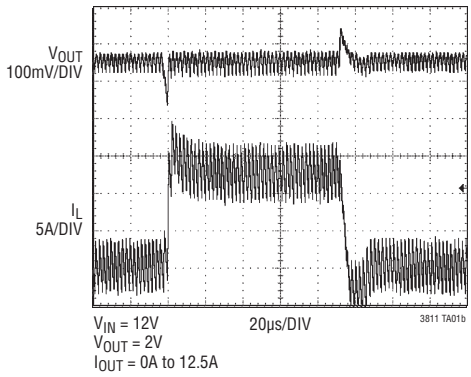
Tracking and sequencing are possible with the LTC3811, and soft-start is programmed with an external capacitor. Shutdown reduces supply current to 20µA.

TYPICAL APPLICATION

Dual Output, 2-Phase Tracking Core and I/O Supply



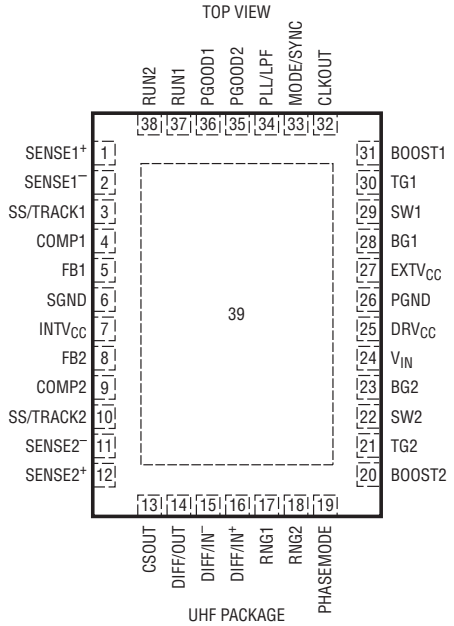
Load Step



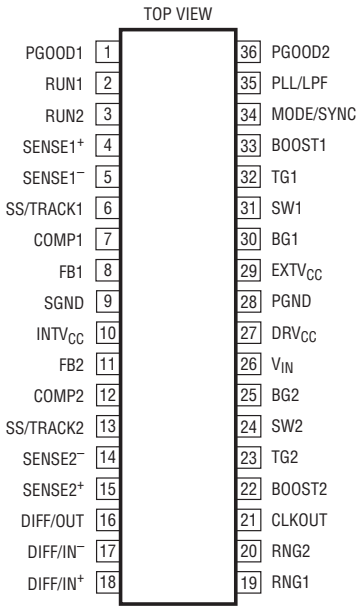
ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage (V_{IN}) ..... –0.3V to 30V
Topside Driver Voltages
(BOOST1, BOOST2) ..... –0.3V to 37V
Switch Voltage (SW1, SW2) ..... –5V to 30V
BOOST1 – SW1, BOOST2 – SW2 ..... –0.3V to 7V
DRV_{CC}, $INTV_{CC}$, $EXTV_{CC}$, RUN1, RUN2, DIFF/IN$^+$, DIFF/IN$^-$, PHASEMODE, PGOOD1, PGOOD2, MODE/SYNC Voltages ..... –0.3V to 7V
FB1, FB2, RNG1, RNG2, SS/TRACK1, SS/TRACK2, PLL/LPF, SENSE1$^+$, SENSE1$^-$, SENSE2$^+$, SENSE2$^-$ Voltages ..... –0.3V to $INTV_{CC}$
DRV_{CC} LDO RMS Output Current 100mA
Operating Temperature Range (Note 2) ..... –40°C to 85°C
Junction Temperature (Note 3) ..... 125°C
Storage Temperature Range ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec)
SSOP Package ..... 300°C

PIN CONFIGURATION



UHF PACKAGE
38-LEAD (5mm × 7mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 39) IS PGND, MUST BE SOLDERED TO PCB



G PACKAGE
36-LEAD PLASTIC SSOP WIDE
T_{JMAX} = 125°C, θ_{JA} = 100°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3811EUHF#PBF	LTC3811EUHF#TRPBF	3811	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 85°C
LTC3811EG#PBF	LTC3811EG#TRPBF	LTC3811EG	36-Lead Plastic SSOP Wide	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_J = 25°C. V_{IN} = 12V, MODE/SYNC = 0V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply							
V_{IN}	Operating Input Voltage Range			4.5		30	V
I_Q	Total Quiescent Supply Current Continuous Mode (Note 4) Shutdown Mode	 $V_{FB1,2}$ = 0.7V $V_{RUN1,2}$ = 0V	 ● ●		 10.5 20	 20 40	 mA µA
RUN Pin ON/OFF Control							
I_{RUN}	RUN Pin Input Leakage	$V_{RUN1,2}$ = 3.3V		–1		1	µA
$V_{IL(RUN)}$	Low Level RUN Input Threshold					0.3	V
$V_{IH(RUN)}$	High Level RUN Input Threshold			1.8			V
Error Amplifier Characteristics (Both Channels)							
V_{FB1}, V_{FB2}	Feedback Voltage Accuracy	(Note 5)	 ●	598 597	600	602 603	mV mV
I_{FB1}, I_{FB2}	Feedback Pin Input Current	V_{COMP} = 1.25V (Note 5)		–100		100	nA
$\Delta V_{FB}/\Delta V_{IN}$	Line Regulation	4.5V ≤ V_{IN} ≤ 30V (Note 5)	●		0.002	0.02	%/V
$\Delta V_{FB}/\Delta V_{COMP}$	Load Regulation	ΔV_{COMP} = 1.25V to 1.5V (Note 5)	●	–0.1	–0.01		%
$f_{0dB(EA)}$	Error Amplifier Unity Gain Crossover Frequency	(Note 6)			8		MHz
$V_{OH(EA)}$	Error Amplifier Maximum Output Voltage (Internally Clamped)	V_{FB} = 0.54V, No Load			2.6		V
$V_{OL(EA)}$	Error Amplifier Minimum Output Voltage	V_{FB} = 0.66V, No Load			10		mV
$V_{FB(OFF)}$	FB Voltage Threshold to Disable Error Amplifier Output	$V_{INTVCC} – V_{FB}$			0.3		V
Soft-Start/Tracking							
I_{SS1}, I_{SS2}	SS/TRACK1, SS/TRACK2 Charging Currents	$V_{SS/TRACK1}$ = $V_{SS/TRACK2}$ = 0.3V			–2.5		µA
R_{SS1}, R_{SS2}	SS/TRACK1, SS/TRACK2 Pull-Down Resistance in Shutdown	V_{RUN1} = V_{RUN2} = 0V			1		kΩ
Differential Amplifier							
A_V	Differential Mode Gain, $\Delta V_{DIFF/OUT}/\Delta V_{DIFF/IN}$	$\Delta V_{DIFF/IN}$ = 1V to 3.5V, $I_{DIFF/OUT}$ = –100µA		0.995	1.000	1.005	V/V
$V_{OS(DIFF)}$	Output Offset Voltage, $V_{DIFF/OUT} – V_{DIFF/IN}$+	$V_{DIFF/IN}$+ = 1.25V, $V_{DIFF/IN}$– = 0V, $I_{DIFF/OUT}$ = –100µA		–6		6	mV
R_{IN}	Input Resistance	Measured at $V_{DIFF/IN}$+			160		kΩ
$PSRR_{DIFF}$	Power Supply Rejection Ratio	7V ≤ V_{IN} ≤ 30V			100		dB
$V_{DM(DIFF)}$	Maximum Differential Mode Input Voltage	$V_{DIFF/IN}$+ – $V_{DIFF/IN}$–, Measured at $V_{DIFF/OUT}$, $I_{DIFF/OUT}$ = –100µA				5.5	V
I_{MAX}+	Maximum Sink Current			2			mA
I_{MAX}–	Maximum Source Current					–2	mA
$f_{0dB(DIFF)}$	Unity Gain Bandwidth	(Note 6)			8		MHz
Current Comparators							
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold (V_{SENSE}+ – V_{SENSE}–)	V_{FB} = 0.575V, V_{CM} = 1.25V V_{RNG} = 0V V_{RNG} = $INTV_{CC}$ V_{RNG} = 2V		 14 32.5 60	 24 50 85	 34 67.5 110	 mV mV mV
$V_{SENSE(MIN)}$	Minimum Current Sense Threshold (V_{SENSE}+ – V_{SENSE}–)	V_{FB} = 0.625V, V_{CM} = 1.25V V_{RNG} = 0V V_{RNG} = $INTV_{CC}$ V_{RNG} = 2V			 –21 –41 –67		 mV mV mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_J = 25°C. V_{IN} = 12V, MODE/SYNC = 0V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{SENSE}	Total Sense Pin Current (V_{SENSE}+ + V_{SENSE}–)	V_{CM} = 1.25V			–1.5		µA
$V_{CM(CS)}$	V_{SENSE}+, V_{SENSE}– Pin Common Mode Input Voltage Range			0		3.5	V
Voltage Position Amplifier (QFN Package Only)							
g_m	Voltage Position Transconductance, $\Delta I_{CSOUT}/\Delta V_{SENSE}$ (Note 8)	V_{SENSE1}+ – V_{SENSE1}– = V_{SENSE2}+ – V_{SENSE2}– = ±50mV, V_{CM} = 1.25V, V_{CSOUT} = 1.25V			5.0		mS
$I_{OS(VP)}$	Output Offset Current, Measured at CSOUT	V_{SENSE1}+ – V_{SENSE1}– = V_{SENSE2}+ – V_{SENSE2}– = 1.25V, V_{CSOUT} = 1.25V		–40		40	µA
Multiphase Oscillator and Phase-Lock Loop (Note 9)							
f_{NOM}	Nominal Frequency	$V_{PLL/LPF}$ Pin Floating, MODE/SYNC = DC Voltage		450	500	550	kHz
f_{LOW}	Lowest Frequency	$V_{PLL/LPF}$ = 0V, MODE/SYNC = DC Voltage		200	250	300	kHz
f_{HIGH}	Highest Frequency	$V_{PLL/LPF}$ = $INTV_{CC}$, MODE/SYNC = DC Voltage		650	750	850	kHz
$f_{SYNC(MIN)}$	Minimum Synchronizable Frequency	MODE/SYNC = External Clock			125	175	kHz
$f_{SYNC(MAX)}$	Maximum Synchronizable Frequency	MODE/SYNC = External Clock		900	1000		kHz
$I_{PLL/LPF}$	Phase Detector Output Current Sinking Sourcing	 $f_{MODE/SYNC} < f_{OSC}$ $f_{MODE/SYNC} > f_{OSC}$			 –4.3 5.1		 µA µA
θ1 – θ2	Channel 1 to Channel 2 Phase Relationship (Note 9)	$V_{PHASMODE}$ = 0V $V_{PHASMODE}$ = 50% $INTV_{CC}$ $V_{PHASMODE}$ = $INTV_{CC}$			180 180 120		deg deg deg
θ1 – θ_{CLKOUT}	Channel 1 to CLKOUT Phase Relationship (Note 9)	$V_{PHASMODE}$ = 0V $V_{PHASMODE}$ = 50% $INTV_{CC}$ $V_{PHASMODE}$ = $INTV_{CC}$			90 60 240		deg deg deg
$V_{OL(CLKOUT)}$	Low Level CLKOUT Output Voltage	R_{CLK} = 50k to Ground				0.2	V
$V_{OH(CLKOUT)}$	High Level CLKOUT Output Voltage	R_{CLK} = 50k to Ground		4.0	5.8		V
$R_{MODE/SYNC}$	MODE/SYNC Input Resistance				75		kΩ
$V_{IL(MODE/SYNC)}$	Low Level MODE/SYNC Input Threshold					0.3	V
$V_{IH(MODE/SYNC)}$	High Level MODE/SYNC Input Threshold			1.8			V
Power Good Indicators							
$V_{OL(PGOOD)}$	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.12	0.30	V
$I_{PGOOD(OFF)}$	PGOOD Leakage Current	V_{PGOOD} = 6V				1.0	µA
$\Delta V_{FB(OV)}$	ΔV_{FB}, PGOOD Overvoltage Threshold	$V_{FB(OV)}$ – $V_{FB(NOM)}$ in Percent		7	10	13	%
$\Delta V_{FB(UV)}$	ΔV_{FB}, PGOOD Undervoltage Threshold	$V_{FB(UV)}$ – $V_{FB(NOM)}$ in Percent		–13	–10	–7	%
$\Delta V_{FB(HYST)}$	ΔV_{FB}, PGOOD Comparator Hysteresis	UV or OV Comparator			12		mV
$t_{PG(FAULT)}$	Delay from UV/OV Condition to PGOOD Falling				145		µs
$t_{PG(OK)}$	Delay from UV/OV Fault Recovery to PGOOD Rising				38		µs
Thermal Protection							
T_{JSD}	Thermal Shutdown Junction Temperature	(Note 6)			165		°C
$T_{JSD(HYST)}$	Thermal Shutdown Junction Temperature Hysteresis	(Note 6)			25		°C

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DRV_{CC} Linear Regulator							
V_{DRVCC}	LDO Regulator Output Voltage	V_{EXTVCC} = 0V	●	5.6	6.0	6.4	V
$\Delta V_{DRVCC(LOAD)}$	DRV_{CC} Load Regulation	I_{LOAD} = 0mA to 50mA		–2.0	–0.5		%
$\Delta V_{DRVCC(LINE)}$	DRV_{CC} Line Regulation	ΔV_{IN} = 8.5V to 30V			0.01	0.2	%/V
$V_{DRVCC(UVLO)}$	LDO Regulator Undervoltage Threshold	DRV_{CC} Rising			3.7		V
$V_{DRVCC(HYST)}$	LDO Regulator Undervoltage Hysteresis				0.56		V
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	I_{DRVCC} = 20mA, $EXTV_{CC}$ Rising			4.5		V
$V_{EXTVCC(HYST)}$	$EXTV_{CC}$ Switchover Hysteresis	I_{DRVCC} = 20mA			400		mV
$V_{EXTVCC(DROP)}$	$EXTV_{CC}$ Voltage Drop	I_{DRVCC} = 20mA, V_{EXTVCC} = 5V			100		mV
Gate Drivers							
t_r (TG1, TG2)	Top Gate Rise Time	C_L = 3300pF (Note 6)			20		ns
t_f (TG1, TG2)	Top Gate Fall Time	C_L = 3300pF (Note 6)			10		ns
t_r (BG1, BG2)	Bottom Gate Rise Time	C_L = 3300pF (Note 6)			20		ns
t_f (BG1, BG2)	Bottom Gate Fall Time	C_L = 3300pF (Note 6)			10		ns
$R_{DS(ON)(TG)}$ TG1, TG2	Top Gate Pull-Down NMOS On-Resistance	TG to SW			0.9		Ω
$R_{DS(ON)(BG)}$ BG1, BG2	Bottom Gate Pull-Down NMOS On-Resistance	BG to PGND			0.9		Ω
$I_{PK(TG)}$ TG1, TG2	Top Gate (TG) Peak Source Current				1.0		A
$I_{PK(BG)}$ BG1, BG2	Bottom Gate (BG) Peak Source Current				1.0		A
t_{DEAD1}	Bottom Gate Off to Top Gate On Deadtime	(Note 6)			30		ns
t_{DEAD2}	Top Gate Off to Bottom Gate On Deadtime	(Note 6)			30		ns
$t_{ON(MIN)}$	Minimum On-Time	V_{COMP} = 1.25V (Note 6, 7)			65		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime. Unless otherwise specified, all voltages are relative to SGND and all currents are positive into a pin.

Note 2: The LTC3811E is guaranteed to meet performance specifications from 0°C to 85°C temperature. Specifications over the –40°C to 85°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$$T_J = T_A + (P_D \bullet TBD°C/W)$$

Note 4: The dynamic input supply current is higher due to power MOSFET gate charging ($Q_G \bullet f_{OSC}$). See Applications Information for more information.

Note 5: The error amplifiers are measured in a feedback loop using an external servo operational amplifier that drives the V_{FB} pin and regulates V_{COMP} to be equal to the external control voltage.

Note 6: Guaranteed by design, not subject to test.

Note 7: The minimum on-time condition corresponds to an inductor peak-to-peak ripple current of 50% of I_{MAX}. See Applications Information for more details.

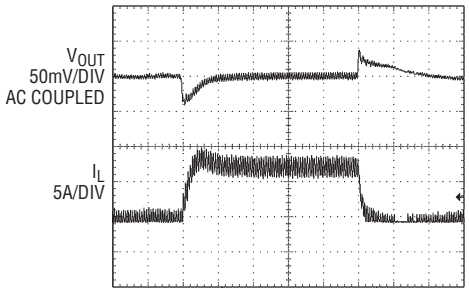
Note 8: The voltage positioning amplifier operates as a transconductance amplifier, where the input voltages are the $SENSE^+$ to $SENSE^-$ potentials for both channels. The amplifier output current flows through an external resistor in order to program the amount of voltage droop at full load.

Note 9: The PHASEMODE function is only available in the QFN package. The 36-lead GW package has a fixed channel 1-to-channel 2 phase relationship of 180°C and a channel 1-to-CLKOUT phase relationship of 90°C. The version in the 36-lead GW package is therefore optimized for 2- and 4-phase operation.

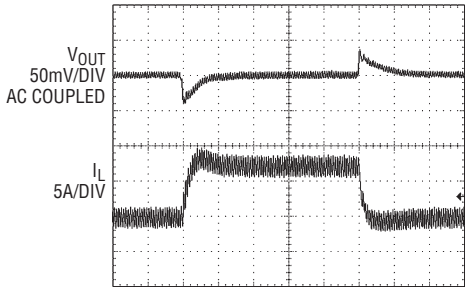
Note 10: Rise and fall times are measured at 10% and 90% levels.

TYPICAL PERFORMANCE CHARACTERISTICS

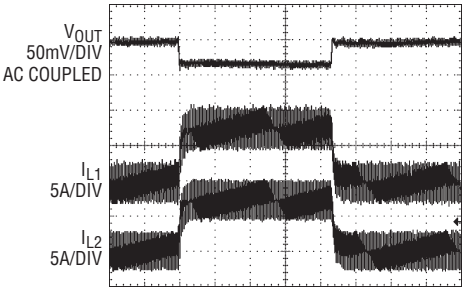
Load Step (Pulse Skip Mode)



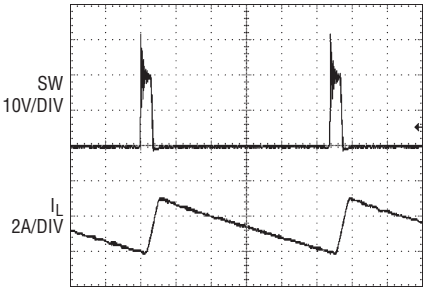
Load Step (Forced Continuous)



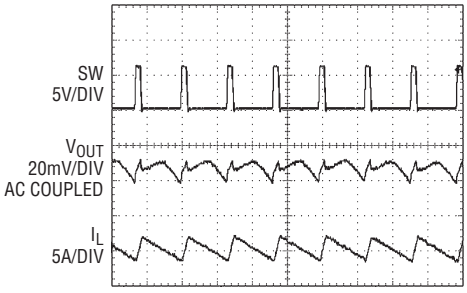
Load Step (Forced Continuous with Voltage Positioning)



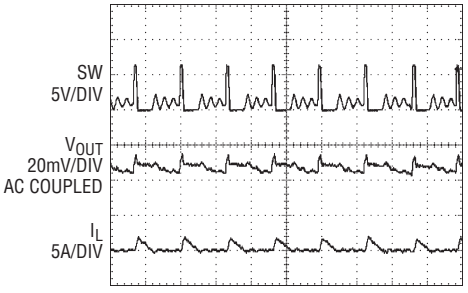
Low Duty Cycle Waveforms



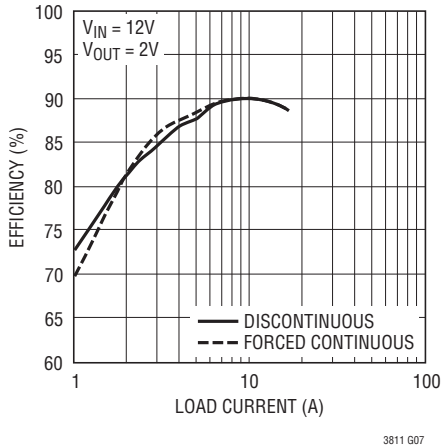
Light Load Waveforms (Forced Continuous Mode)



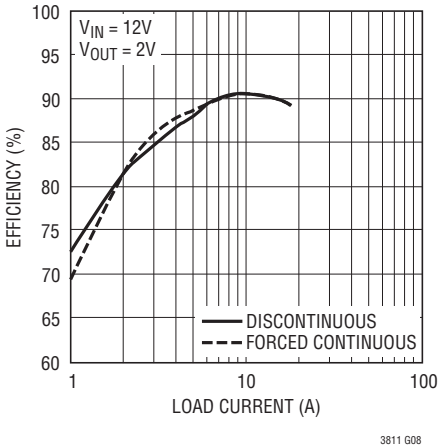
Light Load Waveforms (Pulse Skip Mode)



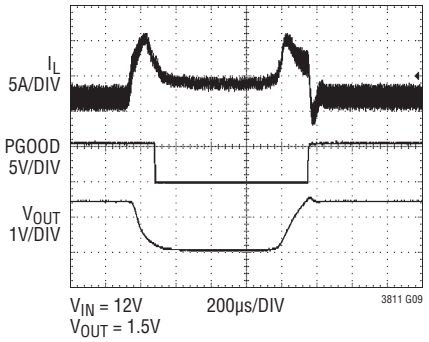
Efficiency vs Load Current with R_{SENSE} = 1.5mΩ



Efficiency vs Load Current with DCR Sensing

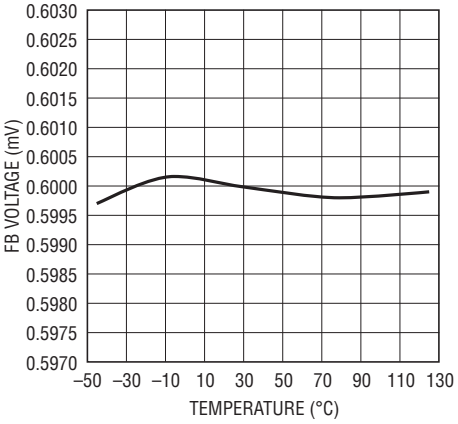


Short-Circut Waveforms

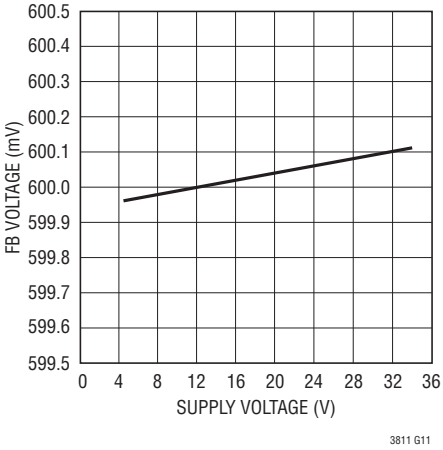


TYPICAL PERFORMANCE CHARACTERISTICS

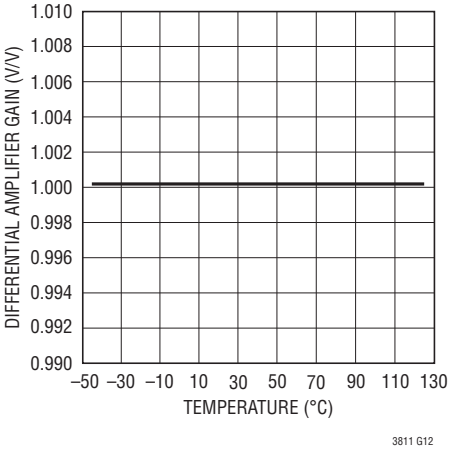
FB Voltage vs Temperature



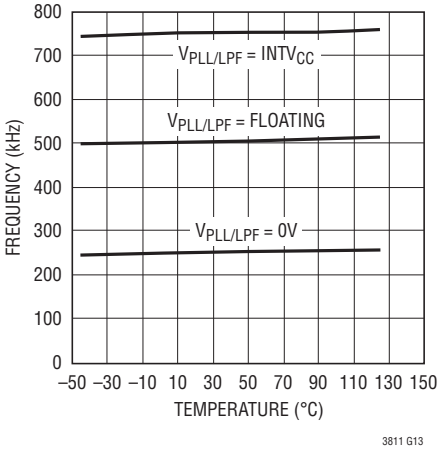
FB Voltage Line Regulation



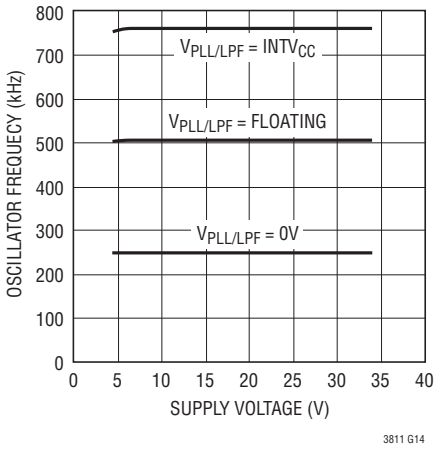
Differential Amplifier Gain vs Temperature



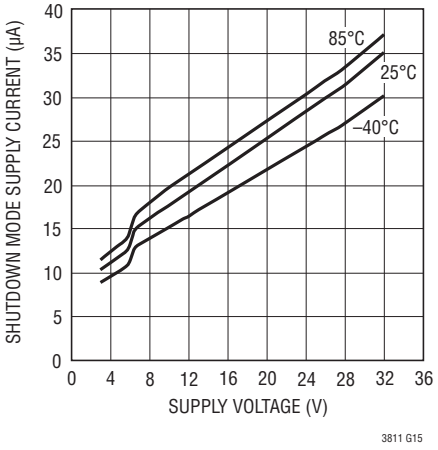
Oscillator Frequency vs Temperature



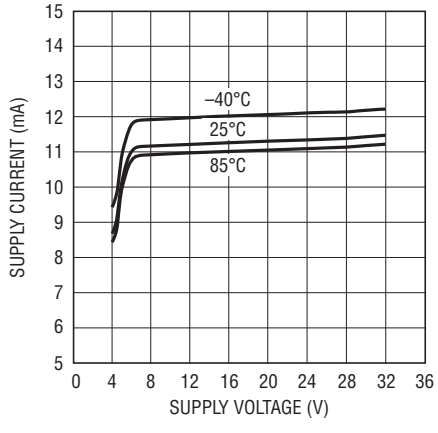
Oscillator Frequency vs Supply Voltage



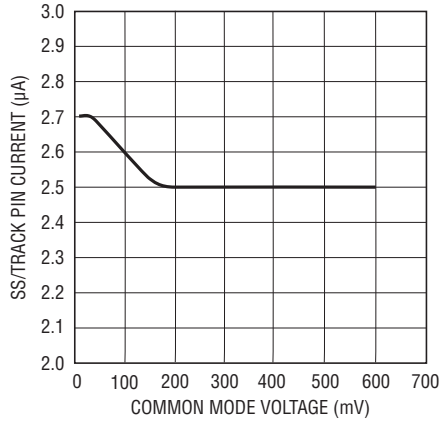
Shutdown Mode Supply Current vs Supply Voltage



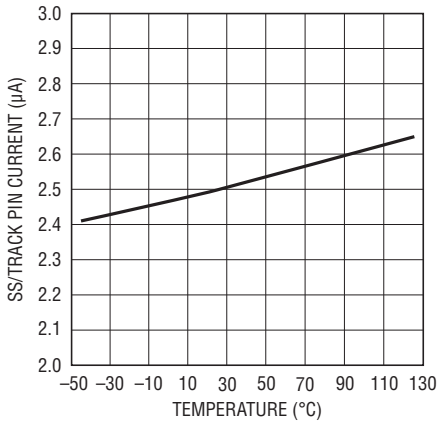
Supply Current vs Supply Voltage



SS/TRACK Pin Current vs Common Mode Voltage

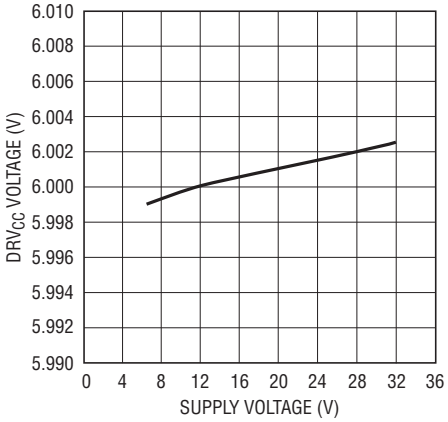


SS/TRACK Pin Current vs Temperature



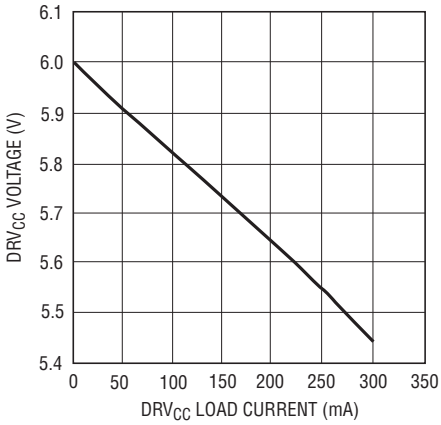
TYPICAL PERFORMANCE CHARACTERISTICS

DRV_{CC} Line Regulation



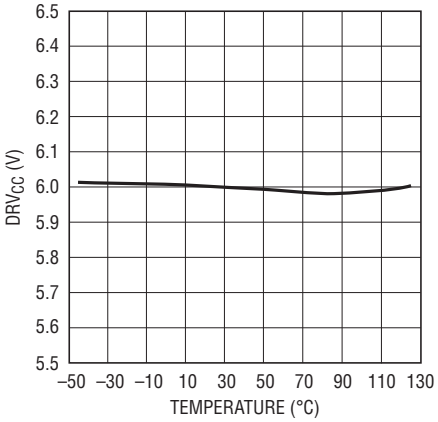
3811 G19

DRV_{CC} Load Regulation



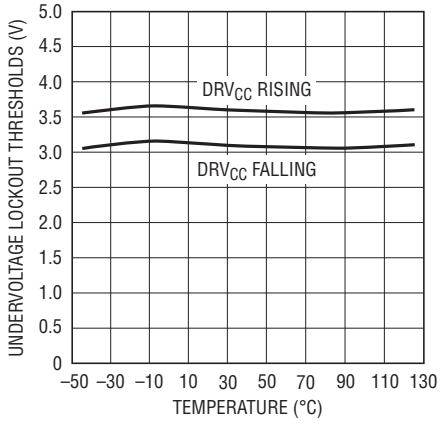
3811 G20

DRV_{CC} vs Temperature



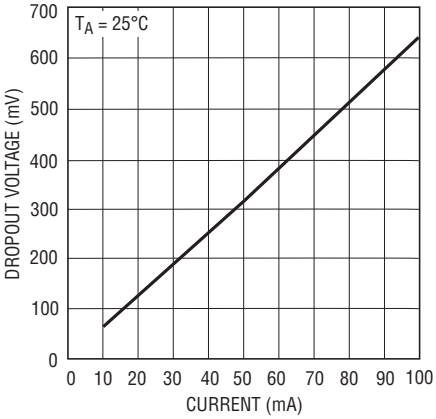
3811 G21

DRV_{CC} Undervoltage Lockout Thresholds vs Temperature



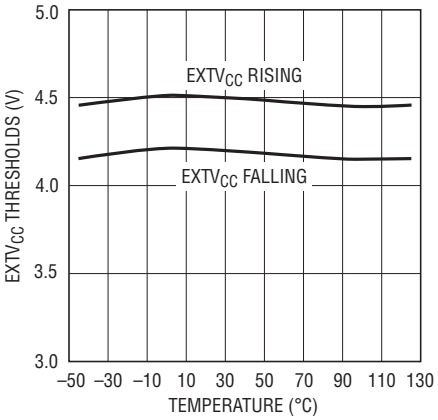
3811 G22

LDO Dropout Voltage vs Current



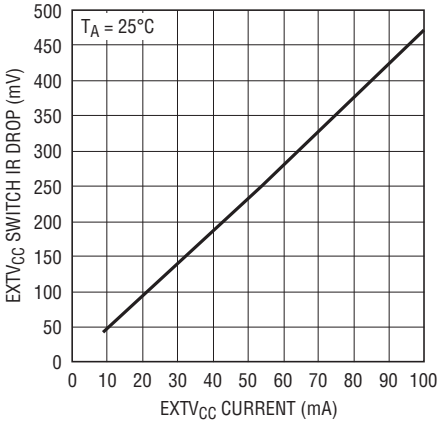
3811 G23

$EXTV_{CC}$ Thresholds vs Temperature



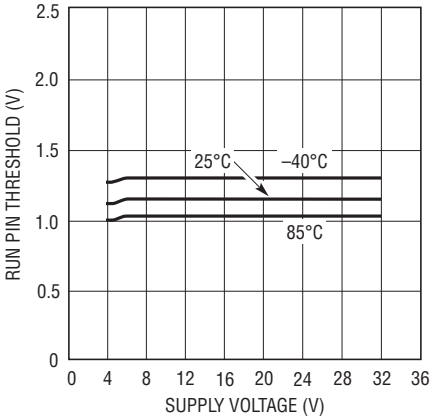
3811 G24

$EXTV_{CC}$ Switch IR Drop vs Current



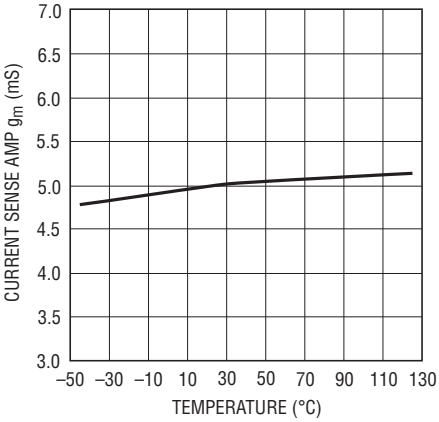
3811 G25

RUN Pin Threshold vs Supply Voltage



3811 G26

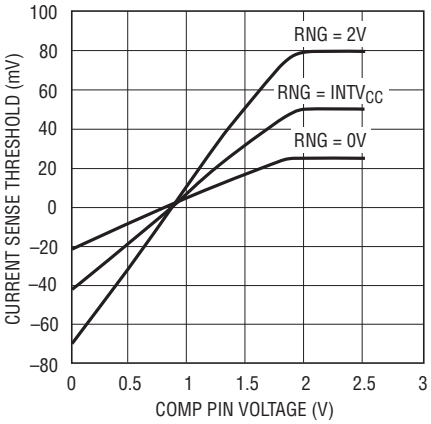
Current Sense Amplifier g_m vs Temperature



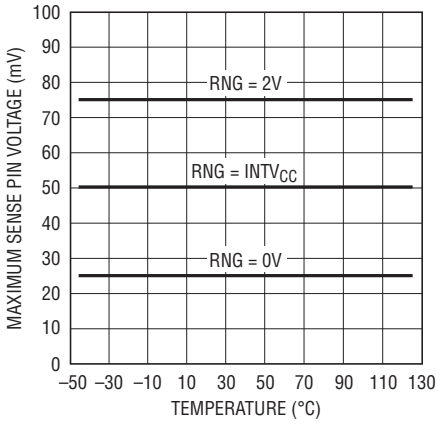
3811 G27

TYPICAL PERFORMANCE CHARACTERISTICS

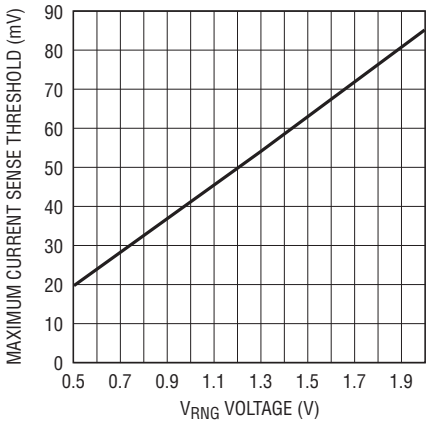
Current Sense Threshold vs COMP Pin Voltage



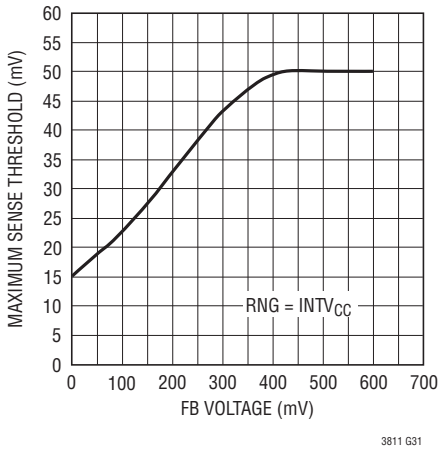
Maximum SENSE Pin Voltage vs Temperature



Maximum Current Sense Threshold vs V_{RNG} Voltage

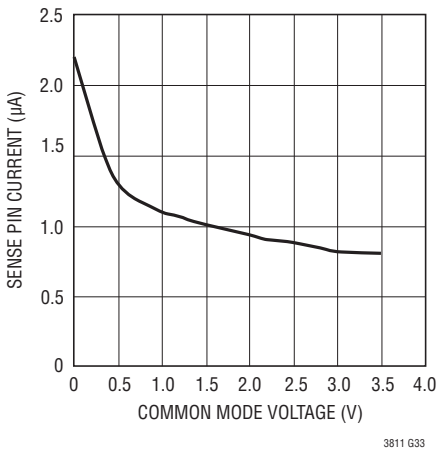


Foldback Current Limit

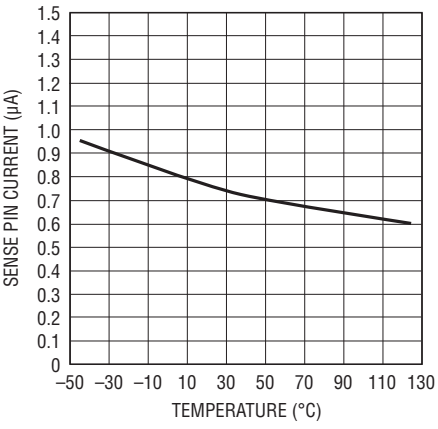


Maximum SENSE Pin Threshold vs Duty Cycle

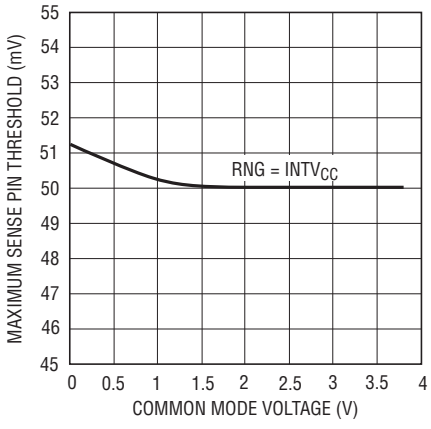
SENSE Pin Current vs Common Mode Voltage



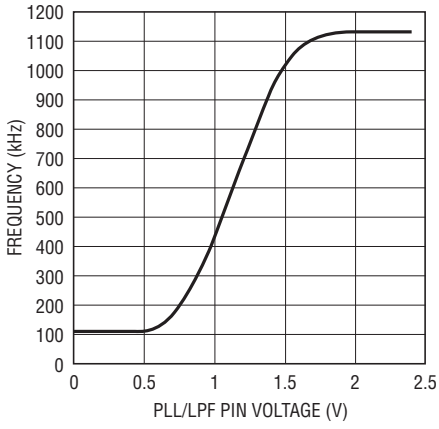
SENSE Pin Current vs Temperature



Maximum SENSE Pin Threshold vs Common Mode Voltage

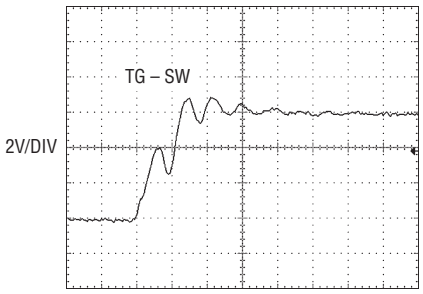


Frequency vs PLL/LPF Pin Voltage

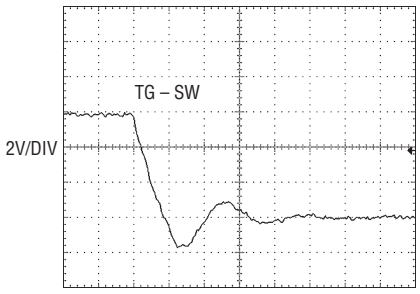


TYPICAL PERFORMANCE CHARACTERISTICS

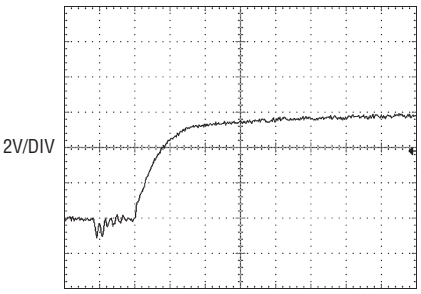
Top Gate Turn-On Waveform Driving Renesas RJK0305DPB



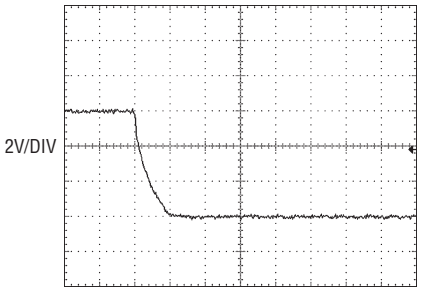
Top Gate Turn-Off Waveform Driving Renesas RJK0305DPB



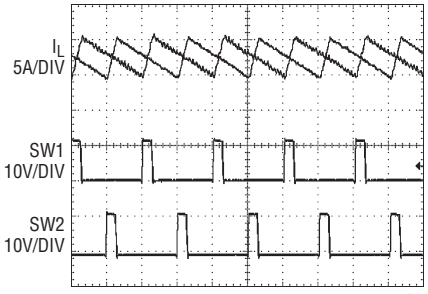
Bottom Gate Turn-On Waveform Driving Renesas RJK0301DPB



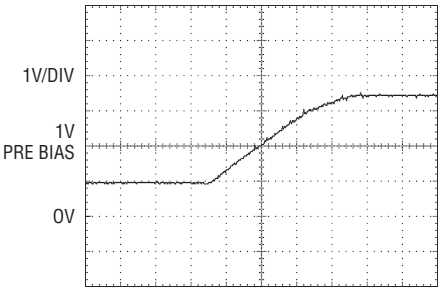
Bottom Gate Turn-Off Waveform Driving Renesas RJK0301DPB



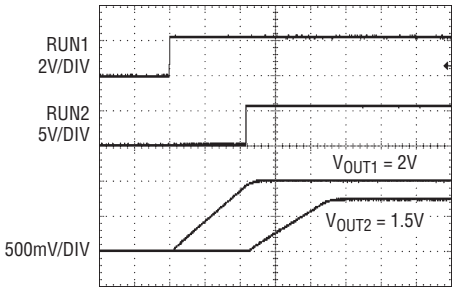
Single Output, 2-Phase Current Sharing Waveforms



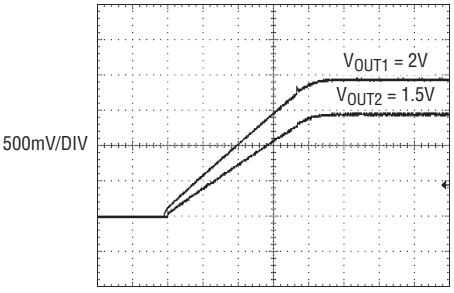
Start-Up Into a Pre-Biased Output Capacitor



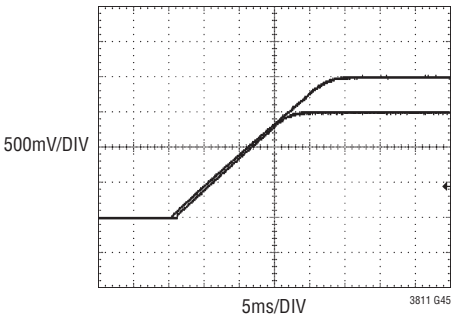
Sequenced Start-Up



Ratiometric Tracking Start-Up



Coincident Tracking Start-Up



PIN FUNCTIONS

BG1, BG2: High Current Gate Driver Outputs for the N-Channel Lower Power MOSFETs.

BOOST1, BOOST2: Bootstrapped Supply Inputs to the Topside Floating Drivers. A low ESR (X5R or better) ceramic bypass capacitor should be connected between the BOOST pin and the SW pin as close as possible to the IC.

CLKOUT: A Digital Output Used for Daisy-Chaining Multiple LTC3811 ICs in Multiphase Systems. The PHASEMODE pin voltage controls the phase relationship between the channel 1 TG signal and CLKOUT.

COMP1, COMP2: Error Amplifier Output Voltages. The error amplifiers in the LTC3811 are high bandwidth, low offset true operational amplifiers that have low output impedance. As a result, the outputs of two active error amplifiers cannot be directly connected together! For multiphase operation, connecting the FB pin of a slave error amplifier to $INTV_{CC}$ will disable the output of that amplifier. Multiphase operation can then be achieved by connecting all of the COMP pins together and using one channel as the master and all of the others as slaves. The FB and COMP pins are also used for compensating the control loop of the converter.

CSOUT (QFN Only): Output of the Voltage Positioning g_m Amplifier. This pin allows the user to program the amount of voltage droop in the output voltage at high load current. The output of the voltage positioning g_m amplifier is a bi-directional current proportional to the ($SENSE^+$ – $SENSE^-$) voltages for both channels. The g_m is internally fixed to 5mS. Forcing the g_m amplifier output current through a low value external resistor will program the amount of voltage droop seen at the output. See Applications Information for more details regarding voltage positioning.

DIFF/IN$^+$: Remote Sense Differential Amplifier Positive Input. A low offset, high bandwidth operational amplifier is configured with four precision 80k resistors for a non-inverting gain of one. This pin is normally connected to the positive terminal of the decoupling capacitor at the load.

DIFF/IN$^-$: Remote Sense Differential Amplifier Negative Input. This pin is normally connected to the negative terminal of the decoupling capacitor at the remote load. The DIFF/IN^+ and DIFF/IN^- PCB traces should be routed as close as possible and parallel to each other from the IC to the output capacitor.

DIFF/OUT: Remote Sense Differential Amplifier Output Voltage, Configured for a Noninverting Gain of One. The voltage at the DIFF/OUT pin is normally connected through an external resistor divider to the FB pin of one channel. The bottom of the divider should be connected to the SGND pin of the IC.

DRV_{CC}: Output of the Internal 6V Low Dropout Regulator (LDO), Supply Pin for the Bottom Gate Drivers and Output of the PMOS $EXTV_{CC}$ Switch. A low ESR (X5R or better) 4.7µF ceramic bypass capacitor should be connected between the DRV_{CC} pin and the PGND pin, as close as possible to the IC.

Exposed Pad (QFN Only): The Exposed Pad of the QFN Leadframe is PGND.

$EXTV_{CC}$: External Power Supply Input to an Internal PMOS Power Switch Connected Between $EXTV_{CC}$ (Drain) and DRV_{CC} (Source). This pin allows an external supply to be used for the high current gate drivers, thereby reducing power dissipation in the LDO and increasing efficiency. When $EXTV_{CC}$ exceeds 4.5V (rising), the high current PMOS switch turns on and shorts $EXTV_{CC}$ to DRV_{CC}, bypassing the internal LDO. See Applications Information for more details.

PIN FUNCTIONS

FB1, FB2: Error Amplifier Feedback Input Pins. The error amplifiers in the LTC3811 are high bandwidth, low offset true operational amplifiers. If differential remote sensing is not used, the FB pin should be connected to a resistor divider from the output of the power supply to SGND with the resistors placed close to the IC. In normal regulation the voltage at the FB pin is 0.6V. If remote sensing is used the FB pin should be connected to a resistor divider from the output of the differential amplifier to SGND. For multiphase operation, connecting the FB pin of a slave error amplifier to $INTV_{CC}$ will disable the output of that amplifier, allowing amplifier outputs to be connected in parallel.

$INTV_{CC}$: Supply Pin for All of the Internal Low Voltage Analog and Digital Control Circuitry, Electrically Isolated from the DRV_{CC} Pin. The $INTV_{CC}$ supply is normally derived by connecting a low value resistor (1Ω) from the output of the LDO (DRV_{CC}) to $INTV_{CC}$ and connecting a 0.1µF low ESR (X5R or better) ceramic bypass capacitor connected from $INTV_{CC}$ to SGND. This RC decoupling configuration prevents gate driver switching noise from coupling into the analog control circuitry. The $INTV_{CC}$ decoupling capacitor should be connected as close as possible to the IC pins.

MODE/SYNC: Mode Control and PLL Synchronization Input. This pin programs the operating mode and serves as the sync input to the internal phase-lock loop (PLL). Connecting this pin to $INTV_{CC}$ forces continuous operation (regardless of the load current) and connecting it to SGND allows discontinuous mode operation at light load. Applying an external clock between 175kHz and 900kHz will cause the operating frequency to synchronize to the clock.

PGND: Power Supply Return Path for the Bottom Side Gate Drivers, Connected to the Sources of the Lower Power MOSFETs. PGND should also be connected to the negative terminal of the DRV_{CC} decoupling capacitor as close as possible to the IC. PGND is electrically isolated from the SGND pin. The Exposed Pad on the bottom of the QFN package is PGND.

PGOOD1, PGOOD2: An Open-Drain NMOS Power Good Output. This output turns on, pulling down the PGOOD pin, when the FB voltage falls out of a ±10% regulation window. The PGOOD monitor circuit contains a 130µs nuisance filter to prevent short duration UV and OV transients from triggering the PGOOD output on, and a 30µs filter for the recovery from a fault condition.

PHASEMODE (QFN Only): The PHASEMODE pin voltage programs the phase relationship between the channel 1 and channel 2 rising TG signals, as well as the phase relationship between the channel 1 TG signal and CLKOUT.

PLL/LPF: Frequency Set and PLL Lowpass Filter Input. When not synchronized, this pin can be used to program the operating frequency. Connecting this pin to SGND forces 250kHz operation and connecting it to $INTV_{CC}$ forces 750kHz operation. Connecting the PLL/LPF pin to a voltage between 0.4V and 2V forces 500kHz operation. When synchronizing to an external clock, this pin serves as the lowpass filter input for the PLL. A series resistor and capacitor connected from PLL/PLF to SGND compensate the PLL feedback loop.

RNG1, RNG2: The voltage at this pin programs the sense voltage range for peak current mode control. Connecting this pin to SGND programs a peak sense voltage of 24mV and connecting it to $INTV_{CC}$ programs a peak sense voltage of 50mV. Alternatively, the sense voltage range can be linearly programmed by programming the RNG pin from 0.6V to 2V with a divider from $INTV_{CC}$ to SGND.

RUN1, RUN2: On/Off Input Pin for Each Controller.

$SENSE1^+$, $SENSE2^+$: Positive Inputs to the Current Comparators and Voltage Positioning g_m Amplifier. The COMP pin voltage programs the current comparator offset in order to set the peak current trip threshold. The LTC3811 is capable of sensing current using a discrete resistor in series with the inductor, or by indirectly sensing the voltage drop across the DCR of the inductor. See Applications Information for more details.

PIN FUNCTIONS

SENSE1⁻, SENSE2⁻: Negative Inputs to the Current Comparators and Voltage Positioning g_m Amplifier. The common mode input voltage range for the current comparators is 0V to 3.5V.

SW1, SW2: Bootstrapped Supply Return Paths for the Topside Gate Drivers, Connected to the Sources of the Upper Power MOSFETs.

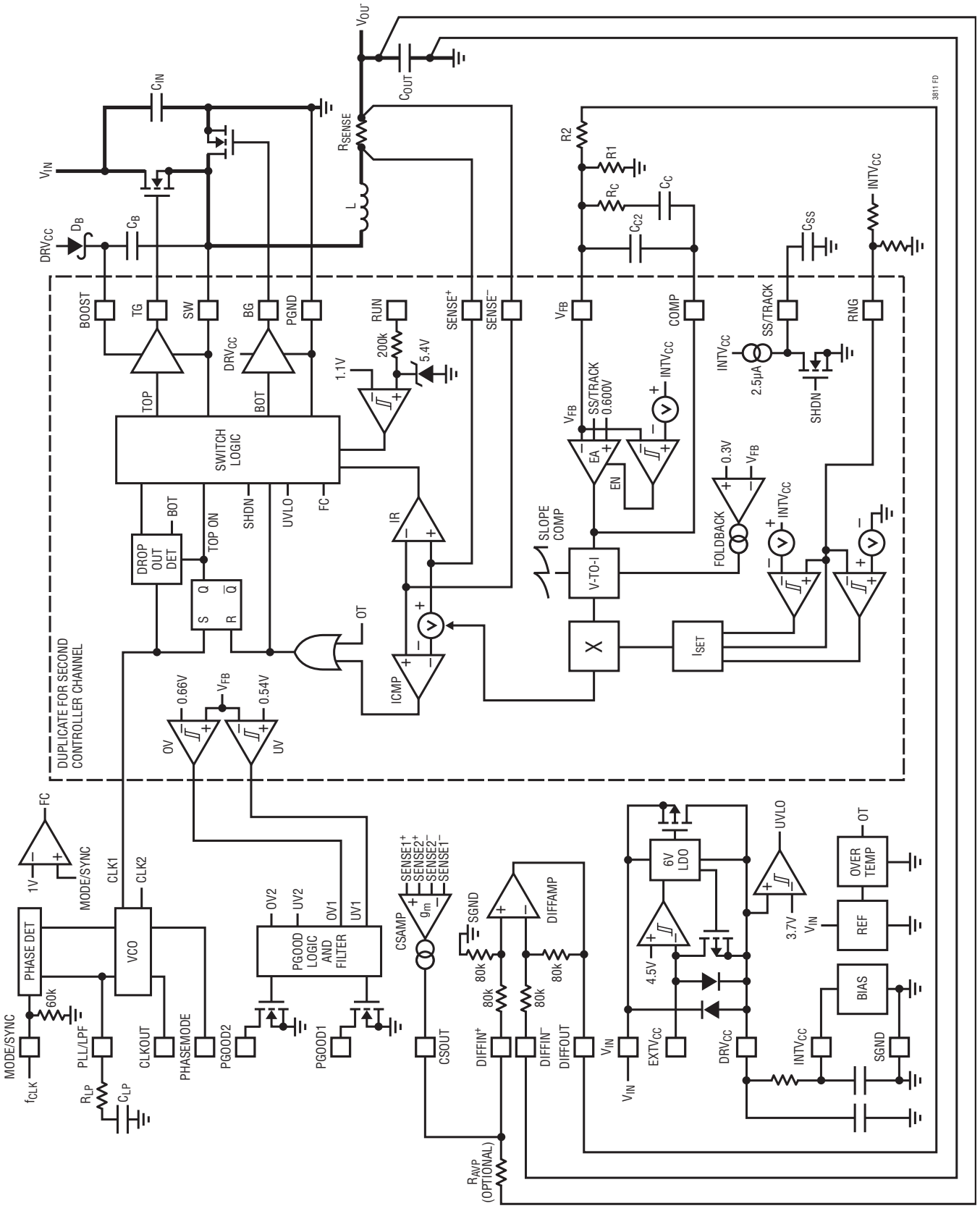
SGND: Signal Ground Pin for the IC. Common to both controllers, this pin should be connected to the negative terminals of the V_{OUT} and $INTV_{CC}$ decoupling capacitors and should be routed separately from any high current paths on the PC board.

SS/TRACK1, SS/TRACK2: Combined Soft-Start and Tracking Inputs. For soft-start operation, connecting a capacitor from this pin to ground will control the voltage ramp at the output of the power supply. An internal 2.5µA current source will charge the capacitor and thereby control an extra input on the reference side of the error amplifier. For tracking operation, this input allows the start-up of a secondary output to track a primary output according to a ratio established by a resistor divider from the primary output to the secondary error amplifier track pin. For coincident tracking of both outputs at start-up, a resistor divider with values equal to those connected to the secondary FB pin from the secondary output should be used to connect the secondary track input from the primary output.

TG1, TG2: High Current Gate Driver Outputs for the N-Channel Upper Power MOSFETs.

V_{IN}: Main Supply Input. A low ESR ceramic bypass capacitor should be connected between this pin and SGND.

FUNCTIONAL DIAGRAM



OPERATION (Refer to the Functional Diagram)

Main Control Loop

The LTC3811 uses a constant frequency peak current mode control architecture. During normal operation, the top MOSFET is turned on each cycle when the oscillator sets the PWM latch and turned off when the main current comparator (ICMP) resets the latch. The peak current at which comparator ICMP resets the latch is controlled by the voltage on the COMP pin, which is the output of the error amplifier. The remote sense amplifier (DIFFAMP) produces a signal equal to the differential voltage sensed across the output capacitor and re-references it to the local IC ground reference (SGND). The FB pin receives a portion of this voltage feedback signal and compares it to the internal 0.6V reference. When the load current increases it causes a slight decrease in the FB pin voltage relative to the 0.6V reference, which in turn causes the COMP pin voltage to rise until the average inductor current is equal to the load current.

The top MOSFET drivers are biased from a floating bootstrap capacitor, C_B, which is normally recharged during the off-time through an external Schottky diode. When V_{IN} decreases to a voltage close to V_{OUT}, however, the loop may enter dropout and attempt to turn on the top MOSFET continuously. A dropout detector senses this condition and forces the top MOSFET to turn off every 10th cycle for one third of a cycle to recharge the bootstrap capacitor.

Differences Between the QFN and G36 Package Options

The LTC3811 is offered in two package options, a 38-pin QFN and a 36-pin SSOP. The full featured QFN package option has no leads and an exposed lead frame that needs to be soldered to the PCB, whereas the 36-pin SSOP has leads and is therefore slightly easier to solder to a PCB and to debug in the lab.

The primary electrical difference between the QFN and SSOP options is the SSOP version lacks the CSOUT and PHASEMODE pins. With no CSOUT pin, the SSOP version has no provision for output voltage positioning. With no PHASEMODE input (it is internally connected to SGND), the SSOP version is limited to 2-phase and 4-phase applications.

In addition to differences in pinout, another difference between the two package options is their thermal resistance. The QFN package, by virtue of its exposed lead frame, has a junction-to-ambient thermal resistance of only 34°C/W, whereas the SSOP package has a thermal resistance of 100°C/W. The power dissipation of the IC is a function of the input voltage, the gate charge of the external power MOSFETs and the operating frequency. The gate charge losses can be partially mitigated by using the $EXTV_{CC}$ input to supply power to the IC, but users should beware that high input voltage applications using very high gate charge power MOSFETs, that also need to operate at high frequency, should only be attempted using the QFN package option. More details covering thermal management are given later in this data sheet.

Supplying Power to the LTC3811

The LTC3811 features several power supply input pins and multiple ways of supplying power to the gate drivers and low voltage analog control circuitry.

The first method of supplying power to the IC uses the internal low dropout linear regulator (LDO) that draws power from V_{IN} and regulates DRV_{CC} to 6V, as shown in Figure 1. The DRV_{CC} input supplies power to the internal gate drivers, which are capable of very high peak transient charge (1A) and discharge (5A) currents. The DRV_{CC} supply should be decoupled to PGND with a minimum of 4.7µF low ESR ceramic (X5R or better) capacitance. If multiple power MOSFETs are being driven in parallel for high current applications it is recommended that this capacitance

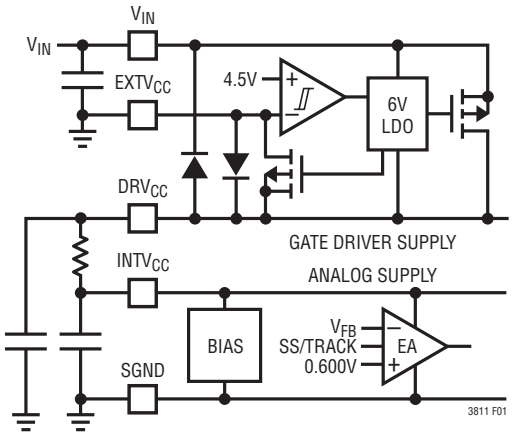


Figure 1. Supplying Power to the LTC3811 from V_{IN}

OPERATION (Refer to the Functional Diagram)

be increased to 10µF. Because of the high peak current capability of the gate driver, it is essential that this capacitor be placed as close as possible to DRV_{CC} and PGND pins, and on the same PCB layer as the IC.

The $INTV_{CC}$ pin supplies power to all of the low voltage analog circuitry and is electrically isolated from DRV_{CC}. The $INTV_{CC}$ supply is normally derived from DRV_{CC} through an RC filter, in order to prevent gate driver supply noise from coupling into sensitive analog control circuitry. Typical values for this RC filter consist of a 1Ω resistor from DRV_{CC} to $INTV_{CC}$ and a 0.1µF low ESR ceramic capacitor from $INTV_{CC}$ to SGND. The $INTV_{CC}$ capacitor should be placed as close as possible to the $INTV_{CC}$ and SGND pins and on the same PCB layer as the IC.

A third power supply pin, $EXTV_{CC}$, serves as an auxiliary input for applications where the power dissipation in the internal LDO is excessive, or where maximum efficiency is essential. This configuration is shown in Figure 2. When the $EXTV_{CC}$ pin is left open or is connected to a voltage less than 4.5V, the internal 6V LDO supplies DRV_{CC} power from V_{IN}. If $EXTV_{CC}$ is tied to an external power supply greater than 4.5V, however, the 6V LDO is turned off and power is supplied to DRV_{CC} through a 5Ω PMOS switch from $EXTV_{CC}$. For 4.5V < $EXTV_{CC}$ < 7V this PMOS switch is on and DRV_{CC} is approximately equal to $EXTV_{CC}$. Using the $EXTV_{CC}$ pin allows the gate driver and control power to be derived from a high efficiency external source, dramatically reducing power dissipation on the IC.

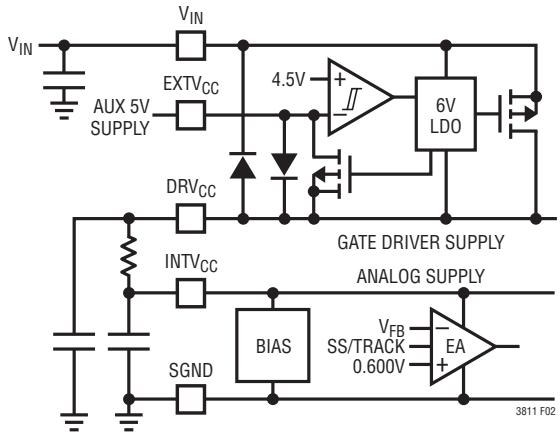


Figure 2. Supplying Power to the LTC3811 from $EXTV_{CC}$

Using an External 5V Supply to Measure Dynamic Quiescent Current

When a voltage above 4.5V is applied to the $EXTV_{CC}$ pin, the internal LDO in the LTC3811 is switched off and the power is supplied by the external 5V power supply as shown in Figure 2. Under these conditions, the quiescent current at the V_{IN} pin of the IC is very low (less than 1mA), and most of the current required to power the analog control circuitry and the gate drivers flows into the $EXTV_{CC}$ pin. As a result, this auxiliary supply can be used as a diagnostic tool in order to measure the total current for thermal calculations. In order to match the actual condition when the internal LDO is on, the voltage applied to $EXTV_{CC}$ when the measurements are taken should be 6V (the same as the regulated LDO output voltage).

Once the total quiescent current for the application is known, the power dissipation, P_D, on the IC will be approximately I_{EXTVCC} times V_{IN}, since the gate drive current and control circuitry quiescent current would be required to flow through the V_{IN} pin. The junction temperature of the IC can then be estimated using the following well-known formula:

$$T_J = T_A + (P_D \bullet R_{\theta JA})$$

If the maximum junction temperature is close to the Absolute Maximum Rating for the particular device being used, the use of an auxiliary supply and the $EXTV_{CC}$ pin may be required. Alternatively, lower gate charge MOSFETs should be used or the switching frequency should be reduced.

Operation at Low Supply Voltage

The LTC3811 control circuit has a minimum input voltage of 4.5V, making it a good choice for applications that experience low supply conditions. However, care should be taken to determine the minimum gate drive supply voltage in order to choose the optimum power MOSFETs. Important parameters that can affect the minimum gate drive voltage are the minimum input voltage (V_{IN}), the LDO dropout voltage, and the $EXTV_{CC}$ supply voltage, if an external gate drive supply is being used.

OPERATION (Refer to the Functional Diagram)

If the internal LDO is supplying power to the gate driver and the input voltage is low enough for the LDO to be in dropout, then the minimum gate drive supply voltage is:

$$V_{DRVCC} = V_{IN(MIN)} - V_{DROPOUT}$$

The LDO dropout voltage is a function of the total gate drive current and the quiescent current of the IC (typically 10mA). A curve of dropout voltage vs output current for the LDO is shown in the Typical Performance Characteristics. The temperature coefficient of the LDO dropout voltage is approximately +4000ppm/°C.

The total Q-current ($I_{Q(TOT)}$) flowing in the LDO is the sum of the controller quiescent current (typically 10mA) and the total gate charge drive current.

$$I_{Q(TOT)} = I_Q + Q_{G(TOT)} \bullet f$$

If an external supply is being used to supply power to the gate driver through the $EXTV_{CC}$ pin, then the minimum gate drive supply voltage is:

$$V_{DRVCC} = V_{EXTVCC} - I_{Q(TOT)} \bullet R_{EXTVCC}$$

The resistance of the internal $EXTV_{CC}$ PMOS switch is typically 5Ω at 25°C and has a temperature coefficient of approximately 3400ppm/°C.

After the calculations have been completed, it is important to measure the gate drive waveforms (BG-to-PGND and TG-to-SW) and the gate driver supply voltage (DRV_{CC}-to-PGND) over all operating conditions (low V_{IN}, mid V_{IN}, and high V_{IN}, as well as from light load-to-full load) to ensure adequate power MOSFET enhancement. Consult the power MOSFET data sheet to determine the actual $R_{DS(ON)}$ for the measured V_{GS}, and verify your thermal calculations by measuring the component temperatures using an infrared camera.

On/Off Control Using the RUN Pin

The two channels of the LTC3811 can be independently turned on and off using the RUN1 and RUN2 pins. Pulling either of these pins low shuts down the main control loop for that channel. Pulling both pins low disables both controllers and most of the internal circuitry, including the DRV_{CC} low dropout regulator (LDO). In shutdown mode (both RUN pins low) the LTC3811 typically draws only 20µA of current.

The RUN pins may be externally pulled up or driven directly by logic. Be careful not to exceed the 7V absolute maximum rating on this pin.

Soft-Start and Tracking Using the SS/TRACK Pin

The start-up of each controller's output voltage V_{OUT} is normally controlled by the voltage on the SS/TRACK pin for that channel. The SS/TRACK pin represents a 2nd noninverting input to the error amplifier, as shown in Figure 3. The error amplifier is configured so that the lower of the two noninverting inputs (the SS/TRACK pin or the 0.6V reference) controls the feedback loop. That is, when the voltage on the SS/TRACK pin is less than the 0.6V internal reference, the LTC3811 regulates the FB pin voltage to be approximately equal to the SS/TRACK pin voltage instead of the internal 0.6V reference. This allows the user to connect a capacitor from the SS/TRACK pin to SGND to program the soft-start of the power supply output. An internal 2.5µA current source charges this capacitor, creating a voltage ramp on the SS/TRACK pin. As the SS/TRACK pin voltage rises from 0V to 0.6V, the output voltage, V_{OUT}, rises smoothly from 0V to its final value. Once the soft-start interval is over, the internal 2.5µA current source will continue to charge the SS/TRACK capacitor up to a maximum voltage equal to $INTV_{CC}$.

Alternately, the SS/TRACK pin can be used to force the start-up of V_{OUT} to track the voltage of another supply. Typically, this requires connecting the SS/TRACK pin to an external divider from the other supply to ground (see Applications Information).

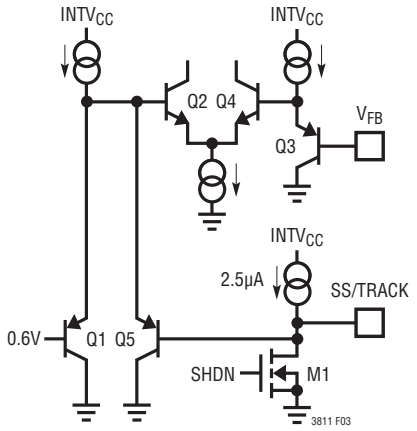


Figure 3. Simplified LTC3811 Error Amplifier Input Stage

OPERATION (Refer to the Functional Diagram)

The SS/TRACK pin has an internal open-drain NMOS pull-down transistor that turns on when the corresponding RUN pin is pulled low to disable that controller, when the voltage on the DRV_{CC} pin is below 3.7V (the rising undervoltage lockout threshold), or during an overtemperature condition. During an undervoltage lockout, UVLO, or overtemperature, OT, condition, both controllers are disabled and the external MOSFETs are held off.

In multiphase applications, one master error amplifier is used to control all of the phase current comparators. The FB pins for the unused error amplifiers are connected to $INTV_{CC}$ in order to three-state these amplifier outputs. As a result, the SS/TRACK pins for the unused error amplifiers should be left open.

Programming the Operating Mode

The MODE/SYNC pin serves to either program the operating mode or to synchronize the operating frequency to an external clock using the internal PLL. Connecting the MODE/SYNC pin to ground programs pulse-skip mode operation and connecting the pin to $INTV_{CC}$ programs forced continuous operation, as shown in Table 1. In pulse-skip mode the inductor current is not allowed to reverse, resulting in discontinuous mode, DCM, operation at light load. Pulse-skip mode is ideal for applications where light load efficiency is a higher priority than transient response. In forced continuous mode, the synchronous switch turns on after the primary switch turns off and remains on for the duration of the clock cycle, regardless of the load current. Forced continuous mode is ideal for applications needing optimized transient response, or for systems where constant frequency operation is important.

Certain applications can result in the startup of the converter into a non-zero load voltage, where residual charge is stored on the output capacitor at the onset of converter switching. In order to prevent a reversal of current in the inductor under these conditions, pulse-skip operation is asserted at startup until the FB pin reaches the lower PGOOD threshold of 0.54V. Once the FB pin voltage exceeds 0.54V, the operating mode is determined by the voltage on the MODE/SYNC pin.

When the operating frequency of the converter is synchronized to an external clock using the MODE/SYNC pin, the operating mode will always be forced continuous. Forcing continuous mode operation results in constant frequency operation and a more predictable noise spectrum from the converter.

Table 1

MODE/SYNC	OPERATING MODE	DESCRIPTION
SGND	Pulse-Skip	DCM Operation at Light Load
$INTV_{CC}$	Forced Continuous	CCM from No Load to Full Load
External Clock	Forced Continuous	Operating Frequency Synchronized Using Internal PLL (CCM)

Frequency Selection and the Phase-Lock Loop

The selection of the switching frequency is a tradeoff between efficiency, transient response and component size. Low frequency operation increases efficiency by reducing MOSEFT switching losses, but requires a larger inductor and output capacitor to maintain low output ripple.

The switching frequency of the LTC3811's controllers can be selected using the PLL/LPF pin. If the MODE/SYNC pin is not being driven by an external clock, the PLL/LPF pin can be tied to SGND, left open or tied to $INTV_{CC}$ to select 250kHz, 500kHz or 750kHz, respectively, as shown in Table 2.

Table 2

PLL/LPF	MODE/SYNC	FREQUENCY
SGND	0V or $INTV_{CC}$ (DC)	250kHz
Floating	0V or $INTV_{CC}$ (DC)	500kHz
$INTV_{CC}$	0V or $INTV_{CC}$ (DC)	750kHz
RC Filter to SGND	Connected to External Clock	Phase Locked to External Clock

A phase-lock loop is available on the LTC3811 to synchronize the internal oscillator to an external clock source connected to the MODE/SYNC pin. In this case, a series RC network connected from the PLL/LPF pin to SGND serves as the PLL's loop filter. The PLL/LPF pin is both the output of the phase detector and the input to the voltage controlled oscillator, VCO. The LTC3811 phase detector adjusts the voltage on the PLL/LPF pin to align the rising edge of TG1 to the leading edge of the external clock signal. The turn-on of the second channel TG2 will depend upon the voltage on the PHASEMODE pin as shown in the Electrical Characteristics.

OPERATION (Refer to the Functional Diagram)

The typical capture range of the LTC3811's PLL is approximately 125kHz to 1.1MHz, with a guarantee over all manufacturing variations to be between 175kHz and 900kHz. The amplitude of the sync pulse to the LTC3811 should be greater than 1.8V and the minimum pulse width should be greater than 200ns.

Using the CLKOUT and PHASEMODE Pins in Multiphase Applications

The LTC3811 features two pins (CLKOUT and PHASEMODE) that allow multiple LTC3811 ICs to be daisy-chained together in multiphase applications. The clock output signal on the CLKOUT pin can be used to synchronize additional power stages in a multiphase power supply solution feeding a single high current output or even separate outputs. The PHASEMODE pin is used to adjust the phase relationship between channel 1 and channel 2, as well as the phase relationship between channel 1 and CLKOUT, as summarized in Table 3. The phases are calculated relative to the zero degrees, defined as the rising edge of the top gate driver output of channel 1, TG1.

The PHASEMODE input comparators are referenced to an internal divider from $INTV_{CC}$ that has 33% and 67% $INTV_{CC}$ thresholds. For 6-phase operation, connect PHASEMODE to an external divider from $INTV_{CC}$ with equal value resistors (e.g., 100k), so that PHASEMODE is always 50% of $INTV_{CC}$.

Table 3

# PHASES	IC #	PHASEMODE	CLKOUT CONNECTS TO
2	1	0V	N/A
3	1	$INTV_{CC}$	MODE/SYNC of IC # 2
	2	0V	N/A
4	1	0V	MODE/SYNC of IC # 2
	2	0V	N/A
6	1	50% $INTV_{CC}$	MODE/SYNC of IC # 2
	2	50% $INTV_{CC}$	MODE/SYNC of IC # 2
	3	50% $INTV_{CC}$	N/A
12	1	50% $INTV_{CC}$	MODE/SYNC of IC # 2
	2	50% $INTV_{CC}$	MODE/SYNC of IC # 3
	3	0V	MODE/SYNC of IC # 4
	4	50% $INTV_{CC}$	MODE/SYNC of IC # 5
	5	50% $INTV_{CC}$	MODE/SYNC of IC # 6
	6	50% $INTV_{CC}$	N/A

Remote Sensing Using the Differential Amplifier

The LTC3811 has a differential amplifier for true remote sensing of the output voltage. The sensing connections should be returned from the load back to the differential amplifier's inputs through a common, tightly coupled pair of PCB traces. The differential amplifier rejects common mode signals capacitively or inductively radiated into the feedback PCB traces, as well as ground loop disturbances. The differential amplifier output signal is typically divided down and compared with the internal precision 0.6V voltage reference by the error amplifier.

The differential amplifier utilizes four precision internal resistors to enable instrumentation-type measurement of the output voltage. The amplifier has a gain of 1.000, contains a CMOS rail-to-rail output stage, and is optimized for low input offset and high bandwidth.

The output voltage is set by an external resistive divider according to the following formula:

$$V_{OUT} = 0.6 \bullet \left[1 + \frac{R2}{R1}\right]$$

where R2 and R1 are the upper and lower divider resistors, respectively. The differential amplifier was optimized for divider currents in the range of 100µA to 600µA, meaning that R1 in the equation above should be 1k to 6k.

Using the LTC3811 Operational Error Amplifiers in Multiphase Applications

The LTC3811 error amplifiers are true operational amplifiers, meaning that they have high DC gain and low output impedance. In previous generations of multiphase controllers, such as the LTC1628 family, the error amplifiers were transconductance amplifiers, meaning that they could be connected in parallel for multiphase applications.

Multiphase applications using the LTC3811 will use one operational error amplifier as the master and will disable all of the slave phase error amplifiers. Typically, the channel 1 amplifier for phase = 0° will be used as the master and phases 2 through n (up to 12 phases) will serve as slaves. To disable the slave error amplifiers but still use their current comparators and power stages, connect the

OPERATION (Refer to the Functional Diagram)

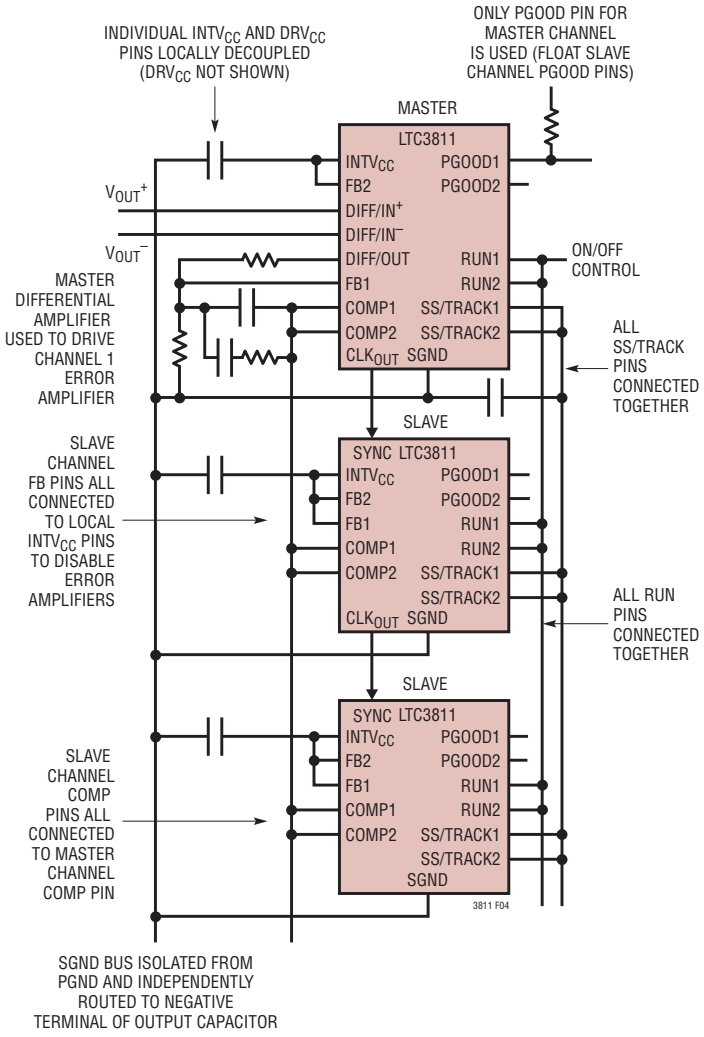


Figure 4. LTC3811 Error Amplifier Configuration for Multiphase Operation

FB pin of a slave phase to $INTV_{CC}$. As shown in the Functional Diagram, a comparator detects when the FB pin is shorted to $INTV_{CC}$ and three-states this amplifier's output and input. The COMP pins for all of the phases can then be shorted together in order to provide compensation for the feedback loop, as shown in Figure 4.

Theory and Benefits of Multiphase Operation

Why the need for multiphase operation? Up until the multiphase family, constant frequency dual switching regulators operated both channels in phase (i.e., single-phase operation). This means that both switches turned on at the same time, causing current pulses of up to twice the amplitude of those for one regulator to be drawn from the input capacitor. These large amplitude current pulses increased the total RMS current flowing from the input capacitor, requiring the use of more expensive input capacitors and increasing both EMI and losses in the input capacitor.

With multiphase operation, the two channels of the dual-switching regulator are operated 180 degrees out of phase. This effectively interleaves the current pulses drawn by the switches, greatly reducing the overlap time where they add together. *The result is a significant reduction in total RMS input current, which in turn allows less expensive input capacitors to be used, reduces shielding requirements for EMI and improves real world operating efficiency.*

Figure 5 illustrates the benefits of multiphase operation. Current ripple at the input is reduced by a factor of 1.41 (square root of 2), reducing the size and cost of the input capacitor. In addition, since power losses are proportional to I_{RMS}^2, significant efficiency improvements in the input power path components (batteries, switches, protection circuitry and PCB traces) can be achieved. Improvements in both conducted and radiated EMI also directly accrue as a result of the reduced RMS input current.

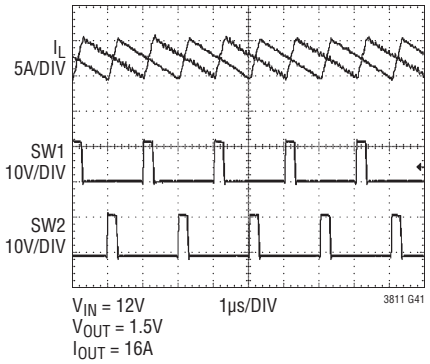


Figure 5. 2-Phase, Single Output Current Sharing Waveforms

Of course, the improvement afforded by 2-phase operation is a function of the dual switching regulator's relative duty cycles which, in turn, are dependent upon the input voltage V_{IN} (Duty Cycle = V_{OUT}/V_{IN}).

Figure 6 shows the net ripple current seen by the output capacitors for the different phase configurations. The output ripple current is plotted for a fixed output voltage as the duty factor is varied between 10% and 90% on the

OPERATION (Refer to the Functional Diagram)

x-axis. The output ripple current is normalized against the inductor ripple current at zero duty factor. The graph can be used in place of tedious calculations. As shown in Figure 6, the zero output ripple current is obtained when:

$$\frac{V_{OUT}}{V_{IN}} = \frac{k}{N} \quad \text{where } k = 1, 2, ..., N-1$$

So the number of phases used can be selected to minimize the output ripple current and therefore the output ripple voltage at the given input and output voltages. In applications having a highly varying input voltage, additional phases will produce the best results.

Accepting larger values of ΔI_L allows the use of low inductances, but can result in higher output voltage ripple. A reasonable starting point for setting ripple current is $\Delta I_L = 0.4(I_{OUT})/N$, where N is the number of channels and I_{OUT} is the total load current. Remember, the maximum ΔI_L occurs at the maximum input voltage. The individual inductor ripple currents are constant determined by the inductor, input and output voltages.

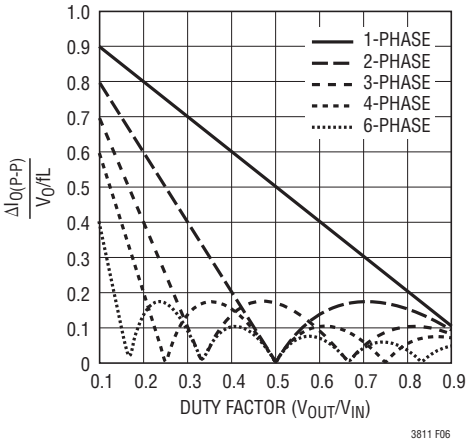


Figure 6. Normalized Peak Output Current vs Duty factor [$I_{RMS} \approx 0.3(\Delta I_{O(P-P)})$]

Power Good Pins (PGOOD1, PGOOD2)

Each PGOOD pin is connected to the open drain of an internal N-channel pull-down MOSFET. The MOSEFT turns on and pulls the PGOOD pin low when the corresponding FB pin is outside a ±10% window around the 0.6V reference voltage. The PGOOD pin is also pulled low when the corresponding RUN pin is low, or during an undervoltage lockout or overtemperature condition. When the FB pin voltage is within the ±10% window, the internal PGOOD MOSFET is turned off and the pin is normally pulled up by an external resistor. The absolute maximum voltage rating of the PGOOD pins is 7V.

The PGOOD logic contains separate filters depending on whether the controller is entering or exiting a fault condition. When the FB pin is exiting a fault condition (such as during normal output voltage start-up, prior to regulation), the PGOOD pin will remain low for an additional 30µs. This allows the output voltage to reach steady-state regulation and prevents the enabling of a heavy load from re-triggering a UVLO condition. When the FB pin is entering either an undervoltage, UV, or overvoltage, OV, fault condition, the PGOOD pin will remain high 130µs after the onset of the fault. This non-integrating filter prevents noise or short duration overload conditions from triggering the PGOOD outputs and causing a false system reset. Figure 7 illustrates the timing diagram for a hypothetical undervoltage event on the FB pin, and the resulting PGOOD waveform.

In multiphase applications, one error amplifier is used to control all of the phase current comparators. In addition, since the FB pins for the unused error amplifiers are connected to $INTV_{CC}$ (in order to three-state these amplifiers), the PGOOD outputs for these amplifiers will be asserted. In order to prevent falsely reporting a fault condition, the

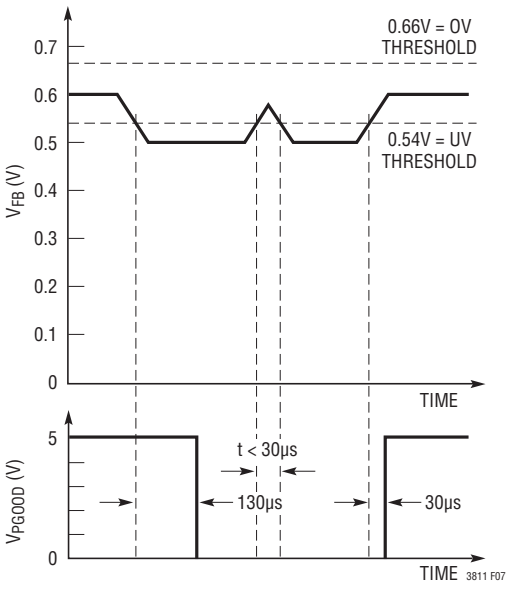


Figure 7. PGOOD Filter Timing Diagram

OPERATION (Refer to the Functional Diagram)

PGOOD outputs for the unused error amplifiers should be left open. Only the PGOOD output for the master control error amplifier should be connected to the fault monitor.

Fault Conditions: Current Limit and Foldback

One of the main advantages of the LTC3811 is the fact that the maximum inductor current is inherently limited due to the use of peak current mode control. The maximum sense voltage is controlled by the voltage on the RNG pins and the maximum DC output current is:

$$I_{LIMIT} = \frac{V_{SENSE(MAX)}}{R_{SENSE}} - \frac{1}{2} \bullet \Delta I_L$$

The current limit value should be checked to ensure that $I_{LIMIT(MIN)} > I_{OUT(MAX)}$. The minimum value of the current limit generally occurs with the largest V_{IN} at the highest ambient temperature, conditions that cause the largest power losses in the converter.

To further limit current in the event of an output short-circuit to ground, the LTC3811 includes foldback current limiting. When the FB pin falls below 0.3V (50% of its nominally regulated value), the foldback circuit is activated, progressively lowering the peak current limit in proportion to the severity of the overcurrent or short circuit condition. If the FB pin reaches 0V, the peak current sense threshold will be reduced to 30% of its maximum value. The foldback current limit transfer function is shown in Figure 8.

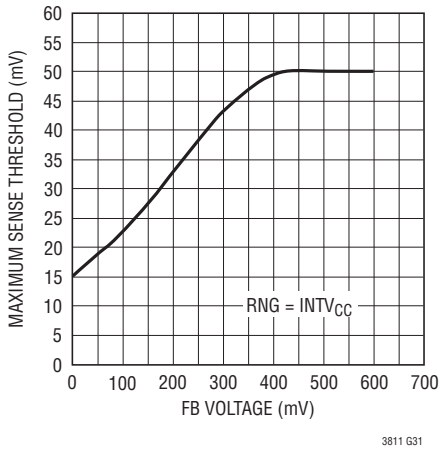


Figure 8. Current Foldback Charactistic

Under short-circuit conditions with very low duty cycles, the LTC3811 may begin to skip pulses in order to limit the maximum current. In this situation the bottom MOSFET will be dissipating most of the power; however this will be less than in normal operation at maximum load. In this case the short circuit ripple current is determined by the minimum on-time, $t_{ON(MIN)}$, of the LTC3811 (about 65ns), the input voltage, and the inductor value, according to the following equation:

$$\Delta I_{L(SC)} = t_{ON(MIN)} \bullet \frac{V_{IN}}{L}$$

The resulting short-circuit current is

$$I_{SC} = \frac{0.3 \bullet V_{SENSE(MAX)}}{R_{SENSE}} - \frac{1}{2} \bullet \Delta I_{L(SC)}$$

Depending upon the ratio of the DC value of the current limit to the maximum load current and the percentage ripple current in the inductor, it is possible that the converter will operate in discontinuous mode when V_{FB} = 0V (a so-called “dead short”). In this case, the short-circuit current of the converter will be:

$$I_{SC} = \frac{\Delta I_{L(SC)}}{2} = t_{ON(MIN)} \bullet \frac{V_{IN}}{2 \bullet L}$$

In order for the converter to start up properly with a nonlinear load, the foldback current limiting circuit in the LTC3811 is disabled during the initial soft-start interval. When the FB pin voltage reaches 0.54V, the soft-start interval is terminated and the foldback circuit is enabled.

In the event the converter is turned on into a shorted load, the foldback circuit will be disabled until the SS/TRACK pin reaches 0.54V. This ensures that the converter will still limit the maximum current to a safe level and reduce the peak power dissipated with a shorted load.

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Duty Cycle Considerations

The duty cycle for a buck converter is well known:

$$D = \frac{V_{OUT}}{V_{IN}} = t_{ON} \bullet f$$

Rearranging, the minimum on-time for a given application can be calculated:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)} \bullet f}$$

For a given input and output voltage, it is important to know how close the minimum on-time of the application comes to the minimum on-time of the control IC. The LTC3811 has a typical minimum on-time of 65ns, allowing both high input to output ratios and high frequency operation.

In an application circuit, if the IC's minimum on-time exceeds the value required in the duty cycle equations, the converter will begin to skip pulses and operate at a fraction of the intended frequency. This frequency division will result in higher current and voltage ripple and is of particular concern in forced continuous applications with low ripple currents at light loads.

Setting the Output Voltage

The LTC3811 output voltages are each set by external feedback resistor dividers, according to the following equation:

$$V_{OUT} = 0.6V \bullet \left[1 + \frac{R2}{R1}\right]$$

Care should be taken to place the output divider resistors and the compensation components as close as possible to the IC FB and SGND pins, in order to prevent switching noise from coupling into the signal path. This configuration is shown in Figure 9. The top of R2 is normally routed to the top of the output capacitor, or to the output of the differential amplifier, if remote sensing is being employed.

Because the common mode range of the current comparator input stages is 0V to 3.5V, the output voltage range is limited from 0.6V to 3.3V.

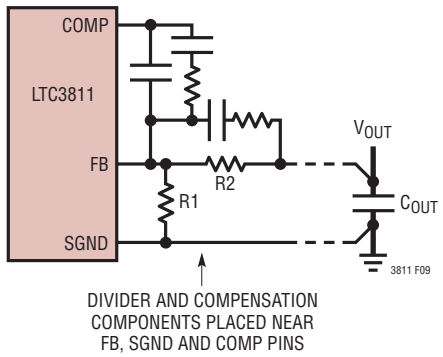

Figure 9. Output Divider and Compensation Component Placement

Sensing the Output Voltage with a Differential Amplifier

The LTC3811 includes a low offset, unity gain, high bandwidth differential amplifier for applications that require true remote sensing. Sensing both SENSE$^+$ and SENSE$^-$ greatly benefits regulation in high current, low voltage applications, where board interconnection losses can be a significant portion of the total error budget.

The LTC3811 differential amplifier has a typical output slew rate of 8V/µs and has rail-to-rail output drive capability. The amplifier is configured for unit gain, meaning that the difference between SENSE$^+$ and SENSE$^-$ is translated to DIFFOUT, relative to SGND.

Care should be taken to route the SENSE$^+$ and SENSE$^-$ PCB traces parallel to each other all the way to the terminals of the output capacitor or remote sensing points on the board. In addition, avoid routing these sensitive traces near any high speed switching nodes in the circuit. Ideally, the SENSE$^+$ and SENSE$^-$ traces should be shielded by a low impedance ground plane to maintain signal integrity.

Choosing the Inductor Value and Saturation Current Rating

The operating frequency and inductor value are interrelated in that higher operating frequencies allow the use of smaller inductors and capacitors. Higher frequency operation also results in higher switching and gate drive losses, so a basic tradeoff exists between size and efficiency.

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For CCM operation, the inductor value can be chosen using the following equation:

$$L = \frac{V_{OUT}}{f \bullet \Delta I_L}\left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

Choosing a larger value of ΔI_L allows the use of a lower value inductor, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting the ripple current is 40% to 50% of the maximum output current, or:

$$\Delta I_L = 0.4 \bullet I_{OUT(MAX)}$$

The inductor saturation current rating needs to be higher than the peak inductor current during an overload condition. If $I_{OUT(MAX)}$ is the maximum rated load current, then the maximum overload current, I_{MAX}, would normally be chosen to be some factor (e.g., 30%) greater than $I_{OUT(MAX)}$:

$$I_{MAX} = 1.3 \bullet I_{OUT(MAX)}$$

$$I_{L(PK)} = I_{MAX} + \frac{1}{2} \bullet \Delta I_L$$

For a 40% ripple application, the minimum saturation current rating of the inductor would therefore be:

$$I_{L(PK)} = 1.5 \bullet I_{O(MAX)}$$

In other words, for an application with 40% inductor ripple current and a maximum output current 30% greater than the full load current, the inductor's saturation current rating needs to be at least 1.5 times the maximum output current.

Inductor Core Selection

Once the value of L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core losses found in low cost powdered iron cores, forcing the use of more expensive ferrite or molypermalloy cores. Actual core loss is independent of core size for a fixed inductor value, but is very dependent on the inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core materials exhibit "hard" saturation, meaning that the inductance collapses abruptly when the peak current capability is exceeded. This results in an abrupt increase in inductor ripple current and output voltage ripple. **Do not allow the core to saturate!**

Programming the Maximum Sense Voltage Using the RNG Pin

The RNG pin can be used in two different ways in order to program the maximum peak current sense voltage. The easiest way to program the peak sense voltage is to tie the RNG pin to either ground or $INTV_{CC}$. Connecting the RNG pin to ground results in a 24mV peak sense voltage and connecting it to $INTV_{CC}$ programs in a 50mV peak sense voltage. Alternately, an external resistor divider from $INTV_{CC}$ to ground can be used to set the RNG pin between 0.6V and 2V, resulting in a nominal peak sense voltage range of 24mV to 85mV. Figure 10 illustrates the transfer function from the RNG pin to the peak sense voltage, which closely follows the following equation for $0.6V < V_{RNG} < 2V$:

$$V_{SENSE(MAX)} = 0.0436 \bullet V_{RNG} - 0.0022$$

In general, the accuracy of the SENSE pin threshold will scale with the peak sense voltage defined by the RNG

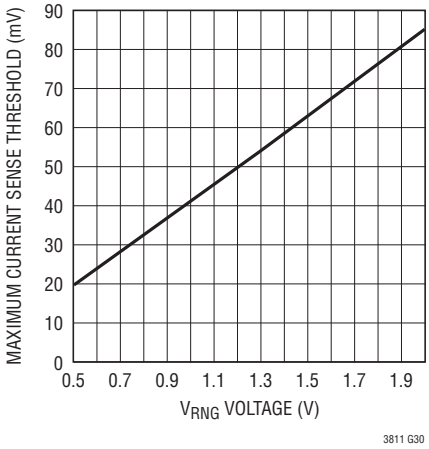

Figure 10. Maximum Current Sense Threshold vs RNG Pin Voltage

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pin. For applications requiring maximum current limit accuracy, a higher peak sense voltage (e.g., 85mV) should be chosen. An additional benefit of a higher peak SENSE pin threshold is a slight reduction in the minimum on-time of the controller. That is, for a given ripple current in the inductor, a higher peak sense voltage results in higher SENSE pin dV/dt, speeding up the input stage of the current comparator slightly. For applications where high efficiency and tight current limit accuracy are both important, the peak current sense voltage can be reduced to as low as 24mV.

In multiphase applications, only one error amplifier is used to control all of the phase current comparators. As a result, in multiphase applications all of the RNG pins should all be tied to the same potential, in order to program the same power stage g_m for each phase.

SENSE+ and SENSE– Pins

The common mode input voltage range of the current comparators is 0V to 3.5V. Continuous linear operation is provided throughout this range, allowing output voltages between 0.6V (the reference input to the error amplifiers) and 3.3V. The SENSE+ and SENSE– pins are also the inputs to the voltage positioning current sense g_m amplifier. Under normal operation, a small current of about 1.5µA flows out of the SENSE inputs and represents the total base current of the two vertical PNP input stages (one in the current comparator and one in the voltage positioning current sense amplifier). When the common mode voltage is lower than about 0.4V, the current flowing out of the SENSE pins increases, up to about 2.2µA at V_{SENSE} = 0V. Figure 11 illustrates the change in the SENSE pin current as a function of common mode voltage.

Sensing Techniques Using Low Value Resistors

For previous generation current mode controllers, the maximum sense voltage was high enough (e.g., 75mV for the LTC1628 family) that the voltage drop across the parasitic inductance of the sense resistor represented a relatively small error. For today's highest current density solutions, however, the value of the sense resistor can be less than 1mΩ and the peak sense voltage can be as low as 24mV. In addition, inductor ripple currents greater than 50% with operation up to 1MHz are becoming more common. Under these conditions the voltage drop across the sense resistor's parasitic inductance is no longer negligible.

A typical sensing circuit using a discrete resistor is shown in Figure 12. In previous generations of controllers, a small RC filter placed near the IC was commonly used to reduce the effects of capacitive and inductive noise coupled in the sense traces on the PCB. A typical filter consists of two series 10Ω resistors connected to a parallel 1000pF capacitor, resulting in a time constant of 20ns.

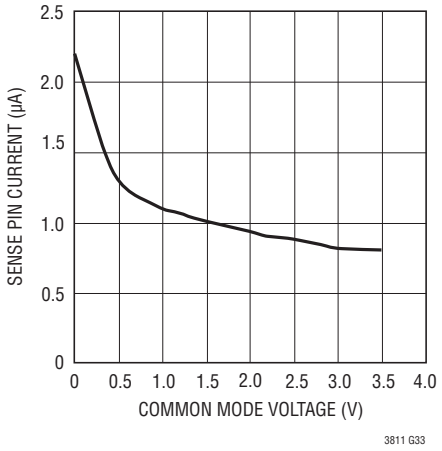

Figure 11. SENSE Pin Input Bias Current vs Common Mode (Output) Voltage

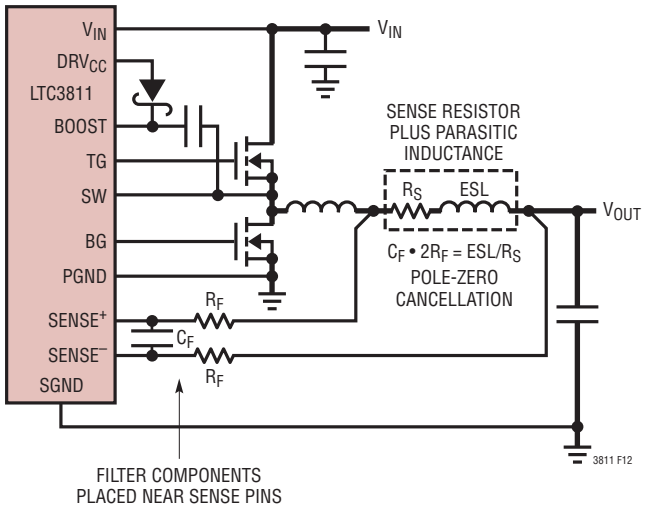

Figure 12. Using a Resistor to Sense Current with the LTC3811

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This same RC filter, with minor modifications, can be used to extract the resistive component of the current sense signal in the presence of parasitic inductance. For example, Figure 13 illustrates the voltage waveform across a 1.5mΩ Panasonic metal strip resistor (ERJ-M1WTJ1M5U). The waveform is the superposition of a purely resistive component and a purely inductive component and was measured with a single low impedance scope probe through a BNC connected directly across the sense resistor terminals. Based on additional measurements of the inductor ripple current and the on- and off-times of the primary switch, the value of the parasitic inductance was determined to be 0.5nH using the equation:

$$V_{ESL(STEP)} = ESL \bullet \left[\frac{\Delta I_L}{t_{ON}} + \frac{\Delta I_L}{t_{OFF}}\right]$$

If the R·C time constant is chosen to be exactly the same as the parasitic inductance divided by the sense resistor (L/R), the resulting waveform looks resistive again, as shown in Figure 14. For applications using low maximum sense voltages, check the sense resistor manufacturer's data sheet for information about parasitic inductance. In the absence of data, measure the voltage drop directly across the sense resistor using a low impedance connection to extract the magnitude of the ESL step and use the equation above to determine the proper filter time constant, keeping the two filter resistor values equal and less than about 200Ω each. Finally, place these filter components close to the IC and run the positive and negative sense traces parallel to each other all the way to the sense resistor.

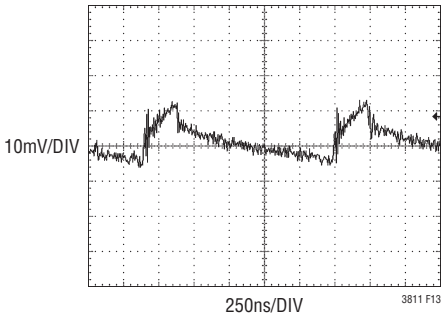

Figure 13. Current Sense Waveform for the Circuit in Figure 33

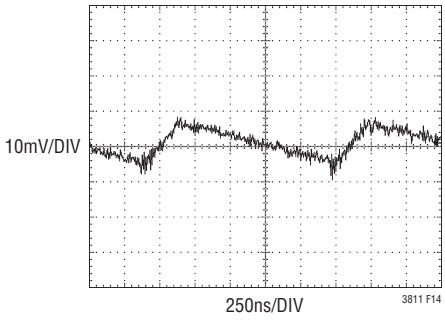

Figure 14. Waveform at the SENSE⁺ and SENSE⁻ Pins Using RC – L/R Time Constant Cancellation

Inductor DCR Sensing

For applications requiring the highest possible efficiency, the LTC3811 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 15. The DCR of the inductor represents the small amount of DC winding resistance of the copper, which can be less than 1mΩ for today's low value, high current inductors. If the external RC time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the voltage drop across the inductor DCR. Check the manufacturer's data sheet for specifications regarding the inductor DCR in order to properly dimension the external filter components. The DCR of the inductor can also be measured using a good RLC meter.

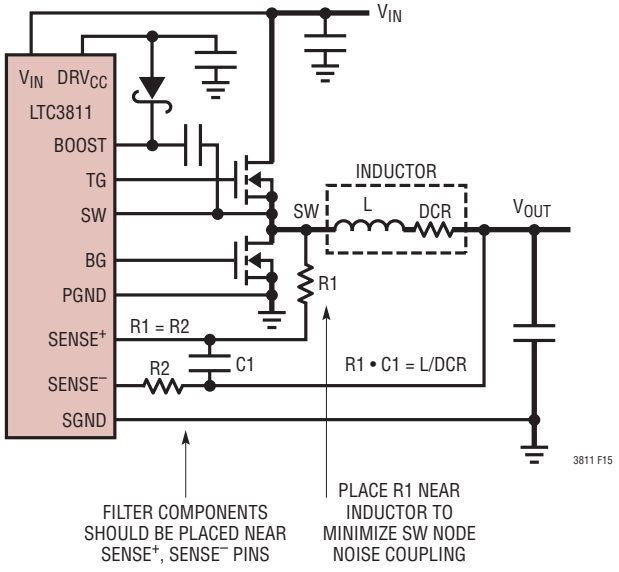

Figure15: Current Mode Control Using the Inductor DCR

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The value of the resistors in the RC filter is a tradeoff between power dissipation and DC accuracy. The power loss on R1 is:

$$P_{R1} = \frac{(V_{IN} - V_O) \bullet V_O}{R1}$$

for a buck converter.

If the value of the filter resistor is too low, its power dissipation will rise, resulting in a larger package size and decreased efficiency at light load. If the value of the filter resistor is too high, the input bias current flowing out of the $SENSE^+$ pin (approximately 1.5µA) could cause the voltage drop across the resistor to be the same order of magnitude of the peak sense voltage, which is also undesirable. A good balance is to use a resistor value of about 1k. An additional 1k resistor (R2) in the $SENSE^-$ path is used to compensate for the drop in the $SENSE^+$ path, and ideally these two resistors (R1 and R2) should match one another.

In general, the larger the sense voltage range is, the smaller the percentage error due to a mismatch in the filter resistor IR drops. The current comparators were designed for low offset and high speed, specifically for applications requiring a small peak sense voltage.

Gate Drive Power Supply Considerations

The LTC3811 user has a choice of how to supply power to the gate drivers and low voltage analog control circuitry. The first of these is to use the internal low dropout linear regulator, LDO, to draw power from V_{IN} and regulate DRV_{CC} to 6V. The second way of supplying power to the gate drivers and analog control circuitry is through the $EXTV_{CC}$ pin. The choice of which supply path to use depends upon system flexibility, power dissipation and the maximum junction temperature in the application.

The internal DRV_{CC} LDO is capable of sourcing up to 100mA, allowing the user to connect multiple power MOSFETs in parallel on both channels for the high power density applications. High input voltage applications in which multiple large MOSFETs are being driven at high frequencies, however, may cause the maximum junction temperature rating for the LTC3811 to be exceeded.

In general, there are three potential sources of power dissipation in the LTC3811:

1. The quiescent current consumed by all of the analog control circuitry connected to $INTV_{CC}$
2. Gate drive losses
3. Losses in the LDO when power is being supplied from V_{IN}

The steady-state quiescent current of the IC is typically 10mA and flows into the $INTV_{CC}$ pin, either through the LDO from V_{IN} or through an auxiliary power supply connected to the $EXTV_{CC}$ pin.

The second source of power dissipation is the gate drivers connected to DRV_{CC}. The lower MOSFET gate drivers are directly connected to DRV_{CC} and the upper ones are connected to DRV_{CC} through the bootstrap diode and floating supply capacitor C_B (refer to Functional Diagram). The gate driver current requirement depends upon the number of MOSFETs being driven, their total gate charge, $Q_{G(TOT)}$, and the operating frequency, f, of the converter. The total current required by the low voltage circuitry is the sum of the DC quiescent current and the gate drive current.

$$I_{VCC} = 10mA + Q_{G(TOT)} \bullet f$$

If the internal LDO in the LTC3811 is used to supply power to DRV_{CC} and $INTV_{CC}$, care should be taken to ensure that the total low voltage current doesn't exceed the 100mA limit for the LDO.

Assuming that $DRV_{CC} = EXTV_{CC} = INTV_{CC} = 6V$, power dissipation due to the quiescent current and gate drive losses is:

$$PV_{CC} = 6V \bullet (10mA + Q_{G(TOT)} \bullet f)$$

The third source of power dissipation occurs in the LDO, which supplies power to the DRV_{CC} pin when $EXTV_{CC}$ is less than 4.7V. When power is being drawn from V_{IN} the power dissipated in the LDO is:

$$P_{LDO} = (V_{IN} - V_{DRVCC}) \bullet (10mA + Q_{G(TOT)} \bullet f)$$

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The total power dissipation is the sum of these two and the junction temperature can then be estimated using the following equation:

$$T_J = T_A + (P_{VCC} + P_{LDO}) \bullet R_{\theta JA}$$

As an example, consider a 2-phase, single-output application with a 12V input voltage and a 1.2V output at up to 30A (15A/phase), using the QFN version of the LTC3811. The upper power MOSFETs are the Renesas RJK0305DPB (one per phase) and the lower power MOSFETs are the RJK0301DPB (one per phase). The upper MOSFETs have a typical $R_{DS(ON)} = 10m\Omega$ at $V_{GS} = 4.5V$ and a typical $Q_G = 8nC$. The lower MOSFETs have a typical $R_{DS(ON)} = 3m\Omega$ at $V_{GS} = 4.5V$ and a typical $Q_G = 32nC$. The total gate charge is therefore 80nC and the operating frequency is 500kHz. With a maximum ambient temperature of 70°C and a thermal resistance of 34°C/W for the QFN package,

$$I_{DRVCC} = 10mA + 500kHz \bullet 80nC = 50mA$$

$$P_{DRVCC} = 6V \bullet (10mA + 500kHz \bullet 80nC) = 300mW$$

$$P_{LDO} = (12V - 6V) \bullet (10mA + 500kHz \bullet 80nC) = 300mW$$

$$T_J = 70°C + (0.3 + 0.3) \bullet 34°C/W = 90°C$$

A 20°C rise in the junction temperature and a maximum LDO current of 50mA are acceptable numbers but could be improved upon by using the $EXTV_{CC}$ pin to supply power to the gate drivers. The use of an auxiliary supply connected to the $EXTV_{CC}$ pin would reduce the junction temperature rise by a factor of 2, resulting in a max junction temperature of:

$$T_J = 70°C + 0.3 \bullet 34°C/W = 80°C$$

For applications where the internal LDO is being used to supply power to the IC, to prevent the maximum junction temperature from being exceeded the input supply current should be monitored at maximum V_{IN} in continuous conduction mode (i.e., with MODE/SYNC connected to $INTV_{CC}$).

Using the $EXTV_{CC}$ Pin to Supply Power to the LTC3811

The LTC3811 contains an internal P-channel MOSFET switch connected between the $EXTV_{CC}$ and DRV_{CC} pins. When the voltage applied to $EXTV_{CC}$ exceeds 4.5V, the internal LDO is turned off and the PMOS switch turns on, connecting the $EXTV_{CC}$ pin to the DRV_{CC} pin and thereby supplying the internal analog and digital circuitry and MOSFET gate drive power. Do not apply greater than 7V to the $EXTV_{CC}$ pin (its absolute maximum rating) and ensure that $EXTV_{CC} < V_{IN} + 0.3V$ when using the application circuits shown. If an external voltage source is applied to the $EXTV_{CC}$ pin when the V_{IN} supply is not present, a diode can be placed in series with the LTC3811's V_{IN} pin and a Schottky diode between the $EXTV_{CC}$ pin and the V_{IN} pin, to prevent current from backfeeding into V_{IN} through the PMOS body diodes.

Significant energy gains can be realized by powering DRV_{CC} and $INTV_{CC}$ from an auxiliary supply, since the V_{IN} current resulting from the driver and analog control circuitry currents will be scaled by the ratio:

Duty Cycle/Efficiency

The following list summarizes the three possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ left open (or grounded). This will cause DRV_{CC} and $INTV_{CC}$ to be powered from the internal 6V LDO, resulting in a significant efficiency penalty and excess power dissipation at high input voltages.
2. $EXTV_{CC}$ connected to an external supply. If an external supply is available in the 5V to 7V range it may be used to power $EXTV_{CC}$, provided it is capable of satisfying the gate drive and control IC current requirements. V_{IN} must be greater than or equal to the voltage applied to the $EXTV_{CC}$ pin.
3. $EXTV_{CC}$ connected to an output-derived boost network. For 3.3V and other low voltage regulators, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output-derived voltage which has been boosted to greater than 4.5V but less than 7V. This can be done with a capacitive charge pump shown in Figure 16.

Power MOSFET and Schottky Diode (Optional) Selection

Two external power MOSFETs must be selected for each controller in the LTC3811: one N-channel MOSFET for the top (main) switch, and one N-channel MOSFET for the bottom (synchronous) switch.

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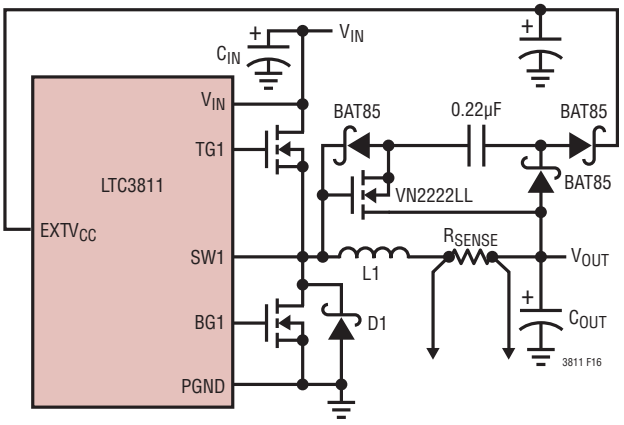

Figure 16. Capacitive Charge Pump for $EXTV_{CC}$

The peak-to-peak drive levels are set by the $INTV_{CC}$ voltage. This voltage is typically 6V during start-up (see $EXTV_{CC}$ Pin Connection). Consequently, logic-level threshold MOSFETs should be used in most applications. The only exception is if low input voltage is expected (V_{IN} < 5V); then, sub-logic level threshold MOSFETs ($V_{GS(TH)}$ < 3V) should be used. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; most of the logic-level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the "ON" resistance $R_{DS(ON)}$, Miller capacitance C_{MILLER}, input voltage and maximum output current. Miller capacitance, C_{MILLER}, can be approximated from the gate charge curve usually provided on the MOSFET manufacturers' data sheet. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat divided by the specified change in V_{DS}. This result is then multiplied by the ratio of the application applied V_{DS} to the Gate charge curve specified V_{DS}. When the IC is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}(I_{MAX})^2 R_{DS(ON)}(1+\delta) + (V_{IN})^2 \left[\frac{I_{MAX}}{2}\right](R_{DR})(C_{MILLER}) \bullet \left[\frac{1}{V_{INTVCC} - V_{THMIN}} + \frac{1}{V_{THMIN}}\right](f)$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}(I_{MAX})^2 (1+\delta) R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$ and R_{DR} (approximately 2Ω) is the effective top gate driver resistance at the MOSFET's Miller threshold voltage. V_{THMIN} is the typical MOSFET minimum threshold voltage.

Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which are highest at high input voltages. For V_{IN} < 20V the high current efficiency generally improves with larger MOSFETs, while for V_{IN} > 20V the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period.

The term (1+δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but δ = 0.005/°C can be used as an approximation for low voltage MOSFETs.

The optional Schottky diode, D1, shown in Figure 16 conducts during the dead-time between the conduction of the two power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on, storing charge during the dead-time and requiring a reverse recovery period that could cost as much as 1% in efficiency at high V_{IN}. A 1A to 3A Schottky is generally a good compromise for both regions of operation due to the relatively small average current. Larger diodes result in additional transition losses due to their larger junction capacitance.

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C_{IN} and C_{OUT} Selection

In continuous mode, the drain current of each top N-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. A low ESR input capacitor sized for the maximum RMS current must be used. The details of a close form equation can be found in Application Note 77. Figure 17 shows the input capacitor ripple current for different phase configurations with the output voltage fixed and input voltage varied. The input ripple current is normalized against the DC output current. The graph can be used in place of tedious calculations. The minimum input ripple current can be achieved when the product of phase number and output voltage, $N(V_{OUT})$, is approximately equal to the input voltage V_{IN} or:

$$\frac{V_{OUT}}{V_{IN}} = \frac{k}{N} \text{ where } k = 1, 2, ..., N - 1$$

So the phase number can be chosen to minimize the input capacitor size for the given input and output voltages.

In the graph of Figure 17, the local maximum input RMS capacitor currents are reached when:

$$\frac{V_{OUT}}{V_{IN}} = \frac{2k - 1}{2N} \text{ where } k = 1, 2, ..., N$$

These worst-case conditions are commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the capacitor manufacturer if there is any question.

The graph shows that the peak RMS input current is reduced linearly, inversely proportional to the number, N of stages used. It is important to note that the efficiency loss is proportional to the input RMS current *squared* and therefore a 2-stage implementation results in 75% less power loss when compared to a single phase design. Battery/input protection fuse resistance (if used), PC board trace and connector resistance losses are also reduced by the reduction of the input ripple current in a PolyPhase

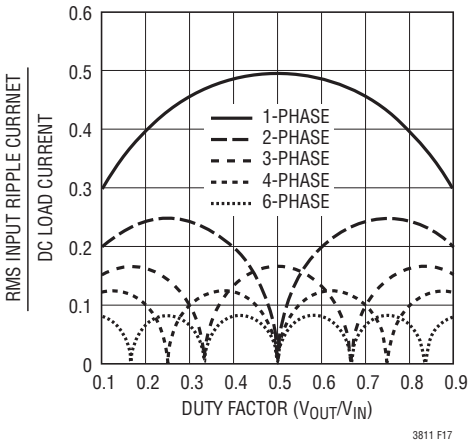

Figure 17. Normilized Input RMS Ripple Current vs Duty Factor for 1 to 6 Output Stages

system. The required amount of input capacitance is further reduced by the factor, N, due to the effective increase in the frequency of the current pulses.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically once the ESR requirement has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirements. The steady-state output ripple (ΔV_{OUT}) is determined by:

$$\Delta V_{OUT} \approx \Delta I_{RIPPLE} \left[ESR + \frac{1}{8NfC_{OUT}} \right]$$

where f = operating frequency of each stage, N is the number of phases, C_{OUT} = output capacitance and ΔI_{RIPPLE} = combined inductor ripple currents.

The output ripple varies with input voltage since ΔI_L is a function of input voltage. The output ripple will be less than 50mV at max V_{IN} with $\Delta I_L = 0.4 I_{OUT(MAX)}/N$ assuming:

C_{OUT} required ESR < $2N(R_{SENSE})$ and

$C_{OUT} > 1/(8Nf)(R_{SENSE})$

The emergence of very low ESR ceramic capacitors in small, surface mount packages makes very physically small implementations possible. The ability to externally compensate the switching regulator loop using the LTC3811's true operational error amplifier allows a much wider selection of output capacitor types. The ability to

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use type III compensation effectively removes constraints on output capacitor ESR. The impedance characteristics of each capacitor type are significantly different than an ideal capacitor and therefore require accurate modeling and bench evaluation during design.

Manufacturers such as Nichicon, United Chemicon and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo and the Panasonic SP surface mount types have the lowest (ESR)(size) product of any aluminum electrolytic at a somewhat higher price. An additional ceramic capacitor in parallel with OS-CON type capacitors is recommended to reduce inductance effects.

In surface mount applications, multiple capacitors may have to be paralleled to meet the ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. New special polymer surface mount capacitors offer very low ESR also but have much lower capacitive density per unit volume. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. Several excellent choices are the AVX TPS, AVX TPSV or the KEMET T510 series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. Other capacitor types include Sanyo OS-CON, Nichicon PL series and Sprague 595D series. Consult the manufacturer for other specific recommendations. A combination of capacitors will often result in maximizing performance and minimizing overall cost and size.

Tracking and Soft-Start (SS/TRACK Pins)

The start-up of each V_{OUT} is controlled by the voltage on the respective SS/TRACK pin. When the voltage on the SS/TRACK pin is less than the internal 0.6V reference, the LTC3811 regulates the V_{FB} pin voltage to the voltage on the SS/TRACK pin instead of 0.6V. The SS/TRACK pin can be used to program an external soft-start function or to allow V_{OUT} to "track" another supply during start-up.

Soft-start is enabled by simply connecting a capacitor from the SS/TRACK pin to ground, as shown in Figure 18. An internal 2.5µA current source charges up the capacitor, providing a linear ramping voltage at the SS/TRACK pin. The LTC3811 will regulate the V_{FB} pin (and hence V_{OUT}) according to the voltage on the SS/TRACK pin, allowing V_{OUT} to rise smoothly from 0V to its final regulated value. The total soft-start time will be approximately:

$$t_{SS} = C_{SS} \bullet \frac{0.6V}{2.5\mu A}$$

Alternatively, the SS/TRACK pin can be used to track two (or more) supplies during start-up, as shown qualitatively in Figures 19a and 19b. To do this, a resistor divider should be connected from the master supply (V_X) to the SS/TRACK pin of the slave supply (V_{OUT}), as shown in Figure 20. During start-up V_{OUT} will track V_X according to the ratio set by the resistor divider:

$$\frac{V_{OUT}}{V_X} = \frac{R_{TRACKA}}{R_A} \bullet \frac{R_A + R_B}{R_{TRACKA} + R_{TRACKB}}$$

For coincident tracking ($V_{OUT} = V_X$ during start-up),

$R_A = R_{TRACKA}$

$R_B = R_{TRACKB}$

Note that the small SS/TRACK charging current is always flowing, producing a small offset error. To minimize this error, select the tracking resistor divider values to be small enough to make this error negligible.

Topside MOSFET Driver Supply (C_B, D_B)

External bootstrap capacitors C_B connected to the BOOST and SW pins supply the gate drive voltages for the topside MOSFETs. Capacitor C_B in the Functional Diagram is charged though external diode D_B from DRV_{CC} when the SW pin is low. When one of the topside MOSFETs is to be turned on, the driver places the C_B voltage across the gate-source of the desired MOSFET. This enhances the MOSFET and turns on the topside switch. The switch

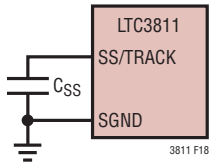

Figure 18. Using the SS/TRACK pin to Program Soft-Start

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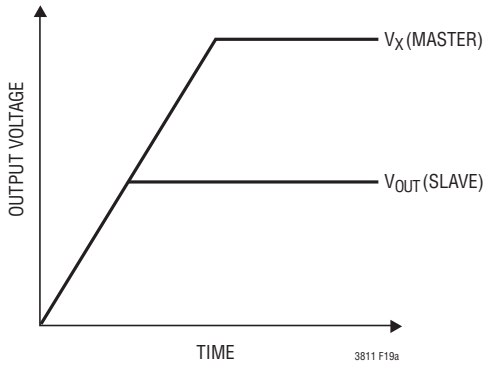
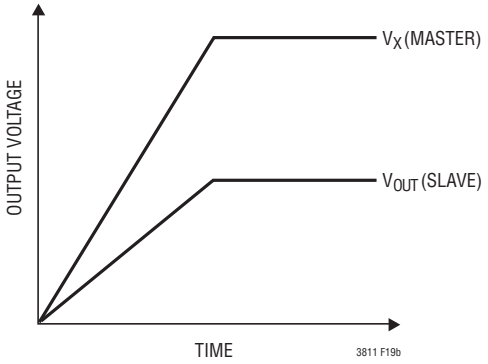
node voltage, SW, rises to V_{IN} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the input supply: $V_{BOOST} = V_{IN} + V_{DRVCC}$. The value of the boost capacitor C_B needs to be 100 times that of the total input capacitance of the topside MOSFET(s). The reverse breakdown of the external Schottky diode must be greater than $V_{IN(MAX)}$. When adjusting the gate drive level, the final arbiter is the total input current for the regulator. If a change is made and the input current decreases, then the efficiency has improved. If there is no change in input current, then there is no change in efficiency.



(19a) Coincident Tracking



(19b) Ratiometric Tracking

Figure 19. Two different Modes of Output Votlage Tracking

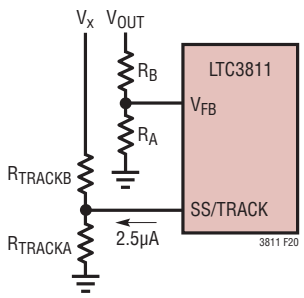


Figure 20. Using the SS/TRACK Pin for Tracking

Overvoltage Protection

The LTC3811 contains a comparator that monitors the FB pin voltage for potential overvoltage conditions. This comparator (OV in the Functional Diagram) detects when the FB pin voltage exceeds 0.66V, or is 10% above nominal regulation. When this condition is sensed, the top MOSFET is turned off and the bottom MOSFET is turned on. For an overvoltage condition that persists, the inductor current will reverse until the negative current limit of the converter is reached. If the OV condition terminates V_{OUT} will return to regulation and normal operation automatically resumes.

The OV signal that controls the top and bottom MOSFET switching does not propagate through the PGOOD filter before action is taken. The OV comparator is capable of sensing a fault condition within 100ns to 200ns, after which the top MOSFET is turned off. The PGOOD filter will delay the signal to the open-drain NMOS transistor connected to the PGOOD pin, however, preventing OV (and UV) transients of less than about 130µs from forcing a system reset.

Phase-Locked Loop and Frequency Synchronization

The LTC3811 has a phase-locked loop (PLL) comprised of an internal voltage-controlled oscillator (VCO) and a phase detector. This allows the turn-on of the top MOSFET of controller 1 to be locked to the rising edge of an external clock signal applied to the MODE/SYNC pin. The turn-on phase of controller 2's top MOSFET is controlled by the voltage on the PHASEMODE pin. The phase detector is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

The output of the phase detector is a pair of complementary current sources that charge or discharge the external filter network connected to the PLL/LPF pin. The relationship between the voltage on the PLL/LPF pin and operating frequency, when there is a clock signal applied

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to MODE/SYNC, is shown in Figure 21 and specified in the Electrical Characteristics table. Note that the LTC3811 can only be synchronized to an external clock whose frequency is within range of the LTC3811's internal VCO, which is nominally 125kHz to 1.1MHz. This is guaranteed to be between 175kHz and 900kHz. A simplified block diagram is shown in Figure 22.

If the external clock frequency is greater than the internal oscillator's frequency, f_{OSC}, then current is sourced continuously from the phase detector output, pulling up the PLL/LPF pin. When the external clock frequency is less than f_{OSC}, current is sunk continuously, pulling down the PLL/LPF pin. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage on the PLL/LPF pin is adjusted until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the phase detector output is high impedance and the filter capacitor C_{LP} holds the voltage.

The loop filter components, C_{LP} and R_{LP}, smooth out the current pulses from the phase detector and provide a stable input to the voltage-controlled oscillator. The filter components C_{LP} and R_{LP} determine how fast the loop acquires lock. Typically R_{LP} = 10k and C_{LP} is 2200pF to 0.01µF.

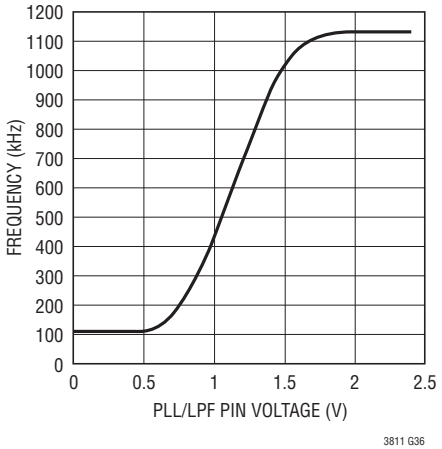

Figure 21. Relationship Between Oscillator Frequency and Voltage at the PLL/LPF Pin When Synchronizing to an External Clock

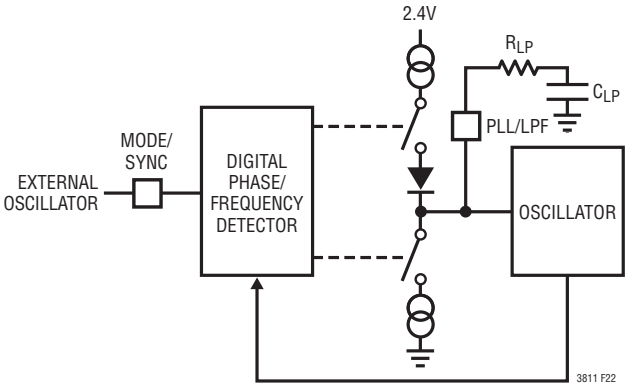

Figure 22. Phase-Locked Loop Block Diagram

Typically, the external clock (on MODE/SYNC pin) input high threshold is 1.1V, while the input low threshold is 1.0V.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

%Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3811 circuits: 1) IC V_{IN} current, 2) DRV_{CC} regulator current, 3) I^2R losses, 4) Topside MOSFET transition losses.

1. The V_{IN} current has two components: the first is the DC supply current given in the Electrical Characteristics table, and the second is the MOSFET driver and control currents.
2. DRV_{CC} current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ

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moves from DRV_{CC} to ground. The resulting dQ/dt is a current out of DRV_{CC} that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the topside and bottom side MOSFETs.

Supplying DRV_{CC} and $INTV_{CC}$ power through the $EXTV_{CC}$ switch input from an output-derived source will scale the V_{IN} current required for the driver and control circuits by a factor of (Duty Cycle)/(Efficiency). For example, in a 20V input to 2.5V output application, 40mA of DRV_{CC} current results in approximately 5mA of V_{IN} current. This reduces the mid-current efficiency loss from 10% or more (if the driver was powered directly from V_{IN}) to only a few percent.

3. I^2R losses are predicted from the DC resistances of the fuse (if used), MOSFET, inductor, current sense resistor, and input and output capacitor ESR. In continuous mode the average output current flows through L and R_{SENSE}, but is "chopped" between the topside MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L, R_{SENSE} and ESR to obtain I^2R losses. For example, if each $R_{DS(ON)} = 5m\Omega$, $R_L = 1m\Omega$, $R_{SENSE} = 1.5m\Omega$ and $R_{ESR} = 4m\Omega$ (sum of both input and output capacitance losses), then the total resistance is $16m\Omega$. This results in losses ranging from 5.6% to 8.4% as the output current increases from 10A to 15A for a 2.5V output. Efficiency varies as the inverse square of V_{OUT} for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems is not doubling but quadrupling the importance of loss terms in the switching regulator system!

4. Transition losses apply only to the topside MOSFET(s), and become significant only when operating at high input voltages (typically 15V or greater). Transition losses can be estimated from:

$$\text{Translation Loss} = (V_{IN})^2 \frac{I_{MAX}}{2} \bullet R_{DR} \bullet C_{MILLER}$$

Other "hidden" losses such as copper trace and internal battery resistances can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these "system" level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. A 25W supply will typically require a minimum of 20µF to 40µF of capacitance having a maximum of $20m\Omega$ to $50m\Omega$ of ESR. The LTC3811 2-phase architecture typically halves this input capacitance requirement over competing solutions. Other losses including Schottky conduction losses during dead-time and inductor core losses generally account for less than 1% total additional loss.

Feedback Loop Compensation

The LTC3811 incorporates a peak current mode control topology. Peak current mode control provides excellent line and load transient response, and inherently provides the best possible phase-to-phase current sharing in multiphase applications.

The LTC3811 incorporates a true operational error amplifier in the feedback loop, enabling the user the flexibility to place poles and zeros at well defined frequencies in the transfer function, thereby optimizing the loop's AC response.

The control-to-output transfer function has a pole at the origin in order to provide DC regulation, and a pole due to the load resistance and capacitance at:

$$f_{P(LOAD)} = \frac{1}{2\pi \bullet R_L \bullet C_L}$$

The output decoupling capacitor ESR contributes a zero to the transfer function at:

$$f_{Z(ESR)} = \frac{1}{2\pi \bullet ESR \bullet C_L}$$

The transfer function also has a mathematical double pole at half the switching frequency due to the sampling nature of current mode control, although the pole-splitting behavior of the LTC3811's internal slope compensation reduces the phase shift for frequencies below $f_{SW}/2$.

For most systems, the simple 2-pole, single-zero response of a Type-II compensation network (shown in Figure 23)

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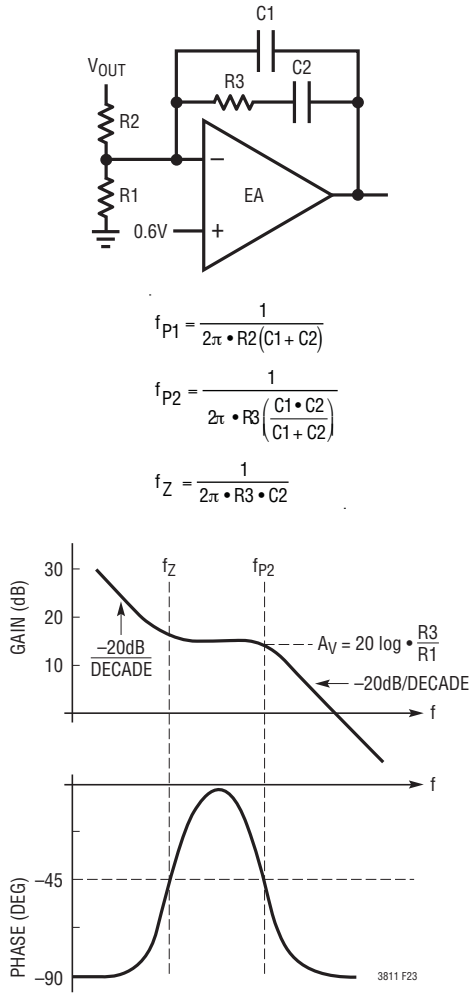
will provide adequate phase margin at the unity-gain frequency of the loop.

In a Type-II compensation scheme, the zero is typically placed below the target unity-gain frequency, depending upon the desired settling time of the converter, and the pole is placed no higher than half the switching frequency in order to attenuate the switching frequency from the loop. The gain between the zero and pole is typically adjusted until the desired phase margin is achieved.

In general, the output capacitor is chosen based on cost and size considerations, given a certain error budget due to output ripple voltage and load transient response. Oftentimes, multiple capacitor types (such as ceramic and special polymer) are connected in parallel in order to achieve a good combination of bulk capacitance and low ESR. In general, the output capacitor is not normally chosen to optimize the bode response.

Due to their small case size and low ESR, ceramic output capacitors are well suited to very low voltage, high current applications. Their low ESR and relatively high RMS current capability make them a good choice for today's demanding processor-based loads. A fully ceramic output stage, however, will result in very low ESR, pushing the ESR zero frequency relatively close to the unity-gain frequency of the loop. In this case a Type-III compensation network using 3 poles and 2 zeros may be necessary (see Figure 24). For particularly demanding applications requirements, please consult Linear Technology's Applications department.

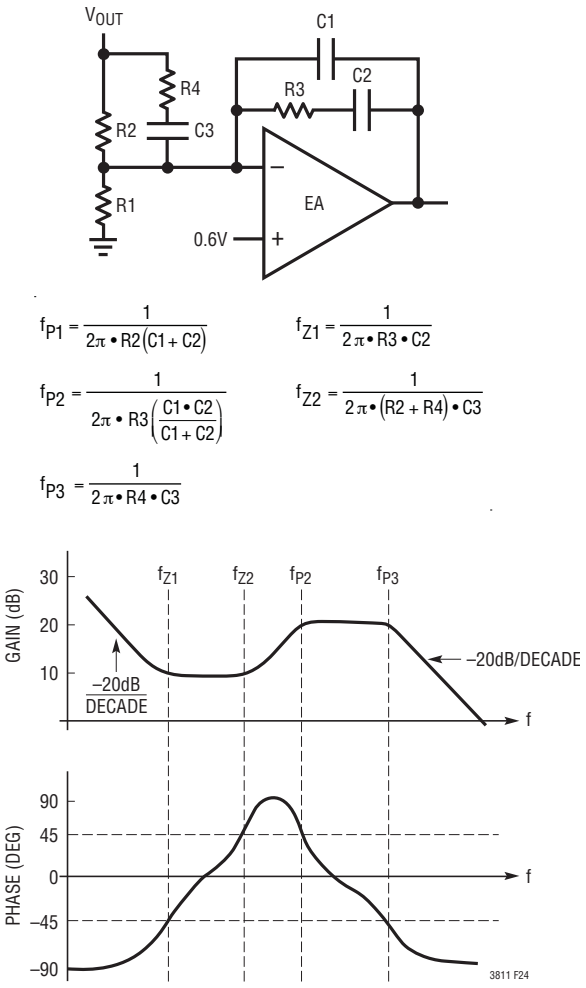


$$f_{P1} = \frac{1}{2\pi \bullet R2(C1+C2)}$$

$$f_{P2} = \frac{1}{2\pi \bullet R3\left(\frac{C1 \bullet C2}{C1+C2}\right)}$$

$$f_{Z} = \frac{1}{2\pi \bullet R3 \bullet C2}$$

Figure 23. Type-II Compensation Network and Frequency Response



$$f_{P1} = \frac{1}{2\pi \bullet R2(C1+C2)}$$

$$f_{Z1} = \frac{1}{2\pi \bullet R3 \bullet C2}$$

$$f_{P2} = \frac{1}{2\pi \bullet R3\left(\frac{C1 \bullet C2}{C1+C2}\right)}$$

$$f_{Z2} = \frac{1}{2\pi \bullet (R2+R4) \bullet C3}$$

$$f_{P3} = \frac{1}{2\pi \bullet R4 \bullet C3}$$

Figure 24. Type-III Compensation Network and Frequency Response

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Measuring the Loop's Transient Response

Once the compensation components have been chosen, the AC performance of the power supply should be verified in the lab. The two most common ways of checking the AC response of the circuit are with load and line steps, and by measuring the loop gain using a network analyzer or Venable measurement system. Both of these measurement techniques should be performed on the final design to ensure adequate correlation between the two, and to identify and correct potential regions of marginal stability. These measurements should be performed over all of the load, line, temperature and components tolerance variations the system will experience in a practical application.

Figure 25 illustrates a typical load step response for the LTC3811. When a positive load step occurs, the output voltage immediately drops by ΔI_{LOAD} • ESR, where ESR is the equivalent series resistance of the output capacitor. The increased load current then begins to discharge the output capacitor, generating a feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state regulated value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing which would indicate a stability problem. Assuming a second order system, the phase margin and/or damping factor can be estimated using the percentage overshoot seen at the output.

An output current pulse of 20% to 100% of full load having a rise time of 0.1µs to 1µs will produce an output voltage waveform that will give an indication of the loop stability without having to break the feedback loop. Placing a power MOSFET directly across the output capacitor and driving the gate with an appropriate signal generator or gate driver is a practical way to produce a realistic load step condition.

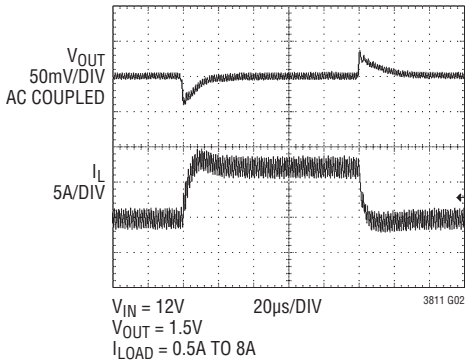

Figure 25. Load Step Response for the LTC3811 Circuit in Figure 33

Voltage Positioning for Single Output, Multiphase Applications

The output voltage load line can be programmed with the LTC3811 using one external resistor, allowing the user to reduce the total output capacitance required for a given error budget. The inductor current information is sensed using the SENSE+ and SENSE– inputs for both channels and fed into a transconductance amplifier with two input stages, as shown in Figure 26. The output current of the transconductance amplifier, along with one external resistor (R_{AVP}), allows the user to inject a load-current-related error signal into the voltage feedback loop. *Please note that because the g_m amplifier mixes the signals from both channels, voltage positioning is only possible for multiphase, single output applications; dual output applications with voltage positioning are not possible.*

The internal mixing of the current sense signals within the voltage positioning amplifier, combined with the fact that the g_m amplifier output signal is a current, allows the user to connect the CSOUT pins of several LTC3811 chips together in multiphase applications. The transconductance (g_m) of the voltage positioning amplifier is 2.5mS/phase, and the load slope is:

$$V_{OUT} = 0.6 \bullet \left[1 + \frac{R2}{R1}\right] - \left[I_{OUT} \bullet \frac{R_{SENSE}}{n} \bullet 5m \bullet R_{AVP}\right]$$

where n is the number of phases.

The input common mode range of the voltage position g_m amplifier is 0.6V to 3.5V, comfortably allowing output voltages up to 3.3V. In addition, the output voltage range of the g_m amplifier for linear operation is limited to voltages above 0.6V, due to the headroom requirements of the NMOS sink transistors in the output stage. And finally, the maximum differential input voltage for linear operation is ±100mV.

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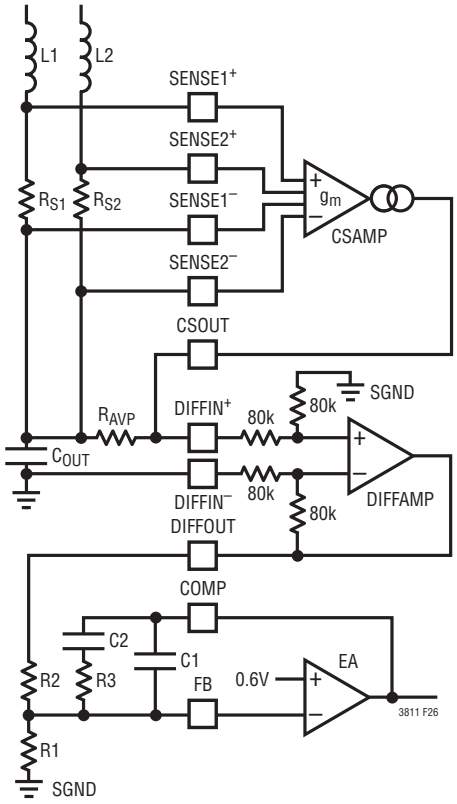

Figure 26. Simplified LTC3811 Voltage Positionig Block Diagram

Figure 27 illustrates the load step response for the circuit in Figure 30, with voltage positioning.

A Design Example

As a design example consider one channel of a 2-phase single output supply. Assume V_{IN} = 4.5V to 14V, V_{OUT} = 1.5V, I_{MAX} = 30A(15A per phase) and f = 500kHz.

In order to achieve the best output accuracy, 1% resistors (or better) should be used in the divider that programs the output voltage. Choosing 600µA for the divider current, R2 = 1.5k and R1 = 1k. The nominal output voltage will therefore be 1.50V.

For the input and output conditions given above, the steady state minimum on-time for this application at V_{IN} = 14V will be approximately:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)} \bullet f} = \frac{1.5V}{14V \bullet 500kHz} = 214ns$$

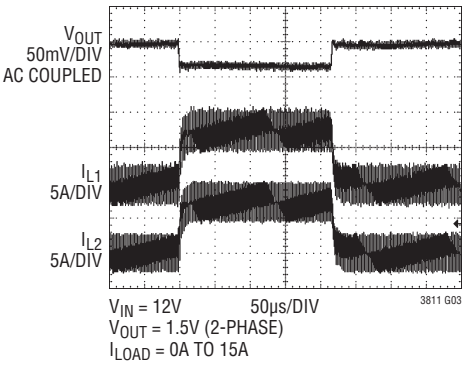

Figure 27. Load Step Response for the Circuit in Figure 30

To program 500kHz operation, float the PLL/LPF pin. The inductor value in this design is chosen assuming 50% ripple current. The highest ripple current occurs at maximum input voltage.

$$L = \frac{V_{OUT}}{f \bullet \Delta I_L} \bullet \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

$$= \frac{1.5V}{500kHz \bullet 0.5 \bullet 15A} \bullet \left[1 - \frac{1.5V}{14V}\right] = 0.36\mu H$$

A 0.4µH inductor will result in 6.7A of ripple current, or 45%. Assuming a value for the current limit value 30% greater than the maximum load current, then I_{MAX} = 1.3 • 15A = 19.5A. The peak inductor current will be the maximum DC value plus one half the ripple current, or:

$$I_{L(PK)} = 19.5A + \frac{1}{2} \bullet 6.7A = 22.9A$$

This represents the minimum saturation current rating for the inductor. For this application, a Vitec 59P9875 inductor was chosen. This inductor has a room temp saturation current rating of 23A and a DCR of 0.32mΩ.

To maintain good cycle-by-cycle control of the inductor current and still have good efficiency, a 1.5mΩ, 1W sense resistor from Panasonic (ERJ-M1WTJ1M5U) connected in series with the inductor is used for current sensing. With a maximum peak inductor current of 22.9A, the peak sense voltage will be:

$$V_{SENSE(PK)} = 22.9A \bullet 0.0015\Omega = 34.4mV$$

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The maximum power dissipation in the sense resistor will be:

$$P_{R(SENSE)} = 22.9A^2 \bullet 0.0015\Omega = 0.79W$$

To ensure that the maximum current can be delivered over all of the power component and IC tolerances, the maximum sense voltage for the LTC3811 is chosen to be 50mV. This is programmed by connecting the RNG pin to $INTV_{CC}$.

Due to the use of a 400nH inductor and 500kHz operation, the magnitude of the inductive voltage drop across the sense resistor should be calculated and compared to the maximum sense voltage (50mV). First calculate the nominal switch on-time:

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \bullet f} = \frac{1.5V}{12V \bullet 500kHz} = 250ns$$

The inductor $\Delta I_L/dt$ is therefore:

$$\frac{\Delta I_L}{dt} = \frac{6.7A}{250ns} = \frac{26.8A}{\mu s}$$

The Panasonic sense resistor has a typical parasitic series inductance (ESL) of 0.5nH, meaning that the inductive voltage drop across the resistor is:

$$V_{L(SENSE)} = ESL \bullet \frac{\Delta I_L}{dt} = 0.5nH \bullet \frac{26.8A}{\mu s} = 13.4mV$$

The ESL/R time constant for the sense resistor is therefore:

$$\tau = \frac{ESL}{R_{SENSE}} = 333ns$$

The sense pins need an RC filter with the same time constant in order for the waveform at the $SENSE^+$ and $SENSE^-$ pin to accurately represent the inductor current. Choosing a value of 1000pF for the filter capacitor, the total resistance should therefore be 333Ω. Split between the $SENSE^+$ and $SENSE^-$ pins, each resistor should be 165Ω. These components should be placed adjacent to the $SENSE^+$ and $SENSE^-$ pins on the LTC3811, and the PCB traces from the 165Ω filter resistors should be minimum width and run parallel to each other all the way to the sense resistor location on the board.

The power MOSFETs chosen for this application are the Renesas RJK0305DPB (top) and RJK0301DPB (bottom). The upper MOSFET, which is optimized for low switching losses, has a typical $R_{DS(ON)}$ of 10mΩ at V_{GS} = 4.5V, a total gate charge of 8nC, and a minimum BV_{DSS} of 30V. The bottom MOSFET, which is zero-voltage switched and is optimized for low on-resistance, has a typical $R_{DS(ON)}$ of 3mΩ at V_{GS} = 4.5V, a total gate charge of 32nC, and a minimum BV_{DSS} of 20V.

From the datasheet of the RJK0305DPB upper MOSFET, the Miller capacitance is calculated to be:

$$C_{MILLER} = \frac{\Delta Q_G}{\Delta V_{DS}} = \frac{2nC}{12V} = 167pF$$

Assuming a top MOSFET junction temperature of 75°C, δ = 0.25 and the power dissipated in this MOSFET is:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}} \bullet {I_{MAX}}^2 \bullet R_{DS(ON)} \bullet (1+\delta) + {V_{IN}}^2 \bullet \frac{I_{MAX}}{2} T \bullet R_{DR} \bullet C_{MILLER} \bullet \left[\frac{1}{V_{INTVCC} - V_{TH(MIN)}} + \frac{1}{V_{TH(MIN)}}\right] \bullet f$$

$$P_{MAIN} = \frac{1.5V}{12V} \bullet 15A^2 \bullet 0.01 \bullet (1+0.25) + 12V^2 \bullet \frac{15A}{2} \bullet 2\Omega \bullet 167pF \bullet \left[\frac{1}{6V-1V} + \frac{1}{1V}\right] \bullet 500kHz$$

$$P_{MAIN} = 0.351W + 0.216W = 0.567W$$

For the synchronous MOSFET the power dissipation is:

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}} \bullet {I_{MAX}}^2 \bullet R_{DS(ON)} \bullet (1+\delta)$$

$$P_{MAIN} = \frac{12V - 1.5V}{12V} \bullet 15A^2 \bullet 0.003 \bullet (1+0.25) = 0.738W$$

To determine the RMS current rating of the input capacitor, we need to first determine the minimum and maximum duty cycle. For an output voltage of 1.5V and an input range of 4.5V to 14V, the duty cycle range is 12.5% to 33.3%. We then use Figure 17 to determine the percentage of

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the maximum load current that represents the minimum RMS current rating of the input capacitor. The worst-case condition occurs when only one output is operational. The output with the highest (V_{OUT})(I_{OUT}) product should be used to determine the minimum RMS current rating of the input capacitor. From Figure 17 we can see that the worst case condition for this output occurs at the maximum duty cycle of 33.3%, and that the minimum RMS current rating of the input capacitor needs to exceed 7A (47% of 15A).

The ceramic output capacitors chosen have an effective ESR of 5mΩ and a bulk capacitance of 660µF. The peak-to-peak output ripple for this configuration is:

$$\Delta V_{OUT} = \Delta I_L \bullet \left[ESR + \frac{1}{8 \bullet n \bullet f \bullet C_{OUT}} \right]$$

$$= 6.7A \bullet \left[0.005\Omega + \frac{1}{8 \bullet 2 \bullet 500kHz \bullet 660\mu F} \right]$$

$$\Delta V_{OUT} = 33.5mV + 1.3mV = 34.8mV$$

This represents a ripple voltage of 2.3%. As can be seen from the calculation, the biggest portion of the output ripple comes from the ESR of the capacitor. This is why low ESR ceramic capacitors are so important in low voltage, high current applications.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the converter:

1. The connection between the SGND pin on the LTC3811 and all of the small-signal components surrounding the IC should be isolated from the power ground and PGND pin, and should be Kelvin-connected to the main ground node near the bottom terminal of the output capacitors.
2. Place the small-signal components away from high frequency switching nodes on the board. The pinout of the LTC3811 was carefully designed in order to make component placement as easy and noise free as possible. All of the power components can be placed on one side of the IC, away from all of the small-signal components.
3. The bottom terminals of the input and output capacitors should be placed as close as possible to one another, with the small-signal ground connection in between them. This component arrangement will reduce differential mode noise due to the two high di/dt loops in the power circuit.
4. If the output capacitor is located far away from the IC and the remote sense differential amplifier is being used to level-shift the output voltage back to the local IC ground, the small-signal ground around the LTC3811 should be Kelvin-connected to the main ground node near the bottom terminal of the input capacitor.
5. The PGND pin should be connected to the sources of the bottom MOSFETs using a wide, short trace on the top layer of the board. The MOSFETs should also be placed on the top layer of the board. The exposed area on the bottom of the QFN package is internally connected to the PGND node of the IC.
6. Place the $INTV_{CC}$ analog supply decoupling capacitor and resistor right next to the $INTV_{CC}$ and SGND pins on the same layer as the IC. A low ESR 0.1µF to 1µF ceramic capacitor should be used.
7. Place the DRV_{CC} gate driver supply decoupling capacitor right next the DRV_{CC} and PGND pins, on the same layer as the IC. This capacitor carries high di/dt MOSFET gate drive currents. A low ESR (X5R or better) 4.7µF to 10µF ceramic capacitor should be used.
8. The floating gate driver supply decoupling capacitor should be located right next the BOOST and SW pins, on the same layer as the IC. This capacitor carries high di/dt currents to drive the upper power MOSFETs. A low ESR (X5R or better) ceramic capacitor at least 100 times the total input capacitance of the upper power MOSFETs for that channel should be used.
9. The resistor divider connected to the FB pin to program the output voltage should be located as near as possible to the IC, with the bottom resistor connecting to the isolated signal ground node near the SGND pin. The PCB trace connecting the top resistor to the upper terminal of the output capacitor should avoid any high

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frequency switching nodes in the circuit and should ideally be shielded (both laterally and vertically) by ground planes.

10. If the differential remote sense amplifier is being used, the PCB traces connecting DIFF/IN$^+$ and DIFF/IN$^-$ to the output capacitor should avoid any high frequency switching nodes in the circuit and should ideally be shielded (both laterally and vertically) by ground planes. In addition, the DIFF/IN$^+$ and DIFF/IN$^-$ PCB traces should be routed parallel to one another with minimum spacing in between. Due to the 160kΩ input impedance of these pins, it is critical that these traces avoid any high frequency switching nodes in the circuit.
11. The high di/dt loops formed by the input capacitor and the power MOSFETs should be kept as small as possible to avoid EMI and differential mode switching noise. The upper power MOSFETs should be located close to one another and as close as possible to the positive terminal of the input decoupling capacitor. Do not attempt to split the input decoupling for the two channels as it can cause a large resonant loop.
12. The bottom MOSFETs sources should also be located close to one another and as close as possible to the negative terminal of the input capacitor. Since the inductor can be modeled as a current source, its placement on the board is less critical than the high di/dt components.
13. The switch node area should be kept small, with the upper power MOSFET sources and lower power MOSFET drains in close proximity.
14. The filter capacitor between the SENSE$^+$ and SENSE$^-$ pins, as well as the filter resistors, should be located as close as possible to the IC. In addition, the connections between the SENSE$^+$ and SENSE$^-$ filter resistors and the sense resistor should be routed parallel to one another with minimum spacing in between. These traces should avoid any high frequency switching nodes in the circuit.
15. Keep the switch nodes (SW1, SW2), the top gate nodes (TG1, TG2) and the boost nodes (BOOST1, BOOST2) away from sensitive small-signal nodes, especially from the opposite channel's voltage- and current-sensing feedback signals. The SW, TG and BOOST nodes can have slew rates in excess of 1V/ns relative to ground and should therefore be kept on the "output side" of the LTC3811.
16. Check the stress on the power MOSFETs by independently measuring the drain-to-source voltages directly across the devices terminals. Beware of inductive ringing that could exceed the maximum voltage rating of the MOSFET. If this ringing cannot be avoided and exceeds the maximum rating of the device, choose a higher voltage rated MOSFET.
17. When synchronizing the LTC3811 to an external clock, use a low impedance source such as a logic gate to drive the MODE/SYNC pin and keep the lead as short as possible.
18. Minimize the capacitive load on the CLKOUT pin to minimize excess phase shift. Buffer the CLKOUT signal with an emitter follower if necessary.

The diagram in Figure 28 illustrates all the branch currents in a 2-phase single output switching regulator. After studying the waveforms it is clear why it is critical to reduce the area of the high dV/dt nodes as much as possible. High electric and magnetic fields will radiate from these "loops," just as a radio station broadcasts a signal. The output capacitor ground should return to the negative terminal of the input capacitor and not share a common ground path with any switched current paths. The left half of the circuit gives rise to the "noise" generated by the switching regulator. The ground terminations of the synchronous MOSFETs and Schottky optional diodes should return to the bottom plate of the input capacitor with a short, isolated PC trace since very high di/dt currents are present. A separate, isolated path from the negative terminals of the input and output capacitors should be used to connect the IC signal ground pin (SGND). This technique keeps inherent signals generated by the high di/dt current pulses from taking alternate current paths that have finite impedances during the total period of the switching regulator.

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PC Board Layout Debugging

Start with one controller on at a time. It is helpful to use a DC-50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (SW pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation should be maintained over the input voltage range.

The duty cycle percentage should be maintained from cycle to cycle in a well-designed, low noise PCB implementation. Variation in the duty cycle at a subharmonic rate can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame a poor PC layout if regulator bandwidth optimization is not required. Only after each controller is checked for its individual performance should both controllers be turned on at the same time. A particularly difficult region of operation is when one controller channel is nearing its current comparator trip point when the other channel is turning on its top MOSFET. This occurs around 50% duty cycle on either channel due to the phasing of the internal clocks and may cause minor duty cycle jitter.

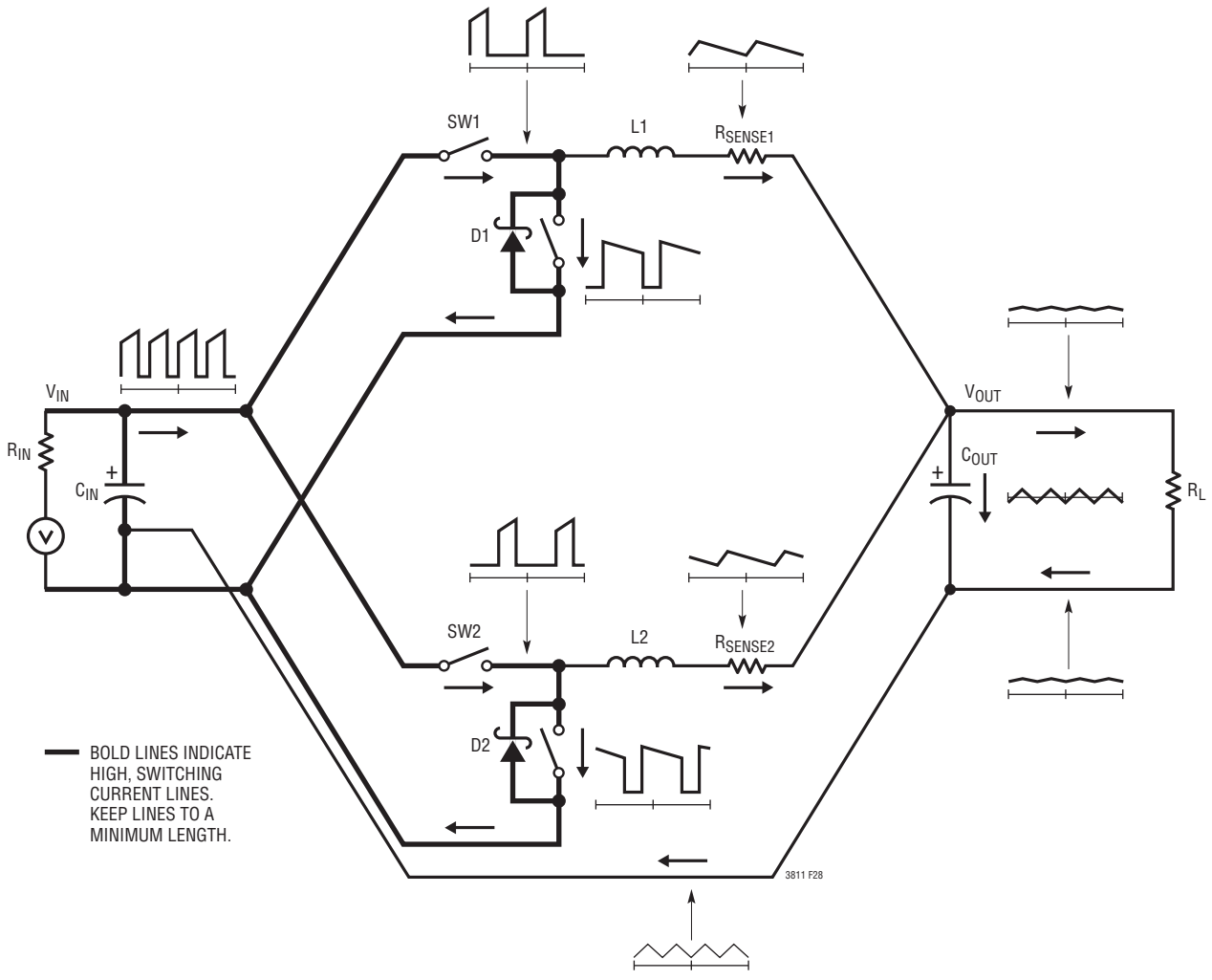


Figure 28. Instantaneous Current Path Flow in a Multiple Phase Switching Regulator

APPLICATIONS INFORMATION

Reduce V_{IN} from its nominal level to verify operation of the regulator at low V_{IN}. Check the operation of the under-voltage lockout circuit by further lowering V_{IN} while monitoring the outputs to verify operation.

Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, TG, and possibly BG connections and the sensitive voltage and current pins. The capacitor placed across the current sensing pins needs to be placed immediately adjacent to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling. If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between C_{IN}, Schottky and the top MOSFET components to the sensitive current and voltage sensing traces. In addition, investigate common ground path voltage pickup between these components and the SGND pin of the IC.

An embarrassing problem, which can be missed in an otherwise properly working switching regulator, results when the current sensing leads are hooked up backwards. The output voltage under this improper hookup will still be maintained but the advantages of current mode control will not be realized. Compensation of the voltage loop will be much more sensitive to component selection. This behavior can be investigated by temporarily shorting out the current sensing resistor—don't worry, the regulator will still maintain control of the output voltage.

TYPICAL APPLICATIONS

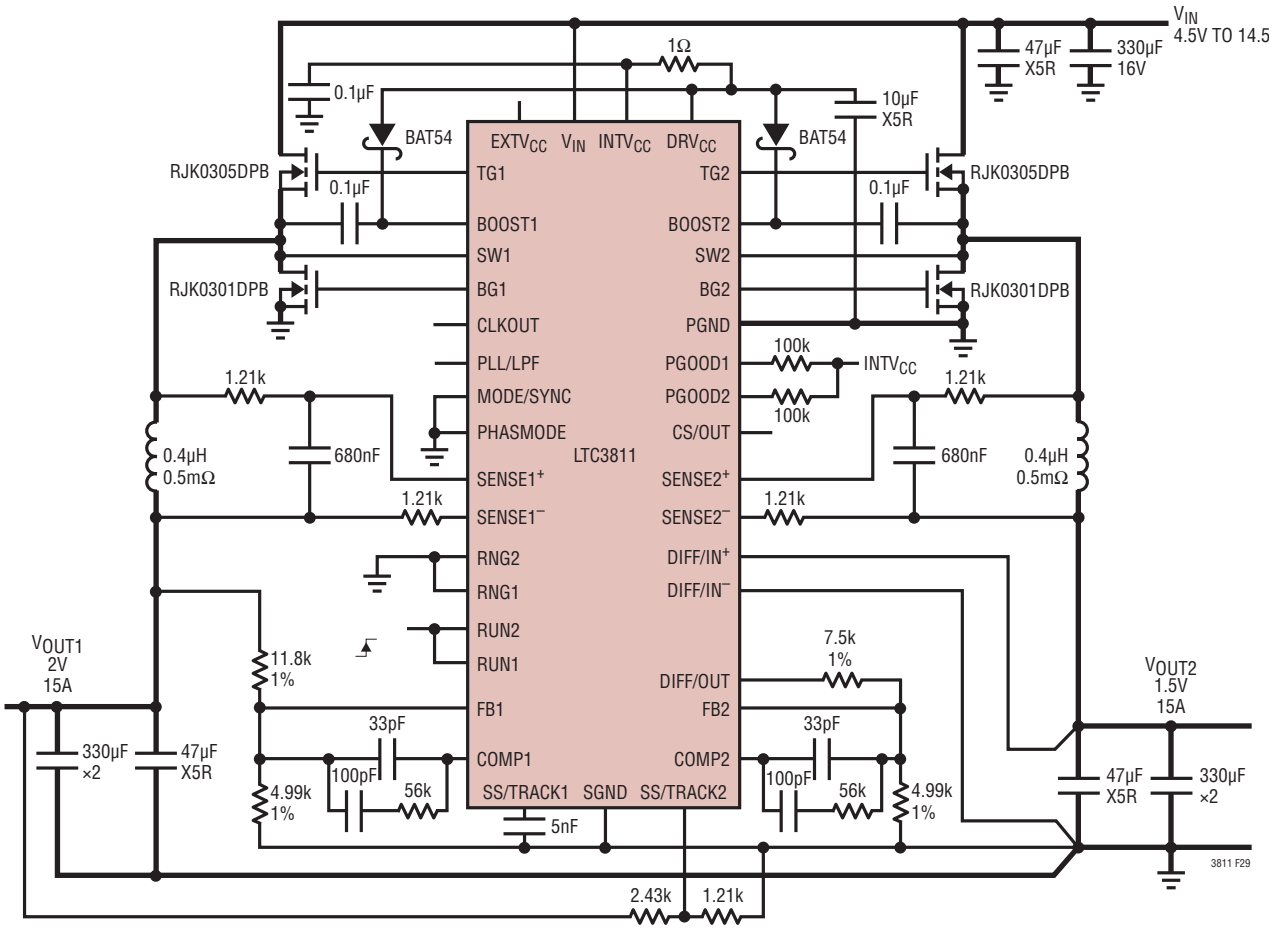


Figure 29. High Efficiency Core-I/O Power Supply with Differential Remote Sensing and Tracking

TYPICAL APPLICATIONS

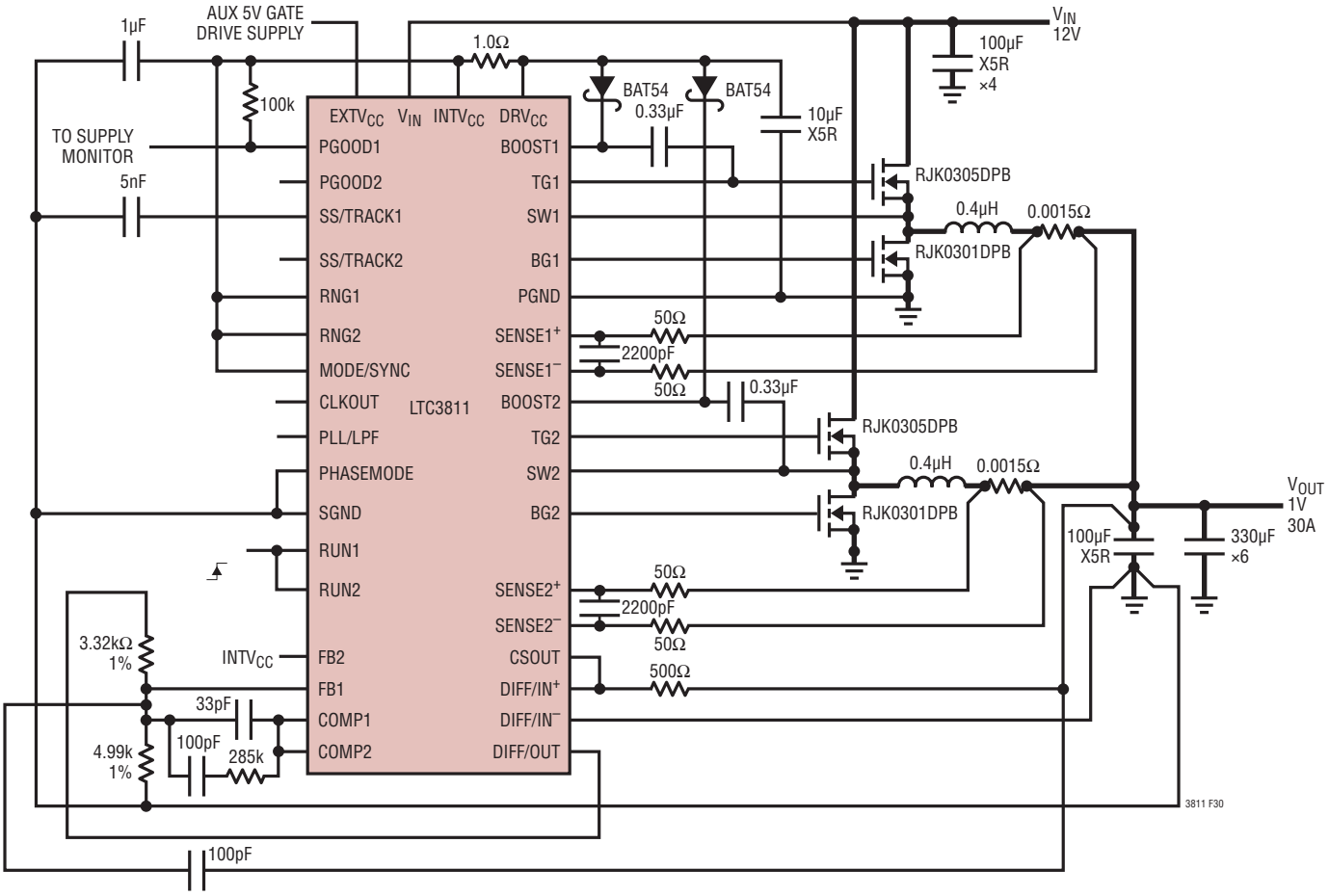


Figure 30. 2-Phase, 12V Input, 1V/30A Output ASIC Supply with Voltage Positioning

TYPICAL APPLICATIONS

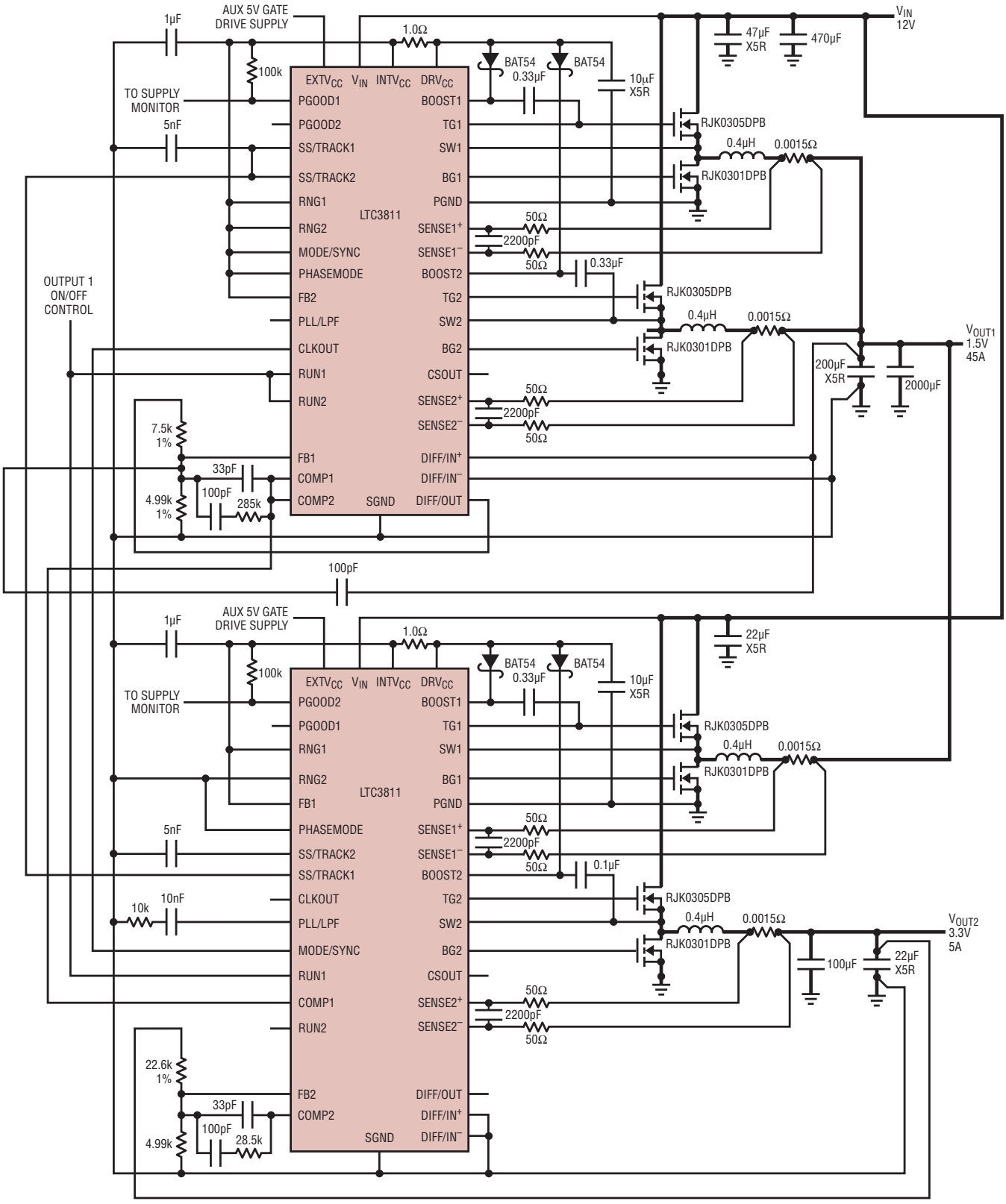
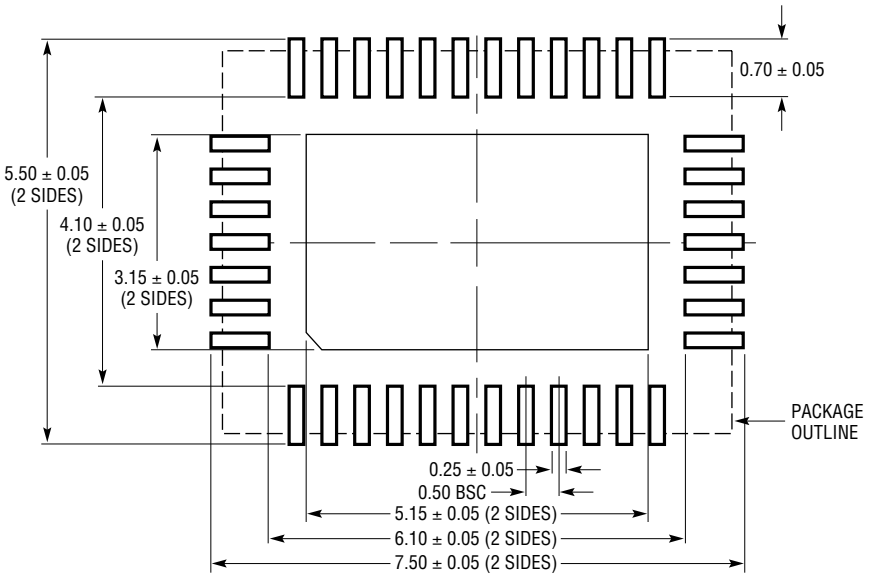


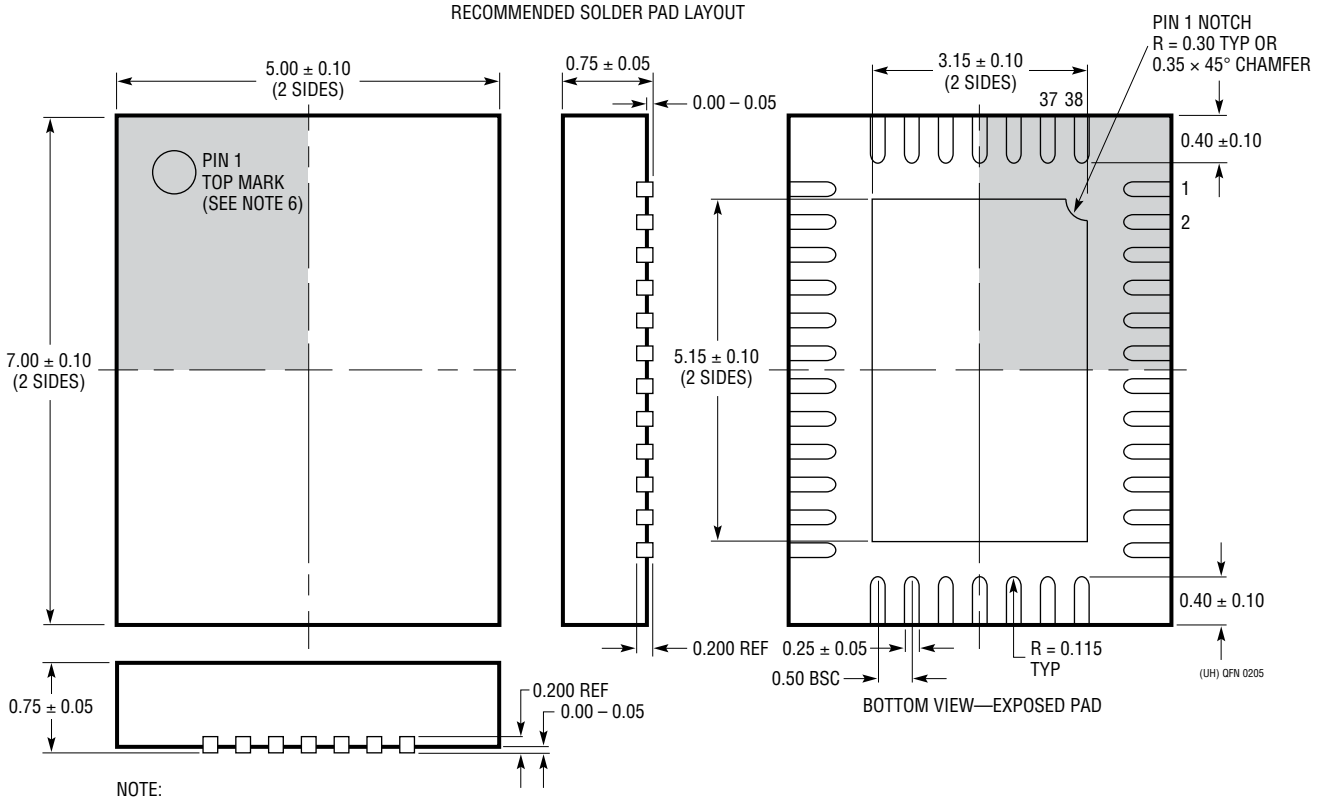
Figure 31. 3-Phase, 12V Input, 1.5V/45A Output with a 3.3V/5A Auxiliary Output

PACKAGE DESCRIPTION

UHF Package
38-Lead Plastic QFN (5mm × 7mm)
(Reference LTC DWG # 05-08-1701)



RECOMMENDED SOLDER PAD LAYOUT

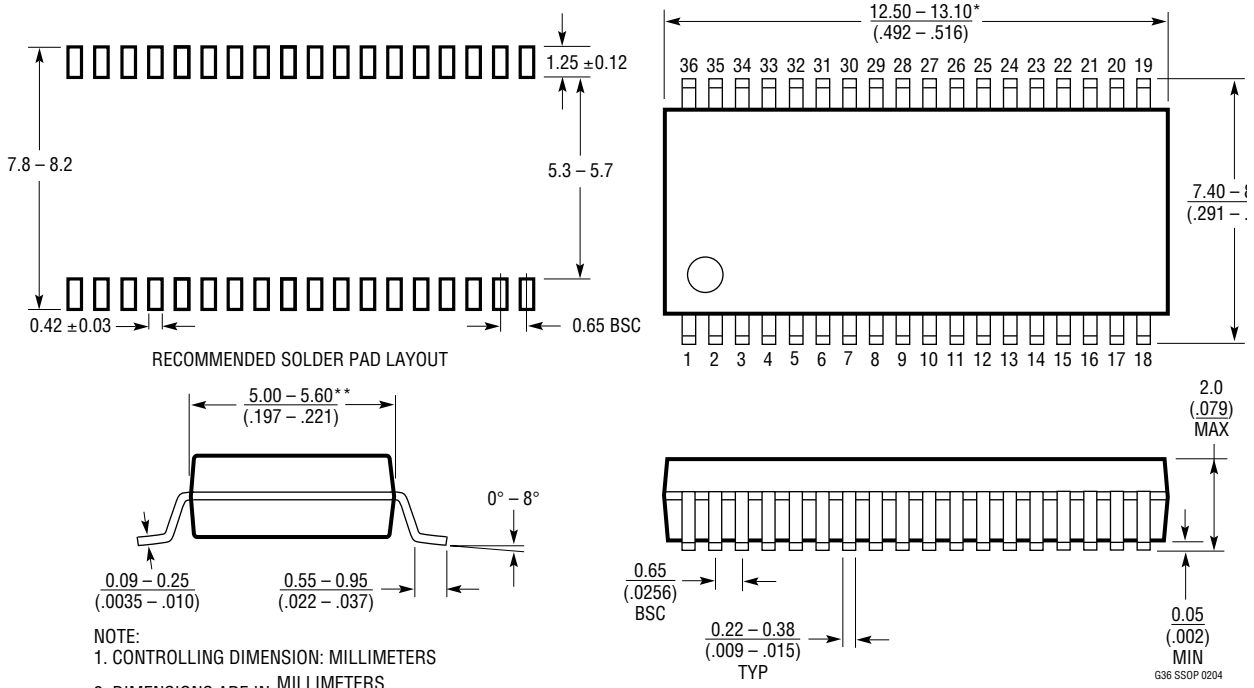


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE M0-220 VARIATION WHKD
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

G Package
36-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1628/LTC1628-PG/ LTC1628-SYNC	2-Phase, Dual Output Synchronous Step-Down DC/DC Controller	Reduces C_{IN} and C_{OUT}, Power Good Output Signal, Synchronizable, $3.5V \le V_{IN} \le 36V$, I_{OUT} Up to 20A, $0.8V \le V_{OUT} \le 5V$
LTC1735	High Efficiency Synchronous Step-Down Switching Regulator	Output Fault Protection, 16-Pin SSOP Package
LTC1778/LTC1778-1	No R_{SENSE}™ Current Mode Synchronous Step-Down Controllers	Up to 97% Efficiency, $4V \le V_{IN} \le 36V$, $0.8V \le V_{OUT} \le (0.9)(V_{IN})$, I_{OUT} Up to 20A
LTC3708	Dual, 2-Phase, DC/DC Controller with Output Tracking	Current Mode, No RSENSE, Up/Down Tracking, Synchronizable
LTC3727/LTC3727A-1	2-Phase Dual Synchronous Controller	$0.8V \le V_{OUT} \le 14V$; $4V \le V_{IN} \le 36V$
LTC3728	Dual, 550kHz, 2-Phase Synchronous Step-Down Controller	Dual 180° Phased Controllers, V_{IN} 3.5V to 35V, 99% Duty Cycle, 5mm × 5mm QFN and SSOP-28 Packages
LTC3729	20A to 200A, 550kHz PolyPhase Synchronous Controller	Expandable from 2-Phase to 12-Phase, Uses All Surface Mount Components, V_{IN} Up to 36V
LTC3731	3- to 12-Phase Step-Down Synchronous Controller	60A to 240A Output Current, $0.6V \le V_{OUT} \le 6V$, $4.5V \le V_{IN} \le 32V$
LTC3773	Triple Output DC/DC Synchronous Controller	3-Phase Step-Down DC/DC Controller, $3.3V \le V_{IN} \le 36V$, Fixed Frequency 160kHz to 700kHz
LTC3826/ LTC3826-1	Ultralow I_Q, Dual Output Synchronous Step-Down DC/DC Controller	50µA I_Q, $0.8V \le V_{OUT} \le 10V$, $4V \le V_{IN} \le 36V$
LTC3827/LTC3827-1	Dual, Selectable 140kHz to 650kHz 2-Phase, Synchronous Step-Down Controller	Low I_Q, V_{IN} from 4V to 36V, V_{OUT} from 0.8V to 10V, 5mm × 5mm QFN32
LTC3828	Dual, 2-Phase Synchronous Step-Down Controller with Tracking	Up to Six Phases, $0.8V \le V_{OUT} \le 7V$, $4.5V \le V_{IN} \le 28V$
LTC3835/LTC3835-1	Low I_Q Synchronous Step-Down Controller	Single Channel LTC3827/LTC3827-1
LT3845	Low I_Q, High Voltage Single Output Synchronous Step-Down DC/DC Controller	$1.23V \le V_{OUT} \le 36V$, $4V \le V_{IN} \le 60V$, 120µA I_Q
LTC3850	Dual, 550kHz, 2-Phase Synchronous Step-Down Controller	Dual 180° Phased Controllers, V_{IN} 4V to 24V, 97% Duty Cycle, 4mm × 4mm QFN-28, SSOP-28 Packages

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