THE DATASHEET OF

LTC3870IUFD#TRPBF

PolyPhase Step-Down Slave Controller for Digital Power System Management

FEATURES

- **LTC3880 Family Phase Extender Supporting LTC3880/3880-1, LTC3883/3883-1, LTC3886, LTC3887 Master Controllers**
- **Cascade with Multiple Chips for Very Large Current Applications**
- **Accurate PolyPhase Current Sharing**
- **$EXTV_{CC}$ Capable of 5V to 14V Input**
- Wide V_{IN} Range: 4.5V to 60V
- Wide Output Voltage Range : 0.5V to 14V
- Wide SYNC Frequency Range: 100kHz to 1MHz
- Pin Programmable of CCM/DCM Operation
- Pin Programmable of Phase-Shift Control
- Integrated Powerful N-Channel MOSFET Gate Drivers
- Available in a 28-Pin (4mm × 5mm) QFN Package

APPLICATIONS

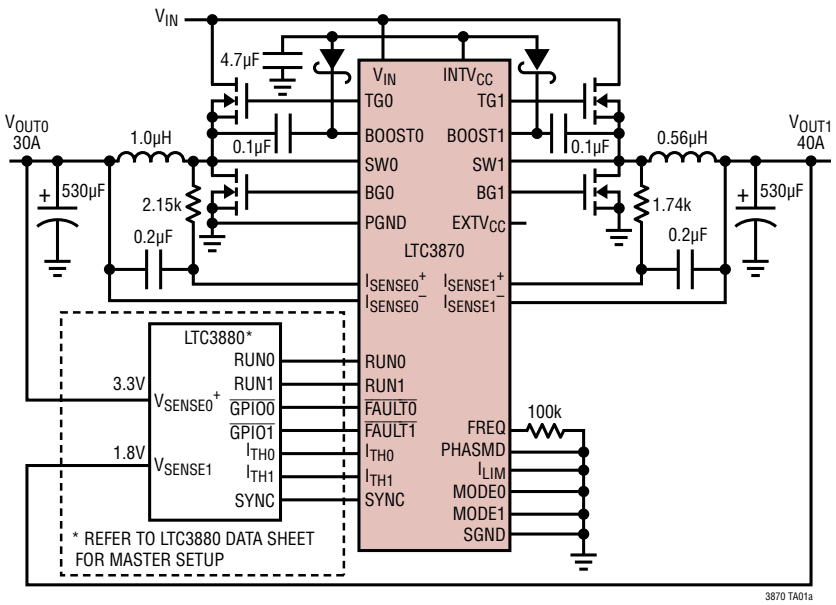
- High Power Distributed Power Systems
- Telecom Systems
- Industrial Applications

DESCRIPTION

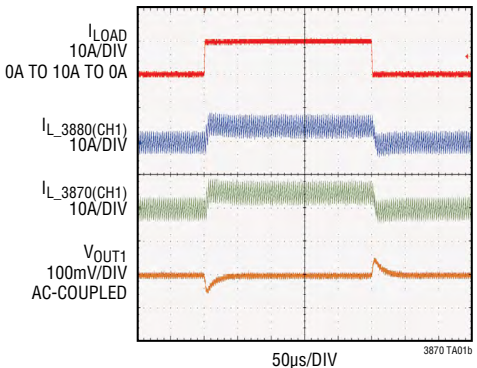
The LTC®3870 is a PolyPhase® step-down slave controller specially designed for multiphase operation with the LTC3880 family digital power system management DC/DC controllers. It provides a small and cost effective solution for supplying very large currents by cascading it with a master controller. A peak current mode architecture provides the LTC3870 with excellent current sharing from phase to phase and from chip to chip.

Coherently working with the LTC3880 family, the LTC3870 does not require additional I^2C addresses, and it supports all programmable features as well as fault protection. The constant switching frequency can be synchronized to an external clock from the master controller from 100kHz to 1MHz.

TYPICAL APPLICATION



Load Transient Response of a 2-Phase Master (3880)/Slave (3870) Converter



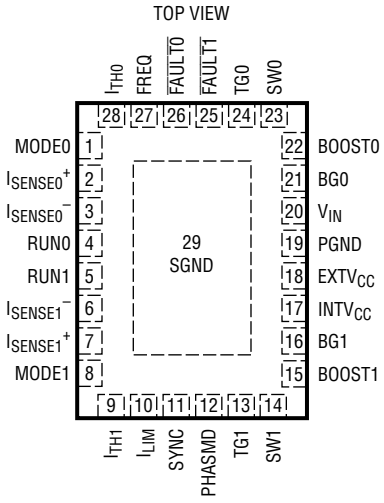
V_{IN} = 12V
V_{OUT1} = 1.8V

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} ..... –0.3V to 65V
BOOST0, BOOST1 ..... –0.3V to 71V
SW0, SW1 ..... –5V to 65V
I_{SENSE0}^+, I_{SENSE0}^-, I_{SENSE1}^+, I_{SENSE1}^- ..... –0.3V to 15V
(BOOST0-SW0), (BOOST1-SW1) ..... –0.3V to 6V
$INTV_{CC}$, RUN0/RUN1 ..... –0.3V to 6V
$EXTV_{CC}$ ..... –0.3V to 14V
MODE0/MODE1, FREQ, PHASMD, I_{LIM} ... –0.3V to $INTV_{CC}$
$\overline{FAULT0}$/$\overline{FAULT1}$, I_{TH0}/I_{TH1}, SYNC ..... –0.3V to 3.6V
$INTV_{CC}$, $EXTV_{CC}$ Peak Current (Note 9) 100mA
Operating Junction Temperature Range
..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W, θ_{JC_BOT} = 3.4°C/W
EXPOSED PAD (PIN 29) IS SGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3870EUFD#PBF	LTC3870EUFD#TRPBF	3870	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3870IUFD#PBF	LTC3870IUFD#TRPBF	3870	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2) V_{IN} = 15V, V_{RUN0}, V_{RUN1} = 3.3V, f_{SYNC} = 350kHz (externally driven) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Range	(Note 3)		4.5		60	V
V_{OUT}	Output Voltage Range	(Note 4)		0.5		14	V
I_Q	Input Voltage Supply Current Normal Operation	V_{RUN0}, V_{RUN1} = 0V (Note 5) V_{RUN0}, V_{RUN1} = 3.3V, No Caps on TG and BG			1.1 2.6		mA mA
V_{UVLO}	Undervoltage Lockout Threshold When V_{IN} > 4.2V	V_{INTVCC} Falling V_{INTVCC} Rising			3.7 4.0		V V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2) V_{IN} = 15V, V_{RUN0},V_{RUN1} = 3.3V, f_{SYNC} = 350kHz (externally driven) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Control Loop							
$I_{ISENSE0}^+$, $I_{ISENSE1}^+$	Current Sense + Pin Current	$V_{ISENSE0,1}^+$ = 3.3V	●		±0.1	±1	µA
$I_{ISENSE0}^-$, $I_{ISENSE1}^-$	Current Sense – Pin Current	$V_{ISENSE0,1}^-$ = 3.3V	●		±0.1	±1	µA
$V_{IILIMIT}$	Maximum Current Sense threshold (High Range)	V_{ITH} = 2.22V, I_{LIM} = $INTV_{CC}$	●	70	75	80	mV
	Maximum Current Sense threshold (Low Range)	V_{ITH} = 2.22V, I_{LIM} = GND	●	45	50	55	mV
Gate Drivers							
TG R_{UP}	Pull-Up On-Resistance	TG High			2.5		Ω
TG R_{DOWN}	Pull-down On-Resistance	TG Low			1.5		Ω
BG R_{UP}	Pull-Up On-Resistance	BG High			2.4		Ω
BG R_{DOWN}	Pull-down On-Resistance	BG Low			1.1		Ω
TG0, TG1 t_r t_f	TG Transition Time: Rise Time Fall Time	(Note 6) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 30 30		 ns ns
BG0, BG1 t_r t_f	BG Transition Time: Rise Time Fall Time	(Note 6) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 30 30		 ns ns
TG/BG t_{1D}	Top Gate Off to Bottom Gate On Delay Time	(Note 6) C_{LOAD} = 3300pF Each Driver			30		ns
BG/TG t_{2D}	Bottom Gate Off to Top Gate On Delay Time	(Note 6) C_{LOAD} = 3300pF Each Driver			30		ns
$t_{ON(MIN)}$	Minimum On-Time	(Note 7)			90		ns
$INTV_{CC}$ Regulator							
V_{INTVCC_VIN}	Internal V_{CC} Voltage No Load	6.0V <V_{IN} <60V, V_{EXTVCC} = 0 V		4.85	5.1	5.35	V
V_{LDO} INT	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 50mA, V_{EXTVCC} = 0V			0.8	±2	%
V_{INTVCC_EXT}	Internal V_{CC} Voltage No Load	V_{EXTVCC} = 8.5V (Note 8)		4.85	5.1	5.35	V
V_{LDO} EXT	$INTV_{CC}$ Load Regulation with $EXTV_{CC}$	I_{CC} = 0 to 20mA, V_{EXTVCC} = 8.5V			0.5	±2	%
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	V_{EXTVCC} Ramping Positive (Note 8)		4.7	4.8	4.9	V
V_{HYS_EXTVCC}	$EXTV_{CC}$ HYSTERESIS				200		mV
Oscillator and Phase-Locked Loop							
f_{SNYC}	Oscillator SYNC Range		●	100		1000	kHz
$V_{TH,SYNC}$	SYNC Input Threshold	$V_{TH,sync}$ Falling (Note 9) $V_{TH,sync}$ Rising			0.4 2.0		V V
f_{NOM}	Nominal Frequency	V_{FREQ} = 1.0V			500		kHz
I_{FREQ}	FREQ setting current			9	10	11	µA
θ_{SYNC}-θ_0	SYNC to Ch0 Phase Relationship Based on the Falling Edge of Sync and Rising Edge of TG0	PHASMD = 0 PHASMD = 1/3 $INTV_{CC}$ PHASMD = 2/3 $INTV_{CC}$ PHASMD = $INTV_{CC}$			180 60 120 90		Deg Deg Deg Deg
θ_{SYNC}-θ_1	SYNC to Ch1 Phase Relationship Based on the Falling Edge of Sync and Rising Edge of TG1	PHASMD = 0 PHASMD = 1/3 $INTV_{CC}$ PHASMD = 2/3 $INTV_{CC}$ PHASMD = $INTV_{CC}$			0 300 240 270		Deg Deg Deg Deg

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2) V_{IN} = 15V, V_{RUN0},V_{RUN1} = 3.3V, f_{SYNC} = 350kHz (externally driven) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Inputs RUN0/RUN1, MODE0/MODE1, $\overline{\text{FAULT0}}$/$\overline{\text{FAULT1}}$							
V_{IH}	Input High Threshold Voltage		●			2.0	V
V_{IL}	Input Low Threshold Voltage		●	1.4			V

Note 1: Stresses beyond those listed in under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3870 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3870E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3870I is guaranteed over the full –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the related package thermal impedance and other environmental factors. The junction temperature T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$T_J = T_A + (P_D \bullet 43°C/W)$

Note 3: When V_{IN} >15V, $EXTV_{CC}$ is recommended to reduce IC Temperature.

Note 4: Output voltage is set and controlled by the master controller in multiphase operations.

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Application Information.

Note 6: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

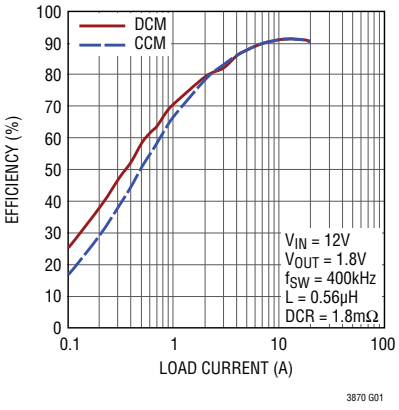
Note 7: The minimum on-time condition corresponds to an inductor peak-to-peak ripple current ≥40% of I_{MAX} (see Minimum On-Time Considerations in the Applications Information section.

Note 8: $EXTV_{CC}$ is enabled only if V_{IN} is higher than 6.5V.

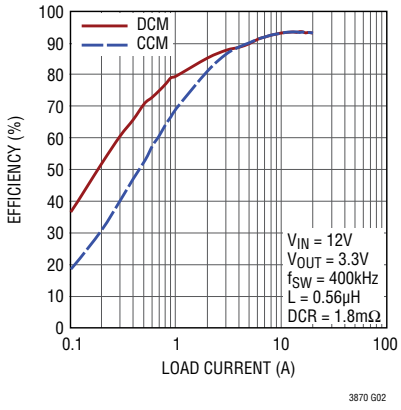
Note 9: Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

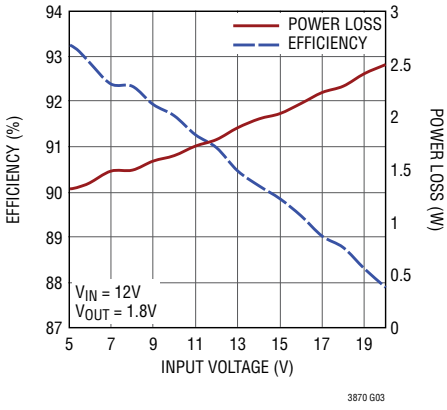
Efficiency vs Load Current



Efficiency vs Load Current

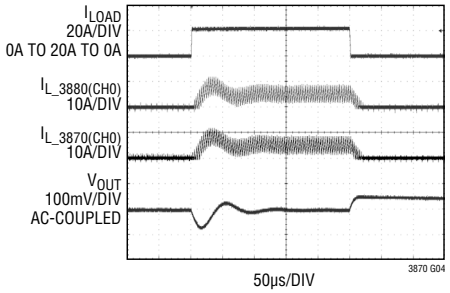


Full Load Efficiency and Power Loss vs Input Voltage



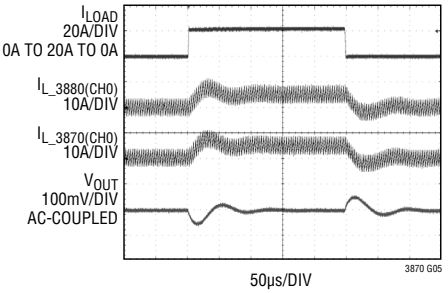
TYPICAL PERFORMANCE CHARACTERISTICS

Load Step (Discontinuous Conduction Mode) 4-Phase Operation LTC3880 and LTC3870



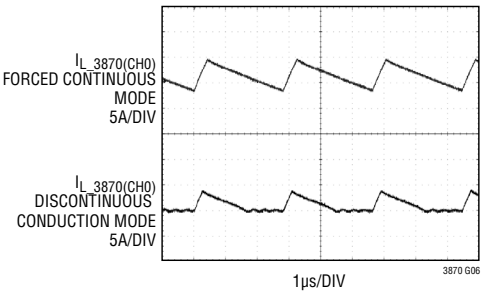
V_{IN} = 12V
V_{OUT} = 1.8V

Load Step (Forced Continuous Mode) 4-Phase Operation LTC3880 and LTC3870



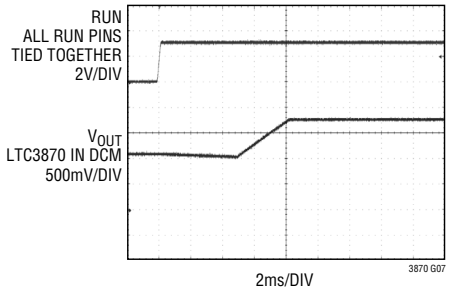
V_{IN} = 12V
V_{OUT} = 1.8V

Inductor Current at Light Load



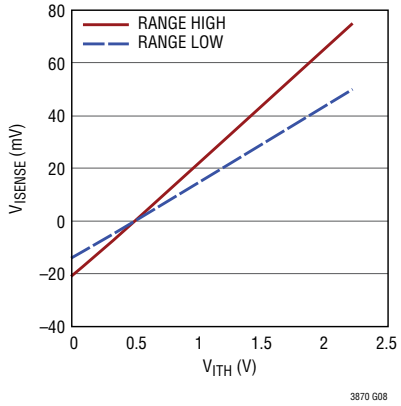
V_{IN} = 12V
V_{OUT} = 1.8V
I_{LOAD} = 1A

Start-Up Into a Pre-Biased Output 4-Phase Operation LTC3880 and LTC3870

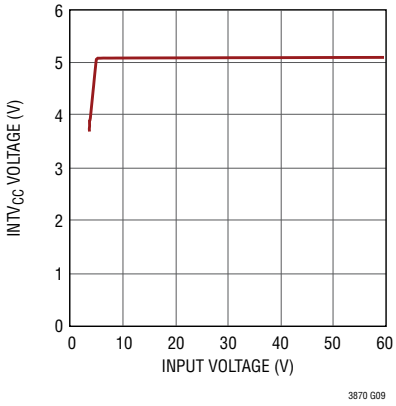


V_{IN} = 12V
V_{OUT} = 1.8V

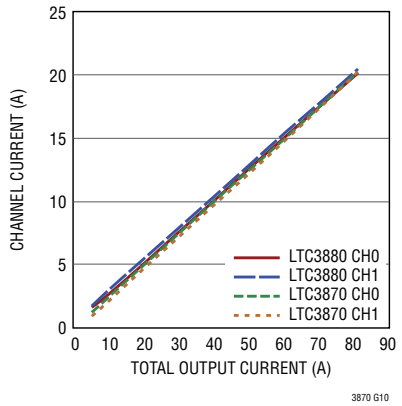
Current Sense Threshold vs I_{TH} Voltage



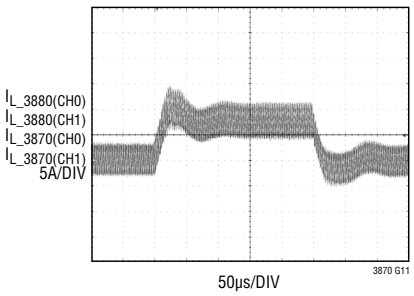
$INTV_{CC}$ Line Regulation



DC Output Current Matching Between LTC3880 and LTC3870

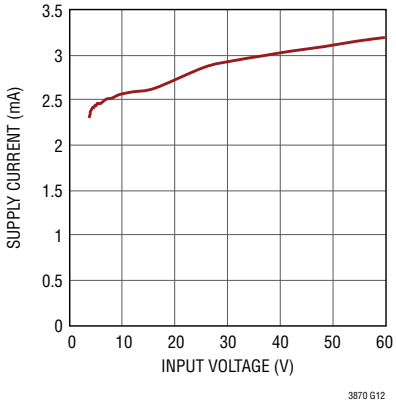


Dynamic Current Sharing During a Load Transient in a 4-Phase Operation LTC3880 and LTC3870



I_{LOAD} 0A TO 32A TO 0A

Quiescent Current vs Input Voltage Without $EXTV_{CC}$



PIN FUNCTIONS

MODE0/MODE1 (Pin 1/Pin 8): DCM/CCM Mode Control Pins. Channel0/Channel1 operates in forced continuous mode if MODE0/MODE1 pin is logic high. There is a 500kΩ pull down resistor on MODE0/MODE1 internally. The default operation mode in each channel is discontinuous mode operation unless these pins are actively driven high.

I_{SENSE0}^+/I_{SENSE1}^+ (Pin 2/Pin 7): Current Sense Comparator positive inputs, normally connected to the positive node of the DCR sensing networks or current sensing resistors.

I_{SENSE0}^-/I_{SENSE1}^- (Pin 3/Pin 6): Current Sense Comparator negative inputs, normally connected to the negative node of the DCR sensing network or current sensing resistors.

RUN0/RUN1 (Pin 4/Pin 5): Enable RUN Input Pins. Logic high on these pins enables the corresponding channel. In multiphase operation, these pins are connected to master RUN pins.

I_{TH0}/I_{TH1} (Pin 28/Pin 9): Current Control Threshold. Each associated channel's current comparator tripping threshold increases with its I_{TH} voltage. In multiphase operation, these pins are connected to the master controller's I_{TH} pins for current sharing.

I_{LIM} (Pin 10): Program Current Comparators' Sense Voltage Range. This pin can be tied to SGND or $INTV_{CC}$ to select the maximum current sense threshold for each current comparator. SGND sets both channels' current low range with maximum 50mV sensing voltage. $INTV_{CC}$ sets both channels' current high range with maximum 75mV sensing voltage. For equal current sharing, the setup on the I_{LIM} pin has to be same as the setup on the bit 7 of MFR_PWM_MODE_3880/3883/3886/3887 register in the master controller. See Table 2 in the Operation Section for details.

SYNC (Pin 11): External Clock Synchronization Input. If an external clock is present at this pin, the switching frequency will be synchronized to the falling edge of the external clock. In multiphase operation, this pin is connected to the master's SYNC pin for frequency synchronization. Do not float the SYNC pin.

PHASMD (Pin 12): Phase Set Pin. This pin can be tied to SGND, $INTV_{CC}$ or a resistor divider from $INTV_{CC}$ to SGND. This pin determines the relative phases between the external clock on the SYNC pin and the internal controllers. See Table 1 in the Operation Section for details.

TG0/TG1 (Pin 24/Pin 13): Top Gate Driver Outputs. These are the outputs of floating drivers with a voltage swing equal to $INTV_{CC}$ superimposed on the switch node voltages.

SW0/SW1 (Pin 23/Pin 14): Switch Node Connections to Inductors. Voltage swings at the pins are from a Schottky diode (external) voltage drop below ground to V_{IN}.

BOOST0/BOOST1 (Pin 22/Pin 15): Boosted Floating Driver Supplies. The (+) terminal of the bootstrap capacitors connect to these pins. These pins swing from a diode voltage drop below $INTV_{CC}$ up to V_{IN} + $INTV_{CC}$.

BG0/BG1 (Pin 21/Pin 16): Bottom Gate Driver Outputs. These pins drive the gates of the bottom N-Channel MOSFETs between PGND and $INTV_{CC}$.

$INTV_{CC}$ (Pin 17): Internal Regulator 5V Output. The internal control circuits are powered from this voltage. Bypass this pin to PGND with a minimum of 4.7µF low ESR tantalum or ceramic capacitor. $INTV_{CC}$ is enabled as soon as V_{IN} is powered.

$EXTV_{CC}$ (Pin 18): External power input to an internal LDO connected to $INTV_{CC}$. This LDO supplies $INTV_{CC}$ power bypassing the internal LDO powered from V_{IN} whenever $EXTV_{CC}$ is higher than 4.8V. See $EXTV_{CC}$ connection in the Applications Information Section. Do not exceed 14V on this pin. Bypass this pin to PGND with a minimum of 4.7µF low ESR tantalum or ceramic capacitor. If the $EXTV_{CC}$ pin is not used, leave it open or tie it to ground. $EXTV_{CC}$ can be present before V_{IN}. However, $EXTV_{CC}$ is enabled only if V_{IN} is higher than 6.5V.

PGND (Pin 19): Power Ground Pin. Connect this pin closely to the sources of the bottom N-Channel MOSFETs and the (–) terminals of C_{IN}.

V_{IN} (Pin 20): Main Input Supply. Bypass this pin to PGND with a capacitor (0.1µF to 1µF).

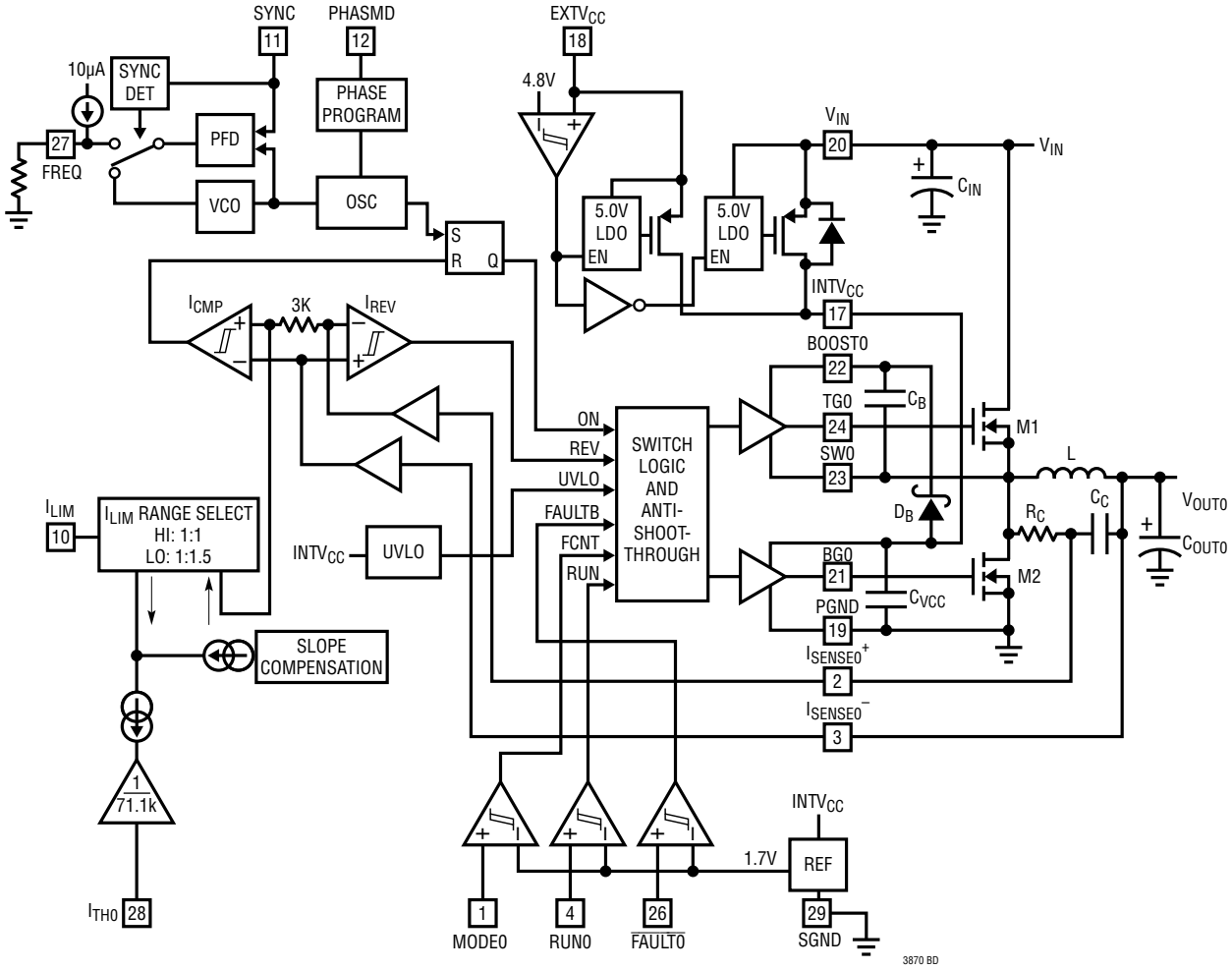
PIN FUNCTIONS

$\overline{\text{FAULT0}}$/$\overline{\text{FAULT1}}$ (Pin 26/Pin 25): Fault Input Pins. Connect these pins to the master chip $\overline{\text{GPIO}}$ pins to respond to fault signals from the master controller. If this pin is low, both TG and BG pins are pulled down at the corresponding channel. There is a 500k pull down resistor on $\overline{\text{FAULT0}}$/$\overline{\text{FAULT1}}$ internally. These pins have to be driven high externally for normal operation.

FREQ (Pin 27): Frequency Set Pin. There is a precision 10µA current flowing out of this pin. A resistor to ground sets a voltage which in turn programs the frequency. This pin sets the default switching frequency when there is no external clock on the SYNC pin. Set the frequency close to the external clock to help the internal PLL sync to the SYNC pin clock quickly and smoothly. See the application section for the detailed information.

SGND (Exposed Pad Pin 29): Signal Ground. All small-signal and compensation components should connect to this ground, which in turn connects to PGND at one point. The exposed pad must be soldered to the PCB, providing a local ground for the control components of the IC, and be tied to PGND under the IC.

BLOCK DIAGRAM (CH0 Shown)



OPERATION

Main Control Loop

The LTC3870 is a constant frequency, current mode step-down slave controller for parallel operation with the LTC3880 family master controllers. During normal operation, each top MOSFET is turned on when the clock for that channel sets the RS latch, and turned off when the main current comparator, ICMP, resets the RS latch. The peak inductor current at which ICMP resets the RS latch is controlled by the voltage on the I_{TH} pin, which is tied directly to the corresponding I_{TH} pin of the master controllers. When the load current increases, master controllers drive and increase the I_{TH} voltage, which in turn cause the peak current in the corresponding slave channels to increase, until the average inductor current matches the new load current. After the top MOSFET has been turned off, the bottom MOSFET is turned on until the beginning of the next cycle in Continuous Conduction Mode (CCM) or until the inductor current starts to reverse, as indicated by the reverse current comparator I_{REV}, in Discontinuous Conduction Mode (DCM). The LTC3870 slave controllers DO NOT regulate the output voltage but regulate the current in each channel for current sharing with master controllers. Output voltage regulation is achieved through the voltage feedback loops in master controllers.

$INTV_{CC}/EXTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most other internal circuitry is derived from the $INTV_{CC}$ pin. Normally an internal 5.0V linear regulator supplies $INTV_{CC}$ power from V_{IN}. In high V_{IN} applications, if a high efficiency external voltage source is available for the $EXTV_{CC}$ pin, another internal 5.0V linear regulator is enabled and supplies $INTV_{CC}$ power from $EXTV_{CC}$. To enable the linear regulator driven by the $EXTV_{CC}$ pin, V_{IN} has to be higher than 6.5V and $EXTV_{CC}$ pin voltage has to be higher than 4.8V. Do not exceed 14V on the $EXTV_{CC}$ pin.

Each top MOSFET driver is biased from the floating bootstrap capacitor C_B, which normally recharges during each off cycle through an external diode when the top MOSFET turns off. If the input voltage V_{IN} decreases to a voltage close to V_{OUT}, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector detects this and forces the top MOSFET off for about one-twelfth of the clock period plus 100ns every three cycles to allow C_B to recharge. However, it is recommended that a load be present or the IC operates at low frequency during the drop-out transition to ensure C_B is recharged.

Start-Up and Shutdown (RUN0, RUN1)

The two channels of the LTC3870 can independently start up and shut down using the RUN0 and RUN1 pins. Pulling either of these pins below 1.4V shuts down the control circuits for that channel. During shutdown, both TG and BG are pulled down to turn off the external power MOSFETs. Pulling either of these pins above 2V enables the corresponding channel and internal circuits. During startup, the RUN0/RUN1 pins are actively pulled down until the $INTV_{CC}$ voltage passes the under-voltage lockout threshold of 4V. For multiphase parallel operation, the RUN0/RUN1 pins have to be connected and driven by the RUN pins of the master controller. Do not exceed the Absolute Maximum Rating of 6V on these pins.

The start-up of each channel's output voltage V_{OUT} is controlled and programmed by the master controller. After the RUN pins are released, the master controller drives the output based on the programmed delay time and rise time, and the slave controller LTC3870 just follows the master to supply equivalent current to the output during startup.

Light Load Current Operation (Discontinuous Conduction Mode, Continuous Conduction Mode)

The LTC3870 can be set to operate either in Discontinuous Conduction Mode (DCM) or forced Continuous Conduction Mode (CCM). To select forced Continuous Mode of operation, tie the MODE pin to a DC voltage above 2V (e.g., $INTV_{CC}$). To select discontinuous conduction mode of operation, tie the MODE pin to a DC voltage below 1.4V (e.g., SGND). In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the I_{TH} pin. In this mode, the efficiency at light loads is lower than in discontinuous Mode operation. However, continuous mode has the advantages of lower output ripple and less interference with audio circuitry. When the MODE pin is connected to

OPERATION

SGND, the LTC3870 operates in discontinuous mode at light loads. At very light loads, the current comparator ICMP may remain tripped for several cycles and force the external top MOSFET to stay off for the same number of cycles (i.e., skipping pulses). This mode provides higher light load efficiency than forced continuous mode and the inductor current is not allowed to reverse. There are 500k pull down resistors internally connected to the MODE0/MODE1 pins. If MODE0/MODE1 pins are floating, both channels default to discontinuous conduction mode.

Multichip Operation (PHASMD and SYNC Pins)

The PHASMD pin determines the relative phases between the internal channels as well as the external clock signal on the SYNC pin, as shown in Table 1. The phases tabulated are relative to zero degree phase being defined as the **falling edge** of the clock on SYNC.

Table 1.

PHASMD	Channel 0 Phase	Channel 1 Phase
GND	180°	0°
1/3 $INTV_{CC}$	60°	300°
2/3 $INTV_{CC}$ or Float	120°	240°
$INTV_{CC}$	90°	270°

The SYNC pin is used to synchronize switching frequency between master and slave controllers. Input capacitance ESR requirements and efficiency losses are substantially reduced because the peak current drawn from the input capacitor is effectively divided by the number of phases used and power loss is proportional to the RMS current squared. A two-phase, single output voltage implementation can reduce input path power loss by 75% and radically reduce the required RMS current rating of the input capacitor(s).

Single Output Multiphase Operation

The LTC3870 is designed for multiphase converters with the master controller by making these connections:

Tie all the I_{TH} pins of paralleled channels together for current sharing between masters and slaves. Note that I_{LIM} setup on slaves has to match MFR_PWM_MODE current range setup in masters.

Tie all SYNC pins together between master and slaves for same switching frequency synchronization; one and only one of the master controllers has to be programmed as master to generate clock signal on the SYNC pin.

Tie all the RUN pins of paralleled channels together between master and slaves for startup and shutdown sequences.

Tie the $\overline{GPIO}$ pin of the master controller to the $\overline{FAULT}$ pin of slave controllers and program the master $\overline{GPIO}$ as fault sharing for fault protections.

Examples of single output multiphase converters are shown in Figure 1.

Inductor Current Sensing

Like the LTC3880/LTC3883, LTC3870 can use either inductor DCR or R_{SENSE} to sense the inductor current. Inductor DCR current sensing provides a lossless method of sensing the instantaneous current. Therefore, it can provide higher efficiency for applications with high output currents. However, the DCR of a copper inductor typically has 10% tolerance. For precise current sensing, a precision sensing resistor R_{SENSE} can be used to sense the inductor current. It is important to match the current sensing circuit between master controllers and slave controllers to guarantee balanced load sharing and overcurrent protection.

OPERATION

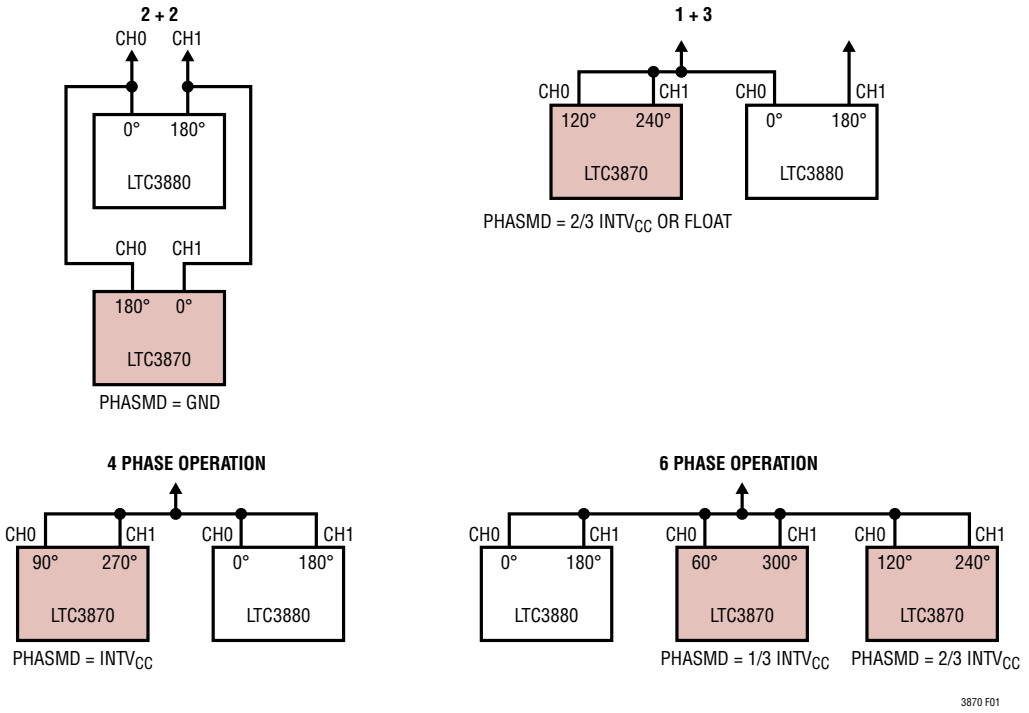


Figure 1. Examples of Single/Dual Output Multiphase Converters

Frequency Selection and Phase-Locked Loop (FREQ and SYNC Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage. The switching frequency of the LTC3870 controllers can be synchronized to the falling edge of the external clock on the SYNC pin or selected using the FREQ pin. A phase-locked loop (PLL) is integrated in the LTC3870 to synchronize the internal oscillator to an external clock source that is connected to the SYNC pin; this source is normally provided by the master controllers. The PLL loop filter network is integrated inside the LTC3870. The phase-locked loop is capable of locking to any frequency within the range of 100kHz to 1MHz.

If the SYNC pin is not being driven by an external clock source, the FREQ pin can be used to program the LTC3870's operating frequency from 100kHz to 1MHz. There is a precision 10µA current flowing out of the FREQ pin, so the user can program the controller's switching frequency with a single resistor to SGND. A curve is provided later in the application section showing the relationship between the voltage on the FREQ pin and switching frequency. The frequency setting resistor should always be present to set the controller's initial switching frequency before locking to the external clock.

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The Typical Application on the first page of this data sheet is a basic LTC3870 application circuit featuring the LTC3880 as a slave controller. In paralleled operation, the current sensing scheme as well as the power stage parameters in LTC3870 must be the same as the master controller to achieve balanced current sharing between masters and slaves. Finally, input and output capacitors are selected based on RMS current rating, ripple, and transient specs.

Current Limit Programming

To match the master controller current limit, each channel of LTC3870 can be programmed separately with two current ranges. The I_{LIM} pin of LTC3870 is a 4-level logic input which sets the current limit of LTC3870. When I_{LIM} is grounded, both channel0 and channel1 are set to be low current range. When I_{LIM} is tied to $INTV_{CC}$, both channel0 and channel1 are set to be high current range. Here, low current range means the current sense threshold linearly increases from 0mV to 50mV as I_{TH} voltage is increased from 0.5V to 2.22V without slope compensation. High current range means the current sense threshold increases to 75mV as I_{TH} voltage is increased to 2.22V without slope compensation. Set I_{LIM} to one-third $INTV_{CC}$ for channel0 high current range and channel1 low current range. Set I_{LIM} to two-thirds $INTV_{CC}$ or float for channel0 low current range and channel1 high current range. The summary of I_{LIM} pin setups is shown in Table 2. For balanced load current sharing, use the same current range setting as in the master controller. Note that the LTC3870 does not have active clamping circuit on I_{TH} pin for peak current limit and over current protection. Over current protection relies on the master controller to drive and clamp the I_{TH} pin voltage not to exceed the programmed voltage through the PMBus command.

Table 2.

I_{LIM}	Channel 0 Current limit	Channel 1 Current limit
GND	Range Low	Range Low
1/3 $INTV_{CC}$	Range High	Range Low
2/3 $INTV_{CC}$ or Float	Range Low	Range High
$INTV_{CC}$	Range High	Range High

$INTV_{CC}$ Regulators and $EXTV_{CC}$

The LTC3870 features a PMOS LDO that supplies power to $INTV_{CC}$ from the V_{IN} supply. $INTV_{CC}$ powers the gate drivers and most of the LTC3870's internal circuitry. The linear regulator regulates the voltage at the $INTV_{CC}$ pin to 5.0V when V_{IN} is greater than 6V. $EXTV_{CC}$ connects to $INTV_{CC}$ through another PMOS LDO and can supply the needed power when its voltage is higher than 4.8V and V_{IN} is higher than 6.5V. Each of these LDOs can supply a peak current of 100mA and must be bypassed to ground with a minimum of 4.7µF ceramic capacitor or low ESR electrolytic capacitor. No matter what type of bulk capacitor is used, an additional 0.1µF ceramic capacitor placed directly adjacent to the $INTV_{CC}$ and PGND pins is highly recommended. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers and to prevent interaction between the channels.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC3870 to be exceeded. The $INTV_{CC}$ current, which is dominated by the gate charge current, may be supplied by either the 5.0V linear regulator from V_{IN} or the linear regulator from $EXTV_{CC}$. When the voltage on the $EXTV_{CC}$ pin is less than 4.8V, the linear regulator from V_{IN} is enabled. Power dissipation for the IC in this case is highest and is equal to $V_{IN} \bullet I_{INTVCC}$. The gate charge current is dependent on operating frequency. The junction temperature can be estimated by using the equations given in Note 2 of the Electrical Characteristics. For example, the LTC3870 $INTV_{CC}$ current is limited to less than 34mA from a 38V supply in the UFD package and not using the $EXTV_{CC}$ supply:

$$T_J = 70°C + (34mA)(38V)(43°C/W) = 125°C$$

where ambient temperature is 70°C and thermal resistance from junction to ambient is 43°C/W.

To prevent the maximum junction temperature from being exceeded, the input supply current must be checked while operating in continuous conduction mode (MODE = $INTV_{CC}$) at maximum V_{IN}. When the voltage applied to $EXTV_{CC}$ rises above 4.8V and V_{IN} above 6.5V, the $INTV_{CC}$ linear regulator is turned off and the $EXTV_{CC}$ linear regulator is turned on. Using the $EXTV_{CC}$ allows the MOSFET driver

APPLICATIONS INFORMATION

and control power to be derived from other high efficiency sources such as +5V or +12V rails in the system. Using $EXTV_{CC}$ can significantly reduce the IC temperature in high V_{IN} applications. Tying the $EXTV_{CC}$ pin to a 5V supply reduces the junction temperature in the previous example from 125°C to: $T_J = 70°C + (34mA)(5V)(43°C/W) = 77°C$. Do not apply more than 14V to the $EXTV_{CC}$ pin.

For applications where the main input power is 5V, tie the V_{IN} and $INTV_{CC}$ pins together and tie the combined pins to the 5V input with a 1Ω or 2.2Ω resistor as shown in Figure 2 to minimize the voltage drop caused by the gate charge current. This will override the $INTV_{CC}$ linear regulator and will prevent $INTV_{CC}$ from dropping too low due to the dropout voltage. Make sure the $INTV_{CC}$ voltage is at or exceeds the $R_{DS(ON)}$ test voltage for the MOSFET which is typically 4.5V for logic-level devices.

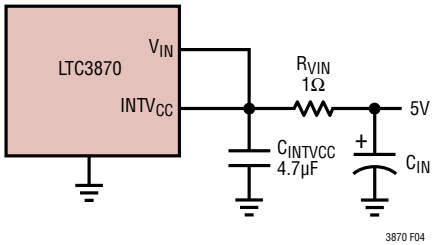

Figure 2. Setup for a 5V Input

Topside MOSFET Driver Supply (CB, DB)

External bootstrap capacitor C_B, connected to the BOOST pin, supplies the gate drive voltages for the topside MOSFET. Capacitor C_B in the Functional Diagram is charged though external diode DB from $INTV_{CC}$ when the SW pin is low. When the topside MOSFET is to be turned on, the driver places the C_B voltage across the gate source of the MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage, SW, rises to V_{IN} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the input supply:

$$V_{BOOST} = V_{IN} + V_{INTVCC} - V_{DB}$$

The value of the boost capacitor, C_B, needs to be 100 times that of the total input capacitance of the topside MOSFET(s).

The reverse breakdown of the external Schottky diode must be greater than $V_{IN(MAX)}$. When adjusting the gate drive level, the final arbiter is the total input current for the regulator. If a change is made and the input current decreases, then the efficiency has improved. If there is no change in input current, then there is no change in efficiency.

Undervoltage Lockout

The LTC3870 has a precision UVLO comparator constantly monitoring the $INTV_{CC}$ voltage to ensure that an adequate gate-drive voltage is present. It locks out the switching action and pulls down RUN pins when $INTV_{CC}$ is below 3.7V. To prevent oscillation when there is a disturbance on the $INTV_{CC}$, the UVLO comparator has 300mV of precision hysteresis. In multiphase operation, when LTC3870 is in undervoltage lockout, the RUN0 and RUN1 pins are pulled down to disable the master's switching action.

Phase-Locked Loop and Frequency Synchronization

The LTC3870 has a phase-locked loop (PLL) comprised of an internal voltage-controlled oscillator (VCO) and a phase detector. This allows the internal clock to be locked to the falling edge of an external clock signal applied to the SYNC pin. The turn-on of channel 0/channel 1's top MOSFET is synchronized or out-of-phase with the falling edge of the external clock. The phase detector is an edge sensitive digital type that provides zero degree phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

The output of the phase detector is a pair of complementary current sources that charge or discharge the internal filter network. There is a precision 10µA of current flowing out of the FREQ pin. This allows the user to use a single resistor to SGND to set the switching frequency when no external clock is applied to the SYNC pin. The voltage on the FREQ pin is equal to the resistance multiplied by 10µA current (e.g. the voltage is 1V with a 100k resistor from the FREQ pin to SGND). The internal switch between FREQ pin and the integrated PLL filter network is ON, allowing the filter network to be pre-charged to the same voltage potential as the FREQ pin. The relationship between the voltage on the FREQ pin and the operating frequency is shown in Figure 3 and specified in the Electrical Characteristic table. If an external clock is detected on the SYNC pin, the internal switch mentioned above will turn off and isolate

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the influence of FREQ pin. Note that the LTC3870 can only be synchronized to an external clock whose frequency is within the range of the LTC3870's internal VCO. This is guaranteed to be between 100kHz and 1MHz. A simplified block diagram is shown in Figure 4.

If the external clock frequency is greater than the internal oscillator's frequency, f_{OSC}, then current is sourced continuously from the phase detector output, pulling up the filter network. When the external clock frequency is less than f_{OSC}, current is sunk continuously, pulling down the filter network. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage on the filter network is adjusted until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the phase detector output is high impedance and the filter capacitor holds the voltage.

Typically, the external clock (on SYNC pin) input high threshold is 2V, while the input low threshold is 0.4V.

Fault Protection and Responses

LTC3880 family master controllers monitor system voltage, current, and temperature and provide many protection features during fault conditions. LTC3870 slave controllers do not provide as many fault monitors as master controllers and have to respond to fault signals from the master controller. $\overline{FAULT0}$ and $\overline{FAULT1}$ pins are designed to share fault signals between masters and slaves. In a typical parallel application, connect the $\overline{FAULT}$ pins on LTC3870 to the master $\overline{GPIO}$ pins of the corresponding paralleled channels and program the master $\overline{GPIO}$ as fault sharing, so that the slave controller can respond to all fault protections from the master. When the $\overline{FAULT}$ pin is pulled below 1.4V, both TG and BG in the corresponding channel are pulled down and external MOSFETs are turned off. When the $\overline{FAULT}$ pin voltage is above 2V, the corresponding channel is back to the normal operation. During fault conditions, all internal circuits in LTC3870 are still running so the slave controllers can immediately go back to normal operation when the $\overline{FAULT}$ pin is released.

LTC3870 has internal thermal shutdown protection which pulls all TG and BG pins low when the junction temperature

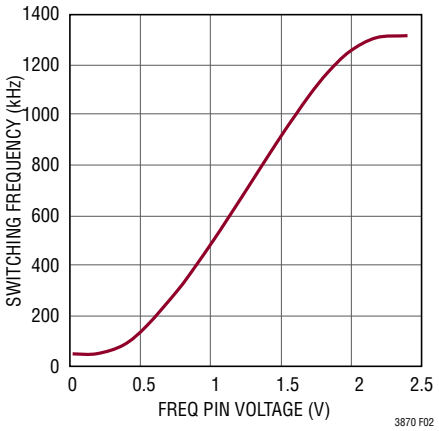

Figure 3. Relationship Between Oscillator Frequency and Voltage at the FREQ Pin

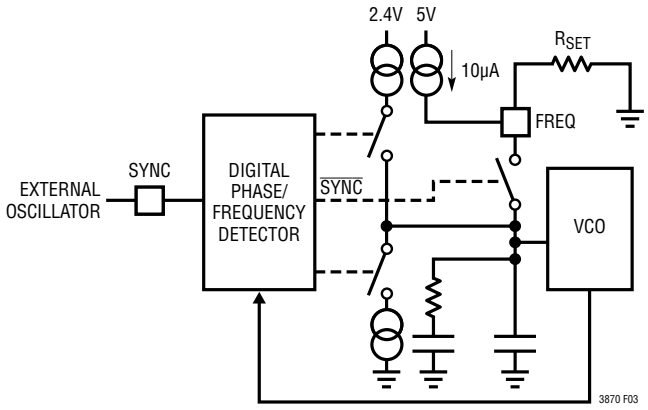

Figure 4. Phase-Locked Loop Block Diagram

is higher than 160°C. In thermal shutdown, $\overline{FAULT0}$ and $\overline{FAULT1}$ pins are also pulled low. There is a 500k pull down resistor on each $\overline{FAULT}$ pin which sets the default voltage on Fault pins low if $\overline{FAULT}$ pins are floating.

Transient Response and Loop Stability

In a typical parallel operation, LTC3870 cooperates with master controllers to supply more current. To achieve balanced current sharing between master and slave, it is recommended that each slave channel copy the design from the master channel. Select same inductors, same power MOSFETs, same current sensing circuit and same output capacitors between the master channel and slave channels. Control loop and compensation design on the I_{TH} pin should start with the single phase operation of the

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master controller. If the master and slave channels are exactly the same, then the transient response and loop stability of the multiphase design is almost the same as the single phase operation of the master by tying the I_{TH} pins together between the master and slaves. For example, design the compensation for a single phase 1.8V/20A output using LTC3880 with a 0.56µH inductor and 530µF output capacitors. To extend the output to 1.8V/40A, simply parallel one channel of LTC3870 with the same inductor and output capacitors (total output capacitors are 1060µF) and tie the I_{TH} pin of LTC3870 to the master I_{TH}. The loop stability and transient responses of the two phase converter are very similar to the single phase design without any extra compensator on the I_{TH} pin of LTC3870 slave controller. Furthermore, LTpowerCAD is provided on the LTC website as a free download for transient and stability analysis.

To minimize the high frequency noise on the I_{TH} trace between master and slave I_{TH} pins, a small filter capacitor in the range of tens of pF can be placed closely at each I_{TH} pin of the slave controller. This small capacitor normally does not significantly affect the closed loop bandwidth but increases the gain margin at high frequency.

Mode Selection and Pre-Biased Startup

There may be situations that require the power supply to start up with a pre-bias on the output capacitors. In this case, it is desirable to start up without discharging the output capacitors. The LTC3870 can be configured to DCM mode for pre-biased start-up. If PGOOD signal is available on the master controller (e.g. LTC3883), the PGOOD pin can be connected to MODE pins of LTC3870 to ensure DCM operation at startup and CCM operation at steady state.

Minimum On-Time Considerations

Minimum on-time $t_{ON(MIN)}$ is the smallest time duration that the LTC3870 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < T_{SW}\ V_{OUT}/V_{IN}$$

where T_{SW} is the switching period.

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the ripple voltage and current will increase. The minimum on-time for the LTC3870 is approximately 90ns, with reasonably good PCB layout, minimum 30% inductor current ripple and at least 10mV ripple on the current sense signal. The minimum on-time can be affected by PCB switching noise in the current loop. As the peak sense voltage decreases, the minimum on-time gradually increases to 130ns. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC. These items are also illustrated graphically in the layout diagram of Figure 5. Figure 6 illustrates the current waveforms present in the various branches of the 2-phase synchronous regulators operating in the continuous mode. Check the following in the PC layout:

1. Are the top N-channel MOSFETs M1 and M3 located within 1cm of each other with a common drain connection at C_{IN}? Do not attempt to split the input bypassing for the two channels as it can cause a large resonant loop.
2. Are the signal and power grounds kept separate? The combined IC signal ground pin and the ground return of C_{INTVCC} must return to the combined C_{OUT} (–) terminals. The I_{TH} traces should be as short as possible. The path formed by the top N-channel MOSFET, Schottky diode and the C_{IN} capacitor should have short leads and PC trace lengths. The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor by placing the capacitors next to each other and away from the Schottky loop described above.
3. Are the I_{SENSE}^+ and I_{SENSE}^- leads routed together with minimum PC trace spacing? The filter capacitor between I_{SENSE}^+ and I_{SENSE}^- should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the sense resistor or inductor, whichever is used for current sensing.

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4. Is the $INTV_{CC}$ bypassing capacitor connected close to the IC, between the $INTV_{CC}$ and the power ground pins? This capacitor carries the MOSFET drivers current peaks. An additional 1µF ceramic capacitor placed immediately next to the $INTV_{CC}$ and PGND pins can help improve noise performance substantially.
5. Keep the switching nodes (SW1, SW0), top gate nodes (TG1, TG0), and boost nodes (BOOST1, BOOST0) away from sensitive small-signal nodes, especially from the opposite channel's current sensing feedback pins. All of these nodes have very large and fast moving signals and therefore should be kept on the "output side" of the LTC3870 and occupy minimum PC trace area. If DCR sensing is used, place the right resistor (Block Diagram, "R_C") close to the switching node.
6. Use a modified "star ground" technique: a low impedance, large copper area central grounding point on the same side of the PC board as the input and output capacitors with tie-ins for the bottom of the $INTV_{CC}$ bypassing capacitor, the bottom of the voltage feedback resistive divider and the SGND pin of the IC.

PC Board Layout Debugging

Start with one controller at a time. It is helpful to use a DC-50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (SW pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation should be maintained over the input voltage range down to dropout and until the output load drops below the low current operation threshold—typically 10% of the maximum designed current level in Burst Mode operation.

The duty cycle percentage should be maintained from cycle to cycle in a well-designed, low noise PCB implementation. Variation in the duty cycle at a sub-harmonic rate can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame a poor PC layout if regulator bandwidth optimization is not required. Only after each controller is checked for its individual performance should both controllers be turned on at the same time. A particularly difficult region of operation is when one controller channel is nearing its current comparator trip point when the other channel is turning on its top MOSFET. This occurs around 50% duty cycle on either channel due to the phasing of the internal clocks and may cause minor duty cycle jitter.

Reduce V_{IN} from its nominal level to verify operation of the regulator in dropout. Check the operation of the undervoltage lockout circuit by further lowering V_{IN} while monitoring the outputs to verify operation.

Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, TG, and possibly BG connections and the sensitive voltage and current pins. The capacitor placed across the current sensing pins needs to be placed immediately adjacent to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling. If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between C_{IN}, Schottky and the top MOSFET components to the sensitive current and voltage sensing traces. In addition, investigate common ground path voltage pickup between these components and the SGND pin of the IC.

Design Example

As a design example using master chip LTC3880 and slave chip LTC3870 for a 4-phase high current regulator, assume V_{IN} = 12V (nominal), V_{IN} = 15V (maximum), V_{OUT} = 1.0V, I_{MAX} = 100A, and f = 425kHz (see Typical Applications).

The master chip LTC3880 design can be found in the LTC3880 data sheet Design Example section.

LTC3880's SYNC pin is connected to LTC3870's SYNC pin and LTC3870's PHASMD is connected to LTC3870's $INTV_{CC}$.

Slave chip LTC3870 should use the same inductor, power MOSFET, C_{IN}, and C_{OUT} as the master chip. DCR sensing is also used for the slave chip.

LTC3870's I_{LIM} pin is forced to 0V to match the master chip's 50mV current limit. Both chips' V_{IN}, V_{OUT}, RUN, I_{TH} pins are connected together. LTC3880's $\overline{GPIO}$ pins are connected to LTC3870's $\overline{FAULT}$ pins so the slave controller will be disabled during fault conditions.

APPLICATIONS INFORMATION

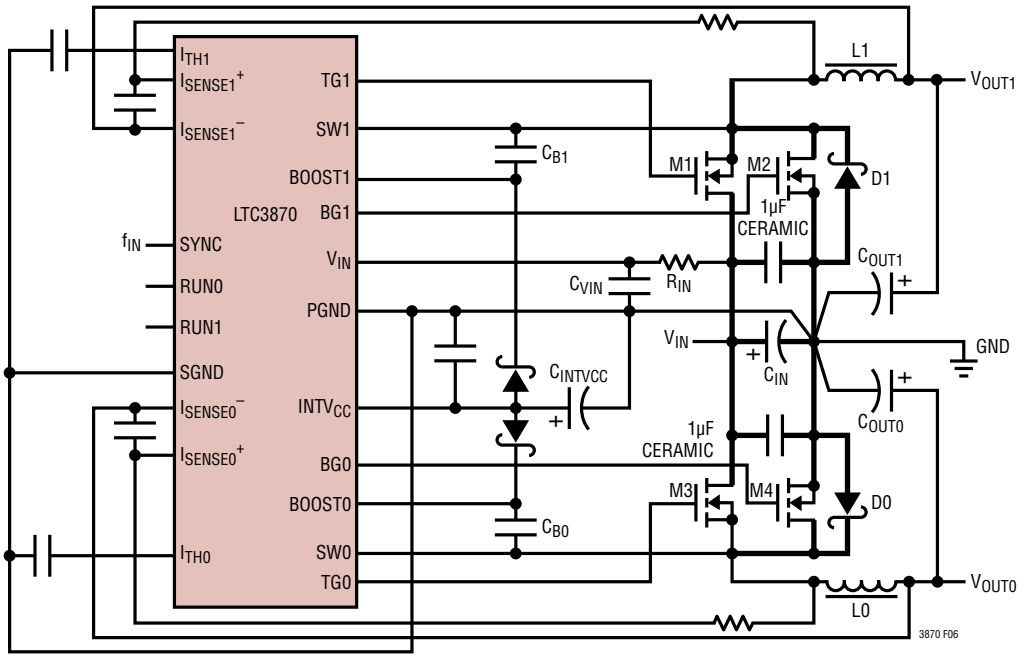


Figure 5. Recommended Printed Circuit Layout Diagram

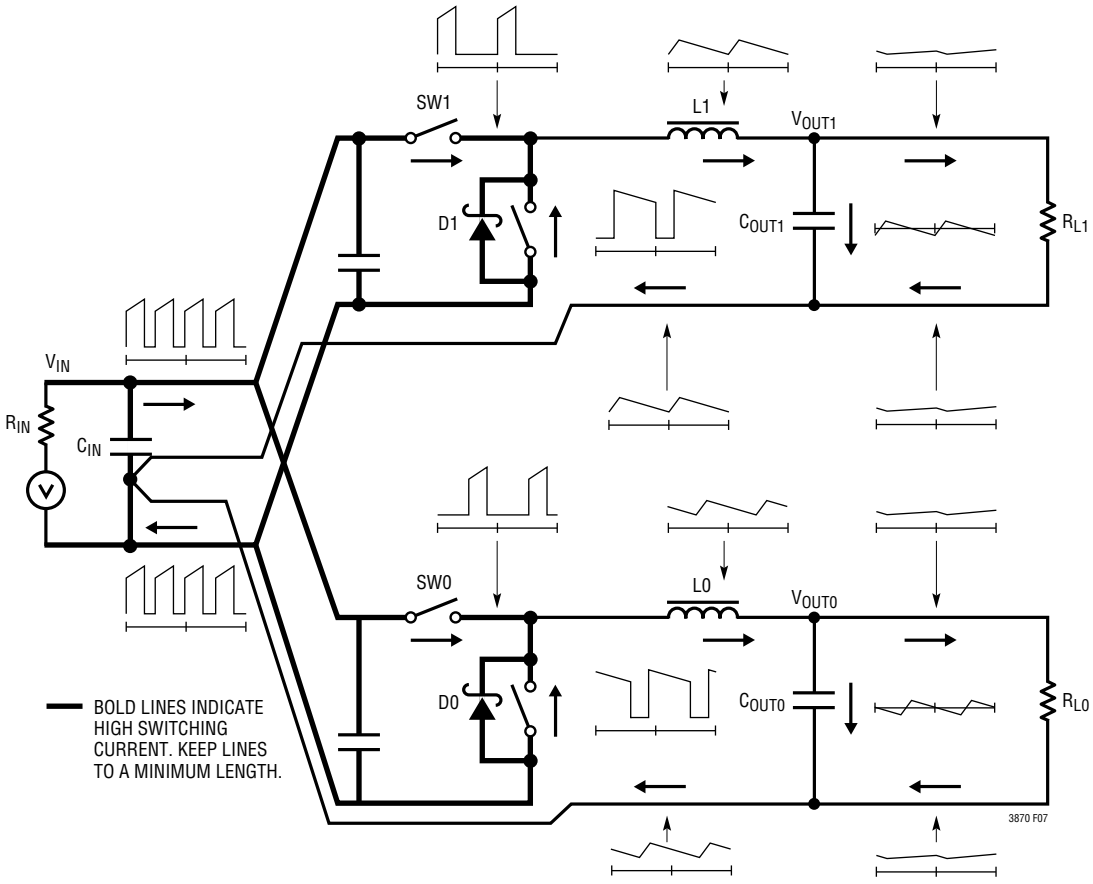
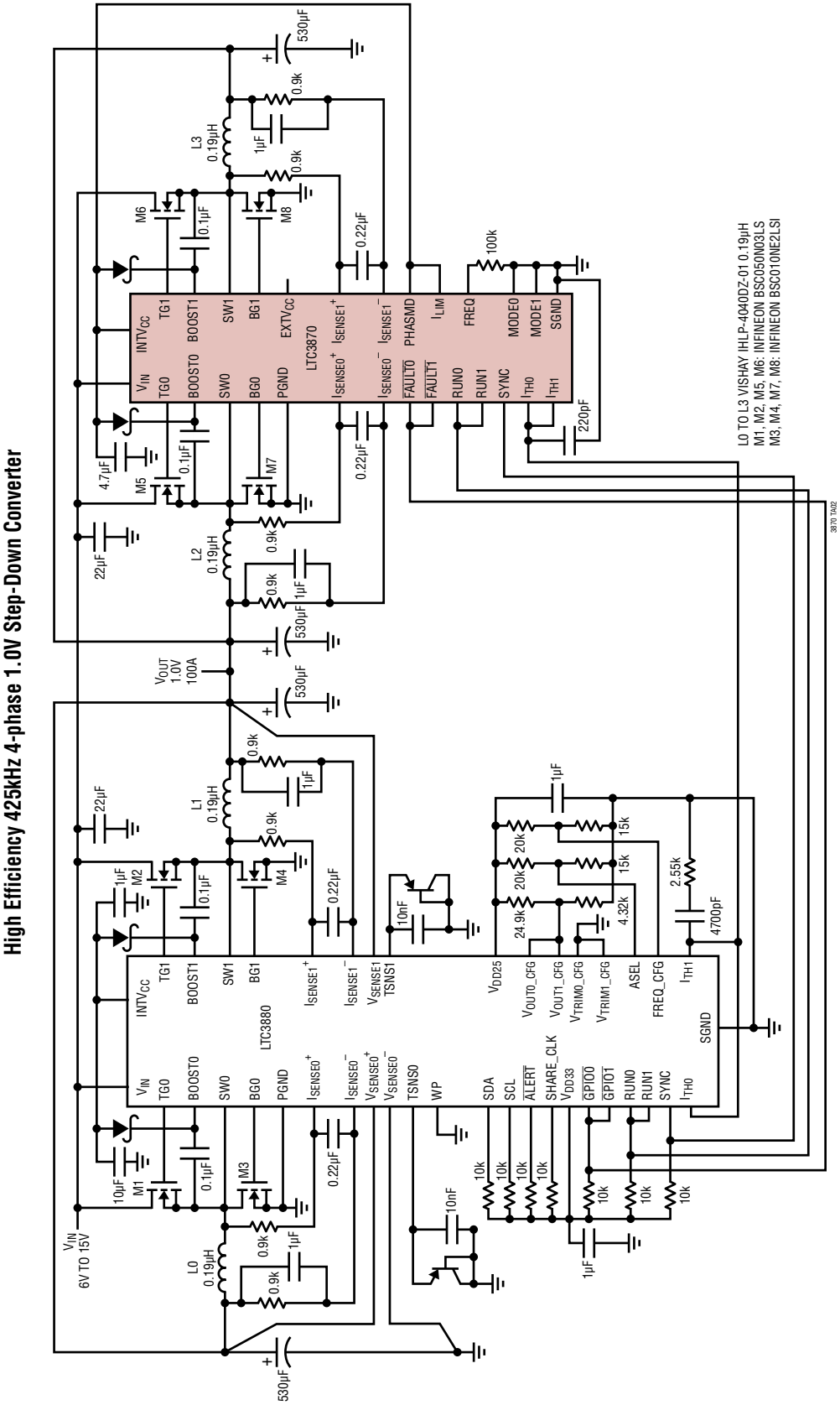


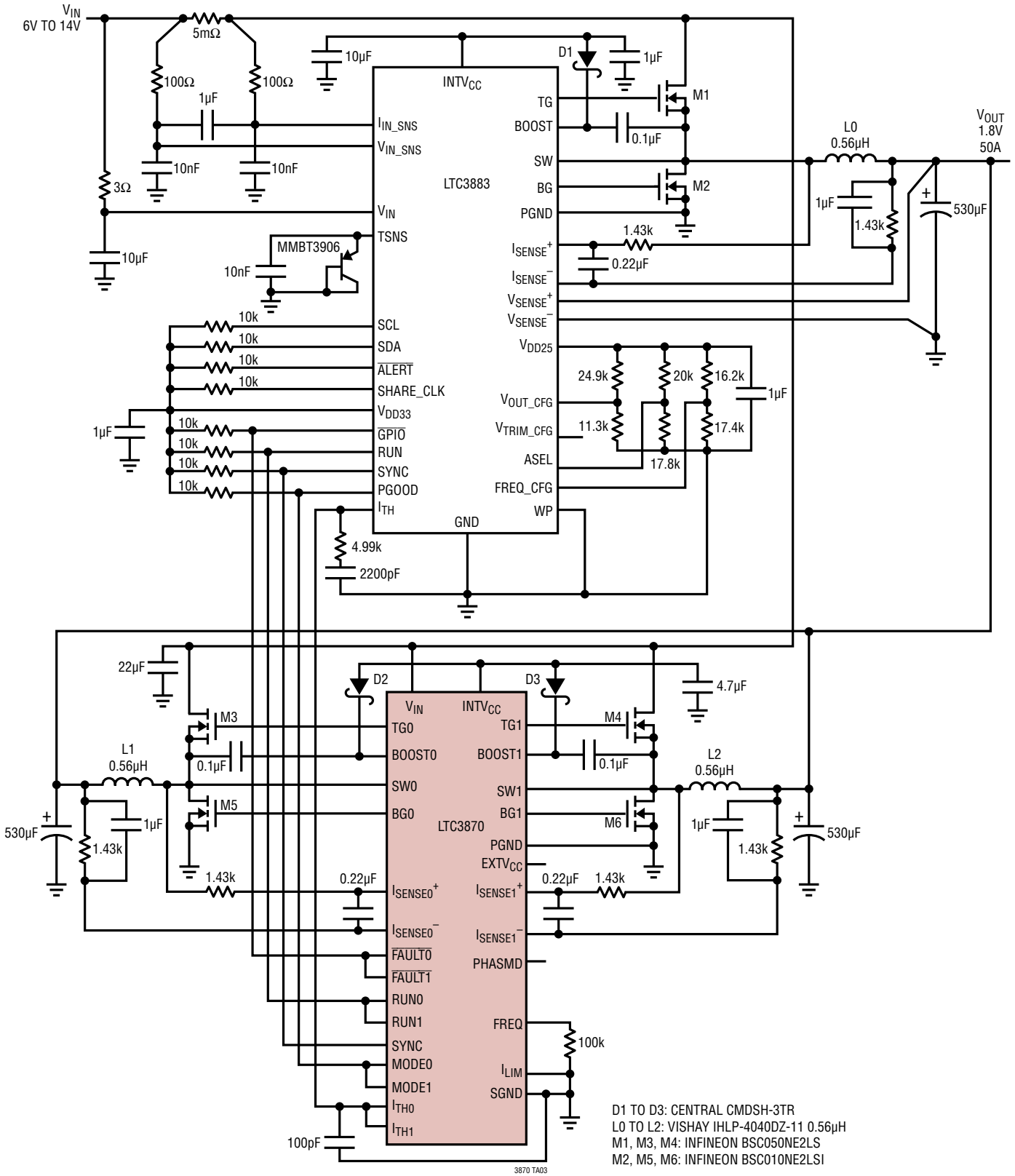
Figure 6. Branch Current Waveforms

TYPICAL APPLICATIONS



TYPICAL APPLICATIONS

High Efficiency 425kHz 3-phase 1.8V Step-Down Converter with Input Current Sensing

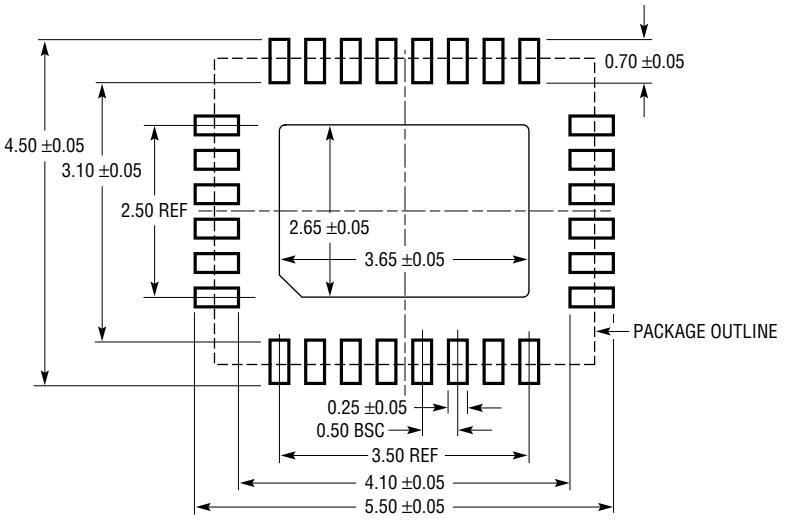


D1 TO D3: CENTRAL CMDSH-3TR
L0 TO L2: VISHAY IHLP-4040DZ-11 0.56µH
M1, M3, M4: INFINEON BSC050NE2LS
M2, M5, M6: INFINEON BSC010NE2LSI

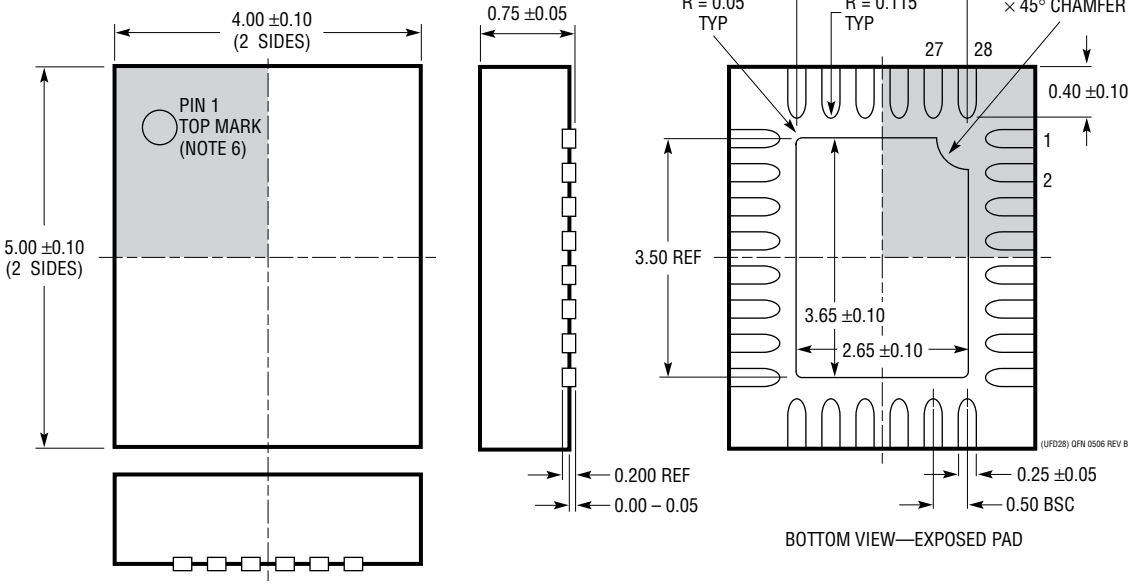
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

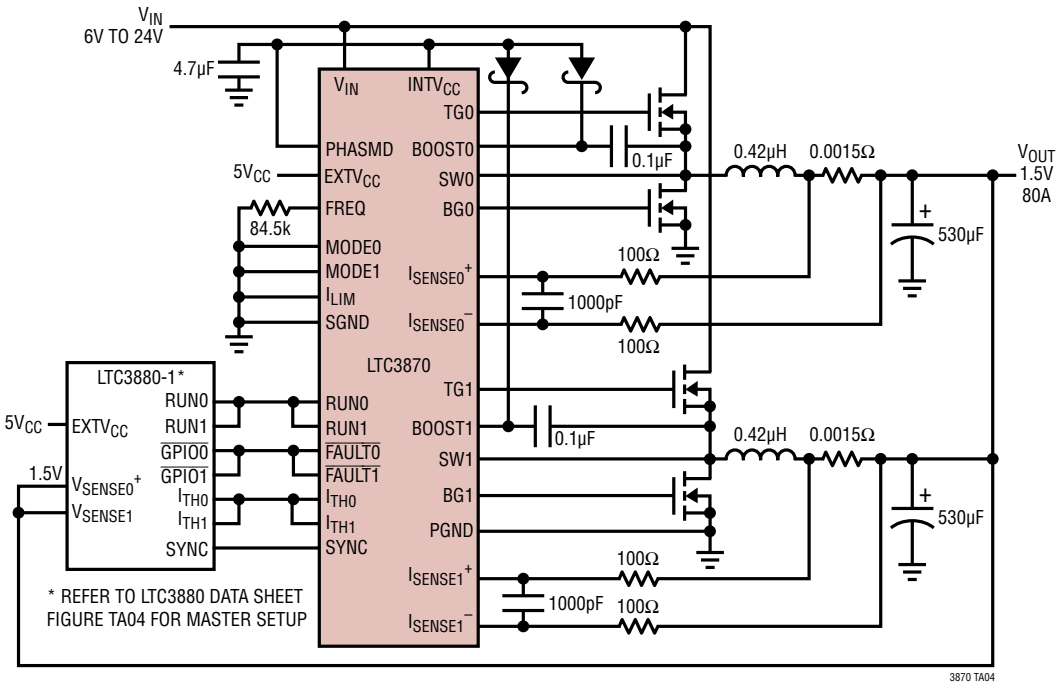
NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	8/14	Added Note 9	2
		Miscellaneous typographical changes	1, 3, 8, 13, 16
B	7/15	Changed title and added master parts supported	1

TYPICAL APPLICATION

4-Phase 1.5V Step-Down Converter with Sensing Resistors and External V_{CC}



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3886	60V Dual Output Step-Down Controller with Digital Power System Management	4.5V ≤ V_{IN} ≤ 60V, 0.5V ≤ V_{OUT} ≤ 13.8V, Programmable Loop Compensation, Input Current Sense
LTM4676/ LTM4676A	Dual 13A or Single 26A Step-Down DC/DC µModule Regulator with Digital Power System Management	4.5V ≤ V_{IN} ≤ 17V/26.5V, 0.5V ≤ V_{OUT} ≤ 4V/5.5V, ±1% V_{OUT} Accuracy, Fault Logging, I^2C/PMBus Interface, 16mm × 16mm × 5mm, BGA Package
LTC3887/ LTC3887-1	Dual Output Multiphase Step-Down DC/DC Controller with Digital Power System Management, 70ms Start-Up	4.5V ≤ V_{IN} ≤ 24V, 0.5V ≤ V_{OUT} ≤ 5.5V, 70mS Start-Up, Analog Control Loop, I^2C/PMBus Interface, -1 Version Drives DrMOS and Power Blocks
LTC3880/ LTC3880-1	Dual Output Multiphase Step-Down DC/DC Controller with Digital Power System Management	4.5V ≤ V_{IN} ≤ 24V, 0.5V ≤ V_{OUT0} ≤ 5.4V, Analog Control Loop, I^2C/PMBus Interface with EEPROM and 16-Bit ADC
LTC3883/ LTC3883-1	Single Phase Step-Down DC/DC Controller with Digital Power System Management	V_{IN} Up to 24V, 0.5V ≤ V_{OUT} ≤ 5.5V, Input Current Sense Amplifier, I^2C/PMBus Interface with EEPROM and 16-Bit ADC
LTC3882	Dual Output Multiphase Step-Down DC/DC Voltage Mode Controller with Digital Power System Management	V_{IN} Up to 38V, 0.5V ≤ $V_{OUT1,2}$ ≤ 5.25V, ±0.5% V_{OUT} Accuracy I^2C/PMBus Interface, Drives DrMOS and Power Blocks
LTC3892-1	60V Low I_Q Dual, 2-Phase Synchronous Step-Down DC/DC Controller	V_{IN} Up to 60V, 0.8V ≤ V_{OUT} ≤ 99%•V_{IN}, 29µA Quiescent Current Adjustable Gate Drive Voltage
LTC2977	8-Channel PMBus Power System Manager Featuring Accurate Output Voltage Measurement	Sequence and Supervise Eight Power Supplies Margin or Trim Supplies to 0.25% Accuracy

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