THE DATASHEET OF

LTC3873EDDB-5#TRPBF

No R_{SENSE}™ Constant Frequency Current Mode Boost/Flyback/SEPIC DC/DC Controller

FEATURES

- **V_{IN} and V_{OUT} Limited Only by External Components**
- **Internal or Programmable External Soft-Start**
- **Constant Frequency 200kHz Operation**
- **Adjustable Current Limit**
- **Current Sense Resistor Optional**
- ±1.5% Voltage Reference Accuracy
- Current Mode Operation for Excellent Line and Load Transient Response
- 4.1V Undervoltage Threshold for Logic Level MOSFET Applications
- Low Quiescent Current: 300µA
- Low Profile (1mm) ThinSOT™ and (0.75mm) 2mm × 3mm DFN Package

APPLICATIONS

- Telecom Power Supplies
- Automotive Power Supplies
- PoE Applications

DESCRIPTION

The LTC®3873-5 is a constant frequency current mode controller for boost, flyback or SEPIC DC/DC converters designed to drive an N-channel MOSFET for high input and output voltage converter applications.

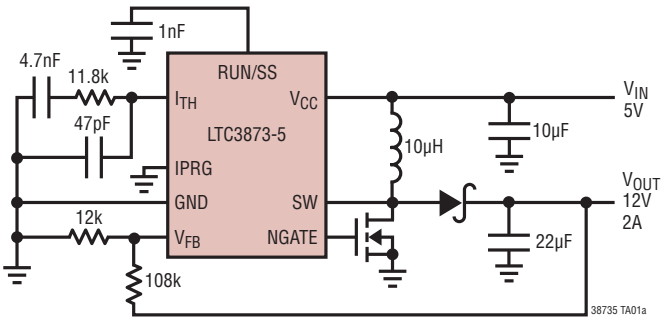
The LTC3873-5 provides ±1.5% output voltage accuracy and consumes only 300µA quiescent current during normal operation and only 50µA during micropower start-up. Using a 9.3V internal shunt regulator, the LTC3873-5 can be powered from a high input voltage through a resistor or it can be powered directly from a low impedance DC voltage of 9V or less. Soft-start can be programmed using an external capacitor.

The LTC3873-5 is available in 8-lead ThinSOT and 2mm × 3mm DFN packages.

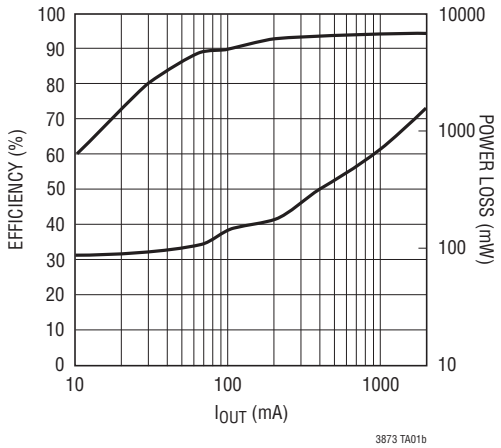
PARAMETER	LTC3873	LTC3873-5
V_{CC} UV^+	8.4V	4.1V
V_{CC} UV^-	4V	2.9V

TYPICAL APPLICATION

High Efficiency 5V Input, 12V Output Boost Converter



Efficiency and Power Loss vs Load Current



ABSOLUTE MAXIMUM RATINGS (Note 1)

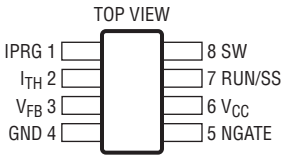
V_{CC} to GND
- Low Impedance Source ..... –0.3V to 9V
- Current Fed ..... 25mA Into V_{CC}

RUN/SS ..... –0.3V to 9V
IPRG Voltage ..... –0.3V to (V_{CC} + 0.3V)
V_{FB}, I_{TH} Voltages ..... –0.3V to 2.4V
SW Voltage ..... –0.3V to 60V

Operating Temperature Range (Note 2)
- LTC3873E-5 ..... –40°C to 85°C
- LTC3873I-5 ..... –40°C to 125°C

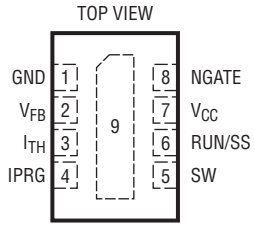
Junction Temperature (Note 3) ..... 125°C
Storage Temperature Range ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec)
- TS8 Package ..... 300°C

PIN CONFIGURATION



TS8 PACKAGE
8-LEAD PLASTIC TSOT-23

T_{JMAX} = 125°C, θ_{JA} = 230°C/W



DDB PACKAGE
8-LEAD (3mm × 2mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 76°C/W
EXPOSED PAD (PIN 9) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3873ETS8-5#PBF	LTC3873ETS8-5#TRPBF	LTCSP	8-Lead Plastic TSOT-23	–40°C to 85°C
LTC3873ITS8-5#PBF	LTC3873ITS8-5#TRPBF	LTCSP	8-Lead Plastic TSOT-23	–40°C to 125°C
LTC3873EDDB-5#PBF	LTC3873EDDB-5#TRPBF	LCSM	8-Lead (3mm × 2mm) Plastic DFN	–40°C to 85°C
LTC3873IDDB-5#PBF	LTC3873IDDB-5#TRPBF	LCSM	8-Lead (3mm × 2mm) Plastic DFN	–40°C to 125°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC3873ETS8-5	LTC3873ETS8-5#TR	LTCSP	8-Lead Plastic TSOT-23	–40°C to 85°C
LTC3873ITS8-5	LTC3873ITS8-5#TR	LTCSP	8-Lead Plastic TSOT-23	–40°C to 125°C
LTC3873EDDB-5	LTC3873EDDB-5#TR	LCSM	8-Lead (3mm × 2mm) Plastic DFN	–40°C to 85°C
LTC3873IDDB-5	LTC3873IDDB-5#TR	LCSM	8-Lead (3mm × 2mm) Plastic DFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input DC Supply Current Normal Operation Shutdown UVLO	Typicals at V_{CC} = 5V (Note 4) V_{ITH} = 1.9V $V_{RUN/SS}$ = 0V V_{CC} = UVLO Threshold – 100mV, $V_{RUN/SS}$ = V_{CC}			 300 50 35	 400 80 50	 µA µA µA
Undervoltage Lockout Threshold	V_{CC} Rising V_{CC} Falling V_{CC} Hysteresis	● ● ●	3.8 2.5 0.9	4.1 2.9 1.25	4.4 3.3 1.7	V V V
Shutdown Threshold (at RUN/SS)	$V_{RUN/SS}$ Falling $V_{RUN/SS}$ Rising	●	0.5 0.6	0.7 0.8	0.9 1.0	V V
Regulated Feedback Voltage	(Note 5)	●	1.182	1.2	1.218	V
Feedback Voltage Line Regulation	3.5V < V_{CC} < 9V (Note 5)			0.1		mV/V
Feedback Voltage Load Regulation	V_{ITH} = 1.6V (Note 5) V_{ITH} = 1V (Note 5)			0.05 –0.05		% %
V_{FB} Input Current	(Note 5)			25	50	nA
RUN/SS Pull Up Current	$V_{RUN/SS}$ = 0V $V_{RUN/SS}$ = 1.3V		1.5 5	3 15	4.5 25	µA µA
Maximum Duty Cycle			70	78	84	%
I_{SLMAX}, Peak Slope Compensation Current				20		µA
Oscillator Frequency			160	200	240	kHz
Gate Drive Rise Time	C_{LOAD} = 3000pF (Note 6)			40		ns
Gate Drive Fall Time	C_{LOAD} = 3000pF (Note 6)			40		ns
Peak Current Sense Voltage	IPRG = GND IPRG = Float IPRG = V_{IN}	● ● ●	95 165 265	110 185 295	125 210 325	mV mV mV
V_{IN} Shunt Regulator Voltage	I_{IN} = 1mA, I_{IN} = 25mA, $V_{RUN/SS}$ = 0V	●	9	9.3	9.6	V
Default Internal Soft-Start				3.3		ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3873E-5 is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3873I-5 is guaranteed to meet performance specifications over the full –40°C to 125°C operating temperature range.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

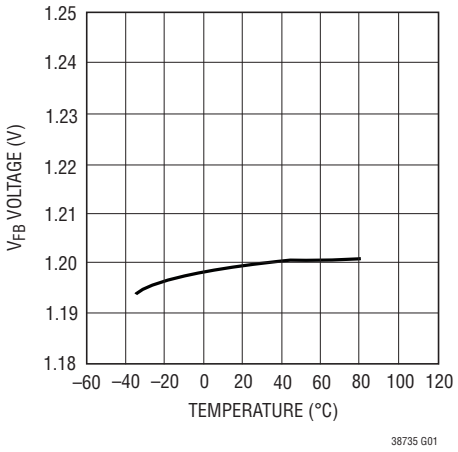
Note 4: The dynamic input supply current is higher due to power MOSFET gate charging ($Q_G \bullet f_{OSC}$). See Applications Information.

Note 5: The LTC3873-5 is tested in a feedback loop which servos V_{FB} to the reference voltage with the I_{TH} pin forced to the midpoint of its voltage range (0.7V ≤ V_{ITH} ≤ 1.9V, midpoint = 1.3V).

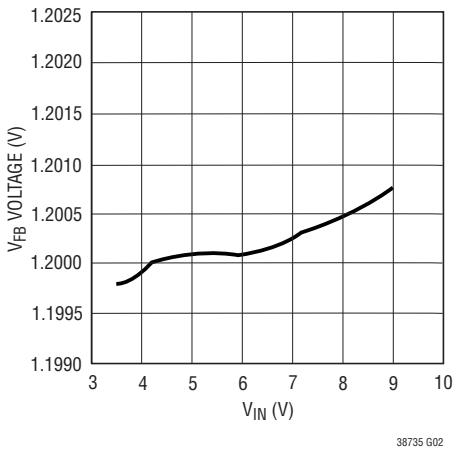
Note 6: Rise and fall times are measured at 10% and 90% levels. V_{CC} = 5.6V.

TYPICAL PERFORMANCE CHARACTERISTICS

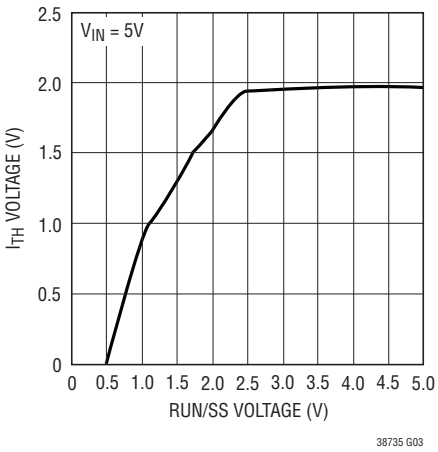
Regulated Feedback Voltage vs Temperature



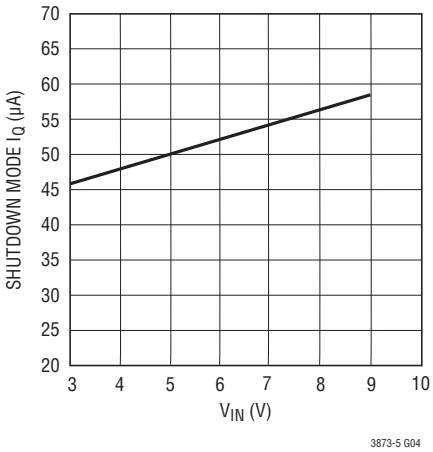
Regulated Feedback Voltage Line Regulation



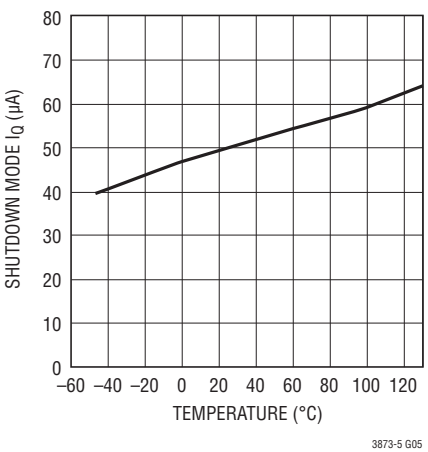
I_{TH} Voltage vs RUN/SS Voltage



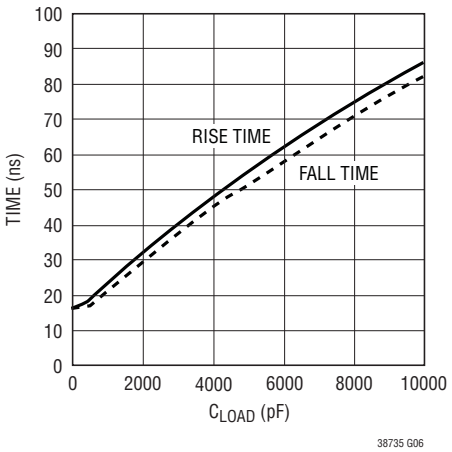
Shutdown Mode I_Q vs V_{IN}



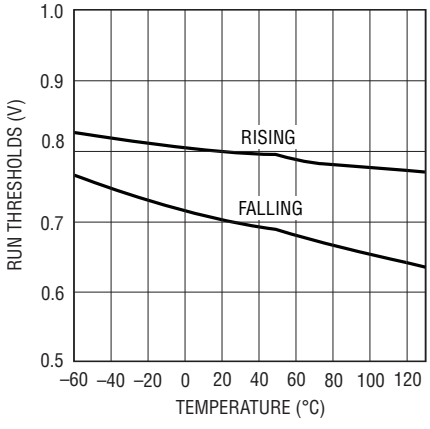
Shutdown I_Q vs Temperature



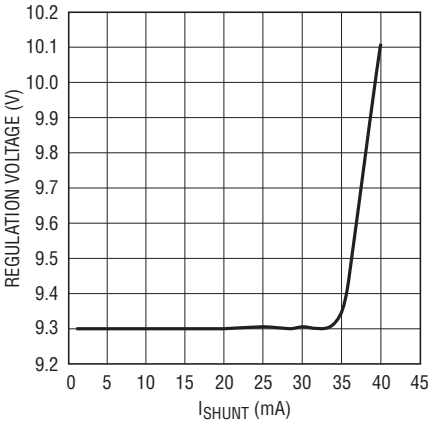
Gate Drive Rise and Fall Time vs C_{LOAD}



RUN Threshold vs Temperature

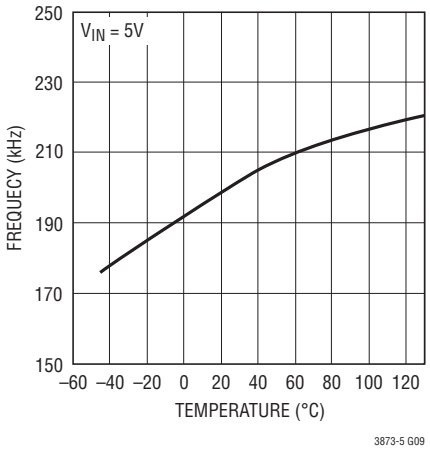


Shunt Regulator Voltage vs I_{SHUNT}

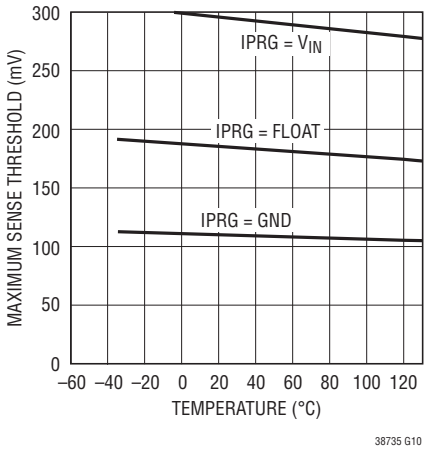


TYPICAL PERFORMANCE CHARACTERISTICS

Frequency vs Temperature



Maximum Sense Threshold vs Temperature



PIN FUNCTIONS (TS8/DD8)

IPRG (Pin 1/Pin 4): Current Sense Limit Select Pin.

I_{TH} (Pin 2/Pin 3): This pin serves as the error amplifier compensation point. Nominal voltage range for this pin is 0.7V to 1.9V.

V_{FB} (Pin 3/Pin 2): This pin receives the feedback voltage from an external resistor divider across the output.

GND (Pin 4/Pin 1): Ground Pin.

NGATE (Pin 5/Pin 8): Gate Drive for the External N-Channel MOSFET. This pin swings from 0V to V_{IN}.

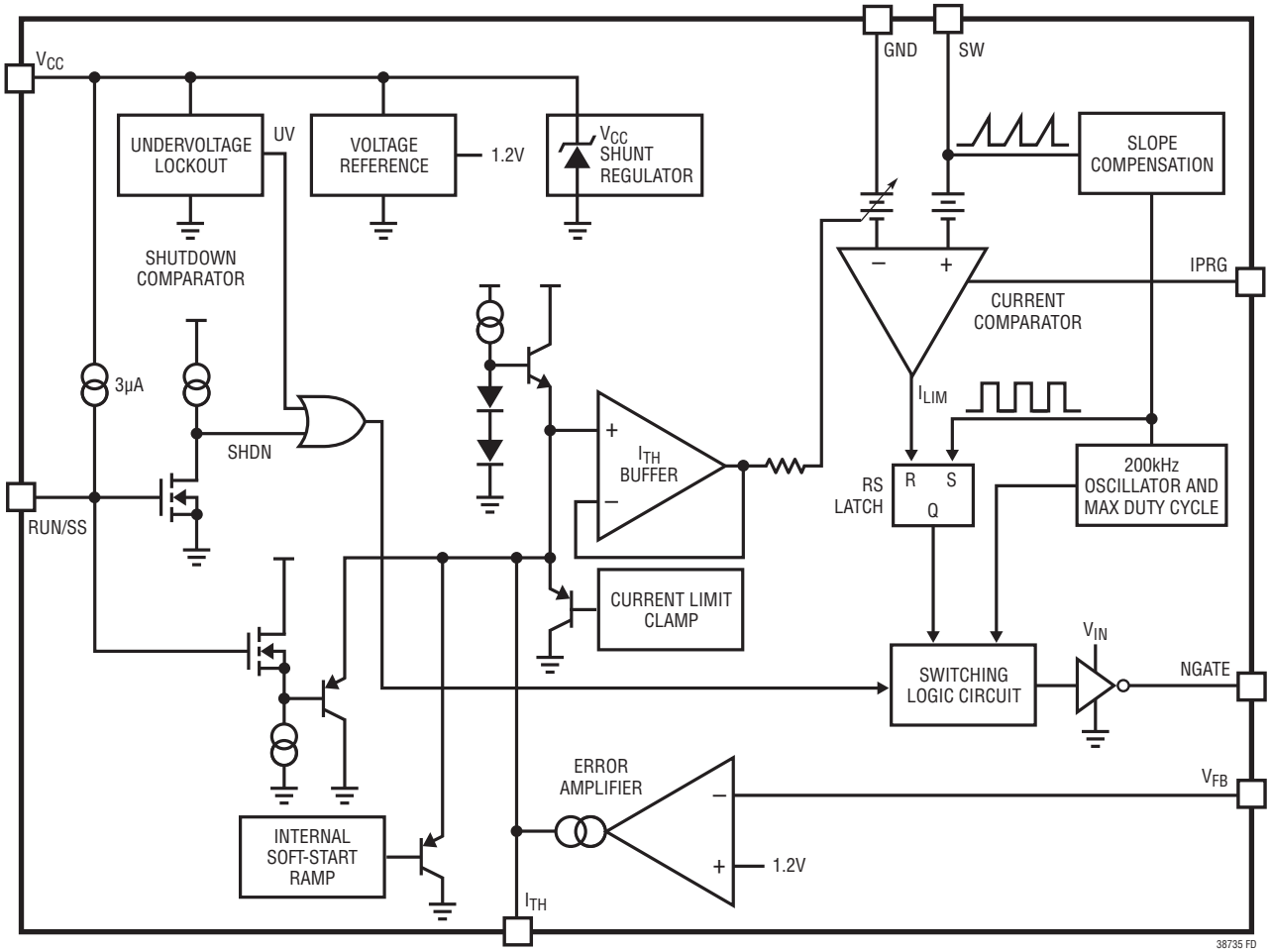
V_{CC} (Pin 6/Pin 7): Supply Pin. This pin must be closely decoupled to GND (Pin 4).

RUN/SS (Pin 7/Pin 6): Shutdown and External Soft-Start Pin. In shutdown, all functions are disabled and the NGATE pin is held low.

SW (Pin 8/Pin 5): Switch node connection to inductor and current sense input pin through external slope compensation resistor. Normally, the external N-channel MOSFET's drain is connected to this pin.

Exposed Pad (NA/Pin 9): Ground. Must be soldered to PCB for electrical contact and rated thermal performance.

FUNCTIONAL DIAGRAM



OPERATION

Main Control Loop

The LTC3873-5 is a general purpose N-channel switching DC/DC converter for boost, flyback and SEPIC applications. Its No R_{SENSE} sensing technique improves efficiency, increases power density and reduces the cost of the overall solution.

For circuit operation, please refer to the Functional Diagram of the IC and the Typical Application on the front page. During normal operation, the power MOSFET is turned on when the oscillator sets the PWM latch and is turned off when the current comparator resets the latch. The divided-down output voltage is compared to an internal 1.2V reference by the error amplifier, which outputs an error signal at the I_{TH} pin. The voltage on the I_{TH} pin sets the current comparator input threshold. When the load current increases, a fall in the V_{FB} voltage relative to the reference voltage causes the I_{TH} pin to rise, causing the current comparator to trip at a higher peak inductor current value. The average inductor current will therefore rise until it equals the load current, thereby maintaining output regulation.

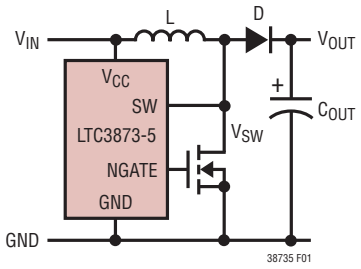


Figure 1. SW Pin (Internal Sense Pin) Connection for Maximum Efficiency

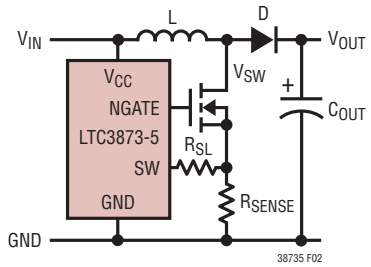


Figure 2. SW Pin (Internal Sense Pin) Connection for Sensing Resistor

The LTC3873-5 can be used either by sensing the voltage drop across the power MOSFET or by connecting the SW pin to a conventional sensing resistor in the source of the power MOSFET. Sensing the voltage across the power MOSFET maximizes converter efficiency and minimizes the component count; the maximum rating for this pin, 60V, allows MOSFET sensing in a wide output voltage range.

Shunt Regulator

A built-in shunt regulator from the V_{CC} pin to GND limits the voltage on the V_{CC} pin to approximately 9.3V as long as the shunt regulator is not forced to sink more than 25mA. The shunt regulator permits the use of a wide variety of powering schemes that exceed the LTC3873-5's absolute maximum ratings. Further details on powering schemes are described in the Application Information section.

Start-Up/Shutdown

The LTC3873-5 has two shutdown mechanisms to disable and enable operation: an undervoltage lockout on the V_{CC} supply pin voltage and a threshold RUN/SS pin. The LTC3873-5 transitions into and out of shutdown according to the state diagram shown in Figure 3.

The undervoltage lockout (UVLO) mechanism prevents the LTC3873-5 from trying to drive a MOSFET with insufficient V_{GS}. The voltage at the V_{CC} pin must exceed

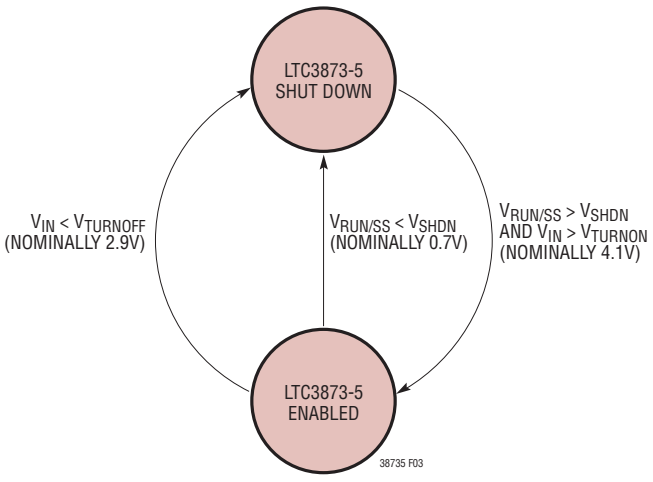


Figure 3. Start-Up/Shut Down State Diagram

OPERATION

V_{TURNON} (nominally 4.1V) at least momentarily to enable LTC3873-5 operation. The V_{CC} voltage is then allowed to fall to $V_{TURNOFF}$ (nominally 2.9V) before undervoltage lockout disables the LTC3873-5. The RUN/SS pin can be driven below V_{SHDN} (nominally 0.7V) to force the LTC3873-5 into shutdown. When the chip is off, the input supply current is typically only 50µA. Keep in mind that V_{CC} should exceed the gate threshold voltage of the switching MOSFET for safe operation.

Soft-Start

Leave the RUN/SS pin open to use the internal 3.3ms soft-start. During the internal soft-start, a voltage ramp limits the V_{ITH}. 3.3ms is required for I_{TH} to ramp from zero current level to full current level. The soft-start can be lengthened by placing an external capacitor from the RUN/SS pin to the GND. A 3µA current will charge the capacitor, pulling the RUN/SS pin above the shutdown threshold and a 15µA pull-up current will continue to ramp RUN/SS to limit V_{ITH} during the start-up. When RUN/SS is driven by an external logic, a minimum of 2.75V logic is recommended to allow the maximum I_{TH} range.

Light Load Operation

Under very light load current conditions, the I_{TH} pin voltage will be very close to 0.85V. As the load current decreases further, an internal offset at the current comparator input will assure that the current comparator remains tripped (even at zero load current) and the regulator will start to skip cycles in order to maintain regulation. This behavior allows the regulator to maintain constant frequency down to very light loads, resulting in low output ripple as well as low audible noise and reduced RF interference while providing high light load efficiency.

Current Sense

During the switch on-time, the control circuit limits the maximum voltage drop across the current sense component to about 295mV, 110mV and 185mV at low duty cycle with IPRG tied to V_{IN}, GND or left floating respectively. It is reduced with increasing duty cycle as shown in Figure 4.

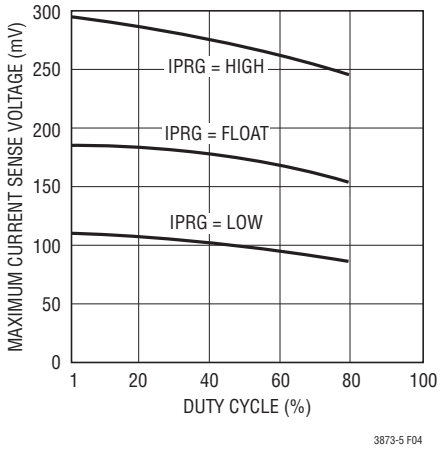


Figure 4. Maximum SENSE Threshold Voltage vs Duty Cycle

APPLICATIONS INFORMATION

V_{CC} Bias Power

The V_{CC} pin must be bypassed to the GND pin with a minimum 10µF ceramic or tantalum capacitor located immediately adjacent to the two pins. Proper supply bypassing is necessary to supply the high transient currents required by the MOSFET gate driver.

For maximum flexibility, the LTC3873-5 is designed so that it can be operated from voltages well beyond the LTC3873-5's absolute maximum ratings. In the simplest case, the LTC3873-5 can be powered with a resistor connected between the input voltage and V_{CC}. The built-in shunt regulator limits the voltage on the V_{CC} pin to around 9.3V as long as the shunt regulator is not forced to sink more than 25mA. This powering scheme has the drawback that the power loss in the resistor reduces converter efficiency and the 25mA shunt regulator maximum may limit the maximum-minimum range of input voltage.

The circuit in Figure 5 shows a second way to power the LTC3873-5. An external series pre-regulator consisting of series pass transistor Q1, zener diode D1 and bias resistor R_B brings V_{CC} to at least 7.6V nominal, well above the undervoltage lockout threshold.

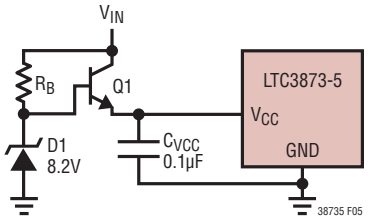


Figure 5. External Pre-Regulator for V_{CC} Bias Power

Slope Compensation

The LTC3873-5 has built-in internal slope compensation to stabilize the control loop against sub-harmonic oscillation. It also provides the ability to externally increase slope compensation by injecting a ramping current out of its SW pin into an external slope compensation resistor (R_{SL} in Figure 2). This current ramp starts at zero right after the NGATE pin has been high. The current rises linearly towards a peak of 20µA at the maximum duty cycle of 80%, shutting off once the NGATE pin goes low. A series resistor (R_{SL}) connecting the SW pin to the current sense resistor (R_{SENSE}) thus develops a ramping voltage drop. From the perspective of the SW pin, this ramping voltage adds to the voltage across the sense resistor, effectively reducing the current comparator threshold in proportion to duty cycle. The amount of reduction in the current comparator threshold (ΔV_{SENSE}) can be calculated using the following equation:

$$\Delta V_{SENSE} = \frac{\text{Duty Cycle} - 6\%}{80\%} 20\mu A \bullet R_{SLOPE}$$

Note the external programmable slope compensation is only needed when the internal slope compensation is not sufficient. In some applications R_{SL} can be shorted. For the LTC3873-5, when the $R_{DS(ON)}$ sensing technique is used, the ringing on the SW pin disrupts the tiny slope compensation current out of the pin. It is not recommended to add external slope compensation in this case.

Output Voltage Programming

The output voltage is set by a resistor divider according to the following formula:

$$V_O = 1.2V \bullet \left(1 + \frac{R2}{R1}\right)$$

The external resistor divider is connected to the output as shown in Figure 4, allowing remote voltage sensing. Choose resistance values for R1 and R2 to be as large as possible in order to minimize any efficiency loss due to the static current drawn from V_{OUT}, but just small enough so that when V_{OUT} is in regulation, the error caused by the nonzero input current to the V_{FB} pin is less than 1%. A good rule of thumb is to choose R1 to be 24k or less.

Transformer Design Considerations

Transformer specification and design is perhaps the most critical part of applying the LTC3873-5 successfully. In addition to the usual list of caveats dealing with high frequency power transformer design, the following should prove useful.

APPLICATIONS INFORMATION

Turns Ratios

Due to the use of the external feedback resistor divider ratio to set output voltage, the user has relative freedom in selecting a transformer turns ratio to suit a given application. Simple ratios of small integers, e.g., 1:1, 2:1, 3:2, etc. can be employed which yield more freedom in setting total turns and mutual inductance. Simple integer turns ratios also facilitate the use of "off-the-shelf" configurable transformers such as the Coiltronics VERSA-PAC series in applications with high input to output voltage ratios. For example, if a 6-winding VERSA-PAC is used with three windings in series on the primary and three windings in parallel on the secondary, a 3:1 turns ratio will be achieved. Turns ratio can be chosen on the basis of desired duty cycle. However, remember that the input supply voltage plus the secondary-to-primary referred version of the flyback pulse (including leakage spike) must not exceed the allowed external MOSFET breakdown rating.

Leakage Inductance

Transformer leakage inductance (on either the primary or secondary) causes a voltage spike to occur after the output switch (Q1) turn-off. This is increasingly prominent at higher load currents where more stored energy must be dissipated. In some cases a "snubber" circuit will be required to avoid overvoltage breakdown at the MOSFET's drain node. Application Note 19 is a good reference on snubber design. A bifilar or similar winding technique is a good way to minimize troublesome leakage inductances. However, remember that this will limit the primary-to-secondary breakdown voltage, so bifilar winding is not always practical.

Power MOSFET Selection

The power MOSFET serves two purposes in the LTC3873-5: it represents the main switching element in the power path and its $R_{DS(ON)}$ represents the current sensing element for the control loop. Important parameters for the power MOSFET include the drain-to-source breakdown voltage (BV_{DSS}), the threshold voltage ($V_{GS(TH)}$), the on-resistance ($R_{DS(ON)}$) versus gate-to-source voltage, the gate-to-source and gate-to-drain charges (Q_{GS} and Q_{GD}, respectively), the maximum drain current ($I_{D(MAX)}$) and the MOSFET's thermal resistances ($R_{TH(JC)}$ and $R_{TH(JA)}$).

Current Limit Programming

During the switch on-time, the control circuit limits the maximum voltage drop across the current sense component to about 270mV, 100mV and 170mV at low duty cycle with IPRG tied to V_{IN}, GND or left floating respectively. For boost applications with $R_{DS(ON)}$ sensing, refer to the LTC3872 data sheet for the selection of MOSFET $R_{DS(ON)}$.

MOSFETs have conduction losses (I^2R) and switching losses. For V_{DS} < 20V, high current efficiency generally improves with large MOSFETs with low $R_{DS(ON)}$, while for V_{DS} > 20V the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower reverse transfer capacitance, C_{RSS}, actually provides higher efficiency.

Output Capacitors

The output capacitor is normally chosen by its effective series resistance (ESR), which determines output ripple voltage and affects efficiency. Low ESR ceramic capacitors are often used to minimize the output ripple. Boost regulators have large RMS ripple current in the output capacitor that must be rated to handle the current. The output ripple current (RMS) is:

$$I_{RMS(COUT)} \approx I_{OUT(MAX)} \bullet \sqrt{\frac{V_{OUT} - V_{IN(MIN)}}{V_{IN(MIN)}}}$$

Output ripple is then simply:

$$V_{OUT} = R_{ESR}(\Delta I_{L(RMS)})$$

The output capacitor for flyback converter should have a ripple current rating greater than:

$$I_{RMS} = I_{OUT} \bullet \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}}$$

APPLICATIONS INFORMATION

Input Capacitors

The input capacitor of a boost converter is less critical due to the fact that the input current waveform is triangular, and does not contain large square wave currents as found in the output capacitor. The input voltage source impedance determines the size of the capacitor that is typically 10µF to 100µF. A low ESR is recommended although not as critical as the output capacitor can be on the order of 0.3Ω.

The RMS input ripple current for a boost converter is:

$$I_{RMS(CIN)} = 0.3 \bullet \frac{V_{IN(MIN)}}{L \bullet f} \bullet D_{MAX}$$

Please note that the input capacitor can see a very high surge current when a battery is suddenly connected to the input of the converter and solid tantalum capacitors can fail catastrophically under these conditions.

In a flyback converter, the input flows in pulses placing severe demands on the input capacitors. Select an input capacitor with a ripple current rating greater than:

$$I_{RMS} = \frac{P_{IN}}{V_{IN(MIN)}} \sqrt{\frac{1-D_{MAX}}{D_{MAX}}}$$

Duty Cycle Considerations

The LTC3873-5 imposes a maximum duty cycle limit of 80% typical. For a flyback converter, the maximum duty cycle prevents the transformer core from saturation. In a boost converter application, however, it sets a limit on the maximum step-up ratio or maximum output voltage with the given input voltage of:

$$V_{OUT(MAX)} = \frac{V_{IN(MIN)}}{1-0.8\%} - V_D$$

Current and voltage stress on the power switch and synchronous rectifiers, input and output capacitor RMS currents and transformer utilization (size vs power) are impacted by duty factor. Unfortunately duty factor cannot be adjusted to simultaneously optimize all of these requirements. In general, avoid extreme duty factors since this severely impacts the current stress on most of the components. A reasonable target for duty factor is 50% at nominal input voltage. Using this rule of thumb, the ideal transformer turns ratio is:

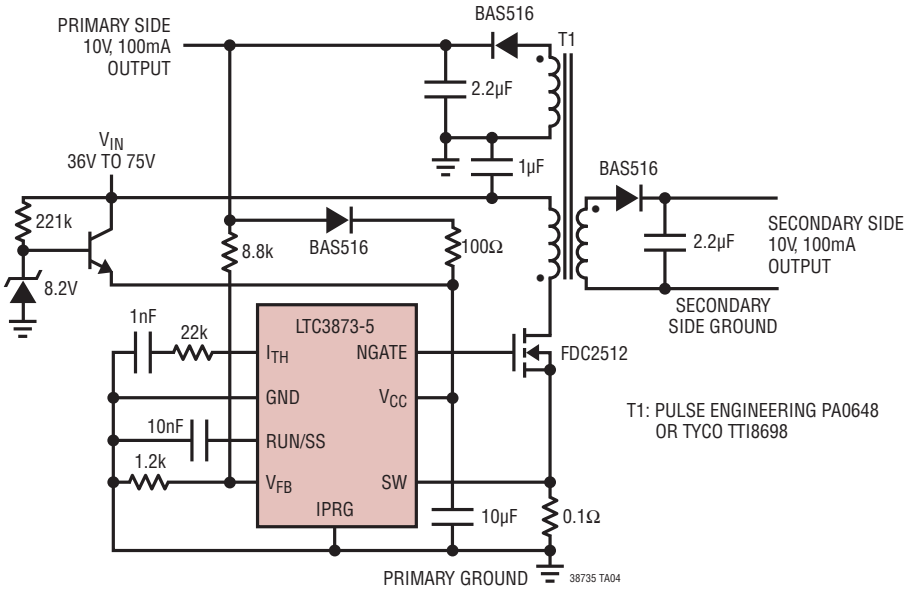
$$N_{IDEAL} = \frac{V_{OUT}}{V_{IN}} \bullet \frac{1-D}{D} = \frac{V_{OUT}}{V_{IN}}$$

Output Diode Selection

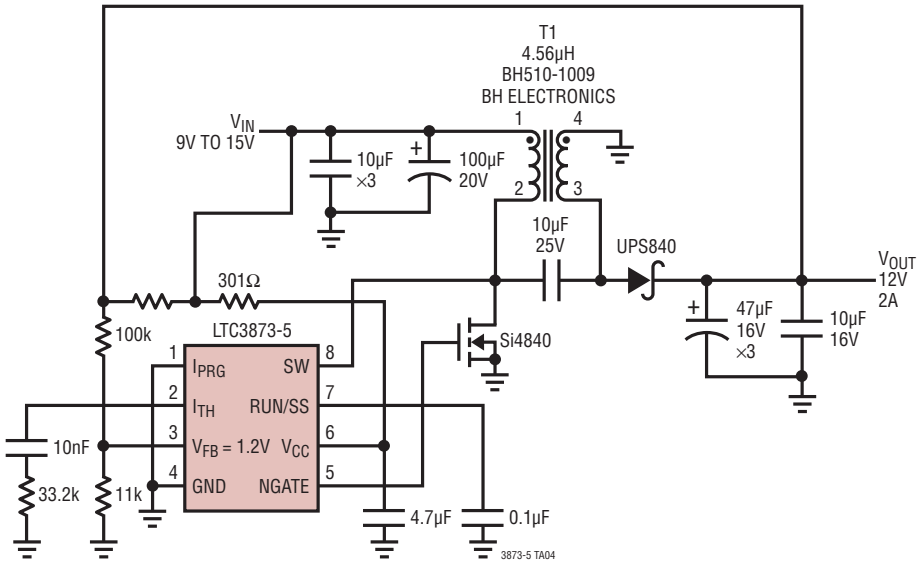
To maximize efficiency, a fast switching diode with low forward drop and low reverse leakage is desired. The output diode in a boost converter conducts current during the switch off-time. The peak reverse voltage that the diode must withstand is equal to the regulator output voltage. The average forward current in normal operation is equal to the output current, and the peak current is equal to the peak inductor current.

TYPICAL APPLICATIONS

1W Isolated Housekeeping Telecom Converter

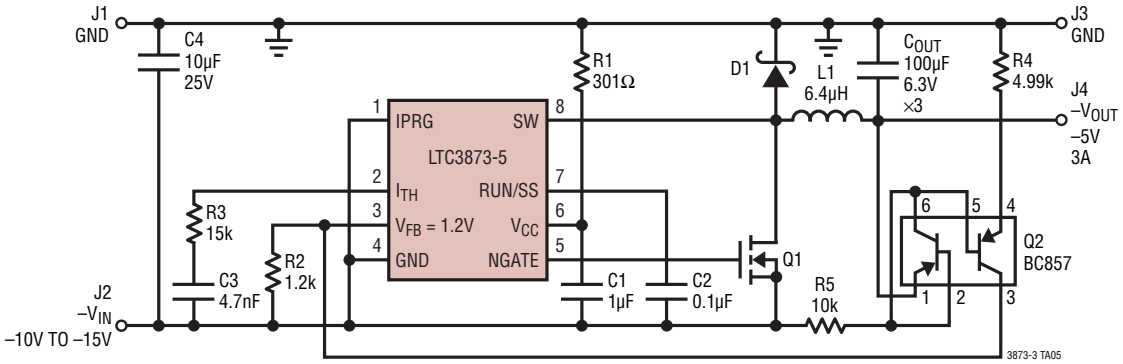


9V to 15V V_{IN}, 12V V_{OUT} SEPIC Converter



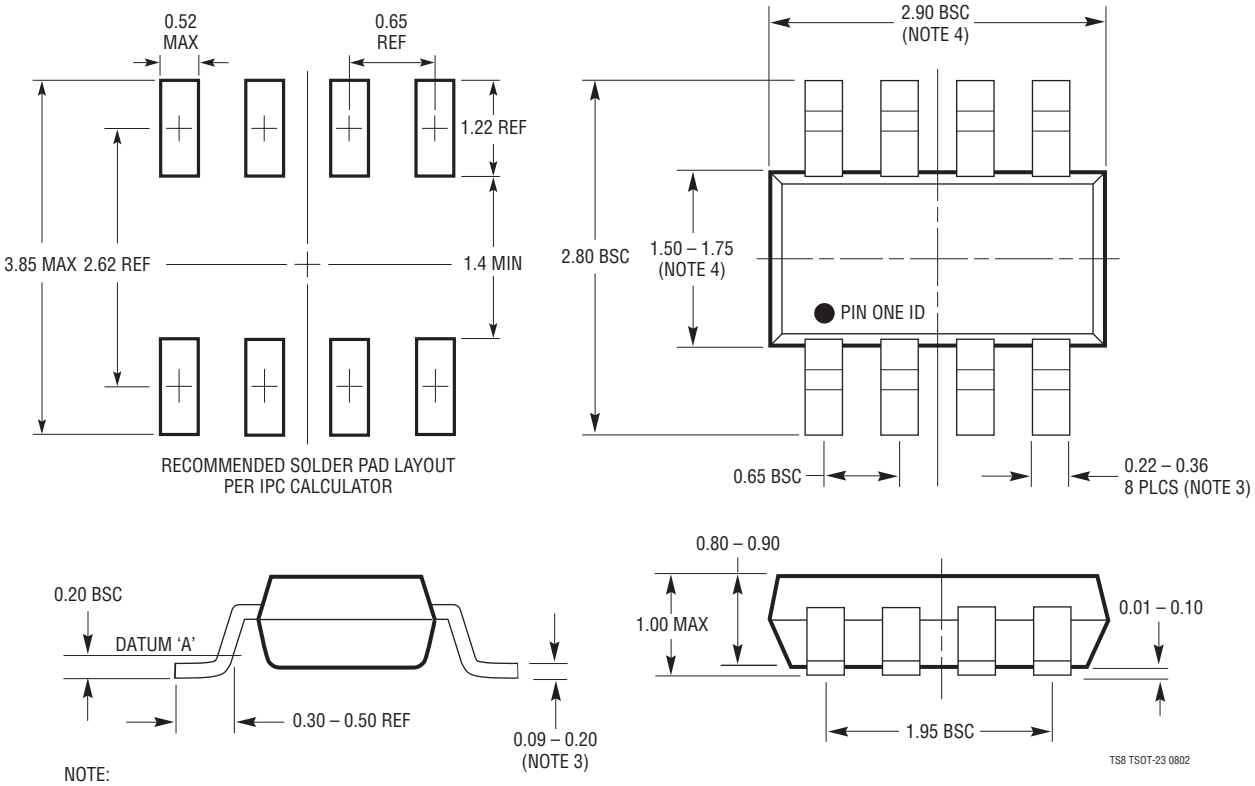
TYPICAL APPLICATIONS

–10V to –15V V_{IN}, –5V V_{OUT} Negative-to-Negative (Negative Buck) Converter



PACKAGE DESCRIPTION

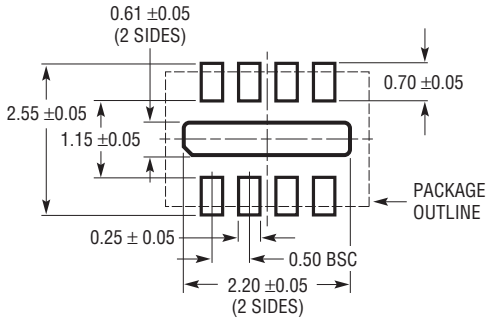
TS8 Package
8-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1637)



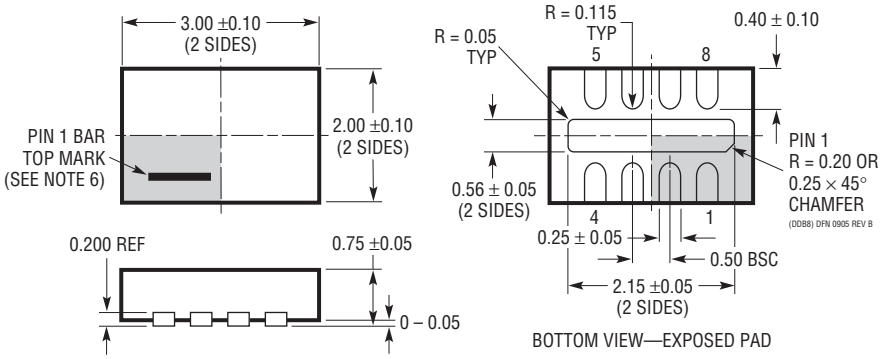
NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

PACKAGE DESCRIPTION

DDB Package
8-Lead Plastic DFN (3mm × 2mm)
(Reference LTC DWG # 05-08-1702 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

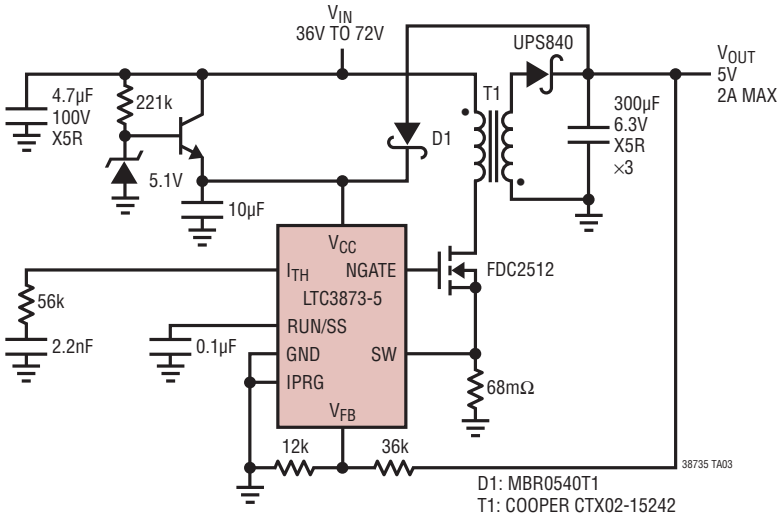


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

5V Output Nonisolated Telecom Housekeeping Power Supply



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT®1619	Current Mode PWM Controller	300kHz Fixed Frequency, Boost, SEPIC, Flyback Topology
LTC1624	Current Mode DC/DC Controller	SO-8; 300kHz Operating Frequency; Buck, Boost, SEPIC Design; V_{IN} Up to 36V
LTC1700	No R_{SENSE} Synchronous Step-Up Controller	Up to 95% Efficiency, Operating as Low as 0.9V Input
LTC1871-7	Wide Input Range Controller	No R_{SENSE}, 7V Gate Drive, Current Mode Control
LTC1872/LTC1872B	SOT-23 Boost Controller	Delievers Up to 5A, 550kHz Fixed Frequency, Current Mode
LT1930	1.2MHz, SOT-23 Boost Converter	Up to 34V Output, 2.6V V_{IN} 16V, Miniature Design
LT1931	Inverting 1.2MHz, SOT-23 Converter	Positive-to Negative DC/DC Conversion, Miniature Design
LTC3401/LTC3402	1A/2A 3MHz Synchronous Boost Converters	Up to 97% Efficiency, Very Small Solution, $0.5V \le V_{IN} \le 5V$
LTC3704	Positive-to Negative DC/DC Controller	No R_{SENSE}, Current Mode Control, 50kHz to 1MHz
LTC1871/LTC1871-7	No R_{SENSE}, Wide Input Range DC/DC Boost Controller	No R_{SENSE}, Current Mode Control, $2.5V \le V_{IN} \le 36V$
LTC3703/LTC3703-5	100V Synchronous Controller	Step-Up or Step Down, 600kHz, SSOP-16, SSOP-28
LTC3803/LTC3803-5	200kHz Flyback DC/DC Controller	V_{IN} and V_{OUT} Limited Only by External Components
LTC3805	Adjustable Frequency Flyback Controller	V_{IN} and V_{OUT} Limited Only by External Components
LT3825	Isolated No-Opto Synchronous Flyback Controller	V_{IN}: 24V to 75V, Up to 80W, Current Mode Control
LT3837	Isolated No-Opto Synchronous Flyback Controller	V_{IN}: 4.5V to 20V, Up to 60W, Current Mode Control
LTC3873	No R_{SENSE} Constant Frequency Boost/Flyback/SEPIC Controller	V_{IN} and V_{OUT} Limited Only by External Components, 200kHz Frequency, ThinSOT or DFN Package

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

LT 0908 REV B • PRINTED IN USA

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View LTC3873EDDB-5#TRPBF on WIN SOURCE
- Analog Devices Inc. Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management