THE DATASHEET OF

MAX14826GTG+

General Description

The MAX14826 transceiver is suitable for IO-Link® devices and 24V binary sensors. All specified IO-Link data rates are supported. In IO-Link applications, the transceiver acts as the physical layer interface to a microcontroller running the data-link layer protocol. Additional 24V digital inputs and outputs are provided. Two internal linear regulators generate common sensor and actuator power requirements: 5V and 3.3V.

On-board C/Q and DO drivers are independently-configurable for push-pull, high-side (PNP), or low-side (NPN) operation. The device detects the IO-Link C/Q wake-up condition and generates a wake-up signal on the active-low $\overline{WU}/\overline{THSD}$ output.

The MAX14826 includes a selectable parallel or SPI interface for configuration and monitoring of the drivers. Extensive alarm conditions are detected and communicated through the interrupt outputs and the SPI interface. The device features reverse-polarity, short-circuit, and thermal protection. All power lines are monitored for undervoltage conditions.

The C/Q and DO drivers are specified for sinking/sourcing 200mA.

The MAX14826 is available in a 4mm x 4mm, 24-pin TQFN package, and is specified over the extended -40°C to +105°C temperature range.

Applications

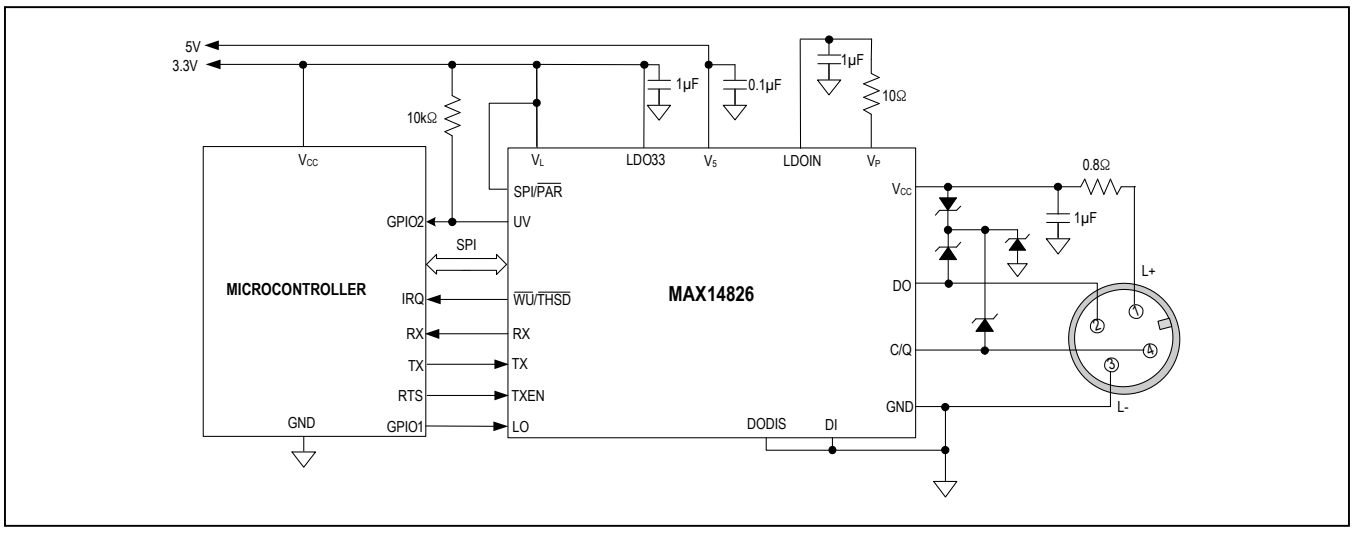
- IO-Link Sensors
- IO-Link Actuators
- Industrial Sensors and Actuators

Benefits and Features

- IO-Link Specification v.1.0 and v.1.1 Physical Layer Compliant
- High Configurability and Integration Reduce SKU's
  - Push-Pull, High-Side, or Low-Side Outputs
  - Supports COM1, COM2, and COM3 Data Rates
  - SPI or Pin-Driven Control and Monitoring
  - 2.5V to 5V Logic Interface Levels
  - C/Q and DO Drivers Can Be Connected in Parallel
  - Auxiliary 24V, 200mA Digital Output (DO)
  - Auxiliary 24V Digital Input (DI)
  - Integrated 5V and 3.3V Linear Regulators
  - Driver Currents Specified for 200mA, 100mA and 50mA
  - 1µF C/Q and DO Load Drive Capability
- Integrated Protection Enables Robust Solutions
  - Extensive Fault-Monitoring and Reporting
  - Reverse-Polarity and Short-Circuit Protection on All 24V Inputs/Outputs
  - Reverse-Polarity Protected 24V Supply Output
  - -40°C to +105°C Operating Temperature Range
- Backwards Pin-and Software-Compatible to MAX14821
- Space-Saving 4mm x 4mm TQFN Package

Ordering Information **appears at end of data sheet.**

Typical Application Circuit



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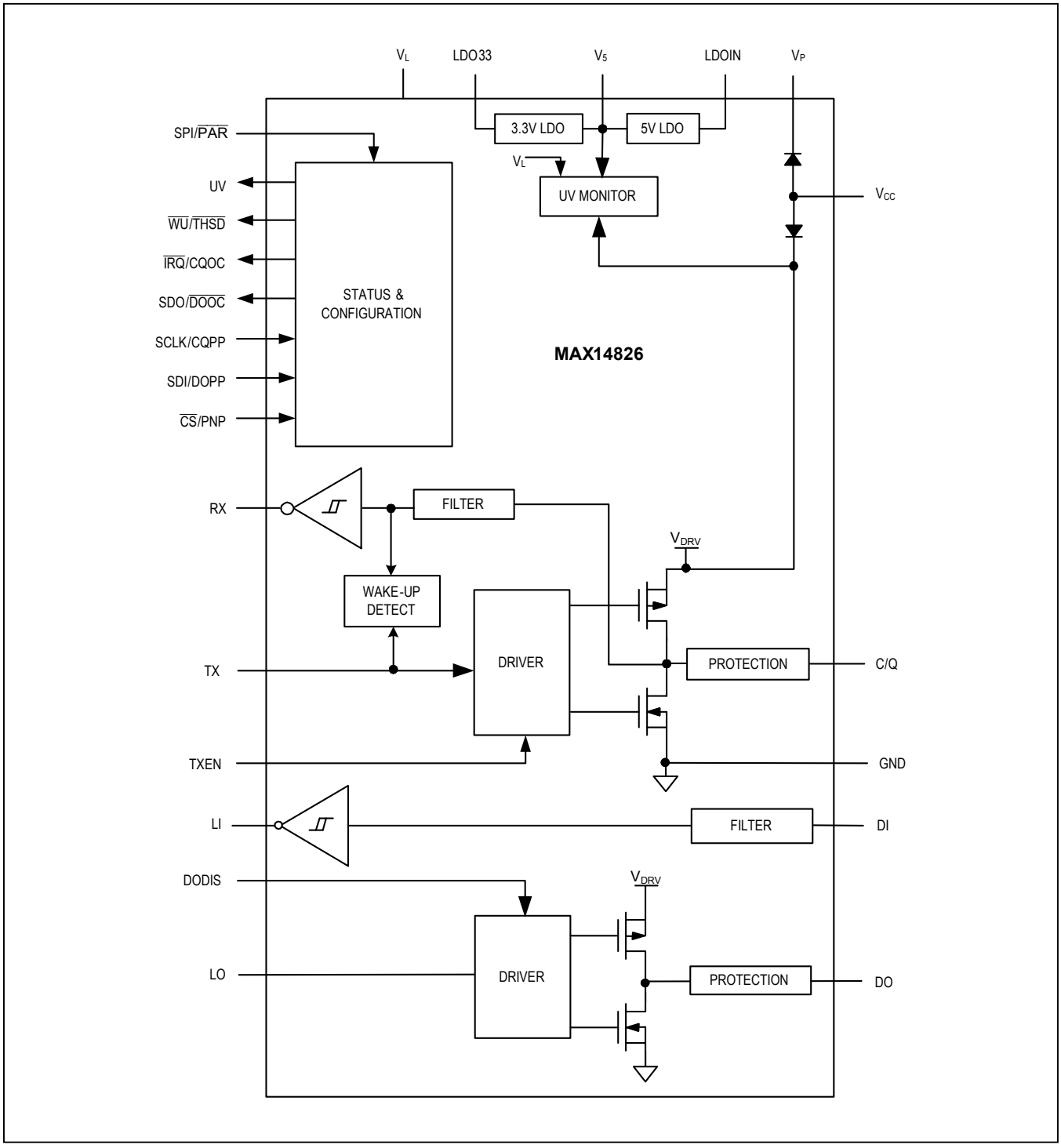
Functional Diagram



Absolute Maximum Ratings

(All voltages referenced to GND, unless otherwise noted.)
V_{CC} ..... -40V to +40V
V_P (I_{VP} < 50mA) ..... the higher of -0.3V and (V_{CC} - 1V) to +40V
LDOIN ..... -0.3V to +40V
V_5 ..... -0.3V to the lesser of (V_{LDOIN} + 0.3V) and +6V
LDO33 ..... -0.3V to the lesser of (V_5 + 0.3V) and +6V
V_L ..... -0.3V to +6V
DI ..... -40V to +40V
C/Q, DO ..... MIN: the higher of -40V and (V_{CC} - 40V)
MAX: the lesser of +40V and (V_{CC} + 40V)
Logic Inputs
TX, TXEN, LO, $\overline{CS}$/PNP, SDI/DOPP, SCLK/CQPP ..... -0.3V to (V_L + 0.3V)
Logic Outputs
RX, $\overline{WU}$/THSD, LI, SDO/$\overline{DOOC}$, $\overline{IRQ}$/$\overline{CQOC}$ ..... -0.3V to (V_L + 0.3V)
UV ..... -0.3V to +6V
Continuous Current Into Any Logic Pin ..... ±50mA
Continuous Power Dissipation
TQFN (derate 27.8mW/°C above +70°C) 2222mW
Operating Temperature Range ..... -40°C to +105°C
Maximum Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 36°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 3°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

(V_{CC} = 18V to 36V, V_L = 2.3V to 5.5V, V_{GND} = 0V; all logic inputs at V_L or GND; T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{CC} = 24V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Supply Voltage	V_{CC}	For driver operation	9		36	V
V_{CC} Supply Current	I_{CC}	V_{CC} = 24V, C/Q as input, no load on V_5 or LDO33, LDOIN not connected to V_P, V_{LDOIN} = 24V		1.2	2.5	mA
V_{CC} Undervoltage Lockout Threshold	V_{CCUVLO}	V_{CC} falling	6	7.4	8.4	V
V_{CC} Undervoltage Lockout Threshold Hysteresis	V_{CCUVLO_HYST}			200		mV
V_5 Supply Current	I_{5_IN}	LDOIN shorted to V_5, external 5V applied to V_5, no switching, LDO33 disabled		3		mA
V_5 Undervoltage Lockout Threshold	V_{5UVLO}	V_5 falling		2.4		V
V_L Logic-Level Supply Voltage	V_L		2.3		5.5	V
V_L Logic-Level Supply Current	I_L	All logic inputs at V_L			5	µA
		All logic inputs at GND			100	µA
V_L Undervoltage Threshold	V_{LUVLO}	V_L falling	0.65	0.95	1.30	V

DC Electrical Characteristics (continued)

(V_{CC} = 18V to 36V, V_L = 2.3V to 5.5V, V_{GND} = 0V; all logic inputs at V_L or GND; T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{CC} = 24V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
5V LDO (V_5)							
LDOIN Input Voltage Range	V_{LDOIN}			7		36	V
LDOIN Supply Current	I_{LDOIN}	V_{LDOIN} = 24V, C/Q is configured as an input, no load on V_5 or LDO33			2.5	5	mA
V_5 Output Voltage Range	V_5	No load on V_5, 7V ≤ V_{LDOIN} ≤ 36V		4.75	5.00	5.25	V
Power Supply Rejection Ratio	V_{5PSRR}	f_{LDOIN} = 100Hz		60	88		dB
V_5 Load Regulation		1mA < I_{LOAD} < 10mA, V_{LDOIN} = 7V, 0.1µF bypass capacitor on V_5			0.8		%
		1mA < I_{LOAD} < 30mA, V_{LDOIN} = 7V, 0.1µF bypass capacitor on V_5, 10Ω–1µF compensation network added to V_5			0.8		
3.3V LDO (LDO33)							
LDO33 Output Voltage	V_{LDO33}	No load on LDO33		3.1	3.3	3.5	V
LDO33 Undervoltage Lockout Threshold	$V_{LDO33UVLO}$	V_{LDO33} falling			2.4		V
LDO33 Load Regulation		1mA < I_{LOAD} < 20mA, V_{LDOIN} = 7V			0.25		%
24V INTERFACE							
C/Q Driver Output Voltage High	$V_{OH\_C/Q}$	C/Q high-side enabled, 9V ≤ V_{CC} ≤ 36V	$I_{C/Q}$ = -200mA	V_{CC} – 1.9	V_{CC} – 1.4		V
			$I_{C/Q}$ = -100mA	V_{CC} – 1.4	V_{CC} – 1		
			$I_{C/Q}$ = -50mA	V_{CC} – 1.1	V_{CC} – 0.83		
C/Q Driver Output Voltage Low	$V_{OL\_C/Q}$	C/Q low-side enabled, 9V ≤ V_{CC} ≤ 36V	$I_{C/Q}$ = +200mA		1.55	2	V
			$I_{C/Q}$ = +100mA		1.2	1.7	
			$I_{C/Q}$ = +50mA		0.98	1.3	
C/Q Driver Source Current Limit	$I_{OH\_C/Q}$	C/Q high-side enabled, $V_{C/Q}$ < (V_{CC} - 5V), 9V ≤ V_{CC} ≤ 36V		+280	+350	+420	mA
C/Q Driver Sink Current Limit	$I_{OL\_C/Q}$	C/Q low-side enabled, $V_{C/Q}$ > 5V, 9V ≤ V_{CC} ≤ 36V		-423	-350	-280	mA
DO Driver Output Voltage High	V_{OH_DO}	DO high-side enabled, 9V ≤ V_{CC} ≤ 36V	I_{DO} = -200mA	V_{CC} – 2.1	V_{CC} – 1.5		V
			I_{DO} = -100mA	V_{CC} – 1.45	1.1		
			I_{DO} = -50mA	V_{CC} – 1.15	0.87		

DC Electrical Characteristics (continued)

(V_{CC} = 18V to 36V, V_L = 2.3V to 5.5V, V_{GND} = 0V; all logic inputs at V_L or GND; T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{CC} = 24V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
DO Driver Output Voltage Low	V_{OL_DO}	DO low-side enabled, 9V ≤ V_{CC} ≤ 36V	I_{DO} = +200mA		1.6	2.3	V
			I_{DO} = +100mA		1.24	1.75	
			I_{DO} = +50mA		1.04	1.4	
DO Source Current Limit	I_{OH_DO}	DO high-side enabled, V_{DO} < (V_{CC} - 5V)		-470	-340	-263	mA
DO Sink Current Limit	I_{OL_DO}	DO low-side enabled, V_{DO} > 5V		270	360	480	mA
C/Q, DI Input Voltage Range	V_{IN}	For valid RX, LI		-1.0		V_{CC} + 1.0	V
C/Q Input Threshold High	$V_{IH\_C/Q}$	C/Q driver disabled		10.5		13	V
C/Q Input Threshold Low	$V_{IL\_C/Q}$	C/Q driver disabled		8.0		11.5	V
C/Q Input Hysteresis	$V_{HYS\_C/Q}$	C/Q driver disabled		1.0	1.6		V
DI Input Threshold High	V_{IH_DI}			6.8		8	V
DI Input Threshold Low	V_{IL_DI}			5.2		6.4	V
DI Input Hysteresis	V_{HYS_DI}			1	1.6		V
C/Q Weak Pulldown Current	$I_{PDC/Q}$	C/Q driver disabled, $V_{C/Q}$ = (V_{CC} - 1V)			48	100	µA
DO Leakage Current	I_{PDDO}	DO driver disabled, V_{CC} = 36V, V_{DO} = (V_{CC} - 1V)		-1		+1	µA
DI Weak Pulldown Current	I_{PDDI}	V_{CC} = 36V, V_{DI} = (V_{CC} - 1V)				102	µA
C/Q Input Capacitance	$C_{C/Q}$	C/Q driver disabled			40		pF
DO Input Capacitance	C_{DO}	DO driver disabled			40		pF
DI Input Capacitance	C_{DI}				20		pF
LOGIC INPUTS (TX, TXEN, LO, $\overline{CS}$/PNP, SDI/DOPP, SCLK/CQPP, SPI/$\overline{PAR}$, DODIS)							
Logic-Input Voltage Low	V_{IL}			0.3 x V_L			V
Logic-Input Voltage High	V_{IH}					0.7 x V_L	V
Logic-Input Leakage Current High	I_{LEAK_H}	Logic input = V_L		-2		+2	µA
Logic-Input Leakage Current Low	I_{LEAK_L}	TX, TXEN, LO, $\overline{CS}$/PNP, SDI/DOPP, SCLK/CQPP, Logic input = GND		-2		+2	µA
SPI/ $\overline{PAR}$ Pull-Up Resistance	R_{PUSPI}				100		kΩ
Logic-Input Capacitance	C_{IN}				5		pF

DC Electrical Characteristics (continued)

(V_{CC} = 18V to 36V, V_L = 2.3V to 5.5V, V_{GND} = 0V; all logic inputs at V_L or GND; T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{CC} = 24V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC OUTPUTS (RX, $\overline{WU}$/$\overline{THSD}$, LI, UV, SDO/$\overline{DOOC}$, $\overline{IRQ}$/$\overline{CQOC}$)						
Logic-Output Voltage Low	V_{OL}	I_{OUT} = -5mA			0.4	V
Logic-Output Voltage High	V_{OHRX}, V_{OHWU}, V_{OHLI}, V_{OHSDO}, V_{OHIRQ},	I_{OUT} = 5mA (Note 3)	V_L - 0.6			V
SDO/$\overline{DOOC}$ Leakage Current	I_{LK_SDO}	SDO/$\overline{DOOC}$ disabled, SDO/$\overline{DOOC}$ = GND or V_L	-2		+2	µA
SDO/$\overline{DOOC}$ Output Voltage HIgh	V_{SDO_DOOC}	SPI/$\overline{PAR}$ = GND; I_{OUT} = 5mA	V_L - 0.6V			V
THERMAL SHUTDOWN						
Thermal Warning Threshold		Die temperature rising, OTemp bit is set		+127		°C
Thermal Warning Threshold Hysteresis		Die temperature falling, OTemp bit is cleared		+23		°C
Thermal-Shutdown Threshold		Die temperature rising		+165		°C
Thermal-Shutdown Hysteresis				20		°C

AC Electrical Characteristics

(V_{CC} = 18V to 36V, V_L = 2.3V to 5.5V, V_{GND} = 0V; all logic inputs at V_L or GND; T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{CC} = 24V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DRIVER (C/Q, DO)						
Driver Low-to-High Propagation Delay	t_{PDLH}	Push-pull or high-side (PNP) configuration, Figure 1		0.5	2	µs
Driver High-to-Low Propagation Delay	t_{PDHL}	Push-pull or low-side (NPN) configuration, Figure 1		0.5	2	µs
Driver Skew	t_{SKEW}	$\lvert t_{PDLH} - t_{PDHL} \rvert$		0.1	2	µs
Driver Rise Time	t_{RISE}	Push-pull or high-side (PNP) configuration, Figure 1		0.4	1	µs
Driver Fall Time	t_{FALL}	Push-pull or low-side (NPN) configuration, Figure 1		0.4	1	µs
Driver Enable Time High	t_{ENH}	Push-pull or high-side (PNP) configuration, Figure 3		0.3	1	µs
Driver Enable Time Low	t_{ENL}	Push-pull or low-side (NPN) configuration, Figure 2		0.3	1	µs
Driver Disable Time High	t_{DISH}	Push-pull or high-side (PNP) configuration, Figure 2 (Note 4)		1.6	3	µs
Driver Disable Time Low	t_{DISL}	Push-pull or low-side (NPN) configuration, Figure 3 (Note 4)		0.1	3	µs
RECEIVER (C/Q, DI) (Figure 4)						
Receiver Low-to-High Propagation Delay	t_{PRLH}	RxFilter = 1 (Note 5), Figure 4		0.2	2	µs
		RxFilter = 0, Figure 4		0.4	2	
Receiver High-to-Low Propagation Delay	t_{PRHL}	RxFilter = 1 (Note 5), Figure 4		0.3	2	µs
		RxFilter = 0, Figure 4		0.5	2	
WAKE-UP DETECTION (Figure 5)						
Wake-Up Input Minimum Pulse Width	t_{WUMIN}		30	40	50	µs
Wake-Up Input Maximum Pulse Width	t_{WUMAX}		120	140	160	µs
$\overline{WU}/\overline{THSD}$ Output Low Time	t_{WUL}	Valid wake-up condition on C/Q	120	200	260	µs
Short-Circuit Detection						
Short-Circuit Blanking Time	t_{SHBLK}		0.17	0.214	0.252	ms
Short-Circuit Auto-Retry Time	t_{SHAR}		11	12.9	14.6	ms

AC Electrical Characteristics (continued)

(V_{CC} = 18V to 36V, V_L = 2.3V to 5.5V, V_{GND} = 0V; all logic inputs at V_L or GND; T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{CC} = 24V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPI TIMING ($\overline{CS}$/PNP, SCLK/CQPP, SDI/DOPP, SDO/$\overline{DOOC}$) (Figure 6)						
SCLK/CQPP Clock Period	t_{CH+CL}		83.3			ns
SCLK/CQPP Pulse-Width High	t_{CH}		41.65			ns
SCLK/CQPP Pulse-Width Low	t_{CL}		41.65			ns
$\overline{CS}$/PNP Fall to SCLK/CQPP Rise Time	t_{CSS}		20			ns
SCLK/CQPP Rise to $\overline{CS}$/PNP Rise Hold Time	t_{CSH}		20			ns
SDI/DOPP Hold Time	t_{DH}		10			ns
SDI/DOPP Setup Time	t_{DS}		10			ns
Output Data Propagation Delay	t_{DO}				36	ns
SDO/$\overline{DOOC}$ Rise and Fall Times	t_{FT}				20	ns
Minimum $\overline{CS}$/PNP Pulse	t_{CSW}		76.8			ns

Note 2: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.
Note 3: UV is an open-drain output. Connect UV to a voltage less than 5.5V through an external pullup resistor.
Note 4: Disable time measurements are load-dependent.
Note 5: RxFilter is on by default in parallel mode (SPI/$\overline{PAR}$ is low).

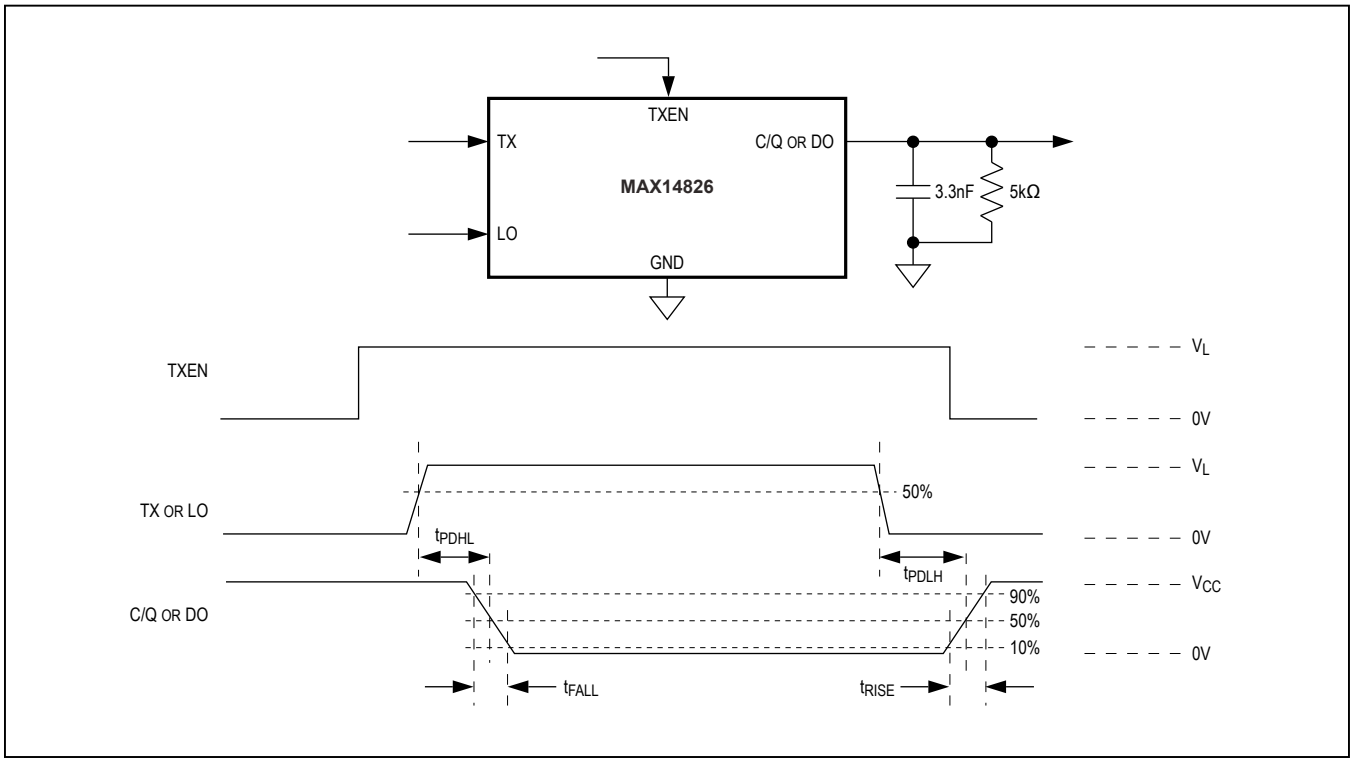


Figure 1. C/Q and LO Driver Propagation Delays and Rise/Fall Times

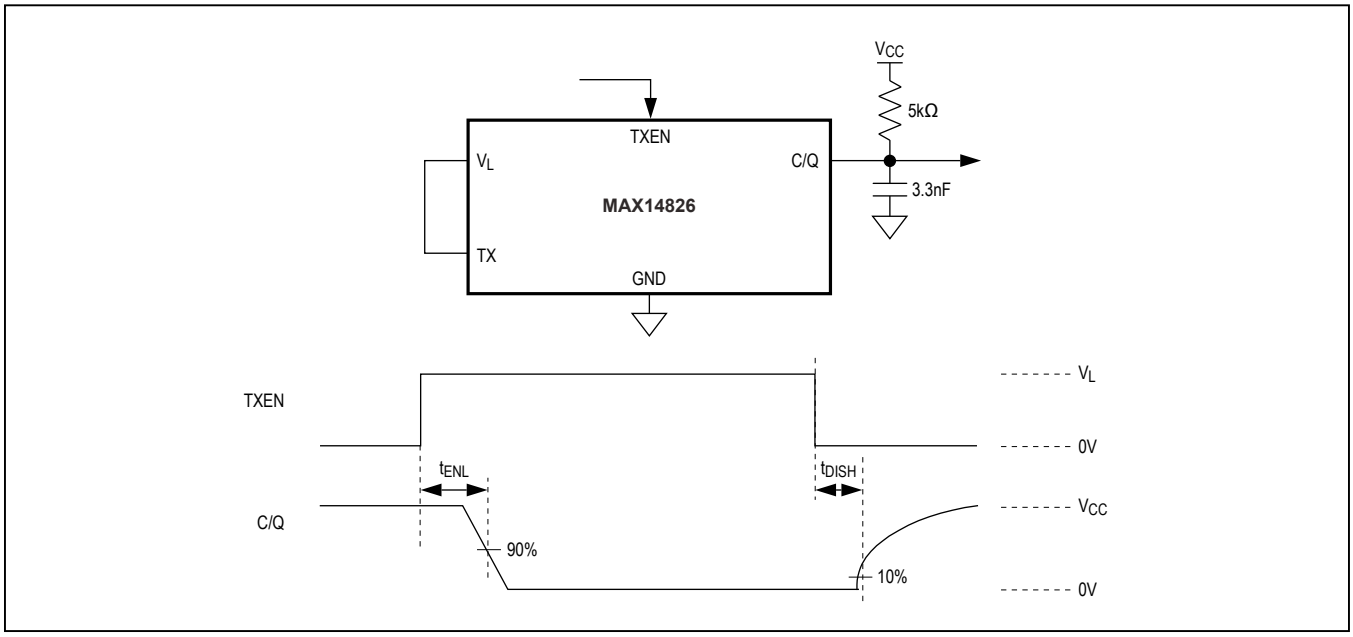


Figure 2. C/Q Driver Enable Low and Disable High Timing with External Pullup Resistor

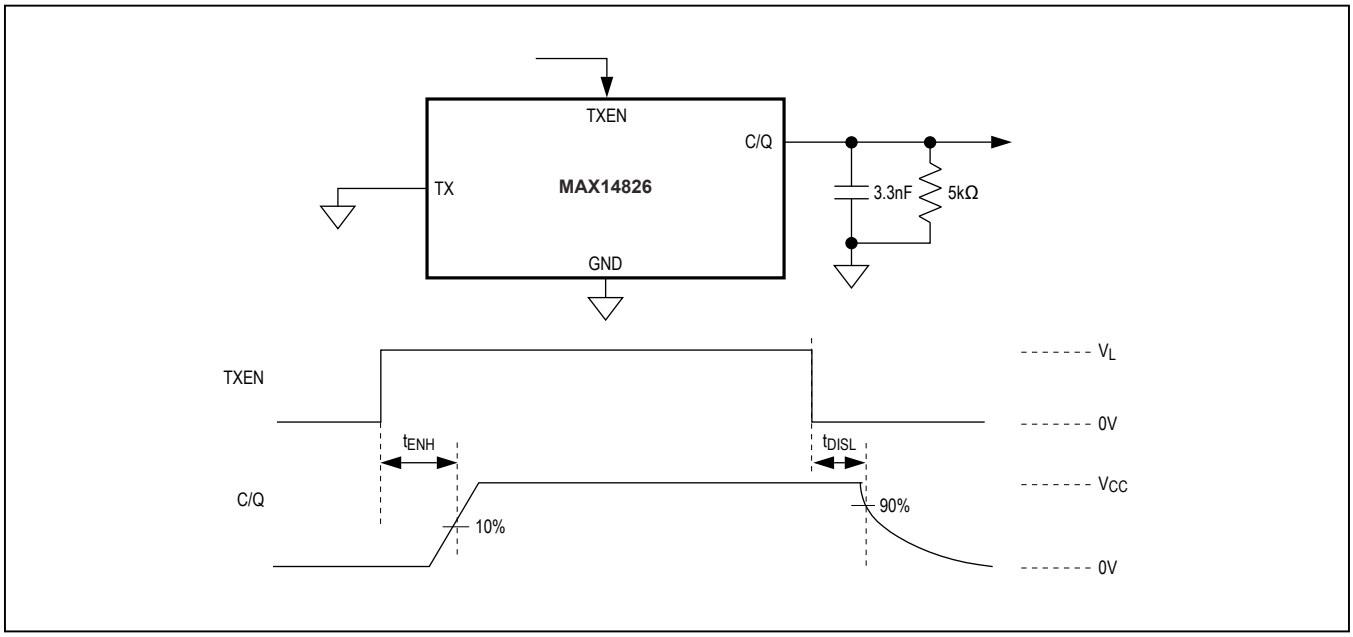


Figure 3. C/Q Driver Enable High and Disable Low Timing

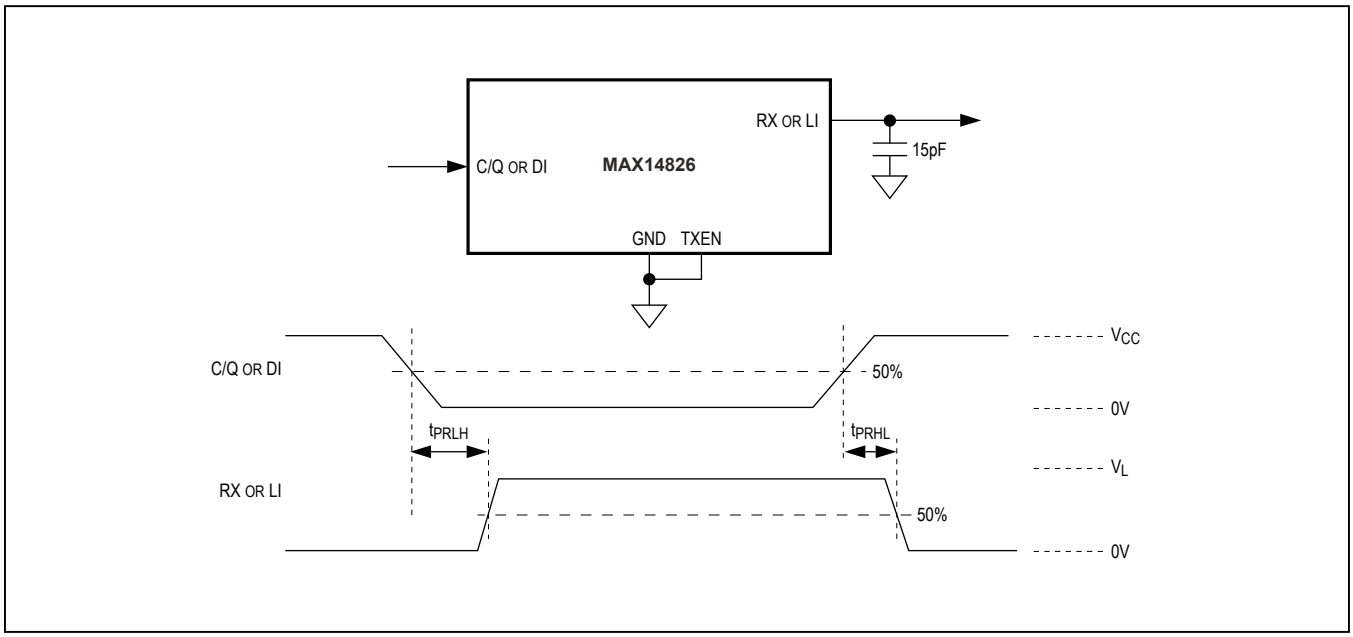
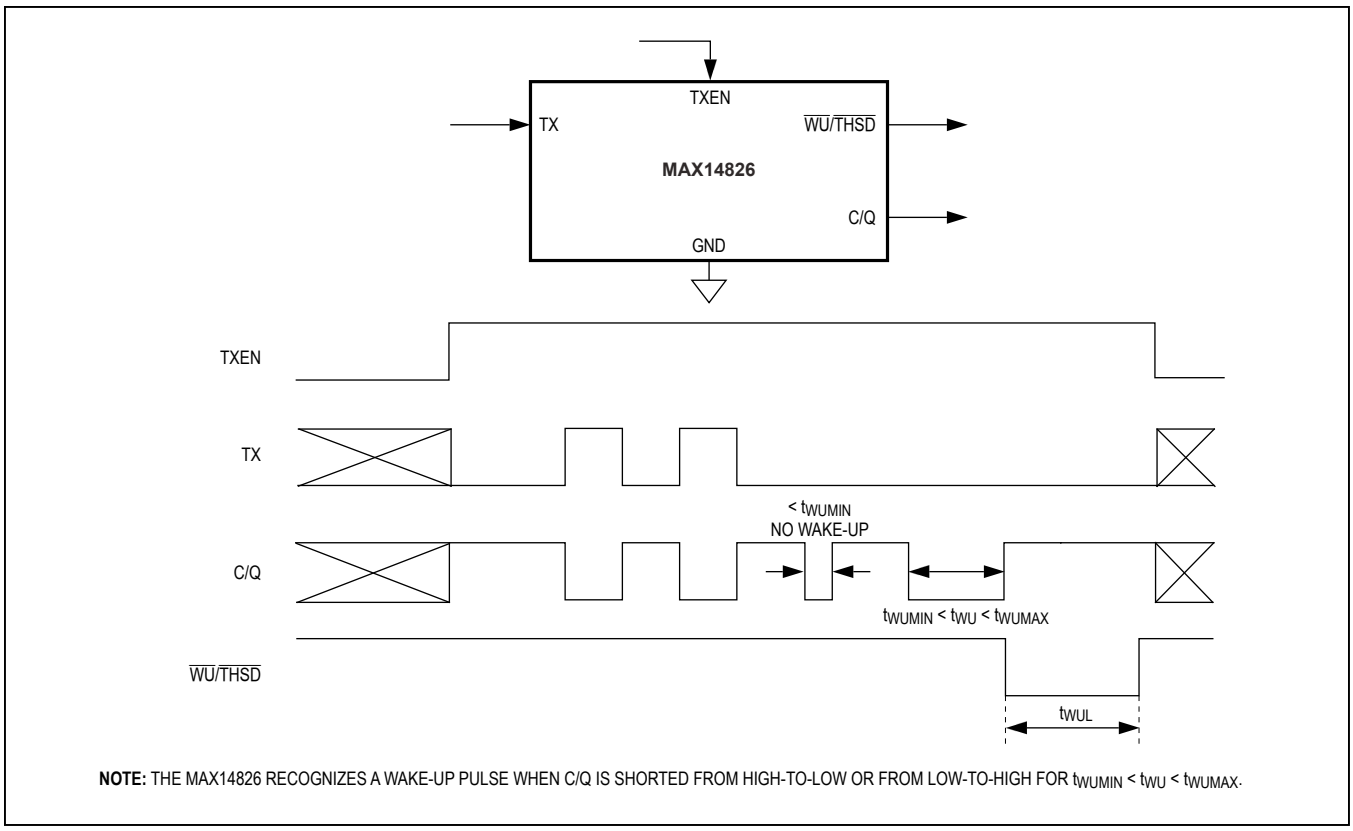


Figure 4. C/Q and DI Receiver Propagation Delays



NOTE: THE MAX14826 RECOGNIZES A WAKE-UP PULSE WHEN C/Q IS SHORTED FROM HIGH-TO-LOW OR FROM LOW-TO-HIGH FOR $t_{WUMIN} < t_{WU} < t_{WUMAX}$.

Figure 5. Wake-Up Detection Timing

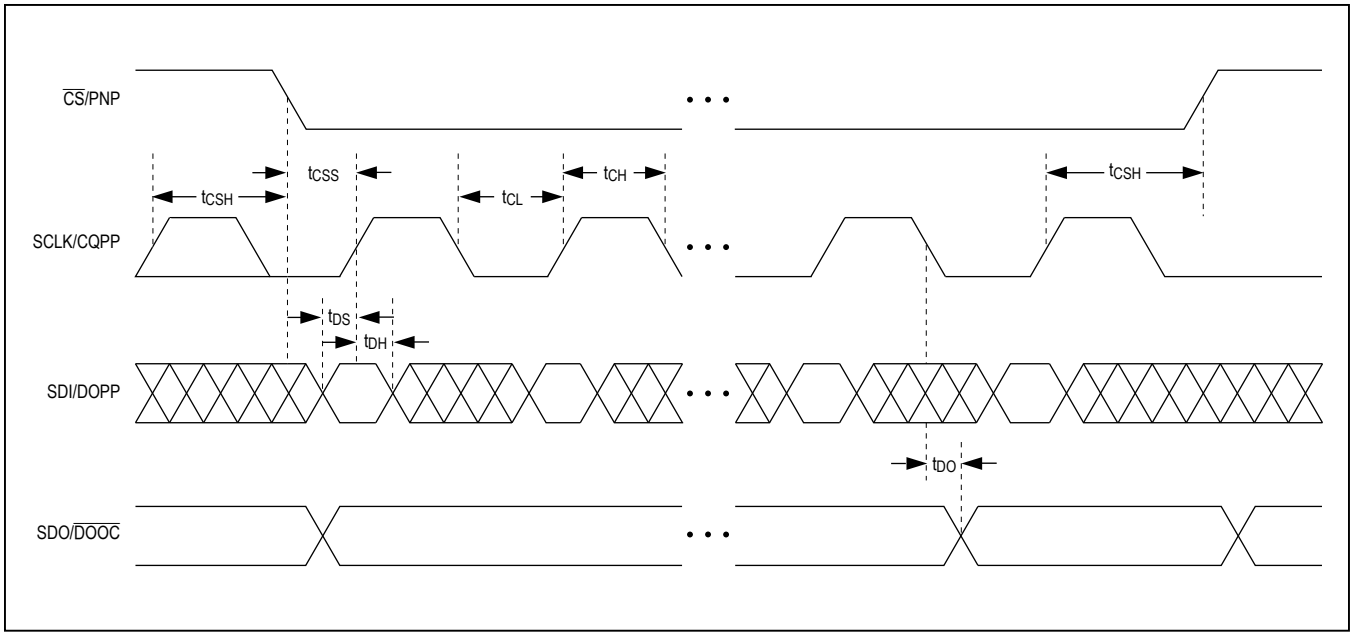
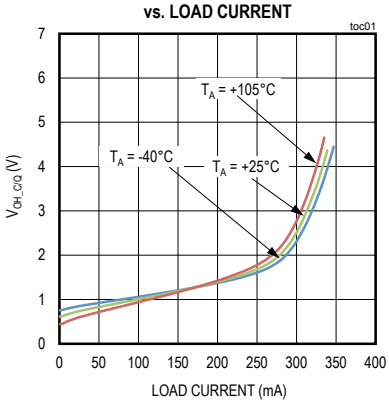


Figure 6. SPI Timing Diagram

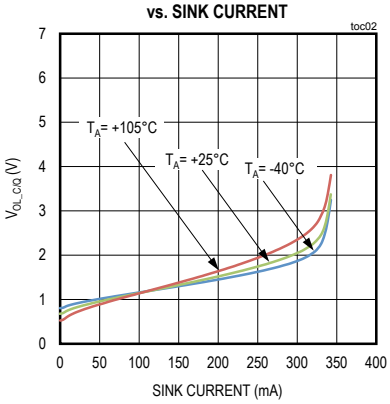
Typical Operating Characteristics

(V_{CC} = 24V, LDOIN = V_P, V_L = LDO33, C/Q and DO in push-pull configuration, T_A = +25°C, unless otherwise noted.)

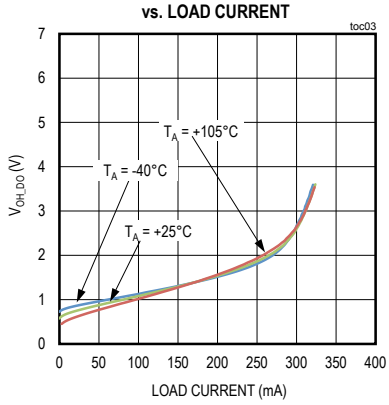
C/Q DRIVER OUTPUT HIGH vs. LOAD CURRENT



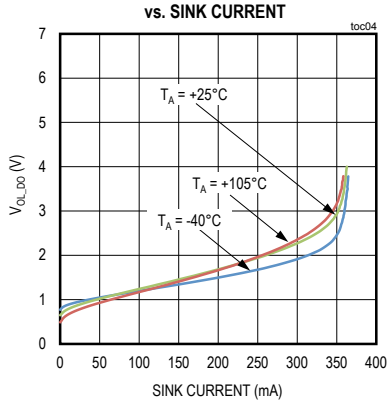
C/Q DRIVER OUTPUT LOW vs. SINK CURRENT



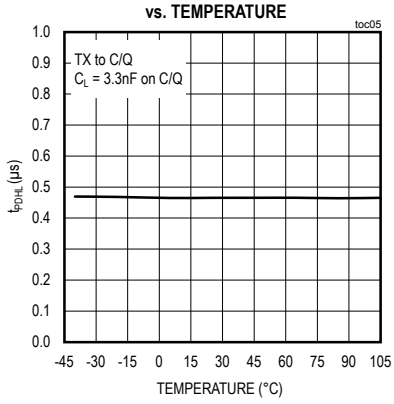
DO DRIVER OUTPUT HIGH vs. LOAD CURRENT



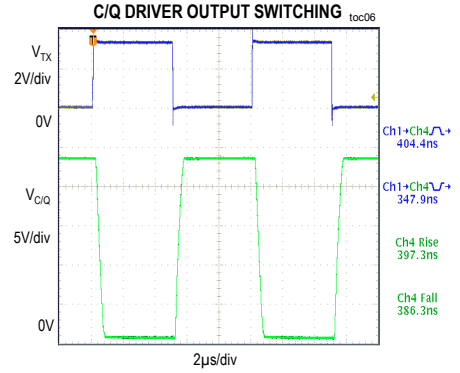
DO DRIVER OUTPUT LOW vs. SINK CURRENT



C/Q DRIVER PROPAGATION DELAY vs. TEMPERATURE



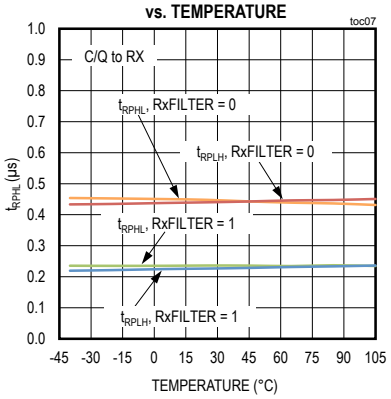
C/Q DRIVER OUTPUT SWITCHING



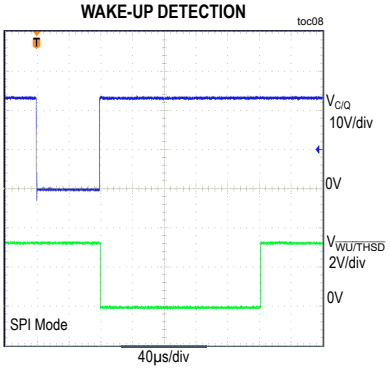
Typical Operating Characteristics (continued)

(V_{CC} = 24V, LDOIN = V_P, V_L = LDO33, C/Q and DO in push-pull configuration, T_A = +25°C, unless otherwise noted.)

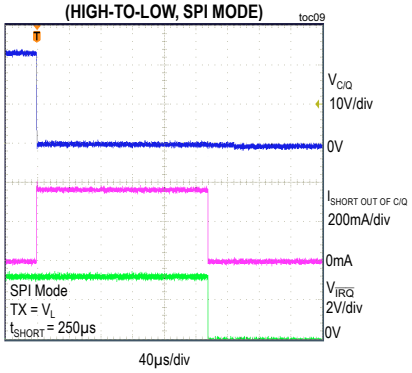
RECEIVER PROPAGATION DELAY vs. TEMPERATURE



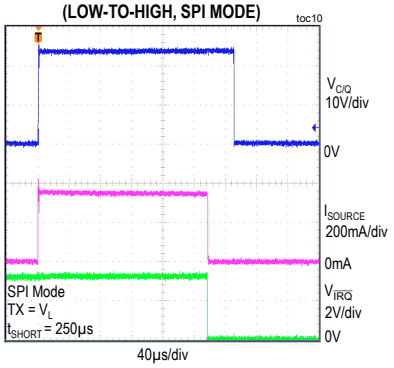
WAKE-UP DETECTION



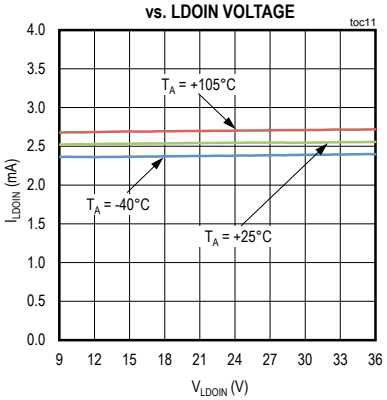
C/Q SHORT-CIRCUIT PROTECTION (HIGH-TO-LOW, SPI MODE)



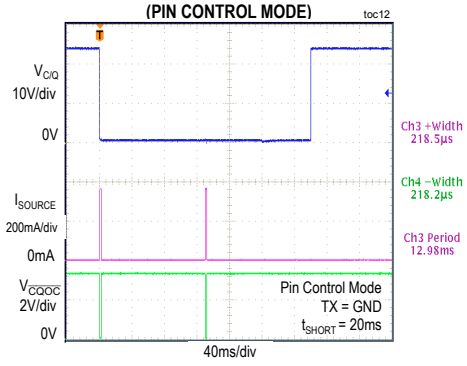
C/Q SHORT-CIRCUIT PROTECTION (LOW-TO-HIGH, SPI MODE)



LDOIN SUPPLY CURRENT vs. LDOIN VOLTAGE

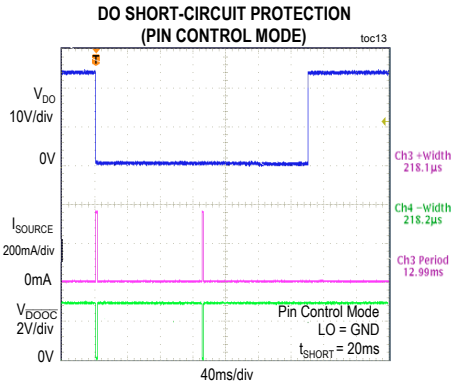


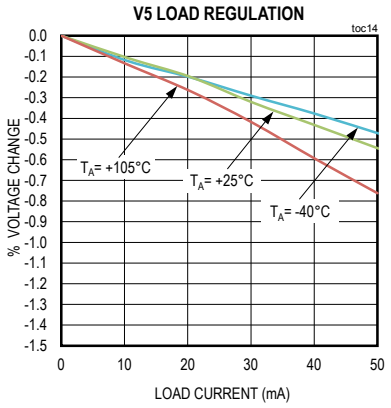
C/Q SHORT-CIRCUIT PROTECTION (PIN CONTROL MODE)

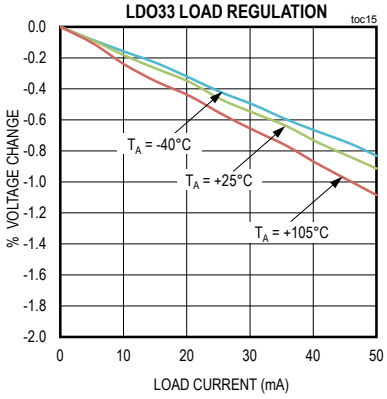


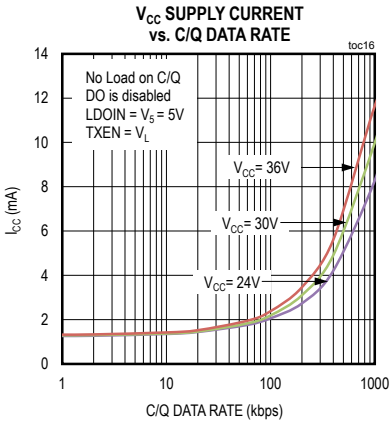
Typical Operating Characteristics (continued)

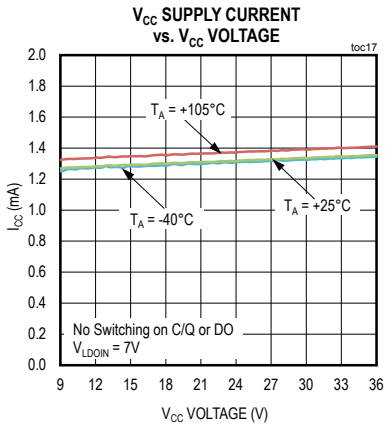
(V_{CC} = 24V, LDOIN = V_P, V_L = LDO33, C/Q and DO in push-pull configuration, T_A = +25°C, unless otherwise noted.)



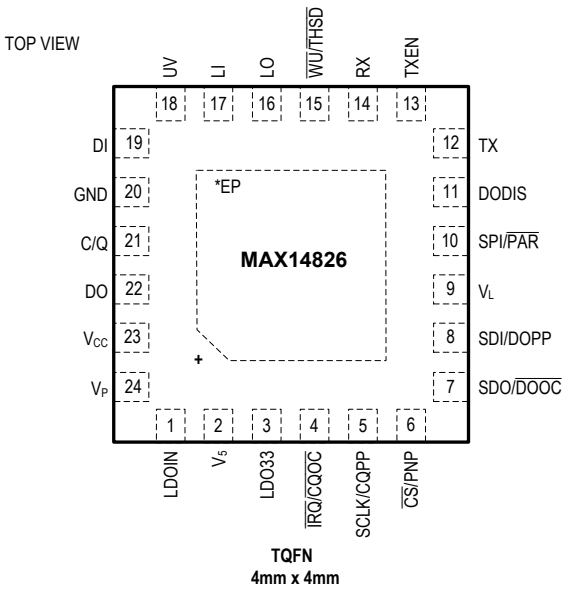








Pin Configuration



*Exposed Pad. Connect to GND.

Pin Description

PIN	NAME	FUNCTION
1	LDOIN	5V Linear Regulator Input. Bypass LDOIN to GND with a 1µF ceramic capacitor. LDOIN can be powered from V_P or from an external source in the 7V to 36V range. If using V_P to power the LDO, connect LDOIN to V_P through a 10Ω resistor.
2	V_5	5V Power-Supply Input and 5V Linear Regulator Output. Bypass V_5 to GND with a 0.1µF ceramic capacitor for 10mA load capability. Add the recommended compensation network to increase the source capability to 30mA. See the 5V and 3.3V Linear Regulators section for more information.
3	LDO33	3.3V Linear Regulator Output. Bypass LDO33 to GND with a 1µF ceramic capacitor.
4	$\overline{IRQ}/\overline{CQOC}$	Interrupt Request Output C/Q Overcurrent Indicator. In SPI mode, $\overline{IRQ}/\overline{CQOC}$ is a standard active-low interrupt request output activated by the bits in the Status register. In parallel mode, $\overline{IRQ}/\overline{CQOC}$ pulses low when an overcurrent condition occurs on C/Q. $\overline{IRQ}/\overline{CQOC}$ is a push-pull output referenced to V_L.
5	SCLK/CQPP	SPI Clock Input C/Q Mode Select Input. In SPI mode, SCLK/CQPP is the SPI clock input. In parallel mode, SCLK/CQPP sets the configuration of the C/Q driver.
6	$\overline{CS}$/PNP	Active-Low SPI Chip-Select Input C/Q and DO Mode Select Input. In SPI mode, $\overline{CS}$/PNP is the SPI chip-select input.In parallel mode, $\overline{CS}$/PNP set the configuration for the C/Q and DO drivers.
7	SDO/$\overline{DOOC}$	SPI Serial-Data Output/DO Overcurrent Indicator. In SPI mode, SDO/$\overline{DOOC}$ the SPI serial-data output. In parallel mode, SDO/$\overline{DOOC}$ pulses low when an overcurrent condition occurs on DO.
8	SDI/DOPP	SPI Serial-Data Input/ DO Mode Select Input. In SPI mode, SDI/DOPP is the SPI serial data input. In parallel mode, SDI/DOPP sets the configuration of the DO driver.
9	V_L	Logic-Level Supply Input. V_L defines the logic levels on all the logic inputs and outputs. Bypass V_L to GND with a 0.1µF ceramic capacitor.

Pin Description (continued)

PIN	NAME	FUNCTION
10	SPI/$\overline{PAR}$	SPI-Mode/Parallel-Mode Select Input. Drive SPI/ $\overline{PAR}$ high to enable SPI functionality. Drive SPI/$\overline{PAR}$ low to enable parallel-mode operation.
11	DODIS	DO Disable Input. Drive DODIS low to enable the DO output. Drive DODIS high to disable the DO output. DO is high-impedance when DODIS is high.
12	TX	Transmit Communication Input. The logic on the C/Q output is the inverse logic level of the signals on the TX input.
13	TXEN	Transmitter Enable. Drive TXEN high to enable the C/Q transmitter. TXEN is referenced to V_L.
14	RX	Receiver Output. RX is the inverse logic level of C/Q. RX is always high when the RxDis bit in the CQConfig register is set to 1.
15	$\overline{WU}$/$\overline{THSD}$	Wake-up Output/Active-Low Thermal-Shutdown Indicator. In SPI mode, $\overline{WU}$/$\overline{THSD}$ is the wake-up output. In this mode, $\overline{WU}$/$\overline{THSD}$ pulses low for 190µs (typ) when a valid wake-up pulse is detected on the C/Q line. In parallel mode, $\overline{WU}$/$\overline{THSD}$ is the thermal-shutdown indicator and asserts low during thermal shutdown. $\overline{WU}$/$\overline{THSD}$ is a push-pull output referenced to V_L.
16	LO	Logic Input of the DO Output. LO is the logic input that drives DO. LO is referenced to V_L.
17	LI	Logic Output of the 24V DI Logic Input. LI is the inverse logic of DI. LI is referenced to V_L.
18	UV	Open-Drain Undervoltage Indicator Output. In case of an undervoltage, the UV open-drain transistor is off.
19	DI	24V Logic-Level Digital Input
20	GND	Ground
21	C/Q	SIO/IO-Link Data Input/Output. Drive TXEN high to enable the C/Q driver. The logic on the C/Q output is the inverse logic level of the signals on the TX input. RX is the logic inverse of C/Q. The C/Q driver output level can be set by the TX input or programmed by the Q bit. The level on C/Q can be read by the RX ouput or the $\overline{Q}$Lvl bit.
22	DO	24V Logic-Level Digital Output. DO is the inverse logic level of the LO input and can be digitally-controlled through the DIOConfig register.
23	V_{CC}	Power-Supply Input. Bypass V_{CC} to GND with a 1µF ceramic capacitor.
24	V_P	Protected 24V Supply Output. V_P is one diode drop below V_{CC}. V_P is reverse-polarity-protected and can be used as a 24V protected supply to the sensor or actuator electronics.
—	EP	Exposed Pad. Connect EP to GND.

Detailed Description

The MAX14826 is a sensor/actuator transceiver designed for IO-Link® device applications supporting all the specified IO-Link data rates. In IO-Link applications, the devices act as the physical layer interface to a microcontroller running the data-link layer protocol. The device contains an additional 24V digital input and an additional 24V digital output. Two internal linear regulators generate common sensor and actuator power requirements: 5V and 3.3V.

The device detects IO-Link wake-up conditions on the C/Q line and generates a wake-up signal on the $\overline{WU}$/$\overline{THSD}$ output. The C/Q and DO drivers are independently-configurable to any one of three driver output types: push-pull, high-side (PNP), or low-side (NPN).

This device is configured and monitored through a pin-selectable parallel or SPI™ interface. Extensive alarms are available through SPI.

24V Interface

The device features an IO-transceiver interface capable of operating with voltages up to 36V. This is the 24V interface and includes the C/Q input/output, the logic-level digital output (DO), and the logic-level digital input (DI).

Configurable Drivers

The device features selectable push-pull, high-side (PNP), or low-side (NPN) switching drivers at C/Q and DO.

Parallel Mode

In parallel mode, the C/Q and DO drivers are independently-configurable using the CQPP/SCLK, DOPP/SDI, and PNP/$\overline{CS}$ inputs. Set CQPP/SCLK high to select push-pull operation on the C/Q driver. Set DOPP/SDI high to select the push-pull operation on the DO driver.

The PNP/$\overline{CS}$ input selects NPN or PNP operation for drivers configured for open-drain operation. Set PNP/$\overline{CS}$ high for PNP operation. Set PNP/$\overline{CS}$ low for NPN operation. See Table 1.

Table 1. Parallel Mode Select Truth Table

CQPP/SCLK	DOPP/SDI	PNP/CS	C/Q MODE	DO MODE
Low	Low	Low	NPN	NPN
Low	Low	High	PNP	PNP
High	Low	Low	Push-pull	NPN
High	Low	High	Push-pull	PNP
Low	High	Low	NPN	Push-pull
Low	High	High	PNP	Push-pull
High	High	x	Push-pull	Push-pull

X = Don't care

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SPI is a trademark of Motorola, Inc.

SPI Mode

In SPI mode, write to the CQConfig and DIOConfig registers to configure the C/Q and DO drivers.

Set the C/Q_N/P and C/Q_PP bits in the CQConfig register to select the driver mode for the C/Q driver. When configured as a push-pull output, C/Q switches between VP and ground. Set the C/Q_PP bit to 1 to select push-pull operation at C/Q. Set the C/Q_PP bit to 0 to configure the C/Q output for open-drain operation. The C/Q_N/P bit selects NPN or PNP operation when C/Q is configured as an open-drain output.

Set the DoN/P and DoPP bits in the DIOConfig register to select the driver mode for the DO output. When configured as a push-pull output, DO switches between V_{CC} and ground. Set the DoPP bit to 1 for push-pull operation. The DoN/P bit selects NPN or PNP operation when DO is configured as an open-drain output. Set the DoPP bit to 0 to select high-side or low-side operation at DO.

C/Q Driver and Receiver

The C/Q driver can be enabled/disabled in either parallel-input mode or SPI mode.

The device's C/Q driver is specified for 200mA to drive large capacitive loads of up to 1µF and dynamic impedances like incandescent lamps. The maximum load current for C/Q is limited to 480mA.

The C/Q receiver is always on. In SPI mode, the RX output through the RxDis bit in the CQConfig register. Set the RxDis bit to 1 to set the RX output high. Set the RxDis bit to 0 for normal receive operation.

The C/Q receiver has an analog lowpass filter to reduce high-frequency noise present on the line.

C/Q Fault Detection

The device registers a C/QFault condition under either of two conditions:

1) When it detects a short-circuit for longer than 214µs (typ). A short condition exists when the C/Q driver's load current exceeds the 350mA (typ) current limit.
2) When it detects a voltage level error at the C/Q output. A voltage level error occurs when the C/Q driver is configured for open-drain operation (NPN or PNP), the driver is turned off, and the C/Q voltage is not pulled to exceed the C/Q receiver's threshold levels (< 8V or > 13V) by the external supply.

When a C/QFault error occurs, the C/QFault and C/QFaultInt bits are set, $\overline{IRQ}$/$\overline{CQOC}$ asserts, and the driver is turned off after the start of the fault condition.

When a short-circuit event occurs on C/Q, the driver enters autoretry mode. In autoretry mode, the device periodically checks whether the short is still present and attempts to correct the driver output. Autoretry attempts last for 214µs (typ) and occur every 12.9ms (typ).

DO Fault Detection

The device registers a DoFault event when a short-circuit is present at the DO output for 214µs (typ). A short condition exists when the load current on the DO driver exceeds the 300mA (typ) DO current limit. When a short-circuit condition is detected, the DO driver enters autoretry mode. In autoretry mode the device periodically checks whether the error is still present. Autoretry attempts last for 214µs (typ) and occur every 12.9ms (typ). When a DoFault error is detected, SDO/DOOC asserts (parallel mode) or the DoFault and DoFaultInt bits are set, $\overline{IRQ}/\overline{CQOC}$ asserts. The driver is turned off 214µs (typ) after the start of the DO faults.

Reverse-Polarity Protection

The device is protected against reverse-polarity connections on V_{CC}, C/Q, DO, DI, and GND. Any combination of these pins can be connected to DC voltages up to 40V (max). A short to 40V results in a current flow of less than 500µA.

Ensure that the maximum voltage between any of these pins does not exceed 40V.

5V and 3.3V Linear Regulators

The MAX14826 includes two internal regulators to generate 5V (V_5) and 3.3V (LDO33). V_5 is specified for a total of 10mA load current, including the load from LDO33, when bypassed with a 0.1µF capacitor to ground. Add the compensation network shown in Figure 7 to draw up to 30mA of total external load current from V_5. LDO33 is specified up to 20mA. The input of V_5 (LDOIN) can be powered from V_P, the protected 24V supply output, or by another voltage in the 7V to 36V range.

If the external circuits powered by the linear regulators require an input bypass capacitance greater than 100nF for 5V, or 1µF for 3.3V, a compensation network must be added on the LDO output. In this situation, connect a capacitor equal to the value required by the external circuit to the LDO output and a 10Ω series resistor between the output and its load (see Figure 8). The capacitors (C5 and C33) in the figure represent the capacitance required by the external circuits. For simplicity, Figure 8 does not show the required protection diodes.

The 5V LDO can be disabled by connecting LDOIN to V_5. When the internal 5V LDO is not used, however, V_5 becomes the supply input for the internal analog and digital functions and must be supplied externally for normal operation. Apply an external voltage of 4.75V to 5.25V to V_5 when the LDO is disabled.

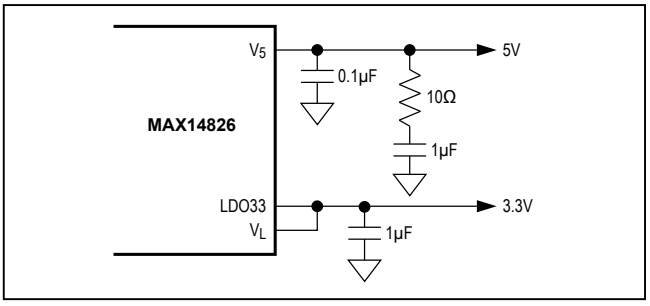

Figure 7. V_5 Compensation Network

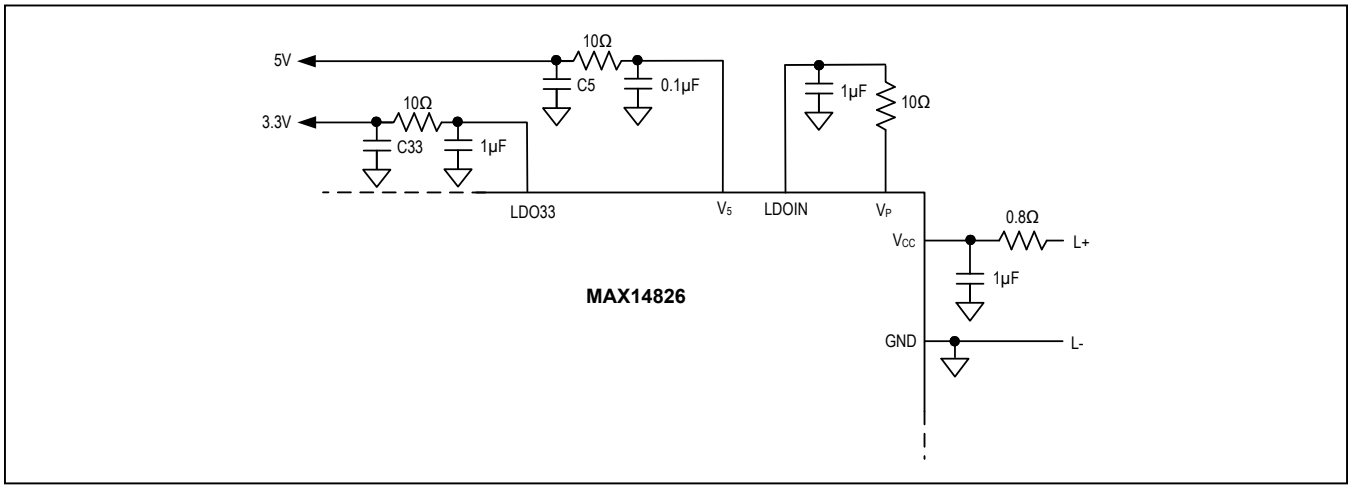

Figure 8. Larger Bypass Capacitance for Powering External Circuits

In SPI mode, use the LDO33Dis bit in the Mode register to disable the 3.3V LDO. See the Mode Register [R1, R0] = [1, 1] section for more information. LDO33 cannot be disabled in parallel mode.

V_5 and LDO33 are not protected against short-circuits.

Power-Up

The C/Q and DO driver outputs and the UV output are high impedance when V_{CC}, V_5, V_L, and/or LDO33 voltages are below their respective undervoltage thresholds during power-up. UV goes low and the drivers are enabled when all these voltages exceed their respective undervoltage lockout thresholds.

The drivers are automatically disabled if V_{CC}, V_5, or V_L falls below its threshold.

Undervoltage Detection

The device monitors V_{CC}, V_5, V_L, and optionally LDO33 for undervoltage conditions. The C/Q and DO drivers, as well as UV, are high-impedance when any monitored voltage falls below its UVLO threshold.

V_{CC}, V_5, and V_L undervoltage detection cannot be disabled. When V_{CC} falls below the V_{CCUVLO} threshold, UV asserts high, and $\overline{IRQ}/\overline{CQOC}$ asserts low. In SPI mode, the UV24 and UV24Int bits are also set.

The SPI register contents are unchanged while V_5 is present, regardless of the state of V_{CC} and LDO33. The SPI interface is not accessible and $\overline{IRQ}/\overline{CQOC}$ is not available when UV is asserted due to a V_5 or V_L undervoltage event.

In SPI mode, the internal 3.3V LDO regulator voltage (V_{LDO33}) falls below the LDO33 undervoltage lockout threshold, the UV33Int bit in the Status register is set and $\overline{IRQ}/\overline{CQOC}$ asserts. UV asserts if the UV33En bit in the Mode register is set to 1.

The UV output deasserts once the undervoltage condition is removed; however, bits in the Status register and the $\overline{IRQ}/\overline{CQOC}$ output are not cleared until the Status register has been read if using SPI functionality.

Wake-Up Detection (SPI Mode Only)

The device detects an IO-Link wake-up condition on the C/Q line in push-pull, high-side (PNP), or low-side (NPN) operation modes. A wake-up condition is detected when the C/Q output is shorted for 80µs (typ). $\overline{WU}/\overline{THSD}$ pulses low for 190µs (typ) when the device detects a wake-up pulse on C/Q (Figure 5).

In SPI mode, set the WuIntEn bit in the Mode register to set the WuInt bit in the Status register and generate an interrupt on $\overline{IRQ}/\overline{CQOC}$ when a wake-up pulse is detected. WuInt is set and $\overline{IRQ}/\overline{CQOC}$ asserts immediately after C/Q is released when WuIntEn = 1.

The wake-up dectection function is not available in parallel mode. For IO-Link applications, monitor the $\overline{CQOC}/\overline{IRQ}$ output with a microcontroller to detect the short-circuit on a C/Q driver during a wake-up event.

Short-Circuit Detect Outputs (Parallel Mode only)

The MAX14826 features independent overcurrent interrupt outputs for the C/Q and DO drivers. When an overcurrent condition occurs on C/Q, $\overline{IRQ}/\overline{CQOC}$ pulses low. (Figure 9) Similarly, when an overcurrent condition occurs on DO, SDO/$\overline{DOOC}$ pulses low.

$\overline{IRQ}/\overline{CQOC}$ and/or SDO/$\overline{DOOC}$ will also pulse low when driving capacitive and lamp loads. The drivers must deliver maximum current to these loads/lamps as they are being charged up or turned on.

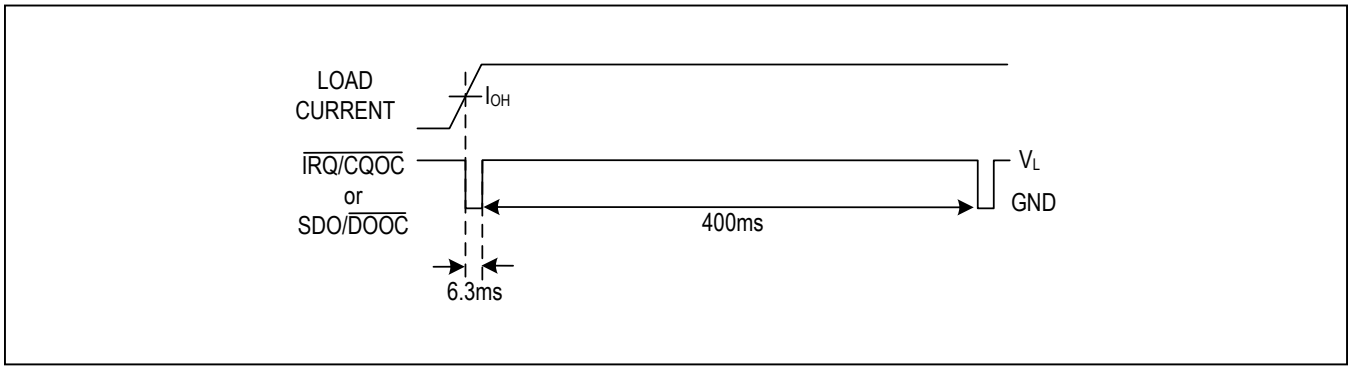

Figure 9. Short-Circuit Detect Output

Note that a short negative pulse on $\overline{IRQ}/CQOC$ and/or SDO/DOOC will occur at each driver switching event, even when no loads are driven.

Thermal Protection and Considerations

The internal LDOs and drivers can generate more power than the package for the devices can safely dissipate. Ensure that the driver LDO loading is less than the package can dissipate. Total power dissipation for the device is calculated using the following equation:

$$P_{TOTAL} = P_{C/Q} + P_{DO} + P_5 + P_{LDO33} + P_Q + P_{CLCQ} + P_{CLDI}$$

where $P_{C/Q}$ is the power generated in the C/Q driver, P_{DO} is the power dissipated by the DO driver, P_5 and P_{LDO33} are the power generated by the LDOs, P_Q is the quiescent power generated by the devices.

Ensure that the total power dissipation is less than the limits listed in the *Absolute Maximum Ratings* section.

Use the following to calculate the power dissipation (in mW) due to the C/Q driver:

$$P_{C/Q} = [I_{C/Q}(max)] \times [0.5 + 7 \times I_{C/Q}(max)]$$

Calculate the internal power dissipation of the DO driver using the following equation:

$$P_{DO} = [I_{DO}(max)] \times [0.5 + 7 \times I_{DO}(max)]$$

Calculate the power dissipation in the 5V LDO, V_5, using the following equation:

$$P_5 = (V_{LDOIN} - V_5) \times I_5$$

where I_5 includes the I_{LDO33} current sourced from LDO33.

Calculate the power dissipated in the 3.3V LDO, LDO33, using the following equation:

$$P_{LDO33} = 1.7V \times I_{LDO33}$$

Calculate the quiescent power dissipation in the device using the following equation:

$$P_Q = I_{CC}(max) \times V_{CC}(max)$$

Thermal Shutdown

All regulators and the C/Q and DO output drivers are automatically switched off when the internal die temperature exceeds the +165°C (typ) thermal shutdown threshold. The $\overline{WU}/\overline{THSD}$ output asserts low during thermal shutdown and SPI communication is not available.

Regulators are automatically switched on and $\overline{WU}/\overline{THSD}$ deaasserts when the internal die temperature falls below the thermal shutdown threshold plus hysteresis. The internal registers return to their default state when the V_5 regulator is switched on.

Overtemperature Warning (SPI Mode only)

In SPI mode, bits in the Status and Mode registers are set when the temperature of the device exceeds +127°C (typ). The OTempInt bit in the Status register is set and $\overline{IRQ}/\overline{CQOC}$ asserts when the OTemp bit in the mode register is set. Read the Status register to clear the OTempInt bit and $\overline{IRQ}/\overline{CQOC}$.

The OTemp bit is cleared when the die temperature falls to +104°C.

The device continues to operate normally unless the die temperature reaches the +165°C thermal shutdown threshold, when the device enters thermal shutdown.

Register Functionality

The devices have four 8-bit-wide registers for configuration and monitoring (Table 2).

Table 2. Register Summary

REGISTER	R1	R0	D7	D6	D5	D4	D3	D2	D1	D0
Status	0	0	WuInt	DoFaultInt	DiLvl	$\overline{Q}$Lvl	C/QFaultInt	UV33Int	UV24Int	OTempInt
CQConfig	0	1	RxFilter	—	C/Q_N/P	C/Q_PP	C/QDEn	Q	RxDis	—
DIOConfig	1	0	DoInv	DoAv	DoN/P	DoPP	DoEn	DoBit	LiDis	—
Mode	1	1	RST	WuIntEn	DoFault	C/QFault	UV24	OTemp	UV33En	LDO33Dis

R1/R0 = Register address.
— = Register not used.

Status Register [R1, R0] = [0,0]

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	WuInt	DoFaultInt	DiLvl	$\overline{Q}$Lvl	C/QFaultInt	UV33Int	UV24Int	OTempInt
Read/Write	R	R	R	R	R	R	R	R
POR State	0	0	X	X	0	0	0	0
Reset Upon Read	Yes	Yes	No	No	Yes	Yes	Yes	Yes
Parallel Pin Configuration (SPI is Low)	X	X	X	X	X	X	X	X

X = Unknown. These bits are dependent on the DI logic and C/Q inputs.

The Status register reflects the logic levels of C/Q and DI and shows the source of interrupts that cause an $\overline{IRQ}/\overline{CQOC}$ hardware interrupt. The $\overline{IRQ}/\overline{CQOC}$ interrupt is asserted when an alarm condition (OTemp, UV33Int, UV24, C/QFault, DoFault, WuInt) is detected. All bits in the Status register are read-only. The interrupt bits return to the default state after the Status register is read. If a C/Q or DO fault condition persists, the associated interrupt bits are immediately set after the Status register is read.

BIT	NAME	DESCRIPTION
D7	WuInt	**Wake-Up Interrupt Request.** WuInt is set when an IO-Link wake-up request pulse is detected on C/Q and the WuIntEn bit in the Mode register is set. $\overline{IRQ}/\overline{CQOC}$ asserts when WuInt is set to 1. Read the Status register to clear the WuInt bit and deassert $\overline{IRQ}/\overline{CQOC}$.
D6	DoFaultInt	**DO Fault Interrupt.** DoFaultInt interrupt bit and DoFault bit (in the Mode register) are set when a fault condition occurs on the DO driver output. The device registers a fault condition when a short-circuit or voltage fault is detected on DO (see the DO Fault Detection section for more information). $\overline{IRQ}/\overline{CQOC}$ asserts when DoFaultInt is 1. Read the Status register to clear the DoFaultInt bit and deassert $\overline{IRQ}/\overline{CQOC}$.
D5	DiLvl	**DI Logic Level.** The DiLvl bit mirrors the current logic level at the DI input. It is the inverse of the LI output and is always active regardless of the state of the LiDis bit (Table 2). DiLvl does not affect $\overline{IRQ}/\overline{CQOC}$. DiLvl is not changed when the Status register is read.

BIT	NAME	DESCRIPTION
D4	$\overline{Q}$Lvl	**C/Q Logic Level.** The $\overline{Q}$Lvl bit is the inverse of the logic level at C/Q. $\overline{Q}$Lvl is 1 when the C/Q input level is low (< 8V) and is 0 when the C/Q logic level is high (> 13V) (Table 3). $\overline{Q}$Lvl remains active when the C/Q receiver output, RX is disabled (RxDis = 1). $\overline{Q}$Lvl does not affect $\overline{IRQ}/\overline{CQOC}$. $\overline{Q}$Lvl is not changed when the Status register is read.
D3	C/QFaultInt	**C/Q Fault Interrupt.** The C/QFaultInt interrupt bit and C/QFault bit (in the Mode register) are set when a short-circuit or voltage fault occurs on the C/Q driver output (see the C/Q Fault Detection section for more information). $\overline{IRQ}/\overline{CQOC}$ asserts when C/QFault is 1. Read the Status register to clear the C/QFaultInt bit and deassert $\overline{IRQ}/\overline{CQOC}$.
D2	UV33Int	**Internal 3.3V LDO (LDO33) Undervoltage Warning.** Both the UV33Int interrupt bit and the UV33En bit (in the Mode register) are set when V_{LDO33} falls below the 2.4V LDO33 undervoltage threshold. If UV33En is set in the Mode register, $\overline{IRQ}/\overline{CQOC}$ asserts low when the UV33Int bit is 1. Read the Status register to clear the UV33Int bit and deassert $\overline{IRQ}/\overline{CQOC}$. Set the UV33En bit to 1 in the Mode register to enable undervoltage monitoring for UV33Int. When enabled, UV asserts high when the UV33Int bit is 1. UV deasserts when V_{LDO33} rises above the LDO33 undervoltage threshold.
D1	UV24Int	**V_{CC} Undervoltage Interrupt.** The UV24Int interrupt bit and the UV24 bit (in the Mode register) are set when the V_{CC} voltage falls below the 7.4V undervoltage threshold. $\overline{IRQ}/\overline{CQOC}$ asserts low when the UV24Int bit is 1. Read the Status register to clear the UV24Int bit and deassert $\overline{IRQ}/\overline{CQOC}$. V_{CC} undervoltage detection cannot be disabled.
D0	OTempInt	**Overtemperature Warning.** The OTempInt interrupt bit and the OTemp bit (in the Mode register) are set when a high-temperature condition is detected by the devices. OTemp is set when the temperature of the die exceeds +127°C (typ). OTempInt is set and $\overline{IRQ}/\overline{CQOC}$ asserts when the OTemp bit is 1. The OTempInt bit is cleared and $\overline{IRQ}/\overline{CQOC}$ deasserts when the Status register is read. Once cleared, OTempInt is not reset if the die temperature remains above the thermal warning threshold and does not fall below +104°C.

Table 3. DiLvl and LI Output

V_{DI} (V)	DiLvl BIT	LI OUTPUT
< 5.2	0	High
> 8	1	Low

Table 4. $\overline{Q}$Lvl and RX Output

$V_{C/Q}$ (V)	$\overline{Q}$Lvl BIT	RX OUTPUT
< 8	1	High
>13	0	Low

CQConfig Register [R1, R0] = [0,1]

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RxFilter	—	C/Q_N/P	C/Q_PP	C/QDEn	Q	RxDis	—
Read/Write	R/W	—	R/W	R/W	R/W	R/W	R/W	—
POR State	0	—	0	0	0	0	0	—
Parallel Pin Configuration (SPI/$\overline{\text{PAR}}$ is low)	0	—	CQPP and PNP pins define mode	CQPP and PNP pins define mode	0	0	0	—

— = Register not used.
X = Unknown.

Use the CQConfig register to control the C/Q receiver and driver parameters. All bits in the CQConfig register are set to 0 at power-up.

BIT	NAME	DESCRIPTION
D7	RxFilter	C/Q and DI Receiver Filter Control. The C/Q and DI receivers have analog lowpass filters to reduce high-frequency noise on the receiver inputs. Set the RxFilter bit to 0 to set the filter corner frequency to 500kHz. Set the RxFilter bit to 1 to set the filter corner frequency to 1MHz (this setting is used for high-speed COM3 operation). Noise filters on C/Q and DI are controlled simultaneously by the RxFilter bit.
D6	—	This bit is not used.
D5	C/Q_N/P	**C/Q Driver NPN/PNP Mode.** The C/Q_N/P bit selects between low-side (NPN) and high-side (PNP) modes when the C/Q driver is configured as an open-drain output (C/Q_PP = 0). Set C/Q_N/P to 1 to configure the driver for low-side (NPN) operation. Set C/Q_N/P to 0 for high-side (PNP) operation.
D4	C/Q_PP	**C/Q Driver Push-Pull Operation.** Set C/Q_PP to 1 to enable push-pull operation on the C/Q driver. The C/Q output is open-drain when C/Q_PP is 0.
D3	C/QDEn	**C/Q Driver Enable/Disable.** Set the C/QDEn bit to 1 to enable the C/Q driver. Set C/QDEn to 0 for hardware (TXEN) control. See Table 4.
D2	Q	**C/Q Driver Output Logic.** The Q bit can be used to program the C/Q output driver through software. The C/Q driver must be enabled and TX must be high to control the C/Q driver through the Q bit (Figure 9). C/Q has the same logic polarity as the Q bit. Set the Q bit to 0 to control the C/Q driver with TX. The C/Q driver output state depends on the C/Q_PP and C/Q_N/P bits as shown in Table 5. Note that Table 5 assumes that the C/Q driver is enabled (TXEN = V_L or C/QDEn = 1).
D1	RxDis	**C/Q Receiver Enable/Disable.** Set the RxDis bit to 1 to disable the C/Q receiver. The RX output is high when RxDis is 1.
D0	—	This bit is not used.

Table 5. C/QDEn and TXEN C/Q Driver Control

C/QDEn	TXEN	C/Q DRIVER
0	Low	Disabled
1	Low	Enabled
X	High	Enabled

X = Don't care.

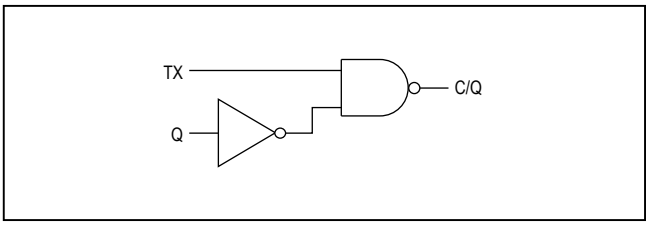

Figure 10. Equivalent C/Q Logic

Table 6. C/Q Driver Output State

TX (SEE NOTE)	Q	C/Q_PP	C/Q_N/P	C/Q CONFIGURATION	C/Q STATE
High	1	0	0	PNP, open-drain	On, C/Q is high
High	0	0	0	PNP, open-drain	Off, C/Q is high-impedance
High	1	0	1	NPN, open-drain	Off, C/Q is high-impedance
High	0	0	1	NPN, open-drain	On, C/Q is low
High	1	1	X	Push-pull	High
High	0	1	X	Push-pull	Low

Note: *TX = V_L.*
X = Don't care.

DIOConfig Register [R1, R0] = [1,0]

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	DoInv	DoAv	DoN/P	DoPP	DoEn	DoBit	LiDis	—
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
POR State	0	0	0	0	0	0	0	0
Parallel Pin Configuration (SPI/$\overline{\text{PAR}}$ is low)	0	0	DOPP and PNP pins define mode	DOPP and PNP pins define mode	0	0	0	X

— = Register not used.
X = Unknown.

Use the DIOConfig register to control the DI and DO interfaces. All bits in the DIOConfig register are set to 0 at power-up.

BIT	NAME	DESCRIPTION
D7	DoInv	**DO Output Polarity.** Set the DoInv bit to 1 to invert the logic of the DO output. This bit also works in conjunction with the DoAv (Table 6). DO tracks the TX input with the opposite polarity when both the DoAv and DoInv bits are set.
D6	DoAv	**DO Antivalent Operation.** Set the DoAv bit to 1 to enable antivalent output operation on DO. DO tracks the TX input (and the Q bit) when DoAv is 1 (Table 6). The LO input and the DoBit are ignored when the DoAv bit is 1.
D5	DoN/P	**DO Driver NPN/PNP Operation.** The DoN/P bit selects between low-side (NPN) and high-side (PNP) modes when the DO driver is configured as an open-drain output (DoPP = 0). Set DoN/P to 1 to configure the driver for low-side (NPN) operation. Set DoN/P to 0 for high-side (PNP) operation.
D4	DoPP	**DO Driver Push-Pull Operation.** Set the DoPP bit to 1 to configure the DO driver output for push-pull operation. DO is an open-drain output when DoPP is 0.
D3	DoEn	**DO Driver Enable/Disable.** Set the DoEn bit to 1 to enable the DO driver. The DO driver is high-impedance with a weak pulldown when DoEn is 0.
D2	DoBit	**DO Driver Output Logic.** The DoBit bit can be used to program the DO output driver through software. Drive LO high to activate DoBit programming (Figure 10). The DO output state is given in Table 7. Note that Table 7 assumes that the DoInv bit is 0.
D1	LiDis	**LI Output Enable/Disable.** Set the LiDis bit to 1 to disable the LI output. The LI output is low when LiDis is 1.
D0	—	This bit is not used.

Table 7. DoAv and DoInv Operation

DoAv	DoInv	TX (NOTE 1)	LO (NOTE 1)	DO (NOTE 2)	C/Q (NOTE 2)
0	0	Low	Low	High	High
0	0	Low	High	Low	High
0	0	High	Low	High	Low
0	0	High	High	Low	Low
0	1	Low	Low	Low	High
0	1	Low	High	High	High
0	1	High	Low	Low	Low
0	1	High	High	High	Low
1	0	Low	Low	Low	High
1	0	Low	High	Low	High
1	0	High	Low	High	Low
1	0	High	High	High	Low
1	1	Low	Low	High	High
1	1	Low	High	High	High
1	1	High	Low	Low	Low
1	1	High	High	Low	Low

Note 1: *Low is when V_{TX} or V_{LO} = 0V; high is when V_{TX} or V_{LO} = V_L.*
Note 2: *Low is when C/Q or DO < 8V; high is when C/Q or DO >13V.*

Table 8. DO Output Programmed by DoBit

LO	DoBit	DoPP	DoN/P	DO CONFIGURATION	DO STATE
High	0	1	X	Push-pull	Low
High	1	1	X	Push-pull	High
High	0	0	0	PNP	Off, DO is high-impedance
High	1	0	0	PNP	On, DO is high
High	0	0	1	NPN	On, DO is low
High	1	0	1	NPN	Off, DO is high-impedance
Low	X	X	X	See Table 6	See Table 6

X = Don't care.

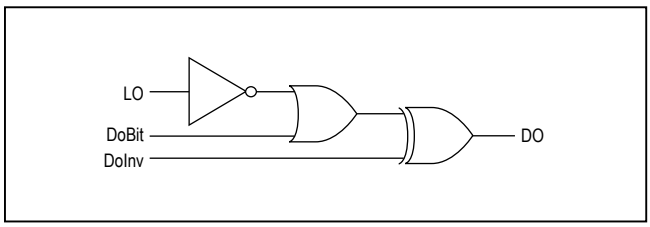

Figure 11. Equivalent DO Logic

Mode Register [R1, R0] = [1,1]

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	RST	WuIntEn	DoFault	C/QFault	UV24	OTemp	UV33En	LDO33Dis
Read/Write	R/W	R/W	R	R	R	R	R	R/W
POR State	0	0	0	0	0	0	0	0
Parallel Pin Configuration (SPI/$\overline{\text{PAR}}$ is low)	0	0	$\overline{\text{DOOC}}$ asserts when DoFault is set	$\overline{\text{CQOC}}$ asserts when C/QFault is set	UV asserts when UV24 is set	0	0	0

X = Unknown.

Use the Mode register to reset the MAX14826 and manage the 3.3V LDO. The Mode register has bits that represent the current status of fault conditions. When writing to the Mode register, the contents of the fault indication bits (bits 2 to 5) do not change.

BIT	NAME	DESCRIPTION
D7	RST	**Register Reset.** Set RST to 1 to reset all registers to their default power-up state. Then set RST to 0 for normal operation. The Status register is cleared and $\overline{\text{IRQ}}$/$\overline{\text{CQOC}}$ deasserts (if asserted) when RST = 1. Interrupts are not generated while RST = 1.
D6	WuIntEn	**Wake-Up Interrupt Enable.** Set WuIntEn to 1 to enable wake-up interrupt generation. When WuIntEn is set, the WuInt bit in the Status register is set and $\overline{\text{IRQ}}$/$\overline{\text{CQOC}}$ asserts when a valid wake-up condition is detected. The C/Q driver must be enabled for wake-up detection. The state of WuIntEn does not affect the $\overline{\text{WU}}$/$\overline{\text{THSD}}$ output. See the *Wake-Up Detection* section for more information.
D5	DoFault	**DO Fault Status.** The DoFault bit is set when a short circuit or voltage fault occurs at the DO driver output (see the *DO Fault Detection* section for more information). The DoFault and DoFaultInt bits are both set when a fault occurs on DO. DoFault is cleared when the fault is removed.
D4	C/QFault	**C/Q Fault Status.** The C/QFault bit is set when a short circuit or voltage fault occurs at the C/Q driver output (see the *C/Q Fault Detection* section for more information). The C/QFault and C/QFaultInt bits are both set when a fault occurs on C/Q. C/QFault is cleared when the fault is removed.
D3	UV24	**V_{CC} Undervoltage Condition.** Both the UV24 and the UV24Int bits are set when V_{CC} falls below V_{CCUVLO}. UV24 is cleared when V_{CC} rises above the V_{CC} threshold. V_5 must be present for SPI V_{CC} undervoltage monitoring.
D2	OTemp	**Temperature Warning.** The OTemp bit is set when a high-temperature condition occurs on the devices. Both the OTempInt interrupt in the Status register and the OTemp bit are set when the junction temperature of the die rises to above +127°C (typ). The OTemp bit is cleared when the junction temperature falls below +104°C (typ).
D1	UV33En	**LDO33 UV Enable.** Set the UV33En bit to 1 to assert the UV output when LDO33 voltage falls below the 2.4V (typ) undervoltage lockout threshold. The UV33En bit does not affect the UV33Int bit in the Status register; $\overline{\text{IRQ}}$/$\overline{\text{CQOC}}$ asserts when V_{LDO33} falls below $V_{LDO33UVLO}$ regardless of the state of UV33En.
D0	LDO33Dis	**LDO33 Enable/Disable.** Set LDO33Dis to 1 to disable the 3.3V linear regulator (LDO33).

SPI Interface

The device communicates through an SPI-compatible 4-wire serial interface when SPI/$\overline{PAR}$ is high. The interface has three inputs—clock (SCLK/CQPP), chip select ($\overline{CS}$/PNP), and data in (SDI/DOPP)—and one data out (SDO/$\overline{DOOC}$). The maximum SPI clock rate for the device is 12MHz. The SPI interface complies with clock polarity CPOL = 0 and clock phase CPHA = 0 (see Figure 12 and Figure 13).

The SPI interface is not available when V_5 or V_L are not present.

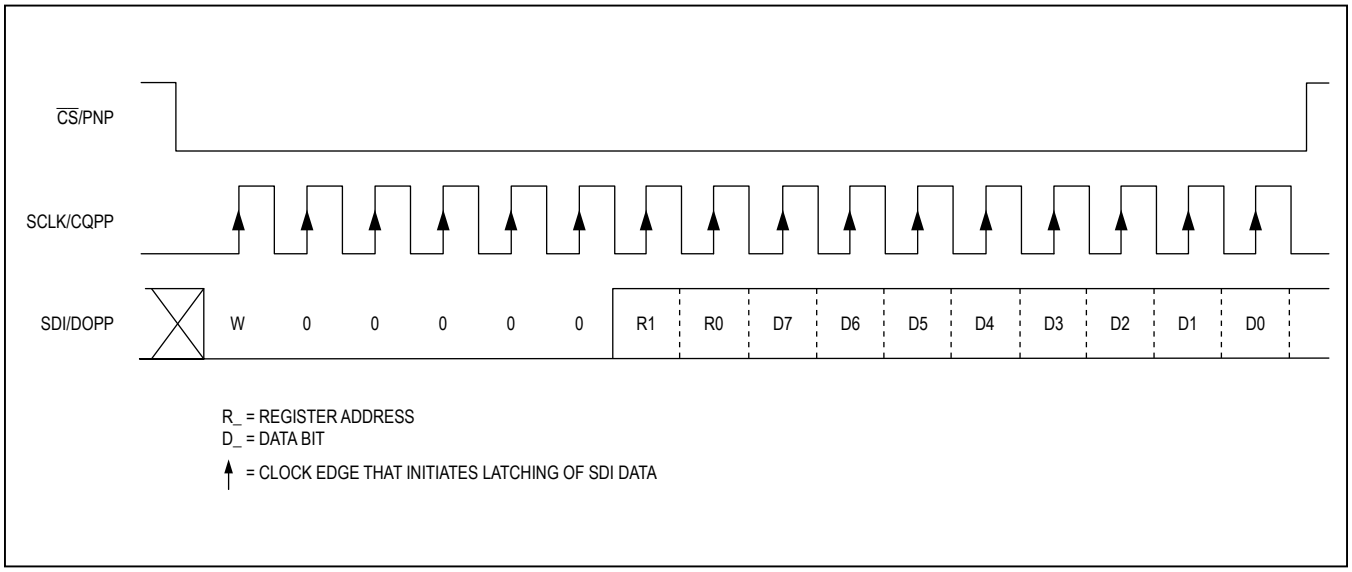

Figure 12. SPI Write Cycle

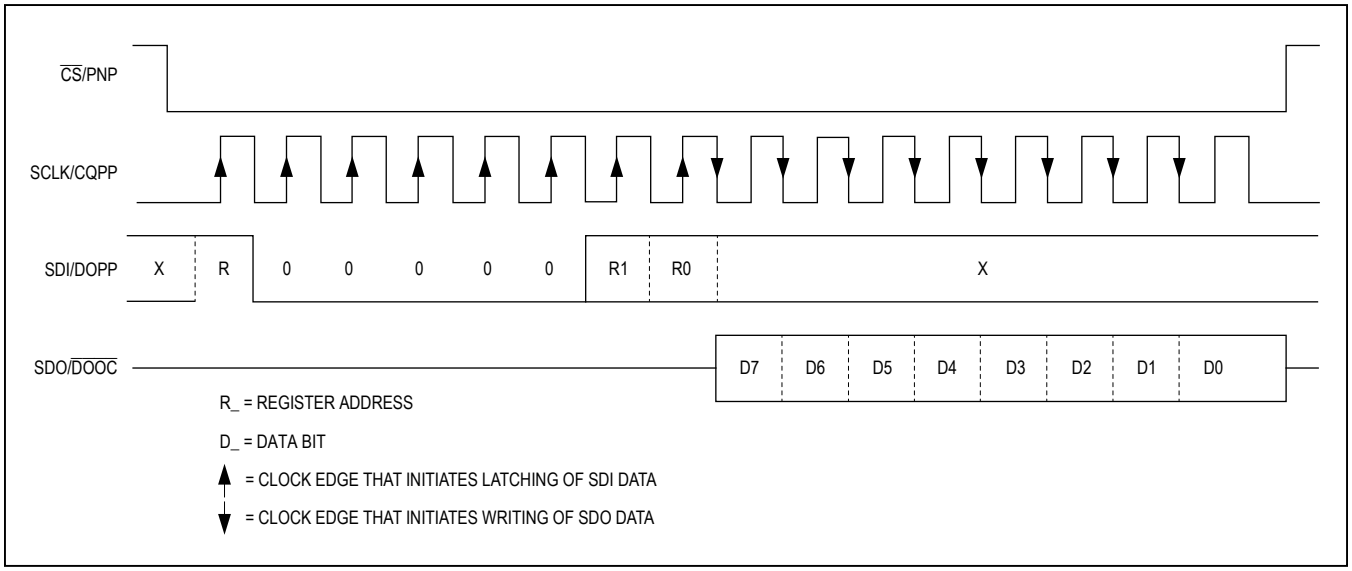

Figure 13. SPI Write Cycle

Applications Information

Transient Protection

Inductive load-switching, surges, and bursts create high transient voltages. C/Q, DO, and DI should be protected against high overvoltage and undervoltage transients. Positive voltage transients on C/Q, DO, and DI must be limited to +55V relative to GND and negative voltage transients must be limited to -55V (relative to V_{CC}) on DO and C/Q and to -55V (relative to GND) on DI. Figure 14 shows suitable protection using TVS diodes to meet both the IEC 61000-4-2 ESD and IEC 61000-4-4 burst testing. Other protection schemes may also be suitable.

The V_{CC} and LDOIN must be protected against transients that occur during hot-plugging of the L+ sensor supply (V_{CC}). To protect the device, place a 10Ω resistor and 1µF capacitor before LDOIN and connect an RC between the sensor supply into and V_{CC}, as shown in Figure 8. Ensure that the RC time constant of the filter on V_{CC} is at least 0.8µs.

Optional External Powering

The MAX14826 is powered by V_{CC} and V_5. V_L is a reference voltage input to set the logic levels of the microcontroller interface. The logic and SPI interface are operational when V_5 and V_L are present even if V_{CC} is not present.

The V_P output provides a reverse-polarity-protected voltage one diode drop below V_{CC} and can be used for supplying external circuitry, like power supplies. The current drawn from V_P cannot exceed 50mA. Be aware that capacitance on V_P can cause transient currents at power-up equal to C x dV_{CC}/dt.

V_5 is typically powered by the internal 5V regulator, but can alternatively be powered by an external 5V regulator. When powering V_5 externally, connect LDOIN to V_5. (Figure 15). This configuration disables operation of the internal 5V regulator and reduces power consumption.

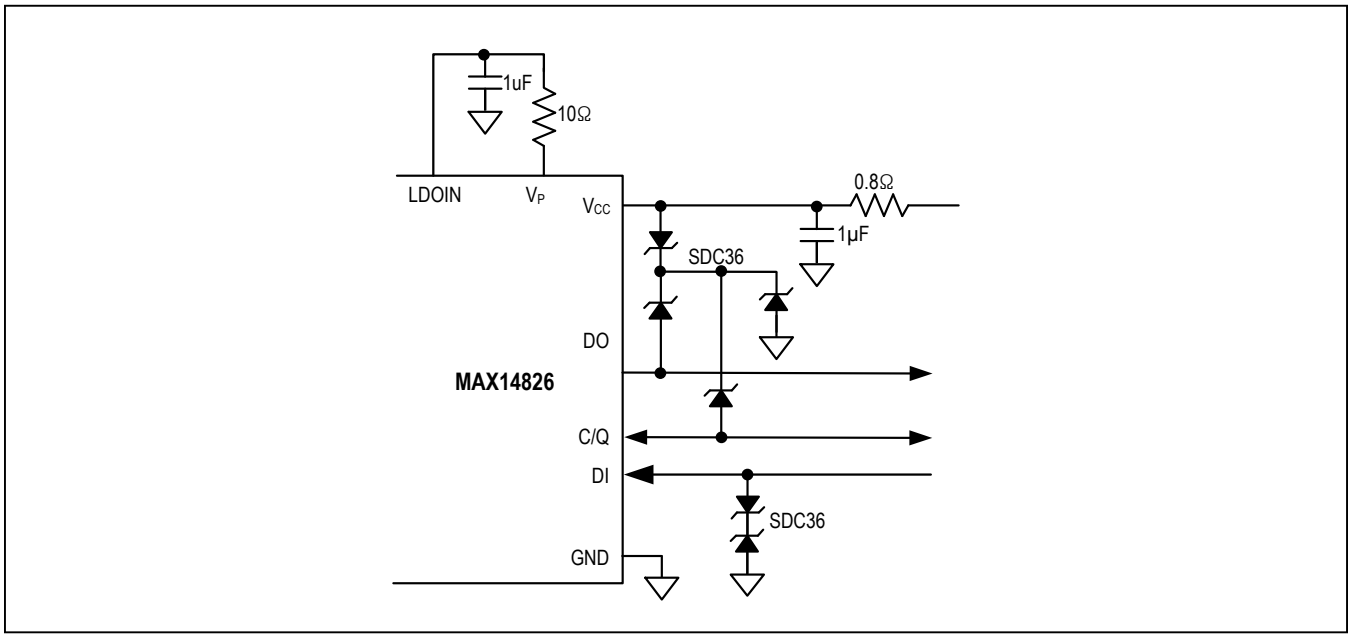

Figure 14. MAX14826 Operating Circuit with TVS Protection

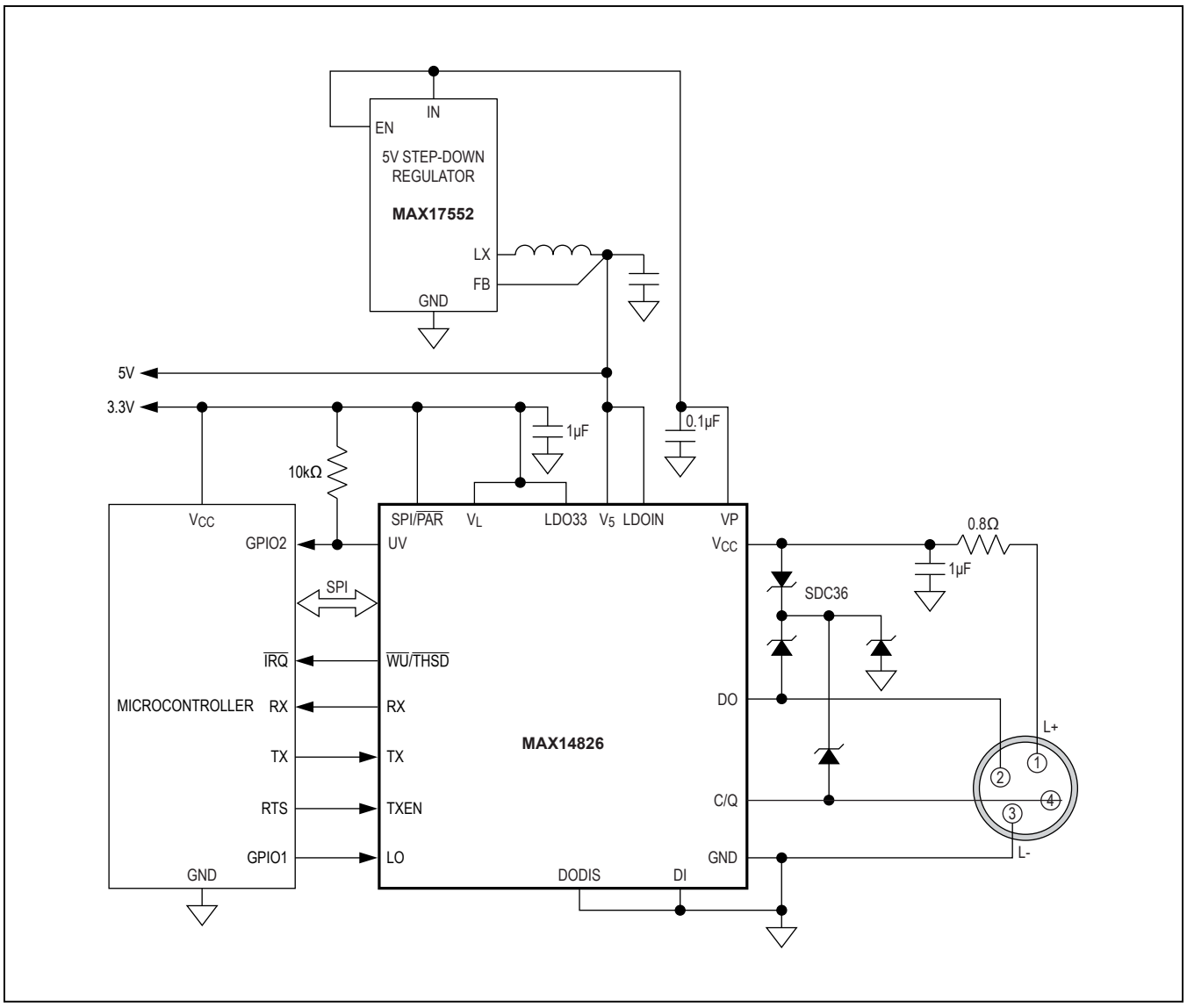

Figure 15. Using an Optional External Supply to Power the MAX14826

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14826GTG+	-40°C to +105°C	24 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 TQFN-EP	T2444+4	21-0139	90-0022

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/14	Initial release	—
1	4/16	Updated WU pin references in *Functional Diagram*, *Typical Operating Characteristics,* and text	2, 13, 19-20

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