



# THE DATASHEET OF MAX1664CUP





# Active-Matrix Liquid Crystal Display (AMLCD) Supply

## ABSOLUTE MAXIMUM RATINGS

RDY, IN, BPV <sub>DD</sub> to GND	-0.3V to +6V	RDY Sink Current	20mA
FB2-, PGND1, PGND2 to GND	±0.3V	LX2P, LX2N Peak Switch Currents	±750mA
LX1 to PGND1	-0.3V to +6V	Continuous Power Dissipation (T <sub>A</sub> = +70°C)	
BPV <sub>SS</sub> to GND	-3.3V to +0.3V	20-Pin TSSOP (derate 7mW/°C above +70°C)	559mW
BPV <sub>DD</sub> to BPV <sub>SS</sub>	-0.3V to +6V	Operating Temperature Range	0°C to +70°C
BPDRV to BPV <sub>SS</sub>	-0.3V to (V <sub>BPVDD</sub> + 0.3V)	Junction Temperature	+150°C
LX2P to INP	-15V to +0.3V	Storage Temperature Range	-65°C to +160°C
LX2N to PGND2	-0.3V to +30V	Lead Temperature (soldering, 10sec)	+300°C
SHDN, INP, FB1, FB2+, REF, PLLC, BPCLK, FPLL to GND	-0.3V to (V <sub>IN</sub> + 0.3V)		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>IN</sub> = V<sub>INP</sub> = 3.3V, SHDN = IN, V<sub>BPVDD</sub> = 4V, V<sub>BPVSS</sub> = -1V, PGND1 = PGND2 = FPLL = GND, f<sub>BPCLK</sub> = 30kHz, T<sub>A</sub> = 0°C to +70°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Range	V <sub>IN</sub>		2.8		5.5	V
Undervoltage Lockout Threshold	V <sub>UVLO</sub>		2.5		2.8	V
Quiescent Current	I <sub>Q</sub>	V <sub>FB1+</sub> = V <sub>FB2+</sub> = 1.3V, V <sub>FB2-</sub> = -0.1V; I <sub>IN</sub> + I <sub>INP</sub>		0.5	2	mA
Shutdown Current	I <sub>SD</sub>	SHDN = GND, V <sub>IN</sub> = 5.5V; I <sub>IN</sub> + I <sub>INP</sub>		0.01	10	μA
<b>DC-DC 1 (PWM MAIN OUTPUT)</b>						
Output Voltage Range	V <sub>OUT1</sub>		V <sub>IN</sub>		5.5	V
Operating Frequency	f <sub>OP1</sub>	FPLL = GND		32 x f <sub>BPCLK</sub>		Hz
		FPLL = REF		24 x f <sub>BPCLK</sub>		
		FPLL = IN		16 x f <sub>BPCLK</sub>		
FB1 Regulation Voltage	V <sub>FB1</sub>	0 < I <sub>LX1</sub> < 1.2A	1.2125	1.2500	1.275	V
FB1 Input Bias Current	I <sub>FB1</sub>	V <sub>FB1</sub> = 1.3V			100	nA
LX1 On Resistance	R <sub>ON(LX1)</sub>			0.25	0.5	Ω
LX1 Leakage Current	I <sub>LKG(LX1)</sub>	V <sub>LX1</sub> = 6V		0.1	10	μA
LX1 Peak Current Limit	I <sub>LIM(LX1)</sub>		1.2	1.5	1.8	A
Power-Ready Trip Level	V <sub>TH_RDY</sub>	Rising edge, 2% hysteresis	1.091	1.125	1.159	V
<b>DC-DC 2 (PFM)</b>						
Positive Output Voltage Range	V <sub>OUT2+</sub>		V <sub>IN</sub>		28	V
Negative Output Voltage Range	V <sub>OUT2-</sub>		-10		0	V
Maximum Operating Frequency	f <sub>OP2(MAX)</sub>	FPLL = GND		16 x f <sub>BPCLK</sub>		Hz
		FPLL = REF		12 x f <sub>BPCLK</sub>		
		FPLL = IN		8 x f <sub>BPCLK</sub>		

# Active-Matrix Liquid Crystal Display (AMLCD) Supply

MAX1664

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{IN} = V_{INP} = 3.3V$ ,  $\overline{SHDN} = IN$ ,  $V_{BPVDD} = 4V$ ,  $V_{BPVSS} = -1V$ ,  $PGND1 = PGND2 = FPLL = GND$ ,  $f_{BPCLK} = 30kHz$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .)

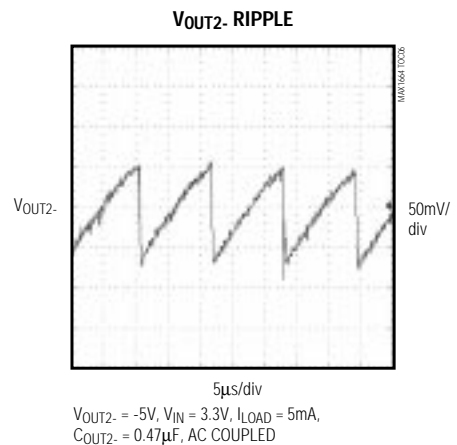
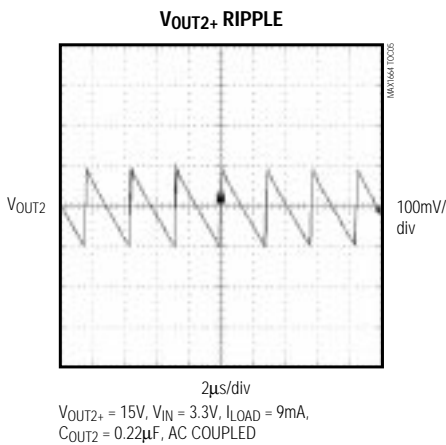
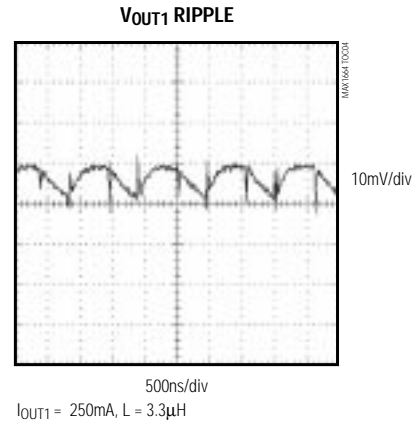
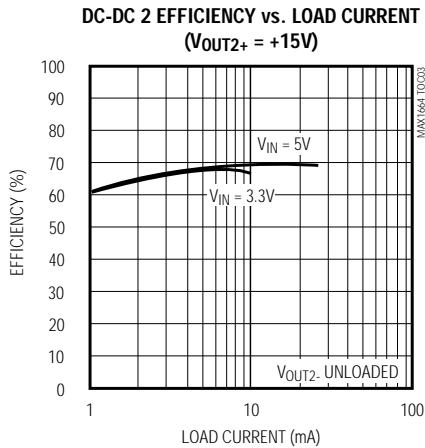
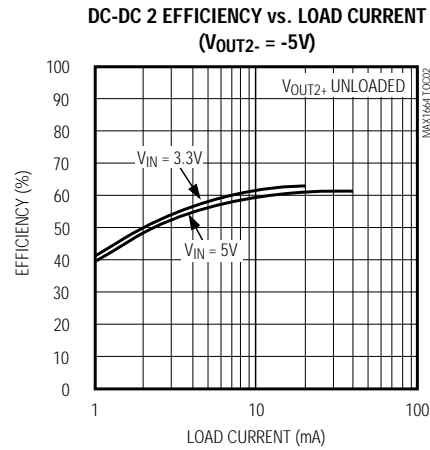
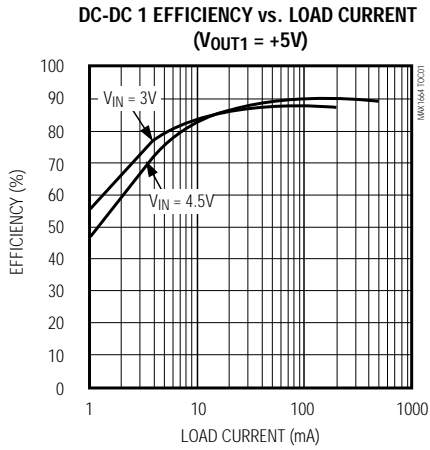
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FB2+ Regulation Voltage	$V_{FB2+}$		1.225	1.25	1.275	V
FB2- Regulation Voltage	$V_{FB2-}$		-15	0	15	mV
FB2+, FB2- Input Bias Current	$I_{FB2+}$ , $I_{FB2-}$	$V_{FB2+} = 1.3V$ , $V_{FB2-} = -0.1V$	-100		100	nA
LX2N, LX2P On-Resistance	$R_{ON(LX2N)}$ , $R_{ON(LX2P)}$			0.9	1.7	$\Omega$
LX2N, LX2P Leakage Current	$I_{LKG(LX2N)}$ , $I_{LKG(LX2P)}$	$V_{LX2N} = 28V$ , $V_{LX2P} = -10V$		0.05	10	$\mu A$
FB2- Power-Ready Trip Level	$V_{TH(RDY)}$	Falling edge, 40mV hysteresis	85	120	165	mV
FB2+ Power-Ready Trip Level	$V_{TH(RDY)}$	Rising edge, 40mV hysteresis	1.091	1.125	1.159	V
<b>BACKPLANE DRIVER</b>						
BPVDD Supply Range	$V_{BPVDD}$		2.5		5.5	V
BPVSS Supply Range	$V_{BPVSS}$		-3		0	V
BPVDD to BPVSS Voltage Range	$V_{VDD}$ to $V_{SS}$		2.5		5.5	V
BPVDD Shutdown Current	$I_{SHDN(BP)}$	$\overline{SHDN} = GND$		0.1	10	$\mu A$
BPDRV On-Resistance	$R_{ON(BPDRV)}$	Source and sink		0.35	0.7	$\Omega$
BPDRV Leakage Current	$I_{LKG(BPDRV)}$	$\overline{SHDN} = GND$	-10		10	$\mu A$
BPVDD Supply Current	$I_{IN(BPVDD)}$	$V_{BPCLK} = 0$ or $3.3V$		80	200	$\mu A$
BPCLK Input Low Voltage	$V_{IL(BPCLK)}$				$0.3 \times V_{IN}$	V
BPCLK Input High Voltage	$V_{IH(BPCLK)}$		$0.7 \times V_{IN}$			V
BPCLK Input Current	$I_{IN(BPCLK)}$			0.01	1	$\mu A$
<b>PLL</b>						
VCO Center Frequency (Note 1)	$f_C$	PLL = REF, BPCLK = GND	1.63	1.92	2.20	MHz
BPCLK Input Frequency Range	$f_{BPCLK}$	$C_{PLL} = 22nF$ $R_{PLL} = 100k\Omega$ $C_{SHUNT} = 2.2nF$	FPLL = GND	20	36	kHz
			FPLL = REF	27	48	
			FPLL = IN	40	72	
Reference Voltage	$V_{REF}$	$-2\mu A < I_{REF} < 50\mu A$	1.225	1.250	1.275	V
Undervoltage Lockout	$V_{REF(UVLO)}$		0.90	1.05	1.20	V
<b>LOGIC SIGNALS</b>						
$\overline{SHDN}$ Input Low Voltage	$V_{IL(\overline{SHDN})}$	( $0.10 \times V_{IN}$ ) typical hysteresis			$0.3 \times V_{IN}$	V
$\overline{SHDN}$ Input High Voltage	$V_{IH(\overline{SHDN})}$		$0.7 \times V_{IN}$			V
$\overline{SHDN}$ Input Current	$I_{IN(\overline{SHDN})}$			0.01	1	$\mu A$
FPLL Input Current	$I_{IN(FPLL)}$	FPLL = GND or IN		0.01	1	$\mu A$
RDY Output Low Voltage	$V_{OL(RDY)}$	$I_{SINK} = 2mA$		0.05	0.4	V
RDY Output High Leakage	$I_{LKG(RDYOH)}$	$V_{RDY} = 5.5V$		0.01	1	$\mu A$

**Note 1:** DC-DC 1 operates at one-half of the  $V_{CO}$  frequency ( $f_C / 2$ ).

# Active-Matrix Liquid Crystal Display (AMLCD) Supply

## Typical Operating Characteristics

(f<sub>BPCLK</sub> = 22.5kHz, F<sub>PLL</sub> = GND, L<sub>1</sub> = 3.3μH, L<sub>2</sub> = 4.7μH, T<sub>A</sub> = +25°C, unless otherwise noted.)



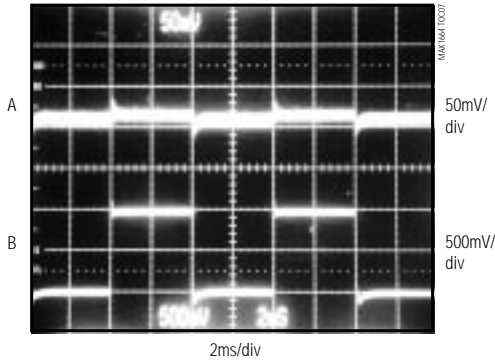
# Active-Matrix Liquid Crystal Display (AMLCD) Supply

MAX1664

## Typical Operating Characteristics (continued)

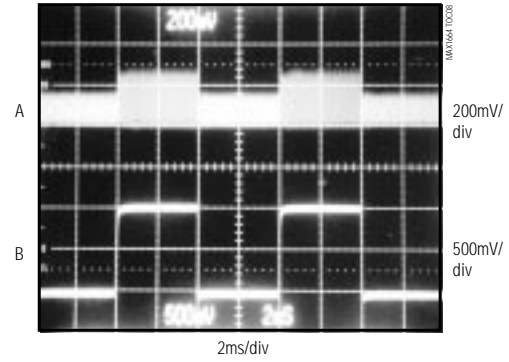
( $f_{BPCLK} = 22.5\text{kHz}$ ,  $FPLL = \text{GND}$ ,  $L1 = 3.3\mu\text{H}$ ,  $L2 = 4.7\mu\text{H}$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

**V<sub>OUT1</sub> LINE-TRANSIENT RESPONSE**



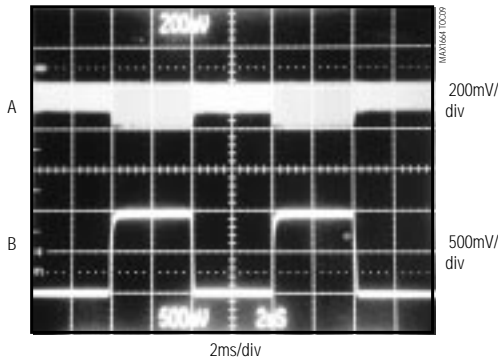
$V_{OUT1} = 5\text{V}$ ,  $I_{LOAD} = 250\text{mA}$ ,  $C_{OUT1} = 20\mu\text{F}$   
 A:  $V_{OUT1}$ , 50mV/div, AC COUPLED  
 B:  $V_{IN}$ , 3V to 4V

**V<sub>OUT2+</sub> LINE-TRANSIENT RESPONSE**



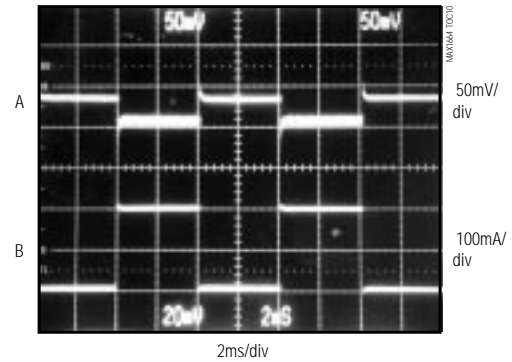
$V_{OUT2+} = 15\text{V}$ ,  $I_{LOAD} = 5\text{mA}$ ,  $C_{OUT2+} = 0.22\mu\text{F}$   
 A:  $V_{OUT2+}$ , 200mV/div, AC COUPLED  
 B:  $V_{IN}$ , 3V to 4V

**V<sub>OUT2-</sub> LINE-TRANSIENT RESPONSE**



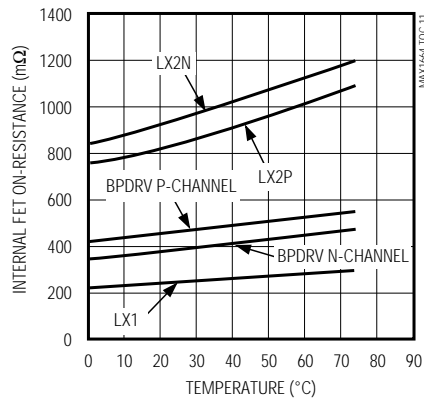
$V_{OUT2-} = -5\text{V}$ ,  $I_{LOAD} = 5\text{mA}$ ,  $C_{OUT2-} = 0.47\mu\text{F}$   
 A:  $V_{OUT2-}$ , 200mV/div, AC COUPLED  
 B:  $V_{IN}$ , 3V to 4V

**V<sub>OUT1</sub> LOAD-TRANSIENT RESPONSE**

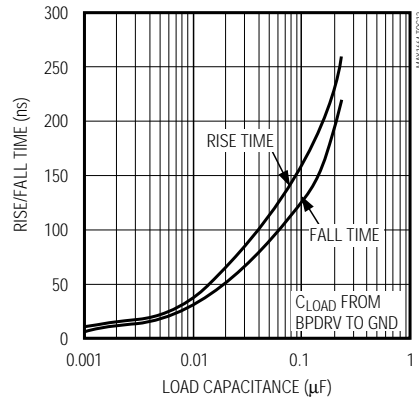


$V_{OUT1} = 5\text{V}$ ,  $V_{IN} = 3.3\text{V}$ ,  $C_{OUT1} = 20\mu\text{F}$   
 A:  $V_{OUT1}$ , 50mV/div, AC COUPLED  
 B:  $I_{OUT1}$ , 25mA TO 225mA, 100mA/div

**INTERNAL FET ON-RESISTANCE vs. TEMPERATURE**



**BPDRV RISE AND FALL TIME vs. LOAD CAPACITANCE**

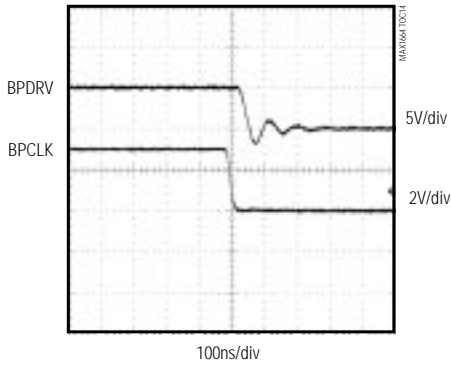


# Active-Matrix Liquid Crystal Display (AMLCD) Supply

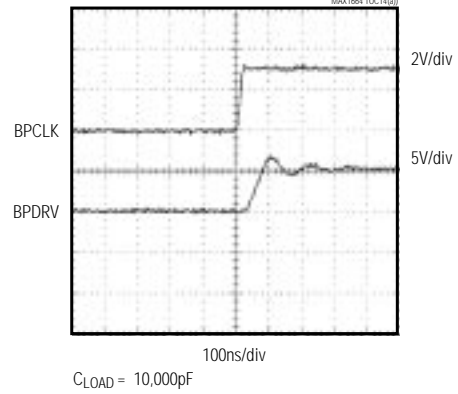
## Typical Operating Characteristics (continued)

( $f_{BPCLK} = 22.5\text{kHz}$ ,  $FPLL = \text{GND}$ ,  $L1 = 3.3\mu\text{H}$ ,  $L2 = 4.7\mu\text{H}$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

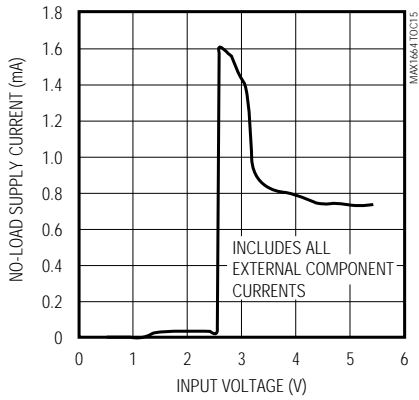
**BPCLK TO BPDRV FALLING DELAY**



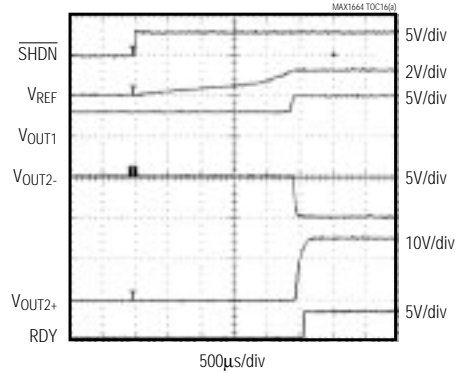
**BPCLK TO BPDRV RISING DELAY**



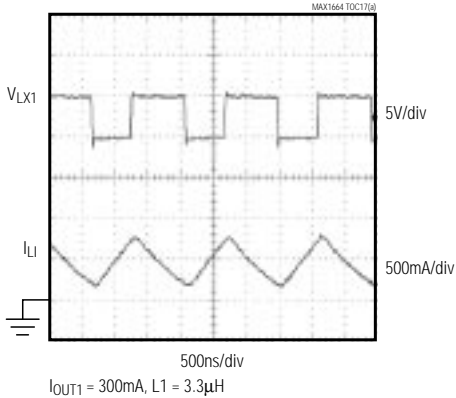
**NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE**



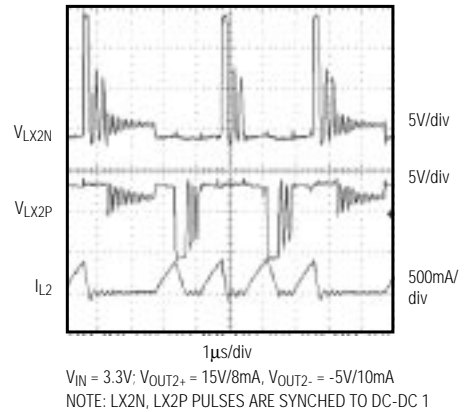
**OUT-OF-SHUTDOWN SEQUENCE**



**DC-DC 1 SWITCHING WAVEFORMS**



**DC-DC 2 SWITCHING WAVEFORMS DISCONTINUOUS CONDUCTION**



# Active-Matrix Liquid Crystal Display (AMLCD) Supply

## Pin Description

MAX1664

PIN	NAME	FUNCTION
1	$\overline{\text{SHDN}}$	Shutdown Input. Drive low to enter shutdown mode. Drive high or connect to IN for normal operation. All IC sections are off when $\overline{\text{SHDN}}$ is low.
2	RDY	Ready Indicator Output, DC-DC 1 and DC-DC 2. Open-drain N-channel output becomes high impedance when all three outputs are within 10% of regulation.
3	FB1	Regulator Feedback Input, DC-DC 1. Regulates to 1.25V nominal.
4	REF	Internal Reference Output. Connect a 0.22 $\mu$ F capacitor from this pin to GND. REF can source up to 50 $\mu$ A.
5	GND	Analog Ground. Connect to PGND1 and PGND2. See <i>Supply Connections and Layout</i> section.
6	IN	Supply Input to the IC. The input voltage range is +2.8V to +5.5V.
7	FB2-	Regulator Feedback Input for Negative Output, DC-DC 2. Regulates to 0V nominal.
8	FB2+	Regulator Feedback Input for Positive Output, DC-DC 2. Regulates to 1.25V nominal.
9	PLLC	PLL Compensation. Connect compensation network as in Figure 4.
10	BPVSS	Backplane Driver Negative Supply. Typically connected to PGND1. May be connected to a separate supply.
11	BPDRV	Backplane Driver Output
12	BPVDD	Backplane Driver Positive Supply. Typically connected to V <sub>OUT1</sub> of DC-DC 1. May be connected to a separate supply.
13	BPCLK	Backplane Driver Clock Input. See Table 1 for input frequency ranges.
14	INP	DC-DC 2 Power Input. Source of Internal LX2P P-channel MOSFET.
15	LX2P	Drain of Internal LX2P P-Channel MOSFET
16	LX2N	Drain of Internal LX2N N-Channel MOSFET
17	PGND2	Power Ground 2. Connect to PGND1. Source of internal LX2N N-channel MOSFET.
18	PGND1	Power Ground 1. Connect to PGND2. Source of internal LX1 N-channel MOSFET.
19	LX1	Drain of Internal LX1 N-Channel MOSFET
20	FPLL	Sets the BPCLK input frequency range for PLL synchronization. Connect to GND, REF, or IN. See Table 1.

# Active-Matrix Liquid Crystal Display (AMLCD) Supply

MAX1664

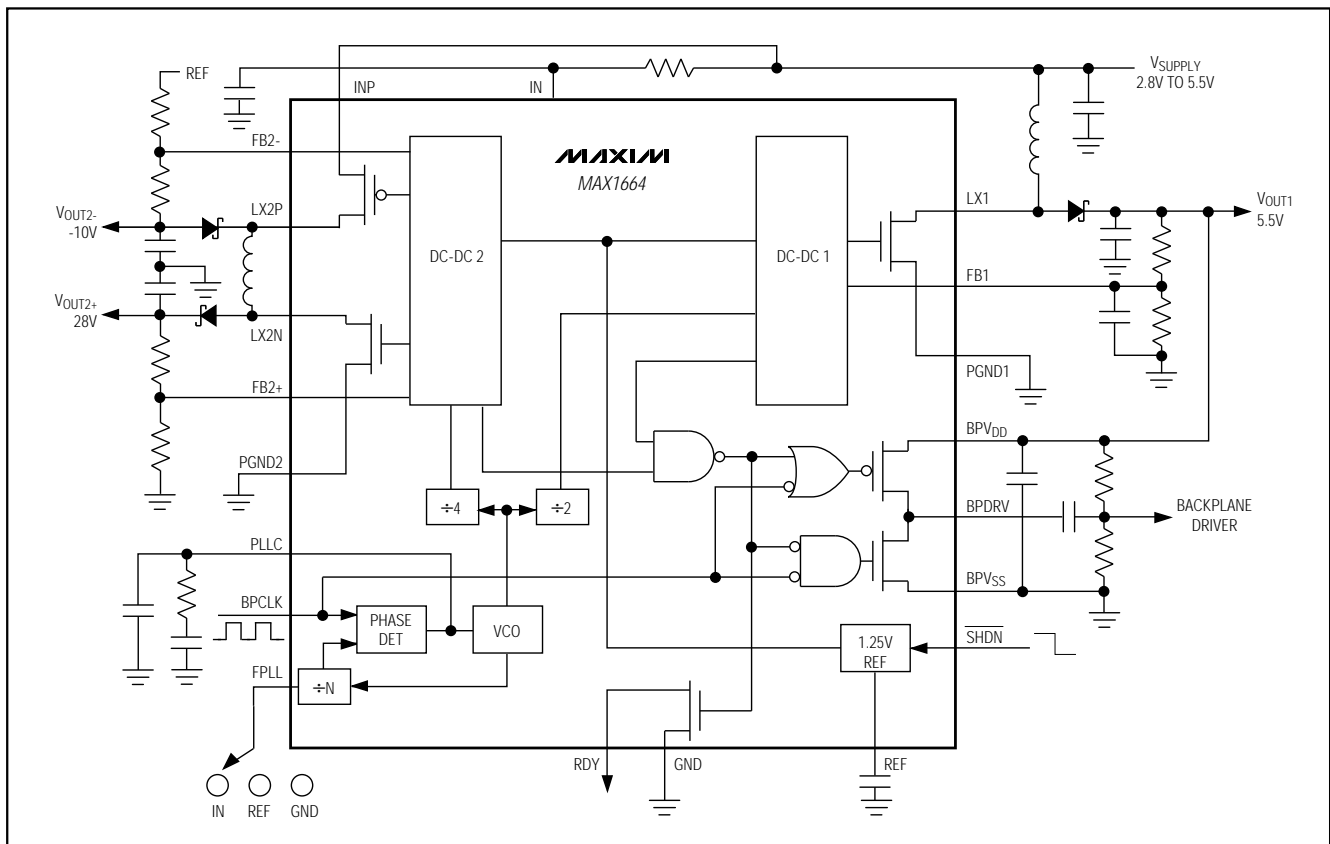


Figure 1. Functional Diagram

## Detailed Description

The MAX1664 combines power supply and backplane drive circuitry for active matrix thin-film-transistor (TFT) liquid crystal displays (LCD) into one IC. Included are a pulse-width-modulation (PWM) boost converter, a dual-output (positive and negative) converter using one inductor, an LCD backplane driver, and a phase-locked loop (PLL) to synchronize all three outputs to the backplane clock.

A high switching frequency (1MHz nominal) and phase-locked operation allow the use of small, minimum-height external components while maintaining low output noise. Output voltages are adjustable to +5.5V (DC-DC 1) and to +28V and -10V (DC-DC 2). The negative output voltage can be set to as low as -20V with additional components.

The frequency ratio between the DC-DC 1 converter and the backplane clock can be set to 16, 24, or 32. This flexibility allows high DC-DC converter frequencies

to be used with LCD backplane clock rates ranging from 20kHz to 72kHz.

### Start-Up

At start-up, both converters remain disabled until  $V_{REF}$  reaches 90% of its nominal value.  $V_{OUT1}$  is activated first. Once  $V_{OUT1}$  is regulated,  $V_{OUT2-}$  is enabled.  $V_{OUT2+}$  is held at 0 until  $V_{OUT2-}$  is within 90% of its regulation target. All three outputs power up in a similar order when power is applied or when coming out of shutdown. See the Out-of-Shutdown Sequence photo in the *Typical Operating Characteristics* section.

### DC-DC 1 Boost Converter

DC-DC 1 uses a current-mode boost PWM architecture to produce a positive regulated voltage, adjustable from 3V to 5.5V (but not less than  $V_{IN}$ ). This converter uses an internal N-channel MOSFET with a maximum on-resistance of  $0.5\Omega$ . Cycle-by-cycle peak current limiting protects the switch under fault conditions. Upon start-up, DC-DC 1 is the first converter to be enabled.

# Active-Matrix Liquid Crystal Display (AMLCD) Supply

**Table 1. Switching Frequency Options**

FPLL	f <sub>BPCLK</sub> (kHz)	f <sub>DC-DC 1</sub> (kHz)	f <sub>DC-DC 2 MAX</sub> (kHz)	f <sub>DC-DC 1</sub> : f <sub>BPCLK</sub>	f <sub>DC-DC 2 MAX</sub> : f <sub>BPCLK</sub>	N*
IN	40 to 72	640 to 1152	320 to 576	16:1	8:1	32
REF	27 to 48	640 to 1152	320 to 576	24:1	12:1	48
GND	20 to 36	640 to 1152	320 to 576	32:1	16:1	64

\*See Figure 2

Fixed-frequency, current-mode operation ensures that the switching noise exists only at the operating frequency and its harmonics. The switching frequency is phase locked to the backplane clock input. Table 1 illustrates the possible switching-frequency options.

### DC-DC 2 Dual Outputs

DC-DC 2 uses a synchronized, fixed on-time PFM architecture to provide the positive and negative output voltages that allow the driver ICs to turn the TFT gates on and off. When pulses occur, they are synchronized to DC-DC 1, thereby minimizing converter interactions and subharmonic interference.

The DC-DC 2 inductor current is always discontinuous, enabling the dual outputs to be regulated independently. This allows one output to be at 100% load while the other is at no load.

### DC-DC 2 Operation

In normal operation, DC-DC 2 alternates between charging the negative and positive outputs (Figure 1). During the first half-cycle of the PFM clock period, both the N-channel and P-channel MOSFETs turn on, applying the input supply across inductor L2. This causes the inductor current to ramp up at a rate proportional to  $V_{INP}$ . During the second half-cycle, the P-channel MOSFET turns off and the inductor transfers its energy into the negative output filter capacitor.

Assuming that the energy transfer is completed during this second half-cycle and the inductor current ramps down to zero, the process is repeated for the positive output during the next clock cycle. During the first half of the second clock cycle, both the N-channel and P-channel MOSFETs turn on again. The current in the inductor again rises at the same rate. During the second half of the second clock cycle, the N-channel MOSFET is turned off and this time the inductor energy transfers to the positive output filter capacitor.

During conditions of heavy loads, DC-DC 2 will continue to operate in this manner, alternately delivering pulses to the negative and positive outputs. For lighter

loads, the controller may skip one or more cycles of either polarity, thereby keeping the outputs in regulation. See Table 1 for the relationship between the maximum DC-DC 2 pulse frequency and the backplane clock frequency.

### Outputs with Low Step-Up or Inversion Ratios

For DC-DC 2 output voltage setpoints, which require minimum step-up or inversion ratios (for example,  $V_{OUT+} < 6V$  or  $V_{OUT-} > -3V$ , when  $V_{INP} = 5V$ ), more than one half-cycle may be required to transfer the inductor energy to the appropriate output filter capacitor. In such cases, subsequent conversion cycles are delayed, as necessary, by one or more PFM clock cycles to preserve discontinuous mode operation.

### Backplane Driver

The MAX1664 provides a low-impedance backplane driver, as shown in Figure 1, that level-translates the BPCLK signal from a logic level to  $BPV_{DD}/BPV_{SS}$  levels. The backplane driver consists of an N-channel/P-channel complementary pair of high-current MOSFETs. These devices drive BPDRV to either  $BPV_{DD}$  or  $BPV_{SS}$  when BPCLK goes either high or low, respectively. The switches have a maximum on-resistance of  $0.7\Omega$  with a typical propagation delay of 50ns. Power for the backplane driver can be taken from the output of DC-DC 1,  $V_{OUT1}$ , as shown in the *Typical Operating Circuit*.

### Phase-Locked Loop

The MAX1664 contains an on-board PLL to synchronize the PWM and PFM converter clocks to the backplane clock (Figure 2). This will minimize noise and interference. The PLL is a frequency-multiplying type, generating a nominal 1MHz clock signal for DC-DC 1 and a nominal 500kHz clock for DC-DC 2. Three input frequency ranges, spanning 20kHz to 72kHz, permit synchronization over a broad range of backplane clock input frequencies while maintaining optimal conversion frequencies (Table 1).

# Active-Matrix Liquid Crystal Display (AMLCD) Supply

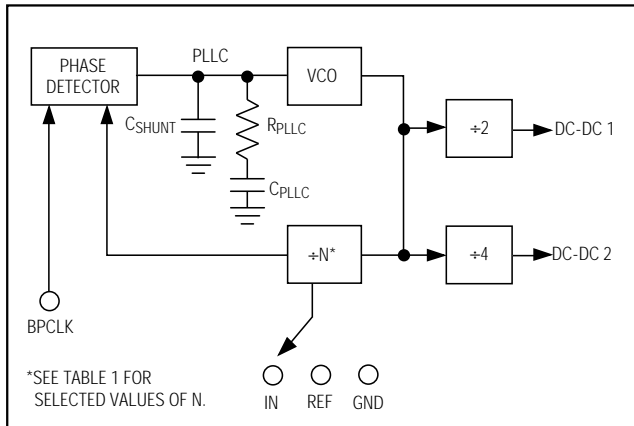


Figure 2. Internal PLL Operation within the MAX1664

The heart of the PLL is the VCO, which is trimmed to a nominal frequency of 1.92MHz for a control voltage (at the PLLC pin) of 1.250V. This high-frequency internal clock is divided digitally with a division ratio selected by pin-strapping FPLL to GND, REF, or IN. This divided clock is compared to the backplane clock by an internal phase comparator (rising-edge triggered). The phase detector in turn adjusts the VCO control voltage until the two frequencies (and phases) match. This feedback loop is compensated at the PLLC pin.

In some applications, the backplane clock may be halted for several cycles between screen scans or may not be immediately applied on power-up. The PLL contains a proprietary phase-detector architecture that minimizes frequency error during clock dropouts of more than two cycles and re-establishes lock immediately when the clock resumes.

### Ready Indicator (RDY)

The RDY pin has an open-drain output and indicates when all three outputs are in regulation. The open-drain output becomes high impedance when all three converter outputs are within 10% of their regulation setpoints.

## Design Procedure and Component Selection

### Output Voltage Selection

The three output voltages as well as the DC bias for the backplane clock are adjustable on the MAX1664, as shown in Figure 3. Set each output using two standard 1% resistors to form a voltage divider between the selected output and its respective feedback pin. Use the following equations to calculate the resistances.

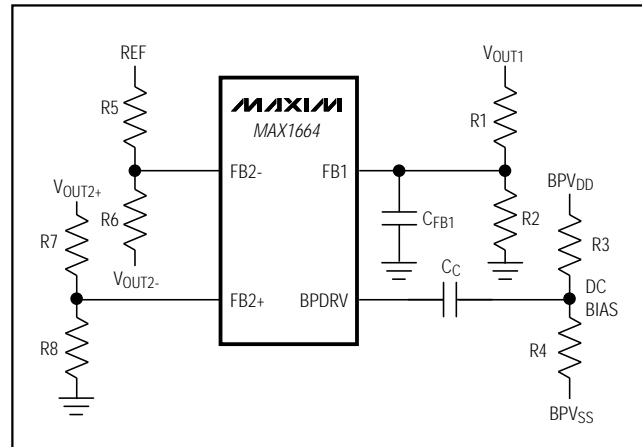


Figure 3. Output Voltage Selection

### DC-DC 1 Output

For  $V_{OUT1} = 5V$ , typical values are  $R2 = 100k\Omega$  and  $R1 = 301k\Omega$ . To set  $V_{OUT1}$  to another voltage, choose  $R2 = 100k\Omega$  and  $C_{FB1} = 50pF$ , and calculate  $R1$  as follows:

$$R1 = R2 \left( \frac{V_{OUT1}}{V_{FB1}} - 1 \right)$$

### DC-DC 2 Positive Output

For  $V_{OUT2+} = 15V$ , typical values are  $R8 = 49.9k\Omega$  and  $R7 = 549k\Omega$ . To set  $V_{OUT2+}$  to another voltage, choose  $R8 = 49.9k\Omega$  and calculate  $R7$  as follows:

$$R7 = R8 \left( \frac{V_{OUT2+}}{V_{FB2+}} - 1 \right)$$

### DC-DC 2 Negative Output

For the negative output voltage, the FB2- threshold voltage is 0. For  $V_{OUT2-} = -5V$ , typical values are  $R5 = 49.9k\Omega$  and  $R6 = 200k\Omega$ . To set  $V_{OUT2-}$  to another voltage, choose  $R5 = 49.9k\Omega$  and calculate  $R6$  as follows:

$$R6 = R5 \left| \frac{V_{OUT2-}}{V_{REF}} \right|$$

### DC Bias for the Backplane Driver

For  $V_{DCBIAS} = V_{BPVDD}/2$ , typical values are  $R3 = R4 = 100k\Omega$ . To set the DC bias to a different value, choose  $R4$  and calculate  $R3$  as follows:

$$R3 = R4 \left( \frac{V_{BPVDD} - V_{BPVSS}}{V_{DCBIAS} - V_{BPVSS}} - 1 \right)$$



# Active Matrix Liquid Crystal Display (AMLCD) Supply

**Table 2. Typical DC-DC 2 Operation**

V <sub>OUT2+</sub> (V)	V <sub>OUT2-</sub> (V)	V <sub>IN</sub> (V)	f <sub>BPCLK</sub> (kHz)	L <sub>2</sub> (μH)	I <sub>OUT2+(MAX)</sub> (mA)	I <sub>OUT2-(MAX)</sub> (mA)	f <sub>DC-DC 2(MAX)</sub> (kHz)	INDUCTOR PEAK CURRENT* (mA)
+15	-5	3.0	22.5	4.7	6	15	360	375
+15	-5	3.0	22.5	2.7	8	23	360	585
+15	-5	3.3	22.5	4.7	7	19	360	425
+15	-5	3.3	22.5	2.7	10	27	360	643
+15	-5	4.5	22.5	4.7	15	35	360	550
+15	-5	5.0	22.5	4.7	20	43	360	600
+20	-10	3.0	22.5	4.7	3	6	360	385
+20	-10	3.0	22.5	2.7	5	10	360	585
+20	-10	3.0	25.0	4.7	2	5	400	340
+20	-10	3.0	25.0	2.7	4	8	400	530
+20	-10	3.0	30.0	4.7	3	4	480	300
+20	-10	3.0	30.0	2.7	3	6	480	451
+20	-10	3.3	22.5	4.7	4	8	360	425
+20	-10	3.3	22.5	2.7	6	12	360	643
+20	-10	3.3	25.0	4.7	4	7	400	370
+20	-10	3.3	25.0	2.7	6	10	400	583
+20	-10	3.3	30.0	4.7	4	5	480	340
+20	-10	3.3	30.0	4.7	4	8	480	496
+20	-10	4.5	22.5	4.7	9	16	360	580
+20	-10	4.5	25.0	4.7	8	14	400	500
+20	-10	4.5	30.0	4.7	8	12	480	450
+20	-10	4.5	30.0	2.7	10	17	480	679
+20	-10	5.0	22.5	4.7	11	20	360	640
+20	-10	5.0	25.0	4.7	10	18	400	550
+20	-10	5.0	30.0	4.7	10	15	480	500

\*Note: Absolute maximum peak current at LX2P and LX2N is 750mA.

### Diode Selection

The MAX1664's high switching frequency requires fast diodes. Schottky diodes such as the MBR0520L and MBR0540L (Motorola) are recommended because they have the necessary power ratings in a low-height SOD-123 package. Also recommended is the MBRM5817 which is 1.1mm high. Use a Schottky diode with a forward current rating greater than:

$$I_F > \frac{I_{OUT} V_{OUT}}{0.9V_{IN}}$$

For the positive output of DC-DC 2, use a Schottky diode with a voltage rating that exceeds V<sub>OUT2+</sub>. For the negative output, use a Schottky diode with a rating

that exceeds V<sub>IN</sub> + |V<sub>OUT2-</sub>|. See Table 3 for more information on Schottky diode manufacturers.

### Filter Capacitor Selection

An output filter capacitor's ESR and size can greatly influence a switching converter's output ripple, as shown in the following equation.

$$V_{RIPPLE(PK-PK)} \cong I_{PEAK} \times R_{ESR} + I_{OUT} \left( \frac{t_{ON}}{C_{OUT}} \right)$$

$$DC-DC 1 t_{ON} = \frac{1}{f_{DC-DC 1}} \left( \frac{V_{OUT1} + V_F - V_{IN}}{V_{OUT1} + V_F} \right)$$

$$DC-DC 2 t_{ON} = \frac{1}{2 f_{DC-DC 1}}$$

# Active-Matrix Liquid Crystal Display (AMLCD) Supply

Ceramic capacitors are recommended because they have low ESR and the lowest profile. Typical ceramic capacitors are the C3225X5R series from TDK and JMK325 series from Taiyo Yuden. See Table 3 for more information on the manufacturers who provide surface-mount ceramic capacitors.

### PLL Compensation

In most applications, the recommended compensation component values shown in Figure 4 will give optimal system performance. If no backplane clock is used, connect PLLC to REF.

**Table 3. Component Manufacturers**

MANUFACTURER	PHONE	FAX
<b>INDUCTORS</b>		
Dale Inductors	(605) 668-4131	(605) 665-1627
Sumida USA	(847) 956-0666	(847) 956-0702
<b>DIODES</b>		
Central Semiconductor	(516) 435-1110	(516) 435-1824
International Rectifier	(310) 322-3331	(310) 322-3232
Motorola	(602) 303-5454	(602) 994-6430
<b>CERAMIC CAPACITORS</b>		
Marcon/United Chemicon	(847) 696-2000	(847) 696-9278
TDK	(847) 390-4373	(847) 390-4428
Taiyo Yuden	(408) 573-4150	(408) 573-4159
Vishay/Vitramon	(203) 268-6261	(203) 452-5670

## Applications Information

### Increasing $V_{OUT}$ Above 5.5V

For  $V_{OUT1}$  output voltages above 5.5V, connect the supplemental charge pump circuit shown in Figure 5. The connection shown supplies a 10V 150mA output, but other voltages from  $2 \times V_{IN}$  to 10V can be set by selecting the appropriate values for R1 and R2 (see *DC-DC 1 Output* section). C2–C4 are shown as parallel combinations of 3.3 $\mu$ F ceramic capacitors so that a 1.1mm height restriction can be met. If height is not restricted, then larger values can be used instead of parallel capacitor combinations.

### 3.3V to -20V Charge-Pump Configuration

For applications requiring negative voltages down to -20V, an inverting charge-pump block can be added to the  $V_{OUT2}$  output (Figure 6). Typical values for  $C_F$  and

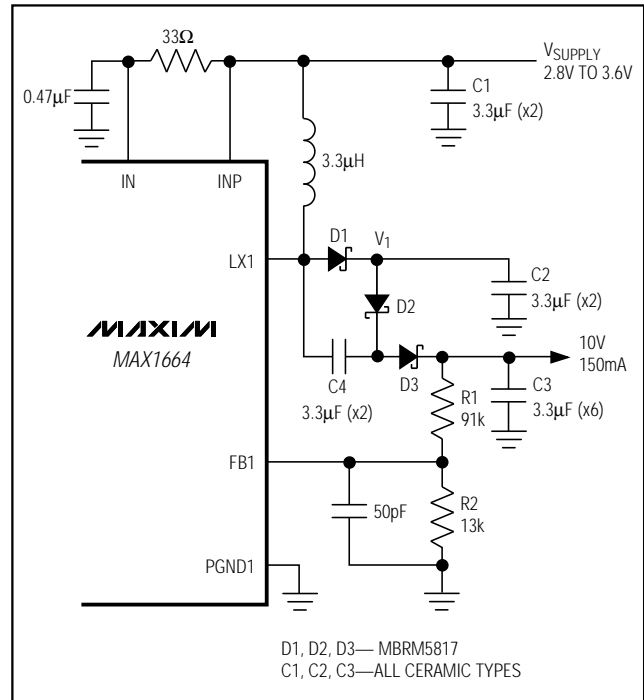


Figure 5. Charge Pump Configuration to Increase  $V_{OUT1}$  Above 5.5V.

$C_{OUT}$  are 0.47 $\mu$ F to 1 $\mu$ F and 4.7 $\mu$ F to 10 $\mu$ F, respectively. As a general rule,  $C_{OUT}$  should be ten times greater than  $C_F$ . This circuit operates as follows:

- 1) During the first PFM cycle, the voltage at V1 is charged by inductor L2 to some fraction of its final steady-state voltage, in the normal manner described in the *Detailed Description*.
- 2) During the first half of subsequent PFM cycles, pin LX2P is pulled to  $V_{INP}$ , and capacitor  $C_F$  is charged to  $(V_{INP} + |V_1| - V_D)$ , where  $V_D$  is a diode forward voltage.
- 3) During subsequent second half-cycles when LX2P flies negatively below V1, capacitor  $C_F$  transfers some of its energy to output capacitor  $C_{OUT}$ , which then is charged to a negative voltage of approximately  $(V_{INP} + 2 \times |V_1| - 2 \times V_D)$ .
- 4) This process continues until  $V_{OUT}$  reaches the desired voltage, as determined by the ratio of the FB2- feedback resistors.
- 5) During steady-state (in-regulation) operation, the magnitude of the voltage at LX2P is equal to  $(|V_{OUT}| / 2 - V_{INP} / 2 + V_D)$ , which must be limited to less than 10V.

# Active-Matrix Liquid Crystal Display (AMLCD) Supply

## Supply Connections and Layout

The MAX1664 performs both precision analog and high-power switching functions. Carefully plan supply connections, bypassing, and layout. Bypass IN and INP with a 33Ω isolation resistor (R9, Figure 4) between them. In addition, sufficient low-ESR bypassing must be provided on the INP bus to ensure stability of DC-DC 1.

A solid ground plane under the power components, with a separate ground plane under the analog nodes, is highly recommended. These ground planes should be connected at a single, quiet point. Analog reference and feedback signals should be referred to and routed over the analog ground plane. Figure 7 shows a typical layout using separate ground planes.

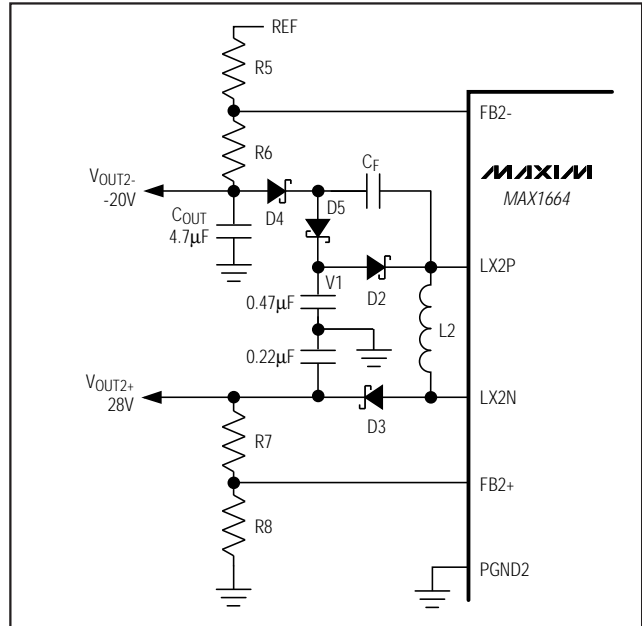


Figure 6. VOUT2- Voltage-Doubler Charge Pump

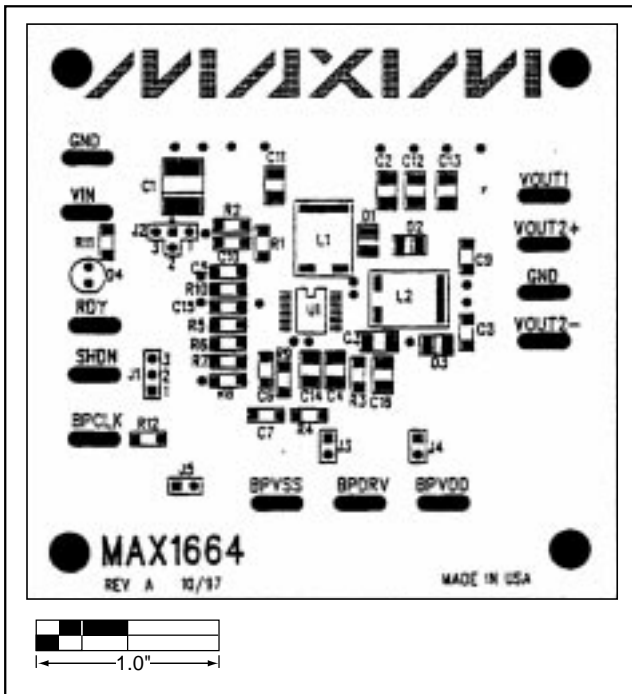


Figure 7a. MAX1664 Component Placement Guide

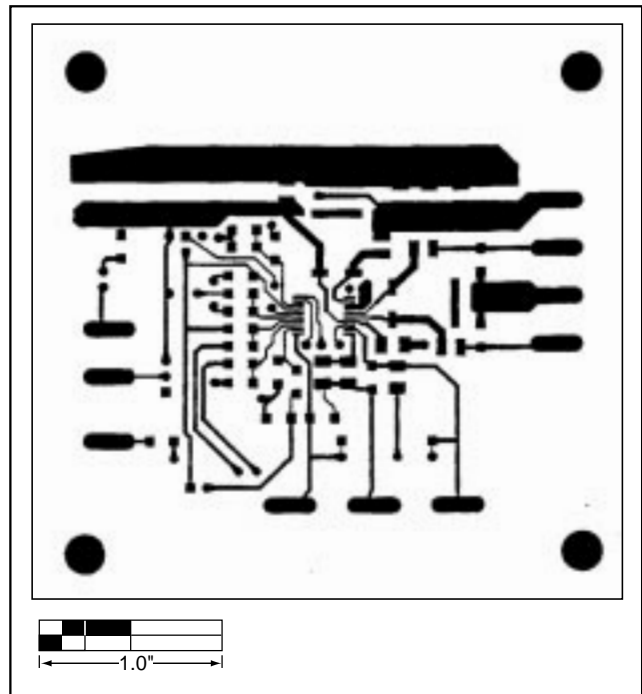
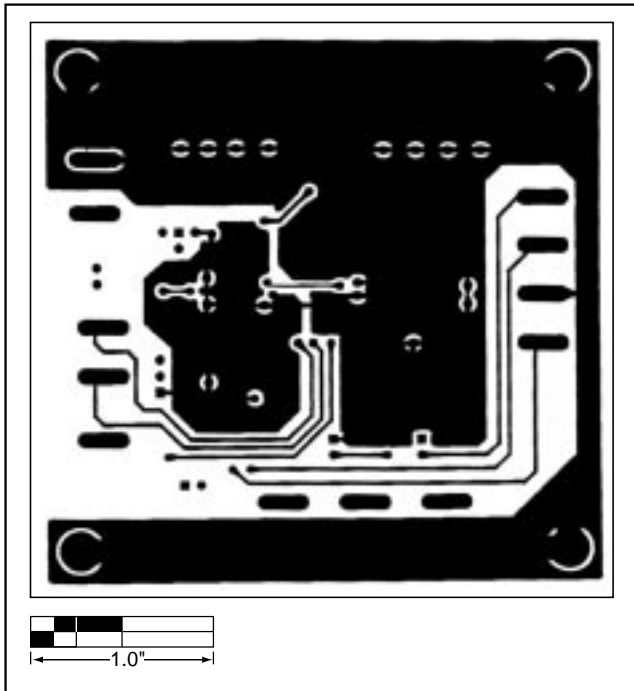


Figure 7b. MAX1664 PC Board Layout—Component Side

# Active-Matrix Liquid Crystal Display (AMLCD) Supply

MAX1664



## Chip Information

TRANSISTOR COUNT: 838

Figure 7c. MAX1664 PC Board Layout—Solder Side

# Active-Matrix Liquid Crystal Display (AMLCD) Supply

## Package Information

**COMMON DIMENSIONS**

Symbol	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.05	0.15	.002	.006
A <sub>1</sub>	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b <sub>1</sub>	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c <sub>1</sub>	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC	N	VARIATIONS				
		MILLIMETERS		INCHES		
		MIN.	MAX.	MIN.	MAX.	
AC	16	D	4.90	5.10	.193	.201
AD	20	D	6.40	6.60	.252	.260
AD-EP	20	D	6.40	6.60	.252	.260
		X	4.00	4.34	.157	.171
		Y	2.94	3.15	.112	.124
AE	24	D	7.70	7.90	.303	.311
AF	28	D	9.60	9.80	.378	.386

**NOTES:**

- DIMENSIONS D AND E DO NOT INCLUDE FLASH.
- MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 mm PER SIDE.
- CONTROLLING DIMENSION: MILLIMETER.
- MEETS JEDEC OUTLINE MO-153 VARIATIONS AB, AC, AD, AE.
- DIMENSIONS X AND Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY.
- EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".

TSSOP-EPS

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