



# MJ14001 (PNP), MJ14002\* (NPN), MJ14003\* (PNP)

\*Preferred Devices

## High-Current Complementary Silicon Power Transistors

Designed for use in high-power amplifier and switching circuit applications.

### Features

- High Current Capability –  $I_C$  Continuous = 60 Amperes
- DC Current Gain –  $h_{FE} = 15-100$  @  $I_C = 50$  Adc
- Low Collector–Emitter Saturation Voltage –  $V_{CE(sat)} = 2.5$  Vdc (Max) @  $I_C = 50$  Adc
- Pb–Free Packages are Available\*

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	60	Vdc
	MJ14001 MJ14002/03	80	
Collector–Base Voltage	$V_{CBO}$	60	Vdc
	MJ14001 MJ14002/03	80	
Emitter–Base Voltage	$V_{EBO}$	5.0	Vdc
Collector Current – Continuous	$I_C$	60	Adc
Base Current – Continuous	$I_B$	15	Adc
Emitter Current – Continuous	$I_E$	75	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate Above $25^\circ\text{C}$	$P_D$	300 1.71	W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +200	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

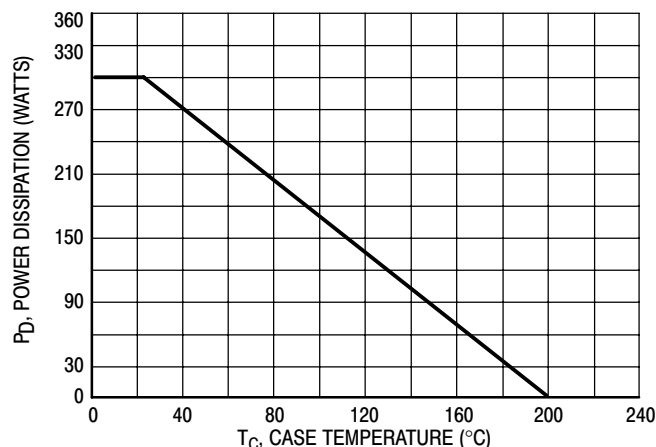


Figure 1. Power Derating

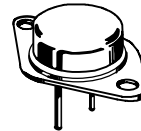


ON Semiconductor®

<http://onsemi.com>

## 60 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 60–80 VOLTS, 300 WATTS

### MARKING DIAGRAM



TO-204 (TO-3)  
CASE 197A  
STYLE 1

MJ1400x = Device Code  
          xx = 1, 2, or 3  
G      = Pb–Free Package  
A      = Location Code  
YY     = Year  
WW     = Work Week  
MEX    = Country of Origin

### ORDERING INFORMATION

Device	Package	Shipping
MJ14001	TO-3	100 Units/Tray
MJ14001G	TO-3 (Pb–Free)	100 Units/Tray
MJ14002	TO-3	100 Units/Tray
MJ14002G	TO-3 (Pb–Free)	100 Units/Tray
MJ14003	TO-3	100 Units/Tray
MJ14003G	TO-3 (Pb–Free)	100 Units/Tray

Preferred devices are recommended choices for future use and best overall value.

\*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MJ14001 (PNP), MJ14002\* (NPN), MJ14003\* (PNP)

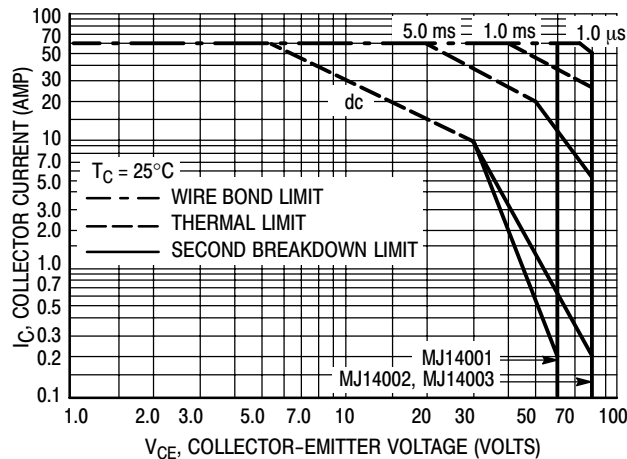
## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.584	$^{\circ}C/W$

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector-Emitter Sustaining Voltage (Note 1) ( $I_C = 200 \text{ mAdc}$ , $I_B = 0$ )	$V_{CE(sus)}$	60 80	– –	Vdc
Collector Cutoff Current ( $V_{CE} = 30 \text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 40 \text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	– –	1.0 1.0	mA
Collector Cutoff Current ( $V_{CE} = 60 \text{ Vdc}$ , $V_{BE(off)} = 1.5 \text{ V}$ ) ( $V_{CE} = 80 \text{ Vdc}$ , $V_{BE(off)} = 1.5 \text{ V}$ )	$I_{CEX}$	– –	1.0 1.0	mA
Collector Cutoff Current ( $V_{CB} = 60 \text{ Vdc}$ , $I_E = 0$ ) ( $V_{CB} = 80 \text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	– –	1.0 1.0	mA
Emitter Cutoff Current ( $V_{BE} = 5.0 \text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	–	1.0	mA
<b>ON CHARACTERISTICS</b>				
DC Current Gain (Note 1) ( $I_C = 25 \text{ Adc}$ , $V_{CE} = 3.0 \text{ V}$ ) ( $I_C = 50 \text{ Adc}$ , $V_{CE} = 3.0 \text{ V}$ ) ( $I_C = 60 \text{ Adc}$ , $V_{CE} = 3.0 \text{ V}$ )	$h_{FE}$	30 15 5.0	– 100 –	–
Collector-Emitter Saturation Voltage (Note 1) ( $I_C = 25 \text{ Adc}$ , $I_B = 2.5 \text{ Adc}$ ) ( $I_C = 50 \text{ Adc}$ , $I_B = 5.0 \text{ Adc}$ ) ( $I_C = 60 \text{ Adc}$ , $I_B = 12 \text{ Adc}$ )	$V_{CE(sat)}$	– – –	1.0 2.5 3.0	Vdc
Base-Emitter Saturation Voltage (Note 1) ( $I_C = 25 \text{ Adc}$ , $I_B = 2.5 \text{ Adc}$ ) ( $I_C = 50 \text{ Adc}$ , $I_B = 5.0 \text{ Adc}$ ) ( $I_C = 60 \text{ Adc}$ , $I_B = 12 \text{ Adc}$ )	$V_{BE(sat)}$	– – –	2.0 3.0 4.0	Vdc
<b>DYNAMIC CHARACTERISTICS</b>				
Output Capacitance ( $V_{CB} = 10 \text{ Vdc}$ , $I_E = 0$ , $f = 0.1 \text{ MHz}$ )	$C_{ob}$	–	2000	pF

1. Pulse Test: Pulse Width  $\leq 300 \mu s$ , Duty Cycle  $\leq 2.0\%$ .



**Figure 2. Maximum Rated Forward Biased Safe Operating Area**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation: i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on  $T_{J(pk)} = 200^{\circ}C$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 200^{\circ}C$ .  $T_{J(pk)}$  may be calculated from the data in Figure 13. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

# MJ14001 (PNP), MJ14002\* (NPN), MJ14003\* (PNP)

## TYPICAL ELECTRICAL CHARACTERISTICS

MJ14002 (NPN)

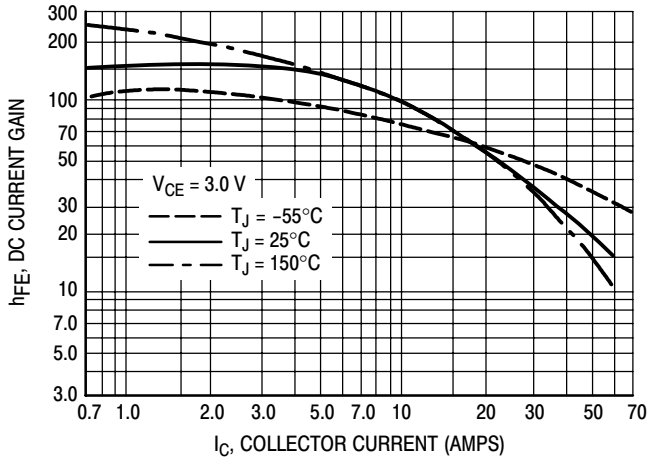


Figure 3. DC Current Gain

MJ14001, MJ14003 (PNP)

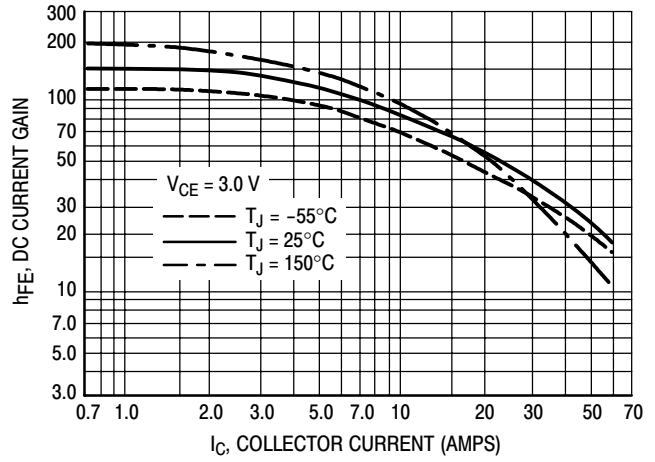


Figure 4. DC Current Gain

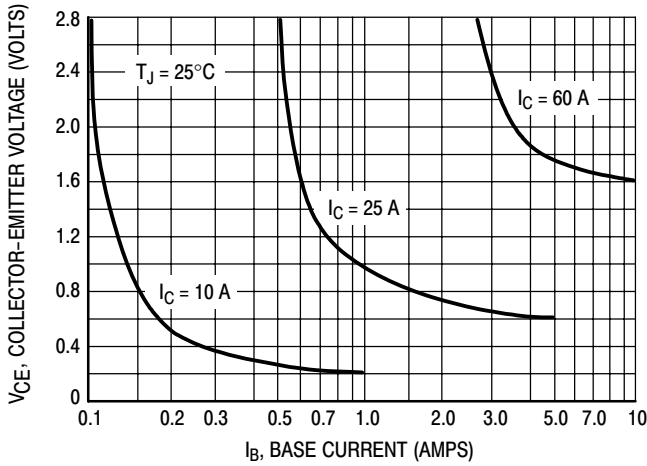


Figure 5. Collector Saturation Region

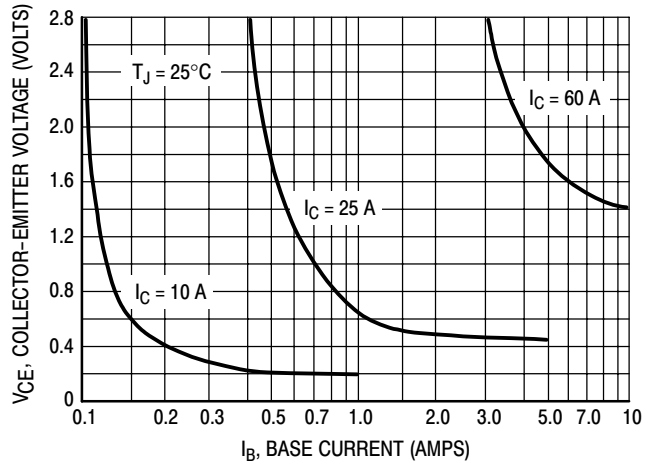


Figure 6. Collector Saturation Region

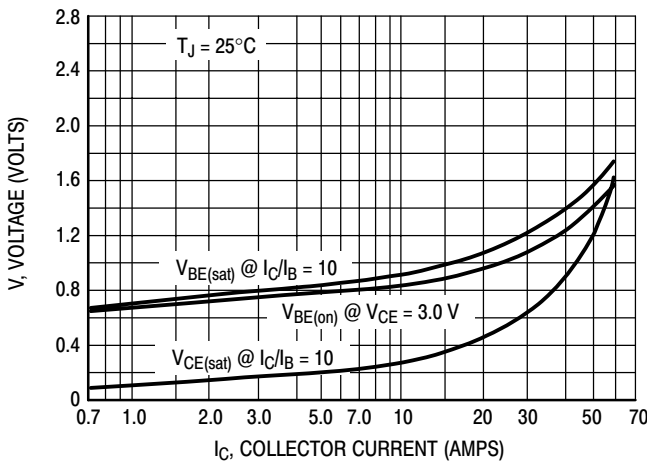


Figure 7. "On" Voltages

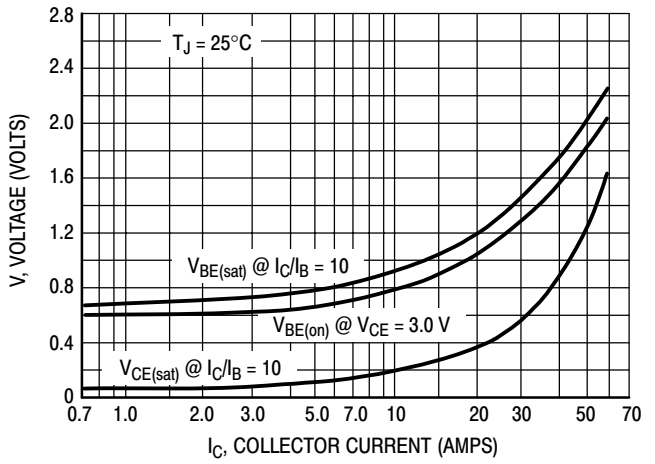


Figure 8. "On" Voltages

# MJ14001 (PNP), MJ14002\* (NPN), MJ14003\* (PNP)

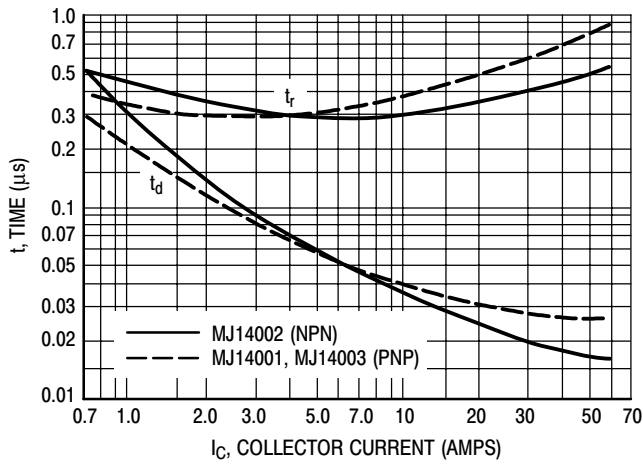


Figure 9. Turn-On Switching Times

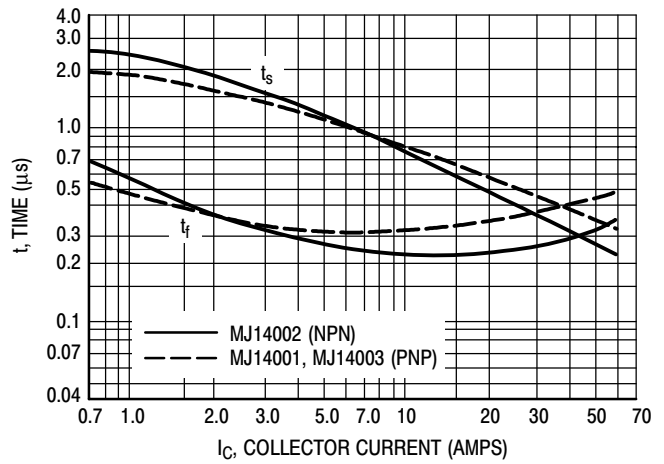


Figure 10. Turn-Off Switching Times

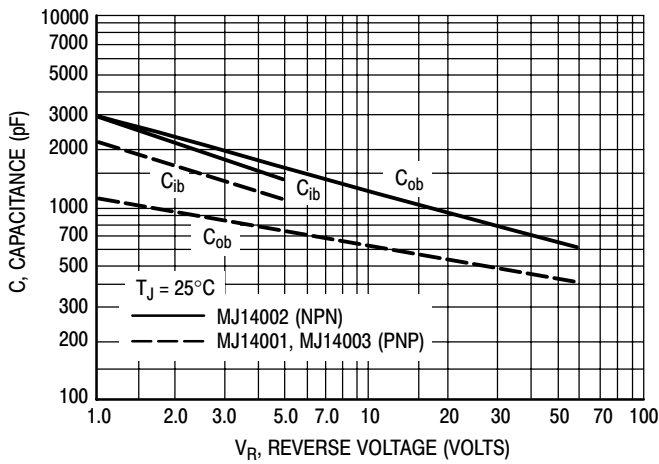
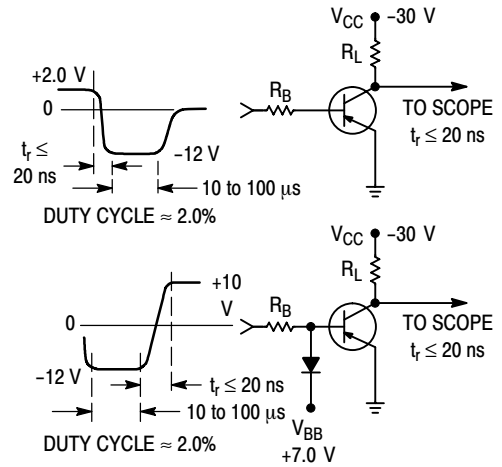


Figure 11. Capacitance Variation



FOR CURVES OF FIGURES 3 & 6,  $R_B$  &  $R_L$  ARE VARIED. INPUT LEVELS ARE APPROXIMATELY AS SHOWN. FOR NPN CIRCUITS, REVERSE ALL POLARITIES.

Figure 12. Switching Test Circuit

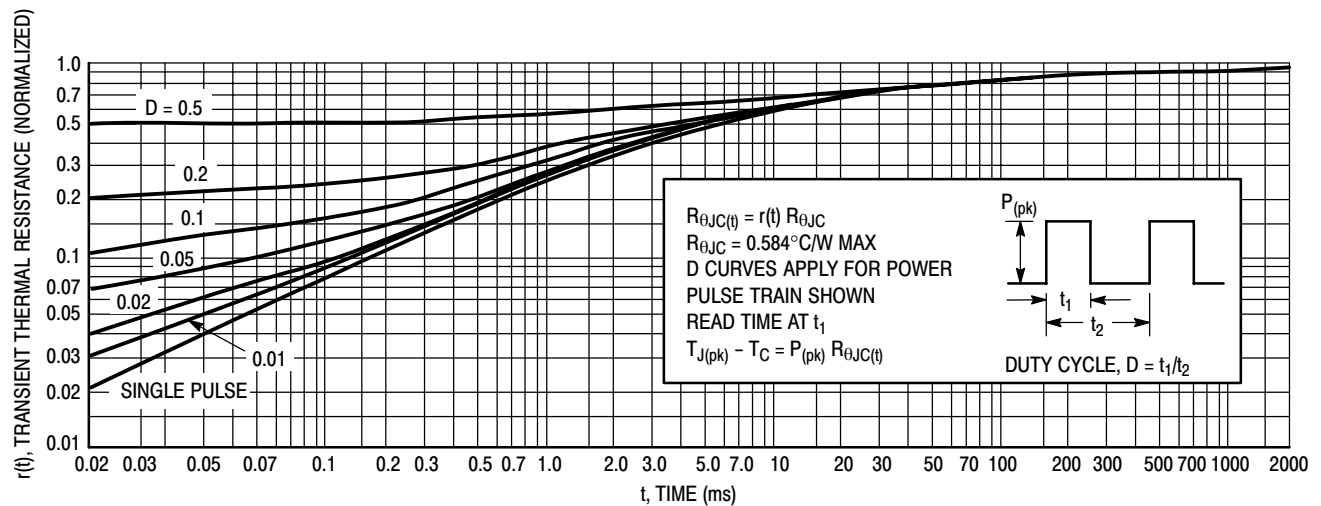
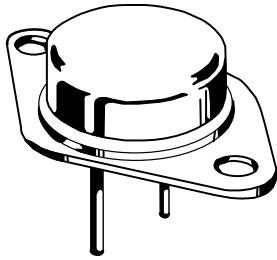


Figure 13. Thermal Response

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

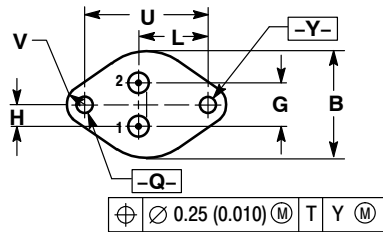
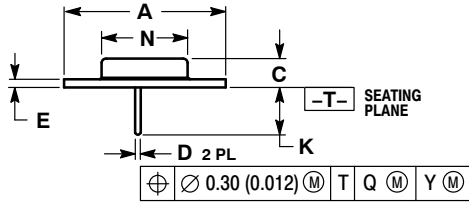
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TO-204 (TO-3)  
CASE 197A-05  
ISSUE K

DATE 21 FEB 2000

SCALE 1:1



STYLE 1:  
PIN 1. BASE  
2. EMITTER  
CASE: COLLECTOR

STYLE 2:  
PIN 1. EMITTER  
2. BASE  
CASE: COLLECTOR

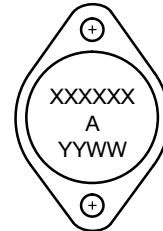
STYLE 3:  
PIN 1. GATE  
2. SOURCE  
CASE: DRAIN

STYLE 4:  
PIN 1. ANODE = 1  
2. ANODE = 2  
CASE: CATHODES

- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.530 REF		38.86 REF	
B	0.990	1.050	25.15	26.67
C	0.250	0.335	6.35	8.51
D	0.057	0.063	1.45	1.60
E	0.060	0.070	1.53	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	0.760	0.830	19.31	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

### GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
A = Assembly Location  
YY = Year  
WW = Work Week

\*This information is generic. Please refer to device data sheet for actual part marking.

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