



**THE DATASHEET OF
MKL03Z32CAF4R**



Kinetis KL03 32 KB Flash

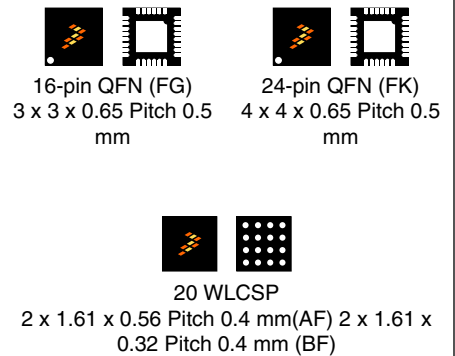
48 MHz Cortex-M0+ Based Microcontroller

Supports ultra low power 48 MHz devices with up to 32 KB Flash.

World's smallest MCU based on ARM® technology. Ideal solution for Internet of Things edge nodes design with ultra small form factor and ultra low power consumption. The products offers:

- Tiny footprint packages, including 1.6 x 2.0 mm² WLCSP
- Run power consumption as low as 50 µA/MHz
- Static power consumption as low as 2.2 µA with 7.5 µs wakeup time for full retention and lowest static mode down to 77 nA in deep sleep
- Highly integrated peripherals, including new boot ROM and high accurate internal voltage reference, etc

MKL03ZxxVFG4
MKL03ZxxVFK4
MKL03Z32CAF4R
MKL03Z32CBF4R



Core

- ARM® Cortex®-M0+ core up to 48 MHz

Memories

- Up to 32 KB program flash memory
- 2 KB SRAM
- 8 KB ROM with build-in bootloader
- 16 bytes regfile

System peripherals

- Nine low-power modes to provide power optimization based on application requirements
- COP Software watchdog
- Low-leakage wakeup unit
- SWD debug interface and Micro Trace Buffer
- Bit Manipulation Engine

Clocks

- 48 MHz high accuracy internal reference clock
- 8/2 MHz low power internal reference clock
- 32 kHz to 40 kHz crystal oscillator
- 1 kHz LPO clock

Operating Characteristics

- Voltage range: 1.71 to 3.6 V
- Flash write voltage range: 1.71 to 3.6 V

- Temperature range (ambient): -40 to 105°C for QFN packages; -40 to 85°C for WLCSP packages

Human-machine interface

- General-purpose input/output up to 22

Communication interfaces

- One 8-bit SPI module
- One LPUART module
- One I2C module supporting up to 1 Mbit/s, with double buffer

Analog Modules

- 12-bit SAR ADC with internal voltage reference, up to 818 ksps and 7 channels
- High-speed analog comparator containing a 6-bit DAC and programmable reference input
- 1.2 V voltage reference (Vref)

Timers

- Two 2-channel Timer/PWM modules
- One low-power timer
- Real time clock

Security and integrity modules

- 80-bit unique identification number per chip

Ordering Information¹

| Part Number | Memory | | Maximum number of I/O's |
|-----------------|------------|-----------|-------------------------|
| | Flash (KB) | SRAM (KB) | |
| MKL03Z8VFG4(R) | 8 | 2 | 14 |
| MKL03Z16VFG4(R) | 16 | 2 | 14 |
| MKL03Z32VFG4(R) | 32 | 2 | 14 |
| MKL03Z32CAF4R | 32 | 2 | 18 |
| MKL03Z32CBF4R | 32 | 2 | 18 |
| MKL03Z8VFK4(R) | 8 | 2 | 22 |
| MKL03Z16VFK4(R) | 16 | 2 | 22 |
| MKL03Z32VFK4(R) | 32 | 2 | 22 |

1. To confirm current availability of orderable part numbers, go to <http://www.nxp.com> and perform a part number search.

Related Resources

| Type | Description | Resource |
|------------------|--------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Selector Guide | The Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector. | Solution Advisor |
| Product Brief | The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability. | KL03PB ¹ |
| Reference Manual | The Reference Manual contains a comprehensive description of the structure and function (operation) of a device. | KL03P24M48SF0RM ¹ |
| Data Sheet | The Data Sheet includes electrical characteristics and signal connections. | KL03P24M48SF0 ¹ |
| Chip Errata | The chip mask set Errata provides additional or corrective information for a particular device mask set. | KL03Z_xN86K ² |
| Package drawing | Package dimensions are provided in package drawings. | QFN 16-pin: 98ASA00525D ¹ QFN 24-pin: 98ASA00602D ¹ WLCSP 20-pin: 98ASA00676D ¹ WLCSP 20-pin (ultra thin): 98ASA00964D ¹ |

1. To find the associated resource, go to <http://www.nxp.com> and perform a search using this term.
2. To find the associated resource, go to <http://www.nxp.com> and perform a search using this term with the “x” replaced by the revision of the device you are using.

Figure 1 shows the functional modules in the chip.

Kinetis KL03 Family

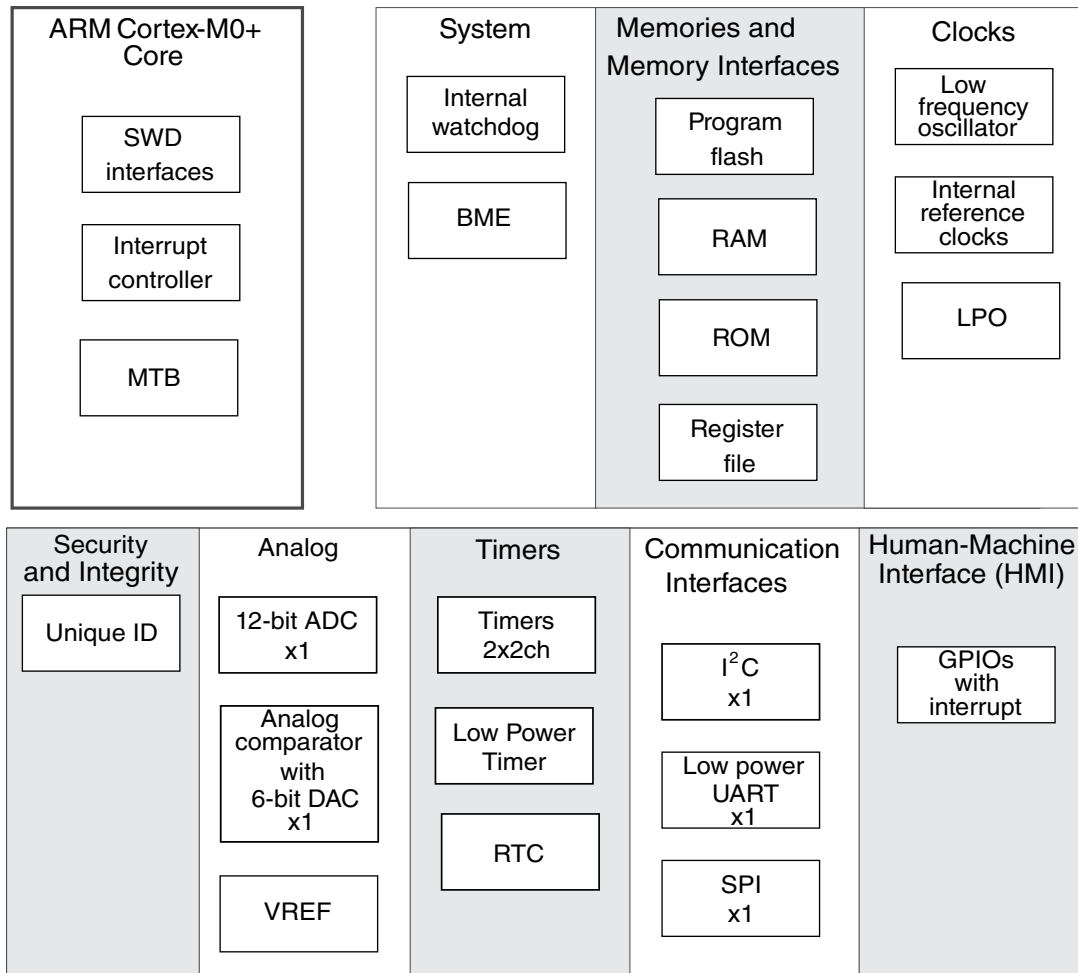


Figure 1. Functional block diagram

Table of Contents

| | | | |
|-----------------------------------------------------------------------|----|---------------------------------------------------------------------|----|
| 1 Ratings..... | 5 | 3.6 Analog..... | 33 |
| 1.1 Thermal handling ratings..... | 5 | 3.6.1 ADC electrical specifications..... | 33 |
| 1.2 Moisture handling ratings..... | 5 | 3.6.2 CMP and 6-bit DAC electrical specifications..... | 37 |
| 1.3 ESD handling ratings..... | 5 | 3.6.3 Voltage reference electrical specifications..... | 39 |
| 1.4 Voltage and current operating ratings..... | 6 | 3.7 Timers..... | 40 |
| 2 General..... | 6 | 3.8 Communication interfaces..... | 40 |
| 2.1 AC electrical characteristics..... | 6 | 3.8.1 SPI switching specifications..... | 41 |
| 2.2 Nonswitching electrical specifications..... | 7 | 3.8.2 Inter-Integrated Circuit Interface (I2C) timing..... | 45 |
| 2.2.1 Voltage and current operating requirements..... | 7 | 3.8.3 UART..... | 47 |
| 2.2.2 LVD and POR operating requirements..... | 7 | 4 Dimensions..... | 47 |
| 2.2.3 Voltage and current operating behaviors..... | 8 | 4.1 Obtaining package dimensions..... | 47 |
| 2.2.4 Power mode transition operating behaviors..... | 9 | 5 Pinout..... | 48 |
| 2.2.5 Power consumption operating behaviors..... | 10 | 5.1 KL03 signal multiplexing and pin assignments..... | 48 |
| 2.2.6 EMC radiated emissions operating behaviors..... | 24 | 5.2 KL03 pinouts..... | 49 |
| 2.2.7 EMC Radiated Emissions Web Search Procedure boilerplate..... | 25 | 6 Ordering parts..... | 51 |
| 2.2.8 Capacitance attributes..... | 25 | 6.1 Determining valid orderable parts..... | 51 |
| 2.3 Switching specifications..... | 25 | 7 Part identification..... | 51 |
| 2.3.1 Device clock specifications..... | 25 | 7.1 Description..... | 51 |
| 2.3.2 General switching specifications..... | 26 | 7.2 Format..... | 52 |
| 2.4 Thermal specifications..... | 26 | 7.3 Fields..... | 52 |
| 2.4.1 Thermal operating requirements..... | 26 | 7.4 Example..... | 52 |
| 2.4.2 Thermal attributes..... | 27 | 8 Terminology and guidelines..... | 53 |
| 3 Peripheral operating requirements and behaviors..... | 27 | 8.1 Definition: Operating requirement..... | 53 |
| 3.1 Core modules..... | 27 | 8.2 Definition: Operating behavior..... | 53 |
| 3.1.1 SWD electricals | 28 | 8.3 Definition: Attribute..... | 54 |
| 3.2 System modules..... | 29 | 8.4 Definition: Rating..... | 54 |
| 3.3 Clock modules..... | 29 | 8.5 Result of exceeding a rating..... | 55 |
| 3.3.1 MCG-Lite specifications..... | 29 | 8.6 Relationship between ratings and operating requirements..... | 55 |
| 3.3.2 Oscillator electrical specifications..... | 30 | 8.7 Guidelines for ratings and operating requirements..... | 55 |
| 3.4 Memories and memory interfaces..... | 31 | 8.8 Definition: Typical value..... | 56 |
| 3.4.1 Flash electrical specifications..... | 31 | 8.9 Typical value conditions..... | 57 |
| 3.5 Security and integrity modules..... | 33 | 9 Revision history..... | 57 |

1 Ratings

1.1 Thermal handling ratings

Table 1. Thermal handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------------|-------------------------------|------|------|------|-------|
| T _{STG} | Storage temperature | -55 | 150 | °C | 1 |
| T _{SDR} | Solder temperature, lead-free | — | 260 | °C | 2 |

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Table 2. QFN packages moisture handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|----------------------------|------|------|------|-------|
| MSL | Moisture sensitivity level | — | 3 | — | 1 |

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

Table 3. WLCSP packages moisture handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|----------------------------|------|------|------|-------|
| MSL | Moisture sensitivity level | — | 1 | — | 1 |

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Table 4. ESD handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------------|-------------------------------------------------------|-------|-------|------|-------|
| V _{HBM} | Electrostatic discharge voltage, human body model | -2000 | +2000 | V | 1 |
| V _{CDM} | Electrostatic discharge voltage, charged-device model | -500 | +500 | V | 2 |
| I _{LAT} | Latch-up current at ambient temperature of 105 °C | -100 | +100 | mA | 3 |

General

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

1.4 Voltage and current operating ratings

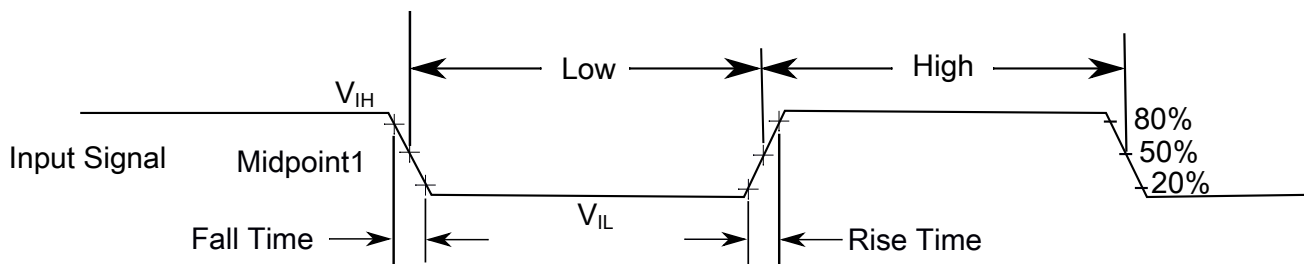
Table 5. Voltage and current operating ratings

| Symbol | Description | Min. | Max. | Unit |
|-----------|---------------------------------------------------------------------------|----------------|----------------|------|
| V_{DD} | Digital supply voltage | -0.3 | 3.8 | V |
| I_{DD} | Digital supply current | — | 120 | mA |
| V_{IO} | IO pin input voltage | -0.3 | $V_{DD} + 0.3$ | V |
| I_D | Instantaneous maximum current single pin limit (applies to all port pins) | -25 | 25 | mA |
| V_{DDA} | Analog supply voltage | $V_{DD} - 0.3$ | $V_{DD} + 0.3$ | V |

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 2. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume the output pins have the following characteristics.

- $C_L=30$ pF loads

- Slew rate disabled
- Normal drive strength

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 6. Voltage and current operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------|---------------------------------------------|--------|-------|
| V_{DD} | Supply voltage | 1.71 | 3.6 | V | |
| V_{DDA} | Analog supply voltage | 1.71 | 3.6 | V | — |
| $V_{DD} - V_{DDA}$ | V_{DD} -to- V_{DDA} differential voltage | -0.1 | 0.1 | V | — |
| $V_{SS} - V_{SSA}$ | V_{SS} -to- V_{SSA} differential voltage | -0.1 | 0.1 | V | — |
| V_{IH} | Input high voltage <ul style="list-style-type: none"> • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ • $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ | $0.7 \times V_{DD}$ $0.75 \times V_{DD}$ | — — | V V | — |
| V_{IL} | Input low voltage <ul style="list-style-type: none"> • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ • $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ | — — | $0.35 \times V_{DD}$ $0.3 \times V_{DD}$ | V V | — |
| V_{HYS} | Input hysteresis | $0.06 \times V_{DD}$ | — | V | — |
| I_{ICIO} | IO pin negative DC injection current—single pin <ul style="list-style-type: none"> • $V_{IN} < V_{SS}-0.3\text{V}$ | -5 | — | mA | 1 |
| I_{ICcont} | Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins <ul style="list-style-type: none"> • Negative current injection | -25 | — | mA | — |
| V_{RAM} | V_{DD} voltage required to retain RAM | 1.2 | — | V | — |

1. All I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to V_{DD} . If V_{IN} greater than V_{IO_MIN} ($= V_{SS}-0.3\text{ V}$) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R = (V_{IO_MIN} - V_{IN})/|I_{ICIO}|$.

2.2.2 LVD and POR operating requirements

Table 7. V_{DD} supply LVD and POR operating requirements

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-------------|---------------------------------------------------------------|------|------|------|------|-------|
| V_{POR} | Falling V_{DD} POR detect voltage | 0.8 | 1.1 | 1.5 | V | — |
| V_{LVDH} | Falling low-voltage detect threshold — high range (LVDV = 01) | 2.48 | 2.56 | 2.64 | V | — |
| V_{LVW1H} | Low-voltage warning thresholds — high range | | | | | 1 |
| | • Level 1 falling (LVWV = 00) | 2.62 | 2.70 | 2.78 | V | |
| V_{LVW2H} | • Level 2 falling (LVWV = 01) | 2.72 | 2.80 | 2.88 | V | |
| V_{LVW3H} | • Level 3 falling (LVWV = 10) | 2.82 | 2.90 | 2.98 | V | |
| V_{LVW4H} | • Level 4 falling (LVWV = 11) | 2.92 | 3.00 | 3.08 | V | |
| V_{HYSH} | Low-voltage inhibit reset/recover hysteresis — high range | — | ±60 | — | mV | — |
| V_{LVDL} | Falling low-voltage detect threshold — low range (LVDV=00) | 1.54 | 1.60 | 1.66 | V | — |
| V_{LVW1L} | Low-voltage warning thresholds — low range | | | | | 1 |
| | • Level 1 falling (LVWV = 00) | 1.74 | 1.80 | 1.86 | V | |
| V_{LVW2L} | • Level 2 falling (LVWV = 01) | 1.84 | 1.90 | 1.96 | V | |
| V_{LVW3L} | • Level 3 falling (LVWV = 10) | 1.94 | 2.00 | 2.06 | V | |
| V_{LVW4L} | • Level 4 falling (LVWV = 11) | 2.04 | 2.10 | 2.16 | V | |
| V_{HYSL} | Low-voltage inhibit reset/recover hysteresis — low range | — | ±40 | — | mV | — |
| V_{BG} | Bandgap voltage reference | 0.97 | 1.00 | 1.03 | V | — |
| t_{LPO} | Internal low power oscillator period — factory trimmed | 900 | 1000 | 1100 | µs | — |

1. Rising thresholds are falling threshold + hysteresis voltage

2.2.3 Voltage and current operating behaviors

Table 8. Voltage and current operating behaviors

| Symbol | Description | Min. | Max. | Unit | Notes |
|----------|-----------------------------------------------------------------------------|----------------|------|------|-------|
| V_{OH} | Output high voltage — Normal drive pad (except RESET) | | | | 1, 2 |
| | • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -5\text{ mA}$ | $V_{DD} - 0.5$ | — | V | |
| | • $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OH} = -2.5\text{ mA}$ | $V_{DD} - 0.5$ | — | V | |
| V_{OH} | Output high voltage — High drive pad (except RESET) | | | | 1, 2 |
| | | $V_{DD} - 0.5$ | — | V | |
| | | $V_{DD} - 0.5$ | — | V | |

Table continues on the next page...

Table 8. Voltage and current operating behaviors (continued)

| Symbol | Description | Min. | Max. | Unit | Notes |
|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|------------|---------------|-------|
| | <ul style="list-style-type: none"> • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -20\text{ mA}$ • $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OH} = -10\text{ mA}$ | | | | |
| I_{OHT} | Output high current total for all ports | — | 100 | mA | — |
| V_{OL} | Output low voltage — Normal drive pad <ul style="list-style-type: none"> • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 5\text{ mA}$ • $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 2.5\text{ mA}$ | — — | 0.5 0.5 | V V | 1 |
| V_{OL} | Output low voltage — High drive pad <ul style="list-style-type: none"> • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 20\text{ mA}$ • $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 10\text{ mA}$ | — — | 0.5 0.5 | V V | 1 |
| I_{OLT} | Output low current total for all ports | — | 100 | mA | — |
| I_{IN} | Input leakage current (per pin) for full temperature range | — | 1 | μA | 3 |
| I_{IN} | Input leakage current (per pin) at 25 °C | — | 0.025 | μA | 3 |
| I_{IN} | Input leakage current (total all pins) for full temperature range | — | 41 | μA | 3 |
| I_{OZ} | Hi-Z (off-state) leakage current (per pin) | — | 1 | μA | — |
| R_{PU} | Internal pullup resistors | 20 | 50 | k Ω | 4 |

1. I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. The reset pin only contains an active pull down device when configured as the RESET signal or as a GPIO. When configured as a GPIO output, it acts as a pseudo open drain output.
3. Measured at $V_{DD} = 3.6\text{ V}$
4. Measured at V_{DD} supply voltage = V_{DD} min and $V_{input} = V_{SS}$

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and $VLLSx \rightarrow RUN$ recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- HIRC clock mode

$VLLSx \rightarrow RUN$ recovery uses LIRC clock mode at the default CPU and system frequency of 8 MHz, and a bus and flash clock frequency of 4 MHz.

Table 9. Power mode transition operating behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit | Note |
|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|------|
| t _{POR} | After a POR event, amount of time from the point V _{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip. | — | — | 300 | μs | 1 |
| | • VLLS0 → RUN | — | 152 | 166 | μs | — |
| | • VLLS1 → RUN | — | 152 | 166 | μs | — |
| | • VLLS3 → RUN | — | 93 | 104 | μs | — |
| | • VLPS → RUN | — | 7.5 | 8 | μs | — |
| | • STOP → RUN | — | 7.5 | 8 | μs | — |

1. Normal boot (FTFA_FOPT[LPBOOT]=11).

2.2.5 Power consumption operating behaviors

Table 10. KL03 QFN packages power consumption operating behaviors

| Symbol | Description | Min. | Typ. | Max. ¹ | Unit | Notes |
|-----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|-------------------|------|-------|
| I _{DDA} | Analog supply current | — | — | See note | mA | 2 |
| I _{DD_RUNCO} | Running CoreMark in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V _{DD} = 3.0 V • at 25 °C | — | 5.49 | 5.71 | mA | 3 |
| | | — | 5.62 | 5.84 | | |
| I _{DD_RUNCO} | Running While(1) loop in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V _{DD} = 3.0 V • at 25 °C | — | 5.16 | 5.37 | mA | 3 |
| | | — | 5.27 | 5.48 | | |
| I _{DD_RUN} | Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 48 MHz core/24 MHz flash, V _{DD} = 3.0 V • at 25 °C | — | 6.03 | 6.27 | mA | 3 |
| | | — | 6.16 | 6.41 | | |
| I _{DD_RUN} | Run mode current—48M HIRC mode, running CoreMark in flash all peripheral clock disable, 24 MHz core/12 MHz flash, V _{DD} = 3.0 V | | | | | 3 |

Table continues on the next page...

Table 10. KL03 QFN packages power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. ¹ | Unit | Notes |
|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|-------------------|------|-------|
| | <ul style="list-style-type: none"> at 25 °C at 105 °C | — | 3.71 | 3.86 | mA | |
| I _{DD_RUN} | Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 12 MHz core/6 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C at 105 °C | — | 2.47 | 2.57 | mA | 3 |
| I _{DD_RUN} | Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock enable 48 MHz core/24 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C at 105 °C | — | 6.43 | 6.69 | mA | 3 |
| I _{DD_RUN} | Run mode current—48M HIRC mode, running While(1) loop in flash all peripheral clock disable, 48 MHz core/24 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C at 105 °C | — | 5.71 | 5.94 | mA | — |
| I _{DD_RUN} | Run mode current—48M HIRC mode, running While(1) loop in Flash all peripheral clock disable, 24 MHz core/12 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C at 105 °C | — | 3.3 | 3.43 | mA | — |
| I _{DD_RUN} | Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock disable, 12 MHz core/6 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C at 105 °C | — | 2.28 | 2.37 | mA | — |
| I _{DD_RUN} | Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock enable, 48 MHz core/24 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C at 105 °C | — | 6.1 | 6.34 | mA | — |
| I _{DD_RUN} | Run mode current—48M HIRC mode, running While(1) loop in SRAM all peripheral clock disable, 48 MHz core/24 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C at 105 °C | — | 3.14 | 3.23 | mA | — |
| I _{DD_RUN} | Run mode current—48M HIRC mode, running While(1) loop in SRAM all peripheral clock enable, 48 MHz core/24 MHz flash, V _{DD} = 3.0 V | — | 3.54 | 3.63 | mA | — |
| | | — | 3.67 | 3.76 | | |

Table continues on the next page...

Table 10. KL03 QFN packages power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. ¹ | Unit | Notes |
|------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|-------------------|------|-------|
| | <ul style="list-style-type: none"> at 25 °C at 105 °C | | | | | |
| I _{DD_VLPRCO} | Very-low-power run While(1) loop in flash in compute operation mode— 2 MHz LIRC mode, 2 MHz core/0.5 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C | — | 500 | 750 | μA | — |
| I _{DD_VLPRCO} | Very-low-power-run While(1) loop in SRAM in compute operation mode— 8 MHz LIRC mode, 4 MHz core / 1 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C | — | 188 | 217 | μA | — |
| I _{DD_VLPRCO} | Very-low-power run While(1) loop in SRAM in compute operation mode:—2 MHz LIRC mode, 2 MHz core / 0.5 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C | — | 82 | 123 | μA | — |
| I _{DD_VLPR} | Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 2 MHz core / 0.5 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C | — | 503 | 754 | μA | — |
| I _{DD_VLPR} | Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 125 kHz core / 31.25 kHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C | — | 60 | 90 | μA | — |
| I _{DD_VLPR} | Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock enable, 2 MHz core / 0.5 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C | — | 516 | 774 | μA | — |
| I _{DD_VLPR} | Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in SRAM in all peripheral clock disable, 4 MHz core / 1 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C | — | 209 | 350 | μA | — |
| I _{DD_VLPR} | Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in SRAM all peripheral clock enable, 4 MHz core / 1 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C | — | 229 | 370 | μA | — |
| I _{DD_VLPR} | Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM in all peripheral clock disable, 2 MHz core / 0.5 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C | — | 93 | 140 | μA | — |
| I _{DD_VLPR} | Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM all peripheral clock disable, 125 kHz core / 31.25 kHz flash, V _{DD} = 3.0 V | — | 31 | 81 | μA | — |

Table continues on the next page...

Table 10. KL03 QFN packages power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. ¹ | Unit | Notes |
|------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-------|-------------------|------|-------|
| | <ul style="list-style-type: none"> at 25 °C | | | | | |
| I _{DD_VLPR} | Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM all peripheral clock enable, 2 MHz core / 0.5 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C | — | 103 | 154 | μA | — |
| I _{DD_WAIT} | Wait mode current—core disabled, 48 MHz system/24 MHz bus, flash disabled (flash doze enabled), all peripheral clocks disabled, MCG_Lite under HIRC mode, V _{DD} = 3.0 V | — | 1.4 | 1.94 | mA | — |
| I _{DD_WAIT} | Wait mode current—core disabled, 24 MHz system/12 MHz bus, flash disabled (flash doze enabled), all peripheral clocks disabled, MCG_Lite under HIRC mode, V _{DD} = 3.0 V | — | 1.02 | 1.24 | mA | — |
| I _{DD_VLPW} | Very-low-power wait mode current, core disabled, 4 MHz system/ 1 MHz bus and flash, all peripheral clocks disabled, V _{DD} = 3.0 V | — | 121 | 181 | μA | — |
| I _{DD_VLPW} | Very-low-power wait mode current, core disabled, 2 MHz system/ 0.5 MHz bus and flash, all peripheral clocks disabled, V _{DD} = 3.0 V | — | 59 | 97 | μA | — |
| I _{DD_VLPW} | Very-low-power wait mode current, core disabled, 125 kHz system/ 31.25 kHz bus and flash, all peripheral clocks disabled, V _{DD} = 3.0 V | — | 28 | 42 | μA | — |
| I _{DD_PSTOP2} | Partial Stop 2, core and system clock disabled, 12 MHz bus and flash, V _{DD} = 3.0 V | — | 1.53 | 2.03 | mA | — |
| I _{DD_PSTOP2} | Partial Stop 2, core and system clock disabled, flash doze enabled, 12 MHz bus, V _{DD} = 3.0 V | — | 0.881 | 1.18 | mA | — |
| I _{DD_STOP} | Stop mode current at 3.0 V <ul style="list-style-type: none"> at 25 °C and below at 50 °C at 85 °C at 105 °C | — | 158 | 175.7 | μA | — |
| | | — | 164 | 179.48 | | |
| | | — | 187 | 199.54 | | |
| | | — | 219 | 236.43 | | |
| I _{DD_VLPS} | Very-low-power stop mode current at 3.0 V <ul style="list-style-type: none"> at 25 °C and below at 50 °C at 85 °C at 105 °C | — | 2.2 | 2.71 | μA | — |
| | | — | 3.9 | 6.63 | | |
| | | — | 13.9 | 18.25 | | |
| | | — | 28.4 | 36.59 | | |
| I _{DD_VLPS} | Very-low-power stop mode current at 1.8 V <ul style="list-style-type: none"> at 25 °C and below at 50 °C | — | 2.2 | 2.674 | | — |
| | | — | 3.8 | 6.44 | | |

Table continues on the next page...

Table 10. KL03 QFN packages power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. ¹ | Unit | Notes |
|-----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|-------------------|------|-------|
| | <ul style="list-style-type: none"> at 85 °C at 105 °C | — | 13.2 | 17.37 | μA | |
| I _{DD_VLLS3} | Very-low-leakage stop mode 3 current, all peripheral disable, at 3.0 V <ul style="list-style-type: none"> at 25 °C and below at 50 °C at 85 °C at 105 °C | — | 1.08 | 1.17 | μA | — |
| I _{DD_VLLS3} | Very-low-leakage stop mode 3 current with RTC current, at 3.0 V <ul style="list-style-type: none"> at 25 °C and below at 50 °C at 85 °C at 105 °C | — | 1.47 | 1.56 | μA | — |
| I _{DD_VLLS3} | Very-low-leakage stop mode 3 current with RTC current, at 1.8 V <ul style="list-style-type: none"> at 25 °C and below at 50 °C at 85 °C at 105 °C | — | 1.33 | 1.42 | μA | — |
| I _{DD_VLLS1} | Very-low-leakage stop mode 1 current all peripheral disabled at 3.0 V <ul style="list-style-type: none"> at 25 °C and below at 50 °C at 85 °C at 105 °C | — | 566 | 690 | nA | — |
| I _{DD_VLLS1} | Very-low-leakage stop mode 1 current RTC enabled at 3.0 V <ul style="list-style-type: none"> at 25 °C and below at 50 °C at 85 °C at 105 °C | — | 969 | 1059 | nA | — |
| I _{DD_VLLS1} | Very-low-leakage stop mode 1 current RTC enabled at 1.8 V <ul style="list-style-type: none"> at 25 °C and below at 50 °C at 85 °C at 105 °C | — | 826 | 916 | nA | — |

Table continues on the next page...

Table 10. KL03 QFN packages power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. ¹ | Unit | Notes |
|-----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|-------------------|------|-------|
| I _{DD_VLLS0} | Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 0) at 3.0 V <ul style="list-style-type: none"> at 25 °C and below at 50 °C at 85 °C at 105 °C | — | 265 | 373 | nA | — |
| I _{DD_VLLS0} | Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 1) at 3 V <ul style="list-style-type: none"> at 25 °C and below at 50 °C at 85 °C at 105 °C | — | 77 | 350 | nA | 4 |
| | | — | 255 | 465.70 | | |
| | | — | 1640 | 1994 | | |
| | | — | 4080 | 4956 | | |

1. The maximum values represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).
2. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
3. MCG_Lite configured for HIRC mode. CoreMark benchmark compiled using IAR 7.10 with optimization level high, optimized for balanced.
4. No brownout

Table 11. KL03 WLCSP package power consumption operating behaviors

| Symbol | Description | Min. | Typ. | Max. ¹ | Unit | Notes |
|-----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|-------------------|------|-------|
| I _{DDA} | Analog supply current | — | — | See note | mA | 2 |
| I _{DD_RUNCO} | Running CoreMark in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C at 85 °C | — | 5.49 | 5.71 | mA | 3 |
| | | — | 5.59 | 5.81 | | |
| I _{DD_RUNCO} | Running While(1) loop in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C at 85 °C | — | 5.16 | 5.37 | mA | 3 |
| | | — | 5.24 | 5.45 | | |
| I _{DD_RUN} | Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 48 MHz core/24 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C at 85 °C | — | 6.03 | 6.27 | mA | 3 |
| | | — | 6.13 | 6.38 | | |

Table continues on the next page...

Table 11. KL03 WLCSP package power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. ¹ | Unit | Notes |
|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|--------------|-------------------|------|-------|
| I _{DD_RUN} | Run mode current—48M HIRC mode, running CoreMark in flash all peripheral clock disable, 24 MHz core/12 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C at 85 °C | — — | 3.71 3.78 | 3.86 3.93 | mA | 3 |
| I _{DD_RUN} | Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 12 MHz core/6 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C at 85 °C | — — | 2.47 2.55 | 2.57 2.65 | mA | 3 |
| I _{DD_RUN} | Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock enable 48 MHz core/24 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C at 85 °C | — — | 6.43 6.53 | 6.69 6.79 | mA | 3 |
| I _{DD_RUN} | Run mode current—48M HIRC mode, running While(1) loop in flash all peripheral clock disable, 48 MHz core/24 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C at 85 °C | — — | 5.71 5.79 | 5.94 6.02 | mA | — |
| I _{DD_RUN} | Run mode current—48M HIRC mode, running While(1) loop in Flash all peripheral clock disable, 24 MHz core/12 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C at 85 °C | — — | 3.3 3.37 | 3.43 3.50 | mA | — |
| I _{DD_RUN} | Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock disable, 12 MHz core/6 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C at 85 °C | — — | 2.28 2.35 | 2.37 2.44 | mA | — |
| I _{DD_RUN} | Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock enable, 48 MHz core/24 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C at 85 °C | — — | 6.1 6.19 | 6.34 6.44 | mA | — |
| I _{DD_RUN} | Run mode current—48M HIRC mode, running While(1) loop in SRAM all peripheral clock disable, 48 MHz core/24 MHz flash, V _{DD} = 3.0 V | — — | 3.14 3.24 | 3.23 3.33 | mA | — |

Table continues on the next page...

Table 11. KL03 WLCSP package power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. ¹ | Unit | Notes |
|------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|--------------|-------------------|------|-------|
| | <ul style="list-style-type: none"> at 25 °C at 85 °C | | | | | |
| I _{DD_RUN} | Run mode current—48M HIRC mode, running While(1) loop in SRAM all peripheral clock enable, 48 MHz core/24 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C at 85 °C | — — | 3.54 3.64 | 3.63 3.73 | mA | — |
| I _{DD_VLPRCO} | Very-low-power run While(1) loop in flash in compute operation mode— 2 MHz LIRC mode, 2 MHz core/0.5 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C | — | 500 | 750 | μA | — |
| I _{DD_VLPRCO} | Very-low-power-run While(1) loop in SRAM in compute operation mode— 8 MHz LIRC mode, 4 MHz core / 1 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C | — | 188 | 217 | μA | — |
| I _{DD_VLPRCO} | Very-low-power run While(1) loop in SRAM in compute operation mode:—2 MHz LIRC mode, 2 MHz core / 0.5 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C | — | 82 | 123 | μA | — |
| I _{DD_VLPR} | Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 2 MHz core / 0.5 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C | — | 503 | 754 | μA | — |
| I _{DD_VLPR} | Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 125 kHz core / 31.25 kHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C | — | 60 | 90 | μA | — |
| I _{DD_VLPR} | Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock enable, 2 MHz core / 0.5 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C | — | 516 | 774 | μA | — |
| I _{DD_VLPR} | Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in SRAM in all peripheral clock disable, 4 MHz core / 1 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C | — | 209 | 350 | μA | — |
| I _{DD_VLPR} | Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in SRAM all peripheral clock enable, 4 MHz core / 1 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C | — | 229 | 370 | μA | — |
| I _{DD_VLPR} | Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM in all | | | | | — |

Table continues on the next page...

Table 11. KL03 WLCSP package power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. ¹ | Unit | Notes |
|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|-------------------|---------------------------|---------|-------|
| | peripheral clock disable, 2 MHz core / 0.5 MHz flash, $V_{DD} = 3.0$ V • at 25 °C | — | 93 | 140 | μ A | |
| I_{DD_VLPR} | Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM all peripheral clock disable, 125 kHz core / 31.25 kHz flash, $V_{DD} = 3.0$ V • at 25 °C | — | 31 | 81 | μ A | — |
| I_{DD_VLPR} | Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM all peripheral clock enable, 2 MHz core / 0.5 MHz flash, $V_{DD} = 3.0$ V • at 25 °C | — | 103 | 154 | μ A | — |
| I_{DD_WAIT} | Wait mode current—core disabled, 48 MHz system/24 MHz bus, flash disabled (flash doze enabled), all peripheral clocks disabled, MCG_Lite under HIRC mode, $V_{DD} = 3.0$ V | — | 1.4 | 1.94 | mA | — |
| I_{DD_WAIT} | Wait mode current—core disabled, 24 MHz system/12 MHz bus, flash disabled (flash doze enabled), all peripheral clocks disabled, MCG_Lite under HIRC mode, $V_{DD} = 3.0$ V | — | 1.02 | 1.24 | mA | — |
| I_{DD_VLPW} | Very-low-power wait mode current, core disabled, 4 MHz system/ 1 MHz bus and flash, all peripheral clocks disabled, $V_{DD} = 3.0$ V | — | 121 | 181 | μ A | — |
| I_{DD_VLPW} | Very-low-power wait mode current, core disabled, 2 MHz system/ 0.5 MHz bus and flash, all peripheral clocks disabled, $V_{DD} = 3.0$ V | — | 59 | 97 | μ A | — |
| I_{DD_VLPW} | Very-low-power wait mode current, core disabled, 125 kHz system/ 31.25 kHz bus and flash, all peripheral clocks disabled, $V_{DD} = 3.0$ V | — | 28 | 42 | μ A | — |
| I_{DD_PSTOP2} | Partial Stop 2, core and system clock disabled, 12 MHz bus and flash, $V_{DD} = 3.0$ V | — | 1.53 | 2.03 | mA | — |
| I_{DD_PSTOP2} | Partial Stop 2, core and system clock disabled, flash doze enabled, 12 MHz bus, $V_{DD} = 3.0$ V | — | 0.881 | 1.18 | mA | — |
| I_{DD_STOP} | Stop mode current at 3.0 V • at 25 °C and below • at 50 °C • at 85 °C | — — — | 158 164 187 | 175.7 179.48 199.54 | μ A | — |
| I_{DD_VLPS} | Very-low-power stop mode current at 3.0 V • at 25 °C and below | — — | 2.2 3.9 | 2.71 6.63 | | — |

Table continues on the next page...

Table 11. KL03 WLCSP package power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. ¹ | Unit | Notes |
|-----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|-------------------|------|-------|
| | <ul style="list-style-type: none"> at 50 °C at 85 °C | — | 13.9 | 18.25 | μA | |
| I _{DD_VLPS} | Very-low-power stop mode current at 1.8 V <ul style="list-style-type: none"> at 25 °C and below at 50 °C at 85 °C | — | 2.2 | 2.674 | μA | — |
| | | — | 3.8 | 6.44 | | |
| | | — | 13.2 | 17.37 | | |
| I _{DD_VLLS3} | Very-low-leakage stop mode 3 current, all peripheral disable, at 3.0 V <ul style="list-style-type: none"> at 25 °C and below at 50 °C at 85 °C | — | 1.08 | 1.17 | μA | — |
| | | — | 1.4 | 1.52 | | |
| | | — | 3.45 | 3.96 | | |
| I _{DD_VLLS3} | Very-low-leakage stop mode 3 current with RTC current, at 3.0 V <ul style="list-style-type: none"> at 25 °C and below at 50 °C at 85 °C | — | 1.47 | 1.56 | μA | — |
| | | — | 1.82 | 1.94 | | |
| | | — | 3.93 | 4.44 | | |
| I _{DD_VLLS3} | Very-low-leakage stop mode 3 current with RTC current, at 1.8 V <ul style="list-style-type: none"> at 25 °C and below at 50 °C at 85 °C | — | 1.33 | 1.42 | μA | — |
| | | — | 1.65 | 1.77 | | |
| | | — | 3.56 | 4.07 | | |
| I _{DD_VLLS1} | Very-low-leakage stop mode 1 current all peripheral disabled at 3.0 V <ul style="list-style-type: none"> at 25 °C and below at 50 °C at 85 °C | — | 566 | 690 | nA | — |
| | | — | 788 | 839 | | |
| | | — | 2270 | 2600 | | |
| I _{DD_VLLS1} | Very-low-leakage stop mode 1 current RTC enabled at 3.0 V <ul style="list-style-type: none"> at 25 °C and below at 50 °C at 85 °C | — | 969 | 1059 | nA | — |
| | | — | 1200 | 1251 | | |
| | | — | 2740 | 3070 | | |
| I _{DD_VLLS1} | Very-low-leakage stop mode 1 current RTC enabled at 1.8 V <ul style="list-style-type: none"> at 25 °C and below at 50 °C at 85 °C | — | 826 | 916 | nA | — |
| | | — | 1040 | 1091 | | |
| | | — | 2400 | 2730 | | |
| I _{DD_VLLS0} | Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 0) at 3.0 V | — | 265 | 373 | | — |

Table continues on the next page...

Table 11. KL03 WLCSP package power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. ¹ | Unit | Notes |
|-----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|-------------------|------|-------|
| | <ul style="list-style-type: none"> at 25 °C and below at 50 °C at 85 °C | — | 467 | 512.9 | nA | |
| I _{DD_VLLS0} | Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 1) at 3 V <ul style="list-style-type: none"> at 25 °C and below at 50 °C at 85 °C | — | 77 | 350 | nA | 4 |
| | | — | 255 | 465.70 | | |
| | | — | 1640 | 1994 | | |

1. The maximum values represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).
2. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
3. MCG_Lite configured for HIRC mode. CoreMark benchmark compiled using IAR 7.10 with optimization level high, optimized for balanced.
4. No brownout

Table 12. Low power mode peripheral adders — typical value

| Symbol | Description | Temperature (°C) | | | | | | Unit |
|----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|-----|-----|-----|-----|------------------|------|
| | | -40 | 25 | 50 | 70 | 85 | 105 ¹ | |
| I _{LIRC8MHz} | 8 MHz internal reference clock (LIRC) adder. Measured by entering STOP or VLPS mode with 8 MHz LIRC enabled, MCG_SC[FCRDIV]=000b, MCG_MC[LIRC_DIV2]=000b. | 68 | 68 | 68 | 68 | 68 | 68 | µA |
| I _{LIRC2MHz} | 2 MHz internal reference clock (LIRC) adder. Measured by entering STOP mode with the 2 MHz LIRC enabled, MCG_SC[FCRDIV]=000b, MCG_MC[LIRC_DIV2]=000b. | 27 | 27 | 27 | 27 | 27 | 27 | µA |
| I _{EREFSTEN32KHz} | External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled. <ul style="list-style-type: none"> VLLS1 VLLS3 VLPS STOP | 340 | 410 | 460 | 470 | 480 | 600 | nA |
| | | 340 | 410 | 460 | 490 | 530 | 600 | |
| | | 340 | 420 | 480 | 570 | 610 | 850 | |
| | | 340 | 420 | 480 | 570 | 610 | 850 | |
| I _{LPTMR} | LPTMR peripheral adder measured by placing the device in VLLS1 mode with LPTMR enabled using LPO. | 30 | 30 | 30 | 85 | 100 | 200 | nA |

Table continues on the next page...

Table 12. Low power mode peripheral adders — typical value (continued)

| Symbol | Description | Temperature (°C) | | | | | | Unit |
|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|-----|-----|-----|-----|------------------|------|
| | | -40 | 25 | 50 | 70 | 85 | 105 ¹ | |
| I_{CMP} | CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption. | 15 | 15 | 15 | 15 | 15 | 15 | μA |
| I_{RTC} | RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption. | 340 | 440 | 440 | 480 | 520 | 620 | nA |
| I_{UART} | UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption. <ul style="list-style-type: none"> LIRC8M (8 MHz internal reference clock) LIRC2M (2 MHz internal reference clock) | | | | | | | |
| | | 85 | 85 | 85 | 85 | 85 | 85 | μA |
| I_{TPM} | TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents. <ul style="list-style-type: none"> LIRC8M (8 MHz internal reference clock) LIRC2M (2 MHz internal reference clock) | 28 | 28 | 28 | 28 | 28 | 28 | |
| | | 93 | 93 | 93 | 93 | 93 | 93 | μA |
| I_{BG} | Bandgap adder when BGEN bit is set and device is placed in VLPx or VLLSx mode. | 35 | 35 | 35 | 35 | 35 | 35 | |
| | | 45 | 45 | 45 | 45 | 45 | 45 | μA |
| I_{ADC} | ADC peripheral adder combining the measured values at V_{DD} and V_{DDA} by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions. | 340 | 340 | 340 | 340 | 340 | 340 | μA |

1. For QFN packages only.

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG-Lite in HIRC for run mode, and LIRC for VLPR mode
- No GPIOs toggled
- Code execution from flash
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

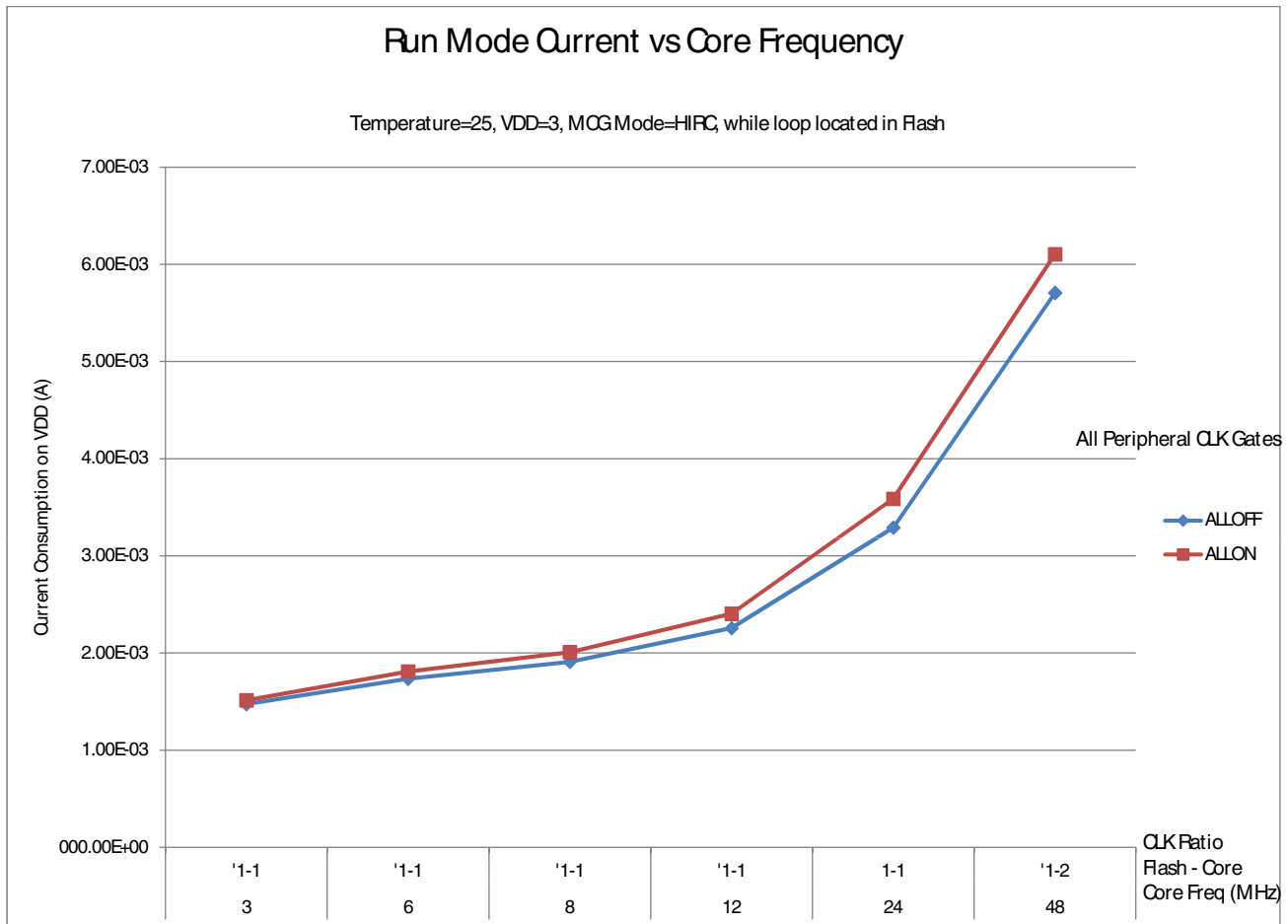


Figure 3. Run mode supply current vs. core frequency (loop located in flash)

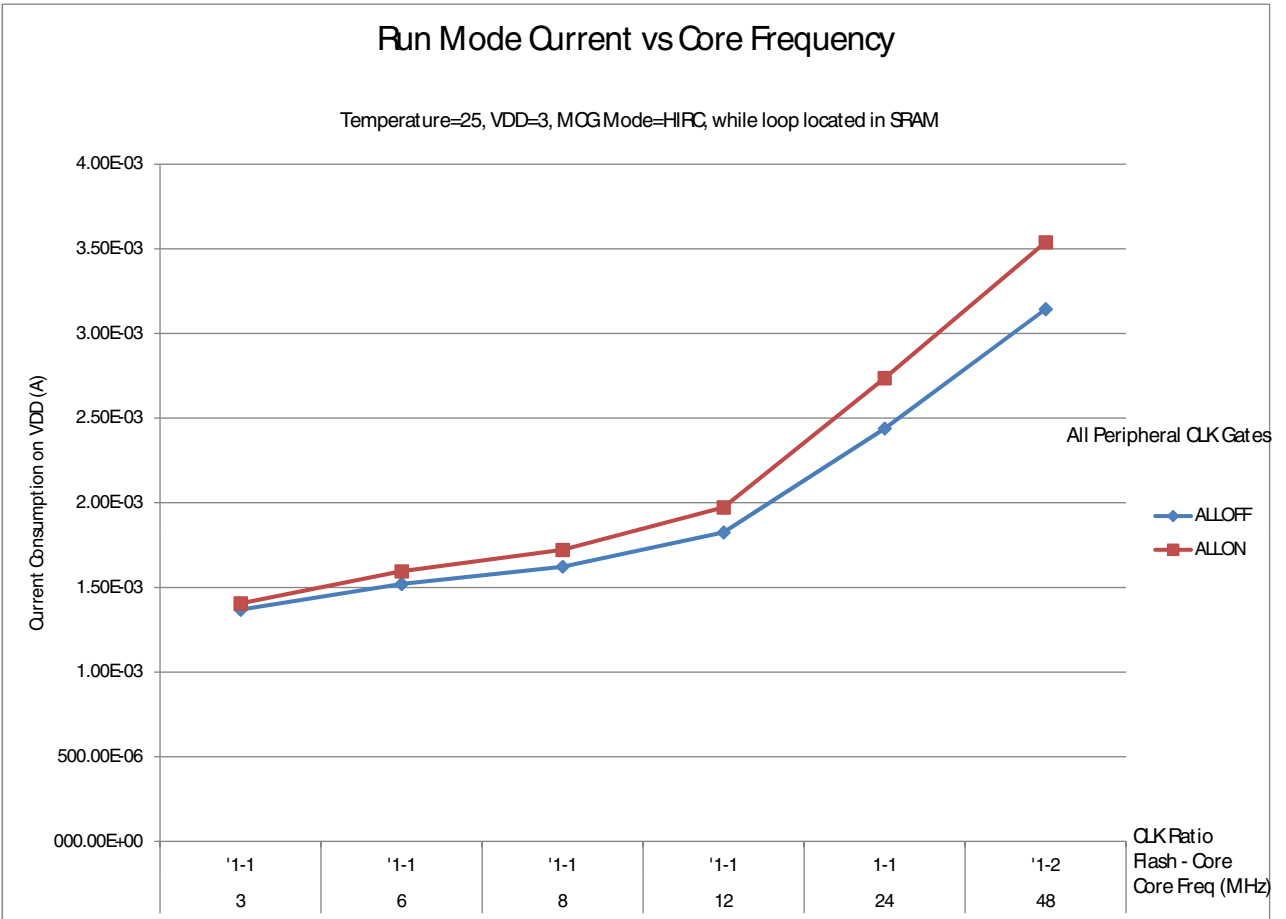


Figure 4. Run mode supply current vs. core frequency (loop located in SRAM)

General

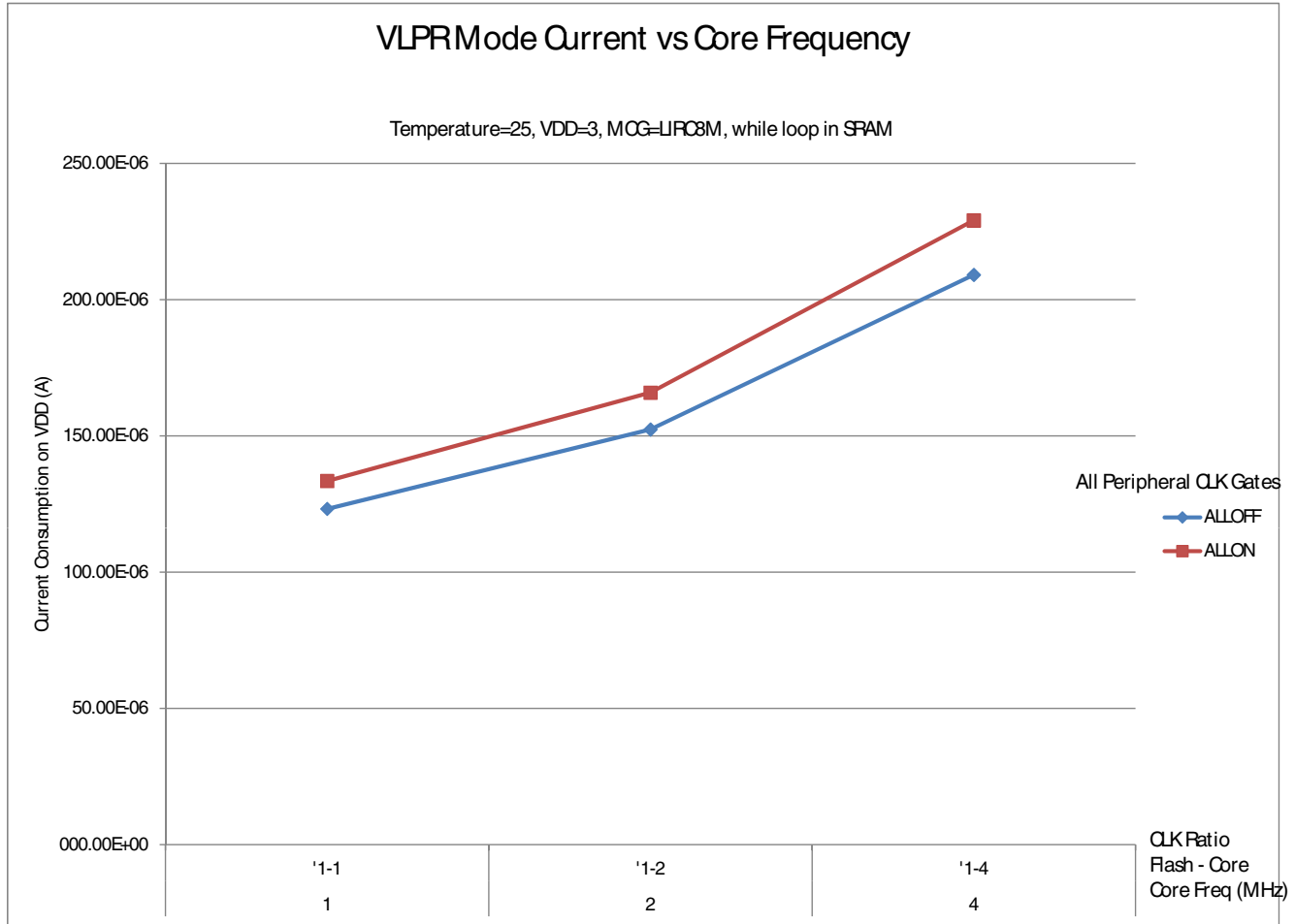


Figure 5. VLPR mode current vs. core frequency (loop in SRAM)

2.2.6 EMC radiated emissions operating behaviors

Table 13. EMC radiated emissions operating behaviors for 24-pin QFN package

| Symbol | Description | Frequency band (MHz) | Typ. | Unit | Notes |
|---------------------|------------------------------------|----------------------|------|------|-------|
| V _{RE1} | Radiated emissions voltage, band 1 | 0.15–50 | 5 | dBμV | 1, 2 |
| V _{RE2} | Radiated emissions voltage, band 2 | 50–150 | 7 | dBμV | |
| V _{RE3} | Radiated emissions voltage, band 3 | 150–500 | 5 | dBμV | |
| V _{RE4} | Radiated emissions voltage, band 4 | 500–1000 | 5 | dBμV | |
| V _{RE_IEC} | IEC/SAE level | 0.15–1000 | N | — | 2, 3 |

1. Determined according to IEC 61967-2 (and SAE J1752/3) radiated radio frequency (RF) emissions measurement standard. Typical Configuration: Appendix B: DUT Software Configuration—2. Typical Configuration.
2. V_{DD} = 3.3 V, T_A = 25 °C, f_{irc48m} = 48 MHz, f_{SYS} = 48 MHz, f_{BUS} = 24 MHz
3. IEC/SAE Level Maximums: N≤12 dBμV, M≤18 dBμV, L≤24 dBμV, K≤30 dBμV, I ≤ 36 dBμV, H ≤ 42 dBμV, G≤48 dBμV.

2.2.7 EMC Radiated Emissions Web Search Procedure boilerplate

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.nxp.com.
2. Perform a keyword search for "EMC design"

2.2.8 Capacitance attributes

Table 14. Capacitance attributes

| Symbol | Description | Min. | Max. | Unit |
|----------|-------------------|------|------|------|
| C_{IN} | Input capacitance | — | 7 | pF |

2.3 Switching specifications

2.3.1 Device clock specifications

Table 15. Device clock specifications

| Symbol | Description | Min. | Max. | Unit |
|----------------------------------|--------------------------------|------|--------|------|
| Normal run mode | | | | |
| f_{SYS} | System and core clock | — | 48 | MHz |
| f_{BUS} | Bus clock | — | 24 | MHz |
| f_{FLASH} | Flash clock | — | 24 | MHz |
| f_{LPTMR} | LPTMR clock | — | 24 | MHz |
| VLPR and VLPS modes ¹ | | | | |
| f_{SYS} | System and core clock | — | 4 | MHz |
| f_{BUS} | Bus clock | — | 1 | MHz |
| f_{FLASH} | Flash clock | — | 1 | MHz |
| f_{LPTMR} | LPTMR clock ² | — | 24 | MHz |
| f_{ERCLK} | External reference clock | — | 16 | MHz |
| f_{ERCLK} | External reference clock | — | 32.768 | kHz |
| f_{LPTMR_ERCLK} | LPTMR external reference clock | — | 16 | MHz |
| f_{TPM} | TPM asynchronous clock | — | 8 | MHz |
| f_{UART0} | UART0 asynchronous clock | — | 8 | MHz |

General

1. The frequency limitations in VLPR and VLPS modes here override any frequency specification listed in the timing specification for any other module. These same frequency limits apply to VLPS, whether VLPS was entered from RUN or from VLPR.
2. The LPTMR can be clocked at this speed in VLPR or VLPS only when the source is an external pin.

2.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO and UART signals.

Table 16. General switching specifications

| Description | Min. | Max. | Unit | Notes |
|------------------------------------------------------------------------------------|------|------|------------------|-------|
| GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path | 1.5 | — | Bus clock cycles | 1 |
| External RESET and NMI pin interrupt pulse width — Asynchronous path | 100 | — | ns | 2 |
| GPIO pin interrupt pulse width — Asynchronous path | 16 | — | ns | 2 |
| Port rise and fall time | — | 36 | ns | 3 |

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. 75 pF load

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 17. Thermal operating requirements of WLCSP package

| Symbol | Description | Min. | Max. | Unit | Note |
|----------------|--------------------------|------|------|------|------|
| T _J | Die junction temperature | -40 | 95 | °C | |
| T _A | Ambient temperature | -40 | 85 | °C | 1 |

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA} \times \text{chip power dissipation}$.

Table 18. Thermal operating requirements of other packages

| Symbol | Description | Min. | Max. | Unit | Note |
|----------------|--------------------------|------|------|------|------|
| T _J | Die junction temperature | -40 | 125 | °C | |
| T _A | Ambient temperature | -40 | 105 | °C | 1 |

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA} \times \text{chip power dissipation}$.

2.4.2 Thermal attributes

Table 19. Thermal attributes

| Board type | Symbol | Description | 16 QFN | 20 WLCSP | 24 QFN | Unit | Notes |
|-------------------|------------------|----------------------------------------------------------------------------------------------------|--------|----------|--------|------|-------|
| Single-layer (1S) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 64.2 | 69.8 | 60.7 | °C/W | 1,2 |
| Four-layer (2s2p) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 53.3 | 57.5 | 48.5 | °C/W | 1,2,3 |
| Single-layer (1S) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 55.4 | 62.03 | 51.0 | °C/W | 1,3 |
| Four-layer (2s2p) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 48.9 | 54.3 | 43.6 | °C/W | 1,3 |
| — | $R_{\theta JB}$ | Thermal resistance, junction to board | 33.5 | 51.64 | 30.4 | °C/W | 4 |
| — | $R_{\theta JC}$ | Thermal resistance, junction to case | 20.9 | 0.73 | 9.8 | °C/W | 5 |
| — | Ψ_{JT} | Thermal characterization parameter, junction to package top outside center (natural convection) | 0.2 | 0.2 | 0.2 | °C/W | 6 |
| — | Ψ_{JB} | Thermal characterization parameter, junction to package bottom outside center (natural convection) | 22.4 | — | 21.8 | °C/W | 7 |

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 SWD electricals

Table 20. SWD full voltage range electricals

| Symbol | Description | Min. | Max. | Unit |
|--------|-------------------------------------------------------|------|------|------|
| | Operating voltage | 1.71 | 3.6 | V |
| J1 | SWD_CLK frequency of operation • Serial wire debug | 0 | 25 | MHz |
| J2 | SWD_CLK cycle period | 1/J1 | — | ns |
| J3 | SWD_CLK clock pulse width • Serial wire debug | 20 | — | ns |
| J4 | SWD_CLK rise and fall times | — | 3 | ns |
| J9 | SWD_DIO input data setup time to SWD_CLK rise | 10 | — | ns |
| J10 | SWD_DIO input data hold time after SWD_CLK rise | 0 | — | ns |
| J11 | SWD_CLK high to SWD_DIO data valid | — | 32 | ns |
| J12 | SWD_CLK high to SWD_DIO high-Z | 5 | — | ns |

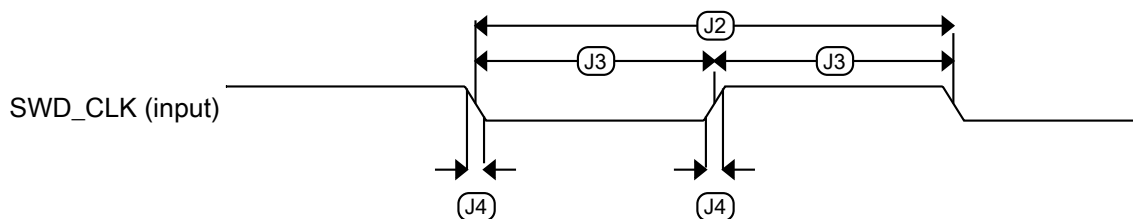


Figure 6. Serial wire clock input timing

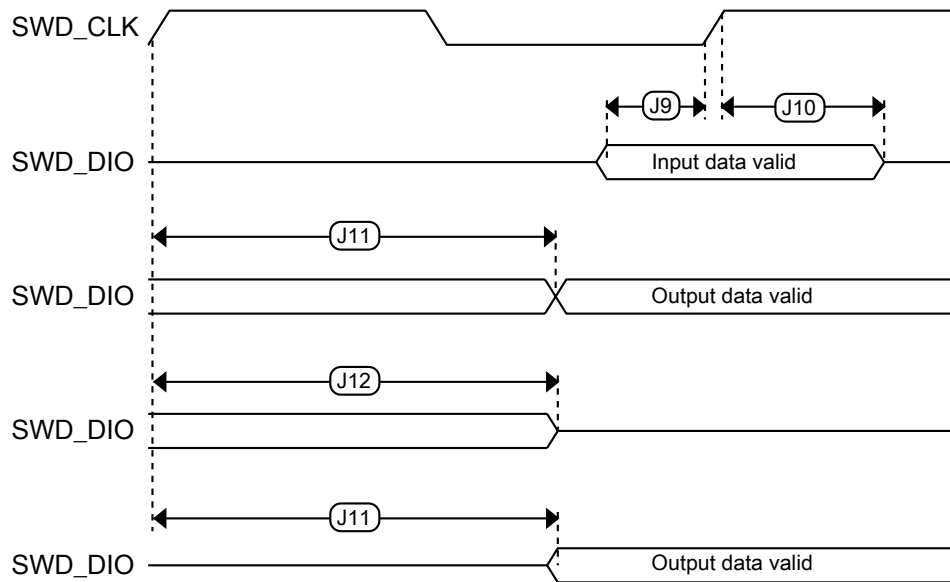


Figure 7. Serial wire data timing

3.2 System modules

There are no specifications necessary for the device's system modules.

3.3 Clock modules

3.3.1 MCG-Lite specifications

Table 21. HIRC48M specification

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-----------------------------|---------------------------------------------------------------------------------------|------|-----------|-----------|----------------|-------|
| V_{DD} | Supply voltage | 1.71 | — | 3.6 | V | — |
| I_{DD48M} | Supply current | — | 400 | 500 | μA | — |
| f_{irc48m} | Internal reference frequency | — | 48 | — | MHz | — |
| $\Delta f_{irc48m_ol_lv}$ | total deviation of IRC48M frequency at low voltage (VDD=1.71V-1.89V) over temperature | — | ± 0.5 | ± 1.5 | $\%f_{irc48m}$ | — |

Table continues on the next page...

Table 21. HIRC48M specification (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-----------------------------|---------------------------------------------------------------------------------------|------|-------|------|----------------|-------|
| $\Delta f_{irc48m_ol_hv}$ | total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over temperature | — | ± 0.5 | ±1.0 | % f_{irc48m} | — |
| J_{cyc_irc48m} | Period Jitter (RMS) | — | 35 | 150 | ps | — |
| $t_{irc48mst}$ | Startup time | — | 2 | 3 | μs | 1 |

1. IRC48M startup time is defined as the time between clock enablement and clock availability for system use. Enable the clock by setting MCG_MC[HIRCEN] = 1. See reference manual for details.

Table 22. LIRC8M/2M specification

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|------------------|----------------------------------|------|------|------|-------------|----------------------|
| V_{DD} | Supply voltage | 1.08 | — | 1.47 | V | — |
| T | Temperature range | -40 | — | 125 | °C | — |
| I_{DD_2M} | Supply current in 2 MHz mode | — | 14 | 17 | μA | — |
| I_{DD_8M} | Supply current in 8 MHz mode | — | 30 | 35 | μA | — |
| f_{IRC_2M} | Output frequency | — | 2 | — | MHz | — |
| f_{IRC_8M} | Output frequency | — | 8 | — | MHz | — |
| $f_{IRC_T_2M}$ | Output frequency range (trimmed) | — | — | ±3 | % f_{IRC} | $V_{DD} \geq 1.89$ V |
| $f_{IRC_T_8M}$ | Output frequency range (trimmed) | — | — | ±3 | % f_{IRC} | $V_{DD} \geq 1.89$ V |
| T_{su_2M} | Startup time | — | — | 12.5 | μs | — |
| T_{su_8M} | Startup time | — | — | 12.5 | μs | — |

3.3.2 Oscillator electrical specifications

3.3.2.1 Oscillator DC electrical specifications

Table 23. Oscillator DC electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-------------|---------------------------------------------------|------|------|------|------|-------|
| V_{DD} | Supply voltage | 1.71 | — | 3.6 | V | — |
| I_{DDOSC} | Supply current — low-power mode • 32 kHz | — | 500 | — | nA | 1 |
| C_x | EXTAL load capacitance | — | — | — | | 2, 3 |
| C_y | XTAL load capacitance | — | — | — | | 2, 3 |
| R_F | Feedback resistor — low-frequency, low-power mode | — | — | — | MΩ | 2, 4 |
| R_S | Series resistor — low-frequency, low-power mode | — | — | — | kΩ | — |

Table continues on the next page...

Table 23. Oscillator DC electrical specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|------------|-----------------------------------------------------------------------------------------|------|------|------|------|-------|
| V_{pp}^5 | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode | — | 0.6 | — | V | — |

1. $V_{DD}=3.3$ V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x, C_y can be provided by using either the integrated capacitors or by using external components.
4. When low power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

3.3.2.2 Oscillator frequency specifications

Table 24. Oscillator frequency specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-----------------|----------------------------------------------------------------|------|------|------|------|-------|
| f_{osc_lo} | Oscillator crystal or resonator frequency — low frequency mode | 32 | — | 40 | kHz | — |
| t_{dc_extal} | Input clock duty cycle (external clock mode) | 40 | 50 | 60 | % | — |
| t_{cst} | Crystal startup time — 32 kHz low-frequency, low-power mode | — | 750 | — | ms | 1, 2 |

1. Proper PC board layout procedures must be followed to achieve specifications.
2. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

3.4 Memories and memory interfaces

3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 25. NVM program/erase timing specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|----------------|------------------------------------|------|------|------|---------|-------|
| t_{hvpgm4} | Longword Program high-voltage time | — | 7.5 | 18 | μ s | — |
| $t_{hversscr}$ | Sector Erase high-voltage time | — | 13 | 113 | ms | 1 |
| $t_{hversall}$ | Erase All high-voltage time | — | 52 | 452 | ms | 1 |

Peripheral operating requirements and behaviors

1. Maximum time based on expectations at cycling end-of-life.

3.4.1.2 Flash timing specifications — commands

Table 26. Flash command timing specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|----------------|-----------------------------------------------|------|------|------|---------|-------|
| $t_{rd1sec1k}$ | Read 1s Section execution time (flash sector) | — | — | 60 | μ s | 1 |
| t_{pgmchk} | Program Check execution time | — | — | 45 | μ s | 1 |
| t_{rdsrc} | Read Resource execution time | — | — | 30 | μ s | 1 |
| t_{pgm4} | Program Longword execution time | — | 65 | 145 | μ s | — |
| t_{ersscr} | Erase Flash Sector execution time | — | 14 | 114 | ms | 2 |
| t_{rd1all} | Read 1s All Blocks execution time | — | — | 0.5 | ms | — |
| t_{rdonce} | Read Once execution time | — | — | 25 | μ s | 1 |
| $t_{pgmonce}$ | Program Once execution time | — | 65 | — | μ s | — |
| t_{ersall} | Erase All Blocks execution time | — | 61 | 500 | ms | 2 |
| t_{vfykey} | Verify Backdoor Access Key execution time | — | — | 30 | μ s | 1 |

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

3.4.1.3 Flash high voltage current behaviors

Table 27. Flash high voltage current behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---------------|-----------------------------------------------------------------------|------|------|------|------|
| I_{DD_PGM} | Average current adder during high voltage flash programming operation | — | 2.5 | 6.0 | mA |
| I_{DD_ERS} | Average current adder during high voltage flash erase operation | — | 1.5 | 4.0 | mA |

3.4.1.4 Reliability specifications

Table 28. NVM reliability specifications

| Symbol | Description | Min. | Typ. ¹ | Max. | Unit | Notes |
|------------------|----------------------------------------|------|-------------------|------|--------|-------|
| Program Flash | | | | | | |
| $t_{nvmretp10k}$ | Data retention after up to 10 K cycles | 5 | 50 | — | years | — |
| $t_{nvmretp1k}$ | Data retention after up to 1 K cycles | 20 | 100 | — | years | — |
| $n_{nvmcycp}$ | Cycling endurance | 10 K | 50 K | — | cycles | 2 |

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at $-40\text{ °C} \leq T_j \leq 125\text{ °C}$.

3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

3.6 Analog

3.6.1 ADC electrical specifications

All ADC channels meet the 12-bit single-ended accuracy specifications.

3.6.1.1 12-bit ADC operating conditions

Table 29. 12-bit ADC operating conditions

| Symbol | Description | Conditions | Min. | Typ. ¹ | Max. | Unit | Notes |
|------------------|-------------------------------------|----------------------------------------------------------------------------------------------------------------|------------|-------------------|------------|------------|-------|
| V_{DDA} | Supply voltage | Absolute | 1.71 | — | 3.6 | V | — |
| ΔV_{DDA} | Supply voltage | Delta to V_{DD} ($V_{DD} - V_{DDA}$) | -100 | 0 | +100 | mV | 2 |
| ΔV_{SSA} | Ground voltage | Delta to V_{SS} ($V_{SS} - V_{SSA}$) | -100 | 0 | +100 | mV | 2 |
| V_{REFH} | ADC reference voltage high | | 1.13 | V_{DDA} | V_{DDA} | V | 3 |
| V_{REFL} | ADC reference voltage low | | V_{SSA} | V_{SSA} | V_{SSA} | V | 3 |
| V_{ADIN} | Input voltage | | V_{REFL} | — | V_{REFH} | V | — |
| C_{ADIN} | Input capacitance | • 8-bit / 10-bit / 12-bit modes | — | 4 | 5 | pF | — |
| R_{ADIN} | Input series resistance | | — | 2 | 5 | k Ω | — |
| R_{AS} | Analog source resistance (external) | 12-bit modes $f_{ADCK} < 4$ MHz | — | — | 5 | k Ω | 4 |
| f_{ADCK} | ADC conversion clock frequency | \leq 12-bit mode | 1.0 | — | 18.0 | MHz | 5 |
| C_{rate} | ADC conversion rate | \leq 12-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time | 20.000 | — | 818.330 | Ksps | 6 |

1. Typical values assume $V_{DDA} = 3.0$ V, Temp = 25 °C, $f_{ADCK} = 1.0$ MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.

Table 30. 12-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

| Symbol | Description | Conditions ¹ . | Min. | Typ. ² | Max. | Unit | Notes |
|---------------------|----------------------------|-------------------------------------------------|------------------------|-------------------|--------------|------------------|----------------------------------------------------------------------------------------------|
| DNL | Differential non-linearity | • 12-bit modes | — | ±0.9 | -1.1 to +1.9 | LSB ⁴ | 5 |
| | | • <12-bit modes | — | ±0.4 | -0.3 to 0.5 | | |
| INL | Integral non-linearity | • 12-bit modes | — | ±1.5 | -2.7 to +1.9 | LSB ⁴ | 5 |
| | | • <12-bit modes | — | ±0.5 | -0.7 to +0.5 | | |
| E _{FS} | Full-scale error | • 12-bit modes | — | 5 | — | LSB ⁴ | V _{ADIN} = V _{DDA} ⁵ |
| | | • <12-bit modes | — | 2 | 3 | | |
| E _Q | Quantization error | • 12-bit modes | — | — | ±0.5 | LSB ⁴ | |
| E _{IL} | Input leakage error | | $I_{in} \times R_{AS}$ | | | mV | I _{in} = leakage current (refer to the MCU's voltage and current operating ratings) |
| | Temp sensor slope | Across the full temperature range of the device | 1.55 | 1.62 | 1.69 | mV/°C | 6 |
| V _{TEMP25} | Temp sensor voltage | 25 °C | 706 | 716 | 726 | mV | 6 |

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
2. Typical values assume $V_{DDA} = 3.0$ V, Temp = 25 °C, $f_{ADCK} = 2.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. ADC conversion clock < 3 MHz

Table 31. 12-bit ADC characteristics ($V_{REFH} = V_{REFO}$, $V_{REFL} = V_{SSA}$)

| Symbol | Description | Conditions ¹ . | Min. | Typ. ² | Max. | Unit | Notes |
|----------------------|-------------------------------|---------------------------|-------|-------------------|------|------|-------------------------------------------|
| I _{DDA_ADC} | Supply current | | 0.215 | — | 1.7 | mA | 3 |
| f _{ADACK} | ADC asynchronous clock source | • ADLPC = 1, ADHSC = 0 | 1.2 | 2.4 | 3.9 | MHz | t _{ADACK} = 1/f _{ADACK} |
| | | • ADLPC = 1, ADHSC = 1 | 2.4 | 4.0 | 6.1 | MHz | |
| | | • ADLPC = 0, ADHSC = 0 | 3.0 | 5.2 | 7.3 | MHz | |
| | | • ADLPC = 0, ADHSC = 1 | 4.4 | 6.2 | 9.5 | MHz | |

Table continues on the next page...

Table 31. 12-bit ADC characteristics ($V_{REFH} = V_{REFO}$, $V_{REFL} = V_{SSA}$) (continued)

| Symbol | Description | Conditions ¹ | Min. | Typ. ² | Max. | Unit | Notes |
|---------------------|----------------------------|------------------------------------------------------------------------------------------|------------------------|-------------------|--------------|------------------|----------------------------------------------------------------------------------------------|
| | Sample Time | See Reference Manual chapter for sample times | | | | | |
| TUE | Total unadjusted error | <ul style="list-style-type: none"> 12-bit modes <12-bit modes | — | ±4 | ±6.8 | LSB ⁴ | 5 |
| | | | — | ±1.4 | ±2.1 | | |
| DNL | Differential non-linearity | <ul style="list-style-type: none"> 12-bit modes <12-bit modes | — | ±0.7 | -1.1 to +1.9 | LSB ⁴ | 5 |
| | | | — | ±0.2 | -0.3 to 0.5 | | |
| INL | Integral non-linearity | <ul style="list-style-type: none"> 12-bit modes <12-bit modes | — | ±1.0 | -2.7 to +1.9 | LSB ⁴ | 5 |
| | | | — | ±0.5 | -0.7 to +0.5 | | |
| E _{FS} | Full-scale error | <ul style="list-style-type: none"> 12-bit modes <12-bit modes | — | -4 | -5.4 | LSB ⁴ | V _{ADIN} = V _{DDA} ⁵ |
| | | | — | -1.4 | -1.8 | | |
| E _Q | Quantization error | <ul style="list-style-type: none"> 12-bit modes | — | — | ±0.5 | LSB ⁴ | |
| E _{IL} | Input leakage error | | $I_{in} \times R_{AS}$ | | | mV | I _{in} = leakage current (refer to the MCU's voltage and current operating ratings) |
| | Temp sensor slope | Across the full temperature range of the device | 1.55 | 1.62 | 1.69 | mV/°C | 6 |
| V _{TEMP25} | Temp sensor voltage | 25 °C | 706 | 716 | 726 | mV | 6 |

- All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{REFO}$
- Typical values assume $V_{REFO} = 1.2$ V, Temp = 25 °C, $f_{ADCK} = 2.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
- 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
- ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
- ADC conversion clock < 3 MHz

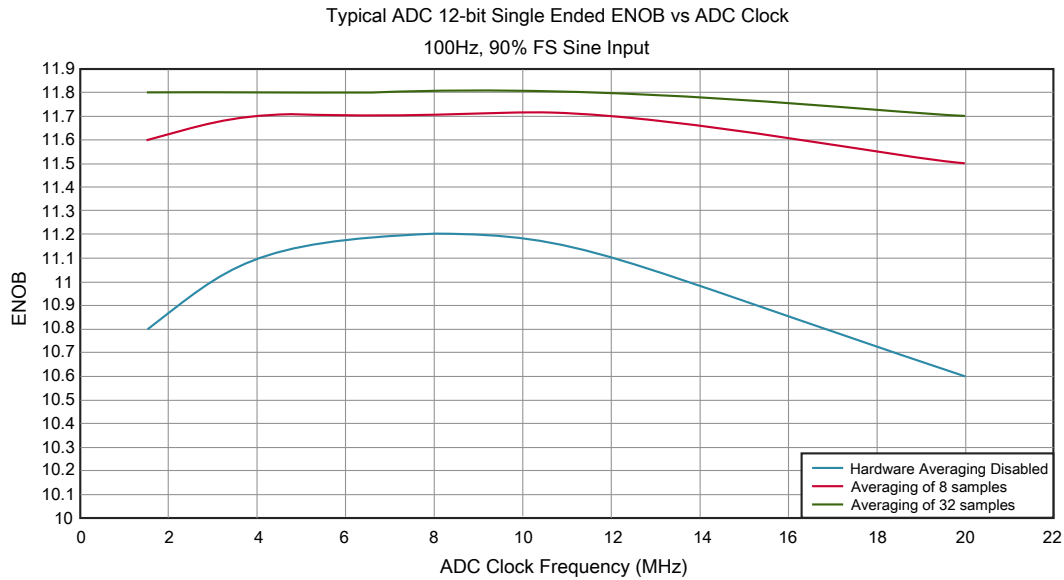


Figure 9. Typical ENOB vs. ADC_CLK for 12-bit single-ended mode

3.6.2 CMP and 6-bit DAC electrical specifications

Table 32. Comparator and 6-bit DAC electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit |
|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|---------------------|----------|---------|
| V_{DD} | Supply voltage | 1.71 | — | 3.6 | V |
| I_{DDHS} | Supply current, High-speed mode (EN=1, PMODE=1) | — | — | 200 | μ A |
| $I_{DDL S}$ | Supply current, low-speed mode (EN=1, PMODE=0) | — | — | 20 | μ A |
| V_{AIN} | Analog input voltage | $V_{SS} - 0.3$ | — | V_{DD} | V |
| V_{AIO} | Analog input offset voltage | — | — | 20 | mV |
| V_H | Analog comparator hysteresis ¹ <ul style="list-style-type: none"> • CR0[HYSTCTR] = 00 • CR0[HYSTCTR] = 01 • CR0[HYSTCTR] = 10 • CR0[HYSTCTR] = 11 | — | 5 10 20 30 | — | mV |
| V_{CMPOh} | Output high | $V_{DD} - 0.5$ | — | — | V |
| V_{CMPOl} | Output low | — | — | 0.5 | V |
| t_{DHS} | Propagation delay, high-speed mode (EN=1, PMODE=1) | 20 | 50 | 200 | ns |
| t_{DLS} | Propagation delay, low-speed mode (EN=1, PMODE=0) | 80 | 250 | 600 | ns |
| | Analog comparator initialization delay ² | — | — | 40 | μ s |

Table continues on the next page...

Table 32. Comparator and 6-bit DAC electrical specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit |
|--------------------|--------------------------------------|------|------|------|------------------|
| I _{DAC6b} | 6-bit DAC current adder (enabled) | — | 7 | — | μA |
| INL | 6-bit DAC integral non-linearity | -0.5 | — | 0.5 | LSB ³ |
| DNL | 6-bit DAC differential non-linearity | -0.3 | — | 0.3 | LSB |

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}-0.6 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB = V_{reference}/64

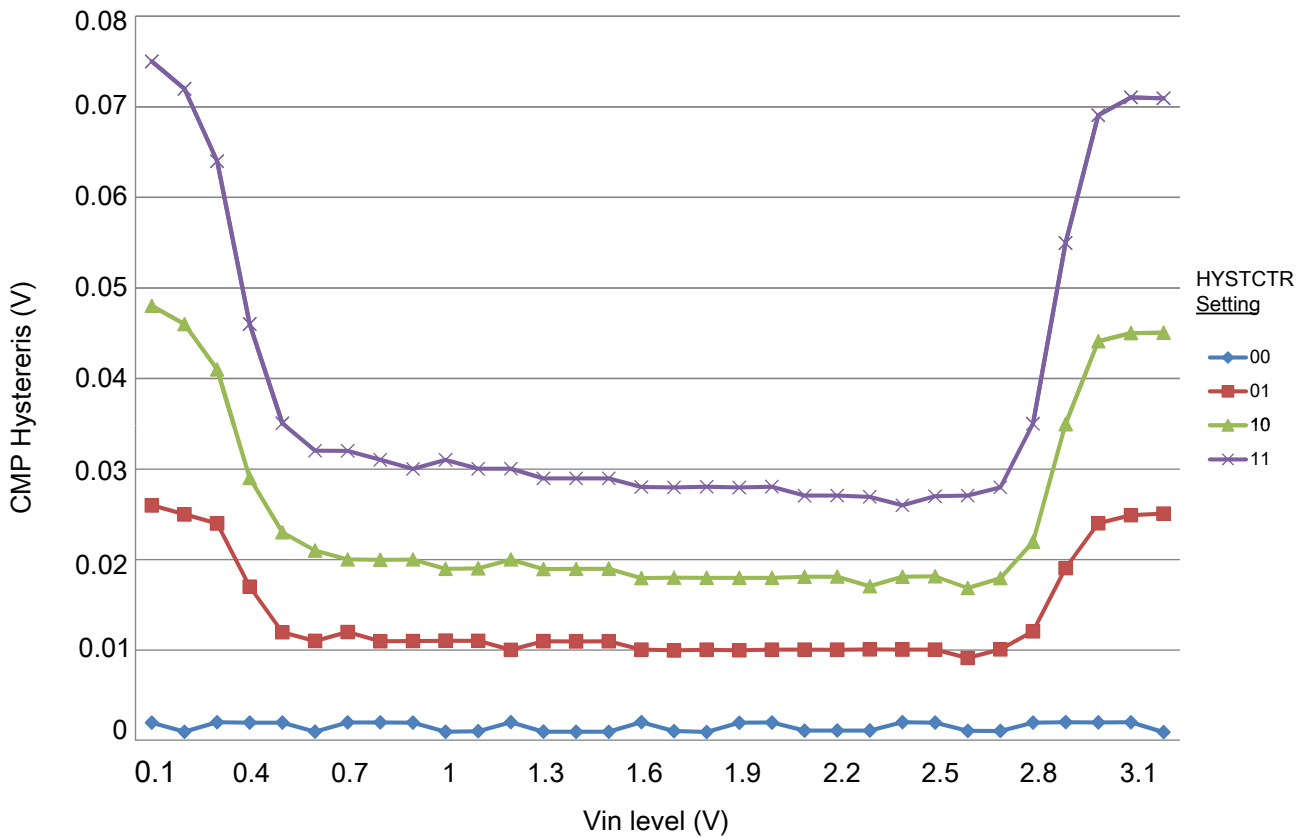


Figure 10. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

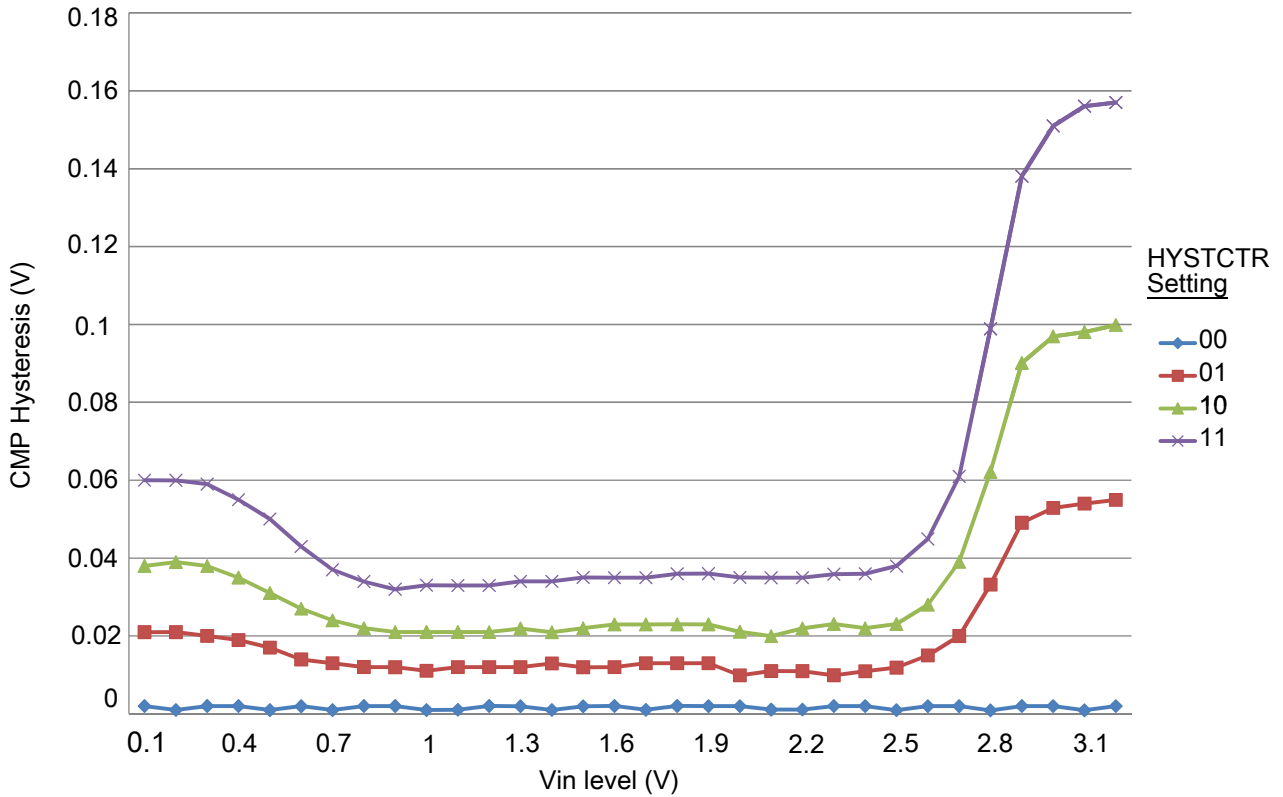


Figure 11. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

3.6.3 Voltage reference electrical specifications

Table 33. VREF full-range operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------------|-------------------------|-------------------------------------------|------|------|-------|
| V _{DDA} | Supply voltage | 1.71 | 3.6 | V | — |
| T _A | Temperature | Operating temperature range of the device | | °C | — |
| C _L | Output load capacitance | 100 | | nF | 1, 2 |

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

Table 34 is tested under the condition of setting VREF_TRM[CHOPEN], VREF_SC[REGEN] and VREF_SC[ICOMPEN] bits to 1.

Table 34. VREF full-range operating behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-------------------|---------------------------------------------------------------------------------------|--------|-------|--------|-------|-------|
| V_{out} | Voltage reference output with factory trim at nominal V_{DDA} and temperature=25C | 1.1915 | 1.195 | 1.1977 | V | 1 |
| V_{out} | Voltage reference output — factory trim | 1.1584 | — | 1.2376 | V | 1 |
| V_{out} | Voltage reference output — user trim | 1.193 | — | 1.197 | V | 1 |
| V_{step} | Voltage reference trim step | — | 0.5 | — | mV | 1 |
| V_{tdrift} | Temperature drift ($V_{max} - V_{min}$ across the full temperature range: 0 to 70°C) | — | — | 50 | mV | 1 |
| Ac | Aging coefficient | — | — | 400 | uV/yr | — |
| I_{bg} | Bandgap only current | — | — | 80 | μA | 1 |
| I_{lp} | Low-power buffer current | — | — | 360 | uA | 1 |
| I_{hp} | High-power buffer current | — | — | 1 | mA | 1 |
| ΔV_{LOAD} | Load regulation • current = ± 1.0 mA | — | 200 | — | μV | 1, 2 |
| T_{stup} | Buffer startup time | — | — | 100 | μs | — |
| V_{vdift} | Voltage drift ($V_{max} - V_{min}$ across the full voltage range) | — | 2 | — | mV | 1 |

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

Table 35. VREF limited-range operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|-------------|------|------|------|-------|
| T_A | Temperature | 0 | 50 | °C | — |

Table 36. VREF limited-range operating behaviors

| Symbol | Description | Min. | Max. | Unit | Notes |
|-----------|--------------------------------------------|-------|-------|------|-------|
| V_{out} | Voltage reference output with factory trim | 1.173 | 1.225 | V | — |

3.7 Timers

See [General switching specifications](#).

3.8 Communication interfaces

3.8.1 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all SPI pins.

Table 37. SPI master mode timing on slew rate disabled pads

| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|------|--------------|--------------------------------|-----------------------|--------------------------|-------------|------|
| 1 | f_{op} | Frequency of operation | $f_{periph}/2048$ | $f_{periph}/2$ | Hz | 1 |
| 2 | t_{SPSCK} | SPSCK period | $2 \times t_{periph}$ | $2048 \times t_{periph}$ | ns | 2 |
| 3 | t_{Lead} | Enable lead time | 1/2 | — | t_{SPSCK} | — |
| 4 | t_{Lag} | Enable lag time | 1/2 | — | t_{SPSCK} | — |
| 5 | t_{WSPSCK} | Clock (SPSCK) high or low time | $t_{periph} - 30$ | $1024 \times t_{periph}$ | ns | — |
| 6 | t_{SU} | Data setup time (inputs) | 22 | — | ns | — |
| 7 | t_{HI} | Data hold time (inputs) | 0 | — | ns | — |
| 8 | t_v | Data valid (after SPSCK edge) | — | 10 | ns | — |
| 9 | t_{HO} | Data hold time (outputs) | 0 | — | ns | — |
| 10 | t_{RI} | Rise time input | — | $t_{periph} - 25$ | ns | — |
| | t_{FI} | Fall time input | | | | |
| 11 | t_{RO} | Rise time output | — | 25 | ns | — |
| | t_{FO} | Fall time output | | | | |

1. For SPI0, f_{periph} is the bus clock (f_{BUS}).

2. $t_{periph} = 1/f_{periph}$

Table 38. SPI master mode timing on slew rate enabled pads

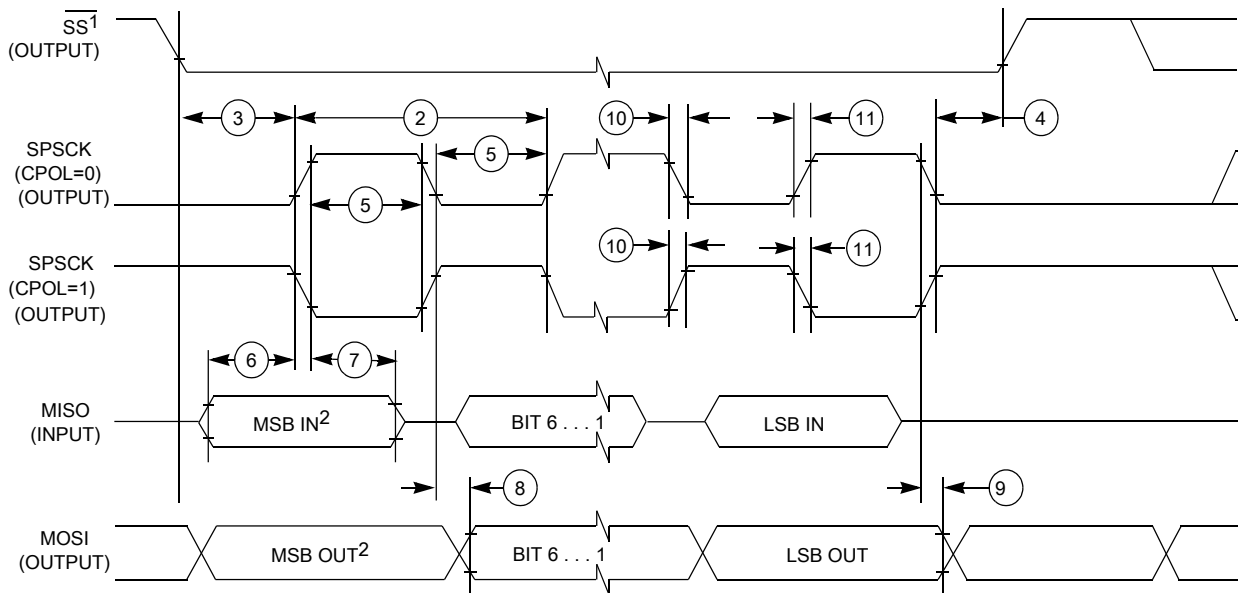
| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|------|-------------|------------------------|-----------------------|--------------------------|-------------|------|
| 1 | f_{op} | Frequency of operation | $f_{periph}/2048$ | $f_{periph}/2$ | Hz | 1 |
| 2 | t_{SPSCK} | SPSCK period | $2 \times t_{periph}$ | $2048 \times t_{periph}$ | ns | 2 |
| 3 | t_{Lead} | Enable lead time | 1/2 | — | t_{SPSCK} | — |
| 4 | t_{Lag} | Enable lag time | 1/2 | — | t_{SPSCK} | — |

Table continues on the next page...

Table 38. SPI master mode timing on slew rate enabled pads (continued)

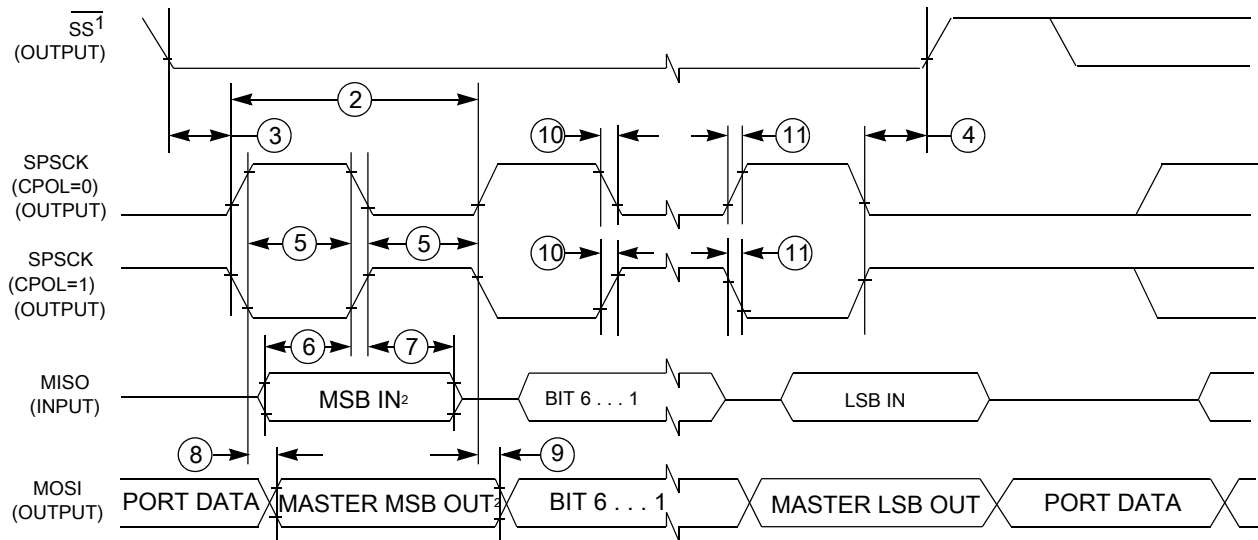
| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|------|--------------|--------------------------------|-------------------|--------------------------|------|------|
| 5 | t_{WSPSCK} | Clock (SPSCK) high or low time | $t_{periph} - 30$ | $1024 \times t_{periph}$ | ns | — |
| 6 | t_{SU} | Data setup time (inputs) | 96 | — | ns | — |
| 7 | t_{HI} | Data hold time (inputs) | 0 | — | ns | — |
| 8 | t_v | Data valid (after SPSCK edge) | — | 52 | ns | — |
| 9 | t_{HO} | Data hold time (outputs) | 0 | — | ns | — |
| 10 | t_{RI} | Rise time input | — | $t_{periph} - 25$ | ns | — |
| | t_{FI} | Fall time input | | | | |
| 11 | t_{RO} | Rise time output | — | 36 | ns | — |
| | t_{FO} | Fall time output | | | | |

1. For SPI0, f_{periph} is the bus clock (f_{BUS}).
2. $t_{periph} = 1/f_{periph}$



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 12. SPI master mode timing (CPHA = 0)



1. If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 13. SPI master mode timing (CPHA = 1)

Table 39. SPI slave mode timing on slew rate disabled pads

| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|------|---------------|---------------------------------|-----------------------|-------------------|--------------|------|
| 1 | f_{op} | Frequency of operation | 0 | $f_{periph}/4$ | Hz | 1 |
| 2 | t_{SPSCCK} | SPSCCK period | $4 \times t_{periph}$ | — | ns | 2 |
| 3 | t_{Lead} | Enable lead time | 1 | — | t_{periph} | — |
| 4 | t_{Lag} | Enable lag time | 1 | — | t_{periph} | — |
| 5 | $t_{WSPSCCK}$ | Clock (SPSCCK) high or low time | $t_{periph} - 30$ | — | ns | — |
| 6 | t_{SU} | Data setup time (inputs) | 3 | — | ns | — |
| 7 | t_{HI} | Data hold time (inputs) | 7 | — | ns | — |
| 8 | t_a | Slave access time | 23 | t_{periph} | ns | 3 |
| 9 | t_{dis} | Slave MISO disable time | 23 | t_{periph} | ns | 4 |
| 10 | t_v | Data valid (after SPSCCK edge) | — | 25.7 | ns | — |
| 11 | t_{HO} | Data hold time (outputs) | 0 | — | ns | — |
| 12 | t_{RI} | Rise time input | — | $t_{periph} - 25$ | ns | — |
| | t_{FI} | Fall time input | | | | |
| 13 | t_{RO} | Rise time output | — | 25 | ns | — |
| | t_{FO} | Fall time output | | | | |

1. For SPI0, f_{periph} is the bus clock (f_{BUS}).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

Table 40. SPI slave mode timing on slew rate enabled pads

| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|------|--------------|--------------------------------|-----------------------|-------------------|--------------|------|
| 1 | f_{op} | Frequency of operation | 0 | $f_{periph}/4$ | Hz | 1 |
| 2 | t_{SPSCK} | SPSCK period | $4 \times t_{periph}$ | — | ns | 2 |
| 3 | t_{Lead} | Enable lead time | 1 | — | t_{periph} | — |
| 4 | t_{Lag} | Enable lag time | 1 | — | t_{periph} | — |
| 5 | t_{WSPSCK} | Clock (SPSCK) high or low time | $t_{periph} - 30$ | — | ns | — |
| 6 | t_{SU} | Data setup time (inputs) | 2 | — | ns | — |
| 7 | t_{HI} | Data hold time (inputs) | 7 | — | ns | — |
| 8 | t_a | Slave access time | — | t_{periph} | ns | 3 |
| 9 | t_{dis} | Slave MISO disable time | — | t_{periph} | ns | 4 |
| 10 | t_v | Data valid (after SPSCK edge) | — | 122 | ns | — |
| 11 | t_{HO} | Data hold time (outputs) | 0 | — | ns | — |
| 12 | t_{RI} | Rise time input | — | $t_{periph} - 25$ | ns | — |
| | t_{FI} | Fall time input | | | | |
| 13 | t_{RO} | Rise time output | — | 36 | ns | — |
| | t_{FO} | Fall time output | | | | |

1. For SPI0, f_{periph} is the bus clock (f_{BUS}).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

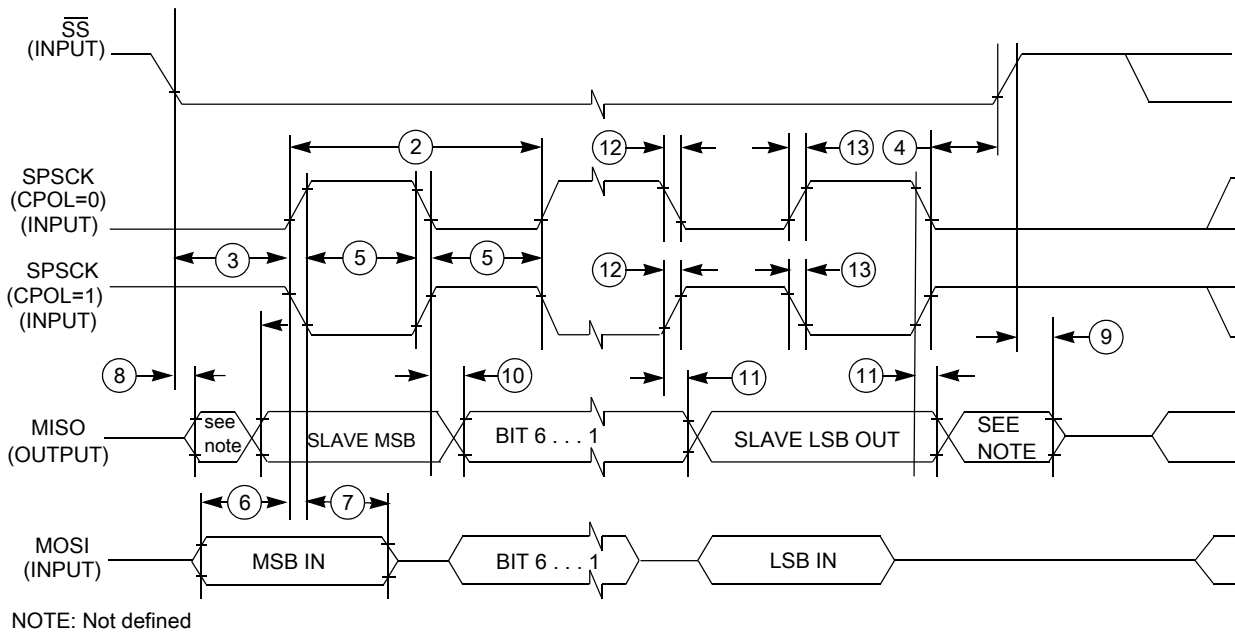


Figure 14. SPI slave mode timing (CPHA = 0)

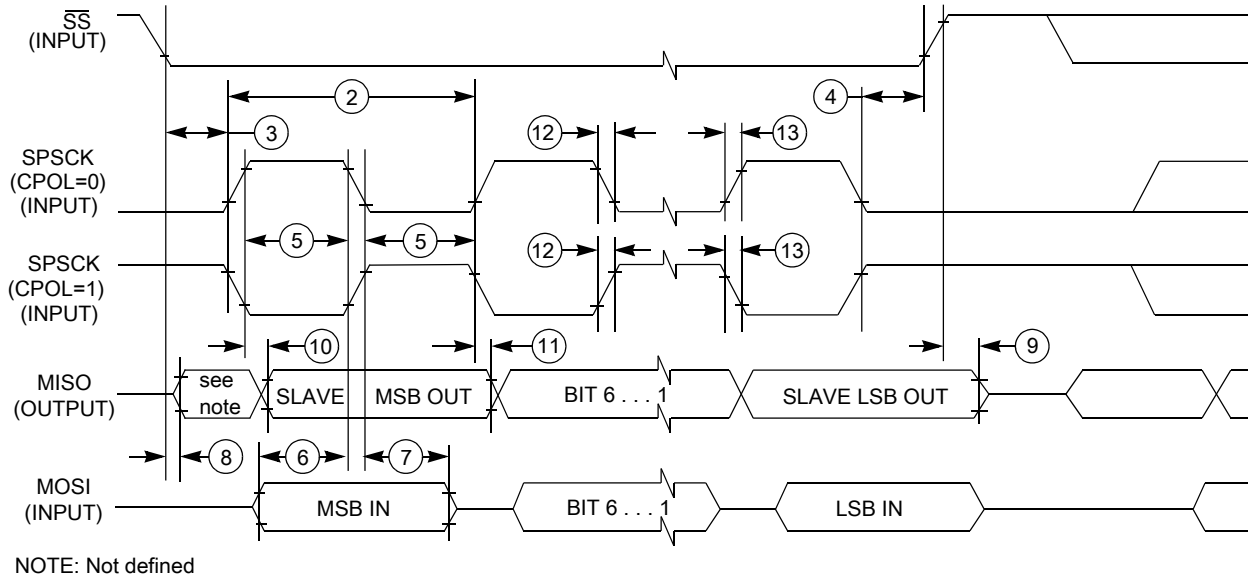


Figure 15. SPI slave mode timing (CPHA = 1)

3.8.2 Inter-Integrated Circuit Interface (I2C) timing

Table 41. I2C timing

| Characteristic | Symbol | Standard Mode | | Fast Mode | | Unit |
|----------------------------------------------------------------------------------------------|---------------|------------------|-------------------|----------------------------|------------------|---------|
| | | Minimum | Maximum | Minimum | Maximum | |
| SCL Clock Frequency | f_{SCL} | 0 | 100 ¹ | 0 | 400 ² | kHz |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated. | $t_{HD}; STA$ | 4 | — | 0.6 | — | μs |
| LOW period of the SCL clock | t_{LOW} | 4.7 | — | 1.25 | — | μs |
| HIGH period of the SCL clock | t_{HIGH} | 4 | — | 0.6 | — | μs |
| Set-up time for a repeated START condition | $t_{SU}; STA$ | 4.7 | — | 0.6 | — | μs |
| Data hold time for I ² C bus devices | $t_{HD}; DAT$ | 0 ³ | 3.45 ⁴ | 0 ⁵ | 0.9 ³ | μs |
| Data set-up time | $t_{SU}; DAT$ | 250 ⁶ | — | 100 ^{4, 7} | — | ns |
| Rise time of SDA and SCL signals | t_r | — | 1000 | $20 + 0.1C_b$ ⁸ | 300 | ns |
| Fall time of SDA and SCL signals | t_f | — | 300 | $20 + 0.1C_b$ ⁷ | 300 | ns |
| Set-up time for STOP condition | $t_{SU}; STO$ | 4 | — | 0.6 | — | μs |
| Bus free time between STOP and START condition | t_{BUF} | 4.7 | — | 1.3 | — | μs |
| Pulse width of spikes that must be suppressed by the input filter | t_{SP} | N/A | N/A | 0 | 50 | ns |

1. The PTB3 and PTB4 pins can support only the Standard mode.

2. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can be achieved only when using the normal drive pins and $V_{DD} \geq 2.7 V$.

Peripheral operating requirements and behaviors

3. The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
4. The maximum t_{HD; DAT} must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
5. Input signal Slew = 10 ns and Output Load = 50 pF
6. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
7. A Fast mode I²C bus device can be used in a Standard mode I²C bus system, but the requirement t_{SU; DAT} ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line t_{rmax} + t_{SU; DAT} = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification) before the SCL line is released.
8. C_b = total capacitance of the one bus line in pF.

To achieve 1MHz I²C clock rates, consider the following recommendations:

- To counter the effects of clock stretching, the I²C baud Rate select bits can be configured for faster than desired baud rate.
- Use high drive pad and DSE bit should be set in PORTx_PCRn register.
- Minimize loading on the I²C SDA and SCL pins to ensure fastest rise times for the SCL line to avoid clock stretching.
- Use smaller pull up resistors on SDA and SCL to reduce the RC time constant.

Table 42. I²C 1Mbit/s timing

| Characteristic | Symbol | Minimum | Maximum | Unit |
|----------------------------------------------------------------------------------------------|----------------------|-------------------------------------|----------------|------|
| SCL Clock Frequency | f _{SCL} | 0 | 1 ¹ | MHz |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated. | t _{HD; STA} | 0.26 | — | μs |
| LOW period of the SCL clock | t _{LOW} | 0.5 | — | μs |
| HIGH period of the SCL clock | t _{HIGH} | 0.26 | — | μs |
| Set-up time for a repeated START condition | t _{SU; STA} | 0.26 | — | μs |
| Data hold time for I ² C bus devices | t _{HD; DAT} | 0 | — | μs |
| Data set-up time | t _{SU; DAT} | 50 | — | ns |
| Rise time of SDA and SCL signals | t _r | 20 + 0.1C _b | 120 | ns |
| Fall time of SDA and SCL signals | t _f | 20 + 0.1C _b ² | 120 | ns |
| Set-up time for STOP condition | t _{SU; STO} | 0.26 | — | μs |
| Bus free time between STOP and START condition | t _{BUF} | 0.5 | — | μs |
| Pulse width of spikes that must be suppressed by the input filter | t _{SP} | 0 | 50 | ns |

1. The maximum SCL clock frequency of 1 Mbit/s can support 200 pF bus loading when using the normal drive pins and VDD ≥ 2.7 V.
2. C_b = total capacitance of the one bus line in pF.

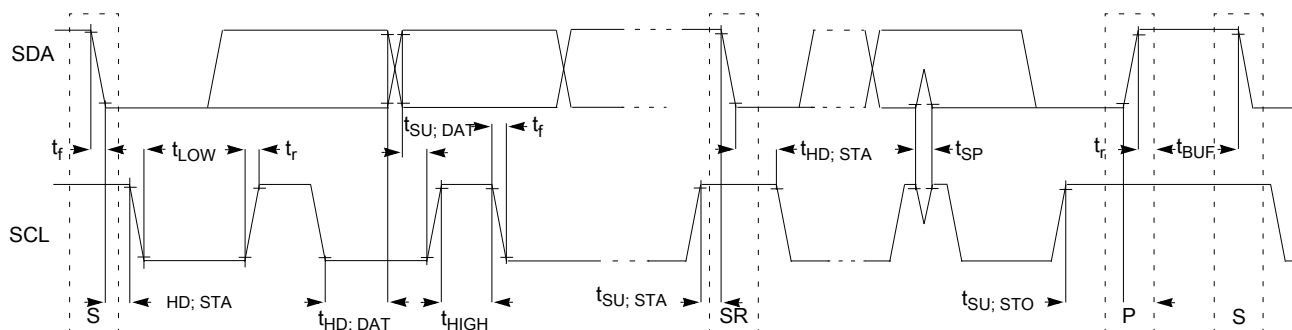


Figure 16. Timing definition for devices on the I²C bus

3.8.3 UART

See [General switching specifications](#).

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number:

| If you want the drawing for this package | Then use this document number |
|------------------------------------------|-------------------------------|
| 16-pin QFN | 98ASA00525D |
| 24-pin QFN | 98ASA00602D |
| 20-pin WLCSP | 98ASA00676D |
| 20-pin WLCSP (ultra thin) | 98ASA00964D |

5 Pinout

5.1 KL03 signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

PTB3 and PTB4 are true open drain pins. The external pullup resistor must be added to make them output correct values in using I2C, GPIO, and LPUART0.

| 24 QFN | 20 WLC SP | 16 QFN | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 |
|--------|-----------|--------|--------------------------------|-----------------------|-----------------------|--------------------------------|------------|------------|------------|--------|
| 1 | — | — | PTB6/ IRQ_2/ LPTMR0_ALT3 | DISABLED | | PTB6/ IRQ_2/ LPTMR0_ALT3 | TPM1_CH1 | TPM_CLKIN1 | | |
| 2 | — | — | PTB7/ IRQ_3 | DISABLED | | PTB7/ IRQ_3 | TPM1_CH0 | | | |
| 3 | B5 | 1 | VDD | VDD | VDD | | | | | |
| 4 | C5 | 2 | VSS | VSS | VSS | | | | | |
| 5 | C4 | 3 | PTA3 | EXTAL0 | EXTAL0 | PTA3 | I2C0_SCL | I2C0_SDA | LPUART0_TX | |
| 6 | C3 | 4 | PTA4 | XTAL0 | XTAL0 | PTA4 | I2C0_SDA | I2C0_SCL | LPUART0_RX | CLKOUT |
| 7 | D3 | 5 | PTA5/ RTC_CLK_IN | DISABLED | | PTA5/ RTC_CLK_IN | TPM0_CH1 | SPI0_SS_b | | |
| 8 | D5 | 6 | PTA6 | DISABLED | | PTA6 | TPM0_CH0 | SPI0_MISO | | |
| 9 | — | — | PTB10 | DISABLED | | PTB10 | TPM0_CH1 | SPI0_SS_b | | |
| 10 | — | — | PTB11 | DISABLED | | PTB11 | TPM0_CH0 | SPI0_MISO | | |
| 11 | D4 | 7 | PTA7/ IRQ_4 | DISABLED | | PTA7/ IRQ_4 | SPI0_MISO | SPI0_MOSI | | |
| 12 | C1 | 8 | PTB0/ IRQ_5/ LLWU_P4 | ADC0_SE9 | ADC0_SE9 | PTB0/ IRQ_5/ LLWU_P4 | EXTRG_IN | SPI0_SCK | I2C0_SCL | |
| 13 | D1 | 9 | PTB1/ IRQ_6 | ADC0_SE8/ CMP0_IN3 | ADC0_SE8/ CMP0_IN3 | PTB1/ IRQ_6 | LPUART0_TX | LPUART0_RX | I2C0_SDA | |
| 14 | B1 | 10 | PTB2/ IRQ_7 | VREF_OUT/ CMP0_IN5 | VREF_OUT/ CMP0_IN5 | PTB2/ IRQ_7 | LPUART0_RX | LPUART0_TX | | |
| 15 | D2 | — | PTA8 | ADC0_SE3 | ADC0_SE3 | PTA8 | I2C0_SCL | SPI0_MOSI | | |
| 16 | C2 | — | PTA9 | ADC0_SE2 | ADC0_SE2 | PTA9 | I2C0_SDA | SPI0_SCK | | |

| 24 QFN | 20 WLC SP | 16 QFN | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 |
|--------|-----------|--------|----------------------------------|-----------------------|------------------------|----------------------------------|------------|------------|------|--------|
| 17 | A1 | 11 | PTB3/ IRQ_10 | DISABLED | | PTB3/ IRQ_10 | I2C0_SCL | LPUART0_TX | | |
| 18 | B2 | 12 | PTB4/ IRQ_11 | DISABLED | | PTB4/ IRQ_11 | I2C0_SDA | LPUART0_RX | | |
| 19 | A2 | 13 | PTB5/ IRQ_12 | NMI_b | ADC0_SE1/ CMP0_IN1 | PTB5/ IRQ_12 | TPM1_CH1 | NMI_b | | |
| 20 | B3 | — | PTA12/ IRQ_13/ LPTMR0_ALT2 | ADC0_SE0/ CMP0_IN0 | ADC0_SE0/ CMP0_IN0 | PTA12/ IRQ_13/ LPTMR0_ALT2 | TPM1_CH0 | TPM_CLKIN0 | | CLKOUT |
| 21 | A3 | — | PTB13/ CLKOUT32K | DISABLED | | PTB13/ CLKOUT32K | TPM1_CH1 | RTC_CLKOUT | | |
| 22 | A4 | 14 | PTA0/ IRQ_0/ LLWU_P7 | SWD_CLK | ADC0_SE15/ CMP0_IN2 | PTA0/ IRQ_0/ LLWU_P7 | TPM1_CH0 | SWD_CLK | | |
| 23 | B4 | 15 | PTA1/ IRQ_1/ LPTMR0_ALT1 | RESET_b | | PTA1/ IRQ_1/ LPTMR0_ALT1 | TPM_CLKIN0 | RESET_b | | |
| 24 | A5 | 16 | PTA2 | SWD_DIO | | PTA2 | CMP0_OUT | SWD_DIO | | |

5.2 KL03 pinouts

The following figures show the pinout diagrams for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see [KL03 signal multiplexing and pin assignments](#).

Pinout

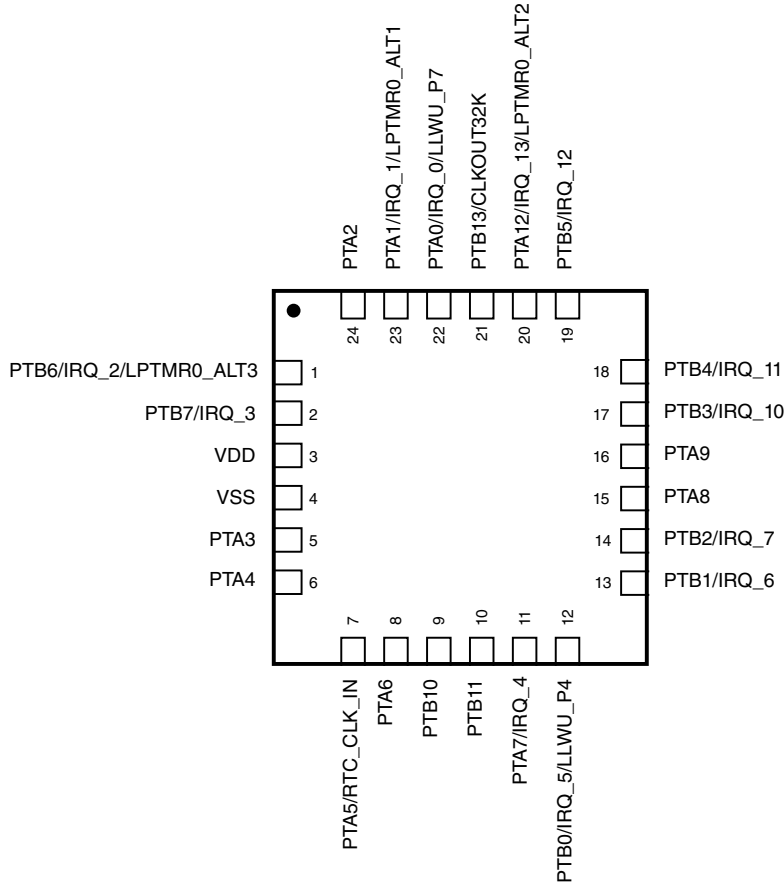


Figure 17. KL03 24-pin QFN pinout diagram

| | 1 | 2 | 3 | 4 | 5 |
|---|------|------|-------|------|------|
| A | PTB3 | PTB5 | PTB13 | PTA0 | PTA2 |
| B | PTB2 | PTB4 | PTA12 | PTA1 | VDD |
| C | PTB0 | PTA9 | PTA4 | PTA3 | VSS |
| D | PTB1 | PTA8 | PTA5 | PTA7 | PTA6 |

Figure 18. KL03 20-pin WLCSP pinout diagram

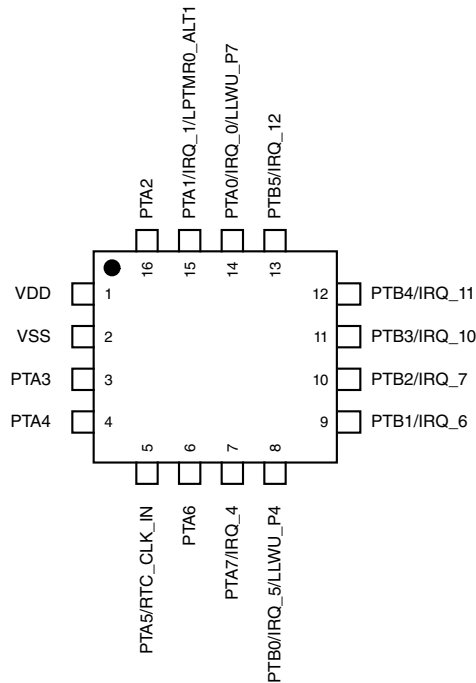


Figure 19. KL03 16-pin QFN pinout diagram

6 Ordering parts

6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to nxp.com and perform a part number search.

7 Part identification

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

Q KL## A FFF R T PP CC N

7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Table 43. Part number fields description

| Field | Description | Values |
|-------|-----------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Q | Qualification status | <ul style="list-style-type: none"> M = Fully qualified, general market flow (full reels for WLCSP) P = Prequalification K = Fully qualified, general market flow, 100 pieces reels (WLCSP only) |
| KL## | Kinetis family | <ul style="list-style-type: none"> KL03 |
| A | Key attribute | <ul style="list-style-type: none"> Z = Cortex-M0+ |
| FFF | Program flash memory size | <ul style="list-style-type: none"> 8 = 8 KB 16 = 16 KB 32 = 32 KB |
| R | Silicon revision | <ul style="list-style-type: none"> (Blank) = Main A = Revision after main |
| T | Temperature range (°C) | <ul style="list-style-type: none"> V = -40 to 105 C = -40 to 85 |
| PP | Package identifier | <ul style="list-style-type: none"> FG = 16 QFN (3 mm x 3 mm) AF = 20 WLCSP (2 mm x 1.61 mm x 0.56 mm) BF = 20 WLCSP (2 mm x 1.61 mm x 0.32 mm) FK = 24 QFN (4 mm x 4 mm) |
| CC | Maximum CPU frequency (MHz) | <ul style="list-style-type: none"> 4 = 48 MHz |
| N | Packaging type | <ul style="list-style-type: none"> R = Tape and reel (Blank) = Trays |

7.4 Example

This is an example part number:

MKL03Z32VFK4

8 Terminology and guidelines

8.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

8.1.1 Example

This is an example of an operating requirement:

| Symbol | Description | Min. | Max. | Unit |
|-----------------|---------------------------|------|------|------|
| V _{DD} | 1.0 V core supply voltage | 0.9 | 1.1 | V |

8.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

8.2.1 Example

This is an example of an operating behavior:

| Symbol | Description | Min. | Max. | Unit |
|-----------------|------------------------------------------|------|------|------|
| I _{WP} | Digital I/O weak pullup/pulldown current | 10 | 130 | μA |

8.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

8.3.1 Example

This is an example of an attribute:

| Symbol | Description | Min. | Max. | Unit |
|--------|------------------------------------|------|------|------|
| CIN_D | Input capacitance: digital pins | — | 7 | pF |

8.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

8.4.1 Example

This is an example of an operating rating:

| Symbol | Description | Min. | Max. | Unit |
|-----------------|------------------------------|------|------|------|
| V _{DD} | 1.0 V core supply voltage | −0.3 | 1.2 | V |

Terminology and guidelines

- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

8.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

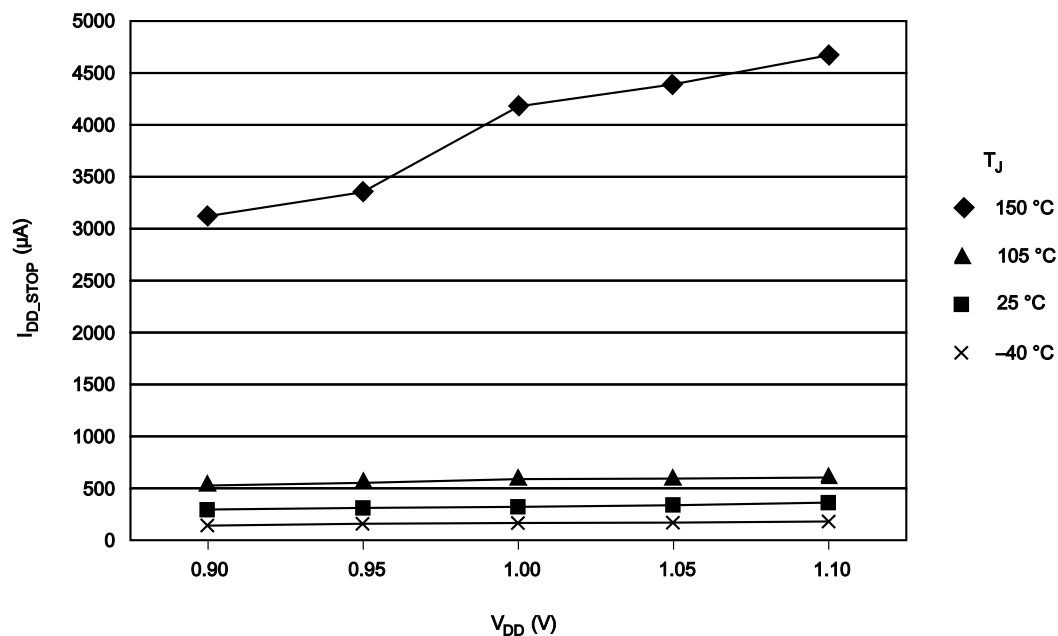
8.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

| Symbol | Description | Min. | Typ. | Max. | Unit |
|----------|------------------------------------------|------|------|------|---------|
| I_{WP} | Digital I/O weak pullup/pulldown current | 10 | 70 | 130 | μA |

8.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



8.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Table 44. Typical value conditions

| Symbol | Description | Value | Unit |
|-----------------|----------------------|-------|------|
| T _A | Ambient temperature | 25 | °C |
| V _{DD} | 3.3 V supply voltage | 3.3 | V |

9 Revision history

The following table provides a revision history for this document.

Table 45. Revision history

| Rev. No. | Date | Substantial Changes |
|----------|---------|-----------------------------------------------------------------------------------------------------------------|
| 3.1 | 07/2014 | Initial public release. |
| 4 | 08/2014 | Changed pinout signal names ADC0_SE5, ADC0_SE6, and ADC0_SE12 to ADC0_SE8, ADC0_SE9 and ADC0_SE15 respectively. |

Table continues on the next page...

Table 45. Revision history (continued)

| Rev. No. | Date | Substantial Changes |
|----------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5 | 07/2017 | <ul style="list-style-type: none"> • Added new part of MKL03Z32CBF4R and its package information. • Updated the Resource and its footnote to the Chip Errata in the front page • Updated the descriptions to the VLPW to be very low power wait mode in the Power consumption operating behaviors • Added a note to the T_A in the Thermal operating requirements • Updated the foot note to the Typ. of the Table 31 to be VREFO = 1.2 V • Added I2C 1 Mbit/s timing specifications in Inter-Integrated Circuit Interface (I2C) timing • Updated Determining valid orderable parts • Updated the 20-pin WLCSP package (AF) size in Fields |
| 5.1 | 08/2017 | Updated the Max. of MSL for WLCSP packages to 1 in the Moisture handling ratings |



How to Reach Us:

Home Page:

nxp.com

Web Support:

nxp.com/support

Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: nxp.com/SalesTermsandConditions.

NXP, the NXP logo, NXP SECURE CONNECTIONS FOR A SMARTER WORLD, Freescale, the Freescale logo, and Kinetis are trademarks of NXP B.V. All other product or service names are the property of their respective owners. ARM, the ARM powered logo, and Cortex are registered trademarks of ARM Limited (or its subsidiaries) in the EU and/or elsewhere. All rights reserved.

©2014-2017 NXP B.V.

Document Number KL03P24M48SF0
Revision 5.1 08/2017



Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View MKL03Z32CAF4R on WIN SOURCE](#)

 [NXP / Nexperia Information](#)

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management