



**THE DATASHEET OF
MKL27Z128VLH4**



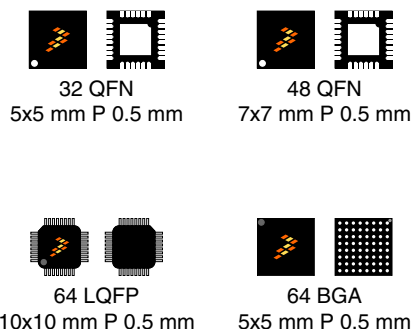
Kinetis KL27 Microcontroller

48 MHz ARM® Cortex®-M0+ and 128/256 KB Flash

MKL27Z128Vxx4
MKL27Z256Vxx4

The KL27 series is optimized for cost-sensitive and battery-powered applications requiring low-power USB connectivity. The product offers:

- USB FS 2.0 device without requiring an external crystal
- Embedded ROM with boot loader for flexible program upgrade
- High accuracy internal voltage and clock reference
- FlexIO to support any standard and customized serial peripheral emulation
- Down to 54uA/MHz in very low power run mode and 1.96uA in deep sleep mode (RAM + RTC retained)



Core Processor

- ARM® Cortex®-M0+ core up to 48 MHz

Memories

- 128/256 KB program flash memory
- 32 KB SRAM
- 16 KB ROM with build-in bootloader
- 32-byte backup register

System

- 4-channel asynchronous DMA controller
- Watchdog
- Low-leakage wakeup unit
- Two-pin Serial Wire Debug (SWD) programming and debug interface
- Micro Trace Buffer
- Bit manipulation engine
- Interrupt controller

Clocks

- 48MHz high accuracy (up to 0.5%) internal reference clock
- 8MHz/2MHz high accuracy (up to 3%) internal reference clock
- 1KHz reference clock active under all low-power modes (except VLLS0)
- 32–40KHz and 3–32MHz crystal oscillator

Peripherals

- USB full-speed 2.0 device controller supporting crystal-less operation
- One UART module supporting ISO7816, operating up to 1.5 Mbit/s
- Two low-power UART modules supporting asynchronous operation in low-power modes
- Two I2C modules and I2C0 supporting up to 1 Mbit/s
- Two 16-bit SPI modules supporting up to 24 Mbit/s
- One FlexIO module supporting emulation of additional UART, IrDA, SPI, I2C, I2S, PWM and other serial modules, etc.
- One serial audio interface I2S
- One 16-bit 818 ksp/s ADC module with high accuracy internal voltage reference (Vref) and up to 16 channels
- High-speed analog comparator containing a 6-bit DAC for programmable reference input
- One 12-bit DAC
- 1.2 V internal voltage reference

Timers

- One 6-channel Timer/PWM module
- Two 2-channel Timer/PWM modules
- One low-power timer
- Periodic interrupt timer
- Real time clock

Operating Characteristics

- Voltage range: 1.71 to 3.6 V
- Flash write voltage range: 1.71 to 3.6 V
- Temperature range: -40 to 105 °C

Packages

- 64 LQFP 10mm x 10mm, 0.5mm pitch, 1.6mm thickness
- 64 MAPBGA 5mm x 5mm, 0.5mm pitch, 1.23mm thickness
- 48 QFN 7mm x 7mm, 0.5mm pitch, 0.65mm thickness
- 32 QFN 5mm x 5mm, 0.5mm pitch, 0.65mm thickness

Security and Integrity

- 80-bit unique identification number per chip
- Advanced flash security

I/O

- Up to 50 general-purpose input/output pins (GPIO) and 6 high-drive pad

Low Power

- Down to 54uA/MHz in very low power run mode
- Down to 1.96uA in VLLS3 mode (RAM + RTC retained)
- Six flexible static modes

Ordering Information

| Product | | Memory | | Package | | IO and ADC channel | | |
|---------------|-----------------------|------------|-----------|-----------|---------|--------------------|-----------------------------|----------------------|
| Part number | Marking (Line1/Line2) | Flash (KB) | SRAM (KB) | Pin count | Package | GPIOs | GPIOs (INT/HD) ¹ | ADC channels (SE/DP) |
| MKL27Z128VFM4 | M27P7V | 128 | 32 | 32 | QFN | 23 | 19/6 | 7/0 |
| MKL27Z256VFM4 | M27P8V | 256 | 32 | 32 | QFN | 23 | 19/6 | 7/0 |
| MKL27Z128VFT4 | M27P7V | 128 | 32 | 48 | QFN | 36 | 24/6 | 14/1 |
| MKL27Z256VFT4 | M27P8V | 256 | 32 | 48 | QFN | 36 | 24/6 | 14/1 |
| MKL27Z128VLH4 | MKL27Z128V//LH4 | 128 | 32 | 64 | LQFP | 50 | 31/6 | 16/2 |
| MKL27Z256VLH4 | MKL27Z256V//LH4 | 256 | 32 | 64 | LQFP | 50 | 31/6 | 16/2 |
| MKL27Z128VMP4 | M27P7V | 128 | 32 | 64 | MAPBGA | 50 | 31/6 | 16/2 |
| MKL27Z256VMP4 | M27P8V | 256 | 32 | 64 | MAPBGA | 50 | 31/6 | 16/2 |

1. INT: interrupt pin numbers; HD: high drive pin numbers

Related Resources

| Type | Description | Resource |
|------------------|--|---|
| Selector Guide | The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector. | Solution Advisor |
| Product Brief | The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability. | KL2XPB ¹ |
| Reference Manual | The Reference Manual contains a comprehensive description of the structure and function (operation) of a device. | KL27P64M48SF6RM ¹ |
| Data Sheet | The Data Sheet includes electrical characteristics and signal connections. | This document. |
| Chip Errata | The chip mask set Errata provides additional or corrective information for a particular device mask set. | KINETIS_L_1N71K ¹ |
| Package drawing | Package dimensions are provided in package drawings. | 64-LQFP: 98ASS23234W ¹ 64 MAPBGA: 98ASA00420D ¹ 32 QFN: 98ASA00615D ¹ 48 QFN: 98ASA00616D ¹ |

1. To find the associated resource, go to <http://www.freescale.com> and perform a search using this term.





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1 Ratings

1.1 Thermal handling ratings

Table 1. Thermal handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------------|-------------------------------|------|------|------|-------|
| T _{STG} | Storage temperature | -55 | 150 | °C | 1 |
| T _{SDR} | Solder temperature, lead-free | — | 260 | °C | 2 |

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Table 2. Moisture handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|----------------------------|------|------|------|-------|
| MSL | Moisture sensitivity level | — | 3 | — | 1 |

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Table 3. ESD handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------------|---|-------|-------|------|-------|
| V _{HBM} | Electrostatic discharge voltage, human body model | -2000 | +2000 | V | 1 |
| V _{CDM} | Electrostatic discharge voltage, charged-device model | -500 | +500 | V | 2 |
| I _{LAT} | Latch-up current at ambient temperature of 105 °C | -100 | +100 | mA | 3 |

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

1.4 Voltage and current operating ratings

Table 4. Voltage and current operating ratings

| Symbol | Description | Min. | Max. | Unit |
|---------------|---|----------------|----------------|------|
| V_{DD} | Digital supply voltage | -0.3 | 3.8 | V |
| I_{DD} | Digital supply current | — | 120 | mA |
| V_{IO} | IO pin input voltage | -0.3 | $V_{DD} + 0.3$ | V |
| I_D | Instantaneous maximum current single pin limit (applies to all port pins) | -25 | 25 | mA |
| V_{DDA} | Analog supply voltage | $V_{DD} - 0.3$ | $V_{DD} + 0.3$ | V |
| V_{USB_DP} | USB_DP input voltage | -0.3 | 3.63 | V |
| V_{USB_DM} | USB_DM input voltage | -0.3 | 3.63 | V |
| V_{REGIN} | USB regulator input | -0.3 | 6.0 | V |

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

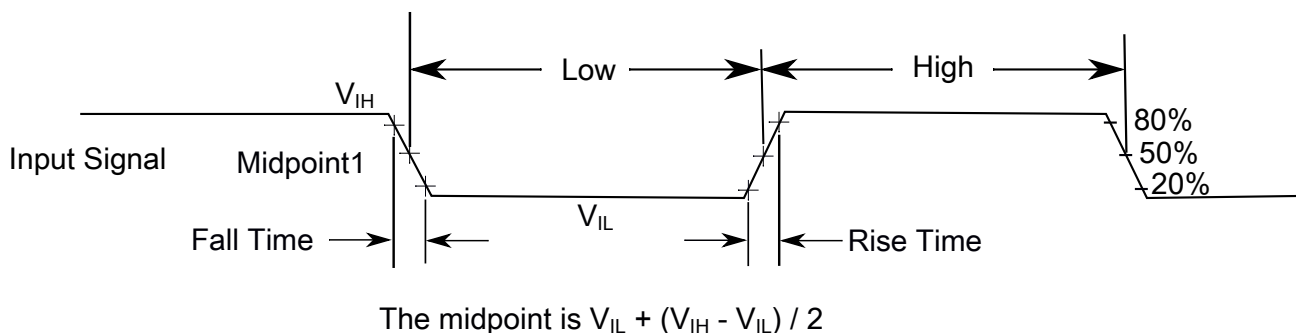


Figure 1. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- $C_L=30$ pF loads
- Slew rate disabled
- Normal drive strength

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 5. Voltage and current operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------------------|--|----------------------|----------------------|------|-------|
| V_{DD} | Supply voltage | 1.71 | 3.6 | V | |
| V_{DDA} | Analog supply voltage | 1.71 | 3.6 | V | |
| $V_{DD} - V_{DDA}$ | V_{DD} -to- V_{DDA} differential voltage | -0.1 | 0.1 | V | |
| $V_{SS} - V_{SSA}$ | V_{SS} -to- V_{SSA} differential voltage | -0.1 | 0.1 | V | |
| V_{IH} | Input high voltage <ul style="list-style-type: none"> • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ • $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ | $0.7 \times V_{DD}$ | — | V | |
| | | $0.75 \times V_{DD}$ | — | V | |
| V_{IL} | Input low voltage <ul style="list-style-type: none"> • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ • $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ | — | $0.35 \times V_{DD}$ | V | |
| | | — | $0.3 \times V_{DD}$ | V | |
| V_{HYS} | Input hysteresis | $0.06 \times V_{DD}$ | — | V | |
| I_{ICIO} | IO pin negative DC injection current — single pin <ul style="list-style-type: none"> • $V_{IN} < V_{SS}-0.3\text{V}$ | -3 | — | mA | 1 |
| I_{ICcont} | Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins <ul style="list-style-type: none"> • Negative current injection | -25 | — | mA | |
| V_{ODPU} | Open drain pullup voltage level | V_{DD} | V_{DD} | V | 2 |
| V_{RAM} | V_{DD} voltage required to retain RAM | 1.2 | — | V | |

1. All I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to V_{DD} . If V_{IN} greater than V_{IO_MIN} ($= V_{SS}-0.3\text{ V}$) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R = (V_{IO_MIN} - V_{IN})/|I_{ICIO}|$.
2. Open drain outputs must be pulled to V_{DD} .

2.2.2 LVD and POR operating requirements

Table 6. V_{DD} supply LVD and POR operating requirements

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-----------|-------------------------------------|------|------|------|------|-------|
| V_{POR} | Falling V_{DD} POR detect voltage | 0.8 | 1.1 | 1.5 | V | — |

Table continues on the next page...

Table 6. V_{DD} supply LVD and POR operating requirements (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------------------|--|------|------|------|------|-------|
| V _{LVDH} | Falling low-voltage detect threshold — high range (LVDV = 01) | 2.48 | 2.56 | 2.64 | V | — |
| V _{LVW1H} | Low-voltage warning thresholds — high range <ul style="list-style-type: none"> • Level 1 falling (LVWV = 00) • Level 2 falling (LVWV = 01) • Level 3 falling (LVWV = 10) • Level 4 falling (LVWV = 11) | 2.62 | 2.70 | 2.78 | V | 1 |
| V _{LVW2H} | | 2.72 | 2.80 | 2.88 | V | |
| V _{LVW3H} | | 2.82 | 2.90 | 2.98 | V | |
| V _{LVW4H} | | 2.92 | 3.00 | 3.08 | V | |
| V _{HYSH} | Low-voltage inhibit reset/recover hysteresis — high range | — | ±60 | — | mV | — |
| V _{LVDL} | Falling low-voltage detect threshold — low range (LVDV=00) | 1.54 | 1.60 | 1.66 | V | — |
| V _{LVW1L} | Low-voltage warning thresholds — low range <ul style="list-style-type: none"> • Level 1 falling (LVWV = 00) • Level 2 falling (LVWV = 01) • Level 3 falling (LVWV = 10) • Level 4 falling (LVWV = 11) | 1.74 | 1.80 | 1.86 | V | 1 |
| V _{LVW2L} | | 1.84 | 1.90 | 1.96 | V | |
| V _{LVW3L} | | 1.94 | 2.00 | 2.06 | V | |
| V _{LVW4L} | | 2.04 | 2.10 | 2.16 | V | |
| V _{HYSL} | Low-voltage inhibit reset/recover hysteresis — low range | — | ±40 | — | mV | — |
| V _{BG} | Bandgap voltage reference | 0.97 | 1.00 | 1.03 | V | — |
| t _{LPO} | Internal low power oscillator period — factory trimmed | 900 | 1000 | 1100 | µs | — |

1. Rising thresholds are falling threshold + hysteresis voltage

2.2.3 Voltage and current operating behaviors

Table 7. Voltage and current operating behaviors

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------------|--|--|--------|--------|-------|
| V _{OH} | Output high voltage — normal drive pad <ul style="list-style-type: none"> • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -5 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -1.5 mA | V _{DD} - 0.5 V _{DD} - 0.5 | — — | V V | 1 |
| V _{OH} | Output high voltage — high drive pad <ul style="list-style-type: none"> • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -18 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -6 mA | V _{DD} - 0.5 V _{DD} - 0.5 | — — | V V | 1 |
| I _{OHT} | Output high current total for all ports | — | 100 | mA | |
| V _{OL} | Output low voltage — normal drive pad | — | 0.5 | V | 1 |

Table continues on the next page...

Table 7. Voltage and current operating behaviors (continued)

| Symbol | Description | Min. | Max. | Unit | Notes |
|-----------|--|------|-------|---------------|-------|
| | <ul style="list-style-type: none"> • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 5\text{ mA}$ • $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 1.5\text{ mA}$ | — | 0.5 | V | |
| V_{OL} | Output low voltage — high drive pad <ul style="list-style-type: none"> • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 18\text{ mA}$ • $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 6\text{ mA}$ | — | 0.5 | V | 1 |
| | | — | 0.5 | V | |
| I_{OLT} | Output low current total for all ports | — | 100 | mA | |
| I_{IN} | Input leakage current (per pin) for full temperature range | — | 1 | μA | 2 |
| I_{IN} | Input leakage current (per pin) at 25 °C | — | 0.025 | μA | 2 |
| I_{IN} | Input leakage current (total all pins) for full temperature range | — | 64 | μA | 2 |
| I_{OZ} | Hi-Z (off-state) leakage current (per pin) | — | 1 | μA | |
| R_{PU} | Internal pullup resistors | 20 | 50 | k Ω | 3 |

1. PTB0, PTB1, PTC3, PTC4, PTD6, and PTD7 I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. Measured at $V_{DD} = 3.6\text{ V}$
3. Measured at V_{DD} supply voltage = V_{DD} min and $V_{input} = V_{SS}$

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and $VLLSx \rightarrow RUN$ recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- HIRC clock mode

Table 8. Power mode transition operating behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-----------|---|------|------|------|---------------|-------|
| t_{POR} | After a POR event, amount of time from the point V_{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip. | — | — | 300 | μs | 1 |
| | <ul style="list-style-type: none"> • $VLLS0 \rightarrow RUN$ | — | 152 | 166 | μs | |
| | <ul style="list-style-type: none"> • $VLLS1 \rightarrow RUN$ | — | 152 | 166 | μs | |
| | <ul style="list-style-type: none"> • $VLLS3 \rightarrow RUN$ | — | 93 | 104 | μs | |

Table continues on the next page...

Table 8. Power mode transition operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------|--------------|------|------|------|------|-------|
| | • LLS → RUN | — | 7.5 | 8 | μs | |
| | • VLPS → RUN | — | 7.5 | 8 | μs | |
| | • STOP → RUN | — | 7.5 | 8 | μs | |

1. Normal boot (FTFA_FOFT[LPBOOT]=11)

2.2.5 Power consumption operating behaviors

The maximum values stated in the following table represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

NOTE

The while (1) test is executed with flash cache enabled.

Table 9. Power consumption operating behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-----------------------|--|--------|--------------|--------------|------|-------|
| I _{DDA} | Analog supply current | — | — | See note | mA | 1 |
| I _{DD_RUNCO} | Running CoreMark in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> • at 25 °C • at 105 °C | — — | 5.76 6.04 | 6.40 6.68 | mA | 2 |
| I _{DD_RUNCO} | Running While(1) loop in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> • at 25 °C • at 105 °C | — — | 3.21 3.49 | 3.85 4.13 | mA | |
| I _{DD_RUN} | Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 48 MHz core/24 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> • at 25 °C • at 105 °C | — — | 6.45 6.75 | 7.09 7.39 | mA | 2 |
| I _{DD_RUN} | Run mode current—48M HIRC mode, running CoreMark in flash all peripheral clock disable, 24 MHz core/12 MHz flash, V _{DD} = 3.0 V | — — | 3.95 4.23 | 4.59 4.87 | mA | 2 |

Table continues on the next page...

Table 9. Power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---------------------|--|------|------|------|------|-------|
| | <ul style="list-style-type: none"> at 25 °C at 105 °C | | | | | |
| I _{DD_RUN} | Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 12 MHz core/6 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C at 105 °C | — | 2.68 | 3.32 | mA | 2 |
| I _{DD_RUN} | Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock enable 48 MHz core/24 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C at 105 °C | — | 8.08 | 8.72 | mA | 2 |
| I _{DD_RUN} | Run mode current—48M HIRC mode, running While(1) loop in flash all peripheral clock disable, 48 MHz core/24 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C at 105 °C | — | 3.90 | 4.54 | mA | |
| I _{DD_RUN} | Run mode current—48M HIRC mode, running While(1) loop in Flash all peripheral clock disable, 24 MHz core/12 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C at 105 °C | — | 2.66 | 3.30 | mA | |
| I _{DD_RUN} | Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock disable, 12 MHz core/6 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C at 105 °C | — | 2.03 | 2.67 | mA | |
| I _{DD_RUN} | Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock enable, 48 MHz core/24 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C at 105 °C | — | 5.52 | 6.16 | mA | |
| I _{DD_RUN} | Run mode current—48M HIRC mode, running While(1) loop in SRAM all peripheral clock disable, 48 MHz core/24 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C at 105 °C | — | 5.29 | 5.93 | mA | |
| I _{DD_RUN} | Run mode current—48M HIRC mode, running While(1) loop in SRAM all peripheral clock enable, 48 MHz core/24 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C at 105 °C | — | 6.91 | 7.55 | mA | |

Table continues on the next page...

Table 9. Power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|------------------------|---|------|------|------|------|-------|
| | <ul style="list-style-type: none"> at 25 °C at 105 °C | | | | | |
| I _{DD_VLPRCO} | Very Low Power Run Core Mark in Flash in Compute Operation mode: Core@4MHz, Flash @1MHz, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C | — | 826 | 907 | μA | |
| I _{DD_VLPRCO} | Very-low-power-run While(1) loop in SRAM in compute operation mode— 8 MHz LIRC mode, 4 MHz core / 1 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C | — | 405 | 486 | μA | |
| I _{DD_VLPRCO} | Very-low-power run While(1) loop in SRAM in compute operation mode:—2 MHz LIRC mode, 2 MHz core / 0.5 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C | — | 154 | 235 | μA | |
| I _{DD_VLPR} | Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 2 MHz core / 0.5 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C | — | 108 | 189 | μA | |
| I _{DD_VLPR} | Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 125 kHz core / 31.25 kHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C | — | 39 | 120 | μA | |
| I _{DD_VLPR} | Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 4 MHz core / 1 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C | — | 249 | 330 | μA | |
| I _{DD_VLPR} | Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in flash all peripheral clock enable, 4 MHz core / 1 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C | — | 337 | 418 | μA | |
| I _{DD_VLPR} | Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in SRAM in all peripheral clock disable, 4 MHz core / 1 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C | — | 416 | 497 | μA | |
| I _{DD_VLPR} | Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in SRAM all peripheral clock enable, 4 MHz core / 1 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C | — | 494 | 575 | μA | |
| I _{DD_VLPR} | Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM in all peripheral clock disable, 2 MHz core / 0.5 MHz flash, V _{DD} = 3.0 V <ul style="list-style-type: none"> at 25 °C | — | 166 | 247 | μA | |
| I _{DD_VLPR} | Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM all peripheral clock | | | | | |

Table continues on the next page...

Table 9. Power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|------------------|---|------|--------|--------|---------------|-------|
| | disable, 125 kHz core / 31.25 kHz flash, $V_{DD} = 3.0\text{ V}$ <ul style="list-style-type: none"> at 25 °C | — | 50 | 131 | μA | |
| I_{DD_VLPR} | Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM all peripheral clock enable, 2 MHz core / 0.5 MHz flash, $V_{DD} = 3.0\text{ V}$ <ul style="list-style-type: none"> at 25 °C | — | 208 | 289 | μA | |
| I_{DD_WAIT} | Wait mode current—core disabled, 48 MHz system/24 MHz bus, flash disabled (flash doze enabled), all peripheral clocks disabled, MCG_Lite under HIRC mode, $V_{DD} = 3.0\text{ V}$ | — | 1.81 | 1.89 | mA | |
| I_{DD_WAIT} | Wait mode current—core disabled, 24 MHz system/12 MHz bus, flash disabled (flash doze enabled), all peripheral clocks disabled, MCG_Lite under HIRC mode, $V_{DD} = 3.0\text{ V}$ | — | 1.22 | 1.39 | mA | |
| I_{DD_VLPW} | Very-low-power wait mode current, core disabled, 4 MHz system/ 1 MHz bus and flash, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$ | — | 172 | 182 | μA | |
| I_{DD_VLPW} | Very-low-power wait mode current, core disabled, 2 MHz system/ 0.5 MHz bus and flash, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$ | — | 69 | 76 | μA | |
| I_{DD_VLPW} | Very-low-power wait mode current, core disabled, 125 kHz system/ 31.25 kHz bus and flash, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$ | — | 36 | 40 | μA | |
| I_{DD_PSTOP2} | Partial Stop 2, core and system clock disabled, 12 MHz bus and flash, $V_{DD} = 3.0\text{ V}$ | — | 1.81 | 2.06 | mA | |
| I_{DD_PSTOP2} | Partial Stop 2, core and system clock disabled, flash doze enabled, 12 MHz bus, $V_{DD} = 3.0\text{ V}$ | — | 1.00 | 1.25 | mA | |
| I_{DD_STOP} | Stop mode current at 3.0 V <ul style="list-style-type: none"> at 25 °C and below at 50 °C at 85 °C at 105 °C | — | 161.93 | 171.82 | μA | |
| | | — | 181.45 | 191.96 | | |
| | | — | 236.29 | 271.17 | | |
| | | — | 390.33 | 465.58 | | |
| I_{DD_VLPS} | Very-low-power stop mode current at 3.0 V <ul style="list-style-type: none"> at 25 °C and below at 50 °C at 85 °C at 105 °C | — | 3.31 | 5.14 | μA | |
| | | — | 10.43 | 17.68 | | |
| | | — | 34.14 | 61.06 | | |
| | | — | 104.38 | 164.44 | | |
| I_{DD_VLPS} | Very-low-power stop mode current at 1.8 V <ul style="list-style-type: none"> at 25 °C and below | — | 3.21 | 5.22 | | |

Table continues on the next page...

Table 9. Power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes | |
|-----------------------|--|------|--------|--------|------|-------|--|
| | <ul style="list-style-type: none"> at 50 °C at 85 °C at 105 °C | — | 10.26 | 17.62 | μA | | |
| | | — | 33.49 | 60.19 | | | |
| | | — | 102.92 | 162.20 | | | |
| I _{DD_LLS} | Low-leakage stop mode current, all peripheral disable, at 3.0 V <ul style="list-style-type: none"> at 25 °C and below at 50 °C at 70 °C at 85 °C at 105 °C | — | 2.06 | 3.33 | μA | | |
| | | — | 4.72 | 6.85 | | | |
| | | — | 8.13 | 13.30 | | | |
| | | — | 13.34 | 24.70 | | | |
| | | — | 41.08 | 52.43 | | | |
| I _{DD_LLS} | Low-leakage stop mode current with RTC current, at 3.0 V <ul style="list-style-type: none"> at 25 °C and below at 50 °C at 70 °C at 85 °C at 105 °C | — | 2.46 | 3.73 | μA | | |
| | | — | 5.12 | 7.25 | | | |
| | | — | 8.53 | 11.78 | | | |
| | | — | 13.74 | 18.91 | | | |
| | | — | 41.48 | 52.83 | | | |
| I _{DD_LLS} | Low-leakage stop mode current with RTC current, at 1.8 V <ul style="list-style-type: none"> at 25 °C and below at 50 °C at 70 °C at 85 °C at 105 °C | — | 2.35 | 2.70 | μA | 3 | |
| | | — | 4.91 | 6.75 | | | |
| | | — | 8.32 | 11.78 | | | |
| | | — | 13.44 | 18.21 | | | |
| | | — | 40.47 | 51.85 | | | |
| I _{DD_VLLS3} | Very-low-leakage stop mode 3 current, all peripheral disable, at 3.0 V <ul style="list-style-type: none"> at 25 °C and below at 50 °C at 70 °C at 85 °C at 105 °C | — | 1.45 | 1.85 | μA | | |
| | | — | 3.37 | 4.39 | | | |
| | | — | 5.76 | 8.48 | | | |
| | | — | 9.72 | 14.30 | | | |
| | | — | 30.41 | 37.50 | | | |
| I _{DD_VLLS3} | Very-low-leakage stop mode 3 current with RTC current, at 3.0 V <ul style="list-style-type: none"> at 25 °C and below at 50 °C at 70 °C at 85 °C at 105 °C | — | 2.05 | 2.45 | μA | 3 | |
| | | — | 3.97 | 4.99 | | | |
| | | — | 6.36 | 9.08 | | | |
| | | — | 10.32 | 14.73 | | | |
| | | — | 31.01 | 38.10 | | | |

Table continues on the next page...

Table 9. Power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-----------------------|---|------|------|------|------|-------|
| I _{DD_VLLS3} | Very-low-leakage stop mode 3 current with RTC current, at 1.8 V <ul style="list-style-type: none"> • at 25 °C and below • at 50 °C • at 70 °C • at 85 °C • at 105 °C | — | 1.96 | 2.36 | μA | 3 |
| I _{DD_VLLS1} | Very-low-leakage stop mode 1 current all peripheral disabled at 3.0 V <ul style="list-style-type: none"> • at 25 °C and below • at 50 °C • at 70 °C • at 85 °C • at 105 °C | — | 0.66 | 0.80 | μA | |
| I _{DD_VLLS1} | Very-low-leakage stop mode 1 current RTC enabled at 3.0 V <ul style="list-style-type: none"> • at 25 °C and below • at 50 °C • at 70 °C • at 85 °C • at 105 °C | — | 1.26 | 1.40 | μA | 3 |
| I _{DD_VLLS1} | Very-low-leakage stop mode 1 current RTC enabled at 1.8 V <ul style="list-style-type: none"> • at 25 °C and below • at 50 °C • at 70 °C • at 85 °C • at 105 °C | — | 1.16 | 1.30 | μA | 3 |
| I _{DD_VLLS0} | Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 0) at 3.0 V <ul style="list-style-type: none"> • at 25 °C and below • at 50 °C • at 70 °C • at 85 °C • at 105 °C | — | 0.35 | 0.47 | μA | |
| I _{DD_VLLS0} | Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 1) at 3 V | | | | | |

Table 9. Power consumption operating behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------|---|------|-------|-------|------|-------|
| | <ul style="list-style-type: none"> at 25 °C and below at 50 °C at 70 °C at 85 °C at 105 °C | — | 0.18 | 0.28 | μA | |
| | | — | 1.09 | 1.31 | | |
| | | — | 2.25 | 2.94 | | |
| | | — | 4.25 | 5.10 | | |
| | | — | 15.95 | 19.10 | | |

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. MCG_Lite configured for HIRC mode. CoreMark benchmark compiled using IAR 7.10 with optimization level high, optimized for balanced.
3. RTC uses external 32 kHz crystal as clock source, and the current includes ERCLK32K power consumption.

Table 10. Low power mode peripheral adders — typical value

| Symbol | Description | Temperature (°C) | | | | | | Unit |
|----------------------------|---|------------------|-----|-----|-----|-----|-----|------|
| | | -40 | 25 | 50 | 70 | 85 | 105 | |
| I _{IRC8MHz} | 8 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 8 MHz IRC enabled, MCG_SC[FCRDIV]=000b, MCG_MC[LIRC_DIV2]=000b. | 93 | 93 | 93 | 93 | 93 | 93 | μA |
| I _{IRC2MHz} | 2 MHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 2 MHz IRC enabled, MCG_SC[FCRDIV]=000b, MCG_MC[LIRC_DIV2]=000b. | 29 | 29 | 29 | 29 | 29 | 29 | μA |
| I _{EREFSTEN4MHz} | External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled. | 206 | 224 | 230 | 238 | 245 | 253 | μA |
| I _{EREFSTEN32KHz} | External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled. <ul style="list-style-type: none"> VLLS1 VLLS3 LLS VLPS STOP | 440 | 490 | 540 | 560 | 570 | 580 | nA |
| | | 440 | 490 | 540 | 560 | 570 | 580 | |
| | | 490 | 490 | 540 | 560 | 570 | 680 | |
| | | 510 | 560 | 560 | 560 | 610 | 680 | |
| | | 510 | 560 | 560 | 560 | 610 | 680 | |
| I _{LPTMR} | LPTMR peripheral adder measured by placing the device in VLLS1 mode with LPTMR enabled using LPO. | 30 | 30 | 30 | 85 | 100 | 200 | |

Table continues on the next page...

Table 10. Low power mode peripheral adders — typical value (continued)

| Symbol | Description | Temperature (°C) | | | | | | Unit |
|------------|---|------------------|-----|-----|-----|-----|-----|---------|
| | | -40 | 25 | 50 | 70 | 85 | 105 | |
| | | | | | | | | nA |
| I_{CMP} | CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption. | 22 | 22 | 22 | 22 | 22 | 22 | μA |
| I_{UART} | UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption. <ul style="list-style-type: none"> • IRC8M (8 MHz internal reference clock) • IRC2M (2 MHz internal reference clock) | 114 | 114 | 114 | 114 | 114 | 114 | μA |
| | | 34 | 34 | 34 | 34 | 34 | 34 | |
| I_{TPM} | TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents. <ul style="list-style-type: none"> • IRC8M (8 MHz internal reference clock) • IRC2M (2 MHz internal reference clock) | 147 | 147 | 147 | 147 | 147 | 147 | μA |
| | | 42 | 42 | 42 | 42 | 42 | 42 | |
| I_{BG} | Bandgap adder when BGEN bit is set and device is placed in VLPx or VLLSx mode. | 45 | 45 | 45 | 45 | 45 | 45 | μA |
| I_{ADC} | ADC peripheral adder combining the measured values at V_{DD} and V_{DDA} by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions. | 330 | 330 | 330 | 330 | 330 | 330 | μA |

2.2.5.1 Diagram: Typical I_{DD_RUN} operating behavior

The following data was measured under these conditions:

- MCG-Lite in HIRC for run mode, and LIRC for VLPR mode
- USB regulator disabled
- No GPIOs toggled
- Code execution from flash
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

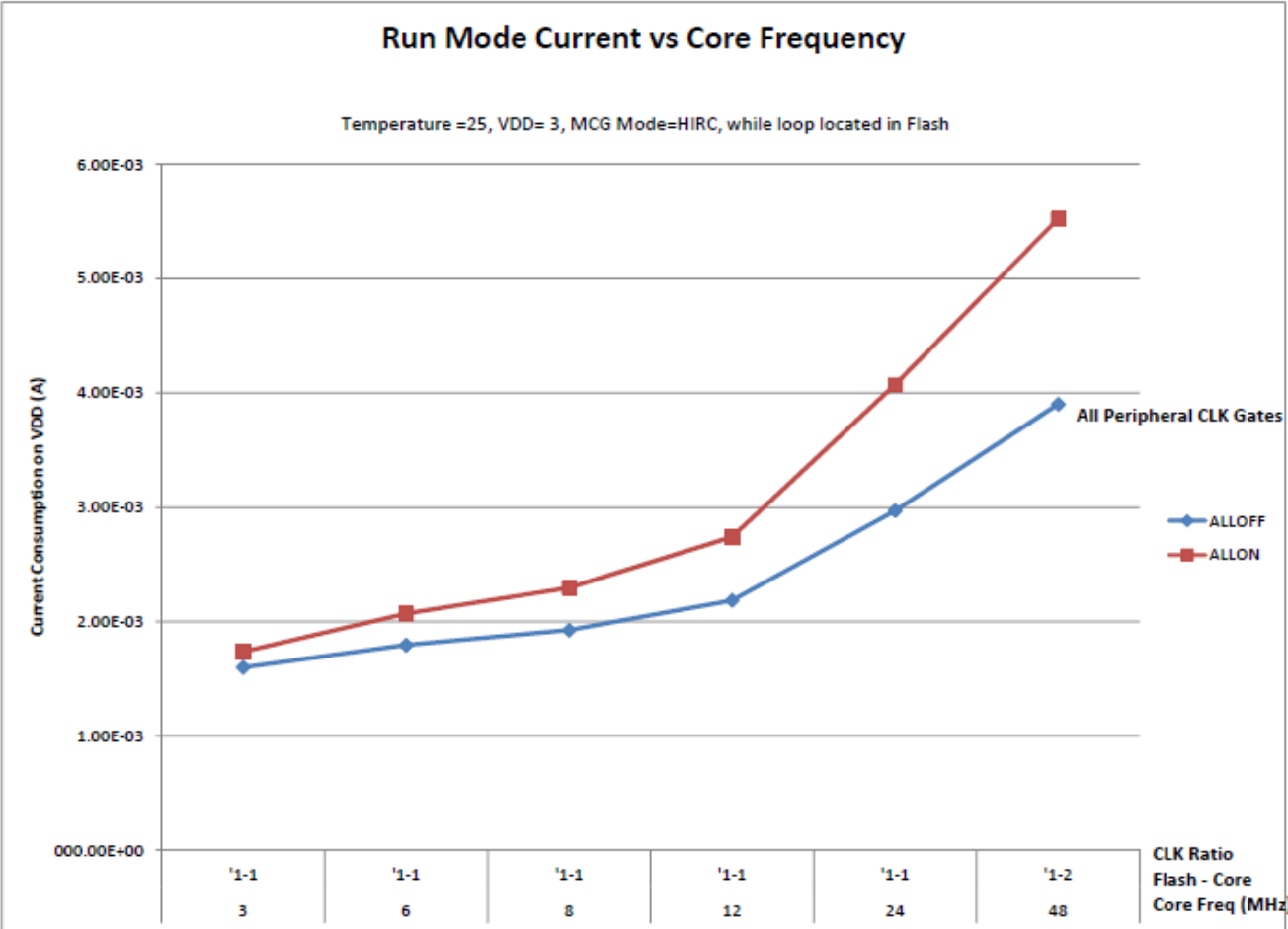
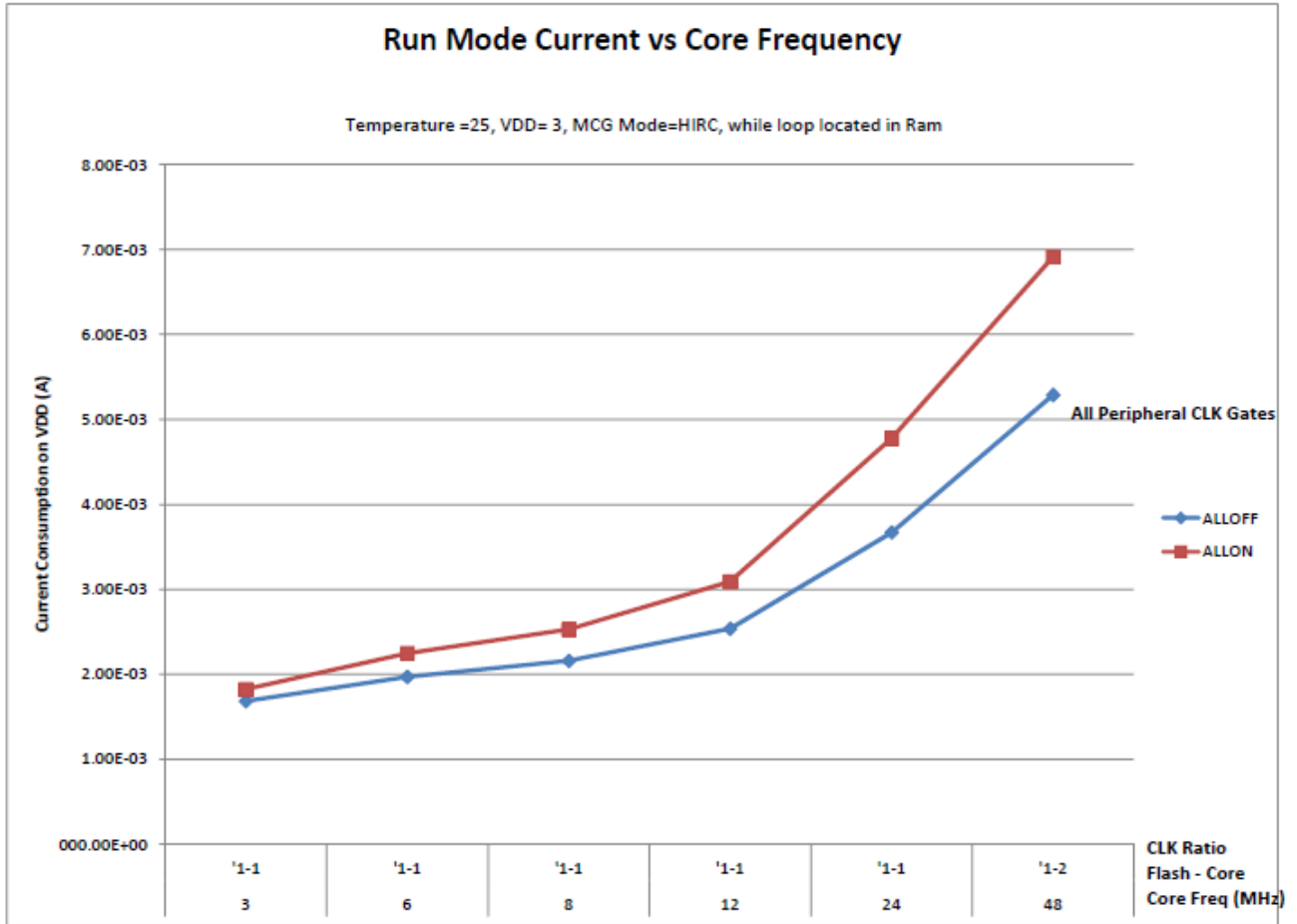


Figure 2. Run mode supply current vs. core frequency



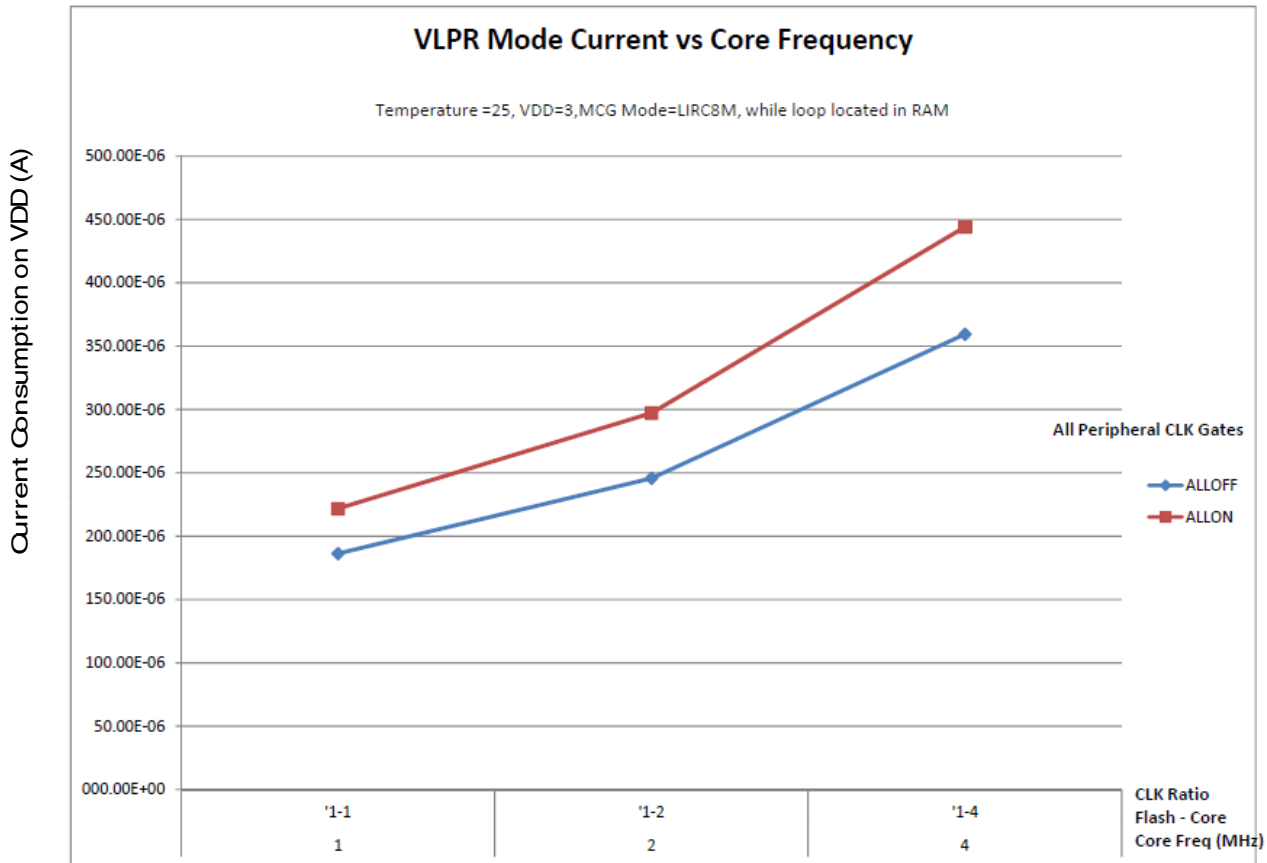


Figure 3. VLPR mode current vs. core frequency

2.2.6 EMC radiated emissions operating behaviors

Table 11. EMC radiated emissions operating behaviors for 64-pin LQFP package

| Symbol | Description | Frequency band (MHz) | Typ. | Unit | Notes |
|---------------------|------------------------------------|----------------------|------|------|-------|
| V _{RE1} | Radiated emissions voltage, band 1 | 0.15–50 | 11 | dBμV | 1, 2 |
| V _{RE2} | Radiated emissions voltage, band 2 | 50–150 | 12 | dBμV | |
| V _{RE3} | Radiated emissions voltage, band 3 | 150–500 | 10 | dBμV | |
| V _{RE4} | Radiated emissions voltage, band 4 | 500–1000 | 6 | dBμV | |
| V _{RE_IEC} | IEC level | 0.15–1000 | N | — | 2, 3 |

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement*

of *Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

2. $V_{DD} = 3.3\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$, $f_{OSC} = \text{IRC48M}$, $f_{SYS} = 48\text{ MHz}$, $f_{BUS} = 24\text{ MHz}$
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

2.2.8 Capacitance attributes

Table 12. Capacitance attributes

| Symbol | Description | Min. | Max. | Unit |
|----------|-------------------|------|------|------|
| C_{IN} | Input capacitance | — | 7 | pF |

2.3 Switching specifications

2.3.1 Device clock specifications

Table 13. Device clock specifications

| Symbol | Description | Min. | Max. | Unit |
|----------------------------------|--|------|------|------|
| Normal run mode | | | | |
| f_{SYS} | System and core clock ¹ | — | 48 | MHz |
| f_{BUS} | Bus clock ¹ | — | 24 | MHz |
| f_{FLASH} | Flash clock ¹ | — | 24 | MHz |
| f_{SYS_USB} | System and core clock when Full Speed USB in operation | 20 | — | MHz |
| f_{LPTMR} | LPTMR clock | — | 24 | MHz |
| VLPR and VLPS modes ² | | | | |
| f_{SYS} | System and core clock | — | 4 | MHz |
| f_{BUS} | Bus clock | — | 1 | MHz |
| f_{FLASH} | Flash clock | — | 1 | MHz |

Table continues on the next page...

Table 13. Device clock specifications (continued)

| Symbol | Description | Min. | Max. | Unit |
|--------------------|---|------|------|------|
| f_{LPTMR} | LPTMR clock ³ | — | 24 | MHz |
| f_{LPTMR_ERCLK} | LPTMR external reference clock | — | 16 | MHz |
| $f_{osc_hi_2}$ | Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x) | — | 16 | MHz |
| f_{TPM} | TPM asynchronous clock | — | 8 | MHz |
| $f_{LPUART0/1}$ | LPUART0/1 asynchronous clock | — | 8 | MHz |

1. The maximum value of system clock, core clock, bus clock, and flash clock under normal run mode can be 3% higher than the specified maximum frequency when IRC 48MHz is used as the clock source.
2. The frequency limitations in VLPR and VLPS modes here override any frequency specification listed in the timing specification for any other module. These same frequency limits apply to VLPS, whether VLPS was entered from RUN or from VLPR.
3. The LPTMR can be clocked at this speed in VLPR or VLPS only when the source is an external pin.

2.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO and UART signals.

Table 14. General switching specifications

| Description | Min. | Max. | Unit | Notes |
|--|------|------|------------------|-------|
| GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path | 1.5 | — | Bus clock cycles | 1 |
| External RESET and NMI pin interrupt pulse width — Asynchronous path | 100 | — | ns | 2 |
| GPIO pin interrupt pulse width — Asynchronous path | 16 | — | ns | 2 |
| Port rise and fall time | — | 36 | ns | 3 |

1. The synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. 75 pF load

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 15. Thermal operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|----------------|--------------------------|------|------|------|-------|
| T _J | Die junction temperature | -40 | 125 | °C | |
| T _A | Ambient temperature | -40 | 105 | °C | 1 |

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is: T_J = T_A + R_{θJA} × chip power dissipation.

2.4.2 Thermal attributes

Table 16. Thermal attributes

| Board type | Symbol | Description | 48 QFN | 32 QFN | 64 LQFP | 64 MAPBG A | Unit | Notes |
|-------------------|-------------------|---|--------|--------|---------|------------|------|-------|
| Single-layer (1S) | R _{θJA} | Thermal resistance, junction to ambient (natural convection) | 86 | 101 | 70 | 50.3 | °C/W | 1 |
| Four-layer (2s2p) | R _{θJA} | Thermal resistance, junction to ambient (natural convection) | 29 | 33 | 51 | 42.9 | °C/W | |
| Single-layer (1S) | R _{θJMA} | Thermal resistance, junction to ambient (200 ft./min. air speed) | 71 | 84 | 58 | 41.4 | °C/W | |
| Four-layer (2s2p) | R _{θJMA} | Thermal resistance, junction to ambient (200 ft./min. air speed) | 24 | 28 | 45 | 38.0 | °C/W | |
| — | R _{θJB} | Thermal resistance, junction to board | 12 | 13 | 33 | 39.6 | °C/W | 2 |
| — | R _{θJC} | Thermal resistance, junction to case | 1.7 | 1.7 | 20 | 27.3 | °C/W | 3 |
| — | Ψ _{JT} | Thermal characterization parameter, junction to package top outside center (natural convection) | 2 | 3 | 4 | 0.4 | °C/W | 4 |
| — | Ψ _{JB} | Thermal characterization parameter, junction to package bottom (natural convection) | - | - | - | 12.6 | °C/W | 5 |

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.

Peripheral operating requirements and behaviors

4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.
5. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 SWD electricals

Table 17. SWD full voltage range electricals

| Symbol | Description | Min. | Max. | Unit |
|--------|--|------|------|------|
| | Operating voltage | 1.71 | 3.6 | V |
| J1 | SWD_CLK frequency of operation <ul style="list-style-type: none"> • Serial wire debug | 0 | 25 | MHz |
| J2 | SWD_CLK cycle period | 1/J1 | — | ns |
| J3 | SWD_CLK clock pulse width <ul style="list-style-type: none"> • Serial wire debug | 20 | — | ns |
| J4 | SWD_CLK rise and fall times | — | 3 | ns |
| J9 | SWD_DIO input data setup time to SWD_CLK rise | 10 | — | ns |
| J10 | SWD_DIO input data hold time after SWD_CLK rise | 0 | — | ns |
| J11 | SWD_CLK high to SWD_DIO data valid | — | 32 | ns |
| J12 | SWD_CLK high to SWD_DIO high-Z | 5 | — | ns |

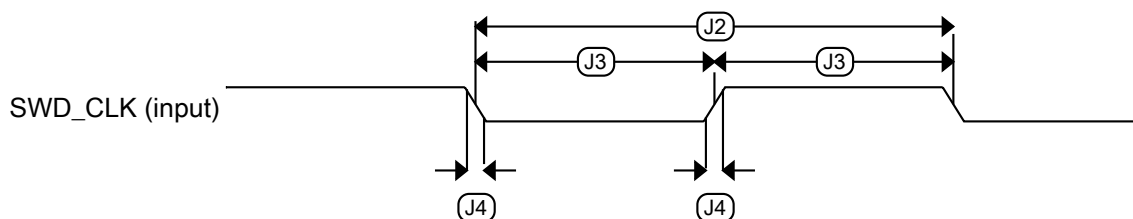


Figure 4. Serial wire clock input timing

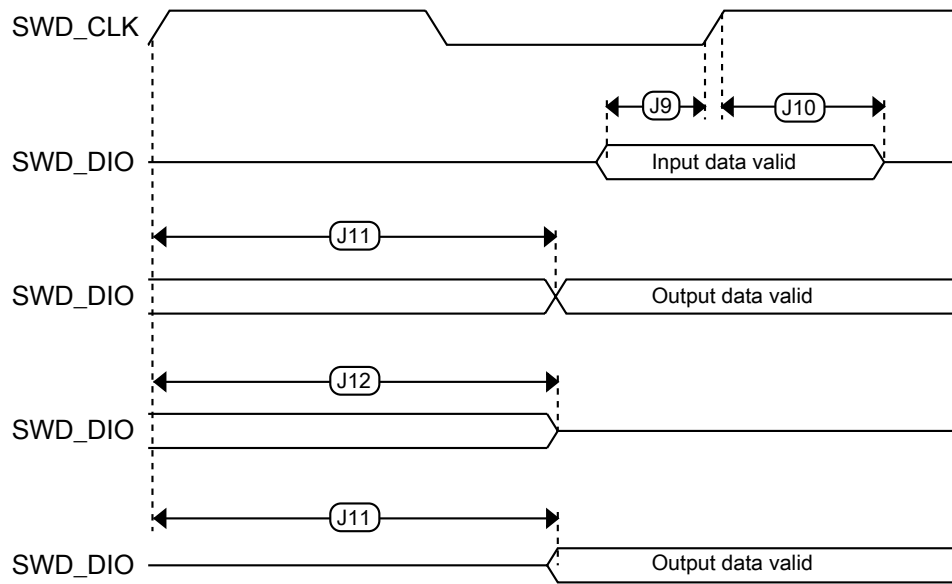


Figure 5. Serial wire data timing

3.2 System modules

There are no specifications necessary for the device's system modules.

3.3 Clock modules

3.3.1 MCG-Lite specifications

Table 18. IRC48M specification

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-----------------------------|---|------|-----------|-----------|----------------|-------|
| I_{DD} | Supply current | — | 400 | 500 | μA | — |
| f_{IRC} | Output frequency | — | 48 | — | MHz | — |
| $\Delta f_{irc48m_ol_lv}$ | Open loop total deviation of IRC48M frequency at low voltage (VDD=1.71V-1.89V) over temperature | — | ± 0.5 | ± 1.5 | $\%f_{irc48m}$ | 1 |
| $\Delta f_{irc48m_ol_hv}$ | Open loop total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over temperature | — | ± 0.5 | ± 1.0 | $\%f_{irc48m}$ | 1 |

Table continues on the next page...

Table 18. IRC48M specification (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|----------|---------------------|------|------|------|---------|-------|
| T_j | Period jitter (RMS) | — | 35 | 150 | ps | — |
| T_{su} | Startup time | — | 2 | 3 | μ s | — |

1. The maximum value represents characterized results equivalent to mean plus or minus three times the standard deviation (mean \pm 3sigma).

Table 19. IRC8M/2M specification

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|------------------|----------------------------------|------|------|---------|-------------|-------|
| I_{DD_2M} | Supply current in 2 MHz mode | — | 14 | 17 | μ A | — |
| I_{DD_8M} | Supply current in 8 MHz mode | — | 30 | 35 | μ A | — |
| f_{IRC_2M} | Output frequency | — | 2 | — | MHz | — |
| f_{IRC_8M} | Output frequency | — | 8 | — | MHz | — |
| $f_{IRC_T_2M}$ | Output frequency range (trimmed) | — | — | \pm 3 | $\%f_{IRC}$ | — |
| $f_{IRC_T_8M}$ | Output frequency range (trimmed) | — | — | \pm 3 | $\%f_{IRC}$ | — |
| T_{su_2M} | Startup time | — | — | 12.5 | μ s | — |
| T_{su_8M} | Startup time | — | — | 12.5 | μ s | — |

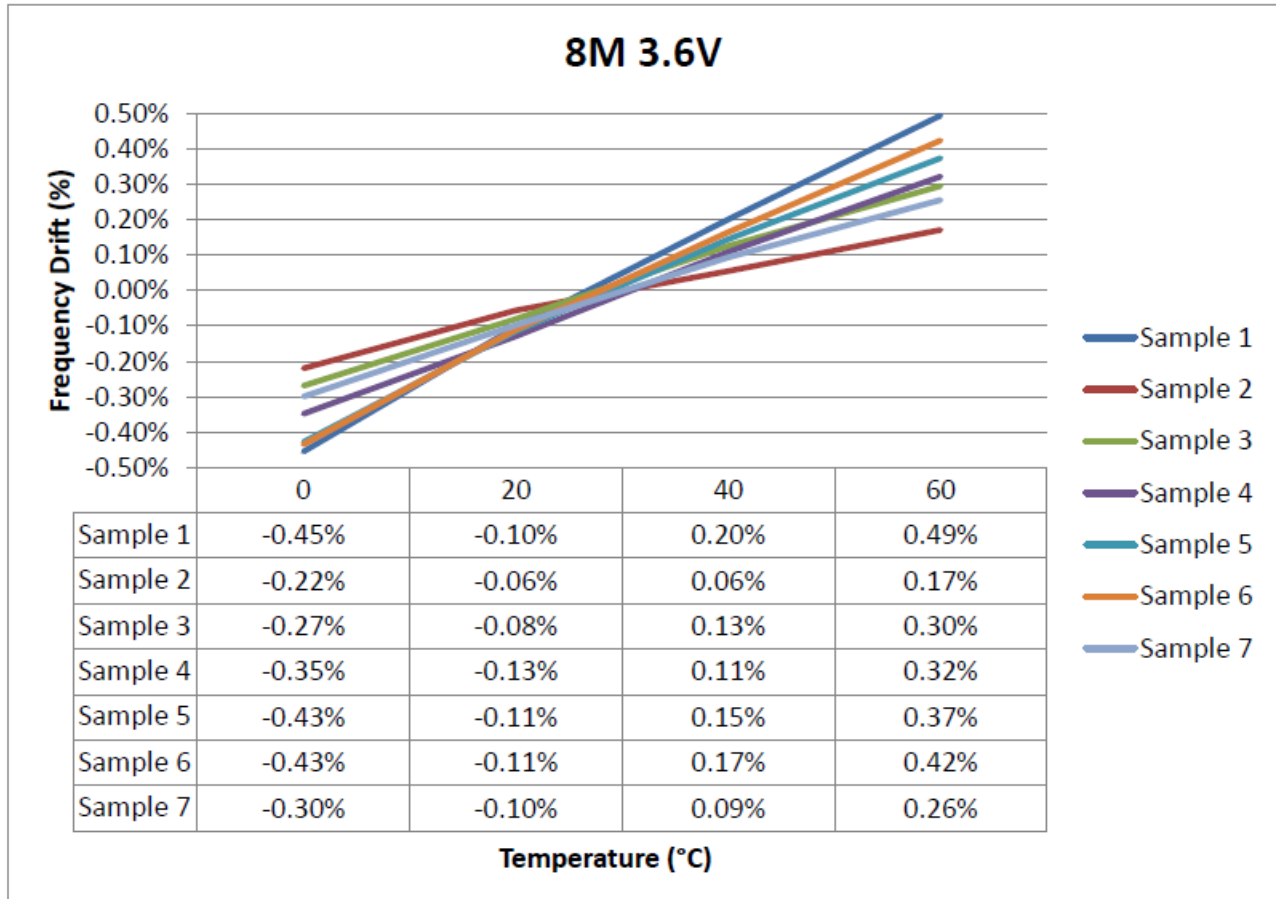


Figure 6. IRC8M Frequency Drift vs Temperature curve

3.3.2 Oscillator electrical specifications

3.3.2.1 Oscillator DC electrical specifications

Table 20. Oscillator DC electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-------------|---|------|------|------|---------|-------|
| V_{DD} | Supply voltage | 1.71 | — | 3.6 | V | |
| I_{DDOSC} | Supply current — low-power mode (HGO=0) | | | | | 1 |
| | • 32 kHz | — | 500 | — | nA | |
| | • 4 MHz | — | 200 | — | μ A | |
| | • 8 MHz (RANGE=01) | — | 300 | — | μ A | |
| | • 16 MHz | — | 950 | — | μ A | |
| | | — | 1.2 | — | mA | |

Table continues on the next page...

Table 20. Oscillator DC electrical specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-------------|---|------|----------|------|------------|-------|
| | <ul style="list-style-type: none"> • 24 MHz • 32 MHz | — | 1.5 | — | mA | |
| I_{DDOSC} | Supply current — high gain mode (HGO=1) <ul style="list-style-type: none"> • 32 kHz • 4 MHz • 8 MHz (RANGE=01) • 16 MHz • 24 MHz • 32 MHz | — | 25 | — | μ A | 1 |
| | | — | 400 | — | μ A | |
| | | — | 500 | — | μ A | |
| | | — | 2.5 | — | mA | |
| | | — | 3 | — | mA | |
| | | — | 4 | — | mA | |
| C_x | EXTAL load capacitance | — | — | — | | 2, 3 |
| C_y | XTAL load capacitance | — | — | — | | 2, 3 |
| R_F | Feedback resistor — low-frequency, low-power mode (HGO=0) | — | — | — | M Ω | 2, 4 |
| | Feedback resistor — low-frequency, high-gain mode (HGO=1) | — | 10 | — | M Ω | |
| | Feedback resistor — high-frequency, low-power mode (HGO=0) | — | — | — | M Ω | |
| | Feedback resistor — high-frequency, high-gain mode (HGO=1) | — | 1 | — | M Ω | |
| R_S | Series resistor — low-frequency, low-power mode (HGO=0) | — | — | — | k Ω | |
| | Series resistor — low-frequency, high-gain mode (HGO=1) | — | 200 | — | k Ω | |
| | Series resistor — high-frequency, low-power mode (HGO=0) | — | — | — | k Ω | |
| | Series resistor — high-frequency, high-gain mode (HGO=1) | — | 0 | — | k Ω | |
| V_{pp}^5 | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1) | — | V_{DD} | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1) | — | V_{DD} | — | V | |

1. $V_{DD}=3.3$ V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation

3. C_x, C_y can be provided by using the integrated capacitors when the low frequency oscillator (RANGE = 00) is used. For all other cases external capacitors must be used.
4. When low power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

3.3.2.2 Oscillator frequency specifications

Table 21. Oscillator frequency specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|------------------|---|------|------|------|------|-------|
| f_{osc_lo} | Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00) | 32 | — | 40 | kHz | |
| $f_{osc_hi_1}$ | Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01) | 3 | — | 8 | MHz | |
| $f_{osc_hi_2}$ | Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x) | 8 | — | 32 | MHz | |
| f_{ec_extal} | Input clock frequency (external clock mode) | — | — | 48 | MHz | 1, 2 |
| t_{dc_extal} | Input clock duty cycle (external clock mode) | 40 | 50 | 60 | % | |
| t_{cst} | Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0) | — | 750 | — | ms | 3, 4 |
| | Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1) | — | 250 | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0) | — | 0.6 | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1) | — | 1 | — | ms | |

1. Other frequency limits may apply when external clock is being used as a reference for the FLL.
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

3.4 Memories and memory interfaces

3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 22. NVM program/erase timing specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|----------------------------------|--|------|------|------|---------------|-------|
| $t_{hvp\text{gm}4}$ | Longword Program high-voltage time | — | 7.5 | 18 | μs | — |
| $t_{h\text{versscr}}$ | Sector Erase high-voltage time | — | 13 | 113 | ms | 1 |
| $t_{h\text{versblk}128\text{k}}$ | Erase Block high-voltage time for 128 KB | — | 52 | 452 | ms | 1 |

1. Maximum time based on expectations at cycling end-of-life.

3.4.1.2 Flash timing specifications — commands

Table 23. Flash command timing specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------------------------------|--|------|------|------|---------------|-------|
| $t_{rd1\text{blk}128\text{k}}$ | Read 1s Block execution time • 128 KB program flash | — | — | 1.7 | ms | 1 |
| $t_{rd1\text{sec}1\text{k}}$ | Read 1s Section execution time (flash sector) | — | — | 60 | μs | 1 |
| $t_{pgm\text{chk}}$ | Program Check execution time | — | — | 45 | μs | 1 |
| $t_{rd\text{rsrc}}$ | Read Resource execution time | — | — | 30 | μs | 1 |
| t_{pgm4} | Program Longword execution time | — | 65 | 145 | μs | — |
| $t_{ers\text{blk}128\text{k}}$ | Erase Flash Block execution time • 128 KB program flash | — | 88 | 600 | ms | 2 |
| $t_{ers\text{scr}}$ | Erase Flash Sector execution time | — | 14 | 114 | ms | 2 |
| $t_{rd1\text{all}}$ | Read 1s All Blocks execution time | — | — | 1.8 | ms | 1 |
| $t_{rd\text{once}}$ | Read Once execution time | — | — | 25 | μs | 1 |
| $t_{pgm\text{once}}$ | Program Once execution time | — | 65 | — | μs | — |
| $t_{ers\text{all}}$ | Erase All Blocks execution time | — | 175 | 1300 | ms | 2 |
| t_{vfykey} | Verify Backdoor Access Key execution time | — | — | 30 | μs | 1 |
| $t_{ers\text{allu}}$ | Erase All Blocks Unsecure execution time | — | 175 | 1300 | ms | 2 |

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

3.4.1.3 Flash high voltage current behaviors

Table 24. Flash high voltage current behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---------------------|---|------|------|------|------|
| I _{DD_PGM} | Average current adder during high voltage flash programming operation | — | 2.5 | 6.0 | mA |
| I _{DD_ERS} | Average current adder during high voltage flash erase operation | — | 1.5 | 4.0 | mA |

3.4.1.4 Reliability specifications

Table 25. NVM reliability specifications

| Symbol | Description | Min. | Typ. ¹ | Max. | Unit | Notes |
|-------------------------|--|------|-------------------|------|--------|-------|
| Program Flash | | | | | | |
| t _{nvmretp10k} | Data retention after up to 10 K cycles | 5 | 50 | — | years | — |
| t _{nvmretp1k} | Data retention after up to 1 K cycles | 20 | 100 | — | years | — |
| n _{nvmcycp} | Cycling endurance | 10 K | 50 K | — | cycles | 2 |

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at $-40\text{ °C} \leq T_j \leq 125\text{ °C}$.

3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

3.6 Analog

3.6.1 ADC electrical specifications

Using differential inputs can achieve better system accuracy than using single-end inputs.

3.6.1.1 16-bit ADC operating conditions

Table 26. 16-bit ADC operating conditions

| Symbol | Description | Conditions | Min. | Typ. ¹ | Max. | Unit | Notes |
|-------------------|-------------------------------------|---|--|-------------------|--|------|-------|
| V _{DDA} | Supply voltage | Absolute | 1.71 | — | 3.6 | V | — |
| ΔV _{DDA} | Supply voltage | Delta to V _{DD} (V _{DD} – V _{DDA}) | -100 | 0 | +100 | mV | 2 |
| ΔV _{SSA} | Ground voltage | Delta to V _{SS} (V _{SS} – V _{SSA}) | -100 | 0 | +100 | mV | 2 |
| V _{REFH} | ADC reference voltage high | | 1.13 | V _{DDA} | V _{DDA} | V | 3 |
| V _{REFL} | ADC reference voltage low | | V _{SSA} | V _{SSA} | V _{SSA} | V | 3 |
| V _{ADIN} | Input voltage | <ul style="list-style-type: none"> 16-bit differential mode All other modes | V _{REFL} V _{REFL} | — — | 31/32 × V _{REFH} V _{REFH} | V | — |
| C _{ADIN} | Input capacitance | <ul style="list-style-type: none"> 16-bit mode 8-bit / 10-bit / 12-bit modes | — — | 8 4 | 10 5 | pF | — |
| R _{ADIN} | Input series resistance | | — | 2 | 5 | kΩ | — |
| R _{AS} | Analog source resistance (external) | 13-bit / 12-bit modes f _{ADCK} < 4 MHz | — | — | 5 | kΩ | 4 |
| f _{ADCK} | ADC conversion clock frequency | ≤ 13-bit mode | 1.0 | — | 24 | MHz | 5 |
| f _{ADCK} | ADC conversion clock frequency | 16-bit mode | 2.0 | — | 12.0 | MHz | 5 |
| C _{rate} | ADC conversion rate | ≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time | 20.000 | — | 1200 | ksps | 6 |
| C _{rate} | ADC conversion rate | 16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time | 37.037 | — | 461.467 | ksps | 6 |

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. V_{REFH} can act as V_{REF_OUT} when V_{REFV1} module is enabled.
4. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
5. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
6. For guidelines and examples of conversion rate calculation, download the [ADC calculator tool](#).

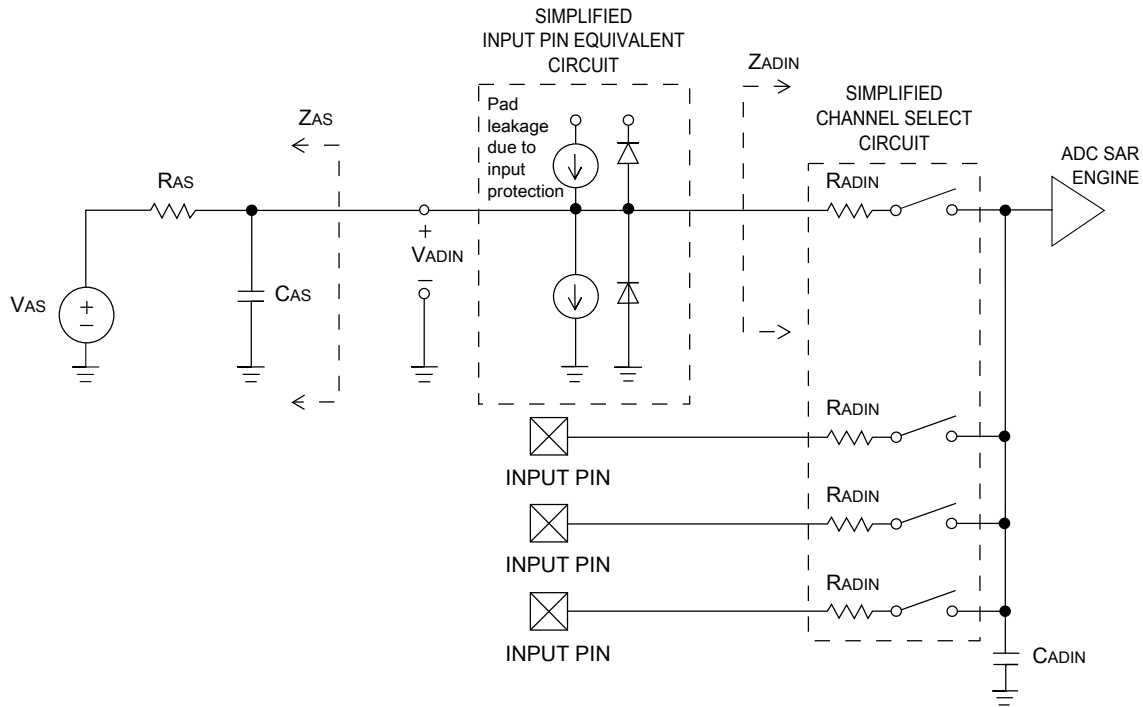


Figure 7. ADC input impedance equivalency diagram

3.6.1.2 16-bit ADC electrical characteristics

Table 27. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

| Symbol | Description | Conditions ¹ | Min. | Typ. ² | Max. | Unit | Notes |
|----------------|-------------------------------|---|-------|-------------------|-----------------------------|------------------|---------------------------|
| I_{DDA_ADC} | Supply current | | 0.215 | — | 1.7 | mA | 3 |
| f_{ADACK} | ADC asynchronous clock source | • ADLPC = 1, ADHSC = 0 | 1.2 | 2.4 | 3.9 | MHz | $t_{ADACK} = 1/f_{ADACK}$ |
| | | • ADLPC = 1, ADHSC = 1 | 2.4 | 4.0 | 6.1 | MHz | |
| | | • ADLPC = 0, ADHSC = 0 | 3.0 | 5.2 | 7.3 | MHz | |
| | | • ADLPC = 0, ADHSC = 1 | 4.4 | 6.2 | 9.5 | MHz | |
| | Sample Time | See Reference Manual chapter for sample times | | | | | |
| TUE | Total unadjusted error | • 12-bit modes • <12-bit modes | — | ±4 ±1.4 | ±6.8 ±2.1 | LSB ⁴ | 5 |
| DNL | Differential non-linearity | • 12-bit modes • <12-bit modes | — | ±0.7 ±0.2 | -1.1 to +1.9 -0.3 to 0.5 | LSB ⁴ | 5 |
| INL | Integral non-linearity | • 12-bit modes | — | ±1.0 | -2.7 to +1.9 | LSB ⁴ | 5 |

Table continues on the next page...

Table 27. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

| Symbol | Description | Conditions ¹ | Min. | Typ. ² | Max. | Unit | Notes | |
|--------------|---------------------------------|--|------------------------|-------------------|--------------|------------------|---|--|
| | | <ul style="list-style-type: none"> <12-bit modes | — | ±0.5 | -0.7 to +0.5 | | | |
| E_{FS} | Full-scale error | <ul style="list-style-type: none"> 12-bit modes <12-bit modes | — | -4 | -5.4 | LSB ⁴ | $V_{ADIN} = V_{DDA}$ ⁵ | |
| E_Q | Quantization error | <ul style="list-style-type: none"> 16-bit modes ≤13-bit modes | — | -1 to 0 | — | LSB ⁴ | | |
| ENOB | Effective number of bits | 16-bit differential mode | | | | | 6 | |
| | | <ul style="list-style-type: none"> Avg = 32 Avg = 4 | 12.8 | 14.5 | | bits | | |
| | | 16-bit single-ended mode | | 11.9 | 13.8 | — | bits | |
| | | <ul style="list-style-type: none"> Avg = 32 Avg = 4 | 12.2 | 13.9 | — | bits | | |
| | | | 11.4 | 13.1 | — | | | |
| SINAD | Signal-to-noise plus distortion | See ENOB | 6.02 × ENOB + 1.76 | | | dB | | |
| THD | Total harmonic distortion | 16-bit differential mode | | | | dB | 7 | |
| | | <ul style="list-style-type: none"> Avg = 32 | — | -94 | — | dB | | |
| | | 16-bit single-ended mode | | | | dB | | |
| | | <ul style="list-style-type: none"> Avg = 32 | — | -85 | — | | | |
| SFDR | Spurious free dynamic range | 16-bit differential mode | | | | dB | 7 | |
| | | <ul style="list-style-type: none"> Avg = 32 | 82 | 95 | — | dB | | |
| | | 16-bit single-ended mode | | | | dB | | |
| | | <ul style="list-style-type: none"> Avg = 32 | 78 | 90 | — | | | |
| E_{IL} | Input leakage error | | $I_{in} \times R_{AS}$ | | | mV | I_{in} = leakage current (refer to the MCU's voltage and current operating ratings) | |
| | Temp sensor slope | Across the full temperature range of the device | 1.55 | 1.62 | 1.69 | mV/°C | 8 | |
| V_{TEMP25} | Temp sensor voltage | 25 °C | 706 | 716 | 726 | mV | 8 | |

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$

2. Typical values assume $V_{DDA} = 3.0\text{ V}$, $\text{Temp} = 25\text{ }^{\circ}\text{C}$, $f_{\text{ADCK}} = 2.0\text{ MHz}$ unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. $1\text{ LSB} = (V_{\text{REFH}} - V_{\text{REFL}})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz

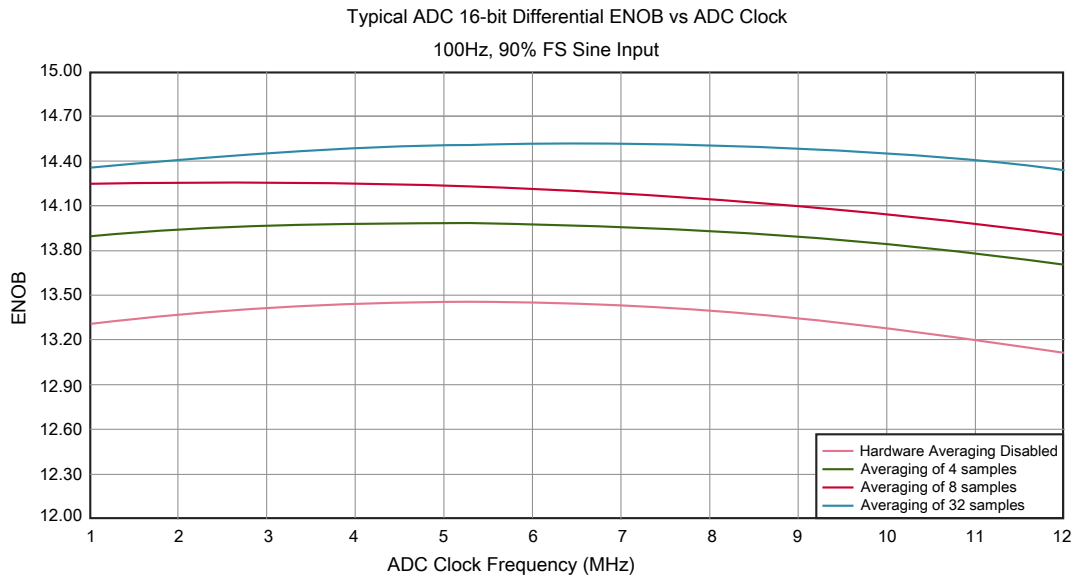


Figure 8. Typical ENOB vs. ADC_CLK for 16-bit differential mode

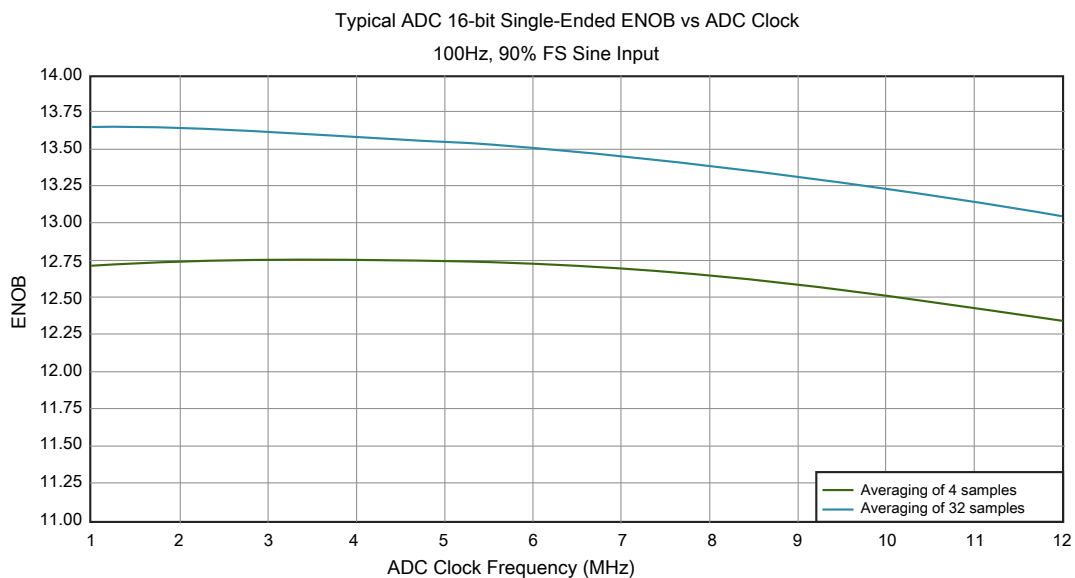


Figure 9. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

3.6.2 Voltage reference electrical specifications

Table 28. VREF full-range operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------------|-------------------------|---|------|------|-------|
| V _{DDA} | Supply voltage | | 3.6 | V | — |
| T _A | Temperature | Operating temperature range of the device | | °C | — |
| C _L | Output load capacitance | 100 | | nF | 1, 2 |

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

Table 29 is tested under the condition of setting VREF_TRM[CHOPEN], VREF_SC[REGEN] and VREF_SC[ICOMPEN] bits to 1.

Table 29. VREF full-range operating behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---------------------------------|---|--------|-------|--------|------|-------|
| V _{out} | Voltage reference output with factory trim at nominal V _{DDA} and temperature=25C | 1.1915 | 1.195 | 1.1977 | V | 1 |
| V _{out} | Voltage reference output — factory trim | 1.1584 | — | 1.2376 | V | 1 |
| V _{out} | Voltage reference output — user trim | 1.193 | — | 1.197 | V | 1 |
| V _{step} | Voltage reference trim step | — | 0.5 | — | mV | 1 |
| V _{tdrift} | Temperature drift (V _{max} -V _{min} across the full temperature range: 0 to 70°C) | — | — | 50 | mV | 1 |
| I _{bg} | Bandgap only current | — | — | 80 | µA | 1 |
| I _{lp} | Low-power buffer current | — | — | 360 | µA | 1 |
| I _{hp} | High-power buffer current | — | — | 1 | mA | 1 |
| ΔV _{LOAD} | Load regulation • current = ± 1.0 mA | — | 200 | — | µV | 1, 2 |
| T _{stup} | Buffer startup time | — | — | 100 | µs | — |
| T _{chop_osc_st up} | Internal bandgap start-up delay with chop oscillator enabled | — | — | 35 | ms | — |
| V _{vdrift} | Voltage drift (V _{max} -V _{min} across the full voltage range) | — | 2 | — | mV | 1 |

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

Table 30. VREF limited-range operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|-------------|------|------|------|-------|
| T_A | Temperature | 0 | 50 | °C | — |

Table 31. VREF limited-range operating behaviors

| Symbol | Description | Min. | Max. | Unit | Notes |
|-----------|--|-------|-------|------|-------|
| V_{out} | Voltage reference output with factory trim | 1.173 | 1.225 | V | — |

3.6.3 CMP and 6-bit DAC electrical specifications

Table 32. Comparator and 6-bit DAC electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit |
|-------------|--|----------------|---------------------|----------|----------------------|
| V_{DD} | Supply voltage | 1.71 | — | 3.6 | V |
| I_{DDHS} | Supply current, High-speed mode (EN=1, PMODE=1) | — | — | 200 | μA |
| $I_{DDL S}$ | Supply current, low-speed mode (EN=1, PMODE=0) | — | — | 20 | μA |
| V_{AIN} | Analog input voltage | $V_{SS} - 0.3$ | — | V_{DD} | V |
| V_{AIO} | Analog input offset voltage | — | — | 20 | mV |
| V_H | Analog comparator hysteresis ¹ <ul style="list-style-type: none"> • CR0[HYSTCTR] = 00 • CR0[HYSTCTR] = 01 • CR0[HYSTCTR] = 10 • CR0[HYSTCTR] = 11 | — | 5 10 20 30 | — | mV mV mV mV |
| V_{CMPOH} | Output high | $V_{DD} - 0.5$ | — | — | V |
| V_{CMPOI} | Output low | — | — | 0.5 | V |
| t_{DHS} | Propagation delay, high-speed mode (EN=1, PMODE=1) | 20 | 50 | 200 | ns |
| t_{DLS} | Propagation delay, low-speed mode (EN=1, PMODE=0) | 80 | 250 | 600 | ns |
| | Analog comparator initialization delay ² | — | — | 40 | μs |
| I_{DAC6b} | 6-bit DAC current adder (enabled) | — | 7 | — | μA |
| INL | 6-bit DAC integral non-linearity | -0.5 | — | 0.5 | LSB ³ |
| DNL | 6-bit DAC differential non-linearity | -0.3 | — | 0.3 | LSB |

1. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD}-0.6$ V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}/64$

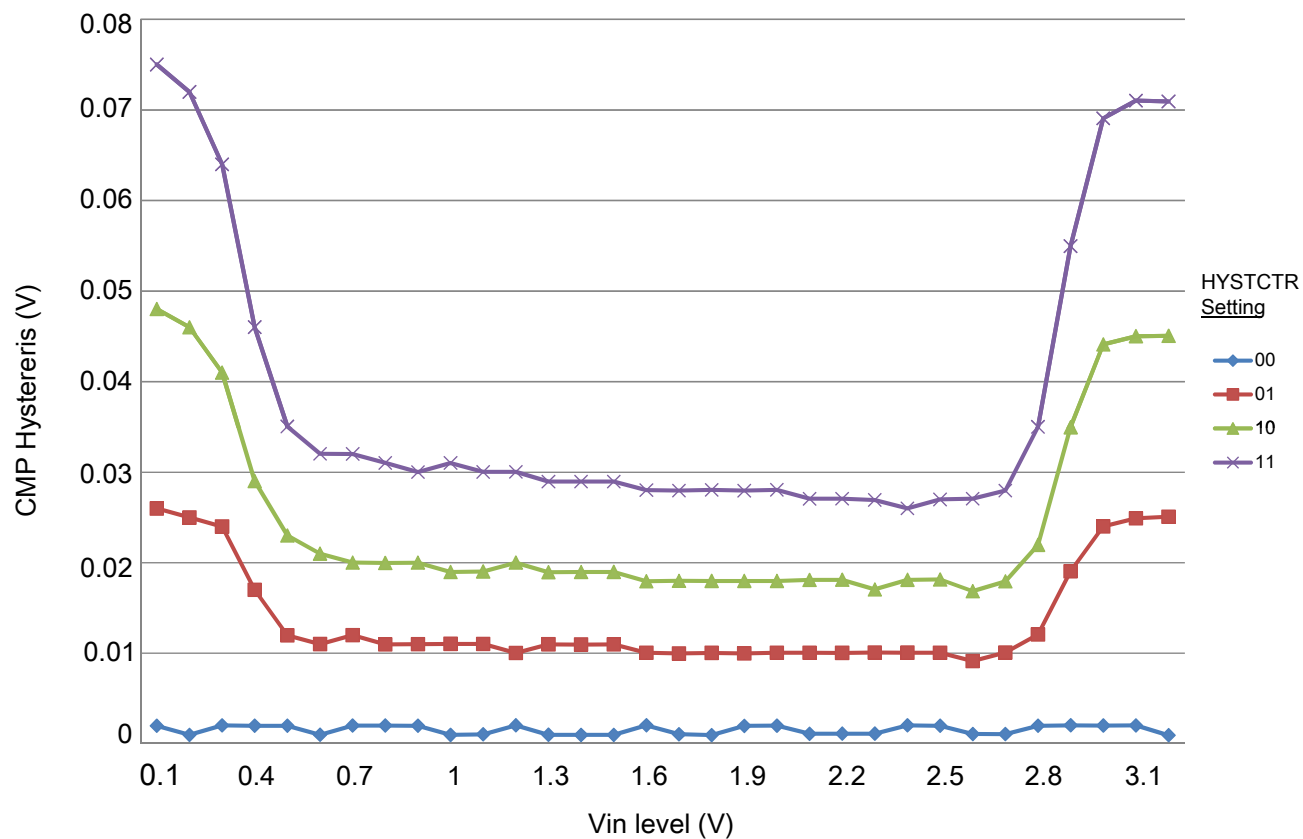


Figure 10. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

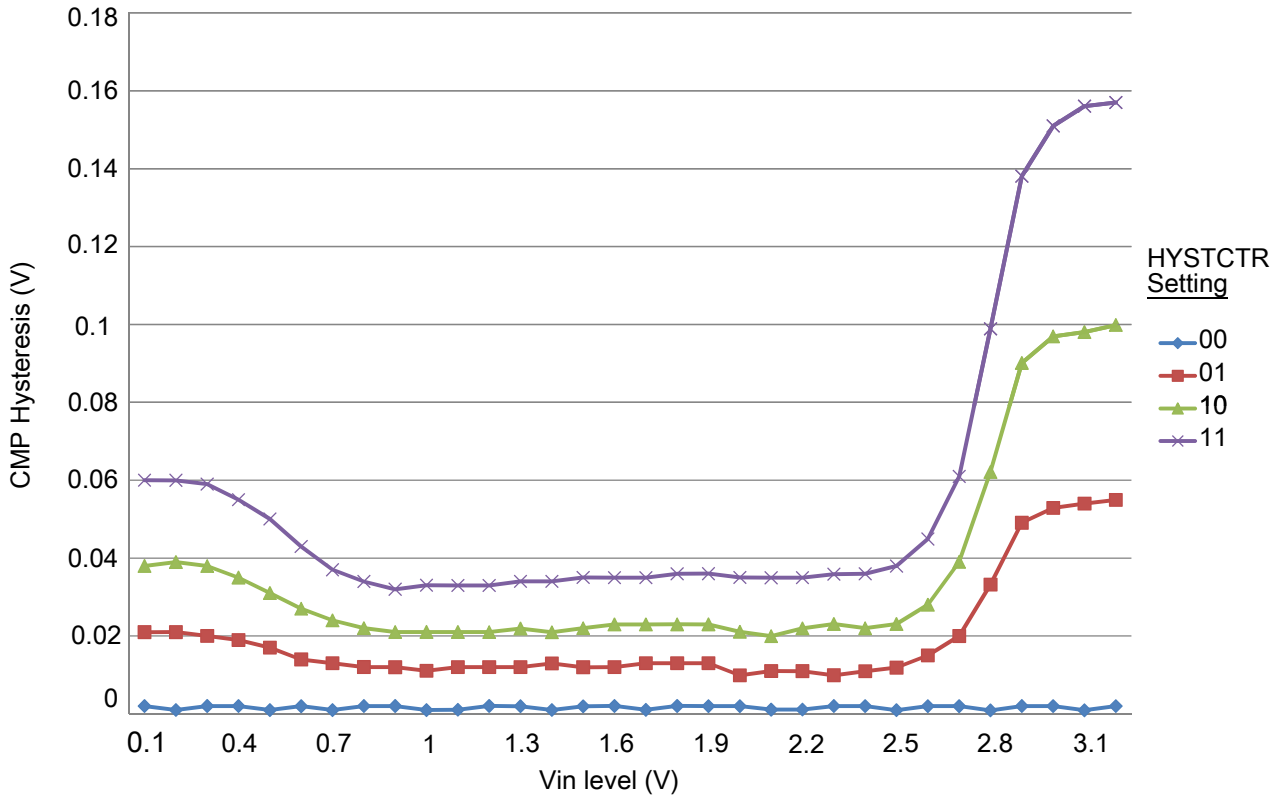


Figure 11. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

3.6.4 12-bit DAC electrical characteristics

3.6.4.1 12-bit DAC operating requirements

Table 33. 12-bit DAC operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------|-------------------------|------|------|------|-------|
| V_{DDA} | Supply voltage | | 3.6 | V | |
| V_{DACR} | Reference voltage | 1.13 | 3.6 | V | 1 |
| C_L | Output load capacitance | — | 100 | pF | 2 |
| I_L | Output load current | — | 1 | mA | |

1. The DAC reference can be selected to be V_{DDA} or V_{REFH} .
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

3.6.4.2 12-bit DAC operating behaviors

Table 34. 12-bit DAC operating behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|------------------|---|------------------|-------------|------------|------------------------|-------|
| I_{DDA_DACLP} | Supply current — low-power mode | — | — | 250 | μA | |
| I_{DDA_DACHP} | Supply current — high-speed mode | — | — | 900 | μA | |
| t_{DACLP} | Full-scale settling time (0x080 to 0xF7F) — low-power mode | — | 100 | 200 | μs | 1 |
| t_{DACHP} | Full-scale settling time (0x080 to 0xF7F) — high-power mode | — | 15 | 30 | μs | 1 |
| $t_{CCDACLP}$ | Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode | — | 0.7 | 1 | μs | 1 |
| $V_{dacoutl}$ | DAC output voltage range low — high-speed mode, no load, DAC set to 0x000 | — | — | 100 | mV | |
| $V_{dacouth}$ | DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFFF | $V_{DACR} - 100$ | — | V_{DACR} | mV | |
| INL | Integral non-linearity error — high speed mode | — | — | ± 8 | LSB | 2 |
| DNL | Differential non-linearity error — $V_{DACR} > 2\text{ V}$ | — | — | ± 1 | LSB | 3 |
| DNL | Differential non-linearity error — $V_{DACR} = V_{REF_OUT}$ | — | — | ± 1 | LSB | 4 |
| V_{OFFSET} | Offset error | — | ± 0.4 | ± 0.8 | %FSR | 5 |
| E_G | Gain error | — | ± 0.1 | ± 0.6 | %FSR | 5 |
| PSRR | Power supply rejection ratio, $V_{DDA} \geq 2.4\text{ V}$ | 60 | — | 90 | dB | |
| T_{CO} | Temperature coefficient offset voltage | — | 3.7 | — | $\mu\text{V}/\text{C}$ | 6 |
| T_{GE} | Temperature coefficient gain error | — | 0.000421 | — | %FSR/C | |
| R_{op} | Output resistance (load = 3 k Ω) | — | — | 250 | Ω | |
| SR | Slew rate -80h → F7Fh → 80h <ul style="list-style-type: none"> • High power (SP_{HP}) • Low power (SP_{LP}) | 1.2 0.05 | 1.7 0.12 | — — | V/ μs | |
| BW | 3dB bandwidth <ul style="list-style-type: none"> • High power (SP_{HP}) • Low power (SP_{LP}) | 550 40 | — — | — — | kHz | |

1. Settling within ± 1 LSB
2. The INL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV
3. The DNL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV
4. The DNL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV with $V_{DDA} > 2.4\text{ V}$
5. Calculated by a best fit curve from $V_{SS} + 100$ mV to $V_{DACR} - 100$ mV
6. $V_{DDA} = 3.0\text{ V}$, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_CO:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

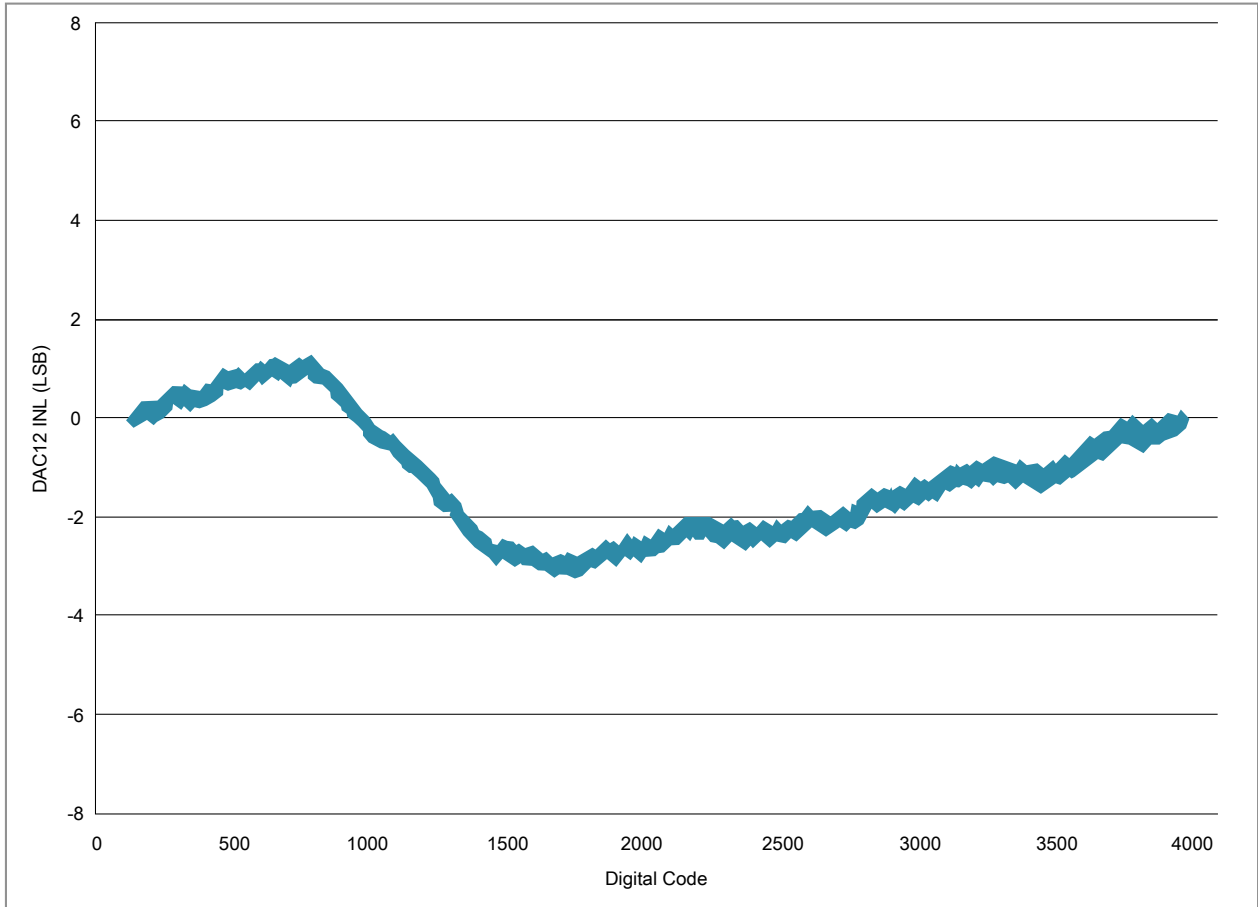


Figure 12. Typical INL error vs. digital code

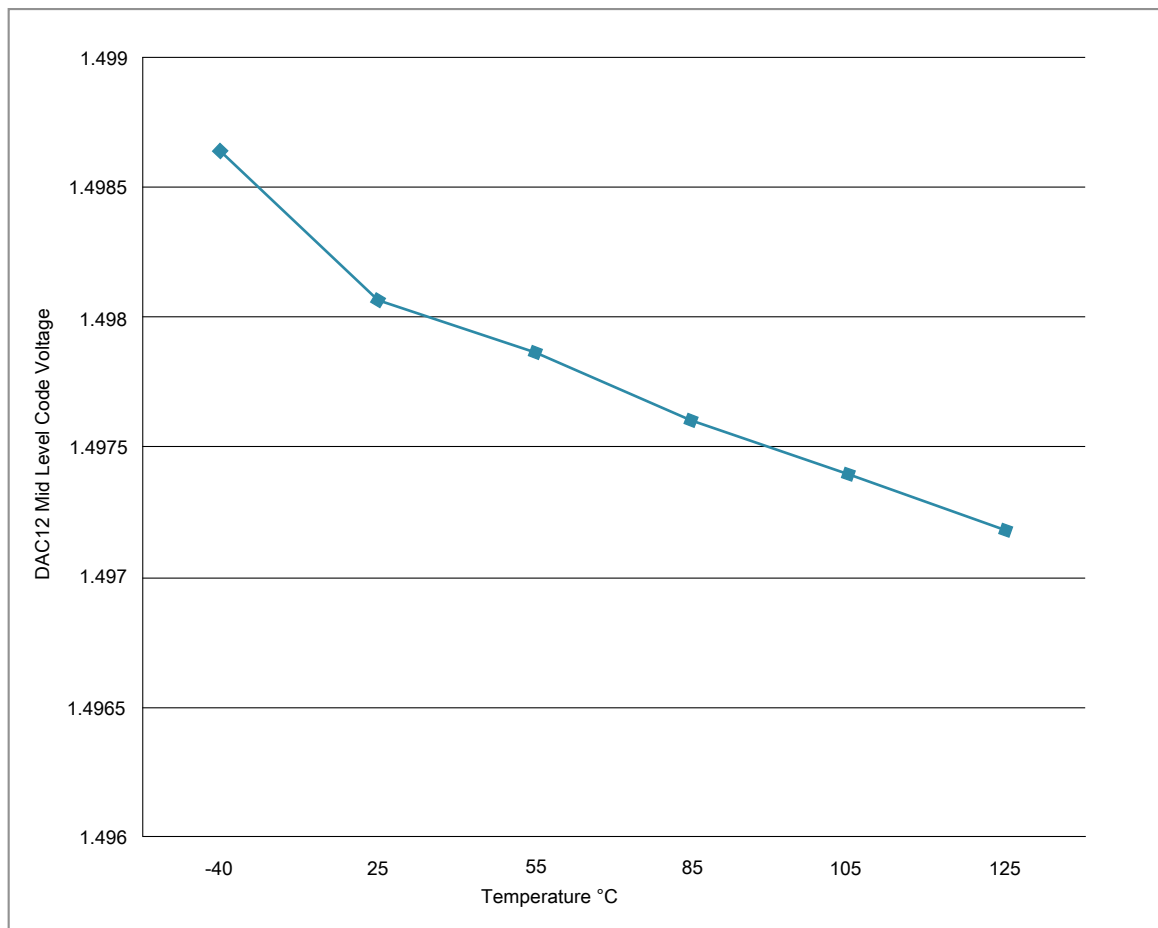


Figure 13. Offset at half scale vs. temperature

3.7 Timers

See [General switching specifications](#).

3.8 Communication interfaces

3.8.1 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit usb.org.

NOTE

The IRC48M do not meet the USB jitter specifications for certification for Host mode operation.

This device cannot support Host mode operation.

3.8.2 USB VREG electrical specifications

Table 35. USB VREG electrical specifications

| Symbol | Description | Min. | Typ. ¹ | Max. | Unit | Notes |
|-----------------------|--|------|-------------------|------|------|-------|
| VREGIN | Input supply voltage | 2.7 | — | 5.5 | V | |
| I _{DDon} | Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V | — | 125 | 186 | μA | |
| I _{DDstby} | Quiescent current — Standby mode, load current equal zero | — | 1.1 | 10 | μA | |
| I _{DDoff} | Quiescent current — Shutdown mode <ul style="list-style-type: none"> VREGIN = 5.0 V and temperature=25 °C Across operating voltage and temperature | — | 650 | — | nA | |
| | | — | — | 4 | μA | |
| I _{LOADrun} | Maximum load current — Run mode | — | — | 120 | mA | |
| I _{LOADstby} | Maximum load current — Standby mode | — | — | 1 | mA | |
| V _{Reg33out} | Regulator output voltage — Input supply (VREGIN) > 3.6 V <ul style="list-style-type: none"> Run mode Standby mode | 3 | 3.3 | 3.6 | V | |
| | | 2.1 | 2.8 | 3.6 | V | |
| V _{Reg33out} | Regulator output voltage — Input supply (VREGIN) < 3.6 V, pass-through mode | 2.1 | — | 3.6 | V | 2 |
| C _{OUT} | External output capacitor | 1.76 | 2.2 | 8.16 | μF | |
| ESR | External output capacitor equivalent series resistance | 1 | — | 100 | mΩ | |
| I _{LIM} | Short circuit current | — | 290 | — | mA | |

1. Typical values assume VREGIN = 5.0 V, Temp = 25 °C unless otherwise stated.

2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to I_{Load}.

3.8.3 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all SPI pins.

Table 36. SPI master mode timing on slew rate disabled pads

| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|------|--------------|--------------------------------|-----------------------|--------------------------|-------------|------|
| 1 | f_{op} | Frequency of operation | $f_{periph}/2048$ | $f_{periph}/2$ | Hz | 1 |
| 2 | t_{SPSCK} | SPSCK period | $2 \times t_{periph}$ | $2048 \times t_{periph}$ | ns | 2 |
| 3 | t_{Lead} | Enable lead time | 1/2 | — | t_{SPSCK} | — |
| 4 | t_{Lag} | Enable lag time | 1/2 | — | t_{SPSCK} | — |
| 5 | t_{WSPSCK} | Clock (SPSCK) high or low time | $t_{periph} - 30$ | $1024 \times t_{periph}$ | ns | — |
| 6 | t_{SU} | Data setup time (inputs) | 18 | — | ns | — |
| 7 | t_{HI} | Data hold time (inputs) | 0 | — | ns | — |
| 8 | t_v | Data valid (after SPSCK edge) | — | 15 | ns | — |
| 9 | t_{HO} | Data hold time (outputs) | 0 | — | ns | — |
| 10 | t_{RI} | Rise time input | — | $t_{periph} - 25$ | ns | — |
| | t_{FI} | Fall time input | | | | |
| 11 | t_{RO} | Rise time output | — | 25 | ns | — |
| | t_{FO} | Fall time output | | | | |

1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).
2. $t_{periph} = 1/f_{periph}$

Table 37. SPI master mode timing on slew rate enabled pads

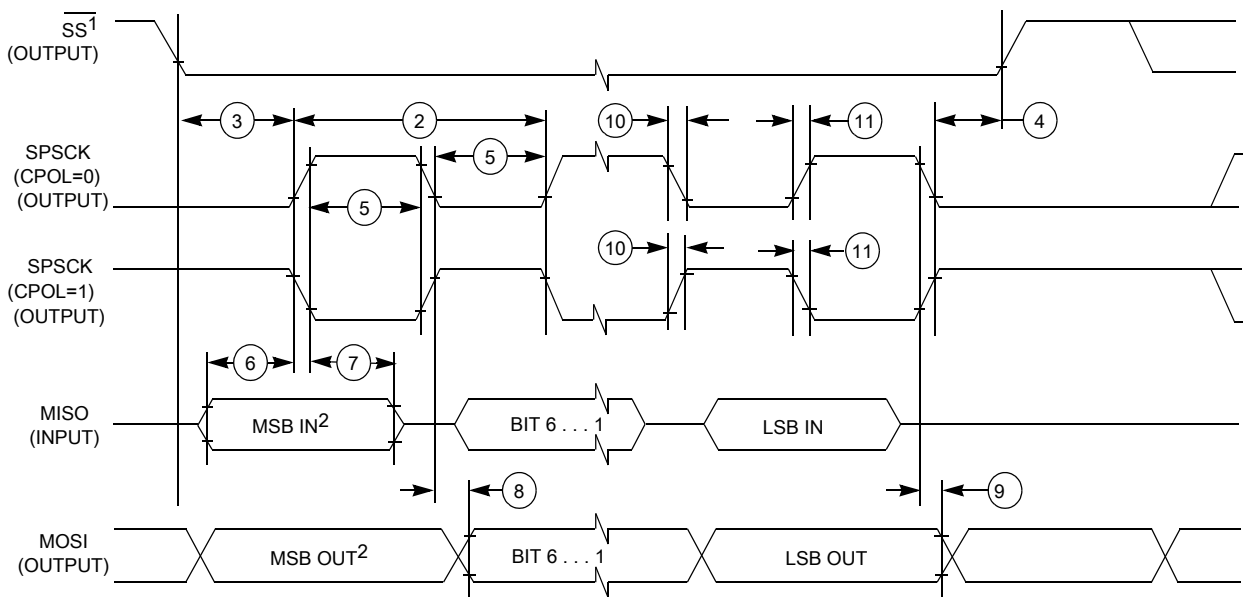
| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|------|--------------|--------------------------------|-----------------------|--------------------------|-------------|------|
| 1 | f_{op} | Frequency of operation | $f_{periph}/2048$ | $f_{periph}/2$ | Hz | 1 |
| 2 | t_{SPSCK} | SPSCK period | $2 \times t_{periph}$ | $2048 \times t_{periph}$ | ns | 2 |
| 3 | t_{Lead} | Enable lead time | 1/2 | — | t_{SPSCK} | — |
| 4 | t_{Lag} | Enable lag time | 1/2 | — | t_{SPSCK} | — |
| 5 | t_{WSPSCK} | Clock (SPSCK) high or low time | $t_{periph} - 30$ | $1024 \times t_{periph}$ | ns | — |
| 6 | t_{SU} | Data setup time (inputs) | 96 | — | ns | — |
| 7 | t_{HI} | Data hold time (inputs) | 0 | — | ns | — |

Table continues on the next page...

Table 37. SPI master mode timing on slew rate enabled pads (continued)

| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|------|----------|--------------------------------|------|-------------------|------|------|
| 8 | t_v | Data valid (after SPSCCK edge) | — | 52 | ns | — |
| 9 | t_{HO} | Data hold time (outputs) | 0 | — | ns | — |
| 10 | t_{RI} | Rise time input | — | $t_{periph} - 25$ | ns | — |
| | t_{FI} | Fall time input | | | | |
| 11 | t_{RO} | Rise time output | — | 36 | ns | — |
| | t_{FO} | Fall time output | | | | |

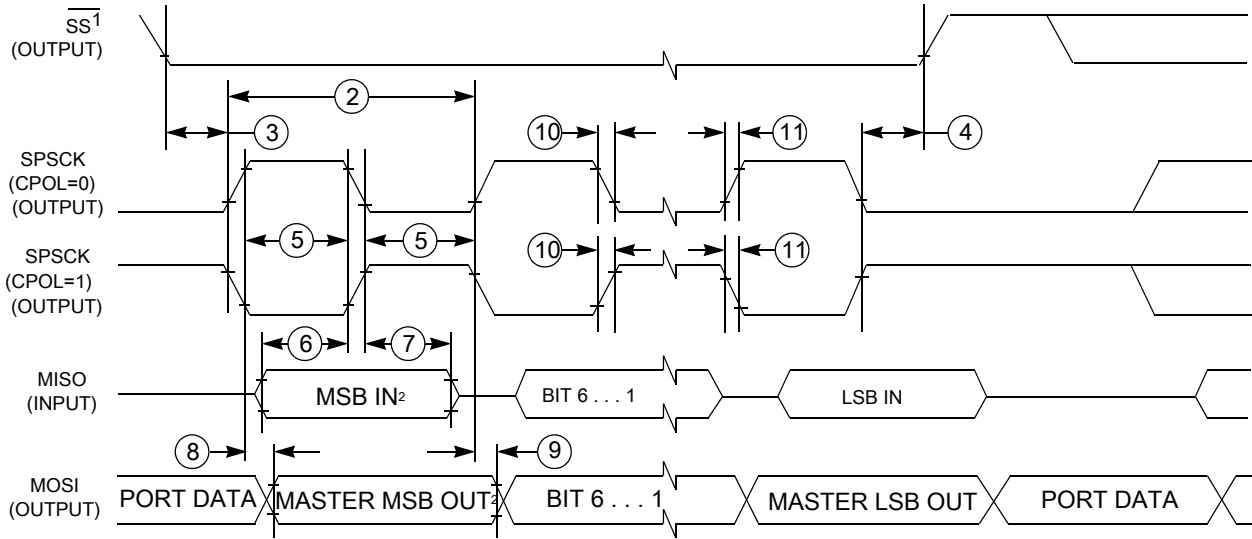
- For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).
- $t_{periph} = 1/f_{periph}$



- If configured as an output.
- LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 14. SPI master mode timing (CPHA = 0)

Peripheral operating requirements and behaviors



- 1. If configured as output
- 2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 15. SPI master mode timing (CPHA = 1)

Table 38. SPI slave mode timing on slew rate disabled pads

| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|------|--------------|--------------------------------|-----------------------|-------------------|--------------|------|
| 1 | f_{op} | Frequency of operation | 0 | $f_{periph}/4$ | Hz | 1 |
| 2 | t_{SPSCK} | SPSCK period | $4 \times t_{periph}$ | — | ns | 2 |
| 3 | t_{Lead} | Enable lead time | 1 | — | t_{periph} | — |
| 4 | t_{Lag} | Enable lag time | 1 | — | t_{periph} | — |
| 5 | t_{WSPSCK} | Clock (SPSCK) high or low time | $t_{periph} - 30$ | — | ns | — |
| 6 | t_{SU} | Data setup time (inputs) | 2.5 | — | ns | — |
| 7 | t_{HI} | Data hold time (inputs) | 3.5 | — | ns | — |
| 8 | t_a | Slave access time | — | t_{periph} | ns | 3 |
| 9 | t_{dis} | Slave MISO disable time | — | t_{periph} | ns | 4 |
| 10 | t_v | Data valid (after SPSCK edge) | — | 31 | ns | — |
| 11 | t_{HO} | Data hold time (outputs) | 0 | — | ns | — |
| 12 | t_{RI} | Rise time input | — | $t_{periph} - 25$ | ns | — |
| | t_{FI} | Fall time input | — | | | |
| 13 | t_{RO} | Rise time output | — | 25 | ns | — |
| | t_{FO} | Fall time output | — | | | |

- 1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).
- 2. $t_{periph} = 1/f_{periph}$
- 3. Time to data active from high-impedance state
- 4. Hold time to high-impedance state

Table 39. SPI slave mode timing on slew rate enabled pads

| Num. | Symbol | Description | Min. | Max. | Unit | Note |
|------|--------------|--------------------------------|-----------------------|-------------------|--------------|------|
| 1 | f_{op} | Frequency of operation | 0 | $f_{periph}/4$ | Hz | 1 |
| 2 | t_{SPSCK} | SPSCK period | $4 \times t_{periph}$ | — | ns | 2 |
| 3 | t_{Lead} | Enable lead time | 1 | — | t_{periph} | — |
| 4 | t_{Lag} | Enable lag time | 1 | — | t_{periph} | — |
| 5 | t_{WSPSCK} | Clock (SPSCK) high or low time | $t_{periph} - 30$ | — | ns | — |
| 6 | t_{SU} | Data setup time (inputs) | 2 | — | ns | — |
| 7 | t_{HI} | Data hold time (inputs) | 7 | — | ns | — |
| 8 | t_a | Slave access time | — | t_{periph} | ns | 3 |
| 9 | t_{dis} | Slave MISO disable time | — | t_{periph} | ns | 4 |
| 10 | t_v | Data valid (after SPSCK edge) | — | 122 | ns | — |
| 11 | t_{HO} | Data hold time (outputs) | 0 | — | ns | — |
| 12 | t_{RI} | Rise time input | — | $t_{periph} - 25$ | ns | — |
| | t_{FI} | Fall time input | | | | |
| 13 | t_{RO} | Rise time output | — | 36 | ns | — |
| | t_{FO} | Fall time output | | | | |

1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

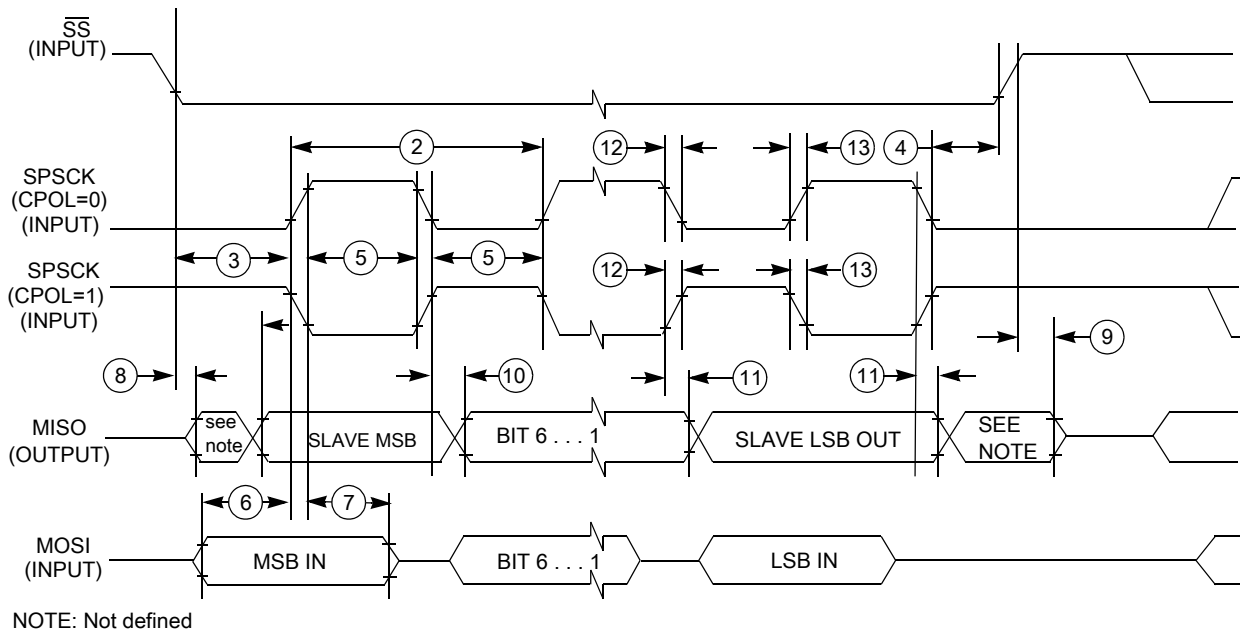


Figure 16. SPI slave mode timing (CPHA = 0)

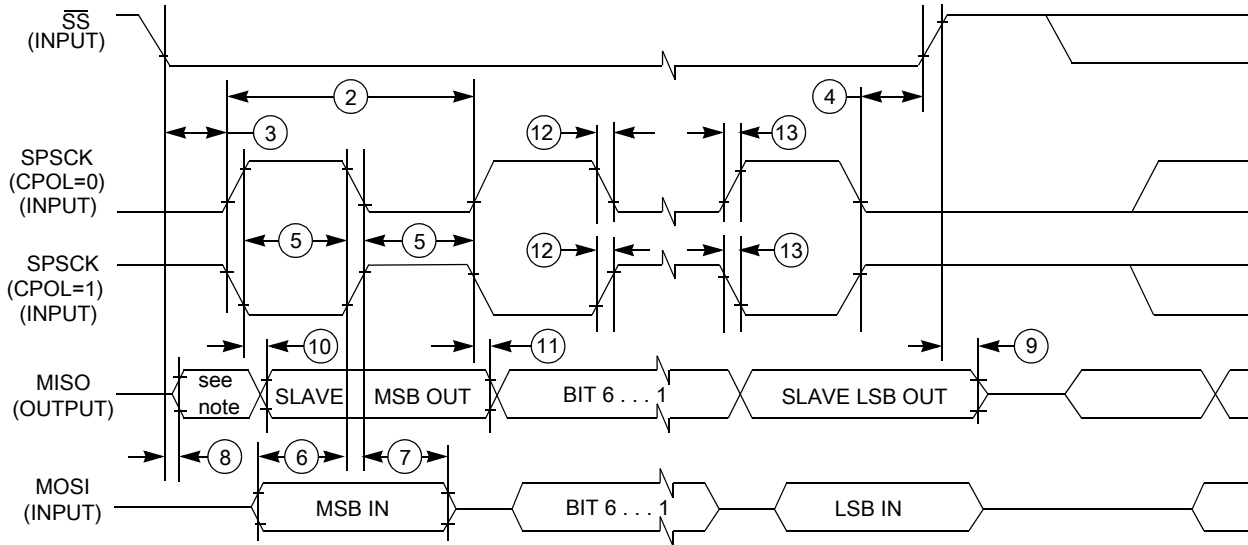


Figure 17. SPI slave mode timing (CPHA = 1)

3.8.4 I²C

3.8.4.1 Inter-Integrated Circuit Interface (I²C) timing

Table 40. I²C timing

| Characteristic | Symbol | Standard Mode | | Fast Mode | | Unit |
|--|-----------------------|------------------|-------------------|-------------------------------------|------------------|------|
| | | Minimum | Maximum | Minimum | Maximum | |
| SCL Clock Frequency | f _{SCL} | 0 | 100 | 0 | 400 ¹ | kHz |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated. | t _{HD} ; STA | 4 | — | 0.6 | — | μs |
| LOW period of the SCL clock | t _{LOW} | 4.7 | — | 1.25 | — | μs |
| HIGH period of the SCL clock | t _{HIGH} | 4 | — | 0.6 | — | μs |
| Set-up time for a repeated START condition | t _{SU} ; STA | 4.7 | — | 0.6 | — | μs |
| Data hold time for I ² C bus devices | t _{HD} ; DAT | 0 ² | 3.45 ³ | 0 ⁴ | 0.9 ² | μs |
| Data set-up time | t _{SU} ; DAT | 250 ⁵ | — | 100 ^{3, 6} | — | ns |
| Rise time of SDA and SCL signals | t _r | — | 1000 | 20 + 0.1C _b ⁷ | 300 | ns |
| Fall time of SDA and SCL signals | t _f | — | 300 | 20 + 0.1C _b ⁶ | 300 | ns |
| Set-up time for STOP condition | t _{SU} ; STO | 4 | — | 0.6 | — | μs |
| Bus free time between STOP and START condition | t _{BUF} | 4.7 | — | 1.3 | — | μs |
| Pulse width of spikes that must be suppressed by the input filter | t _{SP} | N/A | N/A | 0 | 50 | ns |

1. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can be achieved only when using the high drive pins across the full voltage range and when using the normal drive pins and $VDD \geq 2.7 V$.
2. The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
3. The maximum t_{HD; DAT} must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
4. Input signal Slew = 10 ns and Output Load = 50 pF
5. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
6. A Fast mode I²C bus device can be used in a Standard mode I²C bus system, but the requirement t_{SU; DAT} ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line t_{rmax} + t_{SU; DAT} = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification) before the SCL line is released.
7. C_b = total capacitance of the one bus line in pF.

To achieve 1MHz I2C clock rates, consider the following recommendations:

- To counter the effects of clock stretching, the I2C baud Rate select bits can be configured for faster than desired baud rate.
- Use high drive pad and DSE bit should be set in PORTx_PCRn register.
- Minimize loading on the I2C SDA and SCL pins to ensure fastest rise times for the SCL line to avoid clock stretching.
- Use smaller pull up resistors on SDA and SCL to reduce the RC time constant.

Table 41. I²C 1Mbit/s timing

| Characteristic | Symbol | Minimum | Maximum | Unit |
|--|----------------------|-------------------------------------|----------------|------|
| SCL Clock Frequency | f _{SCL} | 0 | 1 ¹ | MHz |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated. | t _{HD; STA} | 0.26 | — | μs |
| LOW period of the SCL clock | t _{LOW} | 0.5 | — | μs |
| HIGH period of the SCL clock | t _{HIGH} | 0.26 | — | μs |
| Set-up time for a repeated START condition | t _{SU; STA} | 0.26 | — | μs |
| Data hold time for I ₂ C bus devices | t _{HD; DAT} | 0 | — | μs |
| Data set-up time | t _{SU; DAT} | 50 | — | ns |
| Rise time of SDA and SCL signals | t _r | 20 + 0.1C _b | 120 | ns |
| Fall time of SDA and SCL signals | t _f | 20 + 0.1C _b ² | 120 | ns |
| Set-up time for STOP condition | t _{SU; STO} | 0.26 | — | μs |
| Bus free time between STOP and START condition | t _{BUF} | 0.5 | — | μs |
| Pulse width of spikes that must be suppressed by the input filter | t _{SP} | 0 | 50 | ns |

1. The maximum SCL clock frequency of 1 Mbit/s can support maximum bus loading when using the high drive pins across the full voltage range.
2. C_b = total capacitance of the one bus line in pF.

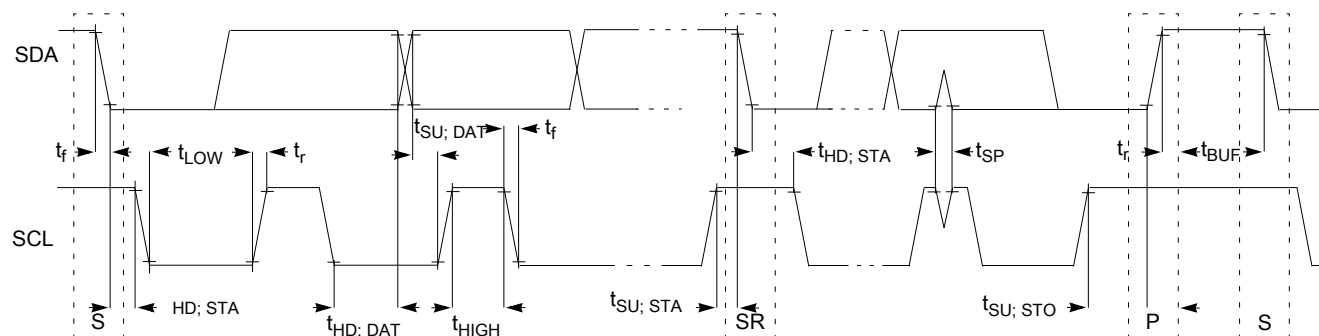


Figure 18. Timing definition for devices on the I²C bus

3.8.5 UART

See [General switching specifications](#).

3.8.6 I2S/SAI switching specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP] is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

3.8.6.1 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

Table 42. I2S/SAI master mode timing

| Num. | Characteristic | Min. | Max. | Unit |
|------|---|------|------|-------------|
| | Operating voltage | 1.71 | 3.6 | V |
| S1 | I2S_MCLK cycle time | 40 | — | ns |
| S2 | I2S_MCLK (as an input) pulse width high/low | 45% | 55% | MCLK period |
| S3 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (output) | 80 | — | ns |
| S4 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low | 45% | 55% | BCLK period |
| S5 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid | — | 15.5 | ns |

Table continues on the next page...

Table 42. I2S/SAI master mode timing (continued)

| Num. | Characteristic | Min. | Max. | Unit |
|------|---|------|------|------|
| S6 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid | 0 | — | ns |
| S7 | I2S_TX_BCLK to I2S_TXD valid | — | 19 | ns |
| S8 | I2S_TX_BCLK to I2S_TXD invalid | 0 | — | ns |
| S9 | I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK | 26 | — | ns |
| S10 | I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK | 0 | — | ns |

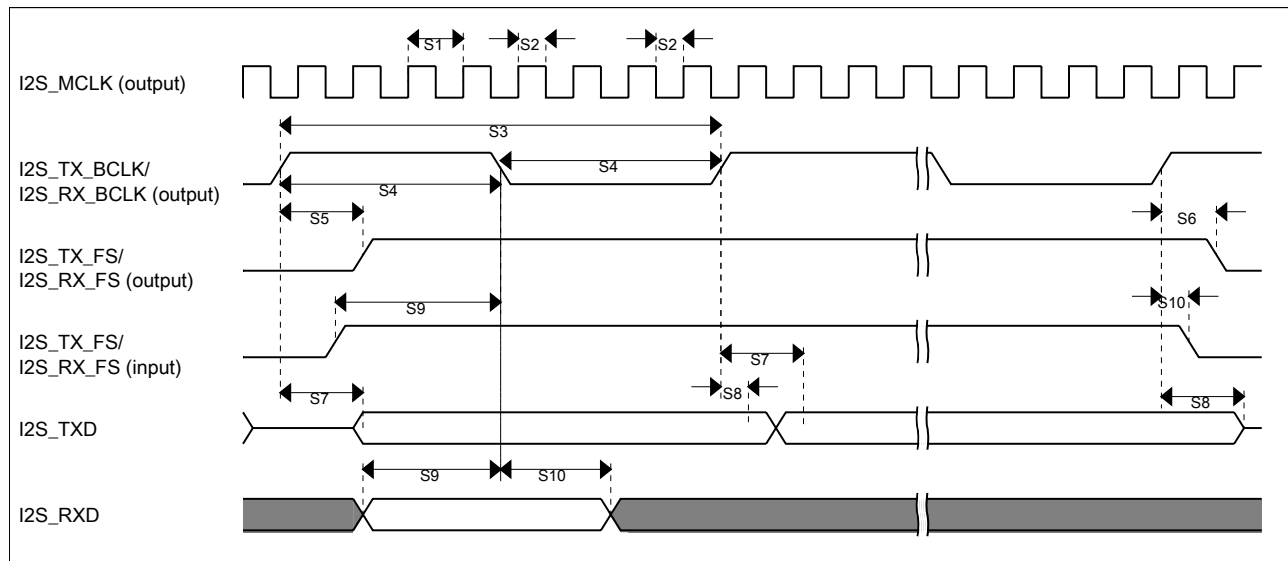


Figure 19. I2S/SAI timing — master modes

Table 43. I2S/SAI slave mode timing

| Num. | Characteristic | Min. | Max. | Unit |
|------|---|------|------|-------------|
| | Operating voltage | 1.71 | 3.6 | V |
| S11 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (input) | 80 | — | ns |
| S12 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input) | 45% | 55% | MCLK period |
| S13 | I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK | 10 | — | ns |
| S14 | I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK | 2 | — | ns |
| S15 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid | — | 33 | ns |
| S16 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid | 0 | — | ns |
| S17 | I2S_RXD setup before I2S_RX_BCLK | 10 | — | ns |

Table continues on the next page...

Table 43. I2S/SAI slave mode timing (continued)

| Num. | Characteristic | Min. | Max. | Unit |
|------|--|------|------|------|
| S18 | I2S_RXD hold after I2S_RX_BCLK | 2 | — | ns |
| S19 | I2S_TX_FS input assertion to I2S_TXD output valid ¹ | — | 28 | ns |

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

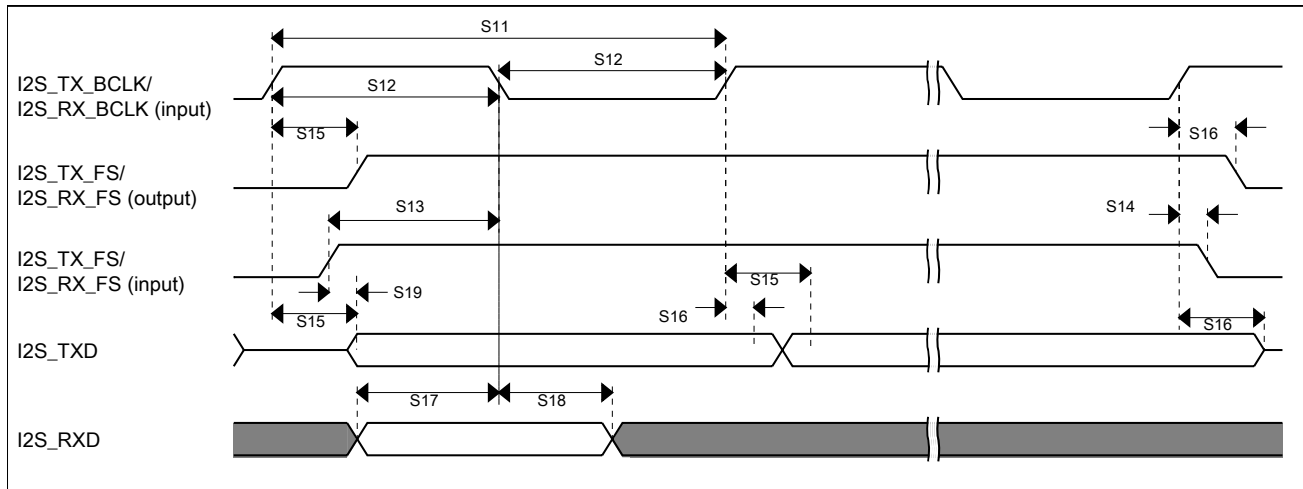


Figure 20. I2S/SAI timing — slave modes

3.8.6.2 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

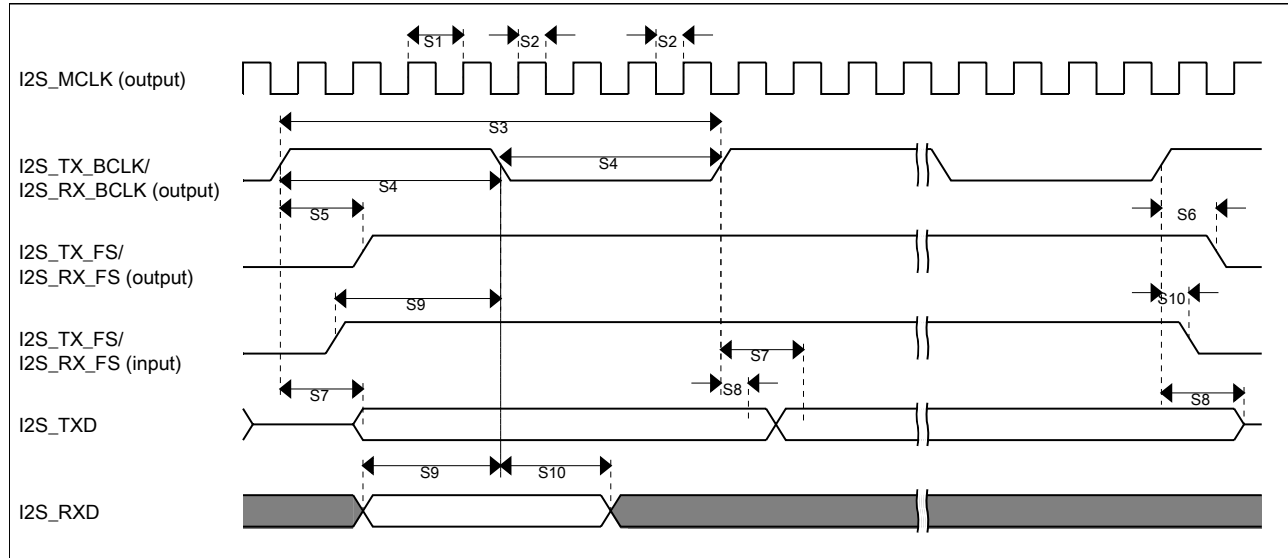
Table 44. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

| Num. | Characteristic | Min. | Max. | Unit |
|------|---|------|------|-------------|
| | Operating voltage | 1.71 | 3.6 | V |
| S1 | I2S_MCLK cycle time | 62.5 | — | ns |
| S2 | I2S_MCLK pulse width high/low | 45% | 55% | MCLK period |
| S3 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (output) | 250 | — | ns |
| S4 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low | 45% | 55% | BCLK period |
| S5 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid | — | 45 | ns |
| S6 | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid | 0 | — | ns |
| S7 | I2S_TX_BCLK to I2S_TXD valid | — | 45 | ns |

Table continues on the next page...

Table 44. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range) (continued)

| Num. | Characteristic | Min. | Max. | Unit |
|------|--|------|------|------|
| S8 | I2S_TX_BCLK to I2S_TXD invalid | 0 | — | ns |
| S9 | I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK | | — | ns |
| S10 | I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK | 0 | — | ns |


Figure 21. I2S/SAI timing — master modes
Table 45. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

| Num. | Characteristic | Min. | Max. | Unit |
|------|--|------|------|-------------|
| | Operating voltage | 1.71 | 3.6 | V |
| S11 | I2S_TX_BCLK/I2S_RX_BCLK cycle time (input) | 250 | — | ns |
| S12 | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input) | 45% | 55% | MCLK period |
| S13 | I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK | 30 | — | ns |
| S14 | I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK | 2 | — | ns |
| S15 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid | — | 87 | ns |
| S16 | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid | 0 | — | ns |
| S17 | I2S_RXD setup before I2S_RX_BCLK | 30 | — | ns |
| S18 | I2S_RXD hold after I2S_RX_BCLK | 2 | — | ns |
| S19 | I2S_TX_FS input assertion to I2S_TXD output valid ¹ | — | 72 | ns |

Dimensions

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

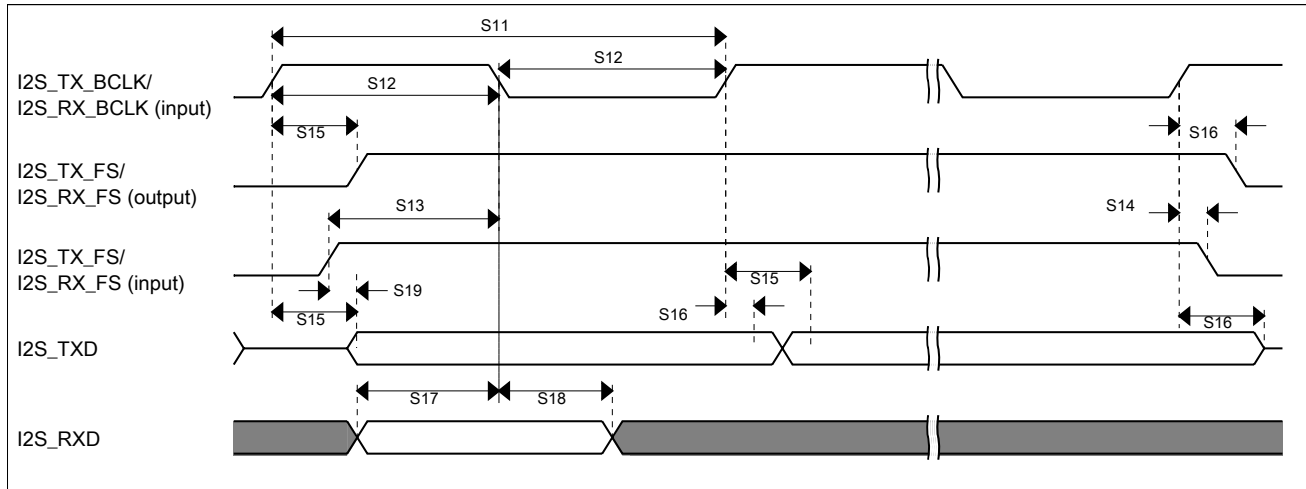


Figure 22. I2S/SAI timing — slave modes

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

| If you want the drawing for this package | Then use this document number |
|--|-------------------------------|
| 32-pin QFN | 98ASA00615D |
| 48-pin QFN | 98ASA00616D |
| 64-pin LQFP | 98ASS23234W |
| 64-pin MAPBGA | 98ASA00420D |

5 Pinouts and Packaging

5.1 KL27 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

VREFH can act as VREF_OUT when VREFV1 module is enabled.

NOTE

It is prohibited to set VREFEN in 32 QFN pin package as 1.2 V on-chip voltage is not available in this package.

| 32 QFN | 48 QFN | 64 MAP BGA | 64 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|--------|--------|------------|---------|----------|------------------------|------------------------|-------|-----------|------------|------------|-----------|--------------|------|
| — | — | B1 | 2 | PTE1 | DISABLED | | PTE1 | SPI1_MOSI | LPUART1_RX | | SPI1_MISO | I2C1_SCL | |
| — | 1 | — | 3 | VDD | VDD | VDD | | | | | | | |
| — | 7 | G1 | 9 | PTE20 | ADC0_DP0/ ADC0_SE0 | ADC0_DP0/ ADC0_SE0 | PTE20 | | TPM1_CH0 | LPUART0_TX | | FXIO0_D4 | |
| — | 8 | F1 | 10 | PTE21 | ADC0_DM0/ ADC0_SE4a | ADC0_DM0/ ADC0_SE4a | PTE21 | | TPM1_CH1 | LPUART0_RX | | FXIO0_D5 | |
| — | — | G2 | 11 | PTE22 | ADC0_DP3/ ADC0_SE3 | ADC0_DP3/ ADC0_SE3 | PTE22 | | TPM2_CH0 | UART2_TX | | FXIO0_D6 | |
| — | — | F2 | 12 | PTE23 | ADC0_DM3/ ADC0_SE7a | ADC0_DM3/ ADC0_SE7a | PTE23 | | TPM2_CH1 | UART2_RX | | FXIO0_D7 | |
| — | 10 | G4 | 14 | VREFH | VREFH | VREFH | | | | | | | |
| — | 11 | G3 | 15 | VREFL | VREFL | VREFL | | | | | | | |
| — | 13 | H1 | 17 | PTE29 | CMP0_IN5/ ADC0_SE4b | CMP0_IN5/ ADC0_SE4b | PTE29 | | TPM0_CH2 | TPM_CLKIN0 | | | |
| — | — | H3 | 19 | PTE31 | DISABLED | | PTE31 | | TPM0_CH4 | | | | |
| — | 15 | H4 | 20 | PTE24 | DISABLED | | PTE24 | | TPM0_CH0 | | I2C0_SCL | | |
| — | 16 | H5 | 21 | PTE25 | DISABLED | | PTE25 | | TPM0_CH1 | | I2C0_SDA | | |
| — | — | F5 | 27 | PTA5 | DISABLED | | PTA5 | USB_CLKIN | TPM0_CH2 | | | I2S0_TX_BCLK | |
| — | — | H6 | 28 | PTA12 | DISABLED | | PTA12 | | TPM1_CH0 | | | I2S0_TXD0 | |
| — | — | G6 | 29 | PTA13 | DISABLED | | PTA13 | | TPM1_CH1 | | | I2S0_TX_FS | |
| — | 29 | E7 | 37 | PTB2 | ADC0_SE12 | ADC0_SE12 | PTB2 | I2C0_SCL | TPM2_CH0 | | | | |
| — | 30 | E8 | 38 | PTB3 | ADC0_SE13 | ADC0_SE13 | PTB3 | I2C0_SDA | TPM2_CH1 | | | | |

Pinouts and Packaging

| 32 QFN | 48 QFN | 64 MAP BGA | 64 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|--------|--------|------------|---------|----------|-------------------------------------|-------------------------------------|----------------|------------|------------|------------------|------------|-------------|---------|
| — | 31 | E6 | 39 | PTB16 | DISABLED | | PTB16 | SPI1_MOSI | LPUART0_RX | TPM_CLKIN0 | SPI1_MISO | | |
| — | 32 | D7 | 40 | PTB17 | DISABLED | | PTB17 | SPI1_MISO | LPUART0_TX | TPM_CLKIN1 | SPI1_MOSI | | |
| — | — | D6 | 41 | PTB18 | DISABLED | | PTB18 | | TPM2_CH0 | I2S0_TX_BCLK | | | |
| — | — | C7 | 42 | PTB19 | DISABLED | | PTB19 | | TPM2_CH1 | I2S0_TX_FS | | | |
| — | 33 | D8 | 43 | PTC0 | ADC0_SE14 | ADC0_SE14 | PTC0 | | EXTRG_IN | audioUSB_SOF_OUT | CMP0_OUT | I2S0_TXD0 | |
| — | — | E3 | 47 | VSS | VSS | VSS | | | | | | | |
| — | — | E4 | 48 | VDD | VDD | VDD | | | | | | | |
| — | — | A6 | 53 | PTC8 | CMP0_IN2 | CMP0_IN2 | PTC8 | I2C0_SCL | TPM0_CH4 | I2S0_MCLK | | | |
| — | — | B5 | 54 | PTC9 | CMP0_IN3 | CMP0_IN3 | PTC9 | I2C0_SDA | TPM0_CH5 | I2S0_RX_BCLK | | | |
| — | — | B4 | 55 | PTC10 | DISABLED | | PTC10 | I2C1_SCL | | I2S0_RX_FS | | | |
| — | — | A5 | 56 | PTC11 | DISABLED | | PTC11 | I2C1_SDA | | I2S0_RXD0 | | | |
| — | 41 | C3 | 57 | PTD0 | DISABLED | | PTD0 | SPI0_SS | | TPM0_CH0 | | FXIO0_D0 | |
| — | 42 | A4 | 58 | PTD1 | ADC0_SE5b | ADC0_SE5b | PTD1 | SPI0_SCK | | TPM0_CH1 | | FXIO0_D1 | |
| — | 43 | C2 | 59 | PTD2 | DISABLED | | PTD2 | SPI0_MOSI | UART2_RX | TPM0_CH2 | SPI0_MISO | FXIO0_D2 | |
| — | 44 | B3 | 60 | PTD3 | DISABLED | | PTD3 | SPI0_MISO | UART2_TX | TPM0_CH3 | SPI0_MOSI | FXIO0_D3 | |
| — | — | C5 | — | NC | NC | NC | | | | | | | |
| 1 | — | A1 | 1 | PTE0 | DISABLED | | PTE0/CLKOUT32K | SPI1_MISO | LPUART1_TX | RTC_CLKOUT | CMP0_OUT | I2C1_SDA | |
| 2 | 2 | C4 | 4 | VSS | VSS | VSS | | | | | | | |
| 3 | 3 | E1 | 5 | USB0_DP | USB0_DP | USB0_DP | | | | | | | |
| 4 | 4 | D1 | 6 | USB0_DM | USB0_DM | USB0_DM | | | | | | | |
| 5 | 5 | E2 | 7 | VOUT33 | VOUT33 | VOUT33 | | | | | | | |
| 6 | 6 | D2 | 8 | VREGIN | VREGIN | VREGIN | | | | | | | |
| 7 | 9 | F4 | 13 | VDDA | VDDA | VDDA | | | | | | | |
| 8 | 12 | F3 | 16 | VSSA | VSSA | VSSA | | | | | | | |
| 9 | 14 | H2 | 18 | PTE30 | DAC0_OUT/ ADC0_SE23/ CMP0_IN4 | DAC0_OUT/ ADC0_SE23/ CMP0_IN4 | PTE30 | | TPM0_CH3 | TPM_CLKIN1 | LPUART1_TX | LPTMR0_ALT1 | |
| 10 | 17 | D3 | 22 | PTA0 | SWD_CLK | | PTA0 | | TPM0_CH5 | | | | SWD_CLK |
| 11 | 18 | D4 | 23 | PTA1 | DISABLED | | PTA1 | LPUART0_RX | TPM2_CH0 | | | | |
| 12 | 19 | E5 | 24 | PTA2 | DISABLED | | PTA2 | LPUART0_TX | TPM2_CH1 | | | | |
| 13 | 20 | D5 | 25 | PTA3 | SWD_DIO | | PTA3 | I2C1_SCL | TPM0_CH0 | | | | SWD_DIO |
| 14 | 21 | G5 | 26 | PTA4 | NMI_b | | PTA4 | I2C1_SDA | TPM0_CH1 | | | | NMI_b |
| 15 | 22 | G7 | 30 | VDD | VDD | VDD | | | | | | | |
| 16 | 23 | H7 | 31 | VSS | VSS | VSS | | | | | | | |

| 32 QFN | 48 QFN | 64 MAP BGA | 64 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|--------|--------|------------|---------|------------------------|-----------|-----------|------------------------|-----------|------------------|--------------|-----------|--------------|---------|
| 17 | 24 | H8 | 32 | PTA18 | EXTAL0 | EXTAL0 | PTA18 | | LPUART1_RX | TPM_CLKIN0 | | | |
| 18 | 25 | G8 | 33 | PTA19 | XTAL0 | XTAL0 | PTA19 | | LPUART1_TX | TPM_CLKIN1 | | LPTMR0_ALT1 | |
| 19 | 26 | F8 | 34 | PTA20 | RESET_b | | PTA20 | | | | | | RESET_b |
| 20 | 27 | F7 | 35 | PTB0/LLWU_P5 | ADC0_SE8 | ADC0_SE8 | PTB0/LLWU_P5 | I2C0_SCL | TPM1_CH0 | | | | |
| 21 | 28 | F6 | 36 | PTB1 | ADC0_SE9 | ADC0_SE9 | PTB1 | I2C0_SDA | TPM1_CH1 | | | | |
| 22 | 34 | C6 | 44 | PTC1/LLWU_P6/RTC_CLKIN | ADC0_SE15 | ADC0_SE15 | PTC1/LLWU_P6/RTC_CLKIN | I2C1_SCL | | TPM0_CH0 | | I2S0_TXD0 | |
| 23 | 35 | B7 | 45 | PTC2 | ADC0_SE11 | ADC0_SE11 | PTC2 | I2C1_SDA | | TPM0_CH1 | | I2S0_TX_FS | |
| 24 | 36 | C8 | 46 | PTC3/LLWU_P7 | DISABLED | | PTC3/LLWU_P7 | SPI1_SCK | LPUART1_RX | TPM0_CH2 | CLKOUT | I2S0_TX_BCLK | |
| 25 | 37 | B8 | 49 | PTC4/LLWU_P8 | DISABLED | | PTC4/LLWU_P8 | SPI0_SS | LPUART1_TX | TPM0_CH3 | I2S0_MCLK | | |
| 26 | 38 | A8 | 50 | PTC5/LLWU_P9 | DISABLED | | PTC5/LLWU_P9 | SPI0_SCK | LPTMR0_ALT2 | I2S0_RXD0 | | CMP0_OUT | |
| 27 | 39 | A7 | 51 | PTC6/LLWU_P10 | CMP0_IN0 | CMP0_IN0 | PTC6/LLWU_P10 | SPI0_MOSI | EXTRG_IN | I2S0_RX_BCLK | SPI0_MISO | I2S0_MCLK | |
| 28 | 40 | B6 | 52 | PTC7 | CMP0_IN1 | CMP0_IN1 | PTC7 | SPI0_MISO | audioUSB_SOF_OUT | I2S0_RX_FS | SPI0_MOSI | | |
| 29 | 45 | A3 | 61 | PTD4/LLWU_P14 | DISABLED | | PTD4/LLWU_P14 | SPI1_SS | UART2_RX | TPM0_CH4 | | FXIO0_D4 | |
| 30 | 46 | C1 | 62 | PTD5 | ADC0_SE6b | ADC0_SE6b | PTD5 | SPI1_SCK | UART2_TX | TPM0_CH5 | | FXIO0_D5 | |
| 31 | 47 | B2 | 63 | PTD6/LLWU_P15 | ADC0_SE7b | ADC0_SE7b | PTD6/LLWU_P15 | SPI1_MOSI | LPUART0_RX | | SPI1_MISO | FXIO0_D6 | |
| 32 | 48 | A2 | 64 | PTD7 | DISABLED | | PTD7 | SPI1_MISO | LPUART0_TX | | SPI1_MOSI | FXIO0_D7 | |

5.2 KL27 Family Pinouts

Figure below shows the 32 QFN pinouts:

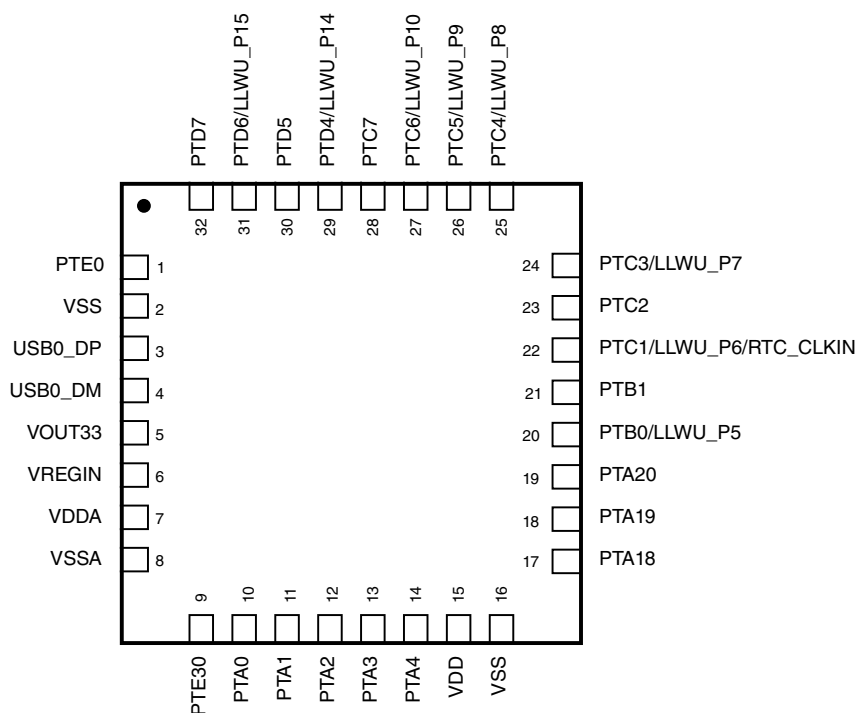


Figure 23. 32 QFN Pinout diagram

Figure below shows the 48 QFN pinouts:

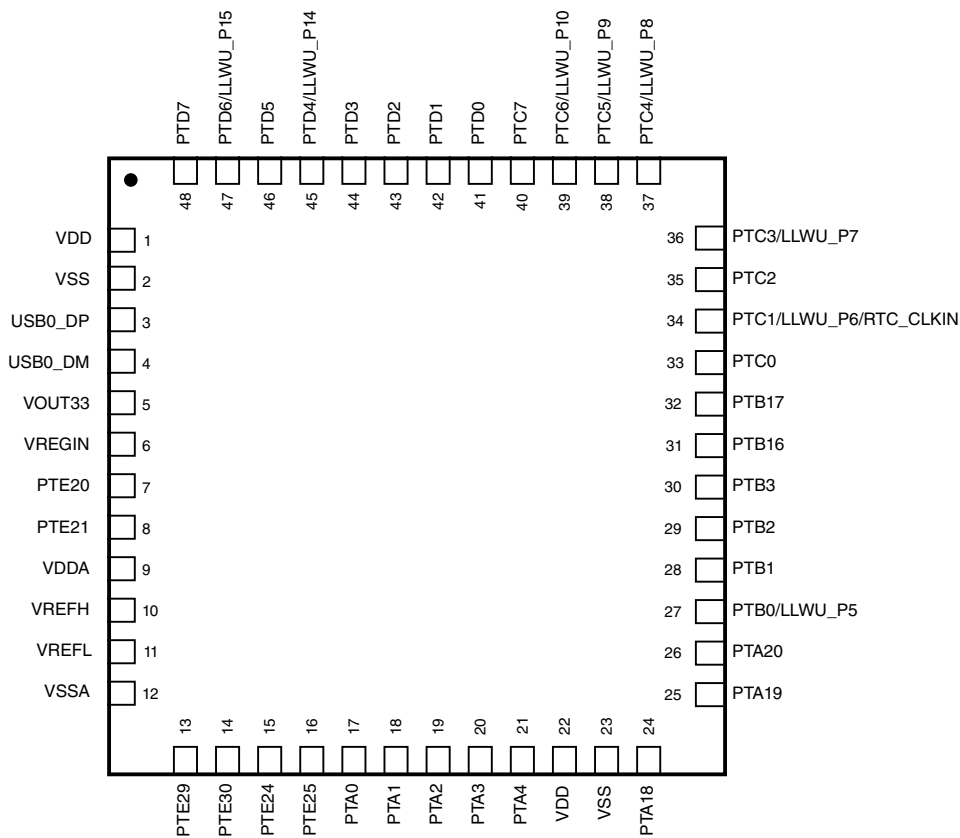


Figure 24. 48 QFN Pinout diagram

Figure below shows the 64 LQFP pinouts:

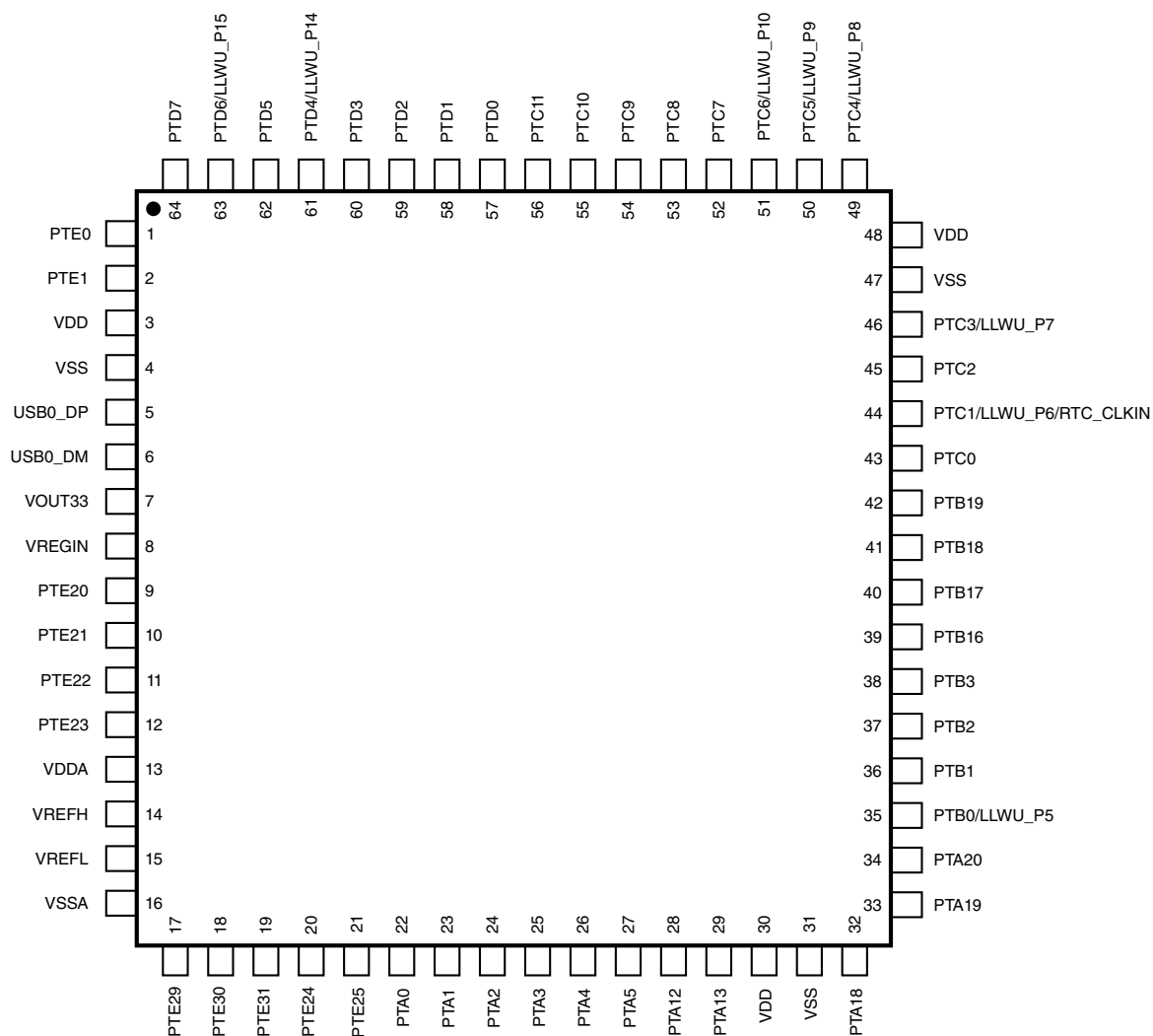


Figure 25. 64 LQFP Pinout diagram

Figure below shows the 64 MAPBGA pinouts:

| | | | | | | | | | |
|---|---------|-------------------|-------------------|-------|-------|--------------------------------|-------------------|------------------|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | |
| A | PTE0 | PTD7 | PTD4/ LLWU_P14 | PTD1 | PTC11 | PTC8 | PTC6/ LLWU_P10 | PTC5/ LLWU_P9 | A |
| B | PTE1 | PTD6/ LLWU_P15 | PTD3 | PTC10 | PTC9 | PTC7 | PTC2 | PTC4/ LLWU_P8 | B |
| C | PTD5 | PTD2 | PTD0 | VSS | NC | PTC1/ LLWU_P6/ RTC_CLKIN | PTB19 | PTC3/ LLWU_P7 | C |
| D | USB0_DM | VREGIN | PTA0 | PTA1 | PTA3 | PTB18 | PTB17 | PTC0 | D |
| E | USB0_DP | VOOUT33 | VSS | VDD | PTA2 | PTB16 | PTB2 | PTB3 | E |
| F | PTE21 | PTE23 | VSSA | VDDA | PTA5 | PTB1 | PTB0/ LLWU_P5 | PTA20 | F |
| G | PTE20 | PTE22 | VREFL | VREFH | PTA4 | PTA13 | VDD | PTA19 | G |
| H | PTE29 | PTE30 | PTE31 | PTE24 | PTE25 | PTA12 | VSS | PTA18 | H |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | |

Figure 26. 64 MAPBGA Pinout diagram

6 Ordering parts

6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the Web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers:

7 Part identification

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

Q KL## A FFF R T PP CC N

7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Table 46. Part number fields descriptions

| Field | Description | Values |
|-------|-----------------------------|--|
| Q | Qualification status | <ul style="list-style-type: none"> M = Fully qualified, general market flow P = Prequalification |
| KL## | Kinetis family | <ul style="list-style-type: none"> KL27 |
| A | Key attribute | <ul style="list-style-type: none"> Z = Cortex-M0+ |
| FFF | Program flash memory size | |
| R | Silicon revision | <ul style="list-style-type: none"> (Blank) = Main A = Revision after main |
| T | Temperature range (°C) | <ul style="list-style-type: none"> V = -40 to 105 |
| PP | Package identifier | <ul style="list-style-type: none"> FM = 32 QFN (5 mm x 5 mm) FT = 48 QFN (7 mm x 7 mm) LH = 64 LQFP (10 mm x 10 mm) MP = 64 MAPBGA (5 mm x 5 mm) |
| CC | Maximum CPU frequency (MHz) | <ul style="list-style-type: none"> 4 = 48 MHz |
| N | Packaging type | <ul style="list-style-type: none"> R = Tape and reel |

7.4 Example

This is an example part number:

MKL27Z256VFT4

8 Terminology and guidelines

8.1 Definitions

Key terms are defined in the following table:

| Term | Definition |
|-----------------------|--|
| Rating | <p>A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:</p> <ul style="list-style-type: none"> • <i>Operating ratings</i> apply during operation of the chip. • <i>Handling ratings</i> apply when the chip is not powered. <p>NOTE: The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.</p> |
| Operating requirement | A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip |
| Operating behavior | A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions |
| Typical value | <p>A specified value for a technical characteristic that:</p> <ul style="list-style-type: none"> • Lies within the range of values specified by the operating behavior • Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions <p>NOTE: Typical values are provided as design guidelines and are neither tested nor guaranteed.</p> |

8.2 Examples

Operating rating:

| Symbol | Description | Min. | Max. | Unit |
|-----------------|---------------------------|------|------|------|
| V _{DD} | 1.0 V core supply voltage | -0.3 | 1.2 | V |

Operating requirement:

| Symbol | Description | Min. | Max. | Unit |
|-----------------|---------------------------|------|------|------|
| V _{DD} | 1.0 V core supply voltage | 0.9 | 1.1 | V |

Operating behavior that includes a typical value:

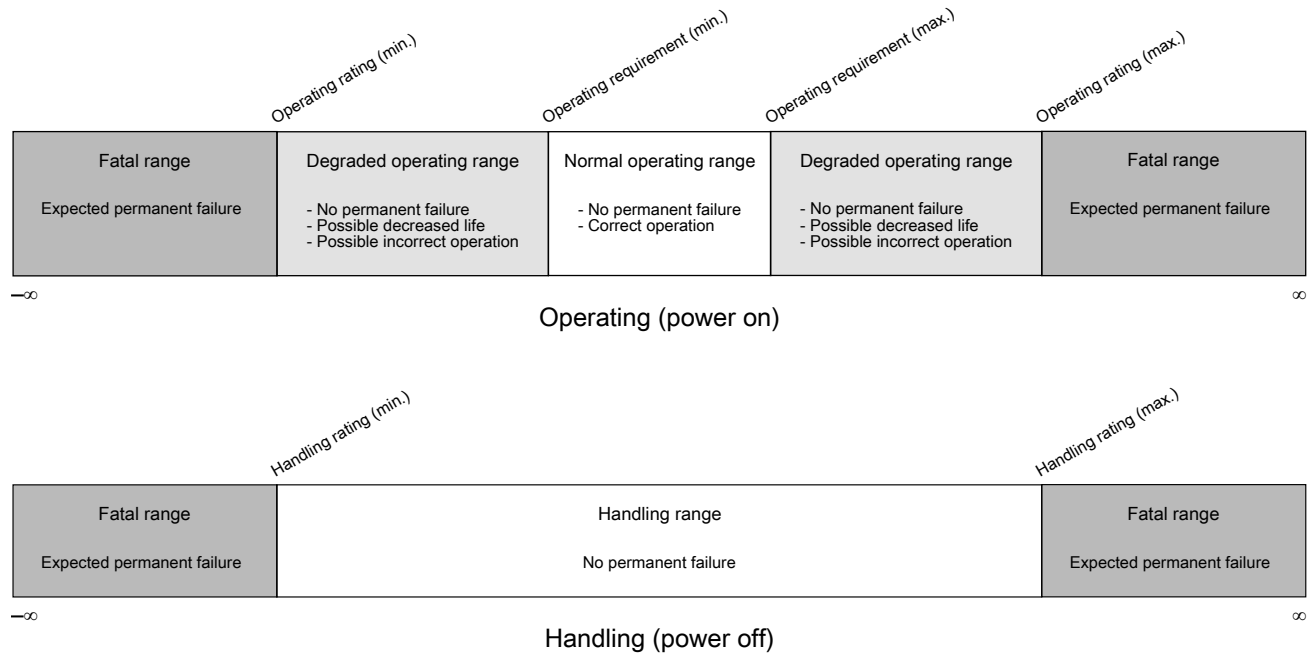
| Symbol | Description | Min. | Typ. | Max. | Unit |
|-----------------|--|------|------|------|------|
| I _{WP} | Digital I/O weak pullup/pulldown current | 10 | 70 | 130 | μA |

8.3 Typical-value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

| Symbol | Description | Value | Unit |
|-----------------|----------------------|-------|------|
| T _A | Ambient temperature | 25 | °C |
| V _{DD} | 3.3 V supply voltage | 3.3 | V |

8.4 Relationship between ratings and operating requirements



8.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip’s ratings.
- During normal operation, don’t exceed any of the chip’s operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

9 Revision History

The following table provides a revision history for this document.

Table 47. Revision History

| Rev. No. | Date | Substantial Changes |
|----------|----------------|---|
| 3 | 09 August 2014 | Initial Public release <ul style="list-style-type: none"> • Updated Table 9 - Power consumption operating behaviors. • Added a note related to 32 QFN pin package in Pinouts topic. |
| 4 | 03 March 2015 | <ul style="list-style-type: none"> • Updated the features and completed the ordering information. • Removed thickness dimension from package diagrams. |

Table continues on the next page...

Table 47. Revision History (continued)

| Rev. No. | Date | Substantial Changes |
|----------|----------------|---|
| | | <ul style="list-style-type: none"> • Updated Related Resources table to include Chip Errata resource name and Package Drawing part numbers in the respective rows. Also updated Product Brief resource references. • Updated Table 7. Voltage and current operating behaviors. <ul style="list-style-type: none"> • Specified correct max. value for I_{IN}. • Updated Table - 9 Power consumption operating behaviors. <ul style="list-style-type: none"> • Rows added for IDD for reset pin hold low ($I_{DD_RESET_LOW}$) at 1.7V and 3V. • Measurement unit updated for I_{DD_VLLS1} from nA to μA. • Footnote 1 was moved in the beginning of the table as text. • Added Table - 11 EMC radiated emissions operating behaviors for 64-pin LQFP package under section 2.2.6. • Updated Table - 18 (IRC48M specification) and Table - 19 (IRC8M/2M specification) under section 3.3.1 - 'MCG-Lite specifications'. <ul style="list-style-type: none"> • Removed supply voltage (V_{DD}), temperature range (T), untrimmed (f_{IRC_UT}), trim function (Δf_{IRC_C}, Δf_{IRC_F}) data from Table - 18 (IRC48M specification). • Removed supply voltage (V_{DD}), temperature range (T) data from Table - 19 (IRC8M/2M specification). • Added Figure 6. IRC8M Frequency Drift vs Temperature curve after Table - 19 (IRC8M/2M specification). • Updated Table 29. VREF full-range operating behaviors. <ul style="list-style-type: none"> • Removed A_c(Aging coefficient) row. • Added $T_{chop_osc_stup}$ parameter. • Added tables: "I2C timing" and "I2C 1Mbit/s timing" under section - I²C. • Added VREF specifications (V_{REFH} and V_{REFL}) to Table 26. 16-bit ADC operating conditions. • Removed note: "This device does not have the USB_CLKIN signal available." |
| 5 | 12 August 2015 | <ul style="list-style-type: none"> • In Table 9. Power consumption operating behaviors: <ul style="list-style-type: none"> • Updated Max. values of I_{DD_WAIT}, I_{DD_VLPW}, I_{DD_STOP}, I_{DD_VLPS}, I_{DD_LLS}, I_{DD_VLLS3}, I_{DD_VLLS1}, I_{DD_VLLS0}. • Modified unit of I_{DD_VLLS0} from nA to μA. • Removed $I_{DD_RESET_LOW}$ information. • In Table 13. Device clock specifications, added a footnote for normal run mode. • In Table 15. Thermal operating requirements, modified the footnote for Ambient temperature. • In Table 18. IRC48M specification, removed f_{IRC_T} data and added $\Delta f_{irc48m_of_lv}$ and $\Delta f_{irc48m_of_hv}$ specifications. • In Table 26. 16-bit ADC operating conditions, updated Max. value of f_{ADCK} and C_{rate}. |

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