THE DATASHEET OF

3003.0452

THAT Corporation

2-Channel Digital Preamplifier Controller IC

THAT5263

FEATURES

- Wide gain range: 0 dB to 51 dB in 3 dB Steps
- Wide supply range: ±5V to ±17V
- Wide output swing: + 29.6 dBu (±17V)
- Wide input swing: + 29.6 dBu (±17V)
- Low Power: 48mW @± 15V Supplies
- Low THD+N: 0.003% @ 24 dB gain
- Zero-crossing detectors minimize switching noise
- Daisy chainable SPI interface
- Two general-purpose logic outputs
- Small 5mm x 5mm QFN24 package

APPLICATIONS

- Digitally controlled microphone preamplifiers
- Digitally controlled instrumentation amplifiers
- Digitally controlled differential amplifiers
- Audio Mixing Consoles
- Computer Audio Interfaces
- Audio Distribution Systems
- Digital Audio Snakes
- Audio Recorders

DESCRIPTION

The THAT 5263 is a 2-channel digital preamplifier controller intended for use with low-noise, analog, differential audio preamplifiers such as the THAT 1580 and 1583. The 5263 controls gain from 0dB to 51 dB in 3dB steps while preserving low noise and distortion. Operating from ±5V to ±17V analog supplies, it supports input signal levels as high as +29.6 dBu (at 0dB gain, ±17V supplies, and THAT1580) without an input pad. Used with a THAT 1580 preamplifier IC, equivalent input noise (EIN) at 51 dB gain is -128.3 dBu (20 Hz - 20 kHz bandwidth, 150-ohm source).

Each 5263 channel includes a zero-crossing detector to minimize glitches (zipper noise) during gain adjustments. A built-in timer forces a gain change if no zero crossing occurs within 24 msec of a gain change command. A busy pin (BSY) allows synchronization of external events and the 5263's own GPOs with the zero-crossing detector.

The 5263 is controlled via an industry standard serial-peripheral interface (SPI) port. The part mates perfectly with the THAT 1580 and 1583 Differential Audio Preamplifier ICs. Together, these combinations provide high performance, space-saving solutions for digitally-controllable audio preamplifiers. However, the 5263 may also be used to control discrete preamplifiers.

Fabricated in a high-voltage CMOS process, the 5263 comes in a small (5x5 mm) 24-pin QFN package, making it suitable for small portable devices.

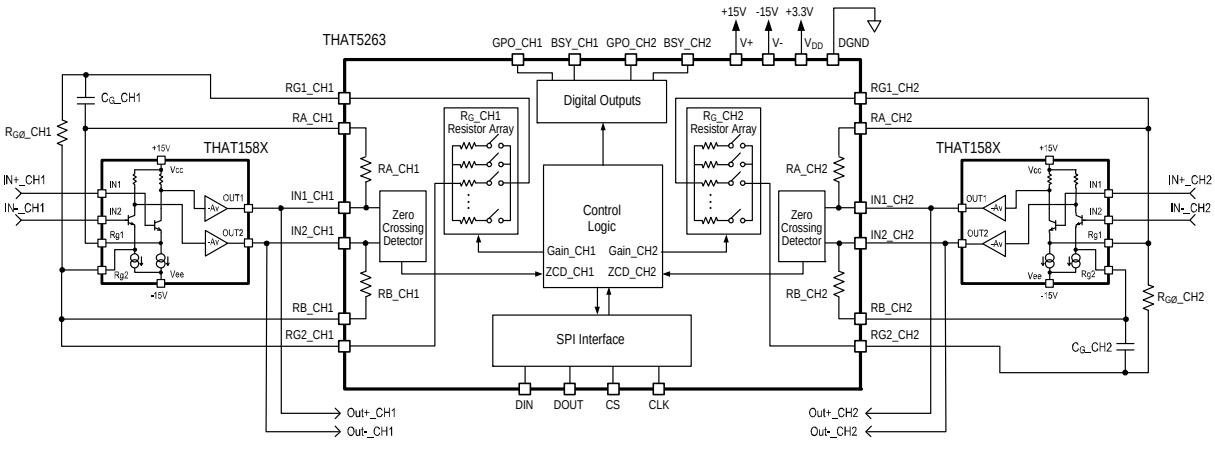

Figure 1. THAT5263 Simplified Application Circuit

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Pin Number	Pin Name	Pin Description
1	RB_CH2	Channel 2 Feedback Resistor B
2	IN2_CH2	Channel 2 Feedback Network Input 2
3	V-	Negative Analog Supply Voltage
4	V+	Positive Analog Supply Voltage
5	IN1_CH1	Channel 1 Feedback Network Input 1
6	RA_CH1	Channel 1 Feedback Resistor A
7	RG1_CH1	Channel 1 Gain Resistor Terminal 1
8	RG2_CH1	Channel 1 Gain Resistor Terminal 2
9	RB_CH1	Channel 1 Feedback Resistor B
10	IN2_CH1	Channel 1 Feedback Network Input 2
11	$\overline{CS}$	Chip Select (Active Low)
12	SCLK	Serial Clock Input
13	DIN	Serial Data Input
14	DOUT	Serial Data Output
15	VDD	Logic Supply voltage (+3.3V)
16	DGND	Digital Ground
17	BSY_CH1	Channel 1 Busy Output
18	BSY_CH2	Channel 2 Busy Output
19	GPO_CH1	General Purpose Logic Output Channel 1
20	GPO_CH2	General Purpose Logic Output Channel 2
21	IN1_CH2	Channel 2 Feedback Network Input 1
22	RA_CH2	Channel 2 Feedback Resistor A
23	RG1_CH2	Channel 2 Gain Resistor Terminal 1
24	RG2_CH2	Channel 2 Gain Resistor Terminal 2

Table 1 - Pin Assignments

SPECIFICATIONS[1,4]

Absolute Maximum Ratings[3,5]

Total Analog Supply Voltage (V+)-(V-)	36 V	Maximum Current Through V_{DD}, D_{GND}	50 mA
Positive Analog Supply Voltage (V+)-(V_{DGND})	18 V	Maximum Digital Input Voltage (V_{IDMax})	V_{DD} + 0.3 V
Negative Analog Supply Voltage (V-)-(V_{DGND})	-18 V	Minimum Digital Input Voltage (V_{IDMin})	D_{GND} - 0.3 V
Digital Supply Voltage (V_{DD}-V_{DGND})	4.5 V	Storage Temperature Range (T_{ST})	-40 to +125 ºC
Positive Voltage at Analog Pins IN, RF, RG	V+	Operating Temperature Range (T_{OP})	-40 to +85 ºC
Negative Voltage at Analog Pins IN, RF, RG	V-	Junction Temperature (T_{JMAX})	+125 ºC

Electrical Characteristics[2,5]

Parameter	Symbol	Conditions	Min.	Typ.	Max	Units
Power Supply						
Analog Supply Voltage	V+ ; -(V-)	Referenced to D_{GND}	4.75	—	17	V
Digital Supply Voltage	V_{DD}	Referenced to D_{GND}	3.0	3.3	3.6	V
Analog Supply Current	I+ ; -(I-)	No Signal	—	1.6	2.2	mA
Digital Supply Current	I_{DD}	No Signal	—	50	70	µA
Resistor Network Characteristics						
Gain Range	G	Internal feedback and gain resistors	—	0 to 51	—	dB
Gain Step Size			2.5	3.0	3.5	dB
Gain Error		Internal feedback and gain resistors				
		0~39 dB gain setting	-0.5	—	0.5	dB
		42~51 dB gain setting	-1.0	—	1.0	dB
Gain Matching		Channel 1 vs Channel 2	-0.25	—	0.25	dB
Feedback Resistors	RA, RB		4	5	6	kΩ
Zero-Crossing Detector Characteristics						
Zero-Crossing Detector Threshold			—	±12.5	—	mV
ZCD Timeout	t_{ZTO}	Built-in time-out	—	24	—	ms
AC Characteristics						
Maximum Voltage at IN1, IN2 pins		Differential signal	—	—	(V+) - 0.3	V
		Common-mode signal	—	—	(V+) - 0.3	V
Minimum Voltage at IN1, IN2 pins		Differential signal	V-	—	—	V
		Common-mode signal	(V-) +1	—	—	V
Voltage at RA, RB pins			V-	—	V+	V
Current in RF resistors			—	—	3.7	mArms
Maximum voltage across RG1 - RG2 pins			[(V-) - (V+)] / G	—	[(V+) - (V-)]/ G	V
Crosstalk		All switches off	117	—	—	dB
THD+N	THD	1 kHz, Gain = 24 dB	—	0.003	—	%
		+24 dBu across IN1-IN2, Pure differential signal				

[1] All specifications subject to change without notice.
[2] Unless otherwise noted, T_A = 25°C, V+ = +15V, V- = -15V, V_{DD} = +3.3V.
[3] Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[4] 0 dBu = 0.775 Vrms
[5] Parameters specified for typical application circuit shown in Figure 1.

Electrical Characteristics (con't) [2,5]

Parameter	Symbol	Conditions	Min.	Typ.	Max	Units
Digital I/O and Switching Characteristics						
High-Level Input Voltage	V_{IH}		0.7 x V_{DD}	–	–	V
Low-Level Input Voltage	V_{IL}		–	–	0.3 x V_{DD}	V
High-Level Output Voltage at Io = 4 mA	V_{OH}		0.8 x V_{DD}	–	–	V
Low-Level Output Voltage at Io = - 4 mA	V_{OL}		–	–	0.4	V
Input Leakage Current	I_{in}		–	2	–	µA
Input Capacitance			–	3.5	–	pF
SCLK Frequency	f_{SCK}		–	–	10	MHz
SCLK Low Time	t_{SCL}		40	–	–	ns
SCLK High Time	t_{SCH}		40	–	–	ns
DIN to SCLK Rising Setup	t_{DSU}		15	–	–	ns
SCLK Rising to DIN Hold Time	t_{DH}		15	–	–	ns
$\overline{CS}$ Enabled to SCLK High	t_{CSCR}		50	–	–	ns
$\overline{RST}$ Release to CS Active	t_{SRS}		100	–	–	ns
$\overline{CS}$ Enabled to DOUT Active	t_{CSDA}		100	–	–	ns
$\overline{CS}$ Release to DOUT Tristate	t_{CSDH}		5	–	20	ns
SCLK Falling to DOUT Valid	t_{CFDO}		–	–	15	ns
$\overline{CS}$ High Time Between Transmissions	t_{CSH}		25	–	–	µs
$\overline{CS}$ Release to SCLK Rising	t_{CSRCR}		100	–	–	ns

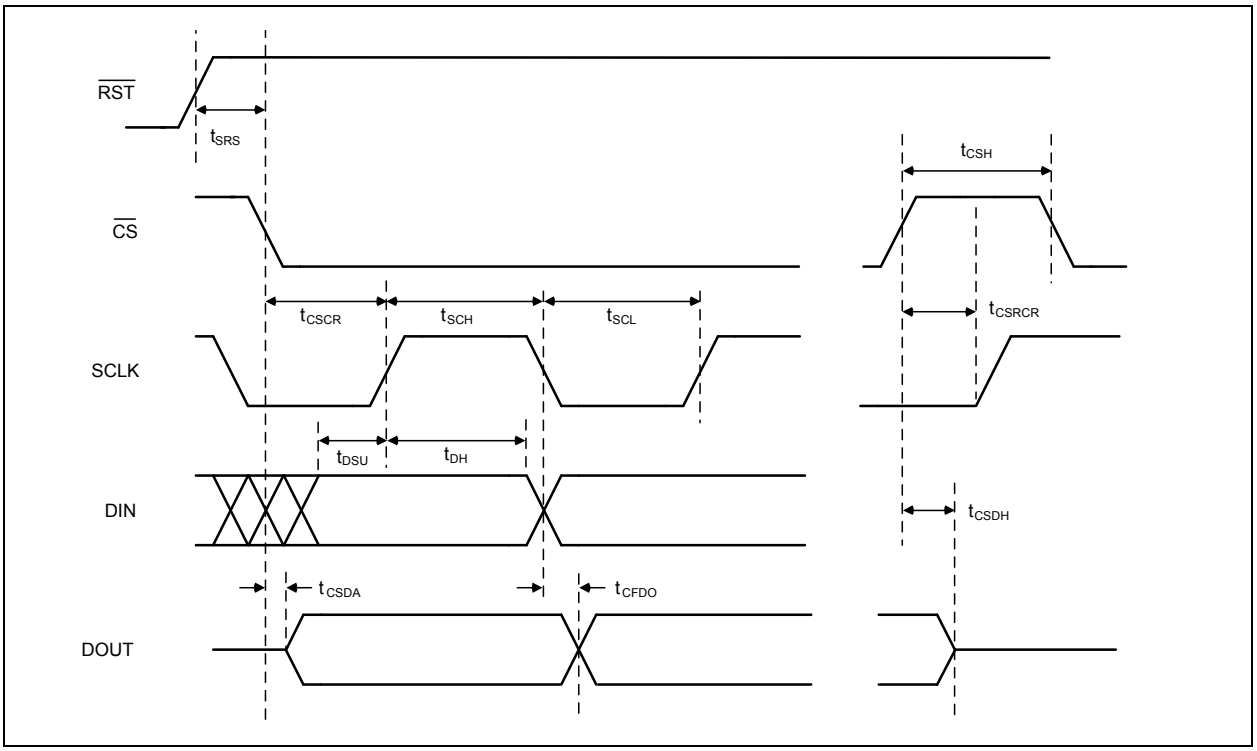


Figure 2. SPI Timing

Theory of Operation

The THAT 5263 contains two sets of precision resistors, switched by a set of CMOS FET switches, configured to create a pair of variable, switched, differential attenuation networks. The networks impedances are ideal for controlling gain in low-noise instrumentation amplifiers, and are optimized for low source-impedance applications.

Using the 5263

The attenuators are intended primarily for use in the feedback loop of differential gain stages, such as the THAT 1580 and 1583. Designed specifically for use in high-performance microphone preamplifiers, THAT's engineers paid careful attention to precision, stability, and control over the resistors and their switches in order to maintain excellent audio performance over a wide range of gains and signal levels.

Figure 3 shows one channel of the 5263 connected to a 158X. Resistors R_A, R_B, and R_G form a differential attenuator ("U-pad"). The amplifier's differential output is applied to R_A and R_B. The output of the attenuator, appearing across R_G, is ac-coupled via C_G to the inverting (differential) inputs of the 158X (the R_{G1} and R_{G2} pins). The voltage divider ratio $(R_B+R_A)/R_G$ thus controls the differential gain of the circuit.

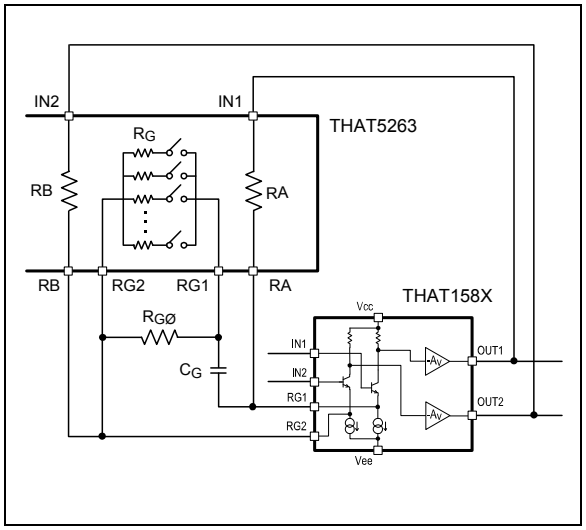


Figure 3. 5263 analog connections to a 158X

The 5263 changes the R_G value based on the gain command provided via the SPI control interface. Resistors R_A and R_B are constant at ~5kΩ. At 0dB gain R_G is an open circuit. At +51dB gain, R_G is ~28.2Ω. To achieve other gains, R_G is varied by internal CMOS switches in order to produce 3dB gain steps from 0 to +51 dB. The nominal value for the R_G resistors for each gain setting is listed in Table 2 below.

Gain Setting (dB)	R_G (Ohms)	"Gain" Register
0	Inf	0
3	24,200	1
6	10,000	2
9	5,680	3
12	3,350	4
15	2,110	5
18	1,440	6
21	966	7
24	671	8
27	470	9
30	325	10
33	230	11
36	162	12
39	113	13
42	80	14
45	56.5	15
48	40	16
51	28.2	17

Table 2. Internal R_G resistance values

Accommodating High Signal Levels

One key objective of the 5263 design was to accommodate full professional-audio signal levels. Accordingly, it is fabricated in a high-voltage CMOS process which allows operation up to ±17V analog power supplies. Along with patented drive circuitry to the switching FETs, this permits low-distortion operation at signal levels up to over +29 dBu in (at minimum gain -- 0dB), and +29dBu out (regardless of gain). See THAT's Design Note DN140 for more discussion and ideas if operation to over +29 dBu is required.

Switching Noise

The 5263 includes several features which minimize switching noise during gain changes. The patented drive circuitry slows down the FET-gate drive to minimize charge injection. This helps suppress clicks when changing gain. When used with THAT's 158x series of amplifiers, in the absence of any program, gain changes are barely audible as clicks. In the presence of signal, gain changes will necessarily modulate the signal. The 5263 includes zero crossing detectors to reduce the audible effect of this modulation.

When enabled, the two built-in zero-crossing detectors restrict gain changes to times when the analog signal is very close to zero. The detectors monitor the

differential signal present between the IN1_CHx and IN2_CHx pins of the 5263. When enabled, this permits gain changes to take place only when the differential (output) signal in the associated channel is typically within ±12.5 mV. An internal ~24msec timeout ensures that a gain change will always occur at the expiration of the timeout in case the signal has not gotten within the voltage window by that time.

When the zero-crossing detector prevents a gain change, the associated channel's BSY pin goes high. Once the gain change is allowed, the BSY pin changes state. This enables external circuitry to synchronize with the signal's zero-crossing behavior. As well, each general purpose output (GPO) may optionally be synchronized with its channel's zero-crossing detector. (See the Applications section for details.)

With the zero-crossing feature enabled, gain changes in the presence of program material are significantly less audible than without it enabled.

DC Offsets

We recommend that the R_Gx resistors be ac-coupled with an external capacitor in order to maintain constant (unity) dc gain at all ac (audio) gain settings. This will ensure that the dc voltage across the outputs of the two amplifiers is constant and relatively small. A single capacitor, either between the RAx and RG1x pins or between the RBx and RG2x pins is sufficient. The choice of which pair of pins to use on either channel can be made based on ease of PCB layout.

The coupling capacitor creates a low-frequency rolloff at gain settings greater than 0dB. At high gains the -3 dB frequency will be

$$f = \frac{1}{2\pi \cdot R_G \cdot C_G}$$

With the 1000uF capacitor shown in Figure 1, at the 51dB gain setting, the response will be down 3dB at 5.6Hz. The capacitor will not see much voltage (very little signal voltage, plus only the offset voltage of the associated analog gain stage); therefore, it can be a low-voltage type. While the manufacturer of the capacitor to be used will have the last word on this subject, THAT understands that most polarized electrolytic types can withstand at least 1V reverse bias without damage. This permits use of a polarized capacitor in this application.

The use of an ac-coupling capacitor in the feedback loop prevents changes in output offset as the gain settings are changed. This, along with the use of the zero-crossing detector, minimizes audible artifacts during gain changes.

SPI Control Interface

The 5263 provides a daisy-chainable serial-peripheral interface (SPI) port for digital control of its internal parameters. The SPI port may be clocked at speeds up to 10MHz, so the full 32-bit control word can be clocked into the chip in less than 4 µs.

The SPI port consists of four signals: Chip Select ($\overline{CS}$), Data In (DIN), Data Out (DOUT), and Serial Clock (SCLK). Figure 4 shows a single 5263 device connected to the SPI port of a typical host microcontroller. A command sequence is initiated when $\overline{CS}$ makes a high to low transition. Data is clocked into DIN on rising edges of SCLK, through an internal 32-bit shift register (16 bits per channel) which holds the 5263 configuration, and then out the DOUT pin on falling edges of SCLK. $\overline{CS}$ makes a low to high transition at the conclusion of a command sequence. The DOUT pin is tristated while $\overline{CS}$ is high so that multiple devices can be connected to a single SPI MISO port on a host processor.

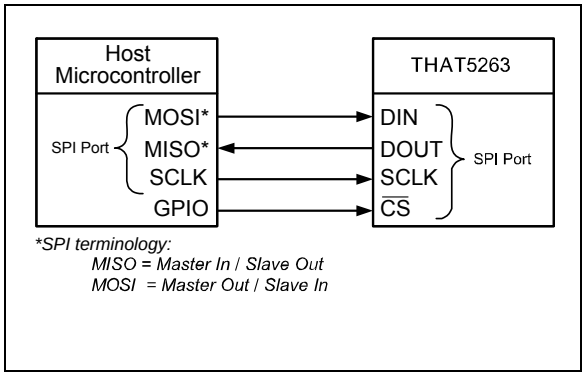


Figure 4. Single 5263 connected to a host computer

The 32-bit control word contains two concatenated 16-bit words, one for each of the 5263's channels. The control word for channel 1 is transmitted first. The word definition is shown in Figure 5.

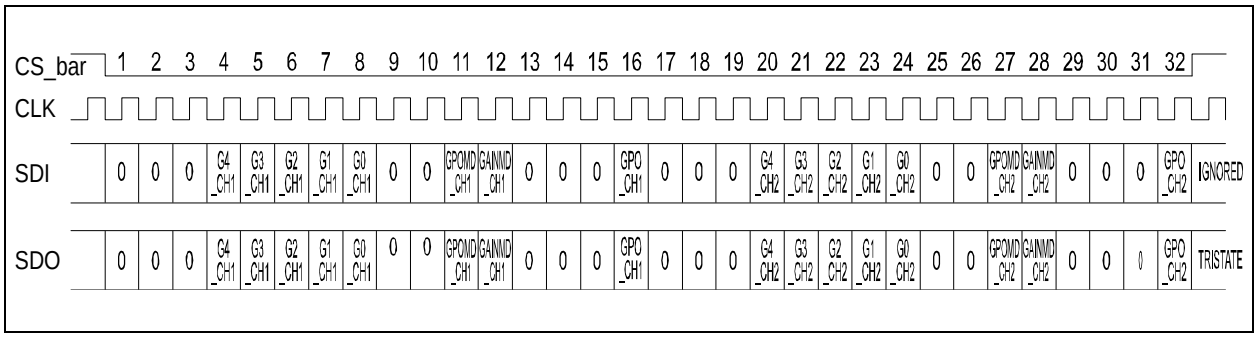


Figure 5. 32 Bit Word Definition

Signal	Pin	I/O	Function
$\overline{CS}$	11	Input	Device chip select input, active low. An SPI transfer begins with a high-to-low $\overline{CS}$ transition and ends with a low-to-high $\overline{CS}$ transition. When $\overline{CS}$ is high, SCLK transitions are ignored.
SCLK	12	Input	SPI serial clock input. An SPI master supplies this clock with frequencies up to 10MHz. Data is clocked into the DIN pin on the rising edge of SCLK. Data is clocked out of DOUT pin on the falling edge of SCLK.
DIN	13	Input	SPI serial data input (Master-Out, Slave-In).
DOUT	14	Output/Tristate	SPI serial data output (Master-In, Slave-Out). DOUT is tristated when $\overline{CS}$ is high.

Table 3. SPI Signals

Parameters

The 5263 parameters that can be controlled via SPI are:

- GAIN_CH1 (CH2) (5 bits)
- GPO_CH1 (CH2) (1 bit)
- GPOMD_CH1 (CH2) and GAINMD_CH1 (CH2) (2 bits)

GAIN_CH1 (CH2) (5 bits)

The GAIN_[n] [4:0] bits set the value of R_G for the designated channel. Note that each increment of 1 in the GAIN value results in a 3dB increment in gain. See Table 4 for gain settings. Note that gain commands between 18 and 31 are ignored.

Reset default = 00000 (0dB)

GPO_CH1 (CH2) (1 bit)

Each of the GPO bits controls the state of the respective GPO port for the designated channel as follows:

0 = GPO_[n] "off" (0V)

1 = GPO_[n] "on" (3.3V)

Reset default = 0 (all ports off)

GPOMD_CH1 (CH2) and GAINMD_CH1 (CH2) (2 bits)

The zero crossing detector for the designated channel can be independently enabled for GPO and gain changes via the GPOMD_[n] and GAINMD_[n] bits respectively. Table 5 shows the bit settings for each of the modes.

Reset default = 00 (ZCD off)

GAIN [4:0]					Decimal Value	5263 Gain
G4	G3	G2	G1	G0		
0	0	0	0	0	0	0
0	0	0	0	1	1	3
0	0	0	1	0	2	6
0	0	0	1	1	3	9
0	0	1	0	0	4	12
0	0	1	0	1	5	15
0	0	1	1	0	6	18
0	0	1	1	1	7	21
0	1	0	0	0	8	24
0	1	0	0	1	9	27
0	1	0	1	0	10	30
0	1	0	1	1	11	33
0	1	1	0	0	12	36
0	1	1	0	1	13	39
0	1	1	1	0	14	42
0	1	1	1	1	15	45
1	0	0	0	0	16	48
1	0	0	0	1	17	51
1	0	0	1	0	18	X
		:			:	:
1	1	1	1	1	31	X

Table 4. Gain Settings, circuit of Figure 1.

GPOMD_[n]	GAINMD_[n]	
X	0	= Immediate GAIN updates
X	1	= GAIN updates on ZC
0	X	= Immediate GPO updates
1	X	= GPO updates on ZC

Table 5. Zero Crossing Detector Enable Bits

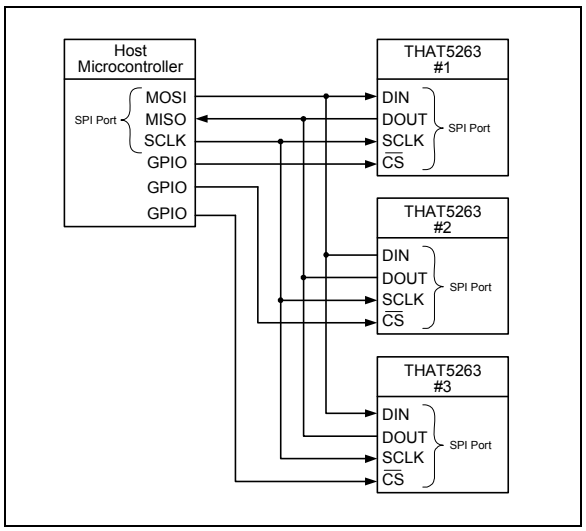


Figure 6. Multiple 5263 ICs connected in parallel to a host microcontroller, with independent chip selects.

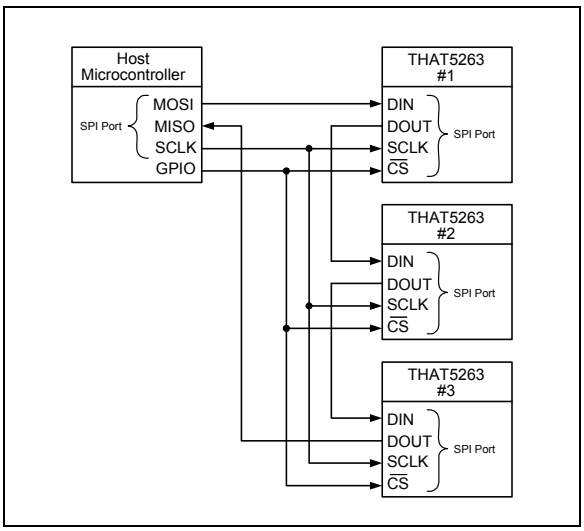


Figure 7. Multiple 5263 ICs connected in a daisy-chained mode to a host microcontroller.

Multiple Devices with Separate Chip Selects

The SPI port can be operated with multiple ("N") devices by using separate chip selects as shown in Figure 6. The advantage of this method over daisy chaining is that any of the N 5263 devices may be updated with a single 32-bit SPI operation (as opposed to the long Nx32 bit data stream required when N devices are daisy chained). The disadvantage of this method is N different chip selects must be supplied -- one to each of the individual devices.

Daisy Chaining

Multiple devices can be daisy-chained by connecting the DOUT of device N to the DIN pin of device N+1, as shown in Figure 7. Data is loaded by holding the common $\overline{CS}$ low for 32 x N SCLK pulses, where N = total number of devices in the daisy chain. All devices are simultaneously updated on the rising edge of $\overline{CS}$. This is particularly useful in applications where updates to a large number of channels must be synchronized. Another advantage of this method is that one chip select can be shared by all devices, simplifying the digital control circuitry on the PCB. The disadvantage is all N devices must be updated as a group, thereby slowing down the rate of control to each individual device.

ESD Protection and Turn-on Time

The 5263 employs a power-rail clamp on the 3.3V logic power supply to protect against ESD. This system is very effective at protecting the part, but can cause some unexpected effects during power-supply turn on.

The ESD clamp is activated during power-up, and the 5263 will not respond, and its input pins will be held low, for a period of time that depends on the available power supply current and the temperature of the part. Figure 8 shows the relationship between the available supply current and the turn-on time for various temperatures.

Note that during power-up the 5263 will draw high current (up to 150mA) from the V_{DD}, 3.3V supply. This will not damage the part. During the power-up period, the part's digital input pins will also draw high currents from whatever is driving them. THAT recommends that this current be limited to under 20mA. As well, this can interfere with other devices connected on the same bus, so we suggest adding at least 100Ω isolation resistors in series with each of the DIN, SCLK and $\overline{CS}$ lines to isolate them. Placing these isolation resistors close to the source will also serve to slow down the rise time of these signals, minimizing any tendency for them to crosstalk into nearby analog circuitry.

For more details on the ESD protection system, see Appendix 1.

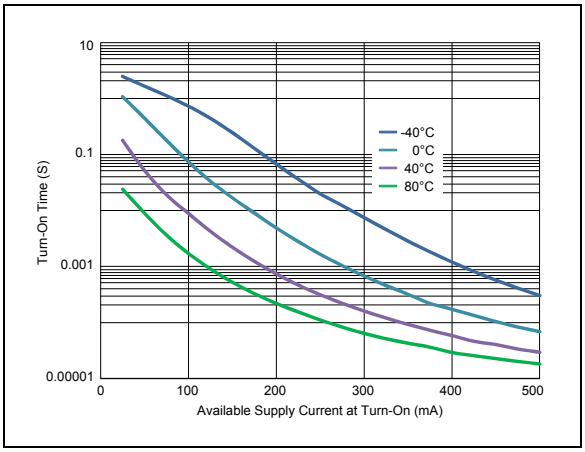


Figure 8. 5263 nominal turn-on time versus available supply current and temperature

Applications

While the 5263 is perfectly suitable as a feedback network for many differential amplifiers, the applications discussed herein are exclusively based on use with THAT's line of low-noise, differential-input, differential-output preamplifiers. For application with other amplifiers, contact us at apps_support@thatcorp.com

Gain Ranges in Basic Configurations

The circuit of Figure 9 pairs the 5263 with a THAT 1580 or 1583 analog gain stage. Pairing with the 1580 offers the best high-gain noise performance among THAT's available analog gain stages. For cost-sensitive applications, the 1583 may be used, but high-gain noise will be dominated by the 1583's somewhat higher input noise floor.

The circuit of Figure 9 offers differential gain that varies from 0 to 51dB in 3-dB steps. At minimum gain (0dB) and with ±15V supply rails, the maximum (differential) input signal level is typically +26.8 dBu, limited by the available headroom of the 1580's input. At maximum gain (+51 dB), signal levels are limited by the output headroom of the 158X, which is typically +27dBu (-24 dBu at the input). All these figures increase by a little over 1.3 dB if the circuit is run from ±17V supplies. The equivalent input noise of the circuit of Figure 9 ranges from -103 dBu at 0dB gain to -128.3 dBu at 51dB gain using a 1580 (all figures are based on 20Hz~20kHz bandwidth, and assume a 150Ω input (source) termination). Since many of these performance specifications are limited by the analog gain stage, performance will vary with other amplifiers.

When either channel of the 5263 is set to 0 dB gain, its internal R_G network is an open circuit. Under this condition external capacitor C_G may accumulate charge and the terminal connected to one of the RG pins on the 5263 can float to a new potential. When the gain is changed to any other setting than 0 dB, C_G charges quickly to the correct potential (typically the preamplifier input voltage offset), resulting in an audible "thump". To prevent this we recommend adding external resistor R_G0_Chx. Note, however, that with the recommended value of 1 MΩ the gain at the 0 dB setting will be about +0.09 dB.

The 5263's internal power-on reset circuitry ensures that the device powers up at 0 dB gain. At this gain setting the charging time constant for the C_G capacitor will be long (1000 seconds for the recommended values of 1000µF for C_G and 1 MΩ for R_G0). Until C_G charges (to the input offset voltage of the preamplifier to which the 5263 is connected) gain changes can result in audible pops. In order to speed up the charging time THAT recommends that the gain be set to a higher value for a short time after power on, while muting the output of the channel. Bringing the gain setting to the maximum of 51 dB shortens the time constant to 28 msec for the recommended 1000µF C_G capacitor. Maintaining this setting for a few hundred milliseconds (presumably

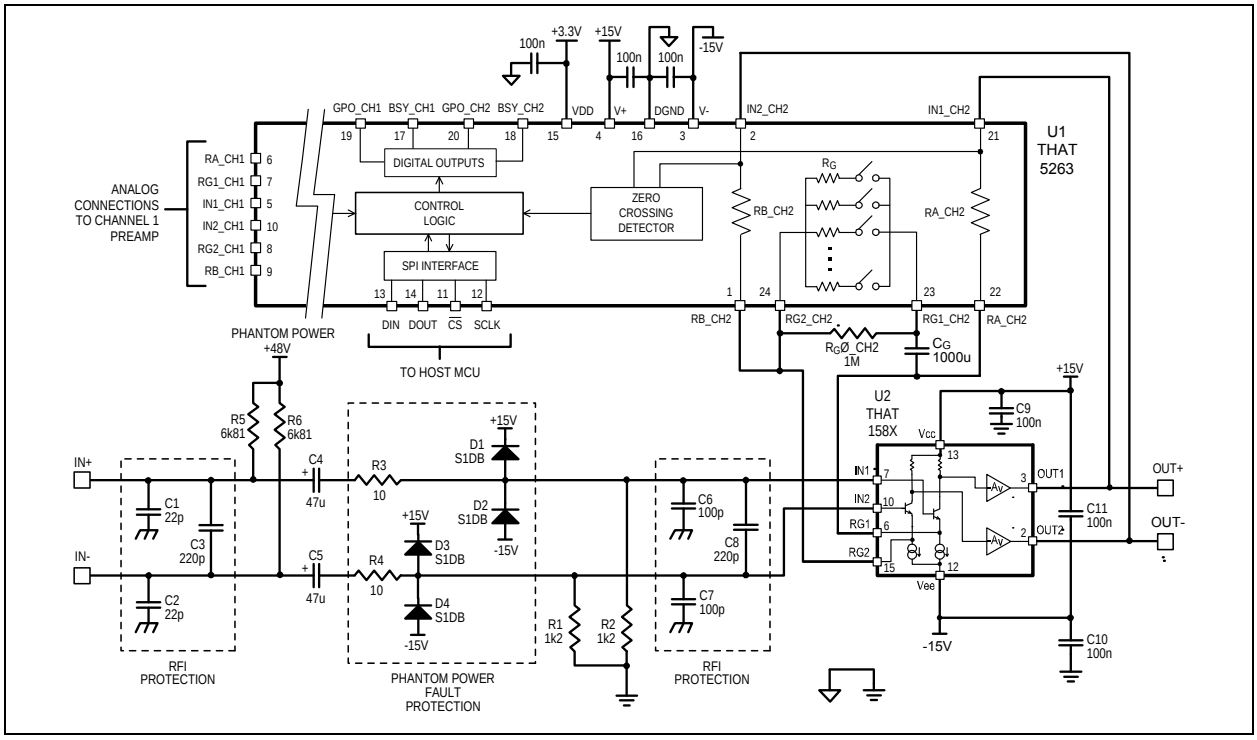


Figure 9. 5263 and 158X basic application circuit.

while the system is still muted) will ensure that the C_G capacitor is properly charged

For single-ended analog outputs, the circuit of Figure 9 can be followed by a differential-to-single-ended converter, as shown in Figure 10. When converting to single-ended signals, take care to select a low-noise opamp, and pay attention to the noise generated by the impedances. The component values shown in Figure 10 will largely preserve the dynamic range of the 158X and 5263 combination.

For many applications, the output of the microphone preamplifier must drive an analog-to-digital converter. Most high-performance A/D converters have differential inputs, and cannot accept differential signals greater than ~+8dBu. For such applications, the output of the mic preamp must be attenuated to prevent overload of the A/D converter. The circuit of Figure 11 shows a simple circuit using a resistive attenuator (R_9 through R_{11}). The impedance levels of the attenuator are chosen to minimize their self-generated voltage noise, and to stay within the load limits of the 158X which drives them.

Figure 11 assumes that the maximum differential input to the A/D converter is +8dBu. For higher (or lower) maximum input levels, or for different supply voltages to the 158X and 5263, scale the attenuation ratio accordingly, keeping its total impedance (R_9+R_{10}+R_{11}) the same. Note that the noise contribution of the U-pad can compromise the theoretical noise performance of the 158X/5263 combination at minimum gain. Moreover, the non-zero impedance drive to the converter may increase distortion with high-performance converters. The impact of this impedance depends on the ADC.

CMRR of the Preamp

One drawback of the circuit of Figure 11 is that it does not attenuate common-signals. The 158X has unity common-mode gain regardless of its differential gain. The U-pad attenuator formed by R_9~R_{11} attenuates differential signals but not common-mode signals, so the CMRR of this section of the circuit is actually -18dB at minimum gain: when the 5263 is set for 0dB gain, differential input signals are attenuated by 18dB, but common-mode signals are passed without any attenuation.

Differential-input A/D converters generally provide high common-mode rejection, so the system CMR, including the converter may well be acceptable, but consider what happens if a large common-mode signal is present along with a large differential input signal. (This is more likely to be the case when using the preamp as a line input than for microphone inputs.) The output of Figure 11 ("To ADC Input") will see that large common-mode input signal, along with an 18dB attenuated version of the differential input signal. If sufficiently large, the common-mode signal can cause the converter to clip prematurely, modulating the differential audio with the common-mode signal. While this may only occur in extreme use conditions, it may be of some concern.

To avoid this issue, consider the circuit of Figure 12, which removes the common-mode signal (depending on

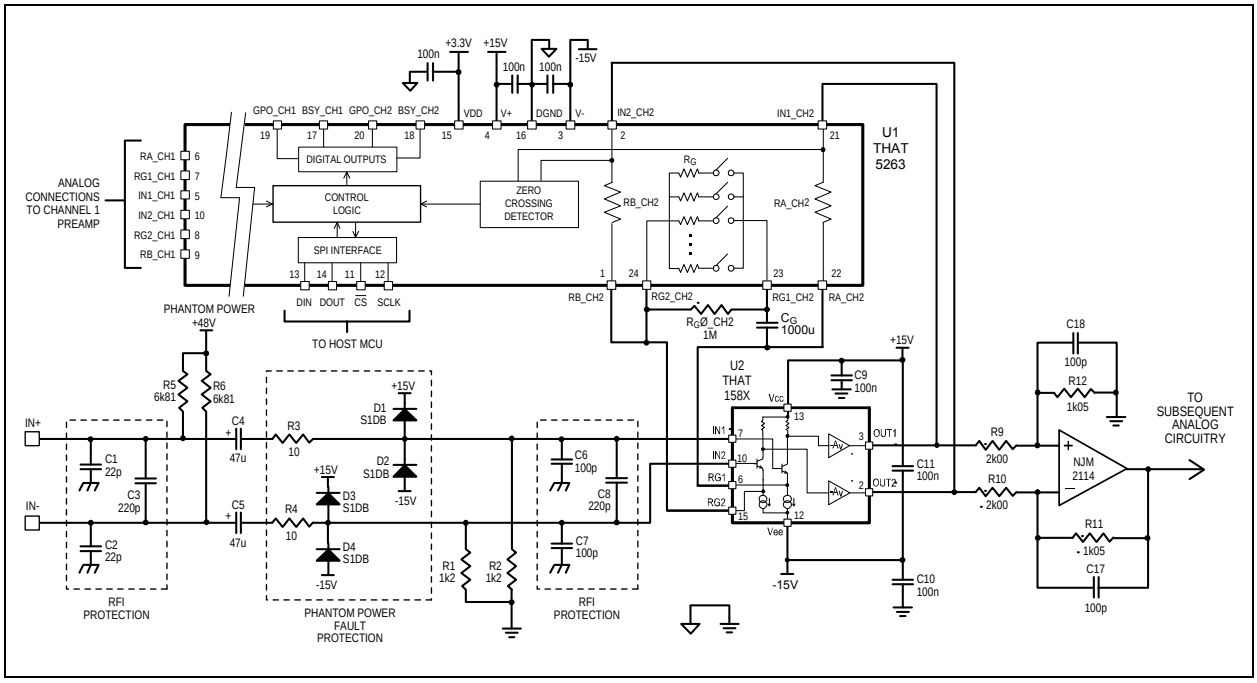


Figure 10. 5263 and 158X typical application with single-ended output.

the matching of resistor ratios R_9/R_{10}, and R_{11}/R_{13}) before it reaches the A/D converter input. This circuit also provides a low-impedance drive for the converter, recommended by many converter makers for best distortion performance. The configuration (after Birt) also minimizes the noise contribution of the second (lower) inverter, since its noise appears in common mode and not differentially at the output.

Note that in this case, at low gains the CMRR of the system will be determined by the matching of resistor ratios R_9/R_{11} and R_{10}/R_{13}, with some contribution at high frequencies from the matching of C_{17} and C_{18}. At high gains, the CMRR of the output stage will be boosted by the differential gain of the 158X/5263 circuitry that precedes it.

RFI Protection (and Common-Mode Rejection)

The circuits of Fig 9 through 12 include RFI protection in two sections. Small capacitors (C_1 and C_2) are used from the positive and negative signal inputs to chassis ground, along with a larger capacitor (C_3) across the two inputs. These components should be located as close as possible to the input signal connector, and are intended to prevent RF from entering the chassis of the device.

A second RF protection network is located close to the amplifier, and is intended to prevent any RF picked up inside the unit from reaching the amplifier input, where it might be rectified and cause audio-band interference. This network consists of a pair of larger capacitors (C_6 and C_7) to ground and one more capacitor (C_8) across the two input lines. C_8 should be kept close to the 158X in order to ensure stability.

The design of these networks was arrived at after some consideration for common-mode rejection. Unbalanced capacitance from either input line (IN+ or IN-) to ground can unbalance common-mode signals, converting them to differential signals, which will be amplified along with the desired (differential) signal. The differential amplifier in the above circuits offers gain only to differential signals: common-mode signal gain is always 0dB. Therefore, its common-mode rejection is equal to the differential gain.

So long as common-mode signals are not converted to differential ones, this common-mode rejection will prevail. Because they are relatively small, differences in the values of C_1 and C_2 are less likely to cause imbalance than the larger capacitors at C_6 and C_7. For this reason, we recommend that capacitors C_6 and C_7 should be at least 5% types, in order to ensure matching between their values. Note that C_3 and C_8 affect only differential signals, and thus do not affect common-mode rejection.

Power Supply Decoupling

Power supply decoupling is required for stability of the 158X, and to minimize digital switching noise from propagating on the power supplies. The V+ and V- pins should be connected to the same analog supply which powers the analog gain stage, while the V_{DD} pin may be powered in common with other logic circuitry (microprocessors, etc.) in the unit.

THAT recommends one decoupling capacitor (C_{16}) for the digital power supply, placed close to pins 16

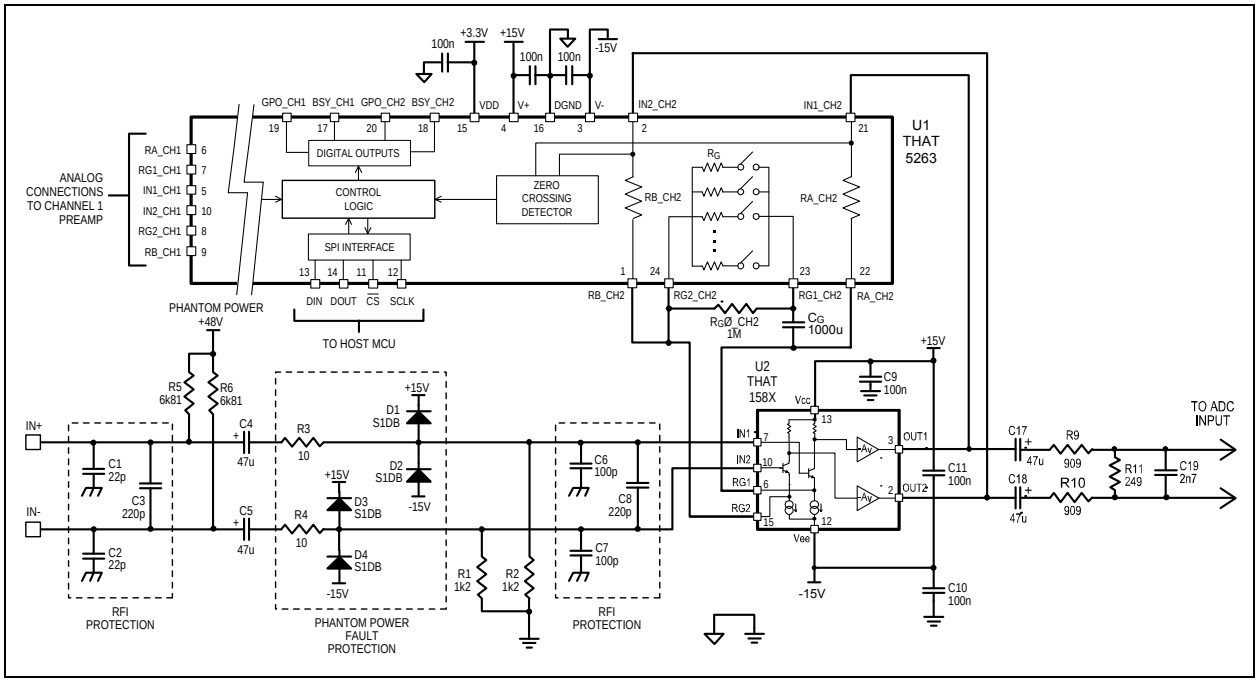


Figure 11. 5263 and 158X low-cost application for output to a A/D convertor.

(D_{GND}) and 15 (V_{DD}), as well as an additional pair of decoupling capacitors from pins 3 and 4 (V- and V+) to ground.

Take care to ensure that the power supply voltages never exceed the absolute maximum ratings even under transient conditions. Designers should especially consider how phantom power faults may cause transient supply disturbances via the diode bridge used to protect the 158X/5263 inputs. For more information, see "The 48 Volt Phantom Menace Returns", which is available on www.thatcorp.com.

Minimizing Digital Crosstalk

As mentioned in the section on ESD Protection and Turn-On Time (in the Theory of Operation Section), it is possible for fast-rising voltages on the SPI port pins to crosstalk into nearby analog circuitry. THAT recommends including 100Ω (or higher) isolation resistors in series with the source of the DIN, SCLK and $\overline{CS}$ lines. These resistors should be placed close to the sources, which will slow down the rise time on the digital lines and reduce pickup in the analog circuits. Also as noted earlier, this will help prevent the digital input pins from loading their driving circuitry during power up.

Zero Crossing Detectors

The integrated zero-crossing detectors for each channel may be enabled or disabled for the GAIN and GPO parameters independently (see Table 5). When enabled, each detector prevents gain and/or GPO changes from occurring until either a) the differential output signal amplitude in the respective channel is within ±12.5mV of 0V (regardless of the common-mode voltage), or b) the timeout (approximately 24 ms) has elapsed, whichever occurs first.,

When the GAINMD{n} or GPOMD{n} bits are zero (Table 5), Gain and GPO updates are made immediately following a rising edge on the $\overline{CS}$ pin. When GAINMD{n} and GPOMD{n} are logic high, updates are made on the next output signal zero-crossing after a rising edge on the $\overline{CS}$ pin.

The choice between "immediate" vs "zero crossing" mode depends on the application. Immediate mode has the advantage of providing gain updates with short and deterministic latency, whereas zero crossing mode has the advantage of minimizing glitches and zipper noise.

When using the zero-crossing detector, an additional consideration is that if a second gain command is sent to the part before the first gain command takes place (either through a zero-crossing or timing out), the timeout resets, and only the second gain command takes effect. In extreme cases, if a series of commands is sent, each within the timeout period, and no zero-crossing is reached before each gain command's timeout, only the last gain command will take effect. Accordingly, we recommend that when using the zero-crossing detector, individual gain commands should be separated by at least the timeout period.

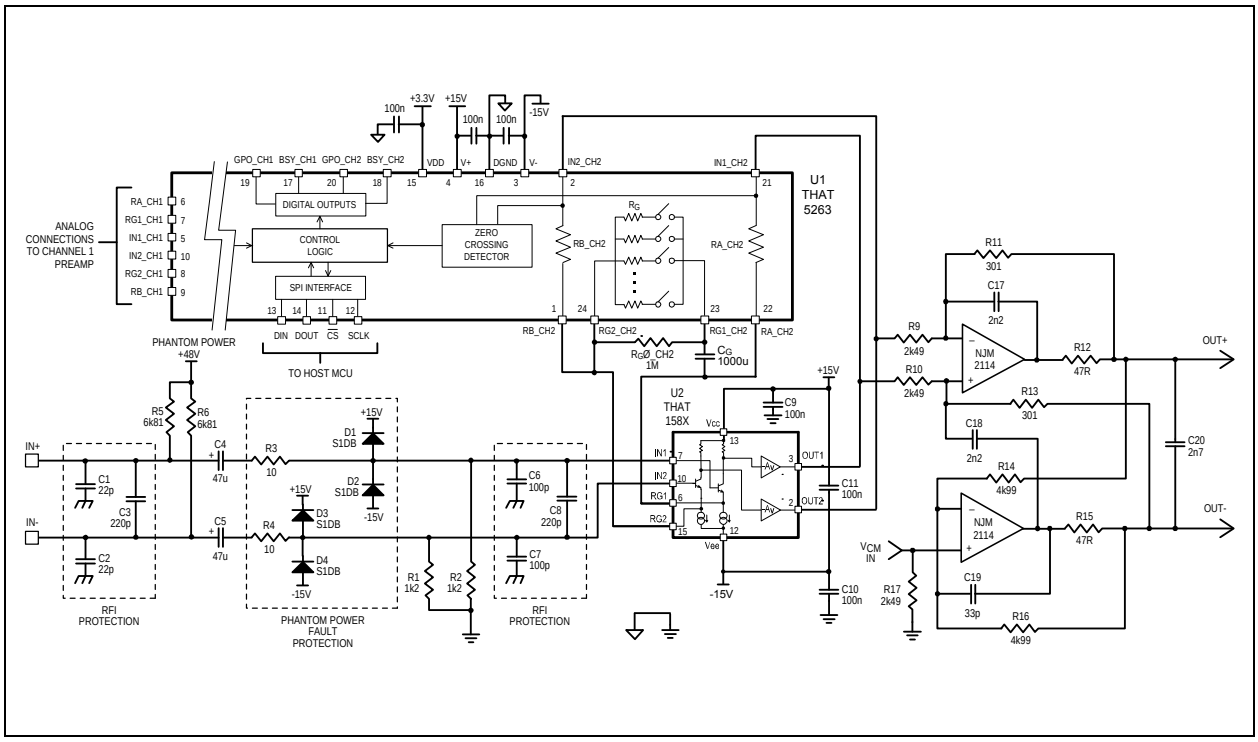


Figure 12. 5263 and 158X high-performance application for output to a A/D convertor.

Busy (BSY pins)

The BSY pin for its associated channel is asserted high when a gain update or GPO update for that channel is pending a zero-crossing. This pin may be monitored by the host microcontroller (e.g. connected to an external interrupt pin) in order to hold off a new gain command until the previous gain command has been executed.

If finer gain steps (e.g. 1dB) are implemented in external processing (DSP or in subsequent analog circuitry) the BSY signal can be employed to synchronize external gain changes with those implemented by the 5263. (This is important when the interpolated gain "wraps" from maximum to minimum as each of the 5263's 3dB steps occurs). Note that latency in A/D conversion must be considered when attempting to synchronize digital with analog gain updates.

Using the GPOs to Control Preamplifier Functions

There is one general-purpose logic output associated with each channel control word. While the General Purpose Outputs (GPOs) can be used to control any binary state functions, they are primarily intended to control analog functions associated with a preamplifier. Because the GPO for each channel may be synchronized with the zero-crossing detector for that channel, the GPOs are particularly useful for controlling external analog gain interpolation schemes.

Low Voltage Operation

In order to control distortion at high signal levels, the 5263 includes circuitry which applies a replica of the input signal across the CMOS switches to maintain a fixed voltage across their gate to source terminals. However, this approach stops tracking the input signals at power supply voltages below ~±8V, At such low supply voltages, the R_G resistance increases, which lowers the gain. The effect varies with gain: typically 1dB reduction between (nominal) 43 dB and 51dB gain, 0.5dB reduction between (nominal) 30 dB and 39dB gain

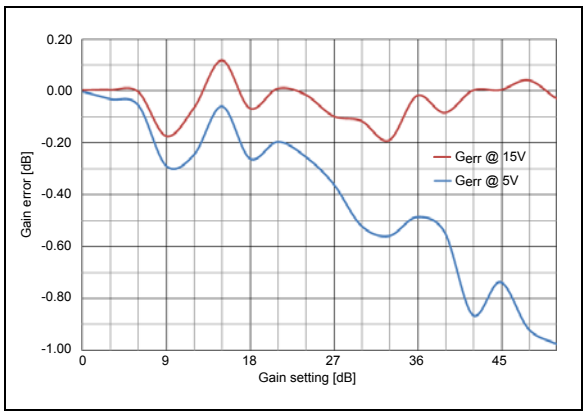


Figure 13. Typical gain error vs gain setting

PCB Layout Information

Figure 14 shows a suggested layout of the 5263 with two 158X preamplifier ICs. This layout is taken from the 5263/158X demonstration board, available from THAT. While the board itself is of course useful to designers, the layout and schematic are published in the demonstration board data sheet which is available for downloading from THAT's web site.

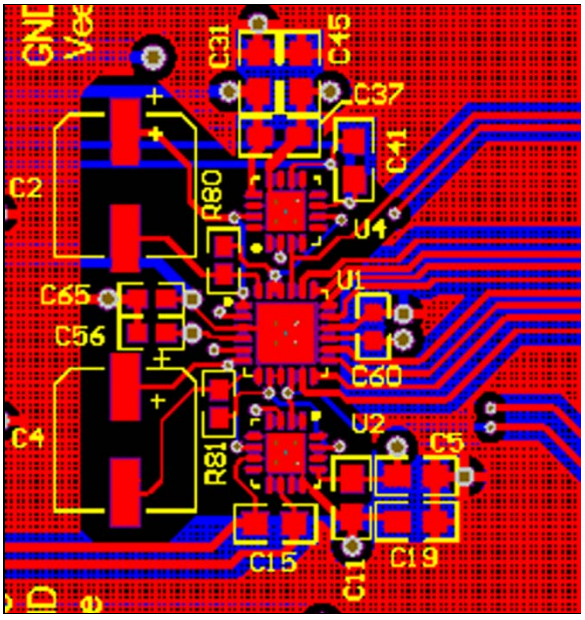


Figure 14. Recommended PCB Layout for THAT158X/THAT5263.

U1:THAT5263
U2, U4: THAT158X
C2, C4: C_G (1000uF)
R80, R81 $R_{G\varnothing}$ (1M)
All other capacitors shown are for supply bypassing (100nF)

Designers should take care to minimize capacitance on the R_G pins, and to ensure that power supply lines do not run close and/or parallel to either the input signal lines or the traces and pins connected to the R_G pins. For current feedback amplifiers such as the 158X, stray capacitance from the R_G pins (inverting input) to ground or power planes results in higher gains at high frequencies. As a result, mismatches in the capacitance on these two nodes will degrade common-mode performance at high frequencies.

Additionally, power supply lines, which often carry non-linear (e.g., half-wave rectified) versions of the signal can magnetically and capacitively couple into the input and R_G lines. This can create distortion, particularly at high gains

Therefore, THAT recommends avoiding ground plane under the RG and RA/RB pins and associated traces.

We recommend that the metal "slug" on the bottom of the QFN package be soldered to provide physical attachment and improve thermal performance. It may be left unconnected electrically, or connected to V-.

When laying out the board, we recommend following advice offered by Henry W. Ott in his book Electromagnetic Compatibility Engineering, published in August 2009 by Wiley (ISBN: 978-0-470-18930-6). In it, Mr. Ott recommends laying out the digital and analog ground scheme using ground planes as if they were separate planes, but not to actually separate them in the final design. As noted earlier, all bypass capacitors should be located very close to their respective power and ground pins.

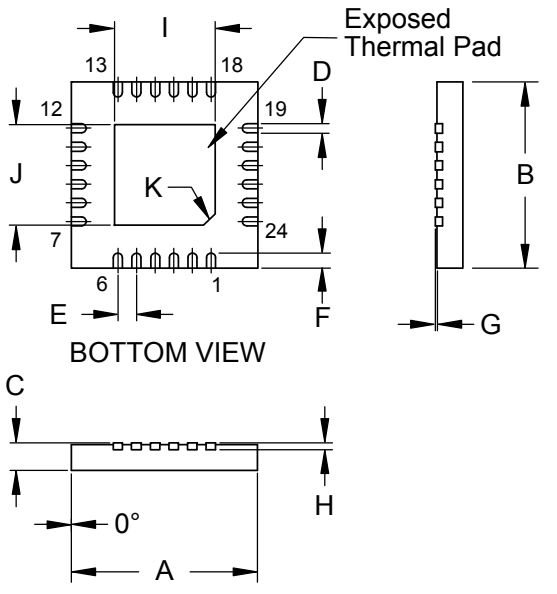
Package and Soldering Information

Package Characteristics

Parameter	Symbol	Conditions	Spec	Units
Package Style		See Fig. 15 for dimensions	5 X 5 mm 24 Pin QFN	
Thermal Resistance	θ_{JA}	QFN package soldered to board,	45	ºC/W
Environmental Regulation Compliance			Complies with RoHS 2 requirements	
Soldering Reflow Profile			JEDEC JESD22-A113-D (250 ºC)	
Moisture Sensitivity Level	MSL	Above-referenced JEDEC soldering profile	MSL-3	

The THAT5263 is available in a 5mm x 5mm 24-pin QFN package. The package dimensions are shown in Figure 15. Pinouts are given in Table 1

The 5263 is lead free and RoHS compliant. Material Declaration Data Sheets on the parts are available at our web site, www.thatcorp.com or upon request. For ordering information, see Table 6.



ITEM	MILLIMETERS	INCHES
A	5.00 ± 0.10	0.197 ± 0.004
B	5.00 ± 0.10	0.197 ± 0.004
C	0.90 ± 0.05	0.035 ± 0.002
D	0.25 ± 0.05	0.010 ± 0.002
E	0.65 ± 0.05	0.026 ± 0.002
F	0.40 ± 0.05	0.016 ± 0.002
G	0.00 ~ 0.05	0.000 ~ 0.020
H	0.20 ± 0.05	0.008 ± 0.002
I	3.40 ± 0.05	0.134 ± 0.002
J	3.40 ± 0.05	0.134 ± 0.002
K	C' 0.4 x 45°	C' 0.016 x 45°

Figure 15. QFN-24 Package Dimensions

Package	Order Number
24 pin QFN	5263N24-U

Table 6. Ordering Information

Appendix 1

ESD Protection and Turn-on Time (Additional Information)

A simplified schematic of the ESD protection scheme is shown in Figure 16. During an ESD event ESD stress currents are diverted through the ESD protection diodes DP and DN. Positive stress currents are steered to the DGND bus via a timer-controlled supply clamp, shown in simplified form in Figure 17. The clamp MOSFET MP turns on once its gate-to-source voltage exceeds ~1.5 V. The clamp remains on for a time period controlled by the R-C timer shown in Figure 17, nominally a few microseconds, which is longer than an ESD event.

The clamp is also activated during the initial turn-on of the 3.3V power supply. The clamp turns off once C in Figure 17 charges to about 1.5V. Since clamp transistor MP is on at power up, the power supply may initially be held low, which will delay charging C. The part will not start up until C reaches ~1.5V.

If the power supply is capable of sourcing the initial surge current required to bring the supply voltage above 1.5V while the clamp is on, the turn on will be quite fast. However, if the supply is current limited, the turn-on time will be extended. Furthermore, because the R and C in Figure 17 are implemented with MOS devices, and because the threshold voltage of the clamp device MP varies with temperature, this turn-on behavior varies with temperature, as shown in Figure 8.

Also, as mentioned earlier, all the digital I/O pins are connected to the same ESD protection system. Until the clamp deactivates during power up, the SPI input pins will be drawn low, and the SPI interface will not respond to external commands. This behavior is not hazardous to the 5263, and there are no requirements for supply sequencing of the high-voltage analog supplies with respect to the 3.3V logic supply, as long as the V- pin (substrate) is never more positive than .3 V above the DGND pin.

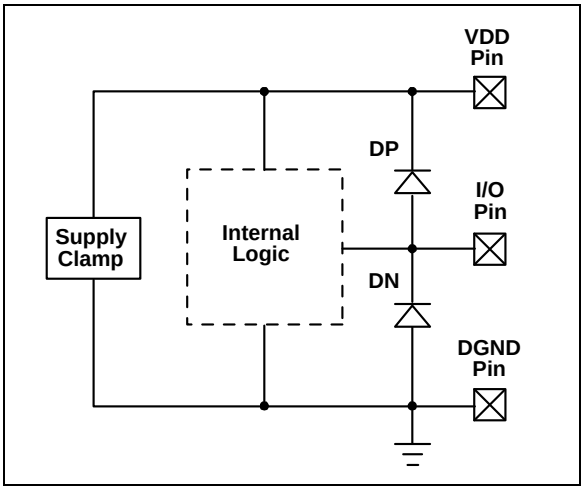


Figure 16. 5263 ESD protection scheme

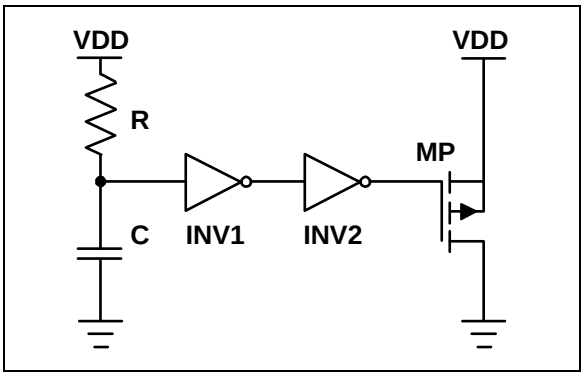


Figure 17. 5263 Supply Clamp Structure

Revision History

Revision	ECO	Date	Changes	Page
00	—	10/27/15	Initial Release	—

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