

RF Power Field Effect Transistors

High Ruggedness N-Channel Enhancement-Mode Lateral MOSFETs

These high ruggedness devices are designed for use in high VSWR industrial (including laser and plasma exciters), broadcast (analog and digital), aerospace and radio/land mobile applications. They are unmatched input and output designs allowing wide frequency range utilization, between 1.8 and 600 MHz.

- Typical Performance: $V_{DD} = 50$ Volts, $I_{DQ} = 100$ mA

| Signal Type | P_{out} (W) | f (MHz) | G_{ps} (dB) | η_D (%) | IRL (dB) |
|----------------------------------------|---------------|---------|---------------|--------------|----------|
| Pulsed (100 μ sec, 20% Duty Cycle) | 600 Peak | 230 | 25.0 | 74.6 | -18 |
| CW | 600 Avg. | 230 | 24.6 | 75.2 | -17 |

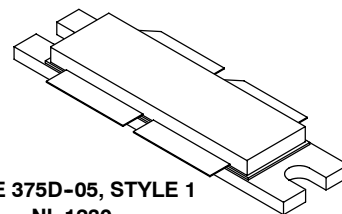
- Capable of Handling a Load Mismatch of 65:1 VSWR, @ 50 Vdc, 230 MHz, at all Phase Angles, Designed for Enhanced Ruggedness
 - 600 Watts Pulsed Peak Power, 20% Duty Cycle, 100 μ sec

Features

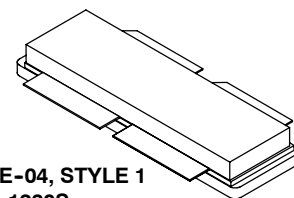
- Unmatched Input and Output Allowing Wide Frequency Range Utilization
- Device can be used Single-Ended or in a Push-Pull Configuration
- Qualified Up to a Maximum of 50 V_{DD} Operation
- Characterized from 30 V to 50 V for Extended Power Range
- Suitable for Linear Application with Appropriate Biasing
- Integrated ESD Protection with Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- RoHS Compliant
- In Tape and Reel. R6 Suffix = 150 Units, 56 mm Tape Width, 13 inch Reel. For R5 Tape and Reel options, see p. 12.

MRFE6VP5600HR6
MRFE6VP5600HSR6

1.8-600 MHz, 600 W CW, 50 V
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFETs



CASE 375D-05, STYLE 1
NI-1230
MRFE6VP5600HR6



CASE 375E-04, STYLE 1
NI-1230S
MRFE6VP5600HSR6

PARTS ARE PUSH-PULL

Table 1. Maximum Ratings

| Rating | Symbol | Value | Unit |
|-------------------------------------------------------------------------------|-----------|--------------|---------------------|
| Drain-Source Voltage | V_{DSS} | -0.5, +130 | Vdc |
| Gate-Source Voltage | V_{GS} | -6.0, +10 | Vdc |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^{\circ}C$ |
| Case Operating Temperature | T_C | 150 | $^{\circ}C$ |
| Total Device Dissipation @ $T_C = 25^{\circ}C$ Derate above 25 $^{\circ}C$ | P_D | 1667 8.33 | W W/ $^{\circ}C$ |
| Operating Junction Temperature (1,2) | T_J | 225 | $^{\circ}C$ |

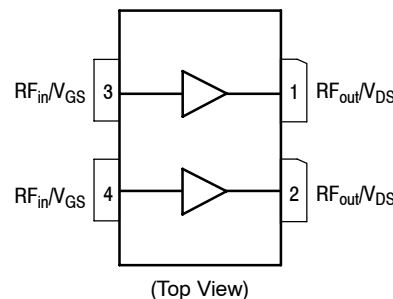


Figure 1. Pin Connections

Table 2. Thermal Characteristics

| Characteristic | Symbol | Value (2,3) | Unit |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------|---------------|---------------|
| Thermal Resistance, Junction to Case Case Temperature 68 $^{\circ}C$, 600 W Pulsed, 100 μ sec Pulse Width, 20% Duty Cycle, 100 mA, 230 MHz Case Temperature 60 $^{\circ}C$, 600 W CW, 100 mA, 230 MHz | $Z_{\theta JC}$ $R_{\theta JC}$ | 0.022 0.12 | $^{\circ}C/W$ |

- Continuous use at maximum temperature will affect MTTF.
- MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
- Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

Table 3. ESD Protection Characteristics

| Test Methodology | Class |
|---------------------------------------|--------------|
| Human Body Model (per JESD22-A114) | 2 (Minimum) |
| Machine Model (per EIA/JESD22-A115) | B (Minimum) |
| Charge Device Model (per JESD22-C101) | IV (Minimum) |

Table 4. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

Off Characteristics ⁽¹⁾

| | | | | | |
|----------------------------------------------------------------------------------------------------|---------------|-----|---|----|---------------|
| Gate-Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$) | I_{GSS} | — | — | 1 | μA |
| Drain-Source Breakdown Voltage ($V_{GS} = 0\text{ Vdc}$, $I_D = 100\text{ mA}$) | $V_{(BR)DSS}$ | 130 | — | — | Vdc |
| Zero Gate Voltage Drain Leakage Current ($V_{DS} = 50\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$) | I_{DSS} | — | — | 10 | μA |
| Zero Gate Voltage Drain Leakage Current ($V_{DS} = 100\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$) | I_{DSS} | — | — | 20 | μA |

On Characteristics

| | | | | | |
|-------------------------------------------------------------------------------------------------------------|--------------|-----|------|-----|-----|
| Gate Threshold Voltage ⁽¹⁾ ($V_{DS} = 10\text{ Vdc}$, $I_D = 960\ \mu\text{A}$) | $V_{GS(th)}$ | 1.7 | 2.2 | 2.7 | Vdc |
| Gate Quiescent Voltage ($V_{DD} = 50\text{ Vdc}$, $I_D = 100\text{ mA}$, Measured in Functional Test) | $V_{GS(Q)}$ | 2.0 | 2.5 | 3.0 | Vdc |
| Drain-Source On-Voltage ⁽¹⁾ ($V_{GS} = 10\text{ Vdc}$, $I_D = 2\text{ A}$) | $V_{DS(on)}$ | — | 0.26 | — | Vdc |

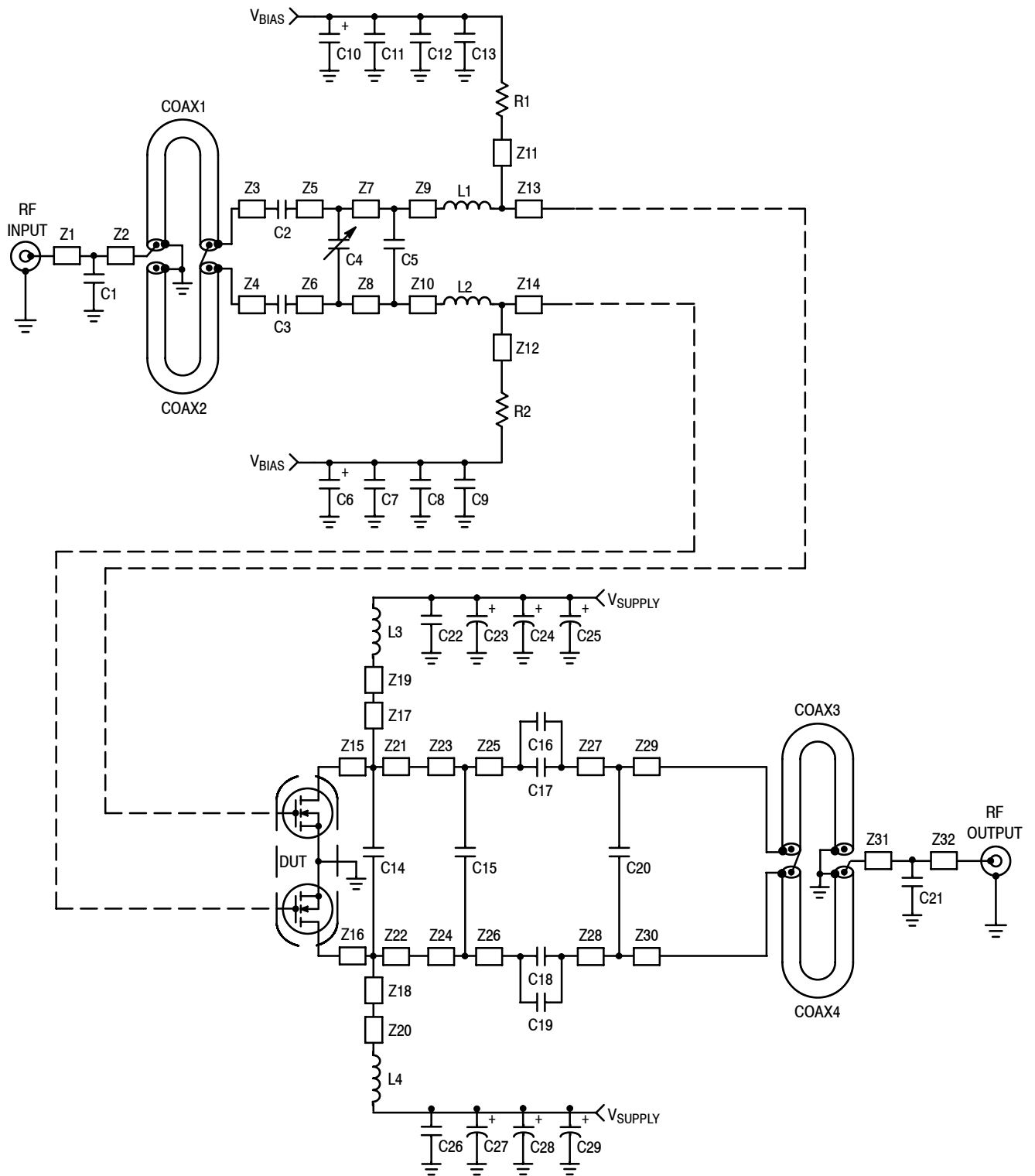
Dynamic Characteristics ⁽¹⁾

| | | | | | |
|------------------------------------------------------------------------------------------------------------------------|-----------|---|------|---|----|
| Reverse Transfer Capacitance ($V_{DS} = 50\text{ Vdc} \pm 30\text{ mV(rms)}$ ac @ 1 MHz, $V_{GS} = 0\text{ Vdc}$) | C_{rss} | — | 1.60 | — | pF |
| Output Capacitance ($V_{DS} = 50\text{ Vdc} \pm 30\text{ mV(rms)}$ ac @ 1 MHz, $V_{GS} = 0\text{ Vdc}$) | C_{oss} | — | 129 | — | pF |
| Input Capacitance ($V_{DS} = 50\text{ Vdc}$, $V_{GS} = 0\text{ Vdc} \pm 30\text{ mV(rms)}$ ac @ 1 MHz) | C_{iss} | — | 342 | — | pF |

Functional Tests (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 50\text{ Vdc}$, $I_{DQ} = 100\text{ mA}$, $P_{out} = 600\text{ W Peak}$ (120 W Avg.), $f = 230\text{ MHz}$, Pulsed, 100 μsec Pulse Width, 20% Duty Cycle

| | | | | | |
|-------------------|----------|------|------|------|----|
| Power Gain | G_{ps} | 23.5 | 25.0 | 26.5 | dB |
| Drain Efficiency | η_D | 73.5 | 74.6 | — | % |
| Input Return Loss | IRL | — | -18 | -12 | dB |

1. Each side of device measured separately.



| | | | | | |
|---------|----------------------------|------------|----------------------------|----------|----------------------------|
| Z1 | 0.192" x 0.082" Microstrip | Z11*, Z12* | 0.872" x 0.058" Microstrip | Z23, Z24 | 1.251" x 0.300" Microstrip |
| Z2 | 0.175" x 0.082" Microstrip | Z13, Z14 | 0.412" x 0.726" Microstrip | Z25, Z26 | 0.127" x 0.300" Microstrip |
| Z3, Z4 | 0.170" x 0.100" Microstrip | Z15, Z16 | 0.371" x 0.507" Microstrip | Z27, Z28 | 0.058" x 0.300" Microstrip |
| Z5, Z6 | 0.116" x 0.285" Microstrip | Z17*, Z18* | 0.466" x 0.363" Microstrip | Z29, Z30 | 0.058" x 0.300" Microstrip |
| Z7, Z8 | 0.116" x 0.285" Microstrip | Z19*, Z20* | 1.187" x 0.154" Microstrip | Z31 | 0.186" x 0.082" Microstrip |
| Z9, Z10 | 0.108" x 0.285" Microstrip | Z21, Z22 | 0.104" x 0.507" Microstrip | Z32 | 0.179" x 0.082" Microstrip |

* Line length includes microstrip bends

Figure 1. MRFE6VP5600HR6(HSR6) Test Circuit Schematic - Pulsed

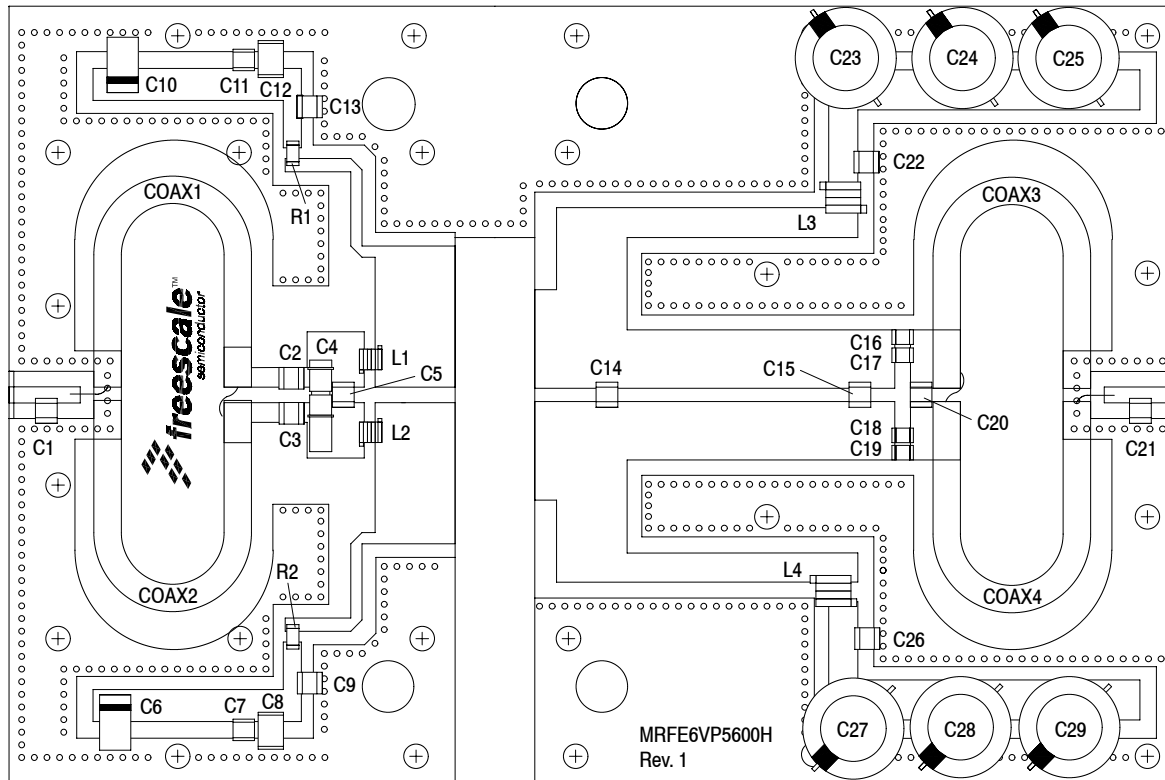
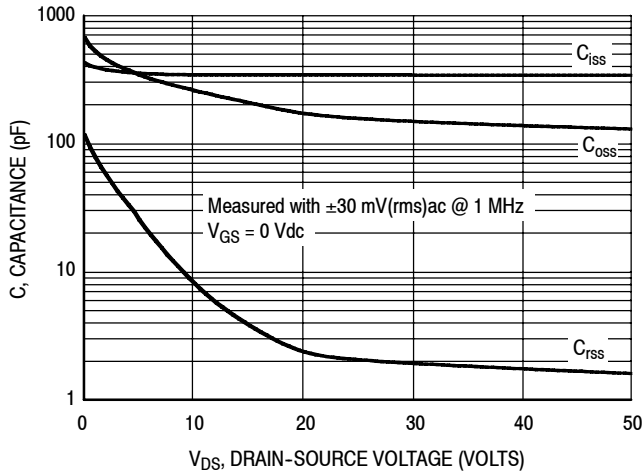


Figure 2. MRFE6VP5600HR6(HSR6) Test Circuit Component Layout - Pulsed

Table 5. MRFE6VP5600HR6(HSR6) Test Circuit Component Designations and Values - Pulsed

| Part | Description | Part Number | Manufacturer |
|------------------------------|-------------------------------------------|----------------------|--------------|
| C1 | 12 pF Chip Capacitor | ATC100B120JT500XT | ATC |
| C2, C3 | 27 pF Chip Capacitors | ATC100B270JT500XT | ATC |
| C4 | 0.8–8.0 pF Variable Capacitor, Gigatrim | 27291SL | Johanson |
| C5 | 33 pF Chip Capacitor | ATC100B330JT500XT | ATC |
| C6, C10 | 22 μ F, 35 V Tantalum Capacitors | T491X226K035AT | Kemet |
| C7, C11 | 0.1 μ F Chip Capacitors | CDR33BX104AKYS | AVX |
| C8, C12 | 220 nF Chip Capacitors | C1812C224K5RACTU | Kemet |
| C9, C13, C22, C26 | 1000 pF Chip Capacitors | ATC100B102JT50XT | ATC |
| C14 | 36 pF Chip Capacitor | ATC100B360JT500XT | ATC |
| C15 | 51 pF Chip Capacitor | ATC100B510GT500XT | ATC |
| C16, C17, C18, C19 | 240 pF Chip Capacitors | ATC100B241JT200XT | ATC |
| C20 | 39 pF Chip Capacitor | ATC100B390JT500XT | ATC |
| C21 | 10 pF Chip Capacitor | ATC100B100JT500XT | ATC |
| C23, C24, C25, C27, C28, C29 | 470 μ F, 63 V Electrolytic Capacitors | MCGPR63V477M13X26-RH | Multicomp |
| Coax1, 2, 3, 4 | 25 Ω Semi Rigid Coax, 2.2" Long | UT-141C-25 | Micro Coax |
| L1, L2 | 5 nH Inductors | A02TKLC | Coilcraft |
| L3, L4 | 6.6 nH Inductors | GA3093-ALC | Coilcraft |
| R1, R2 | 10 Ω Chip Resistors | CRCW120610R0JNEA | Vishay |
| PCB | 0.030", $\epsilon_r = 2.55$ | AD255A | Arlon |

TYPICAL CHARACTERISTICS



Note: Each side of device measured separately.

Figure 3. Capacitance versus Drain-Source Voltage

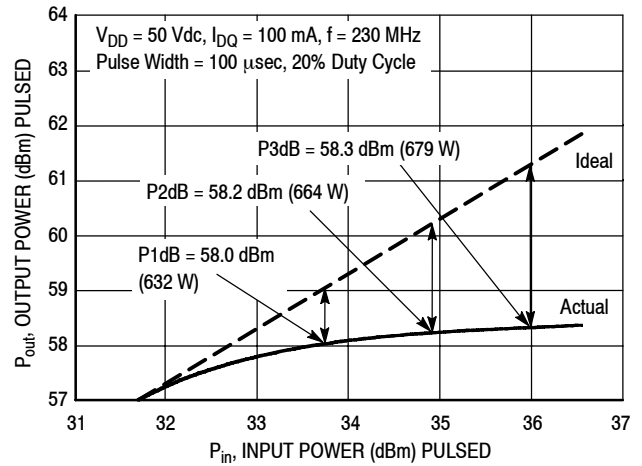


Figure 4. Pulsed Output Power versus Input Power

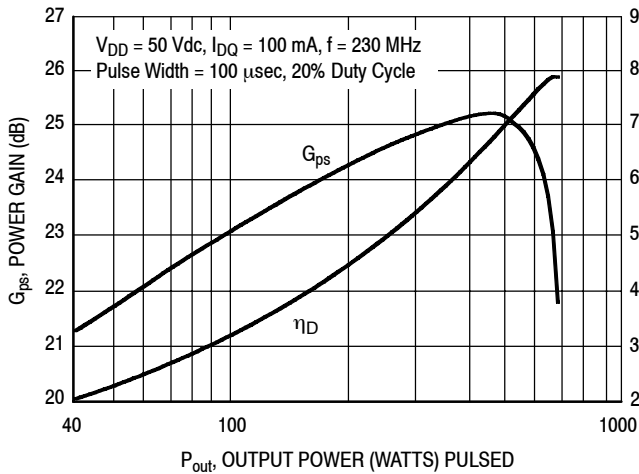


Figure 5. Pulsed Power Gain and Drain Efficiency versus Output Power

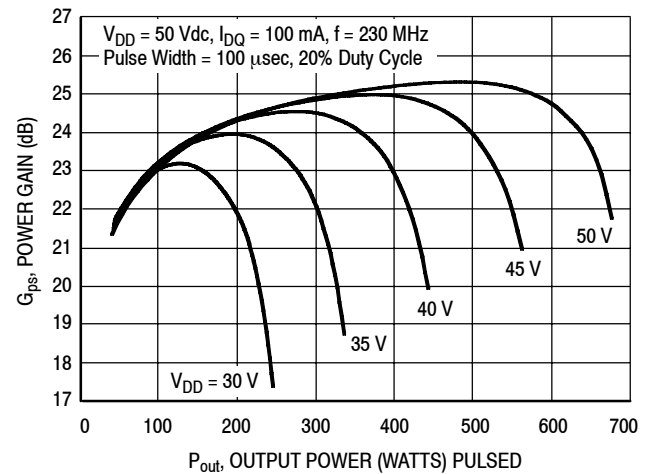


Figure 6. Pulsed Power Gain versus Output Power

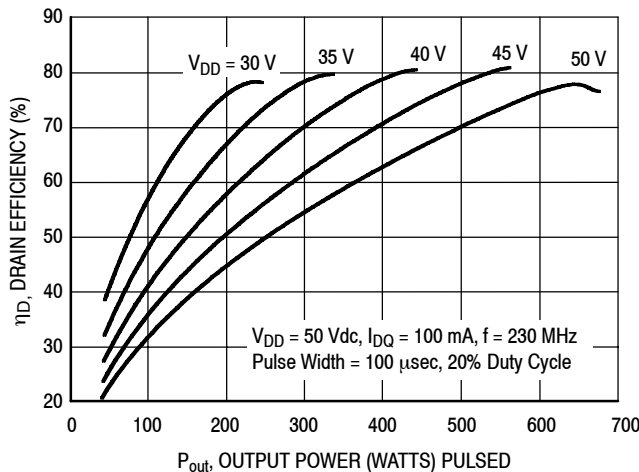


Figure 7. Pulsed Drain Efficiency versus Output Power

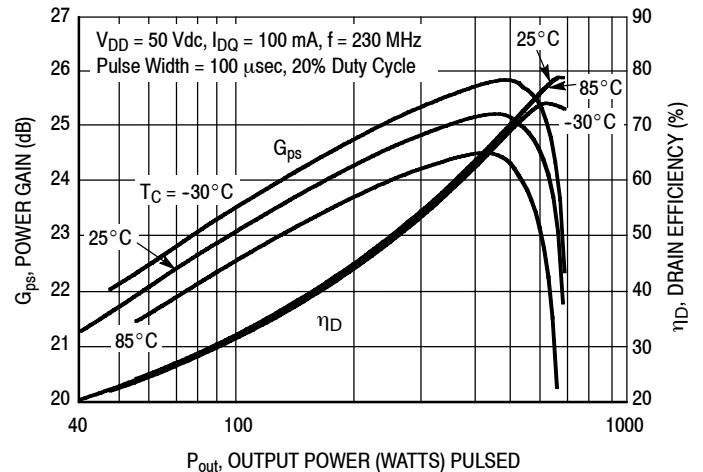
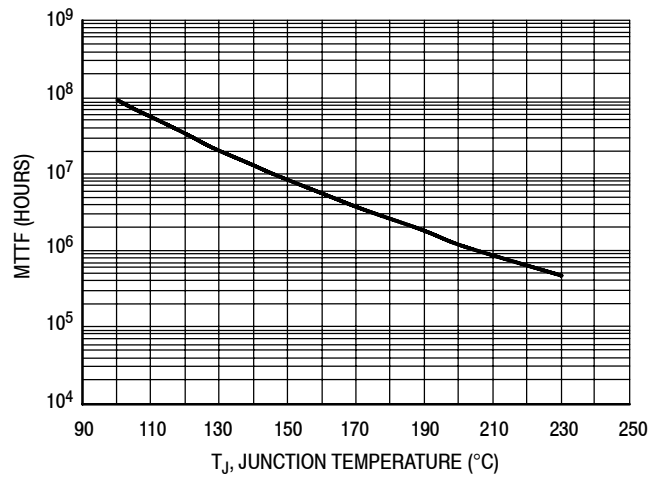


Figure 8. Pulsed Power Gain and Drain Efficiency versus Output Power

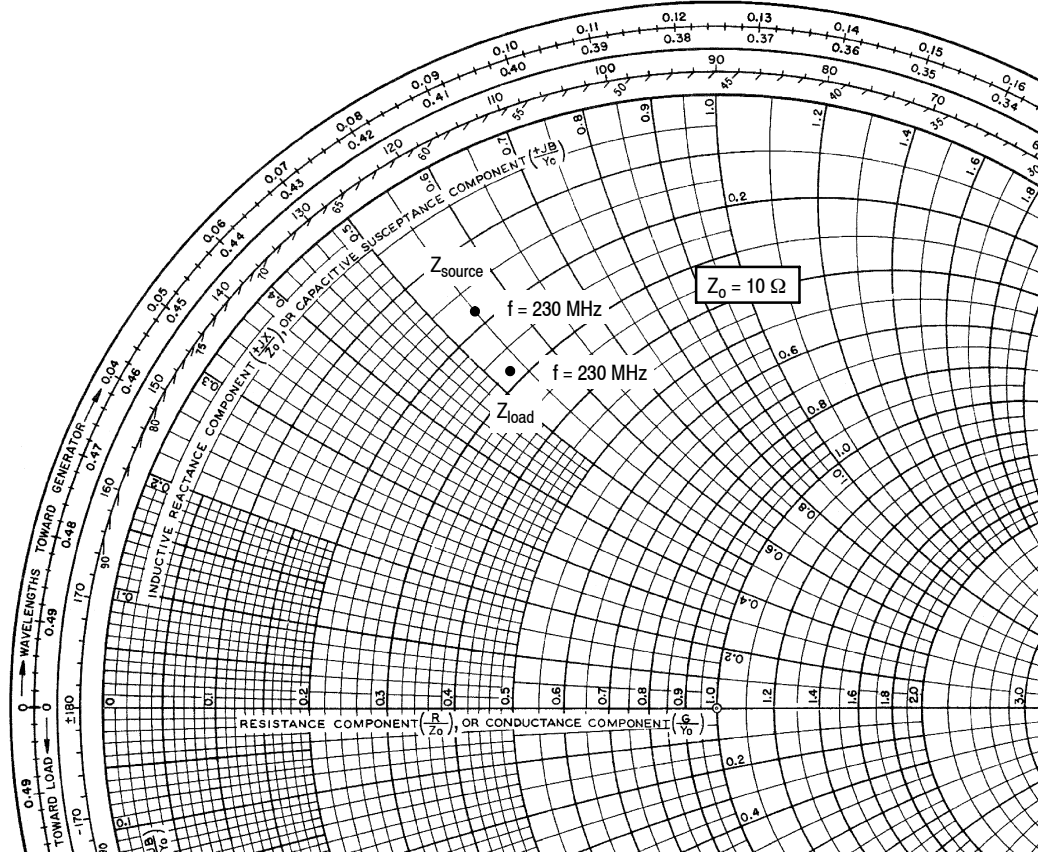
TYPICAL CHARACTERISTICS



This above graph displays calculated MTTF in hours when the device is operated at $V_{DD} = 50 \text{ Vdc}$, $P_{out} = 600 \text{ W Avg.}$, and $\eta_D = 75.2\%$.

MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

Figure 9. MTTF versus Junction Temperature — CW



$V_{DD} = 50 \text{ Vdc}$, $I_{DQ} = 100 \text{ mA}$, $P_{out} = 600 \text{ W Peak}$

| f MHz | Z_{source} Ω | Z_{load} Ω |
|----------|--------------------------|------------------------|
| 230 | $1.78 + j5.45$ | $2.75 + j5.30$ |

Z_{source} = Test circuit impedance as measured from gate to gate, balanced configuration.

Z_{load} = Test circuit impedance as measured from drain to drain, balanced configuration.

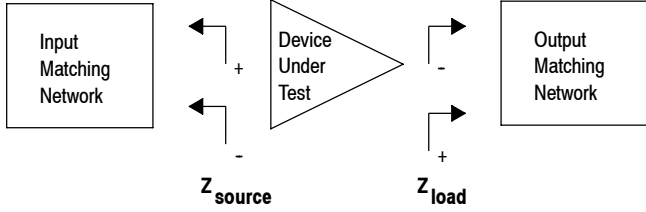
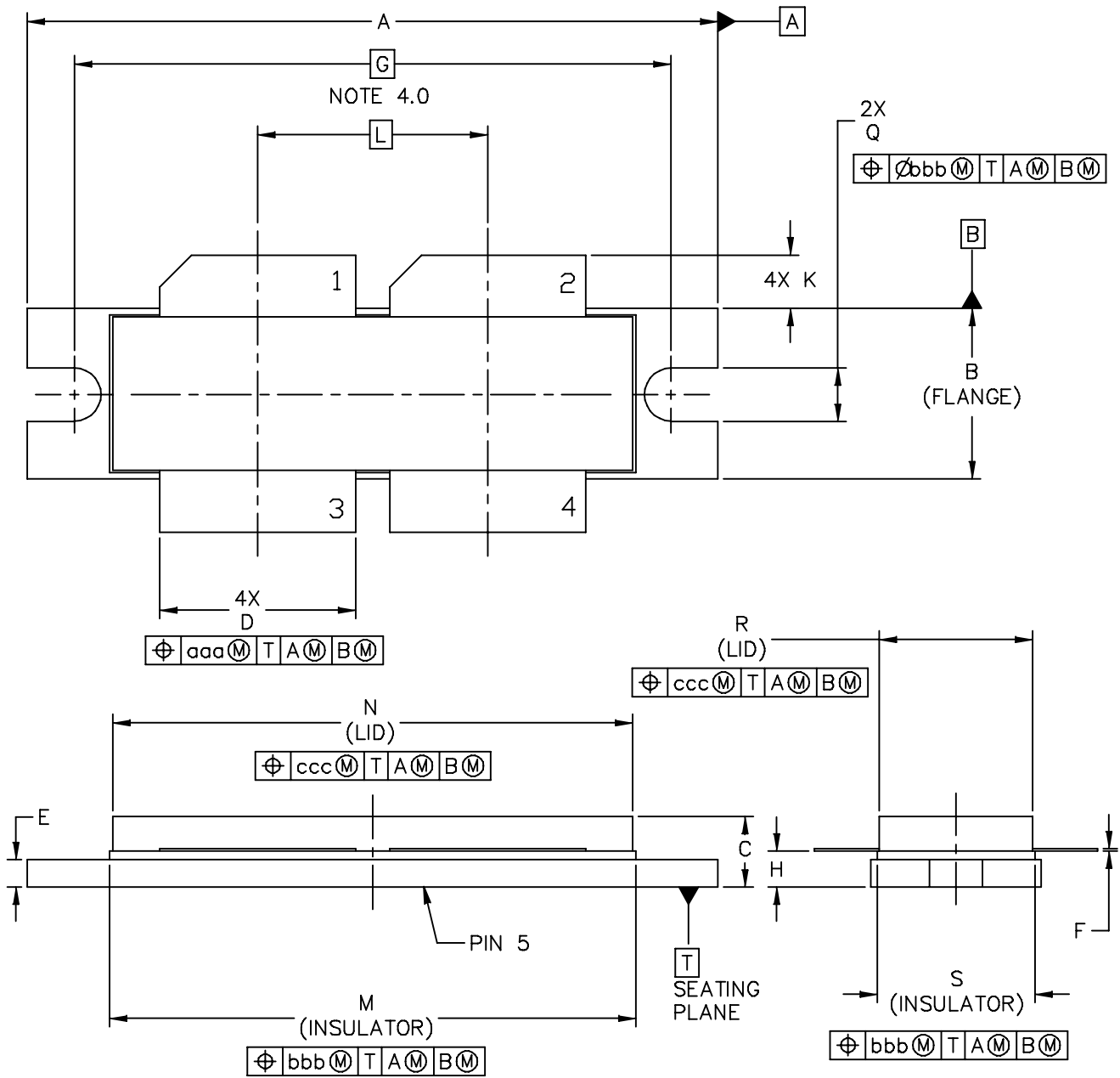


Figure 10. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS



| | | |
|---------------------------------------------------------|--------------------------|----------------------------|
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| TITLE: NI-1230 | DOCUMENT NO: 98ASB16977C | REV: E |
| | CASE NUMBER: 375D-05 | 31 MAR 2005 |
| | STANDARD: NON-JEDEC | |

NOTES:

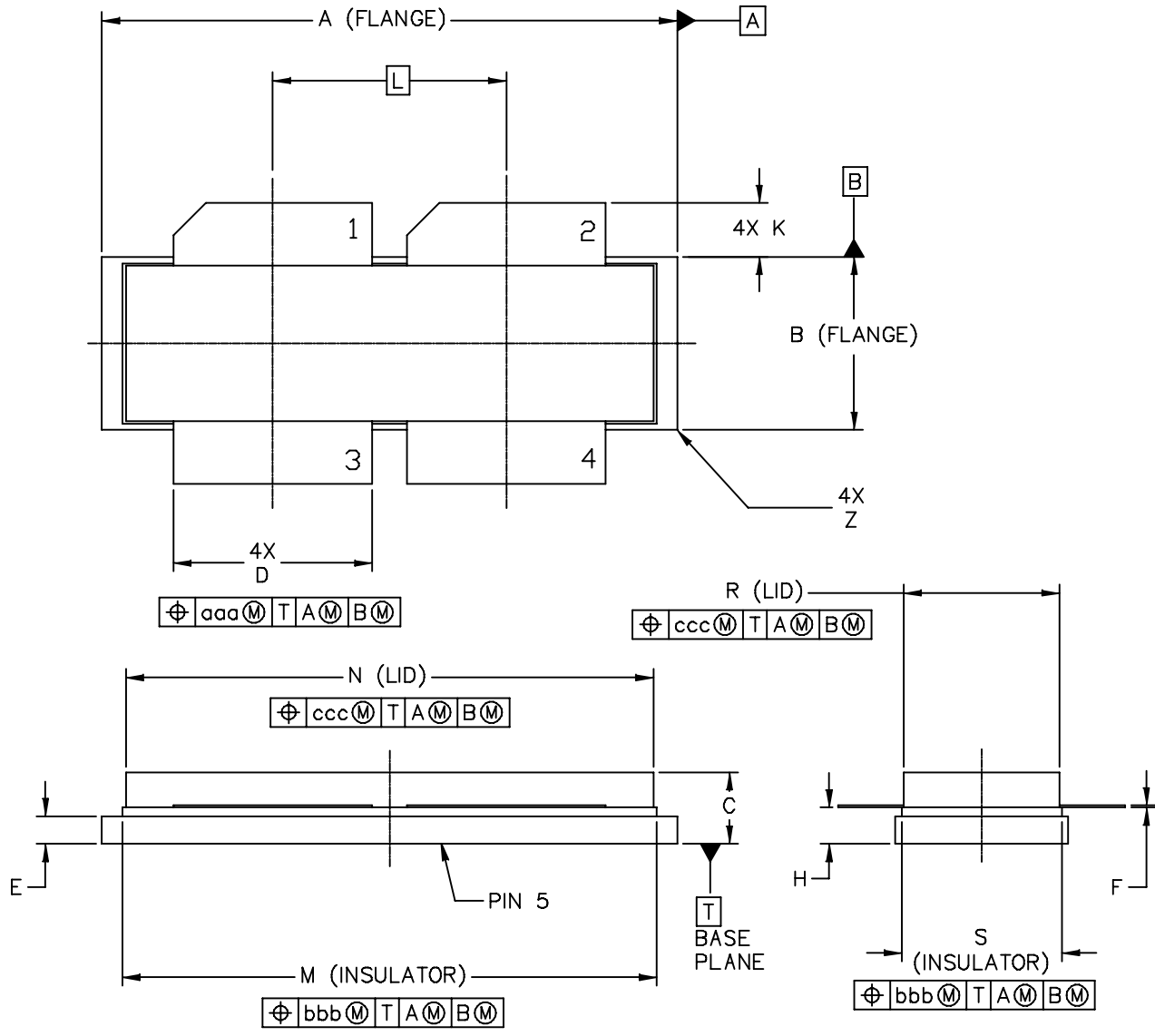
- 1.0 INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
- 2.0 CONTROLLING DIMENSION: INCH
- 3.0 DIMENSION H IS MEASURED .030 (0.762) AWAY FROM PACKAGE BODY.
- 4.0 RECOMMENDED BOLT CENTER DIMENSION OF 1.52 (38.61) BASED ON M3 SCREW.

STYLE 1:

- PIN 1 - DRAIN
- 2 - DRAIN
- 3 - GATE
- 4 - GATE
- 5 - SOURCE

| DIM | INCH | | MILLIMETER | | DIM | INCH | | MILLIMETER | |
|-----|-----------|-------|------------|-------|-----|-------|-------|------------|-------|
| | MIN | MAX | MIN | MAX | | MIN | MAX | MIN | MAX |
| A | 1.615 | 1.625 | 41.02 | 41.28 | N | 1.218 | 1.242 | 30.94 | 31.55 |
| B | .395 | .405 | 10.03 | 10.29 | Q | .120 | .130 | 3.05 | 3.3 |
| C | .150 | .200 | 3.81 | 5.08 | R | .355 | .365 | 9.01 | 9.27 |
| D | .455 | .465 | 11.56 | 11.81 | S | .365 | .375 | 9.27 | 9.53 |
| E | .062 | .066 | 1.57 | 1.68 | | | | | |
| F | .004 | .007 | 0.1 | 0.18 | | | | | |
| G | 1.400 BSC | | 35.56 BSC | | aaa | .013 | | 0.33 | |
| H | .082 | .090 | 2.08 | 2.29 | bbb | .010 | | 0.25 | |
| K | .117 | .137 | 2.97 | 3.48 | ccc | .020 | | 0.51 | |
| L | .540 BSC | | 13.72 BSC | | | | | | |
| M | 1.219 | 1.241 | 30.96 | 31.52 | | | | | |

| | | | |
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| | CASE NUMBER: 375E-04 | 05 AUG 2005 | |
| | STANDARD: NON-JEDEC | | |

NOTES:

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH
3. DIMENSION H IS MEASURED .030 AWAY FROM PACKAGE BODY

STYLE 1:

- PIN 1 - DRAIN
- 2 - DRAIN
- 3 - GATE
- 4 - GATE
- 5 - SOURCE

| DIM | INCHES | | MILLIMETERS | | DIM | INCHES | | MILLIMETERS | |
|---------------------------------------------------------|----------|-------|--------------------|-------|--------------------------|----------------------------|------|-------------|------|
| | MIN | MAX | MIN | MAX | | MIN | MAX | MIN | MAX |
| A | 1.265 | 1.275 | 32.13 | 32.38 | R | .355 | .365 | 9.01 | 9.27 |
| B | .395 | .405 | 10.03 | 10.29 | S | .365 | .375 | 9.27 | 9.53 |
| C | .150 | .200 | 3.81 | 5.08 | Z | --- | .040 | --- | 1.02 |
| D | .455 | .465 | 11.56 | 11.81 | | | | | |
| E | .062 | .066 | 1.57 | 1.68 | aaa | .013 | | 0.33 | |
| F | .004 | .007 | 0.1 | 0.18 | bbb | .010 | | 0.25 | |
| H | .082 | .090 | 2.08 | 2.29 | ccc | .020 | | 0.51 | |
| K | .117 | .137 | 2.97 | 3.48 | | | | | |
| L | .540 BSC | | 13.72 BSC | | | | | | |
| M | 1.219 | 1.241 | 30.96 | 31.52 | | | | | |
| N | 1.218 | 1.242 | 30.94 | 31.55 | | | | | |
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| | | | | | CASE NUMBER: 375E-04 | | | 05 AUG 2005 | |
| | | | | | STANDARD: NON-JEDEC | | | | |

PRODUCT DOCUMENTATION AND SOFTWARE

Refer to the following documents and software to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

For Software, do a Part Number search at <http://www.freescale.com>, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

R5 TAPE AND REEL OPTION

R5 Suffix = 50 Units, 56 mm Tape Width, 13 inch Reel.

The R5 tape and reel option for MRFE6VP5600H and MRFE6VP5600HS parts will be available for 2 years after release of MRFE6VP5600H and MRFE6VP5600HS. Freescale Semiconductor, Inc. reserves the right to limit the quantities that will be delivered in the R5 tape and reel option. At the end of the 2 year period customers who have purchased these devices in the R5 tape and reel option will be offered MRFE6VP5600H and MRFE6VP5600HS in the R6 tape and reel option.

REVISION HISTORY

The following table summarizes revisions to this document.

| Revision | Date | Description |
|----------|-----------|----------------------------------------------------------------------------------------------------|
| 0 | Dec. 2010 | • Initial Release of Data Sheet |
| 1 | Jan. 2011 | • Fig. 1, Pin Connections, corrected pin 4 label from RF_{out}/V_{GS} to RF_{in}/V_{GS} . p. 1 |

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