



THE DATASHEET OF NCP1280DR2



NCP1280

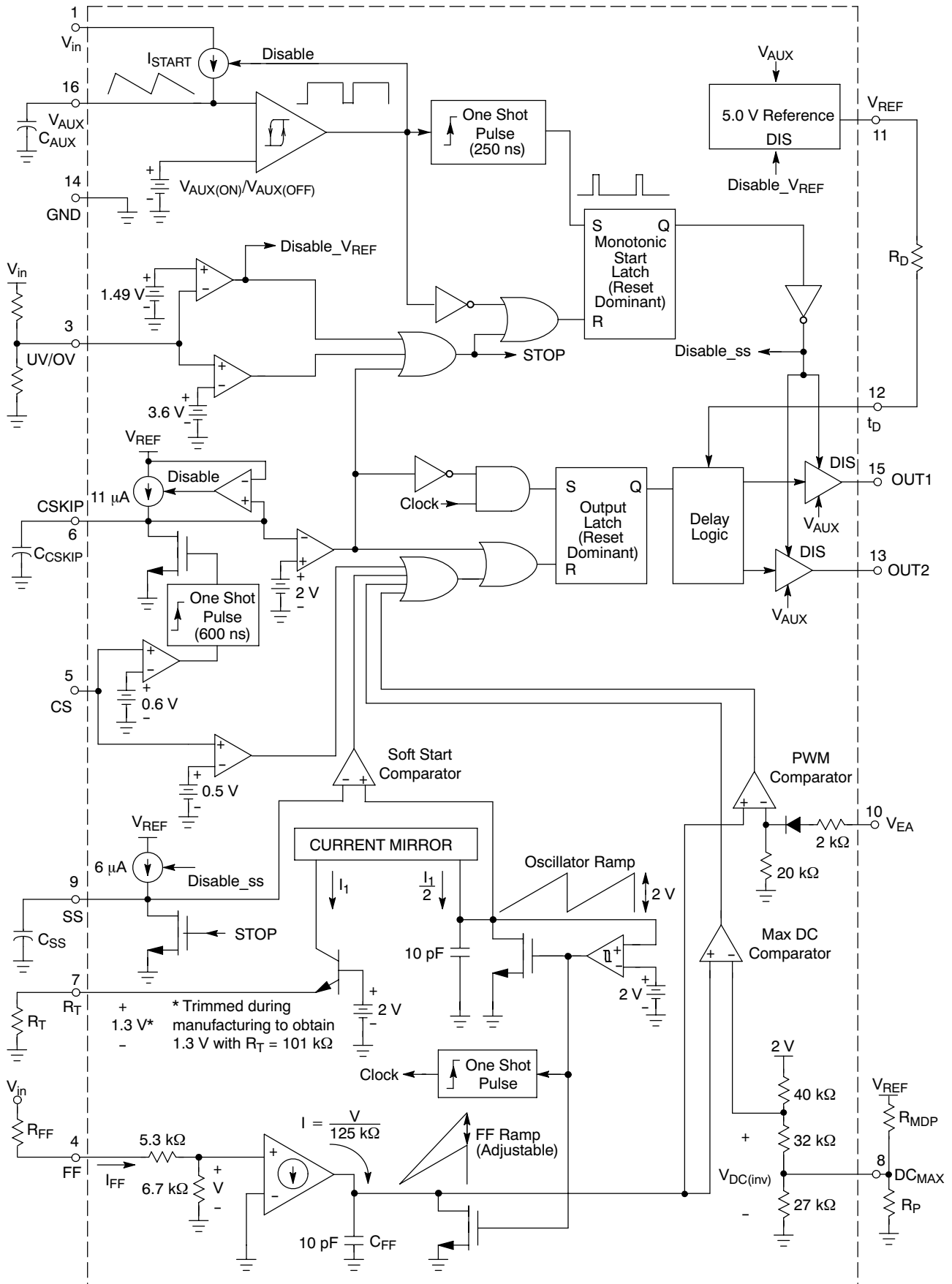


Figure 2. NCP1280 Functional Block Diagram

NCP1280

PIN DESCRIPTION

Pin	Name	Application Information
1	V_{in}	This pin is connected to the input voltage of the system. The voltage can be a rectified, filtered line voltage or output of a power factor correction (PFC) front end. A constant current source supplies current from this pin to the capacitor connected on the V_{AUX} pin. The charge current is typically 13.8 mA. Maximum input voltage is 700 V.
2	NC	Not Connected.
3	UV/OV	Provides protection under line undervoltage and overvoltage conditions. The built in voltage range is ~ 2:1. If needed, the OV function can be disabled by a Zener from this pin to ground.
4	FF	An external resistor between V_{in} and this pin adjusts the amplitude of the Feedforward Ramp in proportion to V_{in} . By varying the feedforward ramp amplitude in proportion to the input voltage, open loop line regulation is improved.
5	CS	Overcurrent sense input. If the CS voltage exceeds 0.48 V or 0.57 V, the converter enters the Cycle by Cycle or Cycle Skip current limit mode, respectively.
6	CSKIP	The capacitor connected between this pin and ground sets the Cycle Skip period. A soft-start sequence follows at the conclusion of the fault period.
7	R_T	A single external resistor between this pin and GND sets the oscillator fixed frequency.
8	DC_{MAX}	An external resistor between this pin and GND sets the voltage on the Max DC Comparator inverting input. The duty cycle is limited by comparing the voltage on the Max DC Comparator inverting input to the Feedforward Ramp.
9	SS	An internal 6.2 μ A current source charges the external capacitor connected to this pin. The duty cycle is limited during startup by comparing the voltage on this pin to the Oscillator Ramp.
10	V_{EA}	The error signal from an external error amplifier, typically supplied through an optocoupler, is fed into this input and compared to the Feedforward Ramp. A series diode and resistor offset the voltage on this pin before it is applied to the PWM Comparator inverting input.
11	V_{REF}	Precision 5.0 V reference output. Maximum output current is 6 mA.
12	t_D	An external resistor between V_{REF} and this pin sets the overlap delay between OUT1 and OUT2 transitions.
13	OUT2	Output of the PWM controller with leading and trailing edge overlap delay. OUT2 can be used to drive a synchronous rectifier topology, an active clamp/reset switch, or both.
14	GND	Control circuit ground.
15	OUT1	Main output of the PWM controller.
16	V_{AUX}	Positive input supply voltage. This pin is connected to an external capacitor for energy storage. An internal current source supplies current from V_{in} to this pin. Once the voltage on V_{AUX} reaches 11 V, the current source turns OFF. It turns ON again once V_{AUX} falls to 7 V. During normal operation, power is supplied to the IC via this pin, by means of an auxiliary winding.

NCP1280

ORDERING INFORMATION

Device	Package	Shipping†
NCP1280DR2	SO-16	2500 / Tape & Reel
NCP1280DR2G	SO-16 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Input Line Voltage	V_{in}	-0.3 to 700	V
Auxiliary Supply Voltage	V_{AUX}	-0.3 to 18	V
Transient Auxiliary Supply Voltage (Duration < 10 ms, I_{AUX} < 10 mA)	$V_{AUX(transient)}$	-0.3 to 20	V
Auxiliary Supply Input Current	I_{AUX}	35	mA
OUT1 and OUT2 Voltage	V_{OUT}	-0.3 to ($V_{AUX} + 0.3$ V)	V
OUT1 and OUT2 Output Current	I_{OUT}	10	mA
5.0 V Reference Voltage	V_{REF}	-0.3 to 6.0	V
5.0 V Reference Output Current	I_{REF}	6.0	mA
All Other Inputs/Outputs Voltage	V_{IO}	-0.3 to V_{REF}	V
All Other Inputs/Outputs Current	I_{IO}	10	mA
Operating Junction Temperature	T_J	-40 to 125	°C
Storage Temperature Range	T_{stg}	-55 to 150	°C
Power Dissipation at $T_A = 25^\circ\text{C}$	P_D	0.77	W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	130	°C/W

1. Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

A. This device series contains ESD protection and exceeds the following tests:

Pin 1 is the HV startup of the device and is rated to the max rating of the part, or 700 V.

Machine Model Method 700 V.

Pins 2-16: Human Body Model 4000 V per MIL-STD-883, Method 3015.

Machine Model Method 200 V.

NCP1280

ELECTRICAL CHARACTERISTICS ($V_{in} = 82\text{ V}$, $V_{AUX} = 12\text{ V}$, $V_{EA} = 2\text{ V}$, $R_T = 101\text{ k}\Omega$, $C_{CSKIP} = 6800\text{ pF}$,
 $R_D = 60.4\text{ k}\Omega$, $R_{FF} = 1.0\text{ M}\Omega$, for typical values $T_J = 25^\circ\text{C}$, for min/max values, $T_J = -40^\circ\text{C}$ to 125°C , unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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STARTUP CONTROL AND V_{AUX} REGULATOR

V_{AUX} Regulation Startup Threshold/ V_{AUX} Regulation Peak (V_{AUX} increasing) Minimum Operating V_{AUX} Valley Voltage After Turn-On Hysteresis	$V_{AUX(ON)}$ $V_{AUX(OFF)}$ V_H	10.5 6.6 -	11.0 7.0 4.0	11.5 7.4 -	V
Minimum Startup Voltage (Pin 1) $I_{START} = 1.5\text{ mA}$, $V_{AUX} = V_{AUX(ON)} - 0.2\text{ V}$, $I_{REF} = 0\text{ A}$	$V_{START(min)}$	-	-	25	V
Startup Circuit Output Current $V_{AUX} = 0\text{ V}$ $T_J = 25^\circ\text{C}$ $T_J = -40^\circ\text{C}$ to 125°C $V_{AUX} = V_{AUX(ON)} - 0.2\text{ V}$ $T_J = 25^\circ\text{C}$ $T_J = -40^\circ\text{C}$ to 125°C	I_{START}	13 10	17.5 -	21 25	mA
Startup Circuit Off-State Leakage Current ($V_{in} = 700\text{ V}$) $T_J = 25^\circ\text{C}$ $T_J = -40^\circ\text{C}$ to 125°C	$I_{START(OFF)}$	- -	23 -	50 100	μA
Startup Circuit Breakdown Voltage (Note 2) $I_{START(OFF)} = 50\text{ }\mu\text{A}$, $T_J = 25^\circ\text{C}$	$V_{(BR)DS}$	700	-	-	V
Auxiliary Supply Current After V_{AUX} Turn-On Outputs Disabled $V_{EA} = 0\text{ V}$ $V_{UV/OV} = 0.7\text{ V}$ Outputs Enabled	I_{AUX1} I_{AUX2} I_{AUX3}	- - -	2.7 1.3 4.6	5.0 2.5 6.5	mA

LINE UNDER/OVERVOLTAGE DETECTOR

Undervoltage Threshold (V_{in} Increasing)	V_{UV}	1.40	1.52	1.64	V
Undervoltage Hysteresis	$V_{UV(H)}$	0.080	0.098	0.120	V
Overvoltage Threshold (V_{in} Increasing)	V_{OV}	3.47	3.61	3.75	V
Overvoltage Hysteresis	$V_{OV(H)}$	-	0.145	-	V
Undervoltage Propagation Delay to Output	t_{UV}	-	250	-	ns
Overvoltage Propagation Delay to Output	t_{OV}	-	160	-	ns

CURRENT LIMIT

Cycle by Cycle Threshold Voltage	I_{LIM1}	0.44	0.48	0.52	V
Propagation Delay to Output ($V_{EA} = 2.0\text{ V}$) $V_{CS} = I_{LIM1}$ to 2.0 V , measured when V_{OUT} reaches $0.5 V_{OH}$	t_{LIM}	-	90	150	ns
Cycle Skip Threshold Voltage	I_{LIM2}	0.54	0.57	0.62	V
Cycle Skip Charge Current ($V_{CSKIP} = 0\text{ V}$)	I_{CSKIP}	8.0	12.3	15	μA

2. Guaranteed by design only.

NCP1280

ELECTRICAL CHARACTERISTICS ($V_{in} = 82\text{ V}$, $V_{AUX} = 12\text{ V}$, $V_{EA} = 2\text{ V}$, $R_T = 101\text{ k}\Omega$, $C_{CSKIP} = 6800\text{ pF}$,
 $R_D = 60.4\text{ k}\Omega$, $R_{FF} = 1.0\text{ M}\Omega$, for typical values $T_J = 25^\circ\text{C}$, for min/max values, $T_J = -40^\circ\text{C}$ to 125°C , unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OSCILLATOR

Frequency ($R_T = 101\text{ k}\Omega$) $T_J = 25^\circ\text{C}$ $T_J = -40^\circ\text{C}$ to 125°C	f_{OSC1}	285 280	300 -	315 320	kHz
Frequency ($R_T = 220\text{ k}\Omega$, $V_{EA} = 1.0\text{ V}$) $T_J = 25^\circ\text{C}$ $T_J = -40^\circ\text{C}$ to 125°C	f_{OSC2}	142 140	150 -	158 160	kHz

MAXIMUM DUTY CYCLE COMPARATOR

Maximum Duty Cycle ($V_{EA} = 3.0\text{ V}$, $T_J = 25^\circ\text{C}$) $R_P = 0\ \Omega$, $R_{MDP} = \text{open}$ $R_P = \text{open}$, $R_{MDP} = \text{open}$	DC_{MAX}	57 75	62 80	66 85	%
Open Circuit Voltage	V_{DCMAX}	0.40	0.47	0.60	V

SOFT-START

Charge Current ($V_{SS} = 1.0\text{ V}$)	$I_{SS(C)}$	5.0	6.2	7.4	μA
Discharge Current ($V_{SS} = 5.0\text{ V}$, $V_{UV/OV} = 0\text{ V}$)	$I_{SS(D)}$	20	52.5	-	mA

PWM COMPARATOR

Input Resistance ($V_1 = 1.25\text{ V}$, $V_2 = 1.50\text{ V}$) $R_{IN(VEA)} = (V_2 - V_1)/(I_2 - I_1)$	$R_{IN(VEA)}$	8.0	22	60	k Ω
Lower Input Threshold	$V_{EA(L)}$	0.3	0.7	0.9	V
Delay to Output (from V_{OH} to $0.5\ V_{OH}$)	t_{PWM}	-	200	-	ns

5.0 V REFERENCE

Output Voltage ($I_{REF} = 0\text{ mA}$) $T_J = 25^\circ\text{C}$ $T_J = -40^\circ\text{C}$ to 125°C	V_{REF}	4.9 4.8	5.0 -	5.1 5.1	V
Load Regulation ($I_{REF} = 0$ to 6 mA)	$V_{REF(Load)}$	-	10	50	mV
Line Regulation ($V_{AUX} = 7.5$ to 16 V)	$V_{REF(Line)}$	-	50	100	mV

CONTROL OUTPUTS

Output Voltage ($I_{OUT} = 0\text{ mA}$) Low State High State	V_{OL} V_{OH}	- -	0.25 11.8	- -	V
Overlap Delay $R_D = 1\text{ M}\Omega$ Leading Trailing $R_D = 60\text{ k}\Omega$ Leading Trailing	t_D	- - 50 32	200 170 90 72	- - 130 130	ns
Drive Resistance ($V_{in} = 15\text{ V}$) Sink ($V_{EA} = 0\text{ V}$, $V_{OUT} = 2\text{ V}$) Source ($V_{EA} = 3\text{ V}$, $V_{OUT} = 10\text{ V}$)	R_{SNK} R_{SRC}	20 50	40 90	80 170	Ω
Rise Time ($C_L = 100\text{ pF}$, 10% to 90% of V_{OH})	t_{on}	-	30	-	ns
Fall Time ($C_L = 100\text{ pF}$, 90% to 10% of V_{OH})	t_{off}	-	12	-	ns

TYPICAL CHARACTERISTICS

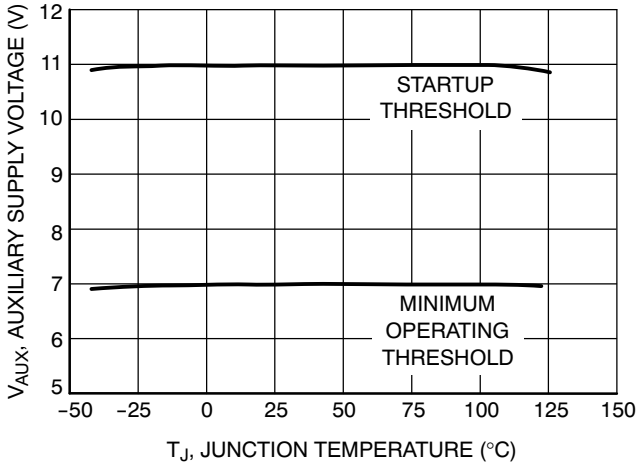


Figure 3. Auxiliary Supply Voltage Thresholds versus Junction Temperature

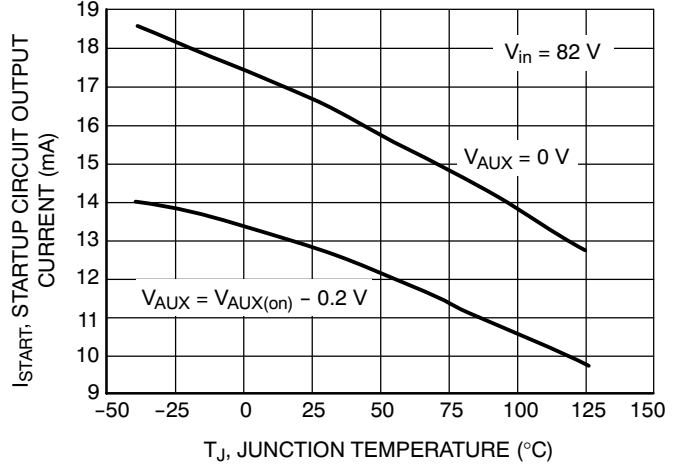


Figure 4. Startup Circuit Output Current versus Junction Temperature

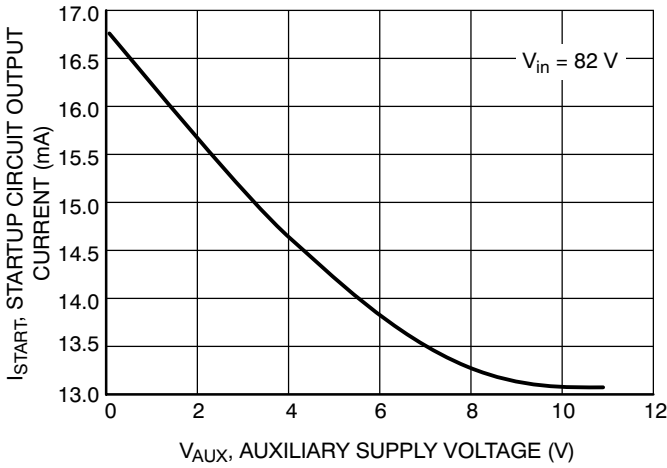


Figure 5. Startup Circuit Output Current versus Auxiliary Supply Voltage

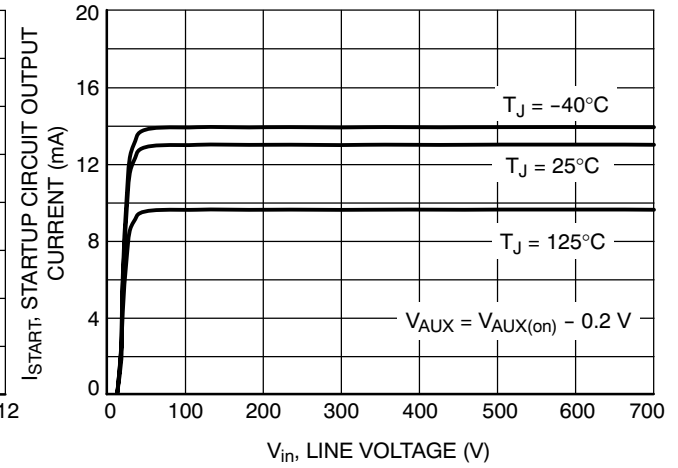


Figure 6. Startup Circuit Output Current versus Line Voltage

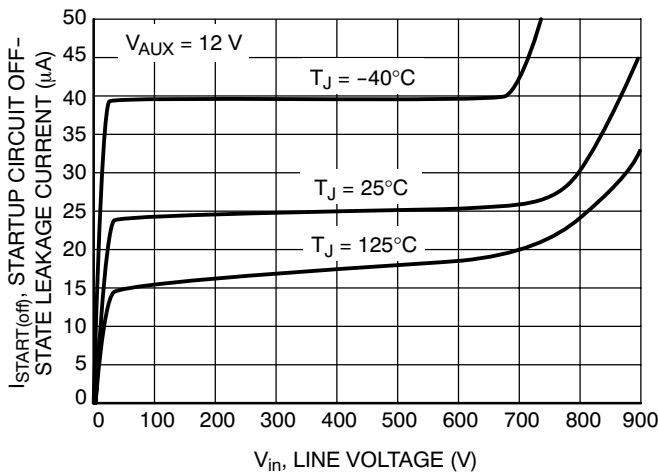


Figure 7. Startup Circuit Off-State Leakage Current versus Line Voltage

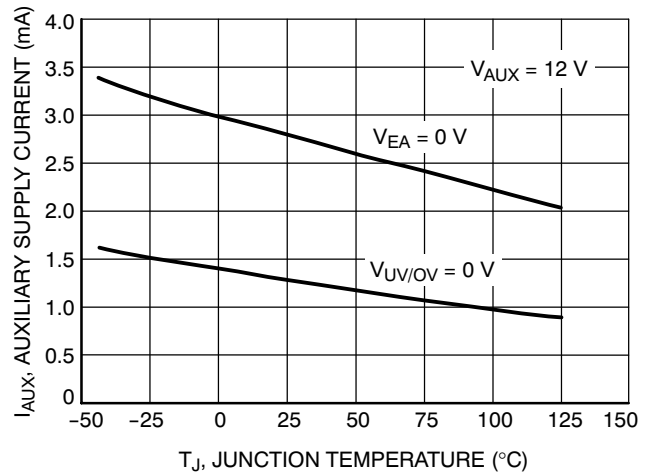


Figure 8. Auxiliary Supply Current versus Junction Temperature

TYPICAL CHARACTERISTICS

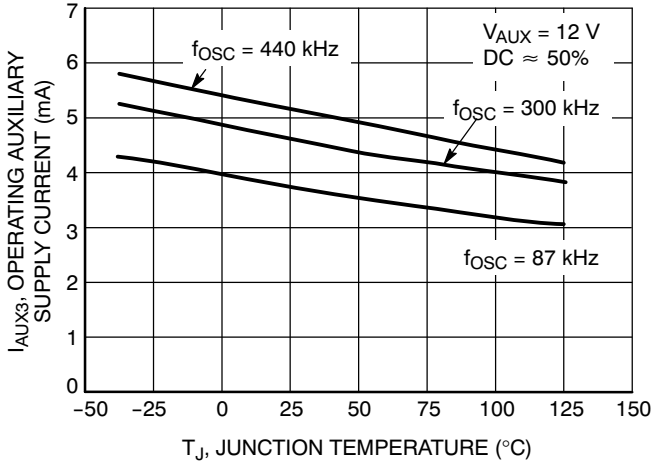


Figure 9. Operating Auxiliary Supply Current versus Junction Temperature

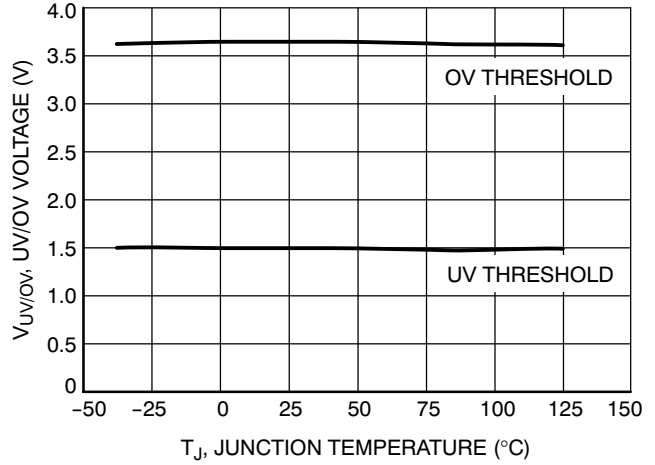


Figure 10. Line Under/Overshoot Thresholds versus Junction Temperature

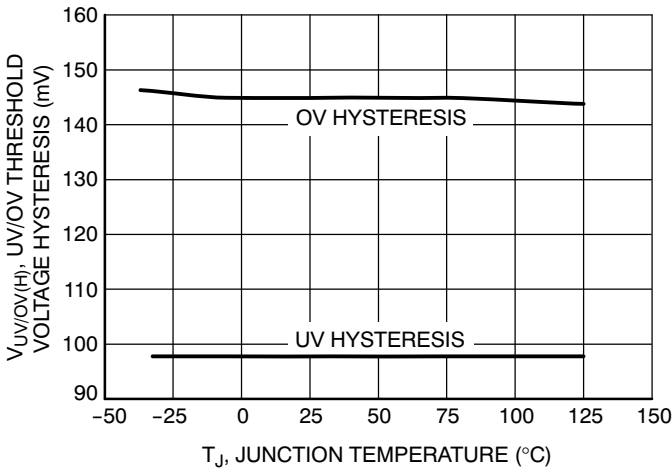


Figure 11. Line Under/Overshoot Thresholds Hysteresis versus Junction Temperature

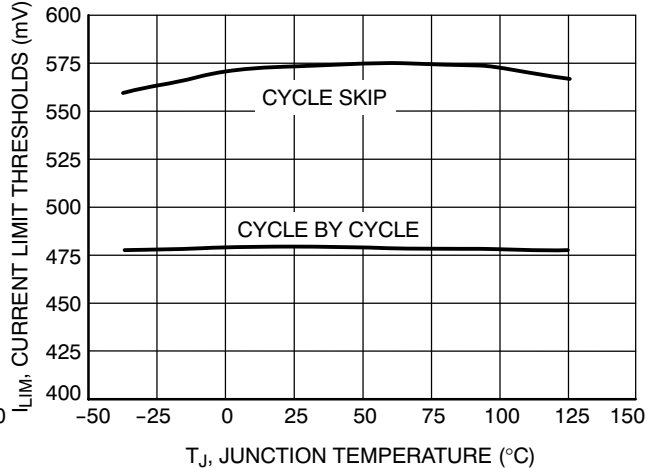


Figure 12. Current Limit Thresholds versus Junction Temperature

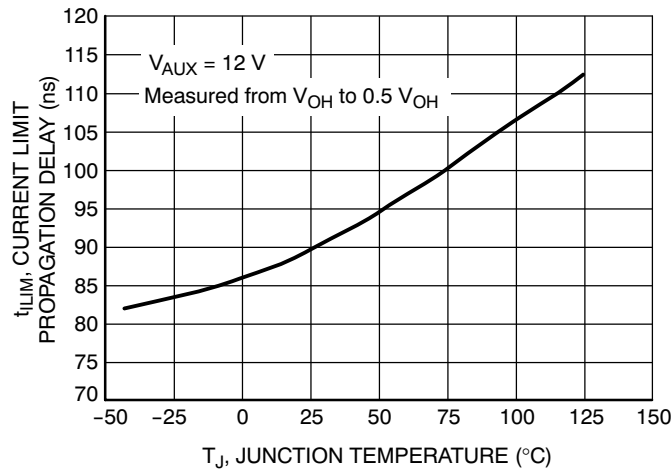


Figure 13. Current Limit Propagation Delay versus Junction Temperature

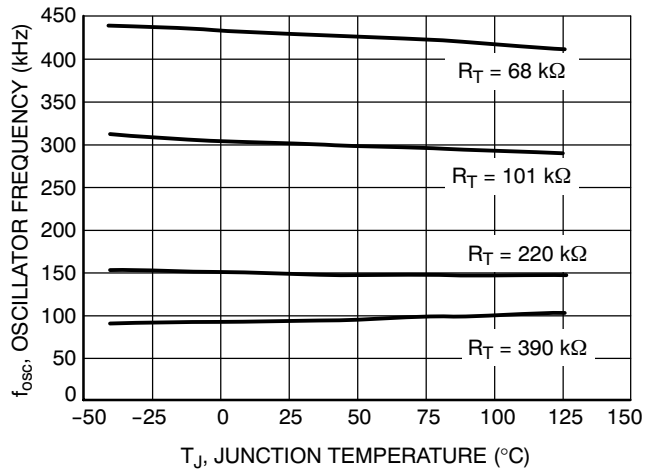


Figure 14. Oscillator Frequency versus Junction Temperature

TYPICAL CHARACTERISTICS

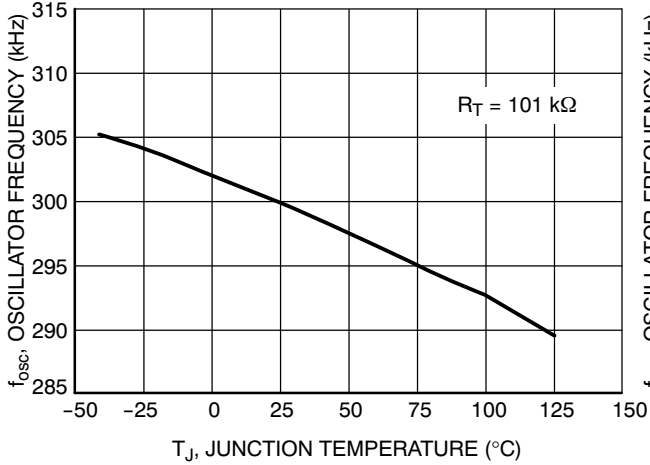


Figure 15. Oscillator Frequency versus Junction Temperature

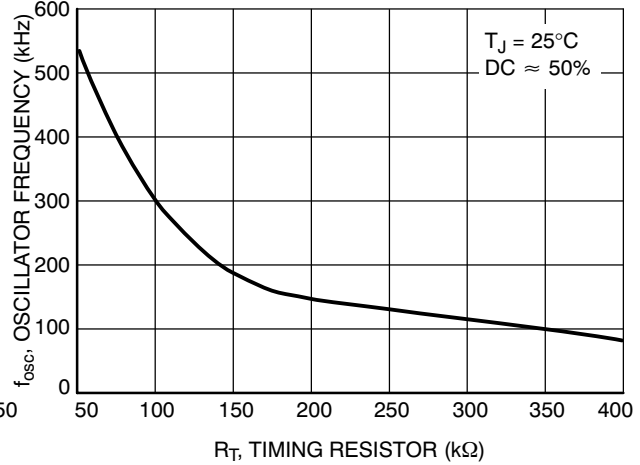


Figure 16. Oscillator Frequency versus Timing Resistor

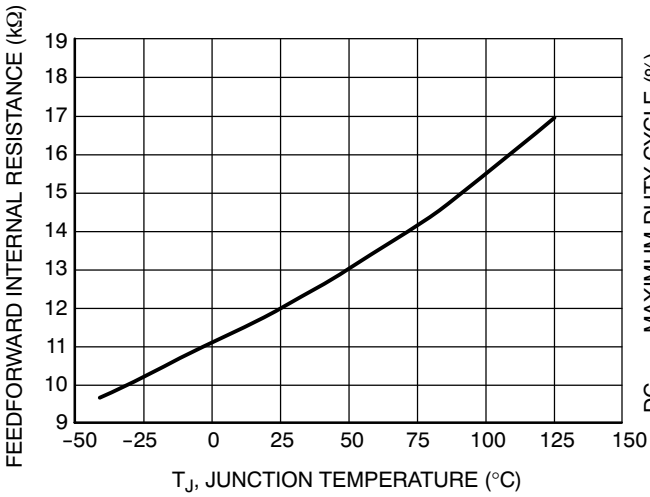


Figure 17. Feedforward Internal Resistance versus Junction Temperature

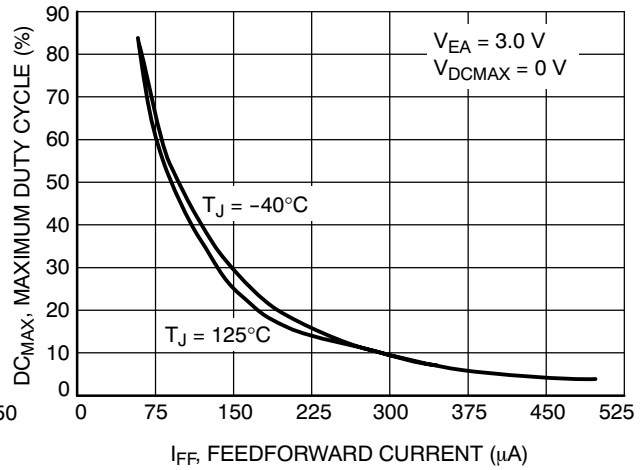


Figure 18. Maximum Duty Cycle versus Feedforward Current

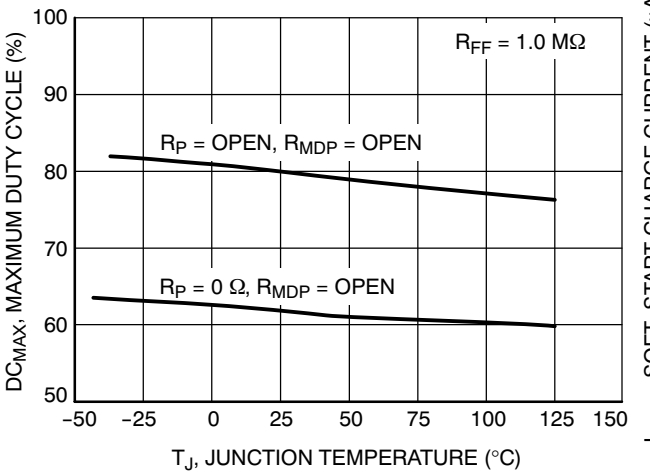


Figure 19. Maximum Duty Cycle versus Junction Temperature

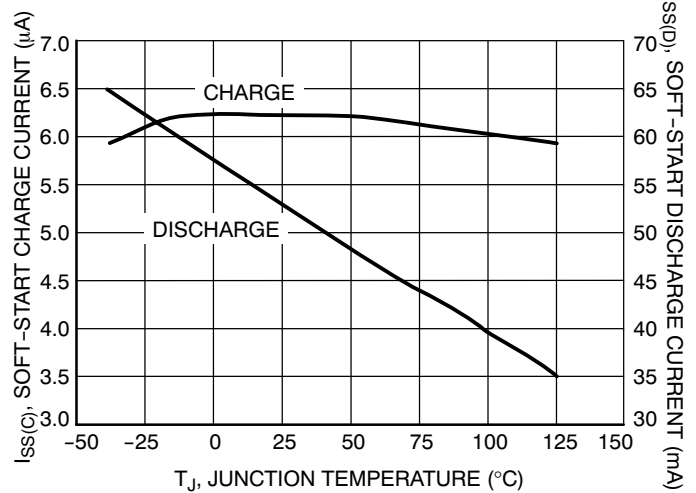


Figure 20. Soft-Start Charge/Discharge Currents versus Junction Temperature

TYPICAL CHARACTERISTICS

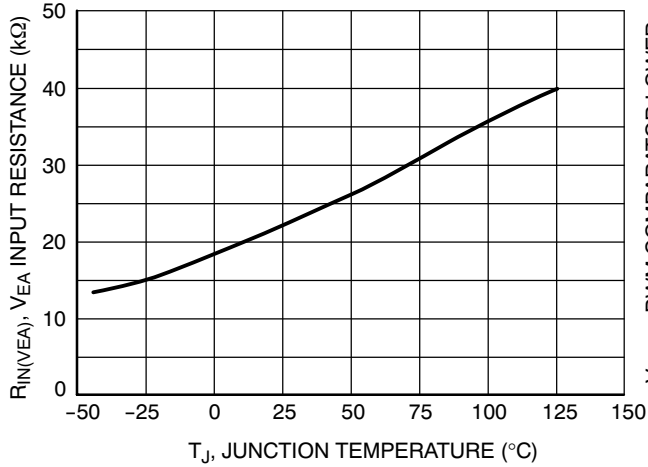


Figure 21. V_{EA} Input Resistance versus Junction Temperature

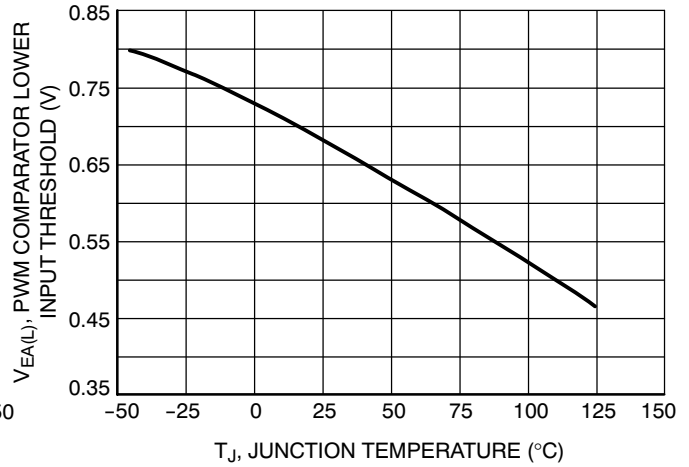


Figure 22. PWM Comparator Lower Input Threshold versus Junction Temperature

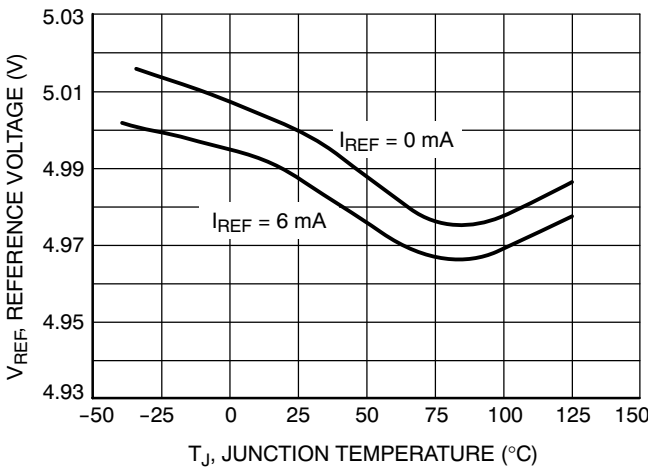


Figure 23. Reference Voltage versus Junction Temperature

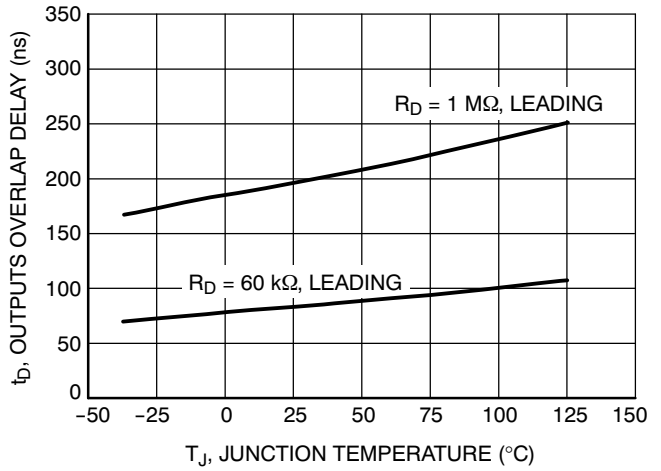


Figure 24. Outputs Overlap Delay versus Junction Temperature

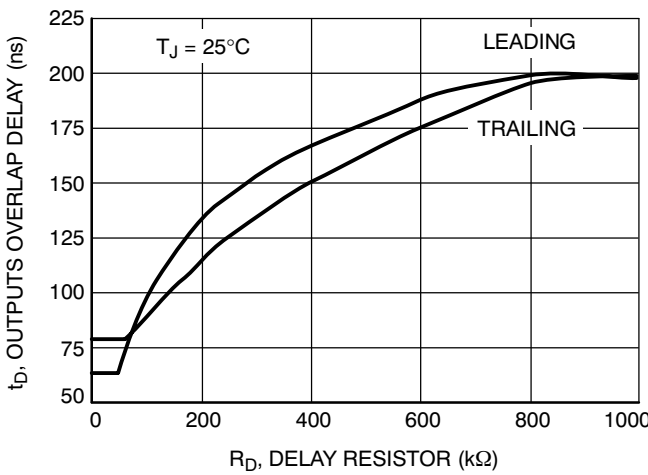


Figure 25. Outputs Overlap Delay versus Delay Resistor

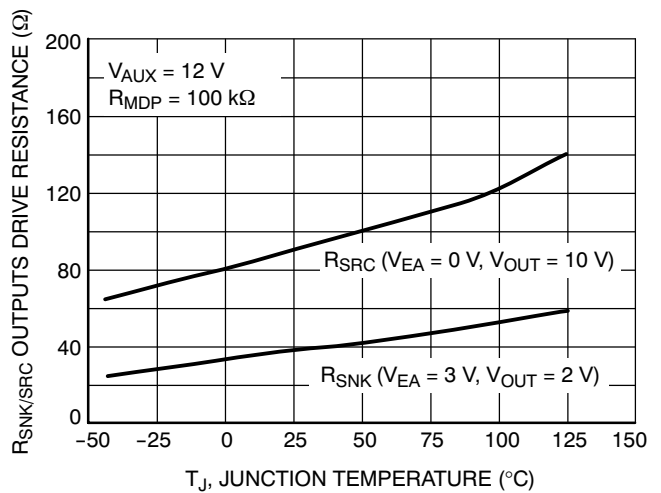


Figure 26. Outputs Drive Resistance Voltage versus Junction Temperature

TYPICAL CHARACTERISTICS

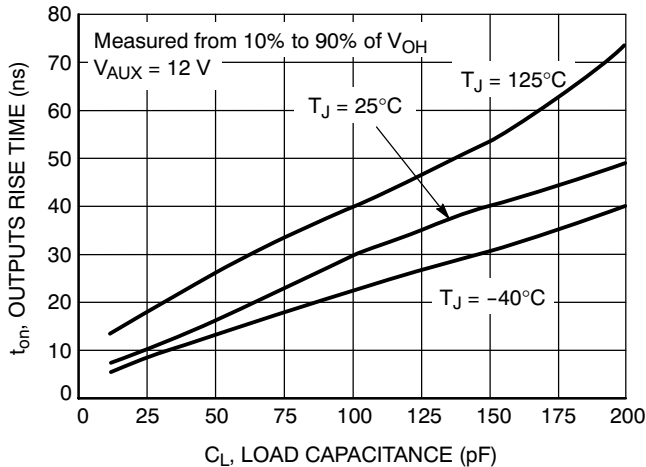


Figure 27. Outputs Rise Time versus Load Capacitance

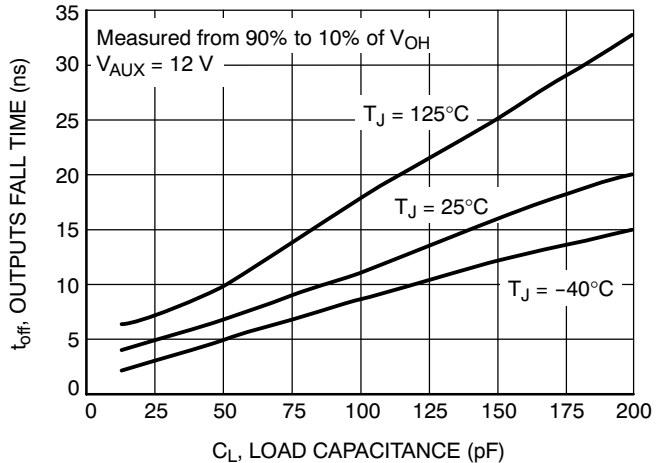


Figure 28. Outputs Fall Time versus Load Capacitance

DETAILED OPERATING DESCRIPTION

Introduction

An NCP1280 based system offers significant efficiency improvements and system cost savings over a converter using a traditional forward topology. The NCP1280 provides two control outputs. OUT1 controls the primary switch of a forward converter. OUT2 has an adjustable overlap delay, which can be used to control an active clamp/reset switch or any other complementary drive topology, such as an asymmetric half-bridge. In addition, OUT2 can be used to control a synchronous rectifier topology, eliminating the need of external control circuitry. Other distinctive features include: two mode overcurrent protection, line under/overvoltage detectors, fast line feedforward, soft-start and a maximum duty cycle limit. The Functional Block Diagram is shown in Figure 2.

The features included in the NCP1280 provide some of the advantages of Current-Mode Control, such as fast line feedforward, and cycle by cycle current limit. It eliminates the disadvantages of low power jitter, slope compensation and noise susceptibility.

Active Clamp Topology

The transformer reset voltage in a traditional forward converter is set by the turns ratio and input voltage. Where as the reset voltage of an active clamp topology is constant over the converter off time and only depends on the input voltage and duty cycle. This translates into a lower voltage stress on the main switch, allowing the use of lower voltage MOSFETs. In general, lower voltage MOSFETs have lower cost and ON resistance. Therefore, lower system cost and higher efficiency can be achieved. In addition, the lower voltage stress allows the converter to operate at a higher duty cycle for a given primary switch voltage stress. This allows a reduction in primary peak current and secondary side voltage stress as well as smaller secondary inductor size.

High Voltage Startup Regulator

The NCP1280 contains an internal 700 V startup regulator that eliminates the need for external startup components. In addition, this regulator increases the efficiency of the supply as it uses no power when in the normal mode of operation, but instead uses power supplied by an auxiliary winding.

The startup regulator consists of a constant current source that supplies current from the input line voltage (V_{in}) to the capacitor on the V_{AUX} pin (C_{AUX}). The startup current is typically 13.8 mA. Once V_{AUX} reaches 11 V, the startup regulator turns OFF and the outputs are enabled. When V_{AUX} reaches 7 V, the outputs are disabled and the startup regulator turns ON. This “7-11” mode of operation is known as Dynamic Self Supply (DSS). The V_{AUX} pin can be biased externally above 7 V once the outputs are enabled to prevent the startup regulator from turning ON. It is recommended to bias the V_{AUX} pin using an auxiliary supply generated by an auxiliary winding from the power transformer. An independent voltage supply can also be used. If using an independent voltage supply and V_{AUX} is biased before the outputs are enabled or while a fault is present, the One Shot Pulse Generator (Figure 2) will not be enabled and the outputs will remain OFF.

As the DSS sources current to the V_{AUX} pin, a diode should be placed between C_{AUX} and the auxiliary supply as shown in Figure 29. This will allow the NCP1280 to charge C_{AUX} while preventing the startup regulator from sourcing current into the auxiliary supply.

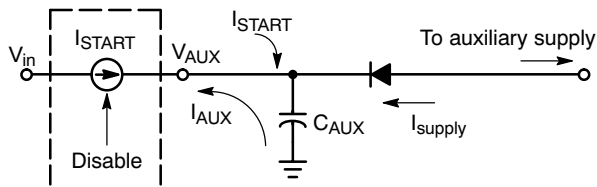


Figure 29. Recommended V_{AUX} Configuration

Power to the controller while operating in the self-bias or DSS mode is provided by C_{AUX} . Therefore, C_{AUX} must be sized such that a V_{AUX} voltage greater than 7 V is maintained while the outputs are switching and the converter reaches regulation. Also, the V_{AUX} discharge time (from 11 V to 7 V) must be greater than the soft-start charge period to assure the converter turns ON.

The startup circuit is rated at a maximum voltage of 700 V. If the device operates in the DSS mode, power dissipation should be controlled to avoid exceeding the maximum power dissipation of the controller.

Line Under/Overvoltage Shutdown

The NCP1280 incorporates line undervoltage and overvoltage shutdown (UV/OV) circuits. The under voltage (UV) threshold is 1.52 V and the overvoltage threshold (OV) is 3.61 V, for a ratio of 1:2.4. If the input voltage range exceeds the pre-set OV threshold, the OV function can be disabled by connecting a Zener from this pin to ground. The Zener voltage should be less than 3.6 V.

The UV/OV circuit can be biased using an external resistor divider from the input line. The resistor divider must be sized to enable the controller once V_{in} is within the required operating range. If the UV or OV threshold is reached, the soft-start capacitor is discharged, and the outputs are immediately disabled with no overlap delay as shown in Figure 30. Also, if an UV condition is detected, the 5.0 V Reference Supply is disabled.

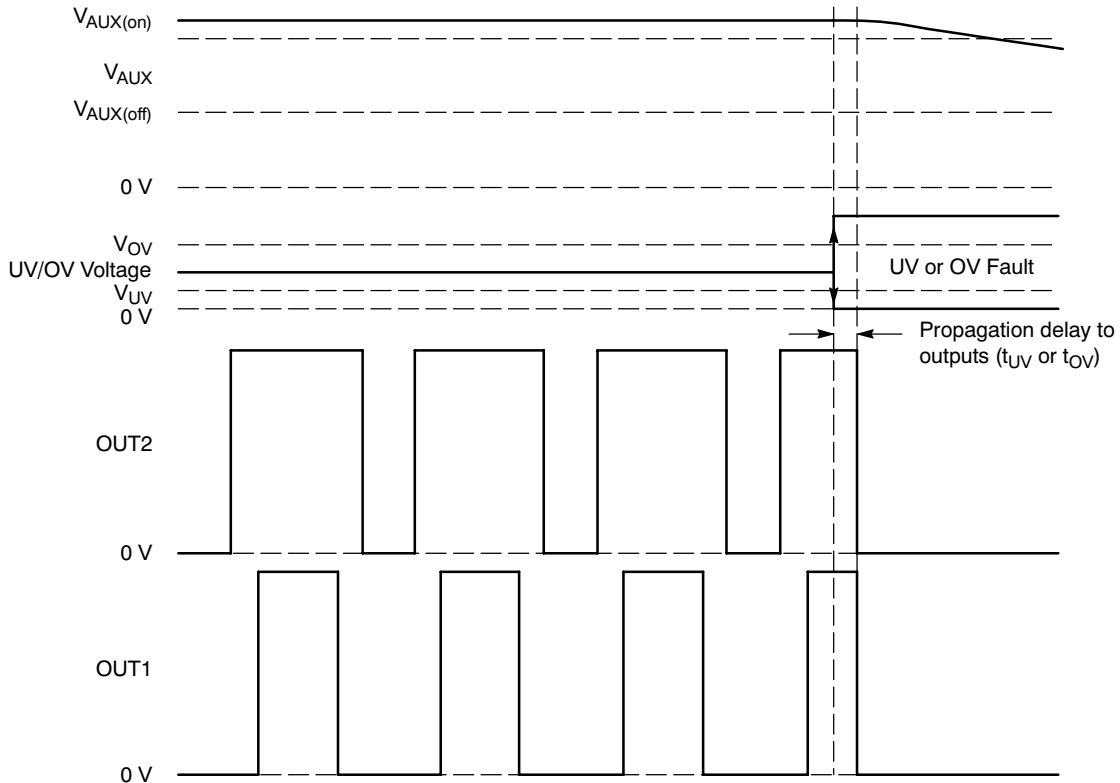


Figure 30. UV/OV Fault Timing Diagram

Once the UV or OV condition is removed and V_{AUX} reaches 11 V, the controller initiates a soft-start cycle. Figure 31 shows the relationship between the UV/OV voltage, the outputs and the soft-start voltage.

The UV/OV pin can also be used to implement a remote enable/disable function. Biasing the UV/OV pin below its UV threshold disables the converter.

NCP1280

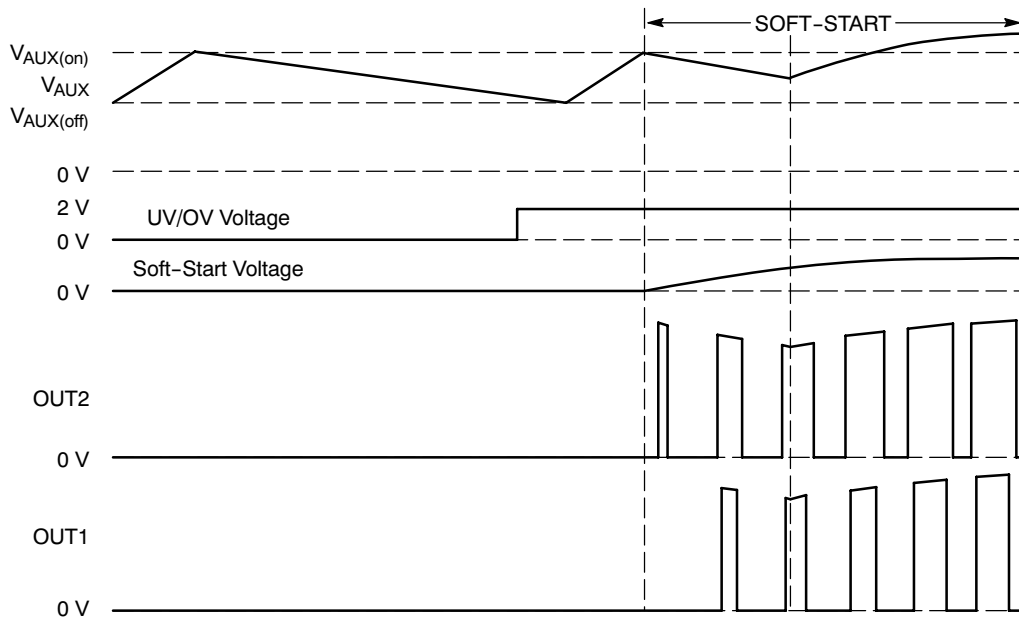


Figure 31. Soft-Start Timing Diagram (Using Auxiliary Winding)

Feedforward Ramp Generator

The NCP1280 incorporates line feedforward (FF) to compensate for changes in line voltage. A FF Ramp proportional to V_{in} is generated and compared to V_{EA} . If the line voltage changes, the FF Ramp slope changes accordingly. The duty cycle will be adjusted immediately instead of waiting for the line voltage change to propagate around the system and be reflected back on V_{EA} .

A resistor between V_{in} and the FF pin (R_{FF}) sets the feedforward current (I_{FF}). The FF Ramp is generated by charging an internal 10 pF capacitor (C_{FF}) with a constant current proportional to I_{FF} . The FF Ramp is finished (capacitor is discharged) once the Oscillator Ramp reaches 2.0 V. Please refer to Figure 2 for a functional drawing of the Feedforward Ramp generator.

I_{FF} is usually a few hundred microamps, depending on the operating frequency and the required duty cycle. If the operating frequency and maximum duty cycle are known, I_{FF} is calculated using the equation below:

$$I_{FF} = \frac{C_{FF} \times V_{DC(inv)} \times 125 \text{ k}\Omega}{6.7 \text{ k}\Omega \times t_{on(max)}}$$

where $V_{DC(inv)}$ is the voltage on the inverting input of the Max DC Comparator and $t_{on(max)}$ is the maximum ON time.

Figure 18 shows the relationship between I_{FF} and DC_{MAX} . For example, if a system is designed to operate at 200 kHz, with a 60% maximum duty cycle at 100 V, the DC_{MAX} pin can be grounded and I_{FF} is calculated as follows:

$$T = \frac{1}{f} = \frac{1}{200 \text{ kHz}} = 5.0 \text{ }\mu\text{s}$$

$$t_{on(max)} = DC_{MAX} \times T = 0.6 \times 5.0 \text{ }\mu\text{s} = 3.0 \text{ }\mu\text{s}$$

$$I_{FF} = \frac{C_{FF} \times V_{DC(inv)} \times 125 \text{ k}\Omega}{6.7 \text{ k}\Omega \times t_{on(max)}} = \frac{10 \text{ pF} \times 0.888 \text{ V} \times 125 \text{ k}\Omega}{6.7 \text{ k}\Omega \times 3.0 \text{ }\mu\text{s}} = 55.2 \text{ }\mu\text{A}$$

For a minimum line voltage of 100 V, the required feedforward resistor is calculated using the equation below:

$$R_{FF} = \frac{V_{in}}{I_{FF}} - 12.0 \text{ k}\Omega = \frac{100 \text{ V}}{55.2 \text{ }\mu\text{A}} - 12.0 \text{ k}\Omega \approx 1.82 \text{ M}\Omega$$

From the above calculations it can be observed that I_{FF} is controlled predominantly by the value of R_{FF} , as the resistance seen into the FF pin is only 12 k Ω . If a tight maximum duty cycle control overtemperature is required, R_{FF} should have a low thermal coefficient.

Current Limit

The NCP1280 has two overcurrent protection modes, cycle by cycle and cycle skip. It allows the NCP1280 to handle momentary and hard shorts differently for the best tradeoff in performance and safety. The outputs are disabled typically 90 ns after a current limit fault is detected.

The cycle by cycle mode terminates the conduction cycle (reducing the duty cycle) if the voltage on the CS pin exceeds 0.48 V. If the voltage on the CS pin exceeds 0.57 V, the converter enters the cycle skip (CSKIP) mode. While in the CSKIP mode, the soft-start capacitor is discharged and the converter is disabled by a time determined by the CSKIP timer.

The CSKIP timer is set by immediately discharging the capacitor on the CSKIP pin (C_{CSKIP}), and then charging it with a constant current source of $12.3 \mu\text{A}$. The cycle skip period ends when the voltage on the cycle skip capacitor reaches 2.0 V. The cycle skip capacitor is calculated using the equation below:

$$C_{CSKIP} \approx \frac{T_{CSKIP} \times 12.3 \mu\text{A}}{2 \text{ V}}$$

Using the above equation, a cycle skip period of $11.0 \mu\text{s}$ requires a cycle skip capacitor of 68 pF. The differences between the cycle by cycle and cycle skip modes are observed in Figure 32.

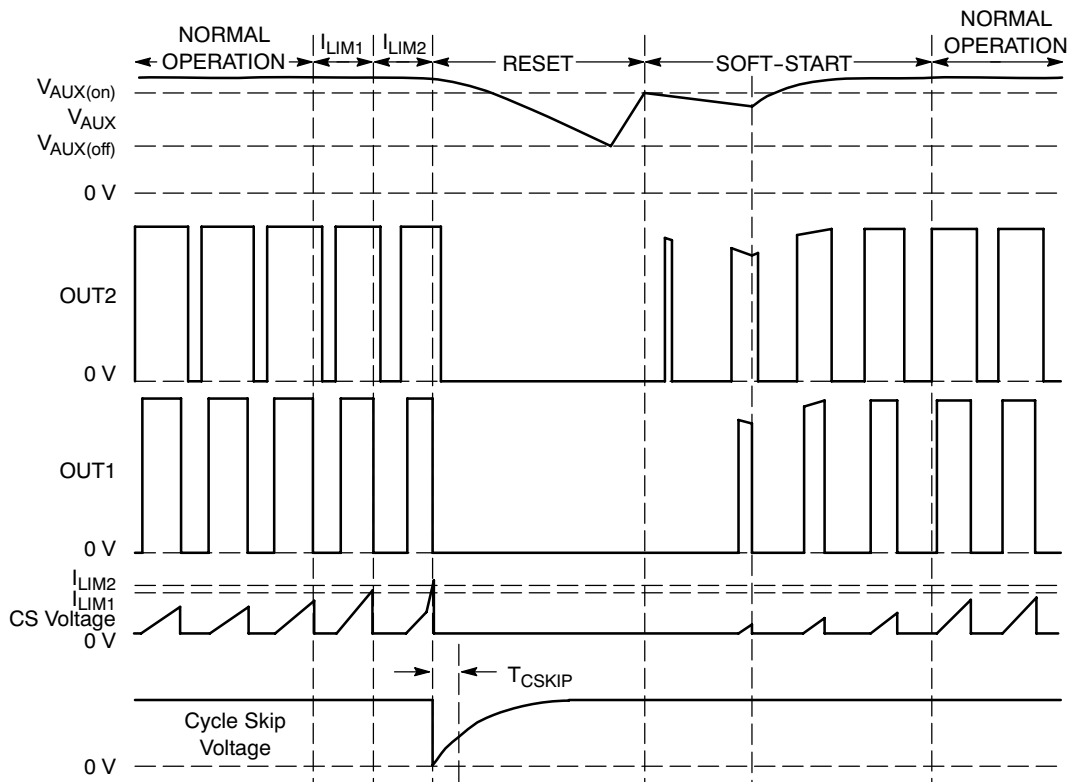


Figure 32. Overcurrent Faults Timing Diagram

Once the cycle skip period is complete and V_{AUX} reaches 11 V, a soft-start sequence commences. The possible minimum OFF time is set by C_{CSKIP} . However, the actual OFF time is generally greater than C_{CSKIP} because it is the cycle skip period added to the time it takes V_{AUX} to reach 11 V.

Oscillator

The NCP1280 oscillator frequency is set by a single external resistor connected between the R_T pin and GND. The oscillator is designed to operate up to 500 kHz.

The voltage on the R_T pin is laser trim adjusted during manufacturing to 1.3 V for an R_T of 101 k Ω . A current set by R_T generates an Oscillator Ramp by charging an internal 10 pF capacitor as shown in Figure 2. The period ends (capacitor is discharged) once the Oscillator Ramp reaches 2.0 V. If R_T increases, the current and the Oscillator Ramp slope decrease, thus reducing the frequency. If R_T decreases, the opposite effect is obtained. Figure 16 shows the relationship between R_T and the oscillator frequency.

Maximum Duty Cycle

A dedicated internal comparator limits the maximum ON time of OUT1 by comparing the FF Ramp to $V_{DC(inv)}$. If the FF Ramp voltage exceeds $V_{DC(inv)}$, the output of the Max DC Comparator goes high. This will reset the Output Latch, thus turning OFF the outputs and limiting the duty cycle.

Duty cycle is defined as:

$$DC = \frac{t_{on}}{T} = t_{on} \times f$$

Therefore, the maximum ON time can be set to yield the desired DC if the operating frequency is known. The maximum ON time is set by adjusting the FF Ramp to reach $V_{DC(inv)}$ in a time equal to $t_{on(max)}$ as shown in Figure 33. The maximum ON time should be set for the minimum line voltage. As line voltage increases, the slope of the FF Ramp increases. This reduces the duty cycle below DC_{MAX} , which is a desirable feature as the duty cycle is inversely proportional to line voltage.

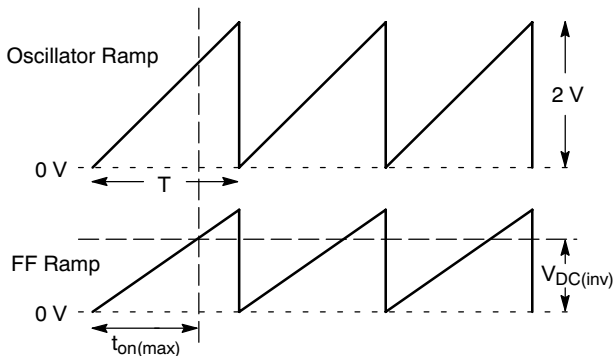


Figure 33. Maximum ON Time Limit Waveforms

An internal resistor divider from a 2.0 V reference is used to set $V_{DC(inv)}$. If the DC_{MAX} pin is grounded, $V_{DC(inv)}$ is 0.88 V. If the pin is floating, $V_{DC(inv)}$ is 1.19 V. This is equivalent to 60% or 80% of a 1.5 V FF Ramp. $V_{DC(inv)}$ can be adjusted to other values by using an external resistor network on the DC_{MAX} pin. For example, if the minimum line voltage is 100 V, R_{FF} is 1.82 M Ω , operating frequency is 200 kHz and a maximum duty cycle of 70% is required, $V_{DC(inv)}$ is calculated as follows:

$$V_{DC(inv)} = \frac{I_{FF} \times 6.7 \text{ k}\Omega \times t_{on(max)}}{C_{FF} \times 125 \text{ k}\Omega}$$

$$V_{DC(inv)} = \frac{55.2 \text{ }\mu\text{A} \times 6.7 \text{ k}\Omega \times 3.5 \text{ }\mu\text{s}}{10 \text{ pF} \times 125 \text{ k}\Omega} = 1.04 \text{ V}$$

This can be achieved by connecting a 19.6 k Ω resistor from the DC_{MAX} pin to GND. The maximum duty cycle limit can be disabled connecting a 100 k Ω resistor between the DC_{MAX} and V_{REF} pins.

5.0 V Reference

The NCP1280 includes a precision 5.0 V reference output. The reference output is biased directly from V_{AUX} and it can supply up to 6 mA. Load regulation is 50 mV and line regulation is 100 mV over the complete operating range.

It is recommended to bypass the reference output with a 0.1 μF ceramic capacitor. The reference output is disabled when an UV fault is present.

PWM Comparator

In steady state operation, the PWM comparator adjusts the duty cycle by comparing the error signal to the FF Ramp. The error signal is fed into the V_{EA} input. The V_{EA} input can be driven directly with an optocoupler and a pullup resistor from V_{REF} . The drive of the V_{EA} pin is simplified by internally incorporating a series diode and resistor. The series diode provides a 0.7 V offset between V_{EA} input and the PWM comparator inverting input. The outputs are enabled if the V_{EA} voltage is approximately 0.7 above the valley voltage of the FF Ramp.

The pullup resistor is selected such that in the absence of the error signal, the voltage on the V_{EA} pin exceeds the peak amplitude of the FF Ramp. Otherwise, the converter will not be able to reach maximum duty cycle. The V_{EA} range required to control the DC from 0% to DC_{MAX} is given by the equation below:

$$V_{EA(L)} < V_{EA} < \left(\frac{I_{FF} \times DC}{186.56 \text{ pf} \times f} + V_{EA(L)} \right)$$

where, $V_{EA(L)}$ is the PWM comparator lower input threshold.

Soft-Start

Soft-start (SS) allows the converter to gradually reach steady state operation, thus reducing startup stress and surges on the system. The duty cycle is limited during a soft-start sequence by comparing the Oscillator Ramp to the SS voltage (V_{SS}) by means of the Soft-Start Comparator.

A 6.2 μA current source starts to charge the capacitor on the SS pin once faults are removed and V_{AUX} reaches 11 V. The Soft-Start Comparator controls the duty cycle while the SS voltage is below 2.0 V. Once V_{SS} reaches 2.0 V, it exceeds the Oscillator Ramp voltage and the Soft-Start Comparator does not limit the duty cycle. Figure 34 shows the relationship between the outputs duty cycle and the soft-start voltage.

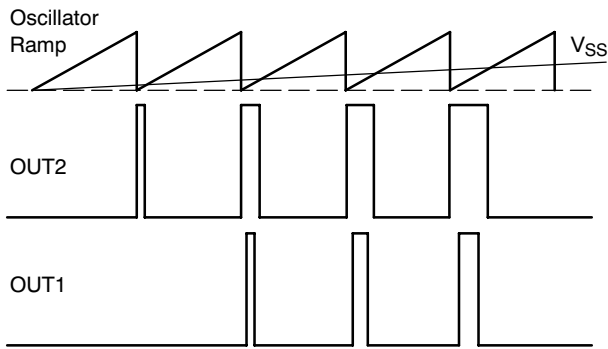


Figure 34. Soft-Start Timing Diagram

If the soft-start period is too long, V_{AUX} will discharge to 7 V before the converter output is completely in regulation causing the outputs to be disabled. If the converter output is not completely discharged when the outputs are re-enabled, the converter will eventually reach regulation exhibiting a non-monotonic startup behavior. But, if the converter output is completely discharged when the outputs are re-enabled, the cycle may repeat and the converter will not start.

In the event of an UV, OV, or cycle skip fault, the soft-start capacitor is discharged. Once the fault is removed, a soft-start cycle commences. The soft-start steady state voltage is approximately 4.1 V.

Control Outputs

The NCP1280 has two in-phase control outputs, OUT1 and OUT2, with adjustable overlap delay (t_D). OUT2 precedes OUT1 during a low to high transition and OUT1 precedes OUT2 at any high to low transition. Figure 35 shows the relationship between OUT1 and OUT2.

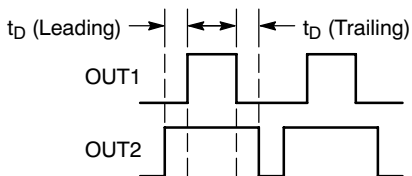


Figure 35. Control Outputs Timing Diagram

Generally, OUT1 controls the main switching element. Output 2, once inverted, can control a synchronous rectifier. The overlap delay prevents simultaneous conduction. Output 2 can also be used to control an active clamp reset.

Once V_{AUX} reaches 11 V, the internal startup circuit is disabled and the One Shot Pulse Generator is enabled. If no faults are present, the outputs turn ON. Otherwise, the outputs remain OFF until the fault is removed and V_{AUX} reaches 11 V again.

The control outputs are biased from V_{AUX} . The outputs can supply up to 10 mA each and their high state voltage is usually 0.2 V below V_{AUX} . Therefore, the auxiliary supply voltage should not exceed the maximum input voltage of the driver stage.

If the control outputs need to drive a large capacitive load, a driver should be used between the NCP1280 and the load. ON Semiconductor's MC33152 is a good selection for an integrated driver. Figures 27 and 28 shows the relationship between the output's rise and fall times vs capacitive load.

Time Delay

The overlap delay between the outputs is set connecting a resistor (R_D) between the t_D and V_{REF} pins. A minimum overlap delay of 80 ns is obtained when R_D is 60 k Ω . If R_D is not present, the delay is 200 ns.

The output duty cycle can be adjusted from 0% to 85% selecting appropriate values of R_{FF} and $V_{DC(inv)}$. It should be noted that the overlap delay may cause OUT2 to reach 100% duty cycle. Therefore, if OUT2 is used, the maximum duty cycle of OUT2 needs to be kept below 100%. The maximum overlap delay, $t_{D(max)}$, depends on the maximum duty cycle and frequency of operation. The maximum overlap delay is calculated using the equation below.

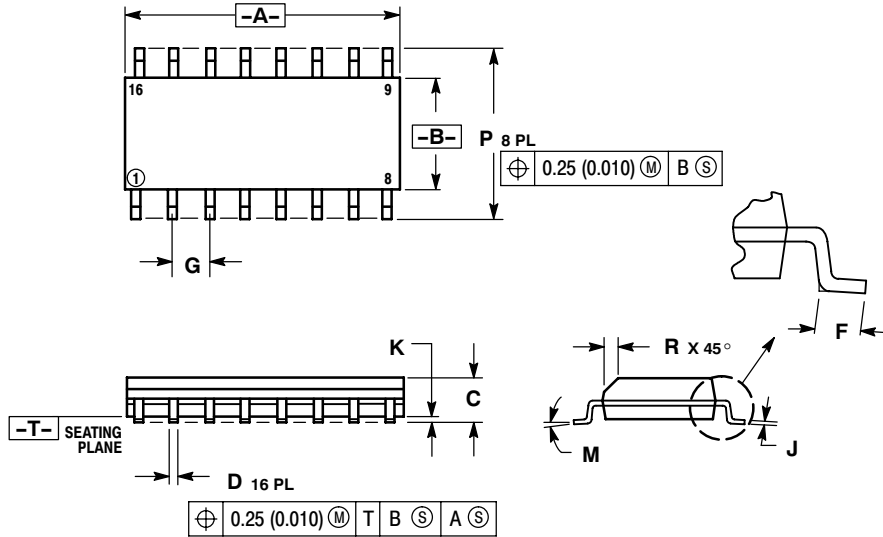
$$t_{D(max)} \leq \frac{(1 - DC)}{2f}$$

For example, if the converter operates at a frequency of 300 kHz with a maximum duty cycle of 80%, the maximum allowed overlap delay is 333 ns. However, this is a theoretical limit and variations over the complete operating range should be considered when selecting the overlap delay.

NCP1280

PACKAGE DIMENSIONS

SO-16
D SUFFIX
CASE 751B-05
ISSUE J




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

NCP1280

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