



**THE DATASHEET OF  
NCV33375ST3.3T3G**



# ON Semiconductor

## Is Now

The logo for onsemi, featuring the word "onsemi" in a dark teal, lowercase, sans-serif font. The letter "i" is stylized with a white dot and a teal vertical bar. A small orange triangle is positioned above the top right of the "i". A trademark symbol (TM) is located to the right of the logo.

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# Voltage Regulator - Low Dropout, On/Off Control 300 mA

## MC33375, NCV33375 Series

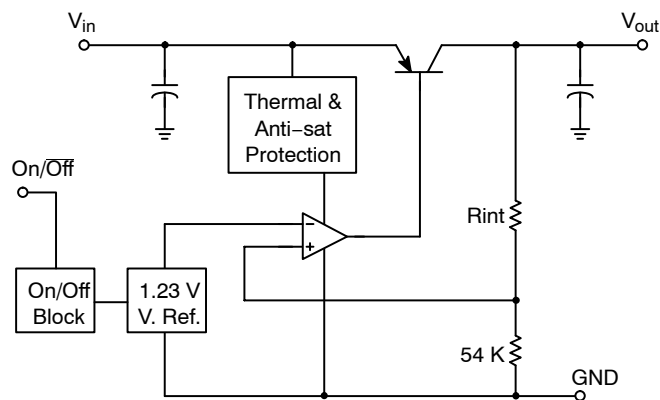
The MC33375 series are micropower low dropout voltage regulators available in a wide variety of output voltages as well as packages, SOT-223 and SOP-8. These devices feature a very low quiescent current and are capable of supplying output currents up to 300 mA. Internal current and thermal limiting protection are provided by the presence of a short circuit at the output and an internal thermal shutdown circuit.

The MC33375 has a control pin that allows a logic level signal to turn-off or turn-on the regulator output.

Due to the low input-to-output voltage differential and bias current specifications, these devices are ideally suited for battery powered computer, consumer, and industrial equipment where an extension of useful battery life is desirable.

### Features:

- Low Quiescent Current (0.3  $\mu$ A in OFF mode; 125  $\mu$ A in ON mode)
- Low Input-to-Output Voltage Differential of 25 mV at  $I_O = 10$  mA, and 260 mV at  $I_O = 300$  mA
- Extremely Tight Line and Load Regulation
- Stable with Output Capacitance of only 0.33  $\mu$ F for 2.5 V Output Voltage
- Internal Current and Thermal Limiting
- Logic Level ON/OFF Control
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These are Pb-Free Devices



This device contains 41 active transistors

Figure 1. Simplified Block Diagram



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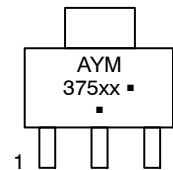
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## LOW DROPOUT MICROPOWER VOLTAGE REGULATOR

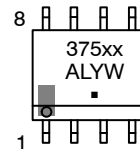
### MARKING DIAGRAMS



SOT-223  
ST SUFFIX  
CASE 318E



SOIC-8  
D SUFFIX  
CASE 751



A = Assembly Location  
Y = Year  
M = Date Code  
L = Wafer Lot  
W = Work Week  
xx = Voltage Version  
▪ = Pb-Free Package

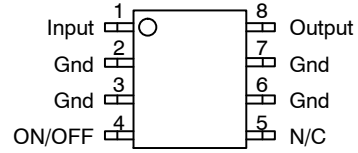
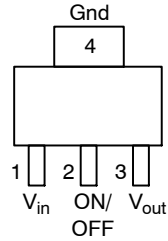
(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

# MC33375, NCV33375 Series

## PIN CONNECTIONS



## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	$V_{CC}$	13	Vdc
Power Dissipation and Thermal Characteristics $T_A = 25^\circ\text{C}$			
Maximum Power Dissipation	$P_D$	Internally Limited	W
Case 751 (SOP-8) D Suffix			
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	160	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	25	$^\circ\text{C/W}$
Case 318E (SOT-223) ST Suffix			
Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	245	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	15	$^\circ\text{C/W}$
Output Current	$I_O$	300	mA
Maximum Junction Temperature	$T_J$	150	$^\circ\text{C}$
Operating Ambient Temperature Range	$T_A$	- 40 to +125	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	- 65 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## MC33375, NCV33375 Series

### ELECTRICAL CHARACTERISTICS ( $C_L = 1.0 \mu\text{F}$ , $T_A = 25^\circ\text{C}$ , for min/max values $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , Note 1)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage $I_O = 0 \text{ mA to } 250 \text{ mA}$ $T_A = 25^\circ\text{C}$ , $V_{in} = [V_O + 1] \text{ V}$ 1.8 V Suffix 2.5 V Suffix 3.0 V Suffix 3.3 V Suffix 5.0 V Suffix  1.8 V Suffix $V_{in} = [V_O + 1] \text{ V}$ , $0 < I_O < 100 \text{ mA}$ 2.5 V Suffix $2\%$ Tolerance from $T_J = -40$ to $+125^\circ\text{C}$ 3.0 V Suffix 3.3 V Suffix 5.0 V Suffix	$V_O$	1.782 2.475 2.970 3.267 4.950  1.764 2.450 2.940 3.234 4.900	1.80 2.50 3.00 3.30 5.00  - - - - -	1.818 2.525 3.030 3.333 5.05  1.836 2.550 3.060 3.366 5.100	Vdc
Line Regulation $V_{in} = [V_O + 1] \text{ V to } 12 \text{ V}$ , $I_O = 250 \text{ mA}$ , All Suffixes $T_A = 25^\circ\text{C}$	$\text{Reg}_{line}$	-	2.0	10	mV
Load Regulation $V_{in} = [V_O + 1] \text{ V}$ , $I_O = 0 \text{ mA to } 250 \text{ mA}$ , All Suffixes $T_A = 25^\circ\text{C}$	$\text{Reg}_{load}$	-	5.0	25	mV
Dropout Voltage (Note 3) $I_O = 10 \text{ mA}$ $T_J = -40^\circ\text{C to } +125^\circ\text{C}$ $I_O = 100 \text{ mA}$ $I_O = 250 \text{ mA}$ $I_O = 300 \text{ mA}$	$V_{in} - V_O$	- - - -	25 115 220 260	100 200 400 500	mV
Ripple Rejection (120 Hz) $V_{in(\text{peak-peak})} = [V_O + 1.5] \text{ V to } [V_O + 5.5] \text{ V}$	-	65	75	-	dB
Output Noise Voltage $C_L = 1.0 \mu\text{F}$ $I_O = 50 \text{ mA}$ (10 Hz to 100 kHz) $C_L = 200 \mu\text{F}$	$V_n$	- -	160 46	- -	$\mu\text{Vrms}$

### CURRENT PARAMETERS

Quiescent Current ON Mode $V_{in} = [V_O + 1] \text{ V}$ , $I_O = 0 \text{ mA}$	$I_{QOn}$	-	125	200	$\mu\text{A}$
Quiescent Current OFF Mode	$I_{QOff}$	-	0.3	4.0	$\mu\text{A}$
Quiescent Current ON Mode SAT 3.0 V Suffix 3.3 V Suffix 5.0 V Suffix	$I_{QSAT}$	- - -	1500 1500 1500	2000 2000 2000	$\mu\text{A}$
Current Limit $V_{in} = [V_O + 1] \text{ V}$ , $V_O$ Shorted	$I_{LIMIT}$	-	450	-	mA

### ON/OFF INPUTS

On/Off Input Voltage Logic "1" (Regulator On) $V_{out} = V_O \pm 2\%$ Logic "0" (Regulator Off) $V_{out} < 0.03 \text{ V}$ Logic "0" (Regulator Off) $V_{out} < 0.05 \text{ V}$ (1.8 V Option)	$V_{CTRL}$	2.4 - -	- - -	- 0.5 0.3	V
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### THERMAL SHUTDOWN

Thermal Shutdown	-	-	150	-	$^\circ\text{C}$
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1. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
2. Quiescent Current is measured where the PNP pass transistor is in saturation.  $V_{in} = [V_O - 0.5] \text{ V}$  guarantees this condition.
3. For 1.8 V version  $V_{DO}$  is constrained by the minimum input voltage of 2.5 V.
4. For 1.8 V and 2.5 V versions,  $I_{QSAT}$  is constrained by the minimum input voltage of 2.5 V.

## DEFINITIONS

**Load Regulation** – The change in output voltage for a change in load current at constant chip temperature.

**Dropout Voltage** – The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 100 mV below its nominal value (which is measured at 1.0 V differential), dropout voltage is affected by junction temperature, load current and minimum input supply requirements.

**Output Noise Voltage** – The RMS AC voltage at the output with a constant load and no input ripple, measured over a specified frequency range.

**Maximum Power Dissipation** – The maximum total dissipation for which the regulator will operate within specifications.

**Quiescent Current** – Current which is used to operate the regulator chip and is not delivered to the load.

**Line Regulation** – The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

**Maximum Package Power Dissipation** – The maximum package power dissipation is the power dissipation level at which the junction temperature reaches its maximum value i.e. 150°C. The junction temperature is rising while the difference between the input power ( $V_{CC} \times I_{CC}$ ) and the output power ( $V_{out} \times I_{out}$ ) is increasing.

Depending on ambient temperature, it is possible to calculate the maximum power dissipation and so the maximum current as following:

$$P_D = \frac{T_J - T_A}{R_{\theta JA}}$$

The maximum operating junction temperature  $T_J$  is specified at 150°C, if  $T_A = 25^\circ\text{C}$ , then  $P_D$  can be found. By neglecting the quiescent current, the maximum power dissipation can be expressed as:

$$I_{out} = \frac{P_D}{V_{CC} - V_{out}}$$

The thermal resistance of the whole circuit can be evaluated by deliberately activating the thermal shutdown of the circuit (by increasing the output current or raising the input voltage for example).

Then you can calculate the power dissipation by subtracting the output power from the input power. All variables are then well known: power dissipation, thermal shutdown temperature (150°C for MC33375) and ambient temperature.

$$R_{\theta JA} = \frac{T_J - T_A}{P_D}$$

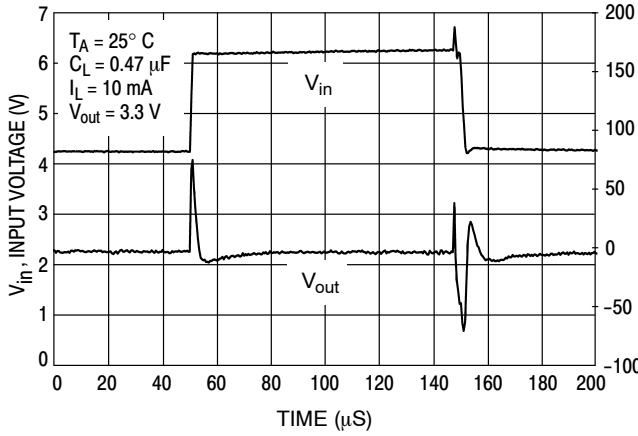


Figure 2. Line Transient Response

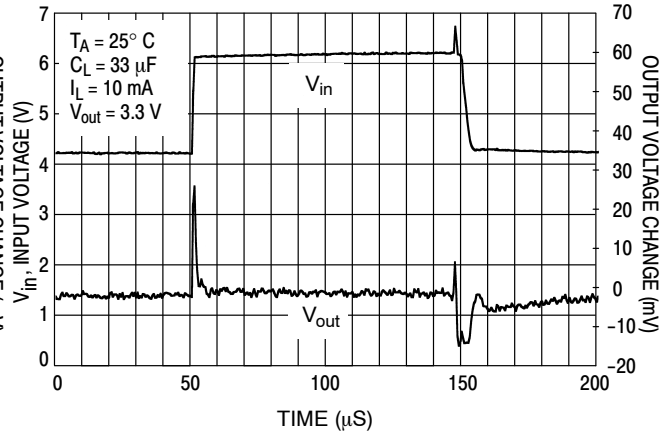


Figure 3. Line Transient Response

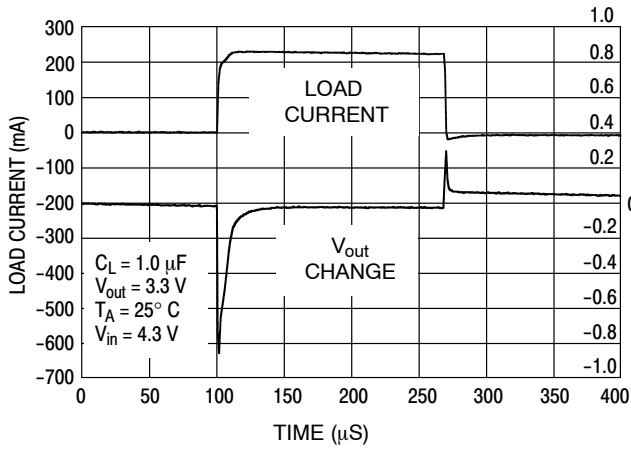


Figure 4. Load Transient Response

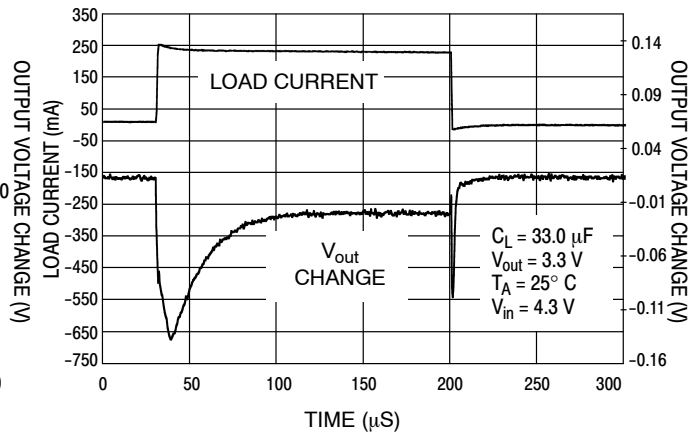


Figure 5. Load Transient Response

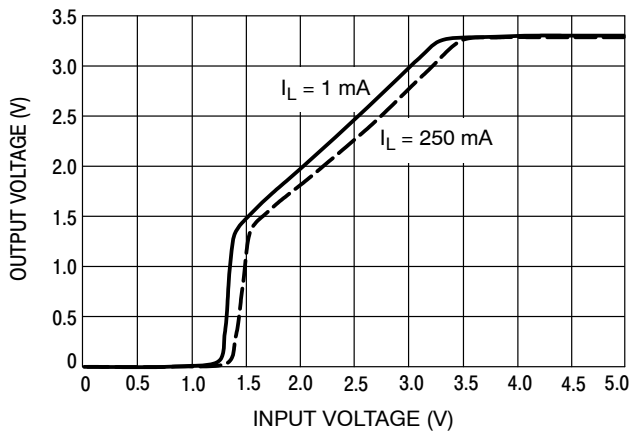


Figure 6. Output Voltage versus Input Voltage

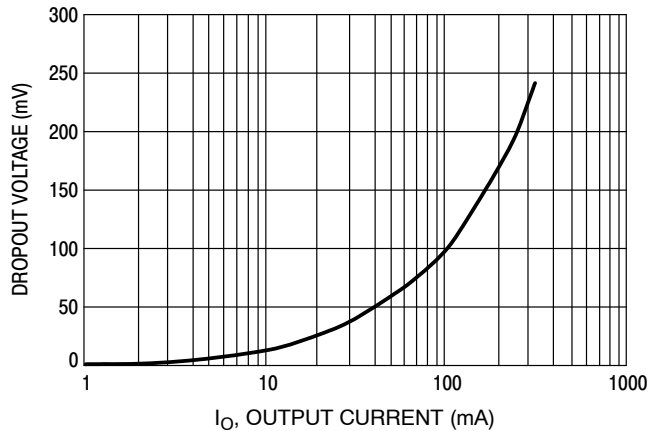


Figure 7. Dropout Voltage versus Output Current

MC33375, NCV33375 Series

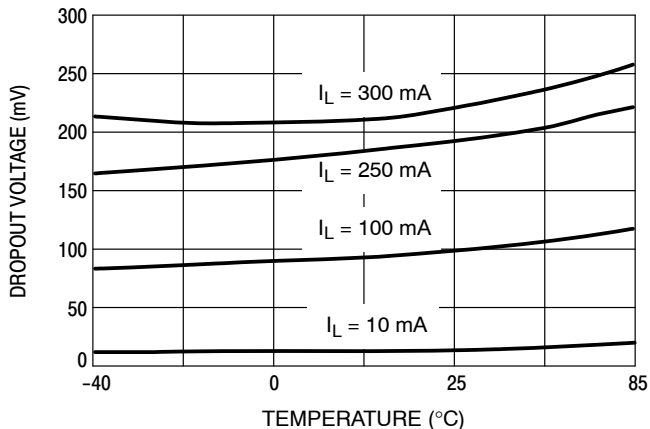


Figure 8. Dropout Voltage versus Temperature

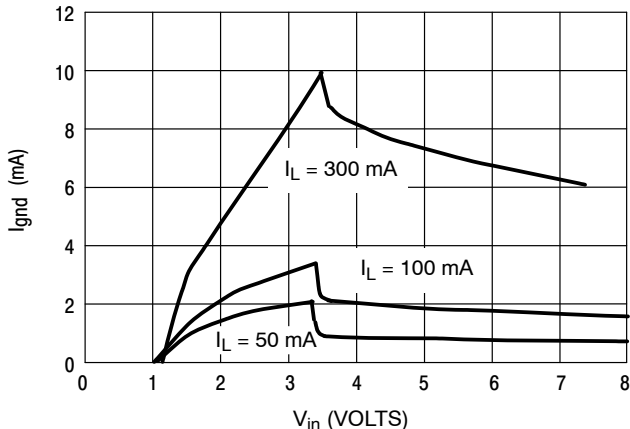


Figure 9. Ground Pin Current versus Input Voltage

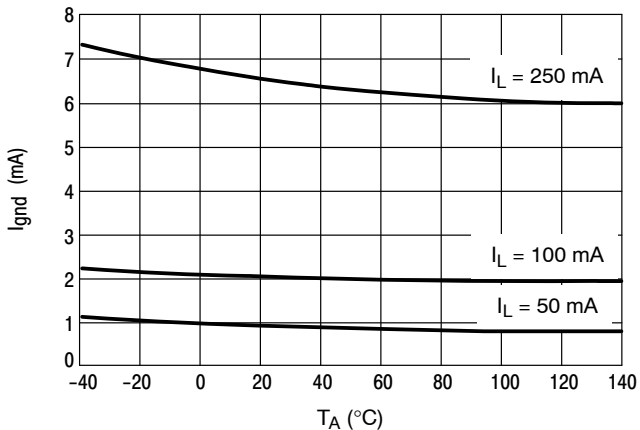


Figure 10. Ground Pin Current versus Ambient Temperature

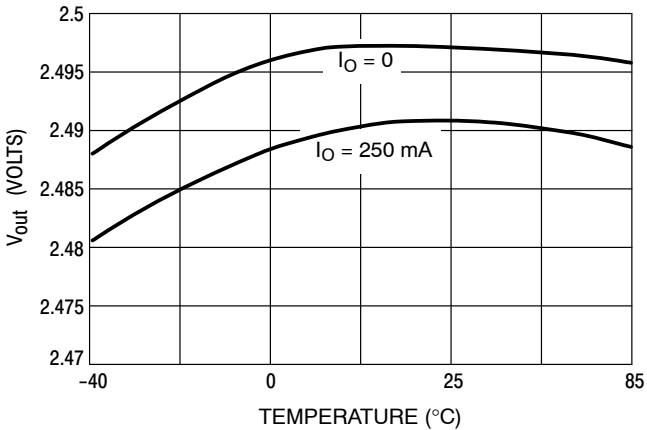
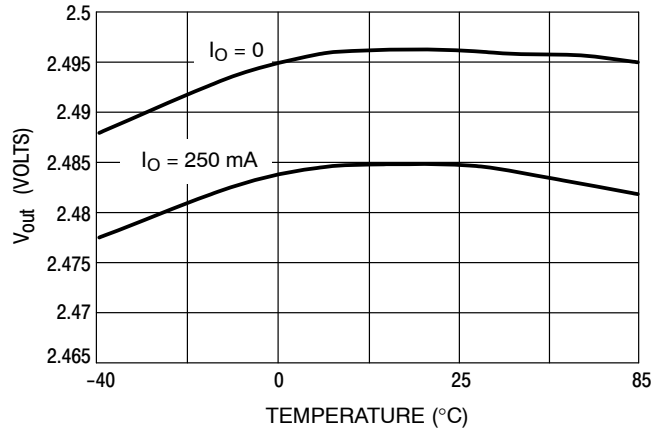
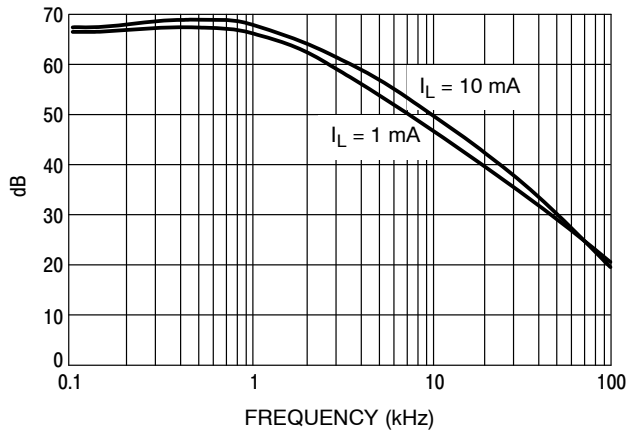


Figure 11. Output Voltage versus Ambient Temperature ( $V_{in} = V_{out} + 1V$ )

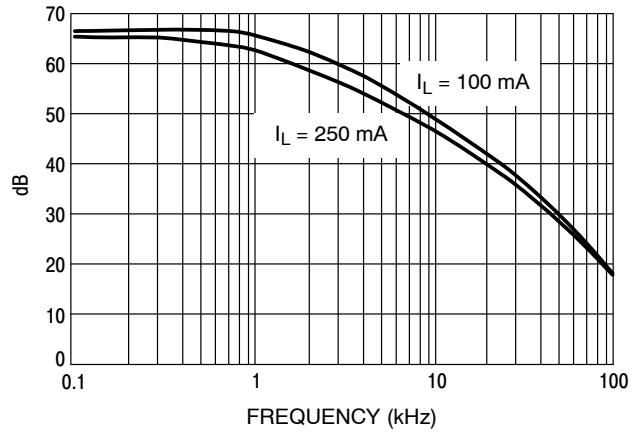
# MC33375, NCV33375 Series



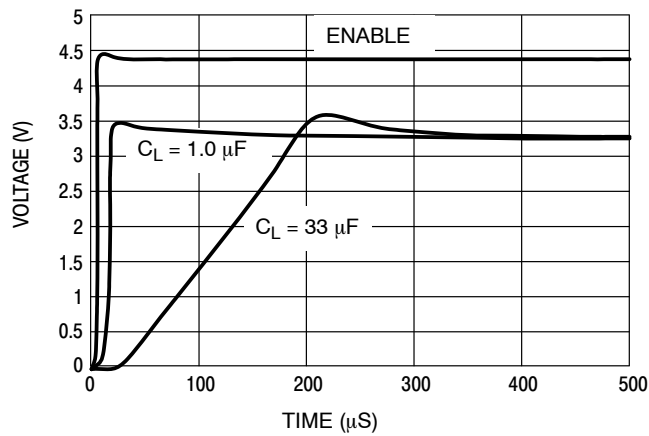
**Figure 12. Output Voltage versus Ambient Temperature ( $V_{in} = 12\text{ V}$ )**



**Figure 13. Ripple Rejection**



**Figure 14. Ripple Rejection**



**Figure 15. Enable Transient**

# MC33375, NCV33375 Series

## 1.8 V Option

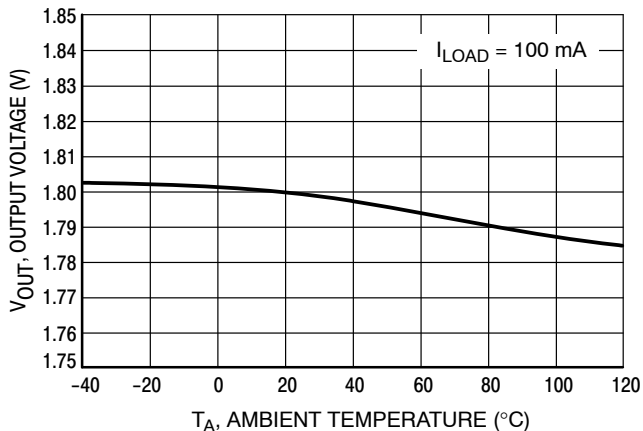


Figure 16. Output Voltage versus Temperature

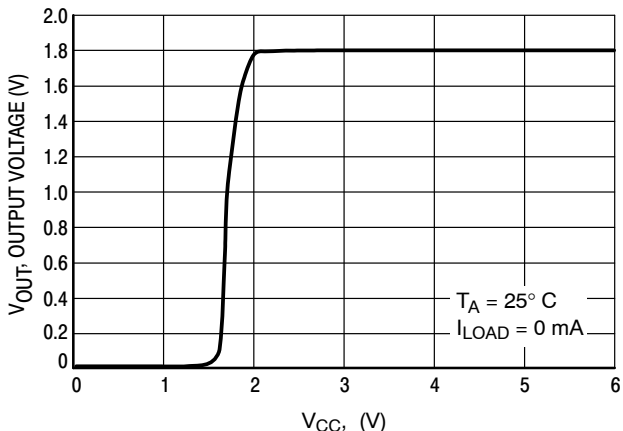


Figure 17. Output Voltage versus Input Voltage

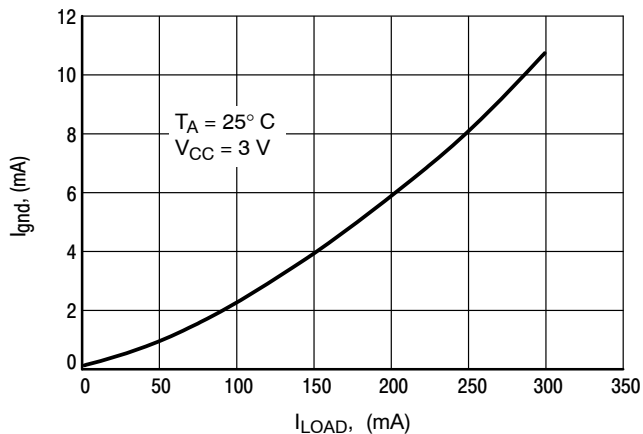


Figure 18. Ground Current versus Load Current

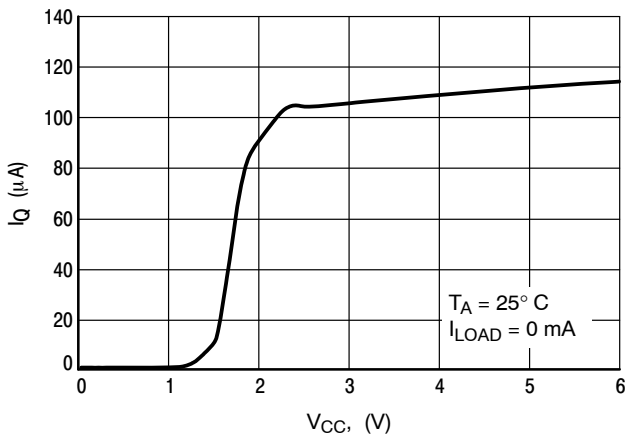


Figure 19. Quiescent Current versus Input Voltage

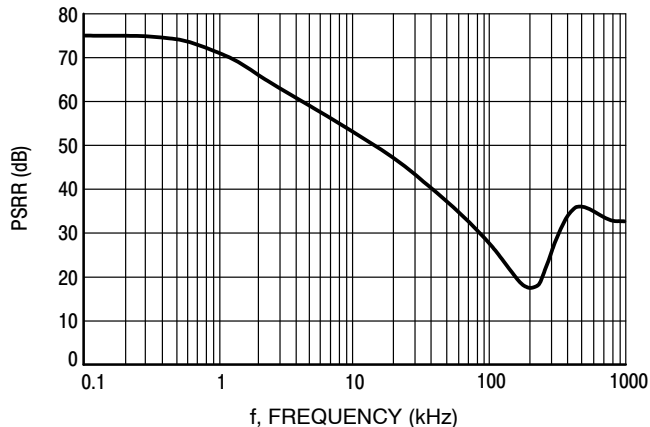


Figure 20. PSRR versus Frequency

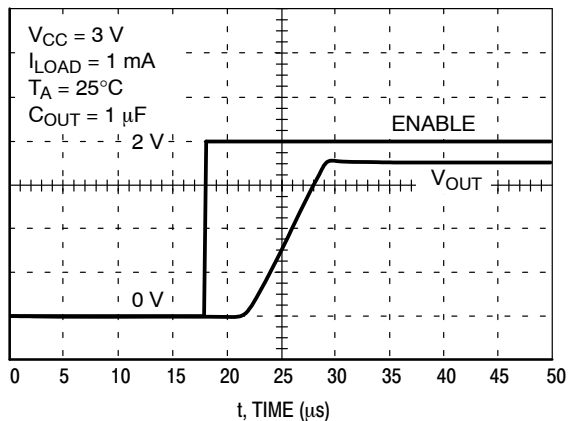


Figure 21. Enable Response

## MC33375, NCV33375 Series

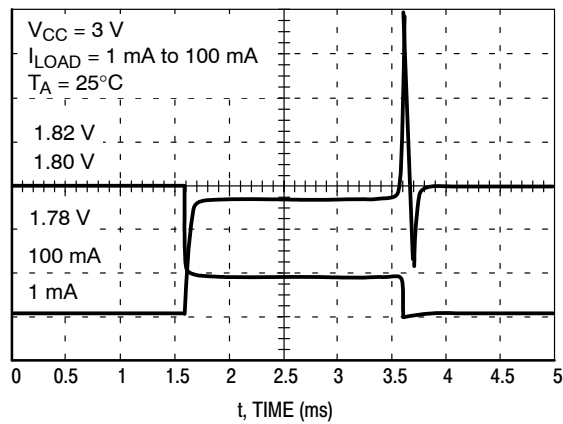


Figure 22. Load Transient Response

### APPLICATIONS INFORMATION

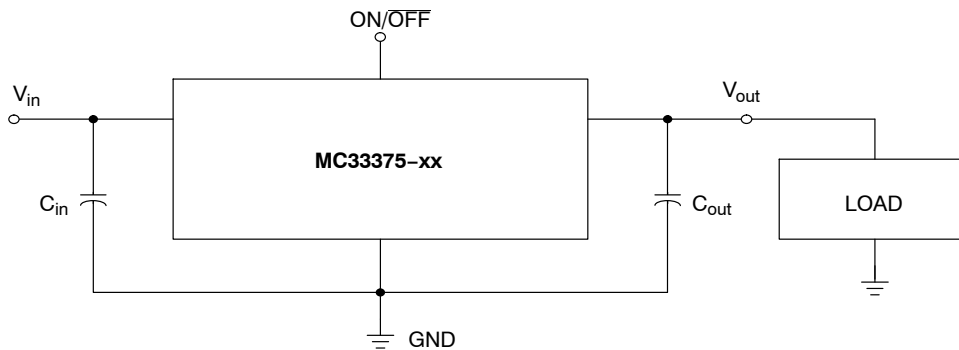


Figure 23. Typical Application Circuit

The MC33375 regulators are designed with internal current limiting and thermal shutdown making them user-friendly. Figure 15 is a typical application circuit. The output capability of the regulator is in excess of 300 mA, with a typical dropout voltage of less than 260 mV. Internal protective features include current and thermal limiting.

#### EXTERNAL CAPACITORS

These regulators require only a 0.33  $\mu\text{F}$  (or greater) capacitance between the output and ground for stability for 1.8 V, 2.5 V, 3.0 V, and 3.3 V output voltage options. Output voltage options of 5.0 V require only 0.22  $\mu\text{F}$  for stability. The output capacitor must be mounted as close as possible to the MC33375. If the output capacitor must be mounted further than two centimeters away from the MC33375, then a larger value of output capacitor may be required for stability. A value of 0.68  $\mu\text{F}$  or larger is recommended. Most type of aluminum, tantalum, or multilayer ceramic will perform adequately. Solid tantalums or appropriate multilayer ceramic capacitors are recommended for operation below 25°C. An input bypass capacitor is recommended to improve transient response or if the regulator is connected to the supply input filter with long wire lengths, more than 4 inches. This will reduce the circuit's sensitivity to the input line impedance at high

frequencies. A 0.33  $\mu\text{F}$  or larger tantalum, mylar, ceramic, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with shortest possible lead or track length directly across the regulator's input terminals. Figure 16 shows the ESR that allows the LDO to remain stable for various load currents.

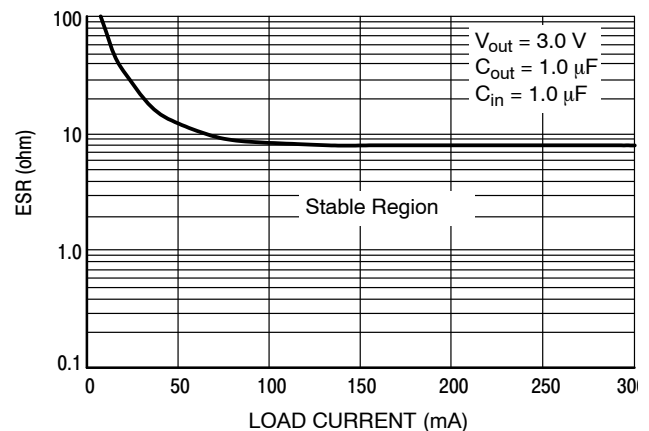


Figure 24. ESR for  $V_{\text{out}} = 3.0\text{V}$

Applications should be tested over all operating conditions to insure stability.

## MC33375, NCV33375 Series

### THERMAL PROTECTION

Internal thermal limiting circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 150°C, the output is disabled. There is no hysteresis built into the thermal protection. As a result the output will appear to be oscillating during thermal limit. The output will turn off until the temperature drops below the 150°C then the output turns on again. The process will repeat if the junction increases above the threshold. This will continue until the existing conditions allow the junction to operate below the temperature threshold.

**Thermal limit is not a substitute for proper heatsinking.**

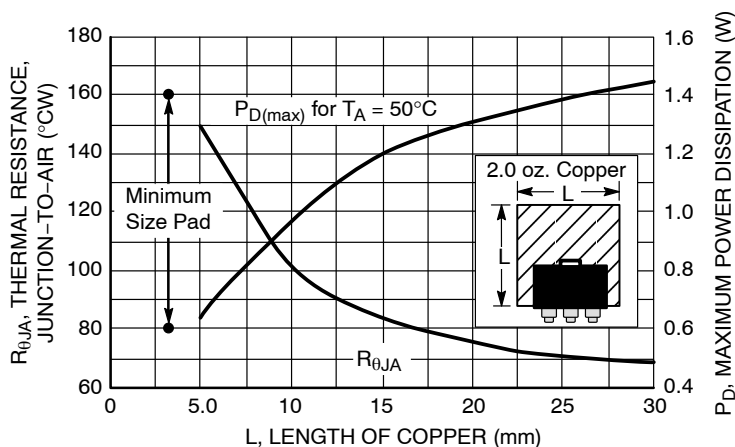
The internal current limit will typically limit current to 450 mA. If during current limit the junction exceeds 150°C, the thermal protection will protect the device also. **Current limit is not a substitute for proper heatsinking.**

### OUTPUT NOISE

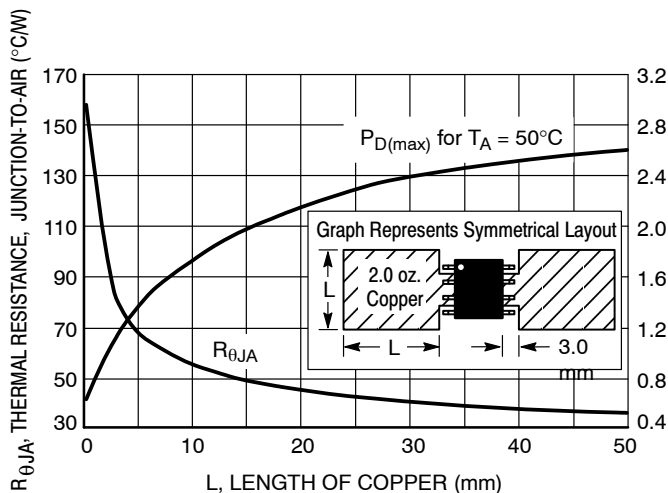
In many applications it is desirable to reduce the noise present at the output. Reducing the regulator bandwidth by increasing the size of the output capacitor will reduce the noise on the MC33375.

### ON/OFF PIN

When this pin is pulled low, the MC33375 is off. This pin should not be left floating. The pin should be pulled high for the MC33375 to operate.



**Figure 25. SOT-223 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length**



**Figure 26. SOP-8 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length**

## MC33375, NCV33375 Series

### ORDERING INFORMATION

Device	Type	Operating Temperature Range, Tolerance	Package	Shipping <sup>†</sup>
MC33375ST-1.8T3G	1.8 V (Fixed Voltage)	1% Tolerance at T <sub>A</sub> = 25°C  2% Tolerance at T <sub>J</sub> from -40 to +125°C	SOT-223 (Pb-Free)	4000 / Tape & Reel
NCV33375ST1.8T3G*				
MC33375D-2.5G	2.5 V (Fixed Voltage)		SOIC-8 (Pb-Free)	98 Units / Rail
MC33375D-2.5R2G			SOIC-8 (Pb-Free)	2500 / Tape & Reel
NCV33375D-2.5R2G*				
MC33375ST-2.5T3G			SOT-223 (Pb-Free)	4000 / Tape & Reel
MC33375D-3.0G	3.0 V (Fixed Voltage)		SOIC-8 (Pb-Free)	98 Units / Rail
MC33375D-3.0R2G			SOIC-8 (Pb-Free)	2500 / Tape & Reel
MC33375ST-3.0T3G			SOT-223 (Pb-Free)	4000 / Tape & Reel
MC33375D-3.3G	3.3 V (Fixed Voltage)		SOIC-8 (Pb-Free)	98 Units / Rail
MC33375D-3.3R2G			SOIC-8 (Pb-Free)	2500 / Tape & Reel
NCV33375D-3.3R2G*				
MC33375ST-3.3T3G			SOT-223 (Pb-Free)	4000 / Tape & Reel
NCV33375ST3.3T3G*				
MC33375D-5.0G	5.0 V (Fixed Voltage)		SOIC-8 (Pb-Free)	98 Units / Rail
MC33375D-5.0R2G			SOIC-8 (Pb-Free)	2500 / Tape & Reel
NCV33375D-5.0R2G*		SOIC-8 (Pb-Free)	2500 / Tape & Reel	
MC33375ST-5.0T3G		SOT-223 (Pb-Free)	4000 / Tape & Reel	

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

### DEVICE MARKING

Device	Version	Marking (1st line)
MC33375, NCV33375	1.8 V	37518
MC33375, NCV33375	2.5 V	37525
MC33375	3.0 V	37530
MC33375, NCV33375	3.3 V	37533
MC33375, NCV33375	5.0 V	37550

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

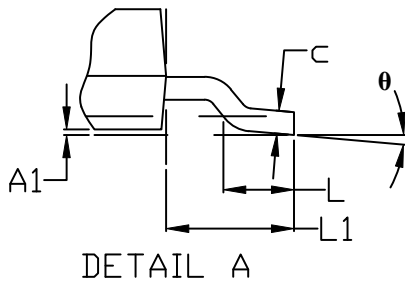
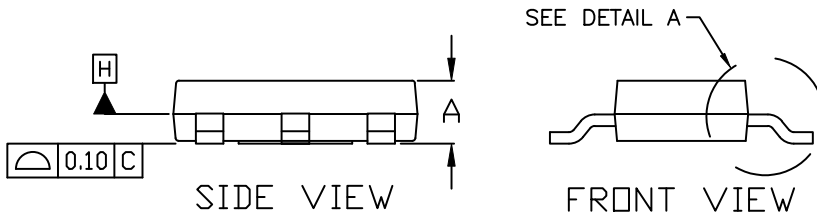
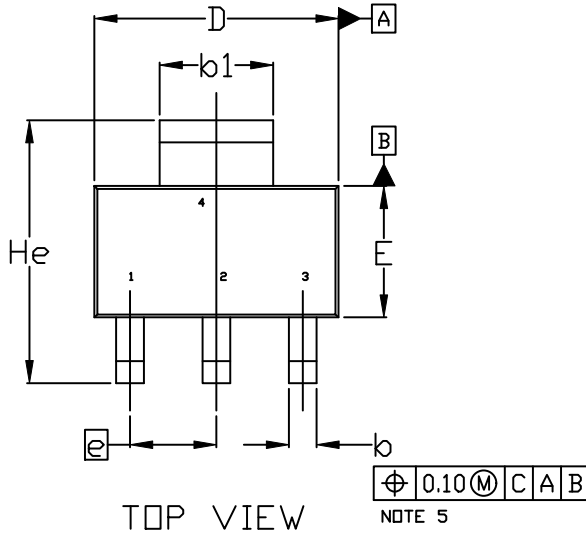
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SCALE 1:1

SOT-223 (TO-261)  
CASE 318E-04  
ISSUE R

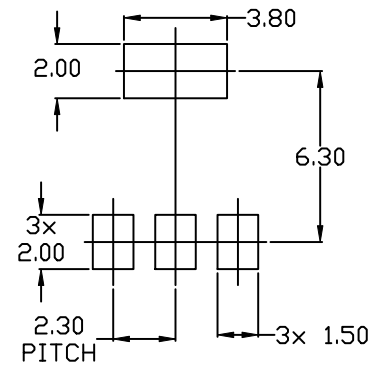
DATE 02 OCT 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
$\theta$	0°	---	10°



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DESCRIPTION:	SOT-223 (TO-261)	PAGE 1 OF 2

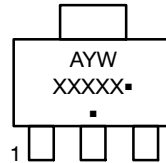
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**SOT-223 (TO-261)**  
**CASE 318E-04**  
**ISSUE R**

DATE 02 OCT 2018

- |  |   |   |   |   |
|--|---|---|---|---|
| <b>STYLE 1:</b><br>PIN 1. BASE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | <b>STYLE 2:</b><br>PIN 1. ANODE<br>2. CATHODE<br>3. NC<br>4. CATHODE        | <b>STYLE 3:</b><br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE<br>4. DRAIN           | <b>STYLE 4:</b><br>PIN 1. SOURCE<br>2. DRAIN<br>3. GATE<br>4. DRAIN   | <b>STYLE 5:</b><br>PIN 1. DRAIN<br>2. GATE<br>3. SOURCE<br>4. GATE    |
| <b>STYLE 6:</b><br>PIN 1. RETURN<br>2. INPUT<br>3. OUTPUT<br>4. INPUT        | <b>STYLE 7:</b><br>PIN 1. ANODE 1<br>2. CATHODE<br>3. ANODE 2<br>4. CATHODE | <b>STYLE 8:</b><br>CANCELLED  | <b>STYLE 9:</b><br>PIN 1. INPUT<br>2. GROUND<br>3. LOGIC<br>4. GROUND | <b>STYLE 10:</b><br>PIN 1. CATHODE<br>2. ANODE<br>3. GATE<br>4. ANODE |
| <b>STYLE 11:</b><br>PIN 1. MT 1<br>2. MT 2<br>3. GATE<br>4. MT 2             | <b>STYLE 12:</b><br>PIN 1. INPUT<br>2. OUTPUT<br>3. NC<br>4. OUTPUT         | <b>STYLE 13:</b><br>PIN 1. GATE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR |   |   |

**GENERIC  
 MARKING DIAGRAM\***




- A = Assembly Location
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

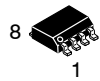
\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

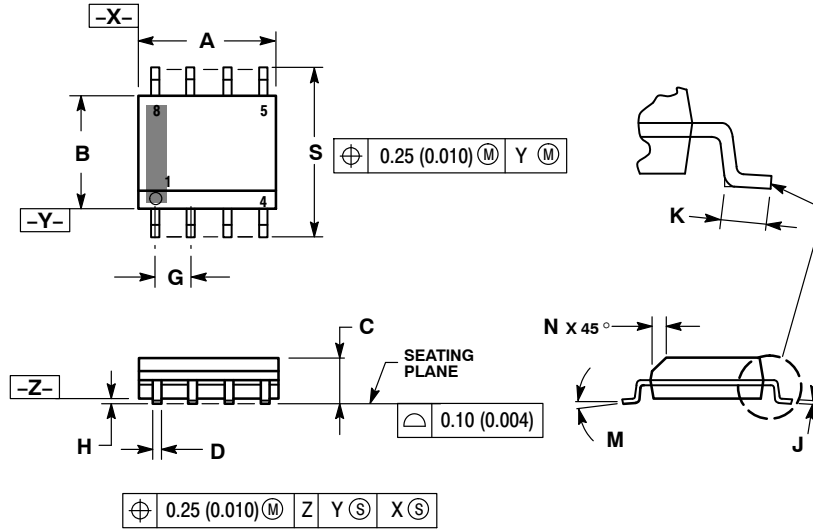
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SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

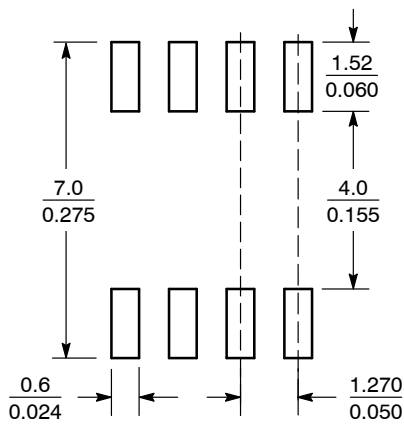
DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

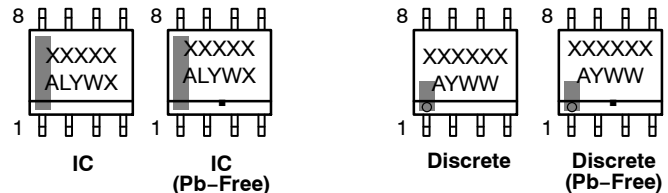
### SOLDERING FOOTPRINT\*



SCALE 6:1 (mm/inches)

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
 A = Assembly Location  
 L = Wafer Lot  
 Y = Year  
 W = Work Week  
 ■ = Pb-Free Package

XXXXXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

- |  |   |   |   |
|--|---|---|---|
| <p><b>STYLE 1:</b><br/>         PIN 1. EMITTER<br/>         2. COLLECTOR<br/>         3. COLLECTOR<br/>         4. EMITTER<br/>         5. EMITTER<br/>         6. BASE<br/>         7. BASE<br/>         8. EMITTER</p>   | <p><b>STYLE 2:</b><br/>         PIN 1. COLLECTOR, DIE, #1<br/>         2. COLLECTOR, #1<br/>         3. COLLECTOR, #2<br/>         4. COLLECTOR, #2<br/>         5. BASE, #2<br/>         6. EMITTER, #2<br/>         7. BASE, #1<br/>         8. EMITTER, #1</p>               | <p><b>STYLE 3:</b><br/>         PIN 1. DRAIN, DIE #1<br/>         2. DRAIN, #1<br/>         3. DRAIN, #2<br/>         4. DRAIN, #2<br/>         5. GATE, #2<br/>         6. SOURCE, #2<br/>         7. GATE, #1<br/>         8. SOURCE, #1</p>                            | <p><b>STYLE 4:</b><br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. ANODE<br/>         4. ANODE<br/>         5. ANODE<br/>         6. ANODE<br/>         7. ANODE<br/>         8. COMMON CATHODE</p>   |
| <p><b>STYLE 5:</b><br/>         PIN 1. DRAIN<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. DRAIN<br/>         5. GATE<br/>         6. GATE<br/>         7. SOURCE<br/>         8. SOURCE</p>   | <p><b>STYLE 6:</b><br/>         PIN 1. SOURCE<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. SOURCE<br/>         5. SOURCE<br/>         6. GATE<br/>         7. GATE<br/>         8. SOURCE</p>  | <p><b>STYLE 7:</b><br/>         PIN 1. INPUT<br/>         2. EXTERNAL BYPASS<br/>         3. THIRD STAGE SOURCE<br/>         4. GROUND<br/>         5. DRAIN<br/>         6. GATE 3<br/>         7. SECOND STAGE Vd<br/>         8. FIRST STAGE Vd</p>                    | <p><b>STYLE 8:</b><br/>         PIN 1. COLLECTOR, DIE #1<br/>         2. BASE, #1<br/>         3. BASE, #2<br/>         4. COLLECTOR, #2<br/>         5. COLLECTOR, #2<br/>         6. EMITTER, #2<br/>         7. EMITTER, #1<br/>         8. COLLECTOR, #1</p>                              |
| <p><b>STYLE 9:</b><br/>         PIN 1. EMITTER, COMMON<br/>         2. COLLECTOR, DIE #1<br/>         3. COLLECTOR, DIE #2<br/>         4. EMITTER, COMMON<br/>         5. EMITTER, COMMON<br/>         6. BASE, DIE #2<br/>         7. BASE, DIE #1<br/>         8. EMITTER, COMMON</p> | <p><b>STYLE 10:</b><br/>         PIN 1. GROUND<br/>         2. BIAS 1<br/>         3. OUTPUT<br/>         4. GROUND<br/>         5. GROUND<br/>         6. BIAS 2<br/>         7. INPUT<br/>         8. GROUND</p>  | <p><b>STYLE 11:</b><br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. DRAIN 2<br/>         7. DRAIN 1<br/>         8. DRAIN 1</p>   | <p><b>STYLE 12:</b><br/>         PIN 1. SOURCE<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p><b>STYLE 13:</b><br/>         PIN 1. N.C.<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>  | <p><b>STYLE 14:</b><br/>         PIN 1. N-SOURCE<br/>         2. N-GATE<br/>         3. P-SOURCE<br/>         4. P-GATE<br/>         5. P-DRAIN<br/>         6. P-DRAIN<br/>         7. N-DRAIN<br/>         8. N-DRAIN</p>   | <p><b>STYLE 15:</b><br/>         PIN 1. ANODE 1<br/>         2. ANODE 1<br/>         3. ANODE 1<br/>         4. ANODE 1<br/>         5. CATHODE, COMMON<br/>         6. CATHODE, COMMON<br/>         7. CATHODE, COMMON<br/>         8. CATHODE, COMMON</p>               | <p><b>STYLE 16:</b><br/>         PIN 1. EMITTER, DIE #1<br/>         2. BASE, DIE #1<br/>         3. EMITTER, DIE #2<br/>         4. BASE, DIE #2<br/>         5. COLLECTOR, DIE #2<br/>         6. COLLECTOR, DIE #2<br/>         7. COLLECTOR, DIE #1<br/>         8. COLLECTOR, DIE #1</p> |
| <p><b>STYLE 17:</b><br/>         PIN 1. VCC<br/>         2. V2OUT<br/>         3. V1OUT<br/>         4. TXE<br/>         5. RXE<br/>         6. VEE<br/>         7. GND<br/>         8. ACC</p>  | <p><b>STYLE 18:</b><br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. CATHODE<br/>         8. CATHODE</p>   | <p><b>STYLE 19:</b><br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. MIRROR 2<br/>         7. DRAIN 1<br/>         8. MIRROR 1</p>   | <p><b>STYLE 20:</b><br/>         PIN 1. SOURCE (N)<br/>         2. GATE (N)<br/>         3. SOURCE (P)<br/>         4. GATE (P)<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p><b>STYLE 21:</b><br/>         PIN 1. CATHODE 1<br/>         2. CATHODE 2<br/>         3. CATHODE 3<br/>         4. CATHODE 4<br/>         5. CATHODE 5<br/>         6. COMMON ANODE<br/>         7. COMMON ANODE<br/>         8. CATHODE 6</p>  | <p><b>STYLE 22:</b><br/>         PIN 1. I/O LINE 1<br/>         2. COMMON CATHODE/VCC<br/>         3. COMMON CATHODE/VCC<br/>         4. I/O LINE 3<br/>         5. COMMON ANODE/GND<br/>         6. I/O LINE 4<br/>         7. I/O LINE 5<br/>         8. COMMON ANODE/GND</p> | <p><b>STYLE 23:</b><br/>         PIN 1. LINE 1 IN<br/>         2. COMMON ANODE/GND<br/>         3. COMMON ANODE/GND<br/>         4. LINE 2 IN<br/>         5. LINE 2 OUT<br/>         6. COMMON ANODE/GND<br/>         7. COMMON ANODE/GND<br/>         8. LINE 1 OUT</p> | <p><b>STYLE 24:</b><br/>         PIN 1. BASE<br/>         2. EMITTER<br/>         3. COLLECTOR/ANODE<br/>         4. COLLECTOR/ANODE<br/>         5. CATHODE<br/>         6. CATHODE<br/>         7. COLLECTOR/ANODE<br/>         8. COLLECTOR/ANODE</p>                                      |
| <p><b>STYLE 25:</b><br/>         PIN 1. VIN<br/>         2. N/C<br/>         3. REXT<br/>         4. GND<br/>         5. IOUT<br/>         6. IOUT<br/>         7. IOUT<br/>         8. IOUT</p>   | <p><b>STYLE 26:</b><br/>         PIN 1. GND<br/>         2. dv/dt<br/>         3. ENABLE<br/>         4. ILIMIT<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. VCC</p>  | <p><b>STYLE 27:</b><br/>         PIN 1. ILIMIT<br/>         2. OVLO<br/>         3. UVLO<br/>         4. INPUT+<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. DRAIN</p>  | <p><b>STYLE 28:</b><br/>         PIN 1. SW_TO_GND<br/>         2. DASIC OFF<br/>         3. DASIC_SW_DET<br/>         4. GND<br/>         5. V_MON<br/>         6. VBULK<br/>         7. VBULK<br/>         8. VIN</p>  |
| <p><b>STYLE 29:</b><br/>         PIN 1. BASE, DIE #1<br/>         2. EMITTER, #1<br/>         3. BASE, #2<br/>         4. EMITTER, #2<br/>         5. COLLECTOR, #2<br/>         6. COLLECTOR, #2<br/>         7. COLLECTOR, #1<br/>         8. COLLECTOR, #1</p>                        | <p><b>STYLE 30:</b><br/>         PIN 1. DRAIN 1<br/>         2. DRAIN 1<br/>         3. GATE 2<br/>         4. SOURCE 2<br/>         5. SOURCE 1/DRAIN 2<br/>         6. SOURCE 1/DRAIN 2<br/>         7. SOURCE 1/DRAIN 2<br/>         8. GATE 1</p>                           |   |   |

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