THE DATASHEET OF

NCV8668ABPD33R2G

NCV8668

LDO Regulator - Very Low I_q, Window Watchdog, Enable and Reset

150 mA

The NCV8668 is 150 mA LDO regulator with integrated window watchdog and reset functions dedicated for microprocessor applications. Its robustness allows NCV8668 to be used in severe automotive environments. Very low quiescent current as low as 38 μA typical makes it suitable for applications permanently connected to battery requiring very low quiescent current with or without load. The Enable function can be used for further decrease of quiescent current down to 1 μA.

The NCV8668 contains protection functions as current limit and thermal shutdown.

Features

- Output Voltage Options: 3.3 V and 5 V
- Output Voltage Accuracy: ±1.5% (T_J = 25°C to 125°C)
- Output Current up to 150 mA
- Very Low Quiescent Current: Typ 38 μA (max 43 μA)
- Very Low Dropout Voltage
- Enable Function
- Microprocessor Compatible Control Functions:
  - Reset with Adjustable Power−on Delay
  - Window Watchdog
- Wide Input Voltage Operation Range: up to 40 V
- Protection Features:
  - Current Limitation
  - Reverse Output Current
  - Thermal Shutdown
- These are Pb−Free Devices

Typical Applications

- Body Control Module
- Instruments and Clusters
- Occupant Protection and Comfort
- Powertrain

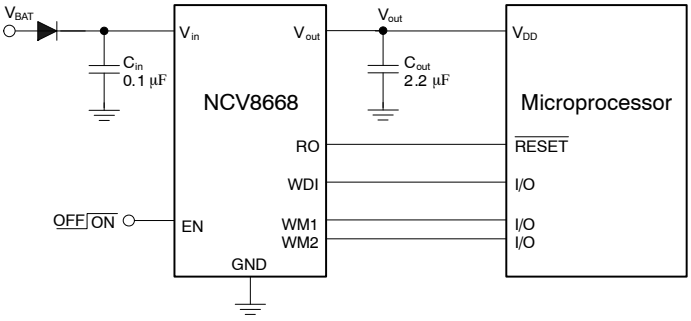

Figure 1. Application Schematic

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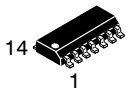
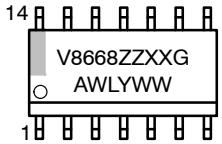
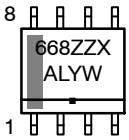
MARKING DIAGRAMS



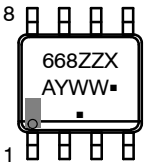
SOIC−14
CASE 751A



SOIC−8
D SUFFIX
CASE 751A



SOIC−8 EP
CASE 751AC

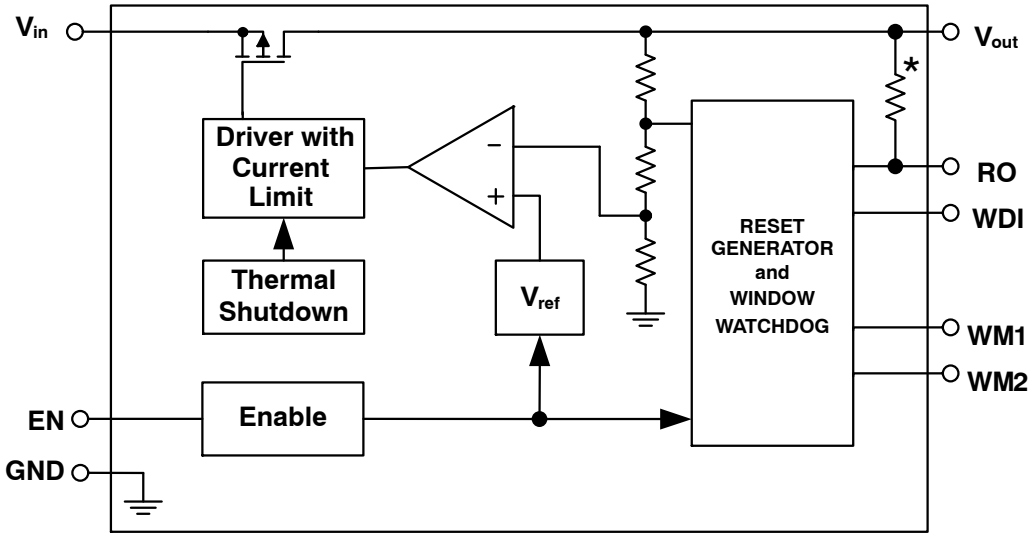


ZZ	=	Timing, Reset Threshold, Watchdog Control Options*
XX,X	=	Voltage Options = 5 V (XX = 50, X = 5) = 3.3 V (XX = 33, X = 3)
A	=	Assembly Location
WL, L	=	Wafer Lot
YY, Y	=	Year
WW, W	=	Work Week
G or ▪	=	Pb−Free Package

*See APPLICATION INFORMATION Section.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 15 of this data sheet.



*** 5 V OPTION ONLY**

Figure 2. Simplified Block Diagram

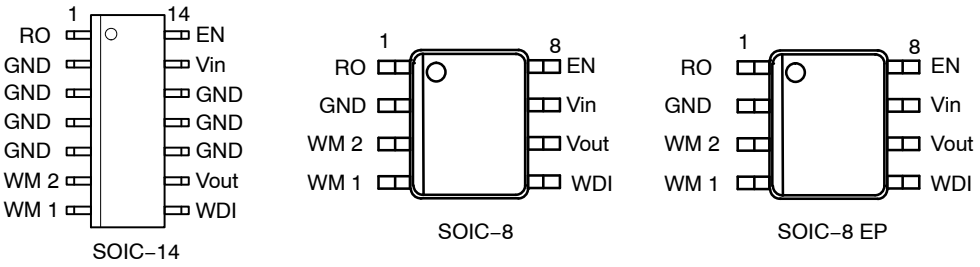


Figure 3. Pin Connections (Top View)

PIN FUNCTION DESCRIPTION

Pin No. SOIC−14	Pin No. SOIC−8	Pin No. SOIC−8 EP	Pin Name	Description
1	1	1	RO	Reset Output. 30 kΩ internal Pull−Up resistor connected to V_{out}. (Open Drain output for 2.5 V, 2.6 V, and 3.3 V voltage options) RO goes Low when V_{out} drops by more than 7% from nominal.
2, 3, 4, 5, 10, 11, 12	2	2	GND	Power Supply Ground. For SOIC−14 − connect pin 2 and 3 to GND − connect pin 4−5 and 10−12 to heatsink area with GND potential
6	3	3	WM2	Watchdog Mode Bit 2; Watchdog and Reset mode selection. Connect to V_{out} or GND.
7	4	4	WM1	Watchdog Mode Bit 1; Watchdog and Reset mode selection. Connect to V_{out} or GND.
8	5	5	WDI	Watchdog Input; Trigger Input for Watchdog pulses. When not used, connect to V_{out} or GND.
9	6	6	V_{out}	Regulated Output Voltage. Connect 2.2 μF capacitor with ESR < 100 Ω to ground.
13	7	7	V_{in}	Positive Power Supply Input. Connect 0.1 μF capacitor to ground.
14	8	8	EN	Enable Input; low level disables the IC.
		EPAD	GND	Exposed Pad is Connected to Ground

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Input Voltage (Note 1) DC Transient, t < 100 ms	V_{in}	 −0.3 −	 40 45	V
Input Current	I_{in}	−5	−	mA
Output Voltage (Note 2)	V_{out}	−0.3	5.5	V
Output Current	I_{out}	−3	Current Limited	mA
Enable Input Voltage Range DC Transient, t < 100 ms	V_{EN}	 −0.3 −	 40 45	V
Enable Input Current Range	I_{EN}	−1	1	mA
Reset Output Voltage (Note 3)	V_{RO}	−0.3	5.5	V
Reset Output Current	I_{RO}	−3	3	mA
Watchdog Input Voltage	V_{WDI}	−0.3	5.5	V
Watchdog Mode 1 Voltage	V_{WM1}	−0.3	5.5	V
Watchdog Mode 1 Current	I_{WM1}	−5	5	mA
Watchdog Mode 2 Voltage	V_{WM2}	−0.3	5.5	V
Watchdog Mode 2 Current	I_{WM2}	−5	5	mA
Junction Temperature	T_J	−40	150	°C
Storage Temperature	TSTG	−55	150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. The Output voltage must not exceed the Input voltage.
3. The Reset Output voltage must not exceed the Output voltage.

ESD CAPABILITY (Note 4)

Rating	Symbol	Min	Max	Unit
ESD Capability, Human Body Model	ESD_{HBM}	−2	2	kV
ESD Capability, Machine Model	ESD_{MM}	−200	200	V

4. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (JS−001−2010)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)

LEAD SOLDERING TEMPERATURE AND MSL (Note 5)

Rating	Symbol	Min	Max	Unit
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 5)	T_{SLD}	−	265 peak	°C
Moisture Sensitivity Level (SOIC−14, SOIC−8) (SOIC−8EP)	MSL	 1 2		−

5. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

THERMAL CHARACTERISTICS (Note 6)

Rating	Symbol	Value	Unit
Thermal Characteristics, SOIC−14 (Note 6) Thermal Resistance, Junction−to−Air (Note 7) Thermal Reference, Junction−to−Lead4 (Note 7)	 $R_{\theta JA}$ $R_{\Psi JL}$	 95 18.2	°C/W
Thermal Characteristics, SOIC−8 (Note 6) Thermal Resistance, Junction−to−Air (Note 7) Thermal Reference, Junction−to−Lead4 (Note 7)	 $R_{\theta JA}$ $R_{\Psi JL}$	 132 49.2	°C/W
Thermal Characteristics, SOIC−8 EP (Note 6) Thermal Resistance, Junction−to−Air (Note 7) Thermal Reference, Junction−to−Lead4 (Note 7) Thermal Reference, Junction−to−Pad (Note 7)	 $R_{\theta JA}$ $R_{\Psi JL4}$ $R_{\Psi JPad}$	 80 28.5 14.8	°C/W

6. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
7. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

RECOMMENDED OPERATING RANGES (Note 8)

Rating	Symbol	Min	Max	Unit
Input Voltage (Note 9)	V_{in}	4.5	40	V
Junction Temperature	T_J	−40	150	°C

8. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
9. Minimum V_{in} = 4.5 V or (V_{out} + V_{DO}), whichever is higher.

ELECTRICAL CHARACTERISTICS

V_{in} = 13.2 V, C_{in} = 0.1 μF, C_{out} = 2.2 μF, for typical values T_J = 25°C, for min/max values T_J = −40°C to 150°C; unless otherwise noted. (Notes 10 and 11)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
REGULATOR OUTPUT						
Output Voltage (Accuracy %) 3.3 V 5.0 V	T_J = 25°C to 125°C V_{in} = 4.5 V to 16 V, I_{out} = 0.1 mA to 100 mA V_{in} = 5.5 V to 16 V, I_{out} = 0.1 mA to 100 mA	V_{out}	 3.2505 4.925 (−1.5%)	 3.3 5.0	 3.3495 5.075 (+1.5%)	V
Output Voltage (Accuracy %) 3.3 V 5.0 V	 V_{in} = 4.5 V to 40 V, I_{out} = 0.1 mA to 100 mA V_{in} = 4.5 V to 16 V, I_{out} = 0.1 mA to 150 mA V_{in} = 5.55 V to 40 V, I_{out} = 0.1 mA to 100 mA V_{in} = 5.7 V to 16 V, I_{out} = 0.1 mA to 150 mA	V_{out}	 3.234 3.234 4.9 4.9 (−2%)	 3.3 3.3 5.0 5.0	 3.366 3.366 5.1 5.1 (+2%)	V
Output Voltage (Accuracy %) 3.3 V 5.0 V	T_J = −40°C to 125°C V_{in} = 4.5 V to 28 V, I_{out} = 0 mA V_{in} = 5.5 V to 28 V, I_{out} = 0 mA	V_{out}	 3.234 4.9 (−2%)	 3.3 5.0	 3.366 5.1 (+2%)	V
Line Regulation 5.0 V 3.3 V	 V_{in} = 5.5 V to 28 V, I_{out} = 5 mA V_{in} = 4.5 V to 28 V, I_{out} = 5 mA	Reg_{line}	−20	0	20	mV
Load Regulation	I_{out} = 0.1 mA to 150 mA	Reg_{load}	−40	10	40	mV
Dropout Voltage (Note 12) 5.0 V	 I_{out} = 100 mA I_{out} = 150 mA	V_{DO}	 − −	 225 300	 450 600	mV
Output Capacitor for Stability (Note 13)	 I_{out} = 5 mA to 150 mA I_{out} = 0 mA to 5 mA	C_{out} ESR	2.2 − 1	− − −	− 100 100	μF Ω Ω

10. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
11. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
12. Measured when output voltage falls 100 mV below the regulated voltage at V_{in} = 13.2 V. If V_{out} < 5 V, then $V_{DO} = V_{in} - V_{out}$. Maximum dropout voltage value is limited by minimum input voltage V_{in} = 4.5 V recommended for guaranteed operation at maximum output current.
13. Values based on design and/or characterization.
14. Recommended for typical trigger time. $T_{WD} = t_{CW} + 1/2 * t_{OW}$

ELECTRICAL CHARACTERISTICS

V_{in} = 13.2 V, C_{in} = 0.1 μF, C_{out} = 2.2 μF, for typical values T_J = 25°C, for min/max values T_J = −40°C to 150°C; unless otherwise noted. (Notes 10 and 11)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Disable and Quiescent Current						
Disable Current	V_{EN} = 0 V,T_J < 85°C	I_{DIS}	–	–	1	μA
Quiescent Current ($I_q = I_{in} - I_{out}$)	I_{out} = 100 μA, T_J = 25°C I_{out} = 100 μA, $T_J \leq$ 125°C	I_q	– –	38 –	43 44	μA
Current Limit Protection						
Current Limit	V_{out} = 0.96 x V_{out_nom}	I_{LIM}	205	–	525	mA
Short Circuit Current Limit	V_{out} = 0 V	I_{SC}	205	–	525	mA
Reverse Output Current Protection						
Reverse Output Current Protection	V_{EN} = 0 V, I_{out} = −1 mA	V_{out_rev}	–	2	5.5	V
PSRR						
Power Supply Ripple Rejection (Note 13)	f = 100 Hz, 0.5V_{pp}	PSRR	–	60	–	dB
Enable Thresholds						
Enable Input Threshold Voltage Logic High Logic Low		$V_{th(EN)}$	 3 –	 – –	 – 0.8	V
Enable Input Current Logic High Logic Low	 V_{EN} = 5 V V_{EN} = 0 V, T_J < 85°C	 I_{EN_ON} I_{EN_OFF}	 – –	 3 0.5	 5 1	μA
Window Watchdog						
Watchdog Mode Bit 1 Threshold Voltage Voltage Increasing, Logic High 3.3 V 5.0 V Voltage Decreasing, Logic Low		 $V_{WM1,H}$ $V_{WM1,L}$	 – – 0.8	 – – –	 2.65 4.0 –	V
Watchdog Mode Bit 2 Threshold Voltage Voltage Increasing, Logic High 3.3 V 5.0 V Voltage Decreasing, Logic Low		 $V_{WM2,H}$ $V_{WM2,L}$	 – – 0.8	 – – –	 2.65 4.0 –	V
Watchdog Input WDI Threshold Voltage Voltage Increasing, Logic High 3.3 V 5.0 V Voltage Decreasing, Logic Low		 $V_{WDI,H}$ $V_{WDI,L}$	 – – 0.8	 – – –	 2.65 4.0 –	V
Watchdog Input WDI Current Logic High Logic Low	 $V_{WDI,H}$ = 5 V $V_{WDI,L}$ = 0 V, T_J < 85 °C	 $I_{WDI,H}$ $I_{WDI,L}$	 – –	 3 0.5	 4 1	μA
Watchdog Sampling Time	Fast: WM2 = L Slow: WM1 = L AND WM2 = H	t_{sam}	0.4 0.8	0.5 1.0	0.6 1.2	ms
Ignore Window Time	Fast: WM2 = L Slow: WM1 = L AND WM2 = H	t_{IW}	25.6 51.2	32.0 64.0	38.4 76.8	ms
Open Window Time	Fast: WM2 = L Slow: WM1 = L AND WM2 = H	t_{OW}	25.6 51.2	32.0 64.0	38.4 76.8	ms
Closed Window Time	Fast: WM2 = L Slow: WM1 = L AND WM2 = H	t_{CW}	25.6 51.2	32.0 64.0	38.4 76.8	ms

10. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
11. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
12. Measured when output voltage falls 100 mV below the regulated voltage at V_{in} = 13.2 V. If V_{out} < 5 V, then $V_{DO} = V_{in} - V_{out}$. Maximum dropout voltage value is limited by minimum input voltage V_{in} = 4.5 V recommended for guaranteed operation at maximum output current.
13. Values based on design and/or characterization.
14. Recommended for typical trigger time. $T_{WD} = t_{CW} + 1/2 * t_{OW}$

ELECTRICAL CHARACTERISTICS

V_{in} = 13.2 V, C_{in} = 0.1 μF, C_{out} = 2.2 μF, for typical values T_J = 25°C, for min/max values T_J = −40°C to 150°C; unless otherwise noted. (Notes 10 and 11)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Window Watchdog						
Window Watchdog Trigger Time (Note 14)	Fast: WM2 = L Slow: WM1 = L AND WM2 = H	t_{WD}	– –	48 96	– –	ms
Watchdog Deactivation Current Threshold 3.3 V 5.0 V	I_{out} decreasing V_{in} > 4.5 V V_{in} > 5.5 V	$I_{out\_WD\_OFF}$	 0.5 0.5	 – –	 – –	mA
Watchdog Activating Current Threshold 3.3 V 5.0 V	I_{out} increasing V_{in} > 4.5 V V_{in} > 5.5 V	$I_{out\_WD\_ON}$	 – –	 2 2	 5 5	mA
Reset Output RO						
Input Voltage Reset Threshold 3.3 V	V_{in} decreasing, V_{out} > V_{RT}	V_{in_RT}	 –	 3.8	 4.2	V
Output Voltage Reset Threshold 3.3 V 5.0 V	V_{out} decreasing V_{in} > 4.5 V V_{in} > 5.5 V	V_{RT}	 90 90	 93 93	 96 96	%V_{out}
Reset Hysteresis		V_{RH}	–	2.0	–	%V_{out}
Maximum Reset Sink Current 3.3 V 5.0 V	 V_{out} = 3 V, V_{RO} = 0.25 V V_{out} = 4.5 V, V_{RO} = 0.25 V	I_{Romax}	 1.3 1.75	 – –	 – –	mA
Reset Output Low Voltage	V_{out} > 1 V, I_{RO} < 200 μA	V_{ROL}	–	0.15	0.25	V
Reset Output High Voltage 5.0 V		V_{ROH}	4.5	–	–	V
Reset High Level Leakage Current 3.3 V		I_{ROLK}	–	–	1	μA
Integrated Reset Pull Up Resistor 5.0 V		R_{RO}	15	30	50	kΩ
Reset Delay Time	Fast: WM1 = L AND WM2 = L Slow:WM1 = H OR (WM1 = L AND WM2 = H)	t_{RD}	12.8 25.6	16 32	19.2 38.4	ms
Reset Reaction Time (See Figure 24)		t_{RR}	16	25	38	μs
THERMAL SHUTDOWN						
Thermal Shutdown Temperature (Note 13)		T_{SD}	150	175	195	°C
Thermal Shutdown Hysteresis (Note 13)		T_{SH}	–	25	–	°C

10. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
11. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
12. Measured when output voltage falls 100 mV below the regulated voltage at V_{in} = 13.2 V. If V_{out} < 5 V, then $V_{DO} = V_{in} - V_{out}$. Maximum dropout voltage value is limited by minimum input voltage V_{in} = 4.5 V recommended for guaranteed operation at maximum output current.
13. Values based on design and/or characterization.
14. Recommended for typical trigger time. $T_{WD} = t_{CW} + 1/2 * t_{OW}$

TYPICAL CHARACTERISTICS

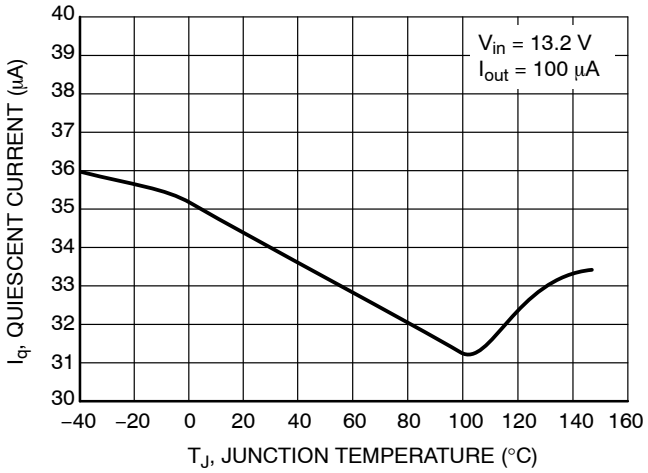


Figure 4. Quiescent Current vs Temperature

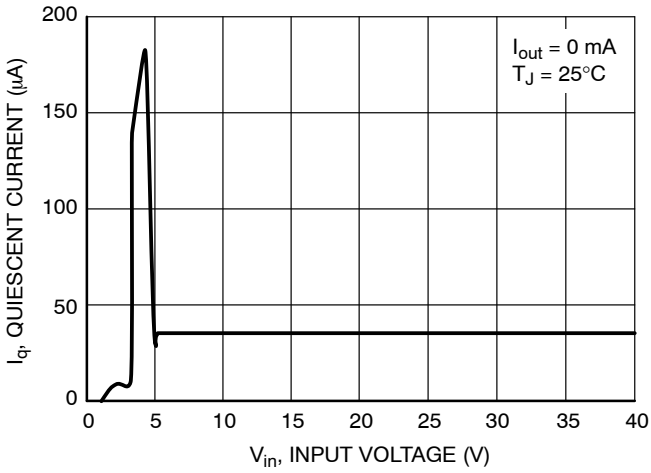


Figure 5. Quiescent Current vs Input Voltage (5 V option)

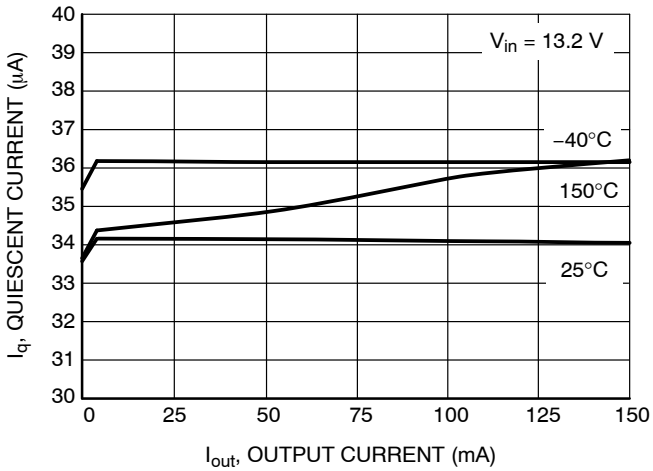


Figure 6. Quiescent Current vs Output Current

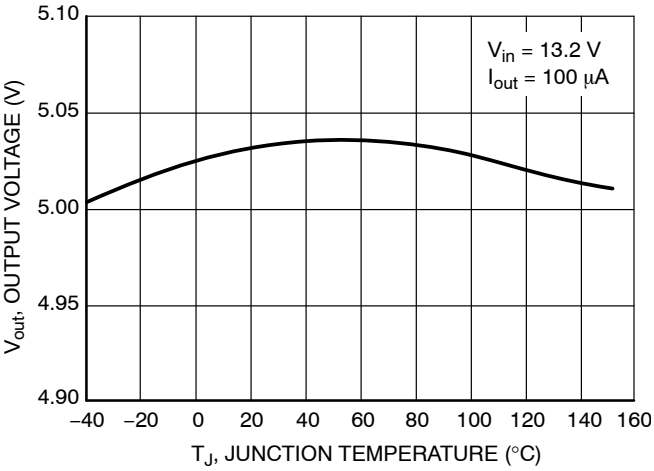


Figure 7. Output Voltage vs Temperature (5 V option)

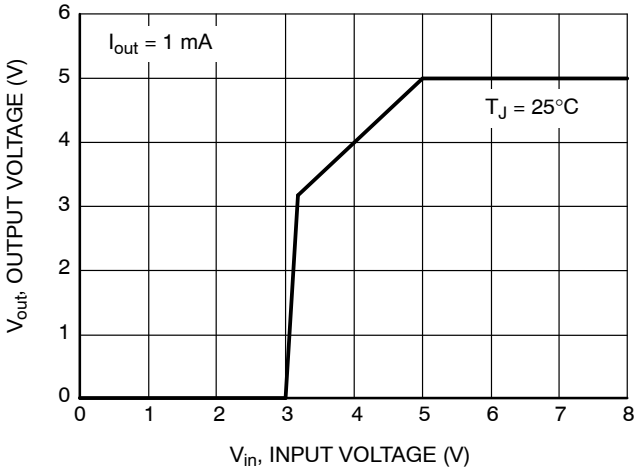


Figure 8. Output Voltage vs Input Voltage (5 V option)

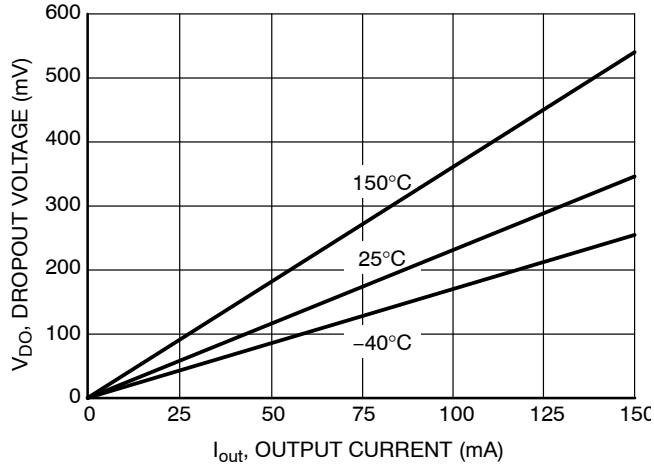


Figure 9. Dropout Voltage vs Output Current (5 V option)

TYPICAL CHARACTERISTICS

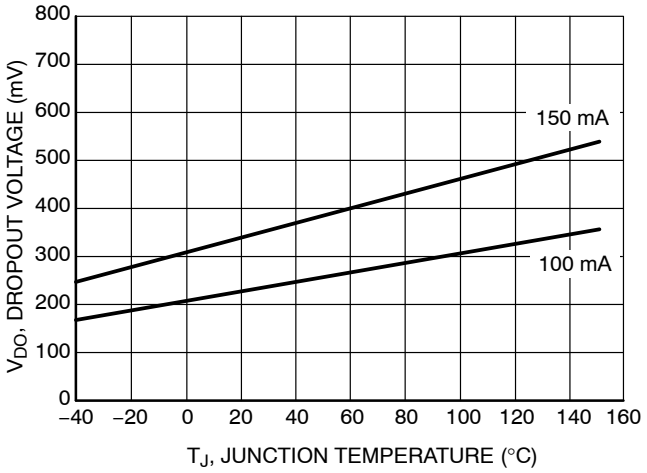


Figure 10. Dropout vs Temperature (5 V option)

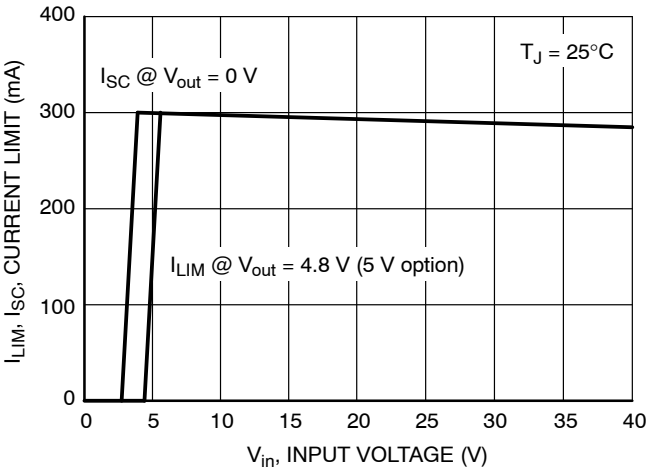


Figure 11. Current Limit vs. Input Voltage

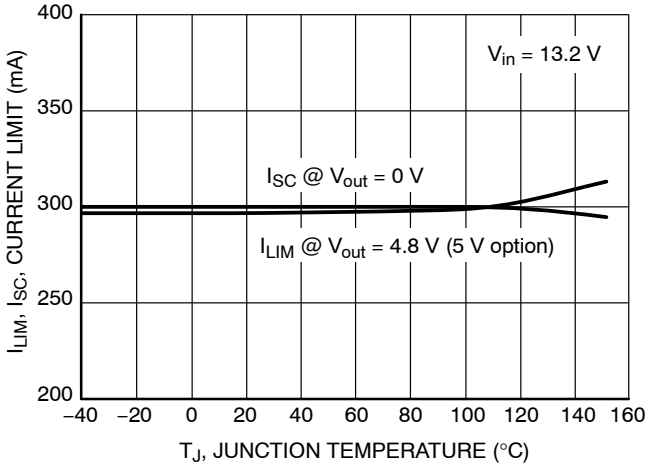


Figure 12. Current Limit vs. Temperature

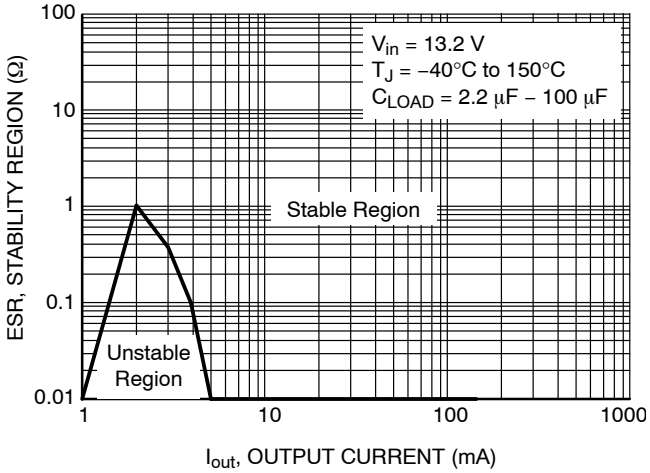


Figure 13. C_{out} ESR Stability Region vs Output Current

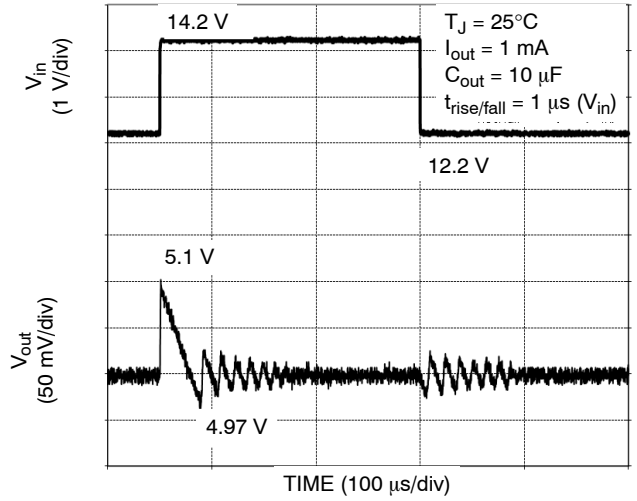


Figure 14. Line Transients (5 V option)

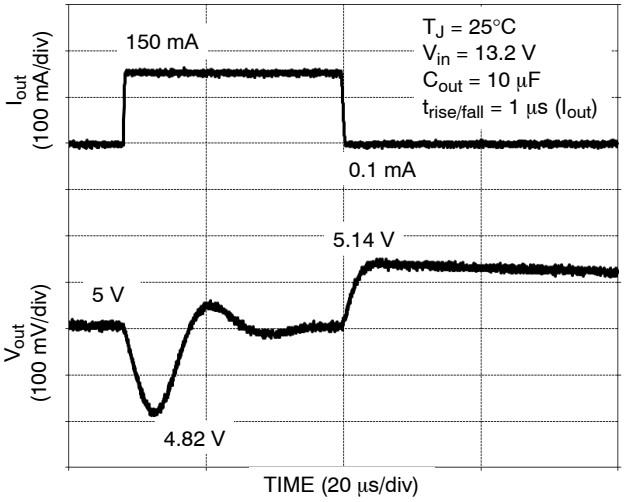


Figure 15. Load Transients (5 V option)

TYPICAL CHARACTERISTICS

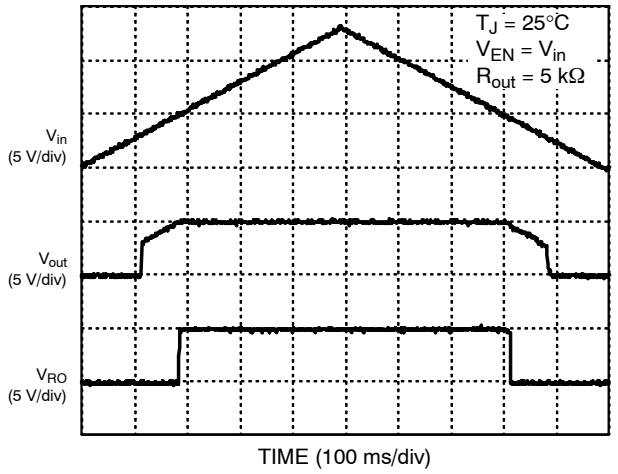


Figure 16. Power Up/Down Response (5 V option)

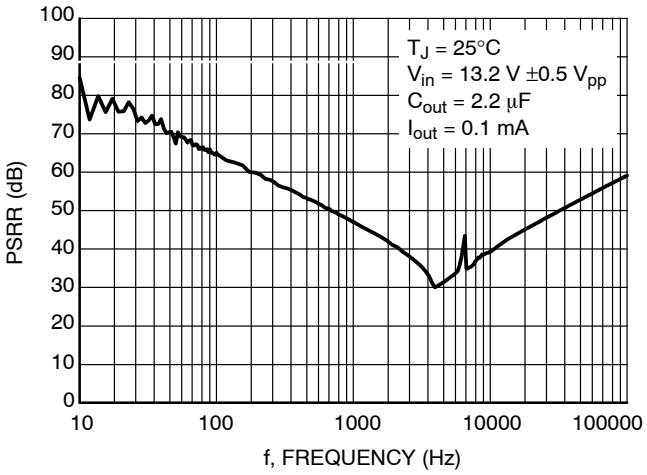


Figure 17. PSRR vs. Frequency (5 V option)

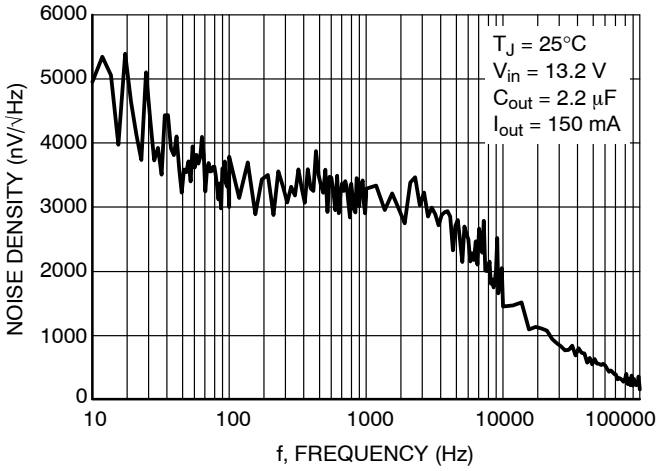


Figure 18. Noise vs. Frequency (5 V option)

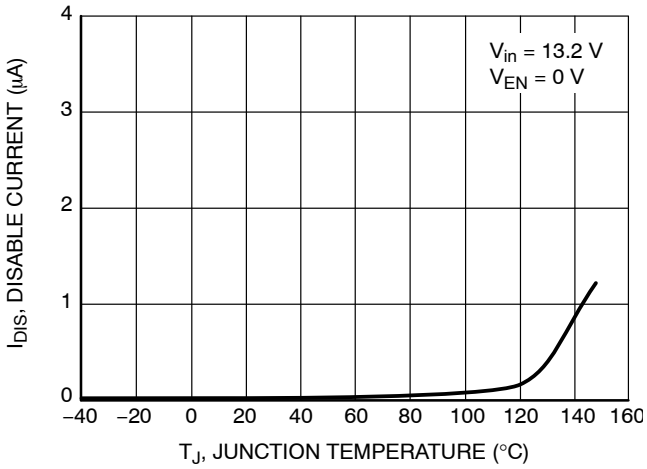


Figure 19. Disable Current vs Temperature

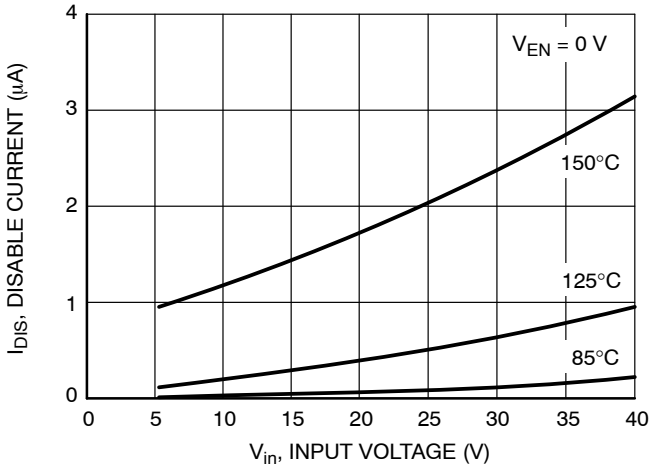


Figure 20. Disable Current vs. Input Voltage

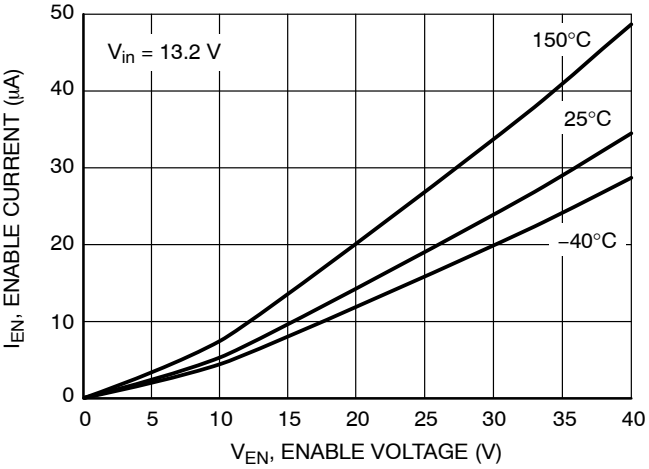


Figure 21. Enable Current vs. Enable Voltage

TYPICAL CHARACTERISTICS

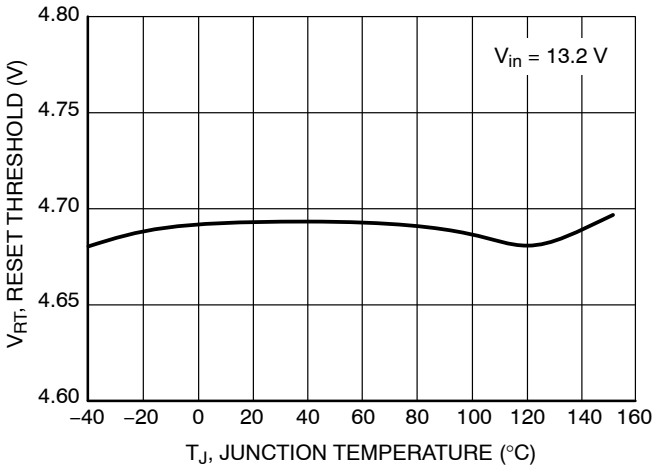


Figure 22. Reset Threshold vs Temperature (5 V option)

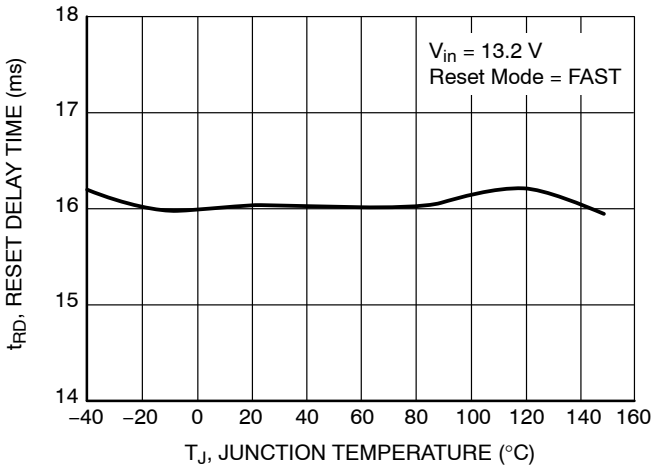


Figure 23. Reset Delay Time vs Temperature

TYPICAL CHARACTERISTICS

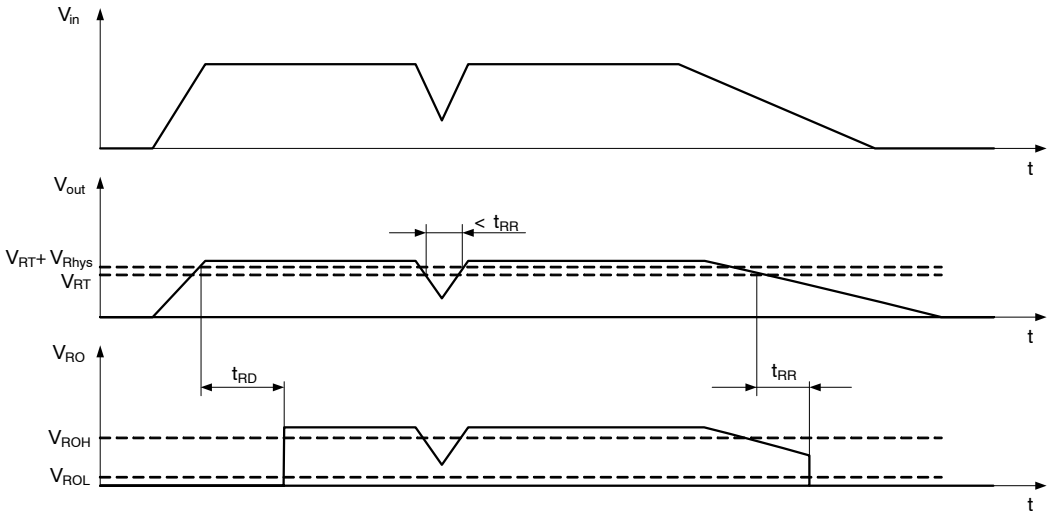
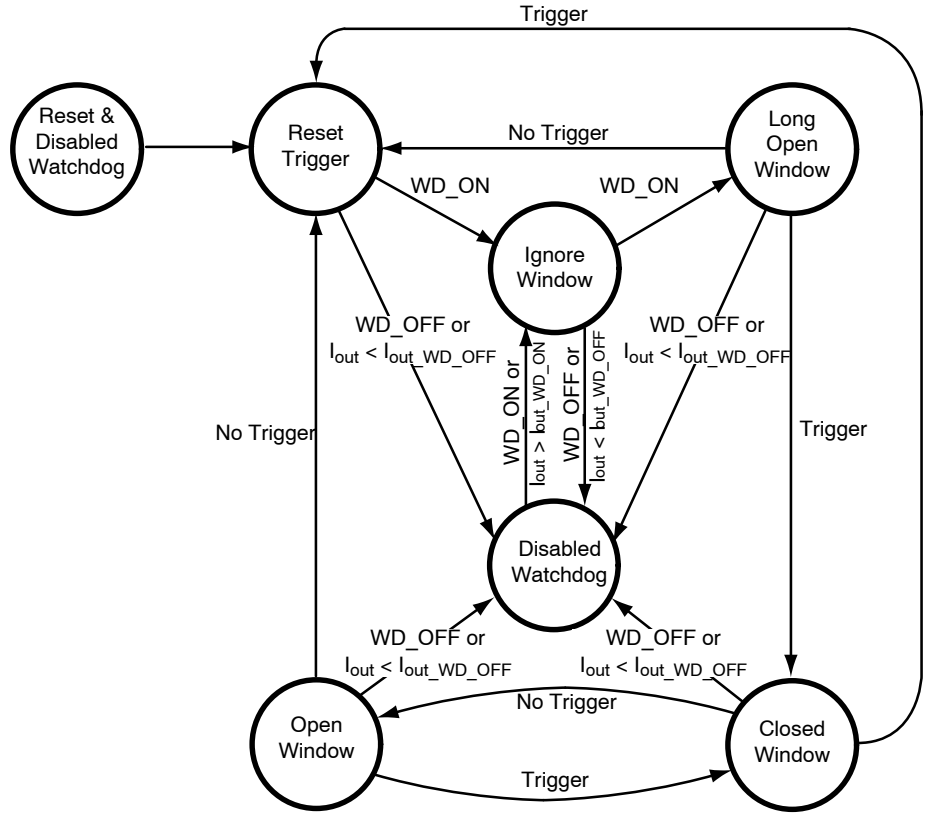


Figure 24. Reset Function and Timing Diagram



WM1	L	L	H	H
WM2	L	H	L	H
Window Watchdog Mode	FAST	SLOW	FAST	OFF
Reset Mode	FAST	SLOW	SLOW	SLOW

Figure 25. Window Watchdog State Diagram, Watchdog and Reset Modes

TYPICAL CHARACTERISTICS

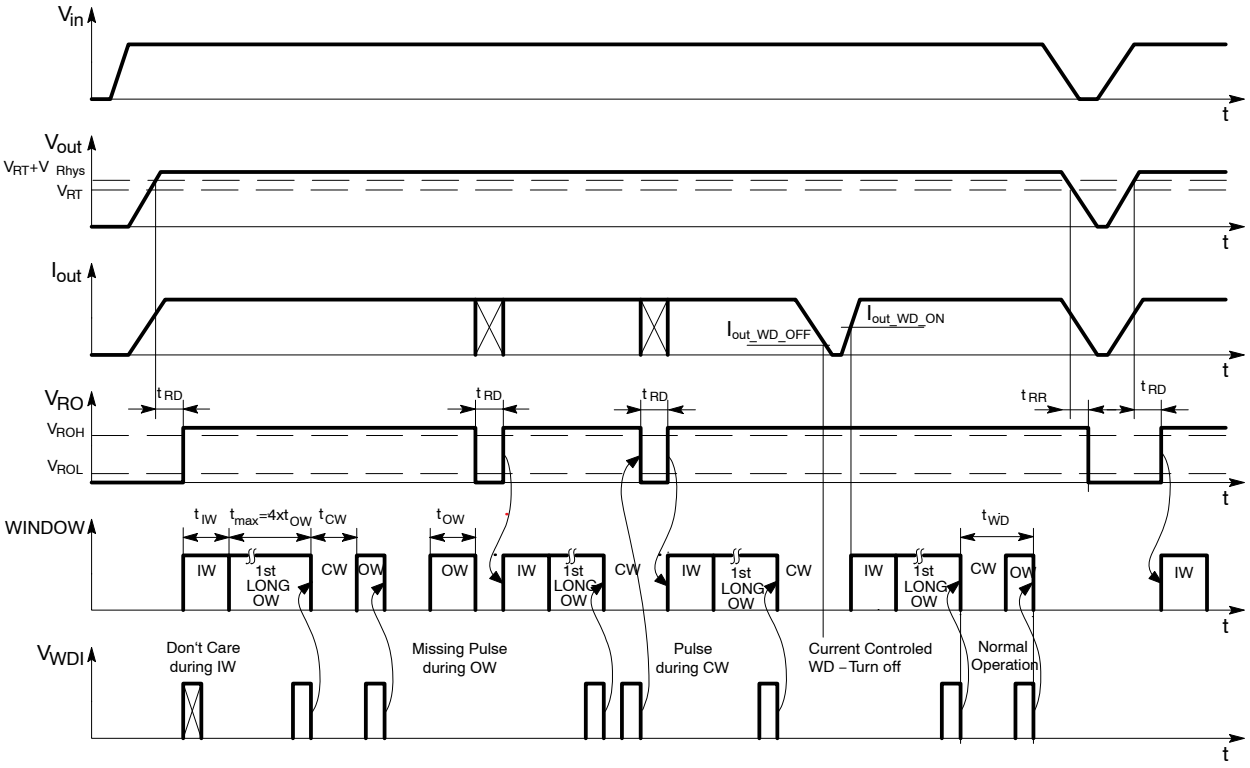
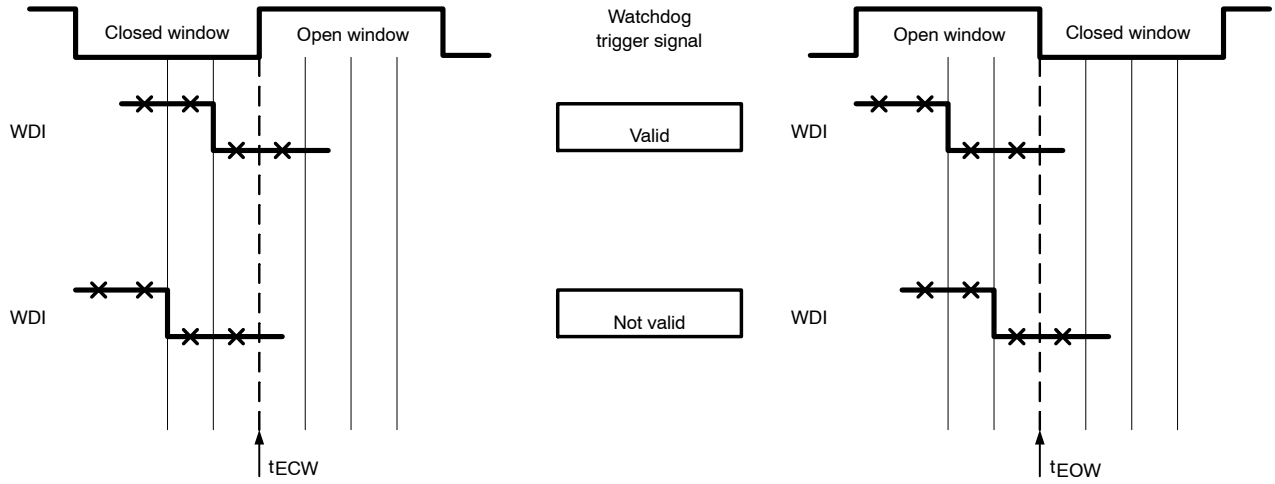


Figure 26. Window Watchdog Signal Diagram



✕ Watchdog decoder sample point

Figure 27. Valid WDI trigger signal

DEFINITIONS

General

All measurements are performed using short pulse low duty cycle techniques to maintain junction temperature as close as possible to ambient temperature.

Output Voltage

The output voltage parameter is defined for specific temperature, input voltage and output current values or specified over Line, Load and Temperature ranges.

Line Regulation

The change in output voltage for a change in input voltage measured for specific output current over operating ambient temperature range.

Load Regulation

The change in output voltage for a change in output current measured for specific input voltage over operating ambient temperature range.

Dropout Voltage

The input to output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. It is measured when the output drops 100 mV below its nominal value. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

Quiescent Currents

Quiescent Current (I_q) is the difference between the input current (measured through the LDO input pin) and the output current.

Current Limit and Short Circuit Current Limit

Current Limit is value of output current by which output voltage drops below 96% of its nominal value. Short Circuit Current Limit is output current value measured with output of the regulator shorted to ground.

PSRR

Power Supply Rejection Ratio is defined as ratio of output voltage and input voltage ripple. It is measured in decibels (dB).

Line Transient Response

Typical output voltage overshoot and undershoot response when the input voltage is excited with a given slope.

Load Transient Response

Typical output voltage overshoot and undershoot response when the output current is excited with a given slope between low−load and high−load conditions.

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 175°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

Maximum Package Power Dissipation

The power dissipation level is maximum allowed power dissipation for particular package or power dissipation at which the junction temperature reaches its maximum operating value, whichever is lower.

APPLICATIONS INFORMATION

The NCV8668 regulator is self−protected with internal thermal shutdown and internal current limit. Typical characteristics are shown in Figures 4 to 27.

Input Decoupling (C_{in})

A ceramic or tantalum 0.1 μF capacitor is recommended and should be connected close to the NCV8668 package. Higher capacitance and lower ESR will improve the overall line and load transient response.

If extremely fast input voltage transients are expected then appropriate input filter must be used in order to decrease rising and/or falling edges below 50 V/μs for proper operation. The filter can be composed of several capacitors in parallel.

Output Decoupling (C_{out})

The NCV8668 is a stable component and does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. Stability region of ESR versus Output Current is shown in Figure 13. The minimum output decoupling value is 2.2 μF and can be augmented to fulfill stringent load transient requirements. The regulator works with ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load regulation transient response.

Enable Operation

The Enable pin will turn the regulator on or off. The threshold limits are covered in the electrical characteristics table in this data sheet.

Reset Operation

A reset signal is provided on the Reset Output (RO) pin to provide feedback to the microprocessor of an out of regulation condition. The timing diagram of reset function is shown in Figure 24. This is in the form of a logic signal on RO. Output voltage conditions below the RESET threshold cause RO to go low. The RO integrity is maintained down to V_{OUT} = 1.0 V. The Reset Output (RO) circuitry includes

a pull−up resistor (30 kΩ) internally connected to the output (V_{OUT}). No external pull−up is necessary.

For voltage option 3.3 V RO is open drain output and external pull−up resistor is required.

Reset signal is also generated in case when input voltage decreases below its minimum operating limit (4.5 V). The Input Voltage Reset Threshold is typically 3.8 V. This applies only to voltage options with nominal value below minimum operating input voltage (3.3 V).

Window Watchdog Operation

The watchdog slow, fast or off state is set by pins WM1 and WM2 (see table in Figure 25). The timing values used in this description refer to typ. Values when WM1 and WM2 are connected to GND (fast watchdog and reset timing). The state diagram of the window watchdog (WWD) and the watchdog and reset mode selection table is shown in Figure 25. The WWD timing is shown in Figure 26. After power−on, the reset output signal at the RO pin (microprocessor reset) is kept LOW for the reset delay time t_{RD} (16 ms). RO signal transition from LOW to HIGH triggers the ignore window (IW) with duration of t_{IW} (32 ms). During this window the signal at the WDI pin is ignored. When IW ends a long open window with maximum duration of (128 ms, $t_{max} = 4xt_{OW}$) is started. When a valid trigger signal is detected during long open window, a closed window (CW) with duration of t_{CW} (32 ms) is initialized immediately. WDI signal transition from HIGH to LOW is taken as a trigger. As valid trigger two HIGH samples followed by two LOW samples (with sampling time t_{sam} = 0.5 ms) have to be present before end of the long window. Valid WDI trigger signal is shown in Figure 27. When CW ends a standard open window (OW) with maximum duration of t_{OW} (32 ms) is initiated immediately. The OW ends immediately when valid trigger appears at WDI input. For normal operation the microprocessor timing of WDI pulses must be stable and correspond to t_{WD}. A reset signal is generated (RO goes LOW) if there is no valid trigger (missing pulse at WDI pin) during OW or if a pre−trigger occurs during the CW (unexpected pulse at WDI pin).

Thermal Considerations

As power in the NCV8668 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCV8668 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the NCV8668 can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \qquad \text{(eq. 1)}$$

Since T_J is not recommended to exceed 150°C, then the NCV8668 soldered on 645 mm^2, 1 oz copper area, FR4 can dissipate up to 1.3 W for SOIC−14 package when the ambient temperature (T_A) is 25°C. See Figure 28 for $R_{\theta JA}$ versus PCB area. The power dissipated by the NCV8668 can be calculated from the following equations:

$$P_D = V_{in}\left(I_q @ I_{out}\right) + I_{out}\left(V_{in} - V_{out}\right) \qquad \text{(eq. 2)}$$

or

$$V_{in(MAX)} = \frac{P_{D(MAX)} + \left(V_{out} \times I_{out}\right)}{I_{out} + I_q} \qquad \text{(eq. 3)}$$

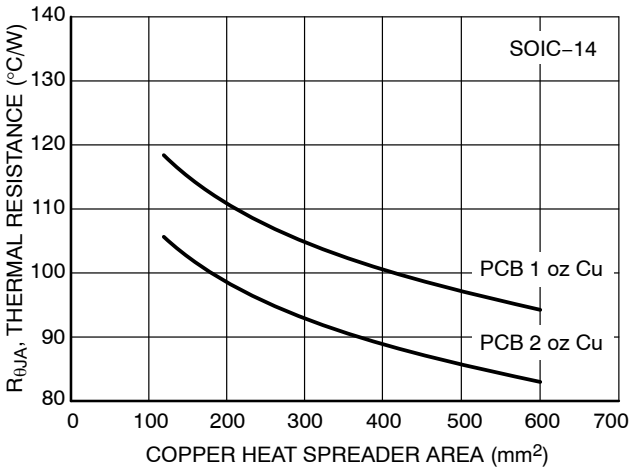


Figure 28. Thermal Resistance vs PCB Copper Area

Hints

V_{in} and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCV8668, and make traces as short as possible.

ORDERING INFORMATION

Device	V_{out}	t_{RD} Fast/ Slow	IW/OW/CW Time Fast/ Slow	1st LOW Time Fast/ Slow	V_{RT}	Output Current WW ON/ OFF	Marking	Package	Shipping†
NCV8668ABD250R2G	5.0 V	16 / 32 ms	32 / 64 ms	128 / 256 ms	93%	Yes	V8668AB50G	SOIC−14 (Pb−Free)	2500 / Tape & Reel
NCV8668ABD150R2G	5.0 V	16 / 32 ms	32 / 64 ms	128 / 256 ms	93%	Yes	668AB5	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCV8668ABPD50R2G	5.0 V	16 / 32 ms	32 / 64 ms	128 / 256 ms	93%	Yes	668AB5	SOIC−8 EPAD (Pb−Free)	2500 / Tape & Reel
NCV8668ABPD33R2G	3.3 V	16 / 32 ms	32 / 64 ms	128 / 256 ms	93%	Yes	668AB3	SOIC−8 EPAD (Pb−Free)	2500 / Tape & Reel
NCV8668ABD133R2G	3.3 V	16 / 32 ms	32 / 64 ms	128 / 256 ms	93%	Yes	668AB3	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

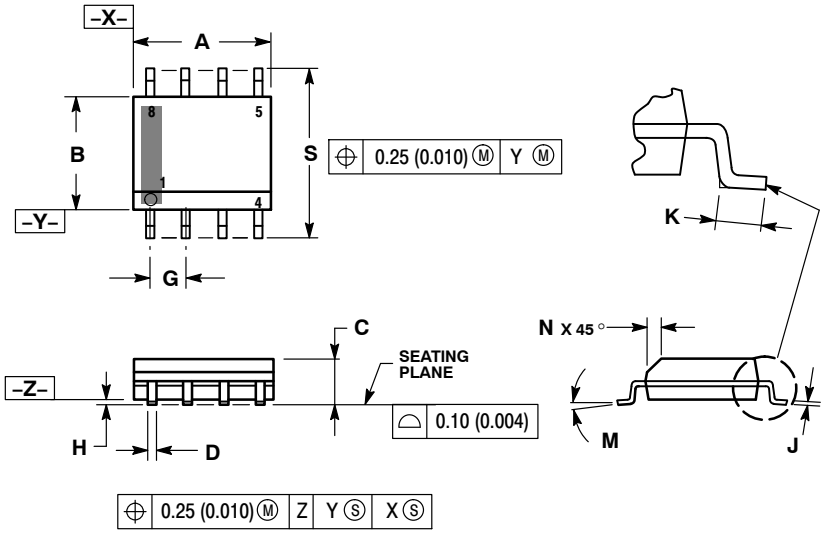
NOTE: Contact factory for other package, output voltage, timing and reset threshold options

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

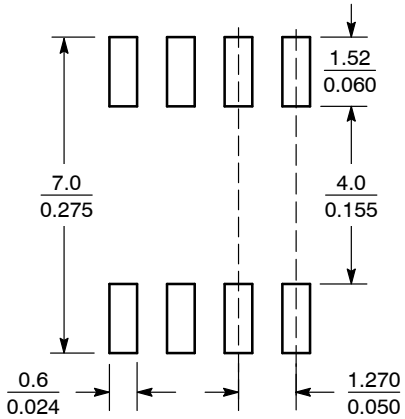
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

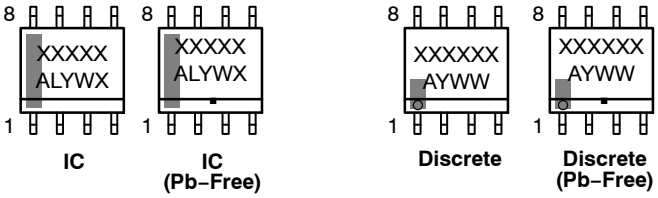
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOIC−8 NB**	**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

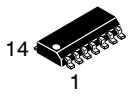
STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 2 OF 2**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



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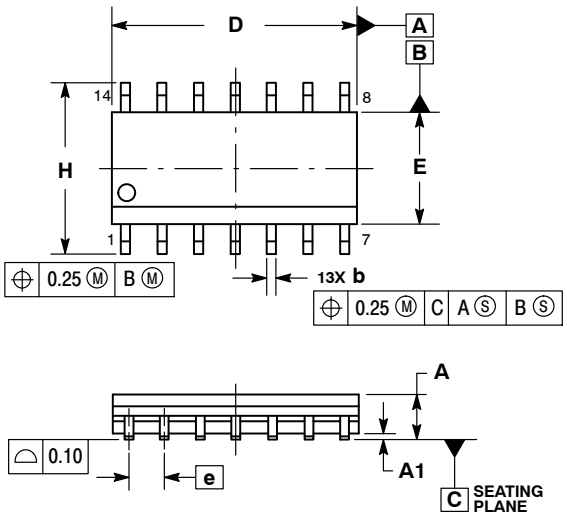
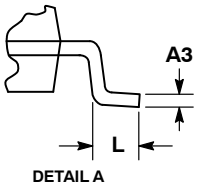
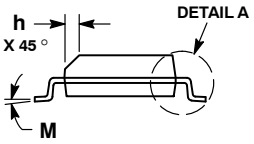
SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



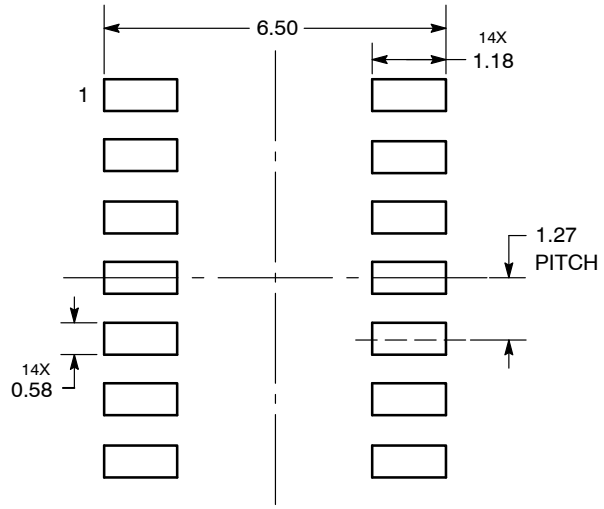




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

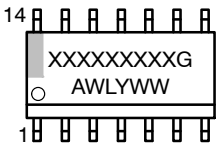
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−14 NB**		**PAGE 1 OF 2**

SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

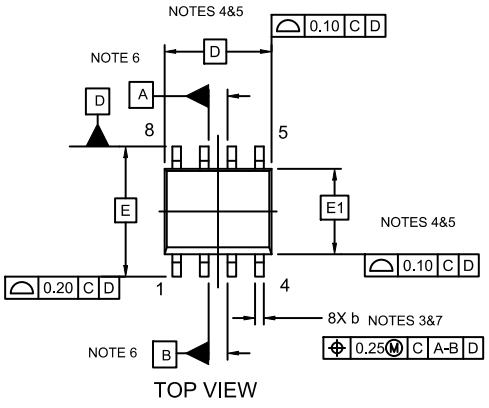
SCALE 1:1

SOIC−8 EP
CASE 751AC
ISSUE E

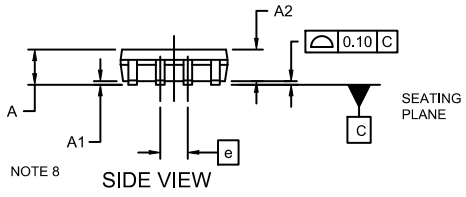
DATE 05 OCT 2022

NOTES:

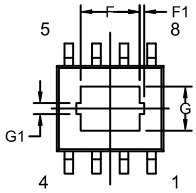
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.004 IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
6. DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



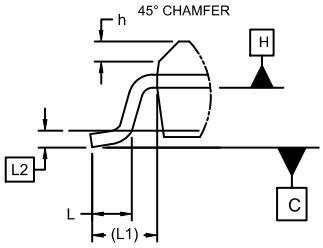
TOP VIEW



SIDE VIEW

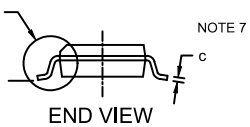


BOTTOM VIEW

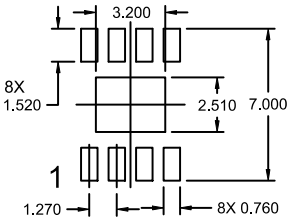


DETAIL A

DETAIL A



END VIEW

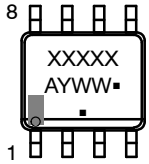


RECOMMENDED
MOUNTING FOOTPRINT*

DIM	MILLIMETERS		
	MIN.	NOM..	MAX.
A	1.35	1.55	1.75
A1	---	0.05	0.10
A2	1.35	1.50	1.65
b	0.31	0.41	0.51
c	0.17	0.21	0.23
D	4.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
F	2.24	2.72	3.20
F1		0.20 REF	
G	1.55	2.03	2.51
G1		0.46 REF	
h	0.25	0.38	0.50
L	0.40	0.84	1.27
L1	1.04 REF		
L2	0.25 REF		
Ø	0°	4°	8°

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D."

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present and may be in either location. Some products may not follow the Generic Marking.

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