



**THE DATASHEET OF  
NTHL110N65S3F**



# NTHL110N65S3F

## MOSFET – Power, N-Channel, SUPERFET III, FRFET

650 V, 30 A, 110 mΩ

### Description

SUPERFET III MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III MOSFET is very suitable for the various power system for miniaturization and higher efficiency.

SUPERFET III FRFET MOSFET's optimized reverse recovery performance of body diode can remove additional component and improve system reliability.

### Features

- 700 V @  $T_J = 150^\circ\text{C}$
- Typ.  $R_{DS(on)} = 98\text{ m}\Omega$
- Ultra Low Gate Charge (Typ.  $Q_g = 58\text{ nC}$ )
- Low Effective Output Capacitance (Typ.  $C_{oss(eff.)} = 553\text{ pF}$ )
- 100% Avalanche Tested
- This Device is Pb-Free and is RoHS Compliant

### Applications

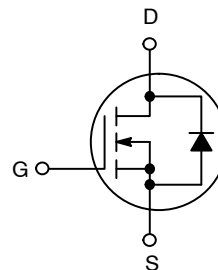
- Telecom / Server Power Supplies
- Industrial Power Supplies
- EV Charger
- UPS / Solar



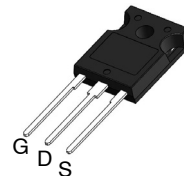
ON Semiconductor®

[www.onsemi.com](http://www.onsemi.com)

$V_{DSS}$	$R_{DS(on)}\text{ MAX}$	$I_D\text{ MAX}$
650 V	110 mΩ @ 10 V	30 A



N-Channel MOSFET



TO-247-3LD  
CASE 340CH

### MARKING DIAGRAM



\$Y = ON Semiconductor Logo  
&Z = Assembly Plant Code  
&3 = Numeric Date Code  
&K = Lot Code  
NTHL110N65S3F = Specific Device Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# NTHL110N65S3F

## ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ , Unless otherwise specified)

Symbol	Parameter	NTHL110N65S3F	Unit
$V_{DSS}$	Drain to Source Voltage	650	V
$V_{GSS}$	Gate to Source Voltage	DC	$\pm 30$
		AC ( $f > 1\text{ Hz}$ )	$\pm 30$
$I_D$	Drain Current	Continuous ( $T_C = 25^\circ\text{C}$ )	30
		Continuous ( $T_C = 100^\circ\text{C}$ )	19.5
$I_{DM}$	Drain Current	Pulsed (Note 1)	69
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	380	mJ
$I_{AR}$	Avalanche Current (Note 2)	4.4	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	2.4	mJ
dv/dt	MOSFET dv/dt	100	V/ns
	Peak Diode Recovery dv/dt (Note 3)	50	
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	240
		Derate Above $25^\circ\text{C}$	1.92
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 s	300	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.

2.  $I_{AS} = 4.4\text{ A}$ ,  $R_G = 25\ \Omega$ , starting  $T_J = 25^\circ\text{C}$ .

3.  $I_{SD} \leq 15\text{ A}$ ,  $di/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq 400\text{ V}$ , starting  $T_J = 25^\circ\text{C}$ .

## THERMAL CHARACTERISTICS

Symbol	Parameter	NTHL110N65S3F	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.52	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

## PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
NTHL110N65S3F	NTHL110N65S3F	TO-247	Tube	N/A	N/A	30 Units

# NTHL110N65S3F

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA, T <sub>J</sub> = 25°C	650	–	–	V
		V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA, T <sub>J</sub> = 150°C	700	–	–	V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 10 mA, Referenced to 25°C	–	0.64	–	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 650 V, V <sub>GS</sub> = 0 V	–	–	10	μA
		V <sub>DS</sub> = 520 V, T <sub>C</sub> = 125°C	–	97	–	
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0 V	–	–	±100	nA

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 0.74 mA	3.0	–	5.0	V
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A	–	98	110	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 15 A	–	17	–	S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 400 V, V <sub>GS</sub> = 0 V, f = 1 MHz	–	2560	–	pF
C <sub>oss</sub>	Output Capacitance		–	50	–	pF
C <sub>oss(eff.)</sub>	Effective Output Capacitance	V <sub>DS</sub> = 0 V to 400 V, V <sub>GS</sub> = 0 V	–	553	–	pF
C <sub>oss(er.)</sub>	Energy Related Output Capacitance	V <sub>DS</sub> = 0 V to 400 V, V <sub>GS</sub> = 0 V	–	83	–	pF
Q <sub>g(tot)</sub>	Total Gate Charge at 10 V	V <sub>DS</sub> = 400 V, I <sub>D</sub> = 15 A, V <sub>GS</sub> = 10 V (Note 4)	–	58	–	nC
Q <sub>gs</sub>	Gate to Source Gate Charge		–	19	–	nC
Q <sub>gd</sub>	Gate to Drain “Miller” Charge		–	23	–	nC
ESR	Equivalent Series Resistance	f = 1 MHz	–	2	–	Ω

### SWITCHING CHARACTERISTICS

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 400 V, I <sub>D</sub> = 15 A, V <sub>GS</sub> = 10 V, R <sub>g</sub> = 4.7 Ω (Note 4)	–	29	–	ns
t <sub>r</sub>	Turn-On Rise Time		–	32	–	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		–	61	–	ns
t <sub>f</sub>	Turn-Off Fall Time		–	16	–	ns

### SOURCE-DRAIN DIODE CHARACTERISTICS

I <sub>S</sub>	Maximum Continuous Source to Drain Diode Forward Current	–	–	30	A	
I <sub>SM</sub>	Maximum Pulsed Source to Drain Diode Forward Current	–	–	69	A	
V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 15 A	–	–	1.3	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 15 A, dI <sub>F</sub> /dt = 100 A/μs	–	94	–	ns
Q <sub>rr</sub>	Reverse Recovery Charge		–	343	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

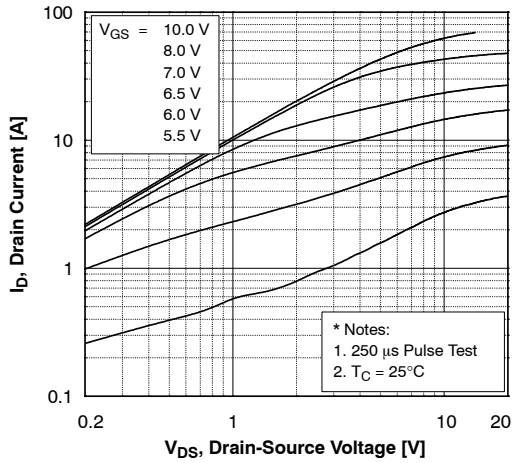


Figure 1. On-Region Characteristics

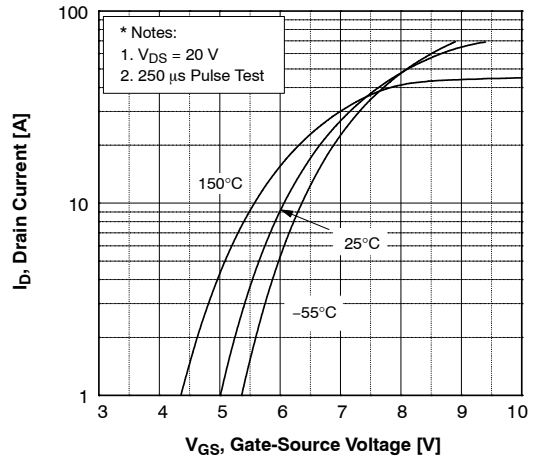


Figure 2. Transfer Characteristics

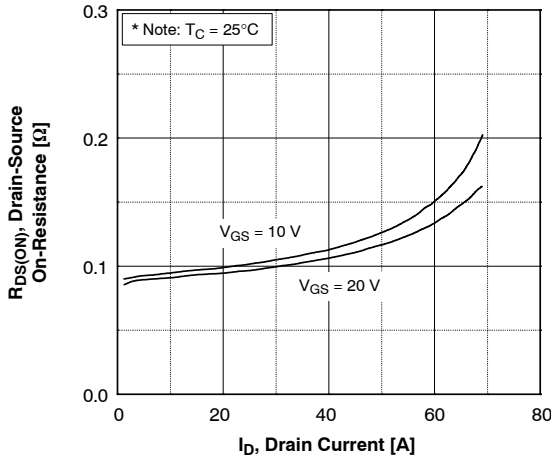


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

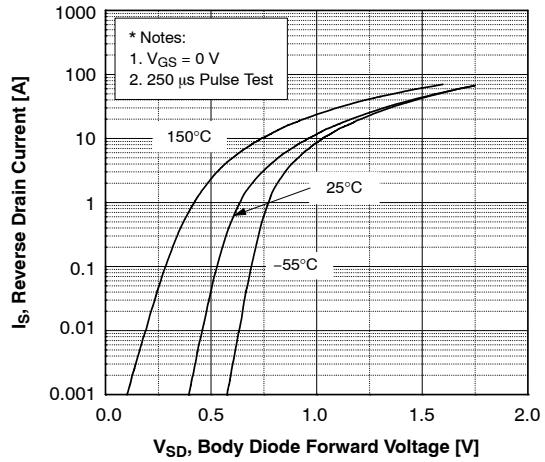


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

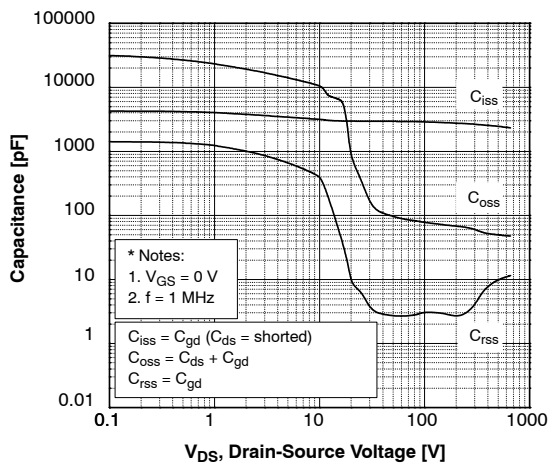


Figure 5. Capacitance Characteristics

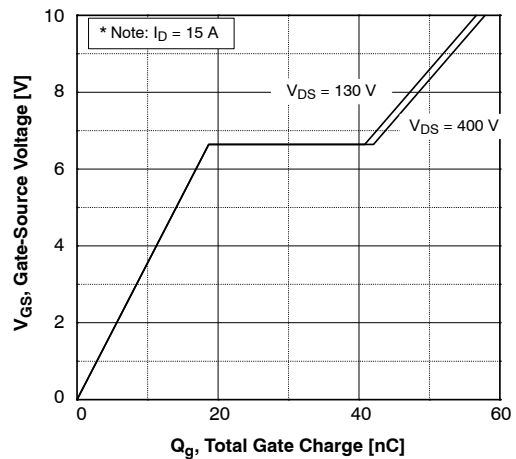


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

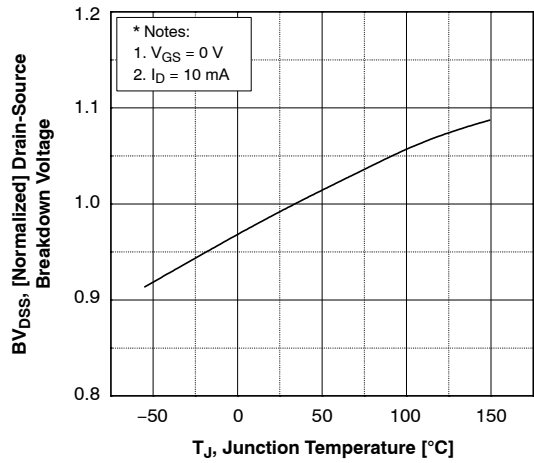


Figure 7. Breakdown Voltage Variation vs. Temperature

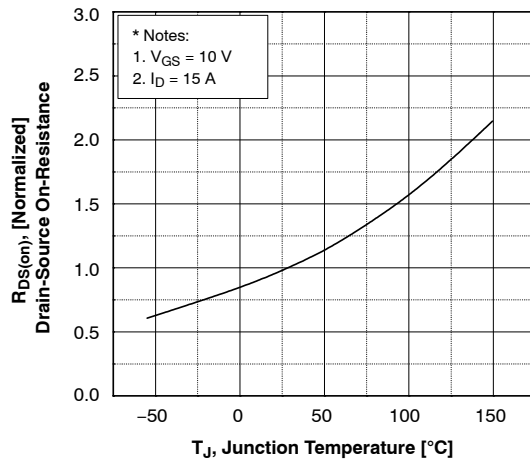


Figure 8. On-Resistance Variant vs. Temperature

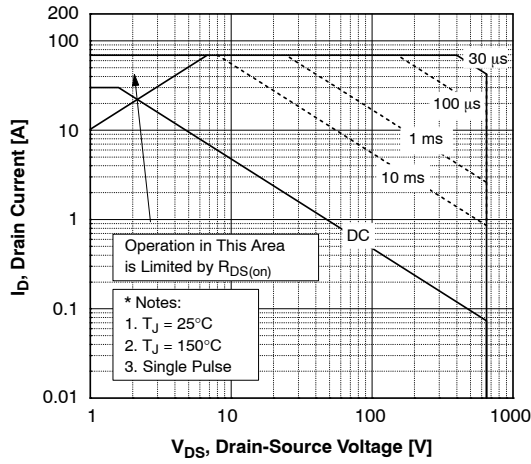


Figure 9. Maximum Safe Operation Area

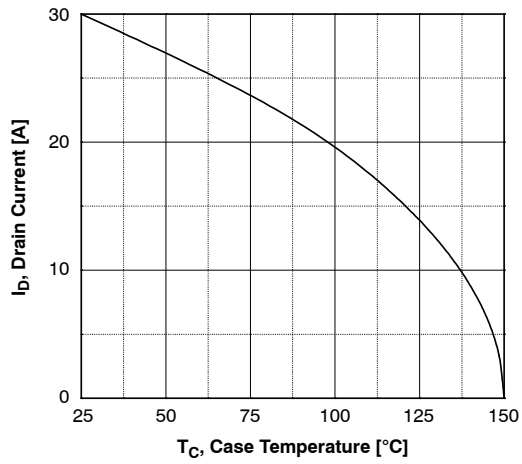


Figure 10. Maximum Drain Current vs. Case Temperature

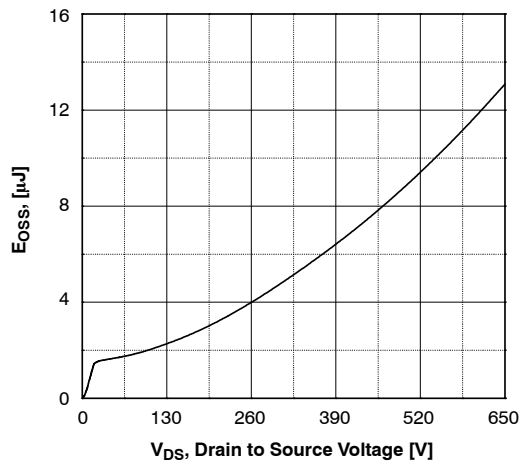


Figure 11.  $E_{OSS}$  vs. Drain to Source Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

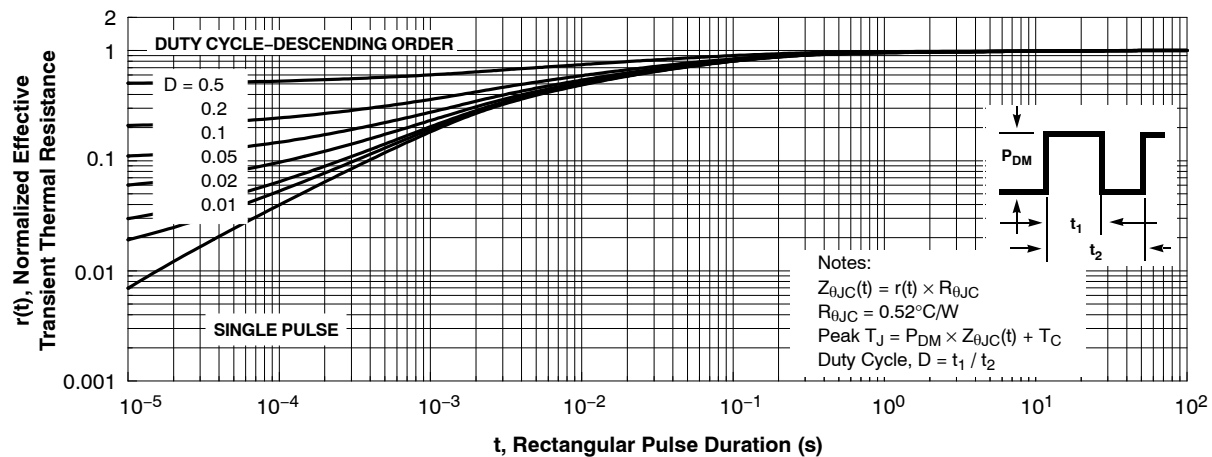


Figure 12. Transient Thermal Response Curve

# NTHL110N65S3F

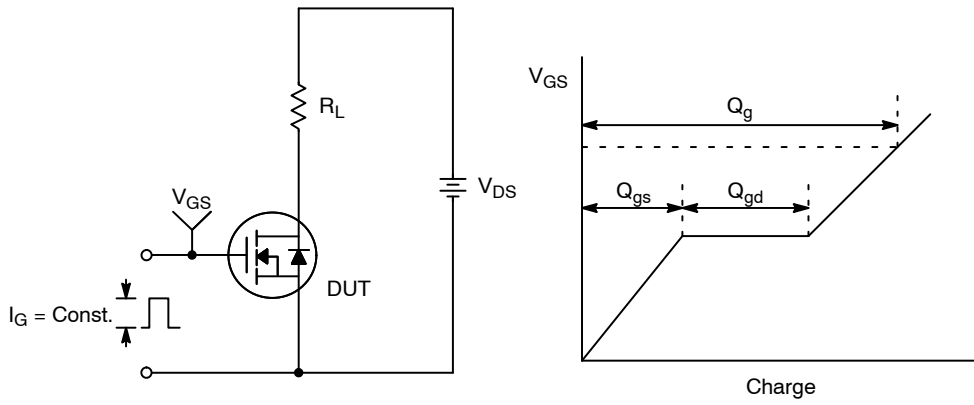


Figure 13. Gate Charge Test Circuit & Waveform

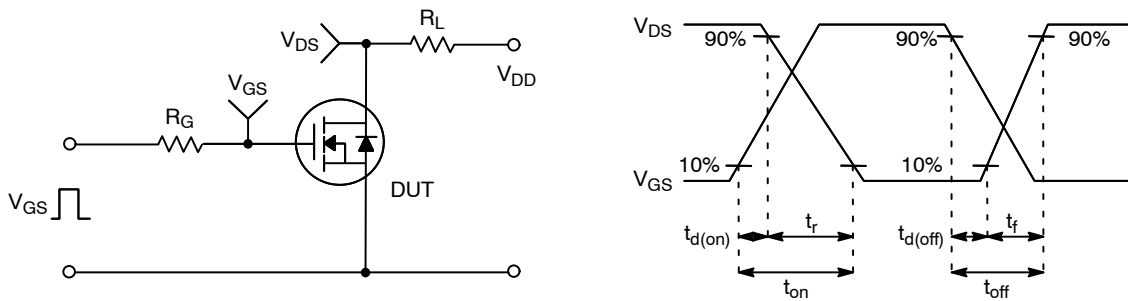


Figure 14. Resistive Switching Test Circuit & Waveforms

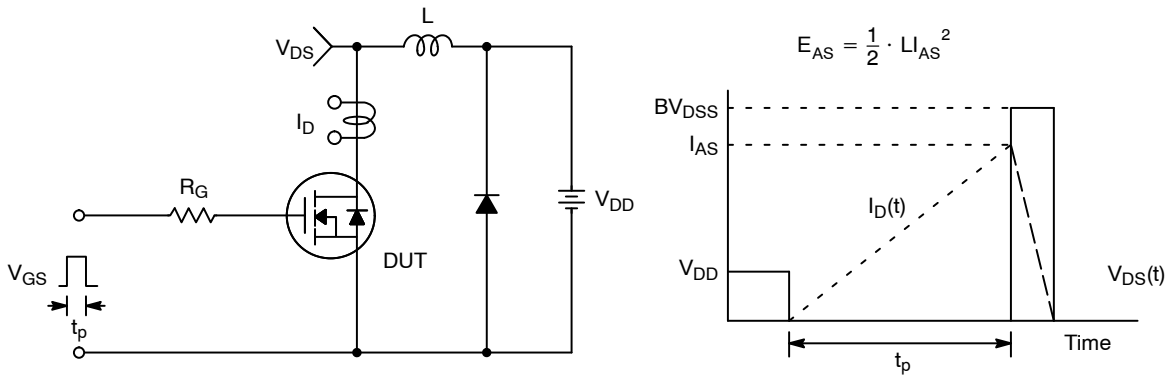
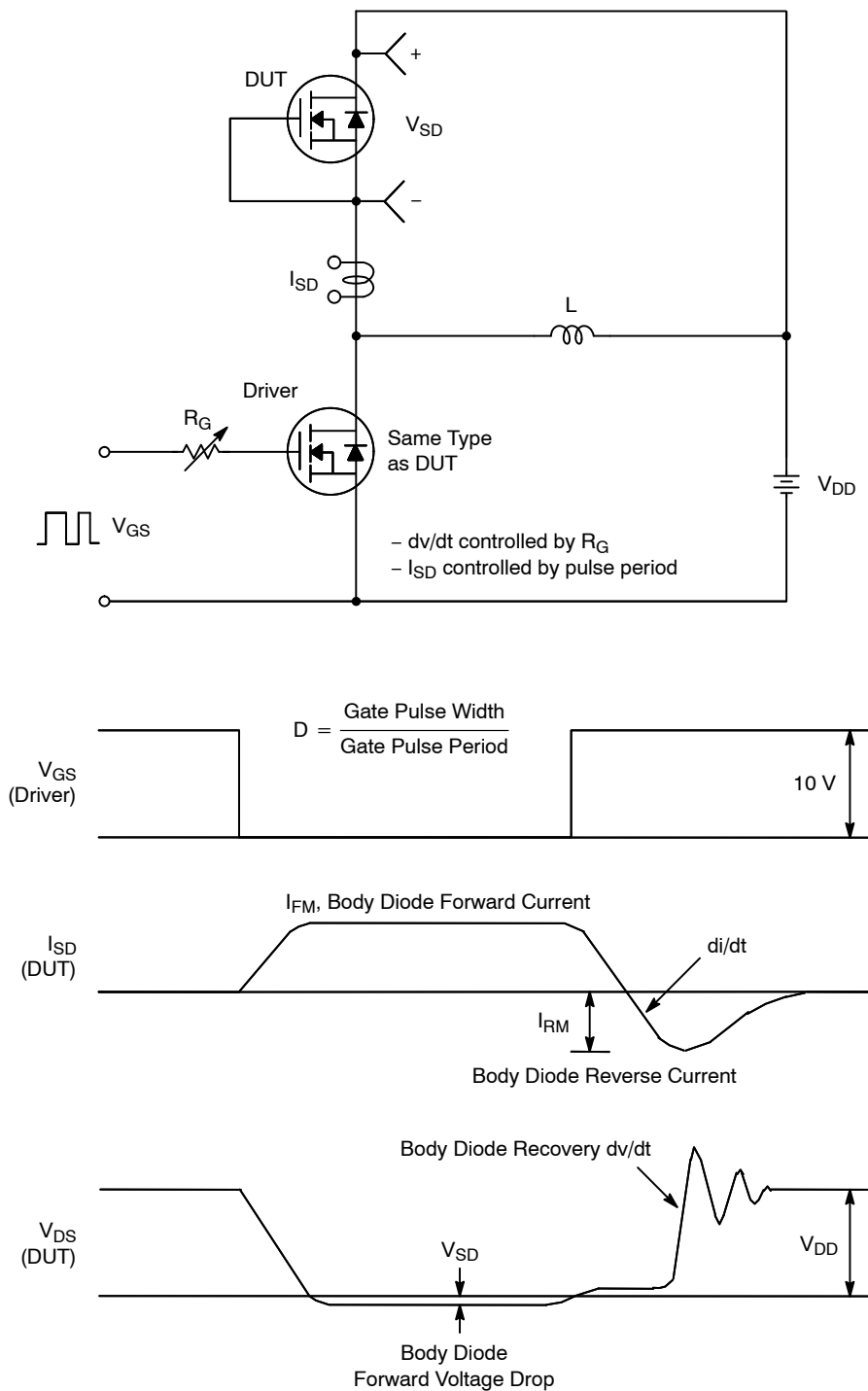


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

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**Figure 16. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms**

# MECHANICAL CASE OUTLINE

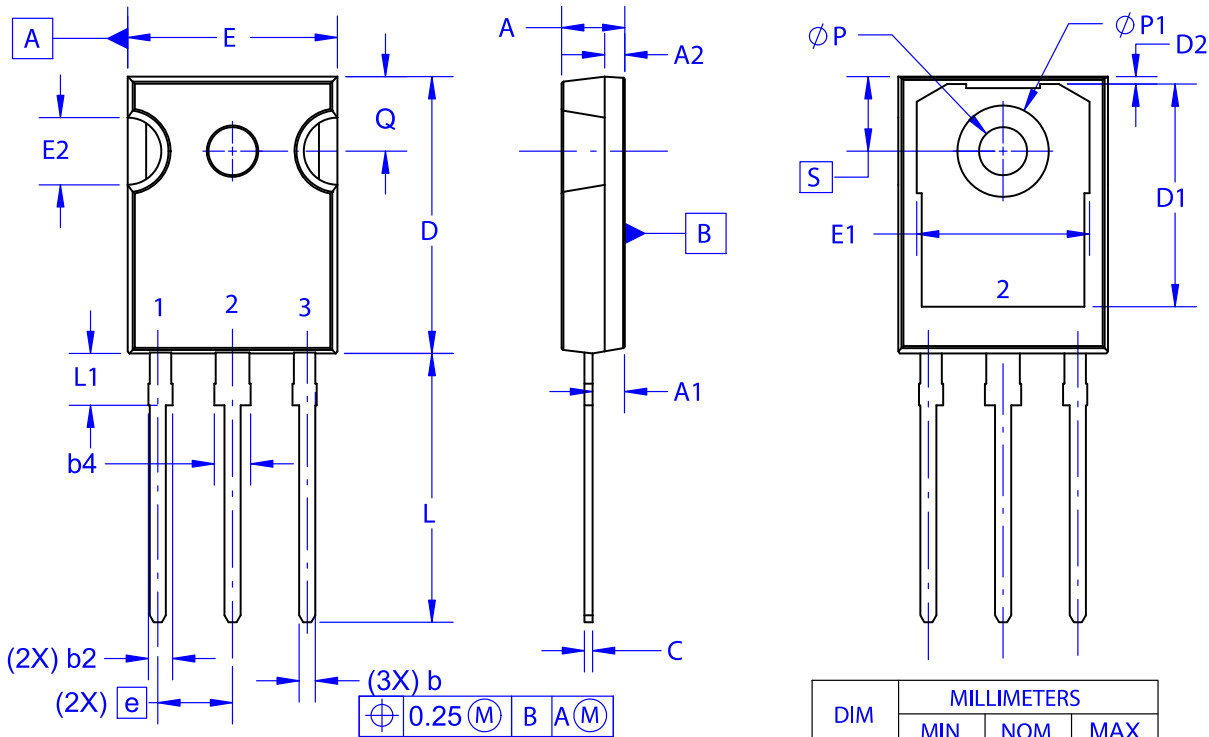
## PACKAGE DIMENSIONS

ON Semiconductor®



TO-247-3LD  
CASE 340CH  
ISSUE A

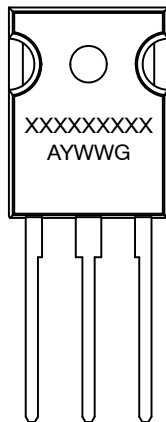
DATE 09 OCT 2019



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
- D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
- E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

### GENERIC MARKING DIAGRAM\*



XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.29	2.475	2.66
A2	1.40	1.50	1.60
D	20.32	20.57	20.82
E	15.37	15.62	15.87
E2	4.96	5.08	5.20
e	~	5.56	~
L	19.75	20.00	20.25
L1	3.69	3.81	3.93
∅P	3.51	3.58	3.65
Q	5.34	5.46	5.58
S	5.34	5.46	5.58
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D1	13.08	~	~
D2	0.51	0.93	1.35
E1	12.81	~	~
∅P1	6.61	6.73	6.85

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-  Alternative Solution
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