

MMBTA63LT1G, MMBTA64LT1G, SMMBTA64LT1G

Darlington Transistors

PNP Silicon

Features

- S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	–30	Vdc
Collector–Base Voltage	V_{CBO}	–30	Vdc
Emitter–Base Voltage	V_{EBO}	–10	Vdc
Collector Current – Continuous	I_C	–500	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR–5 Board, (Note 1) $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	225 1.8	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	556	$^\circ\text{C}/\text{W}$
Total Device Dissipation Alumina Substrate, (Note 2) $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	300 2.4	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	417	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature	T_J, T_{stg}	–55 to +150	$^\circ\text{C}$

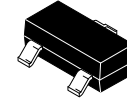
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. FR–5 = 1.0 x 0.75 x 0.062 in.
2. Alumina = 0.4 x 0.3 x 0.024 in. 99.5% alumina.

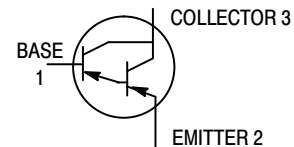


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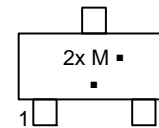
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SOT–23 (TO–236)
CASE 318
STYLE 6



MARKING DIAGRAM



2x = Device Code
 x = U for MMBTA63LT1G
 x = V for MMBTA64LT1G
 SMMBTA64LT1G
 M = Date Code*
 ■ = Pb-Free Package

(Note: Microdot may be in either location)
 *Date Code orientation and/or overbar may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
MMBTA63LT1G	SOT–23 (Pb–Free)	3,000 / Tape & Reel
MMBTA64LT1G	SOT–23 (Pb–Free)	3,000 / Tape & Reel
SMMBTA64LT1G	SOT–23 (Pb–Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MMBTA63LT1G, MMBTA64LT1G, SMMBTA64LT1G

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Breakdown Voltage ($I_C = -100\ \mu\text{Adc}$)	$V_{(BR)CEO}$	-30	-	Vdc
Collector Cutoff Current ($V_{CB} = -30\ \text{Vdc}$)	I_{CBO}	-	-100	nAdc
Emitter Cutoff Current ($V_{EB} = -10\ \text{Vdc}$)	I_{EBO}	-	-100	nAdc
ON CHARACTERISTICS				
DC Current Gain (Note 3) ($I_C = -10\ \text{mAdc}$, $V_{CE} = -5.0\ \text{Vdc}$) MMBTA63 ($I_C = -10\ \text{mAdc}$, $V_{CE} = -5.0\ \text{Vdc}$) MMBTA64, SMMBTA64 ($I_C = -100\ \text{mAdc}$, $V_{CE} = -5.0\ \text{Vdc}$) MMBTA63 ($I_C = -100\ \text{mAdc}$, $V_{CE} = -5.0\ \text{Vdc}$) MMBTA64, SMMBTA64	h_{FE}			-
		5,000	-	
		10,000	-	
		10,000	-	
		20,000	-	
Collector–Emitter Saturation Voltage ($I_C = -100\ \text{mAdc}$, $I_B = -0.1\ \text{mAdc}$)	$V_{CE(sat)}$	-	-1.5	Vdc
Base – Emitter On Voltage ($I_C = -100\ \text{mAdc}$, $V_{CE} = -5.0\ \text{Vdc}$)	$V_{BE(on)}$	-	-2.0	Vdc
SMALL– SIGNAL CHARACTERISTICS				
Current–Gain – Bandwidth Product ($I_C = -10\ \text{mAdc}$, $V_{CE} = -5.0\ \text{Vdc}$, $f = 100\ \text{MHz}$)	f_T	125	-	MHz

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

MMBTA63LT1G, MMBTA64LT1G, SMMBTA64LT1G

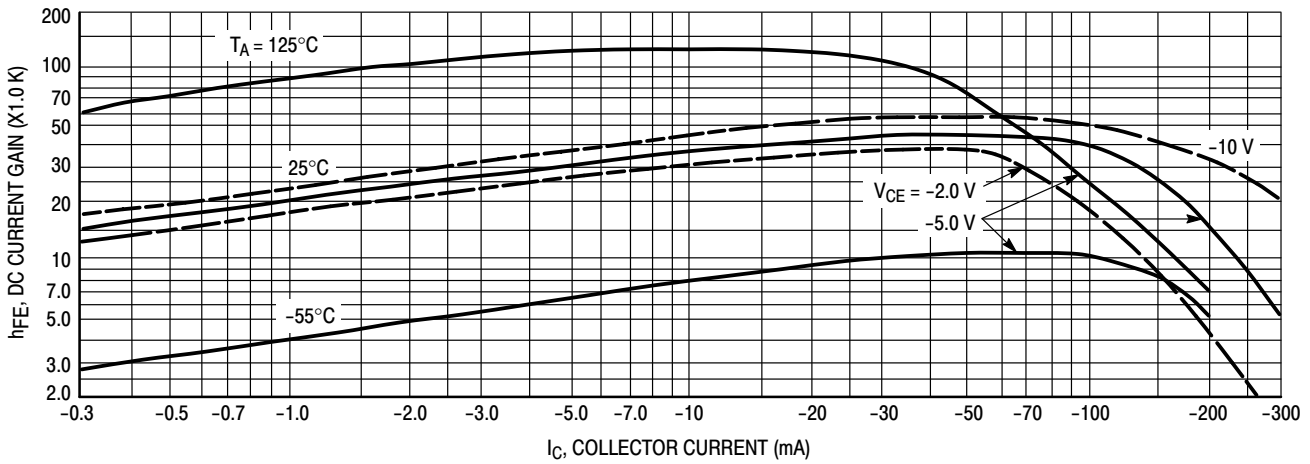


Figure 1. DC Current Gain

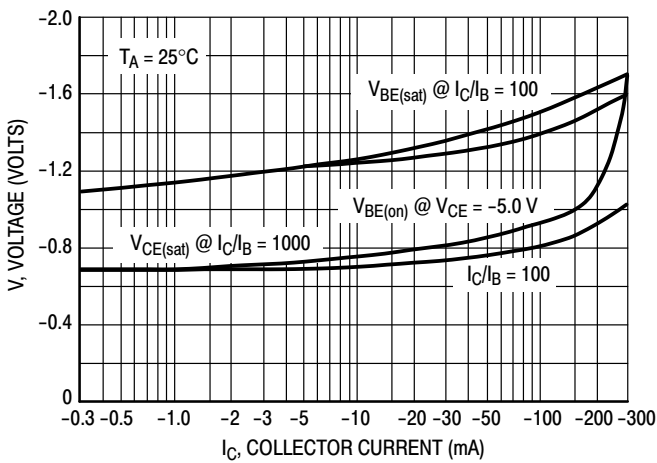


Figure 3. "On" Voltage

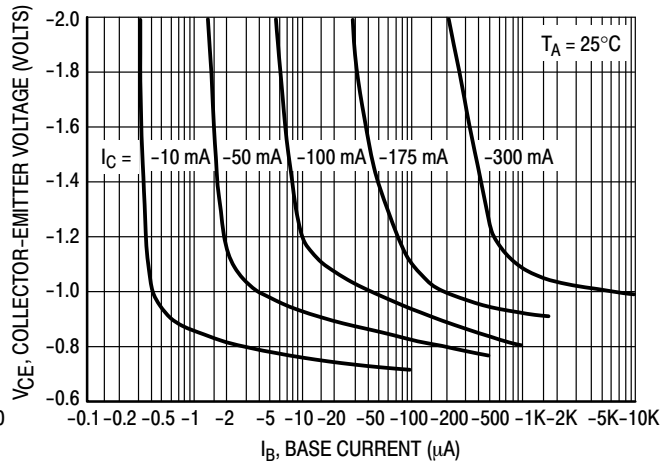


Figure 2. Collector Saturation Region

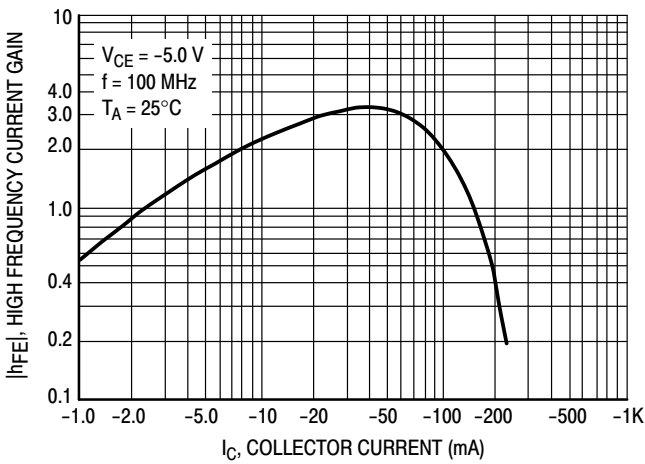


Figure 4. High Frequency Current Gain

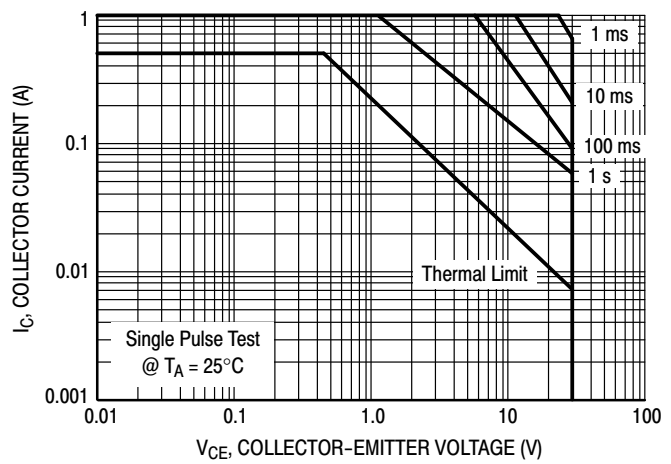


Figure 5. Safe Operating Area

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SOT-23 (TO-236)
CASE 318
ISSUE AT

DATE 01 MAR 2023

SCALE 4:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H _E	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

GENERIC MARKING DIAGRAM*



- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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**MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS**



**SOT-23 (TO-236)
CASE 318
ISSUE AT**

DATE 01 MAR 2023

- | | | | | | |
|---|---|---|---|---|---|
| STYLE 1 THRU 5:
CANCELLED | STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR | STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR | STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE | | |
| STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE | STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE | STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE-ANODE | STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE | STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE | STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE |
| STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE | STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE | STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE | STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE | STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE-ANODE | STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE |
| STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN | STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT | STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE | STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE | STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE | STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION |
| STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE | STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE | | | | |

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