



# THE DATASHEET OF SN74LVC32ANS



## SNx4LVC32A Quadruple 2-Input Positive-OR Gates

### 1 Features

- Operate from 1.65V to 3.6V
- Specified from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , and  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Inputs accept voltages to 5.5V
- Max  $t_{pd}$  of 3.8ns at 3.3V
- Typical  $V_{OLP}$  (output ground bounce)  $< 0.8\text{V}$  at  $V_{CC} = 3.3\text{V}$ ,  $T_A = 25^{\circ}\text{C}$
- Typical  $V_{OHV}$  (output  $V_{OH}$  undershoot)  $> 2\text{V}$  at  $V_{CC} = 3.3\text{V}$ ,  $T_A = 25^{\circ}\text{C}$
- Latch-up performance exceeds 250mA per JESD 17
- On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.
- ESD protection exceeds JESD 22
  - 2000V human-body model
  - 1000V charged-device model

### 2 Applications

- AV Receivers
- Audio Docks: Portable
- Blu-ray Players and Home Theater
- MP3 Players or Recorders
- Personal Digital Assistant (PDA)
- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Solid State Drives (SSDs): Client and Enterprise
- TVs: LCD, Digital, and High-Definition (HDTV)
- Tablets: Enterprise
- Video Analytics: Server
- Wireless Headsets, Keyboards, and Mice

### 3 Description

The SN54LVC32A quadruple 2-input positive-OR gate is designed for 2.7V to 3.6V  $V_{CC}$  operation, and the SN74LVC32A quadruple 2-input positive-OR gate is designed for 1.65V to 3.6V  $V_{CC}$  operation.

The SNx4LVC32A devices perform the Boolean function  $Y = A + B$  or  $Y = \overline{A} \cdot \overline{B}$  in positive logic.

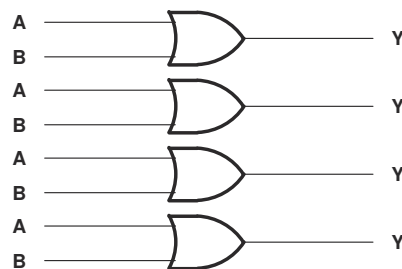
Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V system environment.

#### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>	BODY SIZE <sup>(3)</sup>
SNx4LVC32A	BQA (WQFN, 14)	3mm × 2.5mm	3mm × 2.5mm
	D (SOIC, 14)	8.65mm × 6mm	8.65mm × 3.91mm
	DB (SSOP, 14)	6.2mm × 7.8mm	6.20mm × 5.30mm
	NS (SOP, 14)	10.2mm × 7.8mm	10.30mm × 5.30mm
	PW (TSSOP, 14)	5mm × 6.4mm	5.00mm × 4.40mm
	RGY (VQFN, 14)	3.50mm × 3.50mm	3.50mm × 3.50mm
	FK (LCCC, 20)	8.9mm × 8.9mm	8.9mm × 8.9mm
	J (CDIP, 14)	19.55mm × 7.9mm	19.55 mm × 6.7mm
	W (CFP, 14)	9.21mm × 9mm	9.21mm × 6.28mm

- For more information, see [Section 11](#).
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.

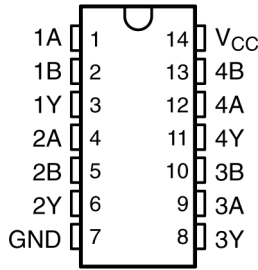
#### Simplified Schematic



## Table of Contents

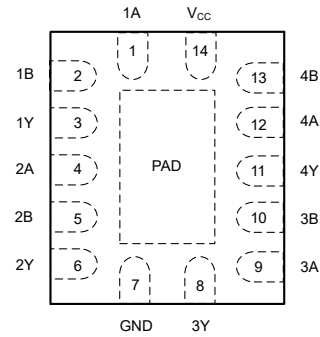
<b>1 Features</b> .....	1	5.11 Typical Characteristics.....	7
<b>2 Applications</b> .....	1	<b>6 Parameter Measurement Information</b> .....	8
<b>3 Description</b> .....	1	<b>7 Detailed Description</b> .....	9
<b>4 Pin Configuration and Functions</b> .....	3	7.1 Overview.....	9
<b>5 Specifications</b> .....	4	7.2 Functional Block Diagram.....	9
5.1 Absolute Maximum Ratings.....	4	7.3 Feature Description.....	9
5.2 ESD Ratings.....	4	7.4 Device Functional Modes.....	9
5.3 Recommended Operating Conditions, SN54LVC32A.....	5	<b>8 Device and Documentation Support</b> .....	12
5.4 Recommended Operating Conditions, SN74LVC32A.....	5	8.1 Documentation Support.....	12
5.5 Thermal Information.....	6	8.2 Receiving Notification of Documentation Updates....	12
5.6 Electrical Characteristics, SN54LVC32A.....	6	8.3 Support Resources.....	12
5.7 Electrical Characteristics, SN74LVC32A.....	6	8.4 Trademarks.....	12
5.8 Switching Characteristics, SN54LVC32A.....	7	8.5 Electrostatic Discharge Caution.....	12
5.9 Switching Characteristics, SN74LVC32A.....	7	8.6 Glossary.....	12
5.10 Operating Characteristics.....	7	<b>9 Revision History</b> .....	12
		<b>10 Mechanical, Packaging, and Orderable Information</b> .....	13

### 4 Pin Configuration and Functions

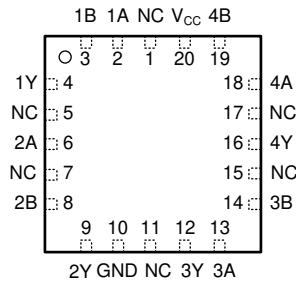


**Figure 4-1. SN54LVC32A J or W Package, 14-Pin (Top View)**

**SN74LVC32A D, DB, NS, or PW Package, 14-Pin CDIP, CFP, SOIC, SSOP, SOP, TSSOP (Top View)**



**Figure 4-2. SN74LVC32A RGY or BQA Package, 14-Pin VQFN or WQFN (Top View)**



**Figure 4-3. SN54LVC32A FK Package, 20-Pin LCCC (Top View)**

**Table 4-1. Pin Functions**

NAME	PIN				TYPE	DESCRIPTION
	SN74LVC32A		SN54LVC32A			
	D, DB, NS, PW	BQA, RGY	J, W	FK		
1A	1	1	1	2	I	Gate 1 input
1B	2	2	2	3	I	Gate 1 input
1Y	3	3	3	4	O	Gate 1 output
2A	4	4	4	6	I	Gate 2 input
2B	5	5	5	8	I	Gate 2 input
2Y	6	6	6	9	O	Gate 2 output
GND	7	7	7	10	—	Ground Pin
3Y	8	8	8	12	O	Gate 3 output
3A	9	9	9	13	I	Gate 3 input
3B	10	10	10	14	I	Gate 3 input
4Y	11	11	11	16	O	Gate 4 output
4A	12	12	12	18	I	Gate 4 input
4B	13	13	13	19	I	Gate 4 input
V <sub>CC</sub>	14	14	14	20	—	Power Pin
NC	—	—	—	1, 5, 7, 11, 15, 17	—	No Connection

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		-0.5	6.5	V
V <sub>I</sub>	Input voltage <sup>(2)</sup>		-0.5	6.5	V
V <sub>O</sub>	Output voltage <sup>(2) (3)</sup>		-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA
I <sub>O</sub>	Continuous output current			±50	mA
	Continuous current through V <sub>CC</sub> or GND			±100	mA
P <sub>tot</sub>	Power dissipation	T <sub>A</sub> = -40°C to +125°C <sup>(4) (5)</sup>		500	mW
T <sub>J</sub>	Junction temperature			150	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V<sub>CC</sub> is provided in the *Recommended Operating Conditions* tables.
- (4) For the D package: above 70°C, the value of P<sub>tot</sub> derates linearly with 8 mW/K.
- (5) For the DB, DGV, NS, and PW packages: above 60°C, the value of P<sub>tot</sub> derates linearly with 5.5 mW/K.

### 5.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions, SN54LVC32A

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		SN54LVC32A		UNIT
		–55 to +125°C		
		MIN	MAX	
V <sub>CC</sub>	Supply voltage	Operating		V
		Data retention only		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2.7 V to 3.6 V		V
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2.7 V to 3.6 V		V
V <sub>I</sub>	Input voltage	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2.7 V		mA
		V <sub>CC</sub> = 3 V		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2.7 V		mA
		V <sub>CC</sub> = 3 V		
Δt/Δv	Input transition rise and fall rate	7		ns/V

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

### 5.4 Recommended Operating Conditions, SN74LVC32A

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		SN74LVC32A						UNIT
		T <sub>A</sub> = 25°C		–40 to +85°C		–40 to +125°C		
		MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	Operating		1.65		3.6		V
		Data retention only		1.5		1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V		0.65 × V <sub>CC</sub>		0.65 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V		1.7		1.7		
		V <sub>CC</sub> = 2.7 V to 3.6 V		2		2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>		0.35 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V		0.7		0.7		
		V <sub>CC</sub> = 2.7 V to 3.6 V		0.8		0.8		
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V		–4		–4		mA
		V <sub>CC</sub> = 2.3 V		–8		–8		
		V <sub>CC</sub> = 2.7 V		–12		–12		
		V <sub>CC</sub> = 3 V		–24		–24		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V		4		4		mA
		V <sub>CC</sub> = 2.3 V		8		8		
		V <sub>CC</sub> = 2.7 V		12		12		
		V <sub>CC</sub> = 3 V		24		24		
Δt/Δv	Input transition rise and fall rate	7		7		7		ns/V

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

## 5.5 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SN74LVC32A						UNIT
	BQA (WQFN)	D (SOIC)	DB (SSOP)	NS (SOP)	PW (TSSOP)	RGY (VQFN)	
	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
R <sub>θJA</sub> Junction-to-ambient thermal resistance	102.3	86	140.4	123.8	150.8	92.1	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.6 Electrical Characteristics, SN54LVC32A

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN54LVC32A		UNIT
			–55 to +125°C		
			MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –100 μA	2.7 V to 3.6 V	V <sub>CC</sub> – 0.2		V
	I <sub>OH</sub> = –12 mA	2.7 V	2.2		
	I <sub>OH</sub> = –24 mA	3 V	2.4		
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	2.7 V to 3.6 V	0.2		V
	I <sub>OL</sub> = 12 mA	2.7 V	0.4		
	I <sub>OL</sub> = 24 mA	3 V	0.55		
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	3.6 V	±5		μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V	10		μA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V	500		μA

## 5.7 Electrical Characteristics, SN74LVC32A

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN74LVC32A						UNIT	
			T <sub>A</sub> = 25°C			–40 to +85°C		–40 to +125°C		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
V <sub>OH</sub>	I <sub>OH</sub> = –100 μA	1.65 V to 3.6 V	V <sub>CC</sub> – 0.2			V <sub>CC</sub> – 0.2		V <sub>CC</sub> – 0.3		V
	I <sub>OH</sub> = –4 mA	1.65 V	1.29			1.2		1.05		
	I <sub>OH</sub> = –8 mA	2.3 V	1.9			1.7		1.55		
	I <sub>OH</sub> = –12 mA	2.7 V	2.2			2.2		2.05		
	I <sub>OH</sub> = –24 mA	3 V	2.4			2.4		2.25		
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V	0.1			0.2		0.3		V
	I <sub>OL</sub> = 4 mA	1.65 V	0.24			0.45		0.6		
	I <sub>OL</sub> = 8 mA	2.3 V	0.3			0.7		0.85		
	I <sub>OL</sub> = 12 mA	2.7 V	0.4			0.4		0.6		
	I <sub>OL</sub> = 24 mA	3 V	0.55			0.55		0.8		
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	3.6 V	±1			±5		±20		μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V	1			10		40		μA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V	500			500		5000		μA

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN74LVC32A						UNIT	
			T <sub>A</sub> = 25°C			–40 to +85°C		–40 to +125°C		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	5						pF	

### 5.8 Switching Characteristics, SN54LVC32A

over operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	SN54LVC32A		UNIT
				–55 to +125°C		
				MIN	MAX	
t <sub>pd</sub>	A or B	Y	2.7V	4.4		ns
			3.3V ± 0.3V	1	3.8	

### 5.9 Switching Characteristics, SN74LVC32A

over operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	SN74LVC32A						UNIT	
				T <sub>A</sub> = 25°C			–40 to +85°C		–40 to +125°C		
				MIN	TYP	MAX	MIN	MAX	MIN		MAX
t <sub>pd</sub>	A or B	Y	1.8V ± 0.15V	1	4.2	8.2	1	8.7	1	10.2	ns
			2.5V ± 0.2V	1	2.6	4.9	1	5.4	1	6.9	
			2.7V	1	3	4.2	1	4.4	1	5.5	
			3.3V ± 0.3V	1	2.5	3.6	1	3.8	1	5	
t <sub>sk(o)</sub>			3.3V ± 0.3V				1		1.5	ns	

### 5.10 Operating Characteristics

T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance per gate	f = 10 MHz	1.8V	7.5	pF
			2.5V	10.6	
			3.3V	12.5	

### 5.11 Typical Characteristics

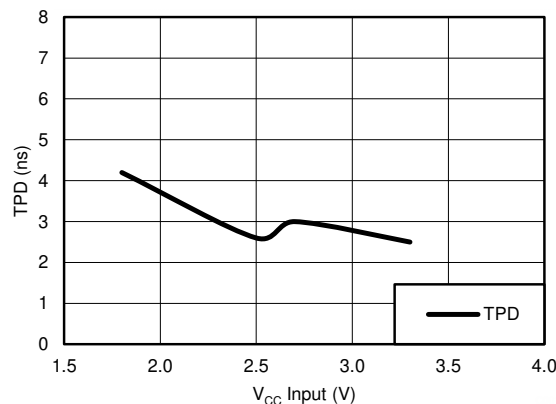
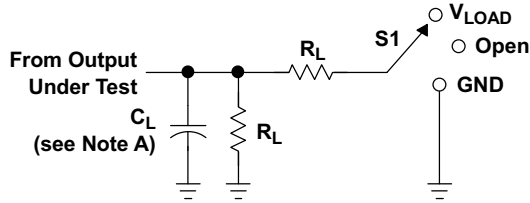


Figure 5-1. TPD vs V<sub>CC</sub> (T<sub>A</sub> = 25°C)

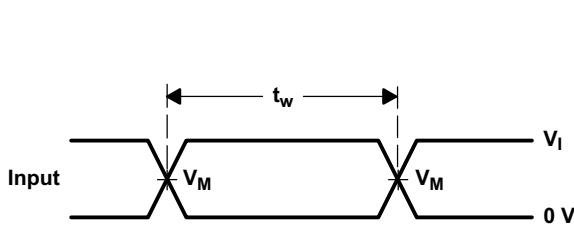
## 6 Parameter Measurement Information



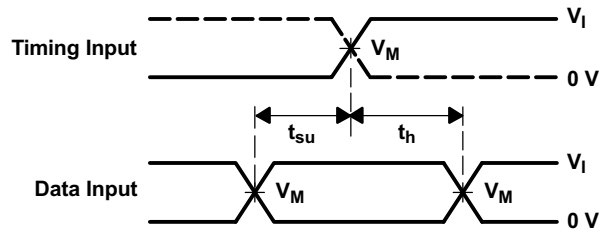
LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

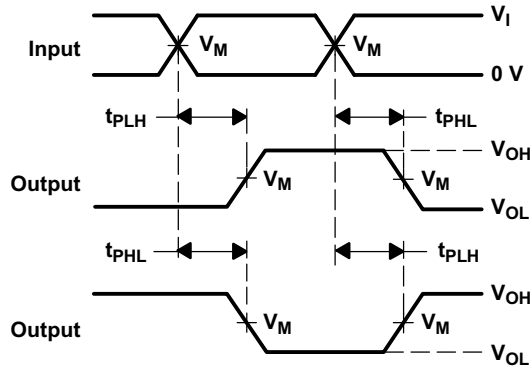
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



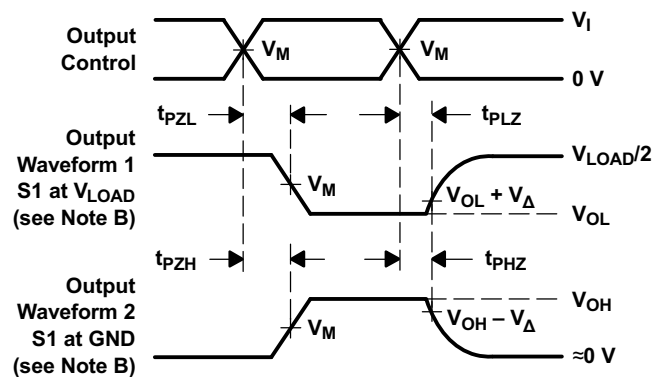
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

## 7 Detailed Description

### 7.1 Overview

The SN54LVC32A quadruple 2-input positive-OR gate is designed for 2-V to 3.6-V  $V_{CC}$  operation, and the SN74LVC32A quadruple 2-input positive-OR gate is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SNx4LVC32A devices perform the Boolean function  $Y = A + B$  or  $Y = \overline{\overline{A} \cdot \overline{B}}$  in positive logic.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as down-translators in a mixed 3.3-V/5-V system environment.

### 7.2 Functional Block Diagram



Logic Diagram, Each Gate (Positive Logic)

### 7.3 Feature Description

- Wide operating voltage range
  - Operates from 1.65 V to 3.6 V
- Allows up or down voltage translation
  - Inputs accept voltages to 5.5 V

### 7.4 Device Functional Modes

Table 7-1 lists the functional modes of SNx4LVC32A.

**Table 7-1. Function Table  
(Each Gate)**

INPUTS		OUTPUT Y
A	B	
H	X	H
X	H	H
L	L	L

## Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 1 Application Information

SN74LVC32A device is a high-drive, CMOS device that can be used for a multitude of buffer-type functions. It can produce 24 mA of drive current at 3 V. Therefore, this device is ideal for driving multiple inputs and for high-speed applications up to 100 MHz. The inputs and outputs are 5.5-V tolerant allowing the device to translate down to  $V_{CC}$ .

## 2 Typical Application

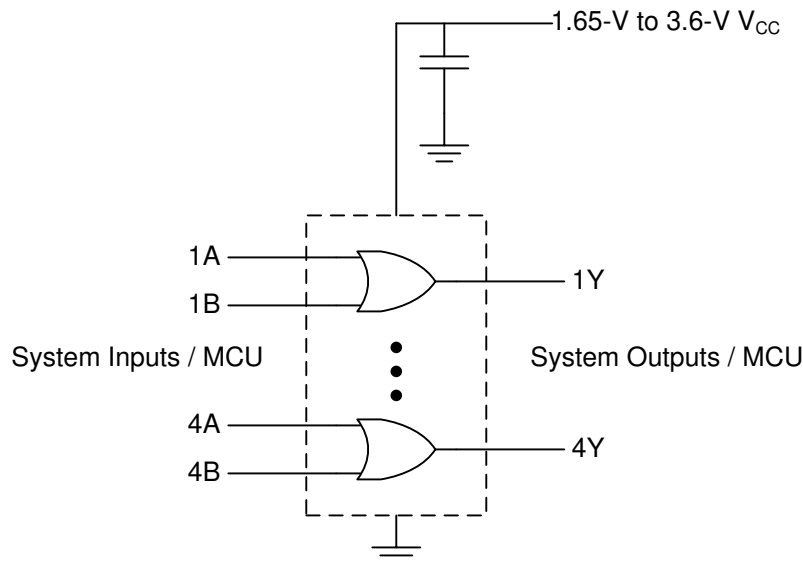


Figure 8-1. Typical OR Gate Application and Supply Voltage

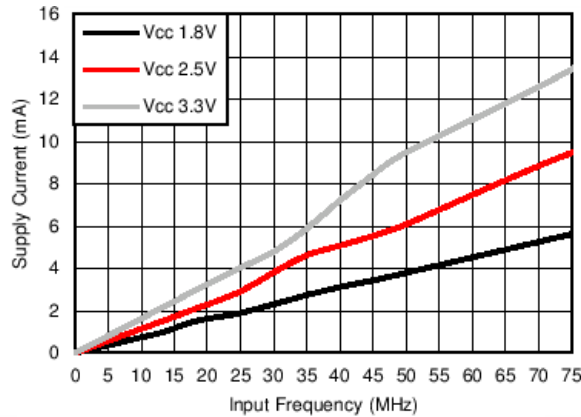
### 2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads; therefore, routing and load conditions should be considered to prevent ringing.

### 2.2 Detailed Design Procedure

- Recommended Input Conditions
  - Rise time and fall time specs: See  $(\Delta t/\Delta V)$  in the [Section 5.4](#) table.
  - Specified high and low levels: See  $(V_{IH}$  and  $V_{IL})$  in the [Section 5.4](#) table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid  $V_{CC}$ .
- Recommended Output Conditions
  - Load currents should not exceed 25 mA per output and 50 mA total for the part.
  - Outputs should not be pulled above 5.5 V.

### 2.3 Application Curve



**Figure 8-2. Supply Current vs Input Frequency**

### Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Section 5.4](#) table.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{F}$  is recommended; if there are multiple  $V_{CC}$  pins, then 0.01  $\mu\text{F}$  or 0.022  $\mu\text{F}$  is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu\text{F}$  and a 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

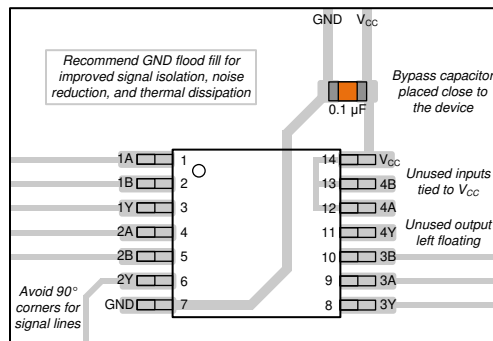
## 3 Layout

### 3.1 Layout Guidelines

When using multiple bit logic devices inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [Section 8.3.2](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver.

### 3.2 Layout Example



**Figure 8-3. Layout Diagram**

## 8 Device and Documentation Support

### 8.1 Documentation Support

#### 8.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 8-1. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54LVC32A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
SN74LVC32A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

#### 8.3.1 Community Resources

### 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments. All trademarks are the property of their respective owners.

### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision S (March 2024) to Revision T (May 2024)	Page
• Updated R0JA values: DB = 96 to 140.4, NS = 76 to 123.8, PW = 113 to 150.8, RGY = 47 to 92.1; Updated DB, NS, PW, and RGY packages for R0JC(top), R0JB, ΨJT, ΨJB, and R0JC(bot), all values in °C/W.....	6

Changes from Revision R (October 2016) to Revision S (March 2024)	Page
• Deleted machine model from <i>Features</i> section.....	1
• Added BQA package to <i>Device Information</i> table.....	1
• Updated structural layout of data sheet.....	1

---

- Added BQA package to *Pin Configuration and Functions* section..... 3
- Added BQA package to *Thermal Information* table .....6
- Updated *Layout Example* ..... 11

---

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9761801Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9761801Q2A SNJ54LVC32AFK	<a href="#">Samples</a>
5962-9761801QCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9761801QC A SNJ54LVC32AJ	<a href="#">Samples</a>
5962-9761801QDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9761801QD A SNJ54LVC32AW	<a href="#">Samples</a>
SN74LVC32ABQAR	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC32A	<a href="#">Samples</a>
SN74LVC32AD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC32A	<a href="#">Samples</a>
SN74LVC32ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC32A	<a href="#">Samples</a>
SN74LVC32ADBRG4	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC32A	<a href="#">Samples</a>
SN74LVC32ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC32A	<a href="#">Samples</a>
SN74LVC32ADRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC32A	<a href="#">Samples</a>
SN74LVC32ADT	ACTIVE	SOIC	D	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC32A	<a href="#">Samples</a>
SN74LVC32ANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC32A	<a href="#">Samples</a>
SN74LVC32APW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC32A	<a href="#">Samples</a>
SN74LVC32APWE4	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC32A	<a href="#">Samples</a>
SN74LVC32APWG4	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC32A	<a href="#">Samples</a>
SN74LVC32APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	LC32A	<a href="#">Samples</a>
SN74LVC32APWRE4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC32A	<a href="#">Samples</a>
SN74LVC32APWRG3	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LC32A	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC32APWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC32A	<a href="#">Samples</a>
SN74LVC32APWT	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC32A	<a href="#">Samples</a>
SN74LVC32ARGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC32A	<a href="#">Samples</a>
SNJ54LVC32AFK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9761801Q2A SNJ54LVC32AFK	<a href="#">Samples</a>
SNJ54LVC32AJ	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9761801QC A SNJ54LVC32AJ	<a href="#">Samples</a>
SNJ54LVC32AW	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9761801QD A SNJ54LVC32AW	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LVC32A, SN74LVC32A :**

- Catalog : [SN74LVC32A](#)
  
- Automotive : [SN74LVC32A-Q1](#), [SN74LVC32A-Q1](#)
  
- Enhanced Product : [SN74LVC32A-EP](#), [SN74LVC32A-EP](#)
  
- Military : [SN54LVC32A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
  
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
  
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
  
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

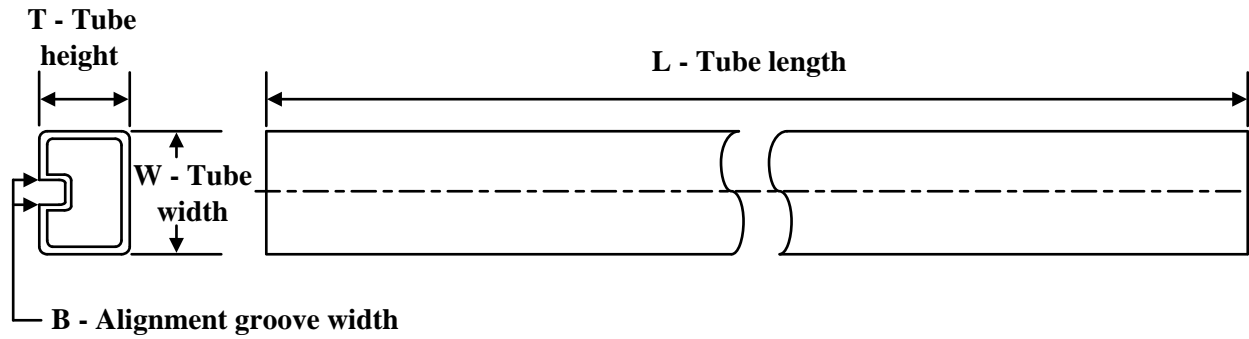

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC32ABQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74LVC32ADBDR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LVC32ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC32ADT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC32ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LVC32APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC32APWRG3	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC32APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC32APWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC32ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC32ABQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74LVC32ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LVC32ADR	SOIC	D	14	2500	333.2	345.9	28.6
SN74LVC32ADT	SOIC	D	14	250	210.0	185.0	35.0
SN74LVC32ANSR	SO	NS	14	2000	356.0	356.0	35.0
SN74LVC32APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LVC32APWRG3	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74LVC32APWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LVC32APWT	TSSOP	PW	14	250	356.0	356.0	35.0
SN74LVC32ARGYR	VQFN	RGY	14	3000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9761801Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9761801QDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74LVC32AD	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC32APW	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC32APWE4	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC32APWG4	PW	TSSOP	14	90	530	10.2	3600	3.5
SNJ54LVC32AFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LVC32AW	W	CFP	14	25	506.98	26.16	6220	NA

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - △ Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - Package complies to JEDEC MO-241 variation BA.

RGY (S-PVQFN-N14)

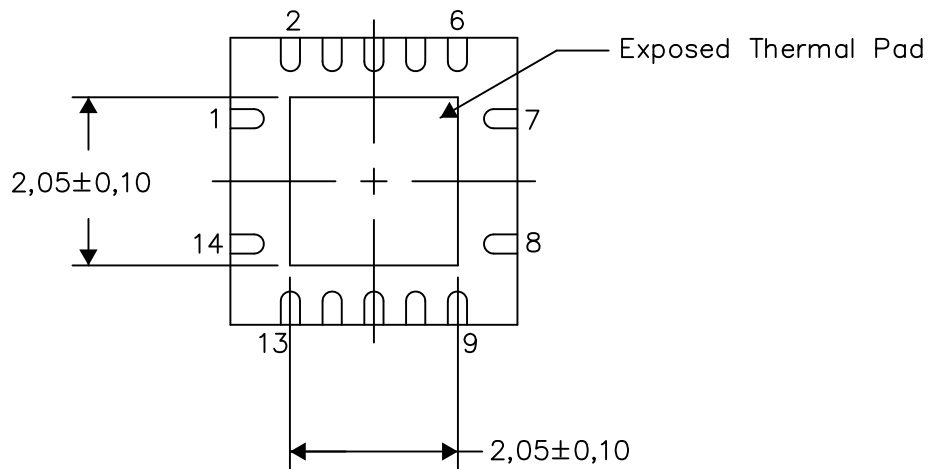
PLASTIC QUAD FLATPACK NO-LEAD

**THERMAL INFORMATION**

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-2/P 03/14

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

## GENERIC PACKAGE VIEW

**BQA 14**

**WQFN - 0.8 mm max height**

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4227145/A



# EXAMPLE BOARD LAYOUT

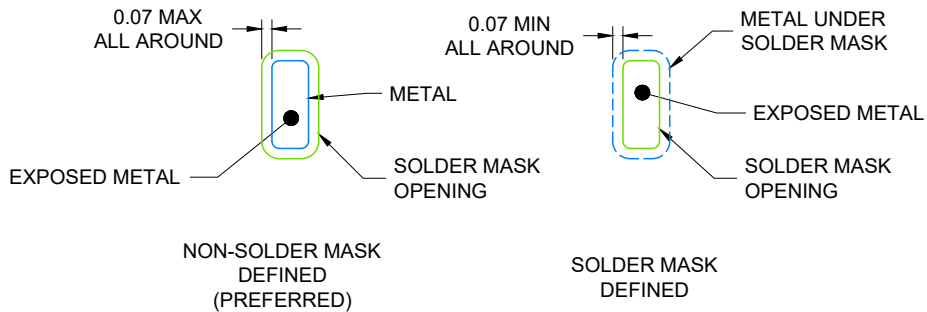
BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
 88% PRINTED COVERAGE BY AREA  
 SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only.
  - Falls within MIL STD 1835 GDFP1-F14

# DB0014A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

J 14

**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

J0014A



# PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

**NOTES:**

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

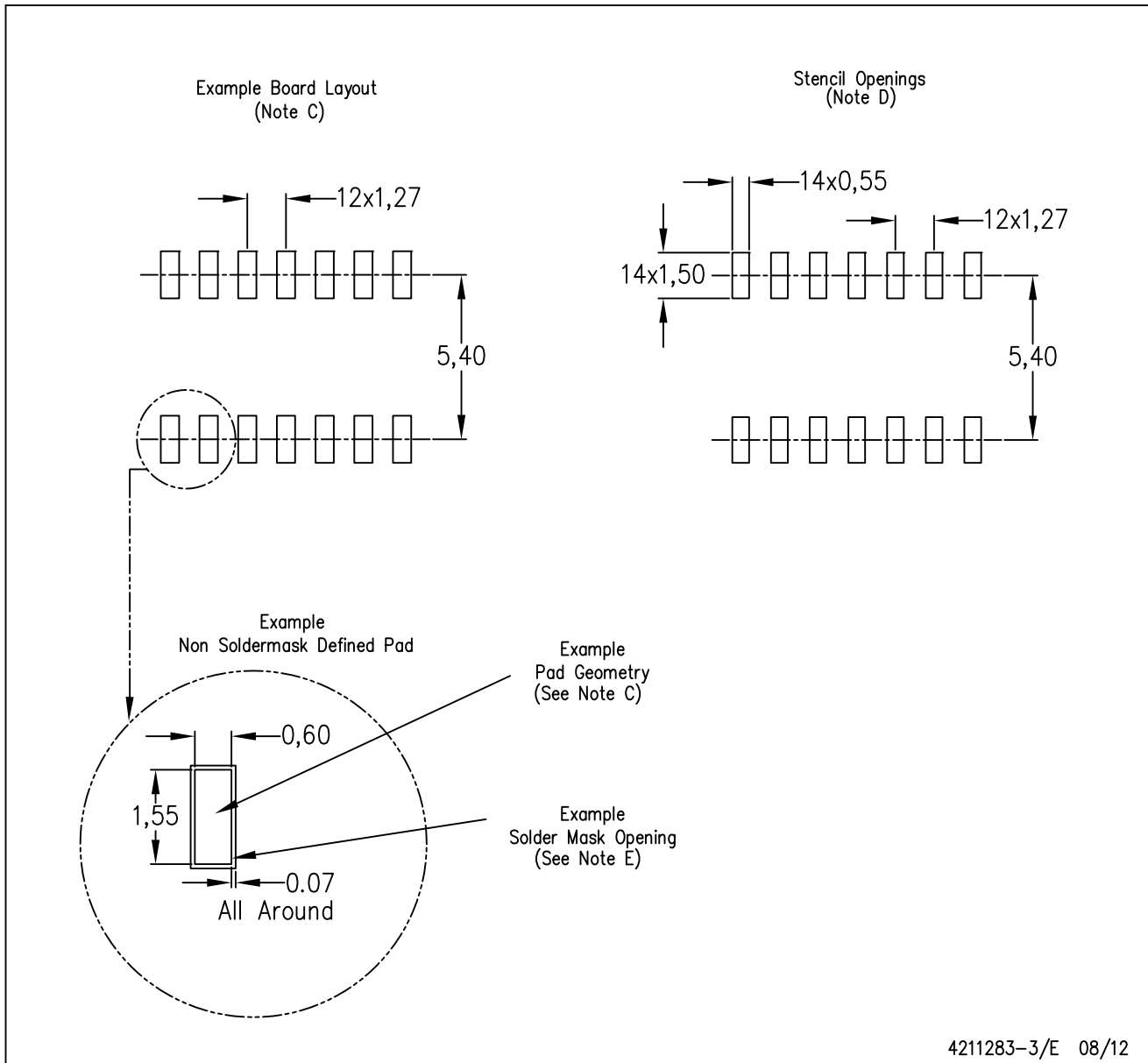
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

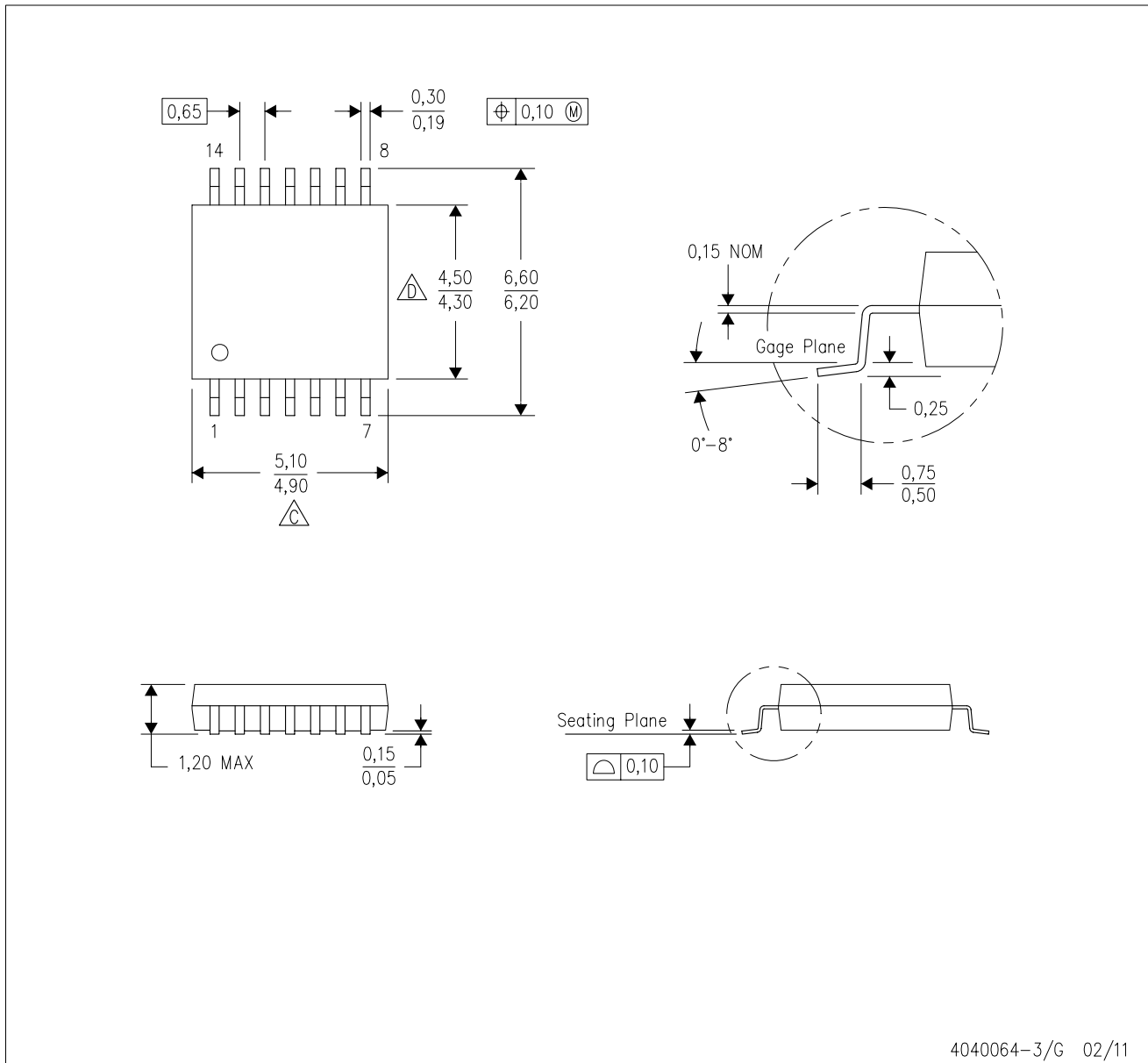


4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View SN74LVC32ANS](#) on WIN SOURCE

 [Texas Instruments](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management