



# THE DATASHEET OF SP8M5TB



# Switching

## SP8M5

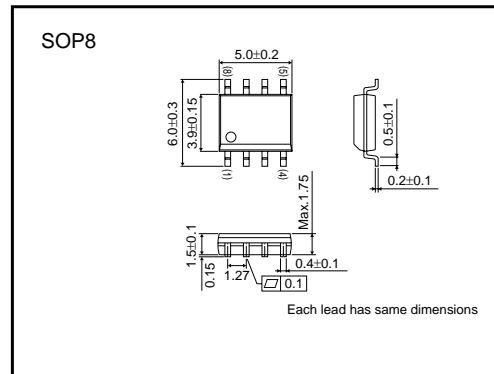
●Features

- 1) Low on-resistance.
- 2) Built-in G-S Protection Diode.
- 3) Small and Surface Mount Package (SOP8).

●Application

Power switching, DC / DC converter.

●External dimensions (Unit : mm)

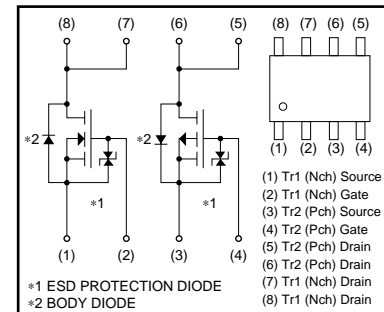


●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits		Unit
		Nchannel	Pchannel	
Drain-source voltage	V <sub>DSS</sub>	30	-30	V
Gate-source voltage	V <sub>GSS</sub>	±20	±20	V
Drain current	Continuous	I <sub>D</sub>	±6.0	A
	Pulsed	I <sub>DP</sub>	±24	A *1
Source current (Body diode)	Continuous	I <sub>S</sub>	1.6	A
	Pulsed	I <sub>SP</sub>	6.4	A *1
Total power dissipation (T <sub>C</sub> =25°C)	P <sub>D</sub>	2	2	W *2
Channel temperature	T <sub>ch</sub>	150	150	°C
Storage temperature	T <sub>stg</sub>	-55 to +150	-55 to +150	°C

\*1 Pw≤10μs, Duty cycles≤1%  
\*2 MOUNTED ON A CERAMIC BOARD.

●Equivalent circuit



\*A protection diode is included between the gate and the source terminals to protect the diode against static electricity when the product is in use. Use the protection circuit when the fixed voltages are exceeded.

●Thermal resistance (Ta=25°C)

Parameter	Symbol	Limits	Unit
Channel to ambient	R <sub>th</sub> (ch-A)	62.5	°C / W *

\*MOUNTED ON A CERAMIC BOARD.

## Transistors

## N-ch

## ●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I <sub>GSS</sub>	–	–	±10	μA	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V
Drain-source breakdown voltage	V <sub>(BR) DSS</sub>	30	–	–	V	I <sub>D</sub> =1mA, V <sub>GS</sub> =0V
Zero gate voltage drain current	I <sub>DSS</sub>	–	–	1	μA	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V
Gate threshold voltage	V <sub>GS(th)</sub>	1.0	–	2.5	V	V <sub>DS</sub> =10V, I <sub>D</sub> =1mA
Static drain-source on-state resistance	R <sub>DS(on)</sub> *	–	21	28	mΩ	I <sub>D</sub> =6.0A, V <sub>GS</sub> =10V
		–	30	41		I <sub>D</sub> =6.0A, V <sub>GS</sub> =4.5V
		–	33	45		I <sub>D</sub> =6.0A, V <sub>GS</sub> =4V
Forward transfer admittance	Y <sub>fs</sub>  *	4.0	–	–	S	I <sub>D</sub> =6.0A, V <sub>DS</sub> =10V
Input capacitance	C <sub>iss</sub>	–	520	–	pF	V <sub>DS</sub> =10V
Output capacitance	C <sub>oss</sub>	–	150	–	pF	V <sub>GS</sub> =0V
Reverse transfer capacitance	C <sub>rss</sub>	–	95	–	pF	f=1MHz
Turn-on delay time	t <sub>d(on)</sub> *	–	9	–	ns	I <sub>D</sub> =3A, V <sub>DD</sub> ≐15V
Rise time	t <sub>r</sub> *	–	21	–	ns	V <sub>GS</sub> =10V
Turn-off delay time	t <sub>d(off)</sub> *	–	36	–	ns	R <sub>L</sub> =5.00Ω
Fall time	t <sub>f</sub> *	–	13	–	ns	R <sub>GS</sub> =10Ω
Total gate charge	Q <sub>g</sub> *	–	7.2	10.1	nC	V <sub>DD</sub> ≐15V
Gate-source charge	Q <sub>gs</sub> *	–	1.8	–	nC	V <sub>GS</sub> =5V
Gate-drain charge	Q <sub>gd</sub> *	–	2.8	–	nC	I <sub>D</sub> =6.0A

\*Pulsed

## ●Body diode characteristics (Source-Drain Characteristics) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V <sub>SD</sub> *	–	–	1.2	V	I <sub>S</sub> =6.4A, V <sub>GS</sub> =0V

\*Pulsed

## Transistors

## P-ch

## ●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I <sub>GSS</sub>	–	–	±10	μA	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V
Drain-source breakdown voltage	V <sub>(BR) DSS</sub>	–30	–	–	V	I <sub>D</sub> = –1mA, V <sub>GS</sub> =0V
Zero gate voltage drain current	I <sub>DSS</sub>	–	–	–1	μA	V <sub>DS</sub> = –30V, V <sub>GS</sub> =0V
Gate threshold voltage	V <sub>GS(th)</sub>	–1.0	–	–2.5	V	V <sub>DS</sub> = –10V, I <sub>D</sub> = –1mA
Static drain-source on-state resistance	R <sub>DS(on)</sub> *	–	20	28	mΩ	I <sub>D</sub> = –7.0A, V <sub>GS</sub> = –10V
		–	25	35		I <sub>D</sub> = –7.0A, V <sub>GS</sub> = –4.5V
		–	30	42		I <sub>D</sub> = –7.0A, V <sub>GS</sub> = –4.0V
Forward transfer admittance	Y <sub>fs</sub>   *	6.0	–	–	S	I <sub>D</sub> = –7.0A, V <sub>DS</sub> = –10V
Input capacitance	C <sub>iss</sub>	–	2600	–	pF	V <sub>DS</sub> = –10V
Output capacitance	C <sub>oss</sub>	–	450	–	pF	V <sub>GS</sub> =0V
Reverse transfer capacitance	C <sub>rss</sub>	–	350	–	pF	f=1MHz
Turn-on delay time	t <sub>d(on)</sub> *	–	20	–	ns	I <sub>D</sub> = –3.5A, V <sub>DD</sub> ≐ –15V
Rise time	t <sub>r</sub> *	–	50	–	ns	V <sub>GS</sub> = –10V
Turn-off delay time	t <sub>d(off)</sub> *	–	110	–	ns	R <sub>L</sub> =4.3Ω
Fall time	t <sub>f</sub> *	–	70	–	ns	R <sub>GS</sub> =10Ω
Total gate charge	Q <sub>g</sub> *	–	25	–	nC	V <sub>DD</sub> ≐ –15V
Gate-source charge	Q <sub>gs</sub> *	–	5.5	–	nC	V <sub>GS</sub> = –5V
Gate-drain charge	Q <sub>gd</sub> *	–	10	–	nC	I <sub>D</sub> = –7.0A

\*Pulsed

## ●Body diode characteristics (Source-Drain Characteristics) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V <sub>SD</sub> *	–	–	–1.2	V	I <sub>S</sub> = –1.6A, V <sub>GS</sub> =0V

\*Pulsed

Transistors

N-ch

●Electrical characteristic curves

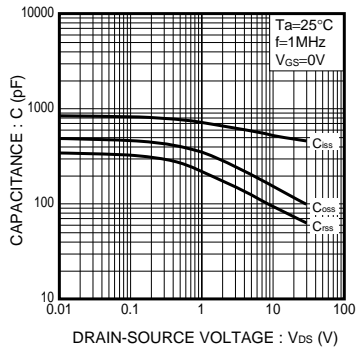


Fig.1 Typical Capacitance vs. Drain-Source Voltage

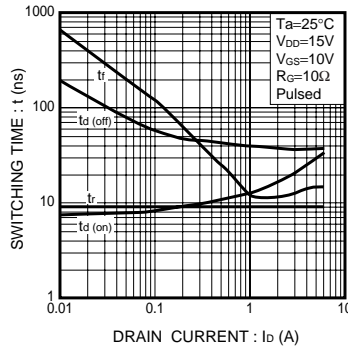


Fig.2 Switching Characteristics

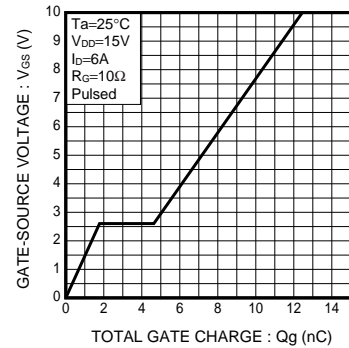


Fig.3 Dynamic Input Characteristics

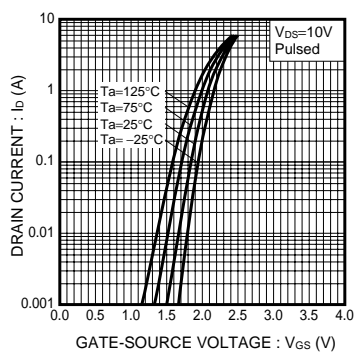


Fig.4 Typical Transfer Characteristics

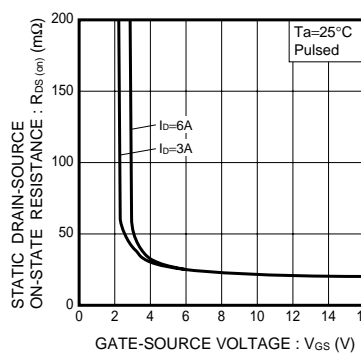


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

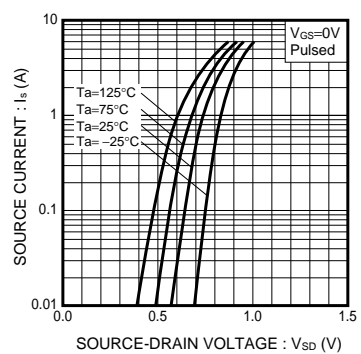


Fig.6 Source Current vs. Source-Drain Voltage

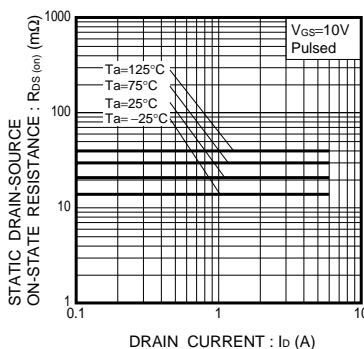


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (I)

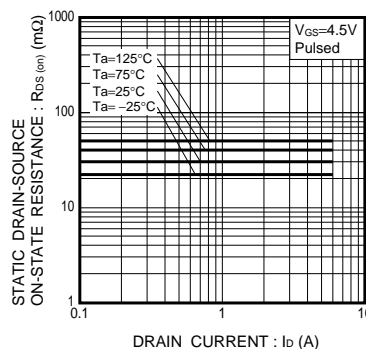


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (II)

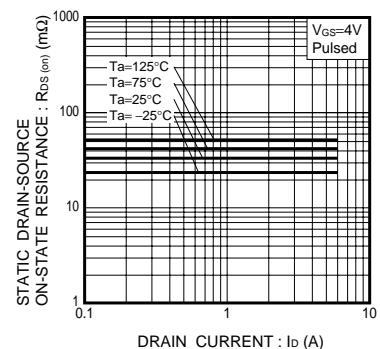


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (III)

Transistors

P-ch

●Electrical characteristic curves

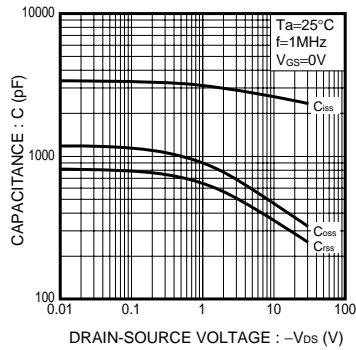


Fig.1 Typical Capacitance vs. Drain-Source Voltage

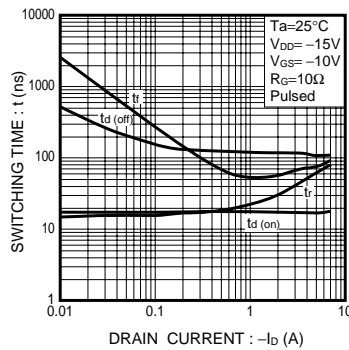


Fig.2 Switching Characteristics

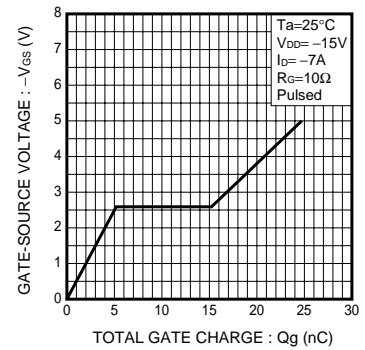


Fig.3 Dynamic Input Characteristics

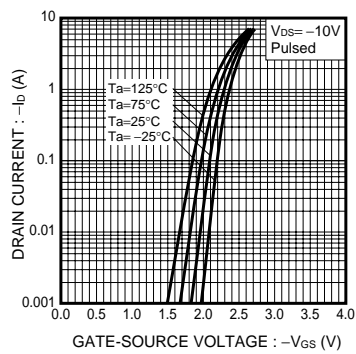


Fig.4 Typical Transfer Characteristics

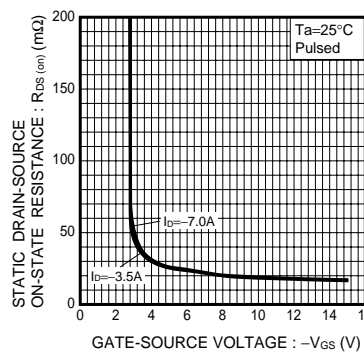


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

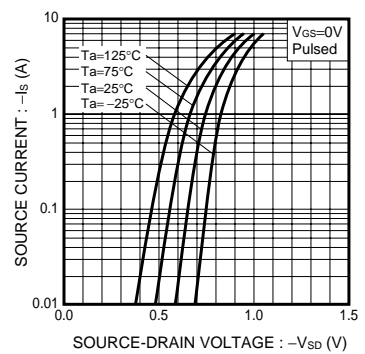


Fig.6 Source Current vs. Source-Drain Voltage

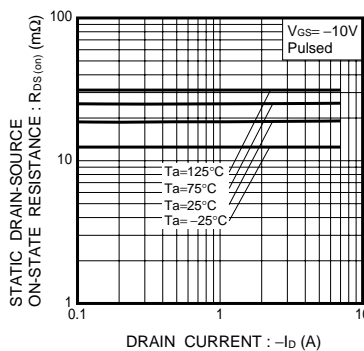


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (I)

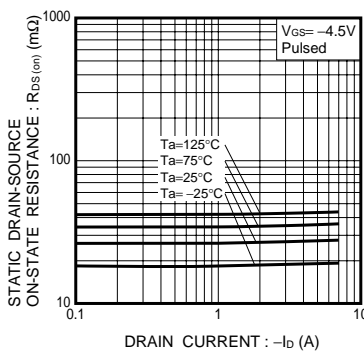


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (II)

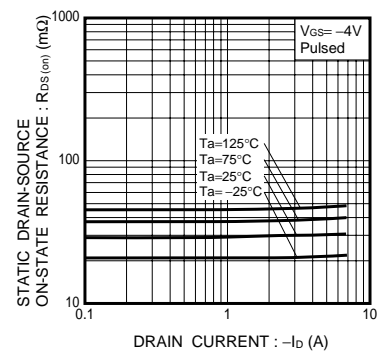


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (III)

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