



**THE DATASHEET OF  
SPZT751T1G**



# PNP Silicon Planar Epitaxial Transistor

## PZT751T1

This PNP Silicon Epitaxial transistor is designed for use in industrial and consumer applications. The device is housed in the SOT-223 package which is designed for medium power surface mount applications.

### Features

- High Current
- The SOT-223 Package can be soldered using wave or reflow.
- SOT-223 Package Ensures Level Mounting, Resulting in Improved Thermal Conduction, and Allows Visual Inspection of Soldered Joints. The Formed Leads Absorb Thermal Stress During Soldering, Eliminating the Possibility of Damage to the Die
- NPN Complement is PZT651T1G
- S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant\*

### MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO}$	-60	Vdc
Collector-Base Voltage	$V_{CBO}$	-80	Vdc
Emitter-Base Voltage	$V_{EBO}$	-5.0	Vdc
Collector Current	$I_C$	-2.0	Adc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1) Derate above $25^\circ\text{C}$	$P_D$	0.8 6.4	W mW/ $^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-65 to 150	$^\circ\text{C}$
Junction Temperature	$T_J$	150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

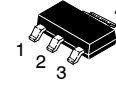
1. Device mounted on a FR-4 glass epoxy printed circuit board using minimum recommended footprint.

### THERMAL CHARACTERISTICS

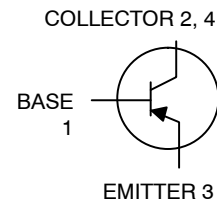
Rating	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient in Free Air	$R_{\theta JA}$	156	$^\circ\text{C}/\text{W}$
Maximum Temperature for Soldering Purposes Time in Solder Bath	$T_L$	260 10	$^\circ\text{C}$ Sec

\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

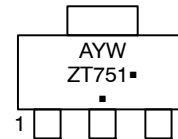
## SOT-223 PACKAGE HIGH CURRENT NPN SILICON TRANSISTOR SURFACE MOUNT



SOT-223  
CASE 318E  
STYLE 1



### MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
PZT751T1G	SOT-223 (Pb-Free)	1,000 / Tape & Reel
SPZT751T1G	SOT-223 (Pb-Free)	1,000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# PZT751T1

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Breakdown Voltage ( $I_C = -10\text{ mAdc}$ , $I_B = 0$ )	$V_{(BR)CEO}$	-60	-	Vdc
Collector–Emitter Breakdown Voltage ( $I_C = -100\ \mu\text{Adc}$ , $I_E = 0$ )	$V_{(BR)CBO}$	-80	-	Vdc
Emitter–Base Breakdown Voltage ( $I_E = -10\ \mu\text{Adc}$ , $I_C = 0$ )	$V_{(BR)EBO}$	-5.0	-	Vdc
Base–Emitter Cutoff Current ( $V_{EB} = -4.0\text{ Vdc}$ )	$I_{EBO}$	-	-0.1	$\mu\text{Adc}$
Collector–Base Cutoff Current ( $V_{CB} = -80\text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	-	-100	nAdc
<b>ON CHARACTERISTICS (Note 2)</b>				
DC Current Gain ( $I_C = -50\text{ mAdc}$ , $V_{CE} = -2.0\text{ Vdc}$ ) ( $I_C = -500\text{ mAdc}$ , $V_{CE} = -2.0\text{ Vdc}$ ) ( $I_C = -1.0\text{ Adc}$ , $V_{CE} = -2.0\text{ Vdc}$ ) ( $I_C = -2.0\text{ Adc}$ , $V_{CE} = -2.0\text{ Vdc}$ )	$h_{FE}$	75 75 75 40	- - - -	-
Collector–Emitter Saturation Voltages ( $I_C = -2.0\text{ Adc}$ , $I_B = -200\text{ mAdc}$ ) ( $I_C = -1.0\text{ Adc}$ , $I_B = -100\text{ mAdc}$ )	$V_{CE(sat)}$	- -	-0.5 -0.3	Vdc
Base–Emitter Voltages ( $I_C = -1.0\text{ Adc}$ , $V_{CE} = -2.0\text{ Vdc}$ )	$V_{BE(on)}$	-	-1.0	Vdc
Base–Emitter Saturation Voltage ( $I_C = -1.0\text{ Adc}$ , $I_B = -100\text{ mAdc}$ )	$V_{BE(sat)}$	-	-1.2	Vdc
Current–Gain–Bandwidth ( $I_C = -50\text{ mAdc}$ , $V_{CE} = -5.0\text{ Vdc}$ , $f = 100\text{ MHz}$ )	$f_T$	75	-	MHz

2. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle = 2.0%.

# PZT751T1

## TYPICAL CHARACTERISTICS

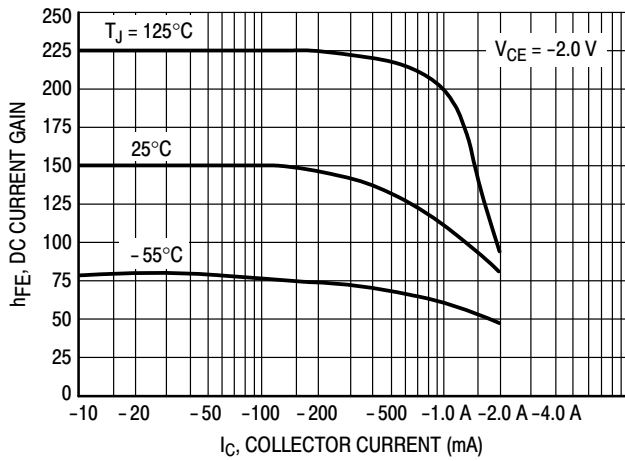


Figure 1. Typical DC Current Gain

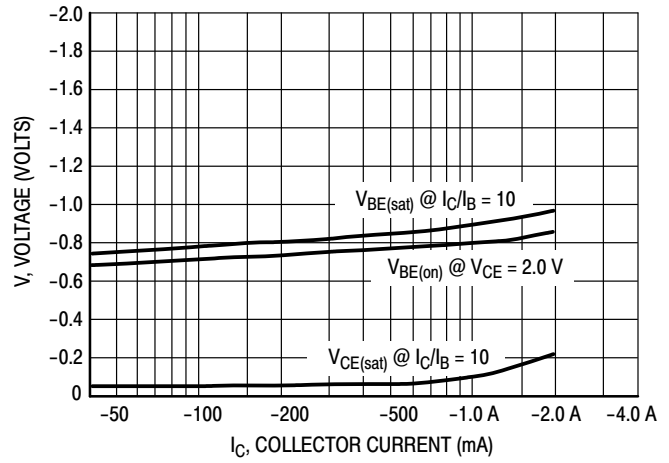


Figure 2. On Voltages

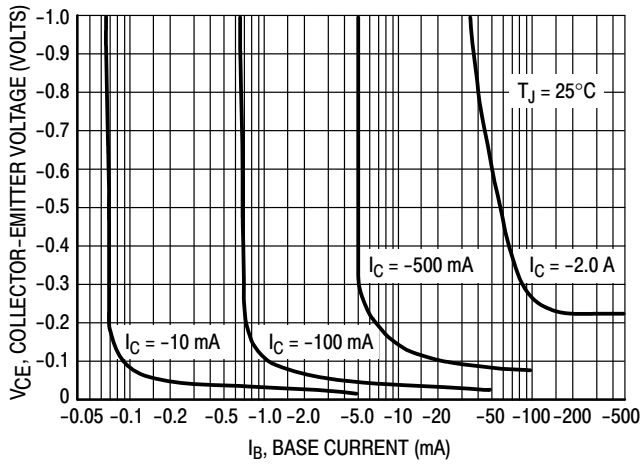


Figure 3. Collector Saturation Region

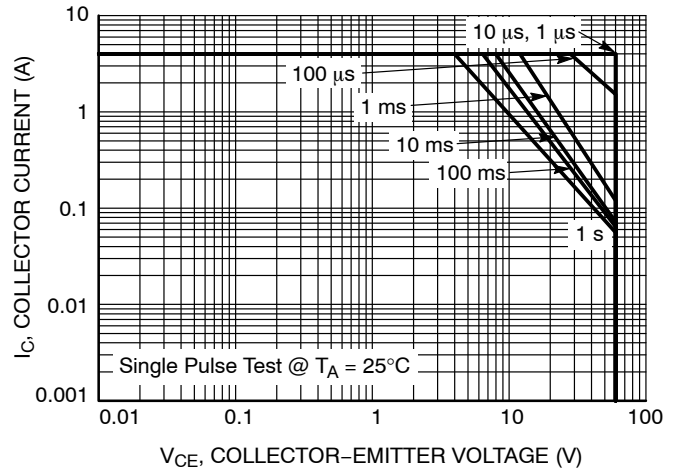


Figure 4. Safe Operating Area

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

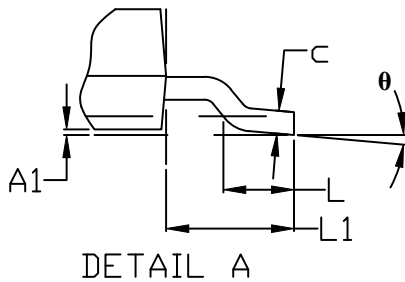
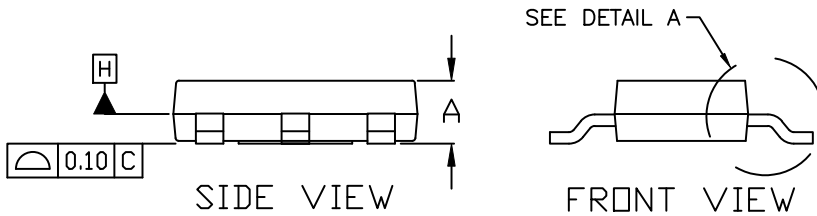
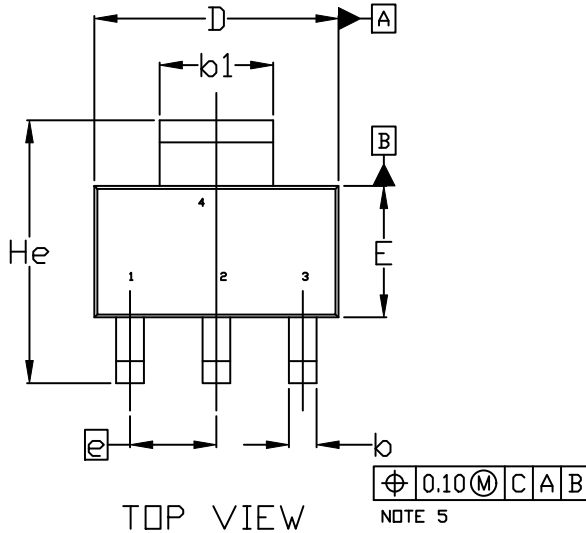
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SCALE 1:1

SOT-223 (TO-261)  
CASE 318E-04  
ISSUE R

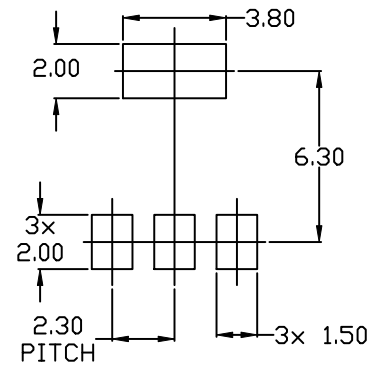
DATE 02 OCT 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
$\theta$	0°	---	10°



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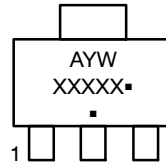
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**SOT-223 (TO-261)**  
**CASE 318E-04**  
**ISSUE R**

DATE 02 OCT 2018

- |  |   |   |   |   |
|--|---|---|---|---|
| <b>STYLE 1:</b><br>PIN 1. BASE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | <b>STYLE 2:</b><br>PIN 1. ANODE<br>2. CATHODE<br>3. NC<br>4. CATHODE        | <b>STYLE 3:</b><br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE<br>4. DRAIN           | <b>STYLE 4:</b><br>PIN 1. SOURCE<br>2. DRAIN<br>3. GATE<br>4. DRAIN   | <b>STYLE 5:</b><br>PIN 1. DRAIN<br>2. GATE<br>3. SOURCE<br>4. GATE    |
| <b>STYLE 6:</b><br>PIN 1. RETURN<br>2. INPUT<br>3. OUTPUT<br>4. INPUT        | <b>STYLE 7:</b><br>PIN 1. ANODE 1<br>2. CATHODE<br>3. ANODE 2<br>4. CATHODE | <b>STYLE 8:</b><br>CANCELLED  | <b>STYLE 9:</b><br>PIN 1. INPUT<br>2. GROUND<br>3. LOGIC<br>4. GROUND | <b>STYLE 10:</b><br>PIN 1. CATHODE<br>2. ANODE<br>3. GATE<br>4. ANODE |
| <b>STYLE 11:</b><br>PIN 1. MT 1<br>2. MT 2<br>3. GATE<br>4. MT 2             | <b>STYLE 12:</b><br>PIN 1. INPUT<br>2. OUTPUT<br>3. NC<br>4. OUTPUT         | <b>STYLE 13:</b><br>PIN 1. GATE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR |   |   |

**GENERIC  
 MARKING DIAGRAM\***



- A = Assembly Location
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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