THE DATASHEET OF

XR71211EHTR-F

XR75100

40V Synchronous Step Down COT Controller

General Description

The XR75100 is a synchronous step-down controller for point-of load supplies up to 20A. A wide 5.5V to 40V input voltage range allows for single supply operation from industry standard 12V, 18V, and 24V DC and AC rails.

With a proprietary emulated current mode Constant On-Time (COT) control scheme, the XR75100 provides extremely fast line and load transient response using ceramic output capacitors. It requires no loop compensation hence simplifying circuit implementation and reducing overall component count. The control loop also provides exceptional load and line regulation and maintains constant operating frequency. A selectable power saving mode allows the user to operate in discontinuous mode (DCM) at light current loads, thereby significantly increasing the converter efficiency.

A host of protection features, including over-current, over-temperature, short-circuit and UVLO, help achieve safe operation under abnormal operating conditions.

The XR75100 is available in a RoHS compliant, green / halogen free space-saving 16-pin 3x3mm QFN package.

FEATURES

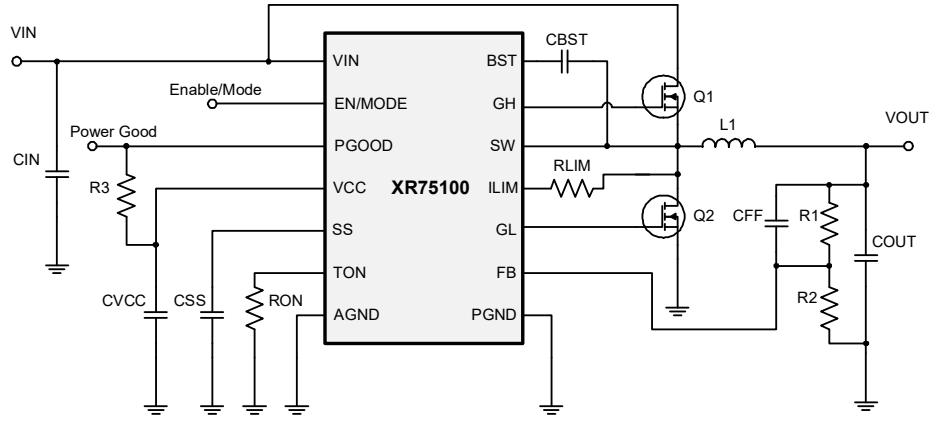
- 20A capable step-down controller
  - Wide 5.5V to 40V input voltage range
  - Integrated high current 2A / 3A drivers
  - 0.6 to 30V adjustable output voltage
- Proprietary Constant On-Time control
  - No loop compensation required
  - Stable ceramic output capacitor operation
  - Programmable 200ns to 2µs on-time
  - Constant 100kHz to 800kHz frequency
  - Selectable CCM or CCM / DCM operation
- Programmable hiccup current limit with thermal compensation
- Precision enable and Power Good flag
- Programmable soft-start
- Integrated bootstrap diode
- 16-pin QFN package

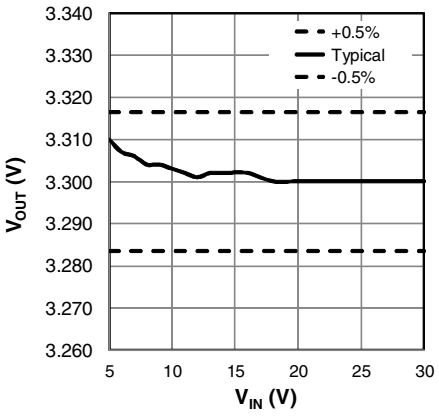
APPLICATIONS

- Networking and communications
- Fast transient Point-of-Loads
- Industrial and medical equipment
- Embedded high power FPGA

Ordering Information – back page

Typical Application





Absolute Maximum Ratings

Stresses beyond the limits listed below may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

V_{IN}.....-0.3V to 43V

V_{CC}.....-0.3V to 6.0V

BST.....-0.3V to 48V[2]

BST-SW.....-0.3V to 6V

SW, ILIM.....-5V to 43V[1, 2]

GH.....-0.3V to BST+0.3V

GH-SW.....-0.3V to 6V

ALL other pins.....-0.3V to VCC+0.3V

Storage temperature.....-65°C to +150°C

Junction temperature.....150°C

Power dissipation.....Internally Limited

Lead temperature (soldering, 10 sec).....300°C

ESD rating (HBM - Human Body Model).....2kV

Operating Conditions

V_{IN}.....-0.3V to 40V

V_{CC}.....-0.3V to 5.5V

SW, ILIM.....-1V to 40V[1]

PGOOD, TON, SS, EN, GL, FB.....-0.3V to 5.5V

Switching frequency.....100kHz to 800kHz[3]

Junction temperature range.....-40°C to +125°C

Note 1: SW pin's minimum DC range is -1V, transient is -5V for less than 50ns.

Note 2: No external voltage applied.

Note 3: Recommended

Electrical Characteristics

Unless otherwise noted: T_J= 25°C, V_{IN} = 24V, BST = V_{CC}, SW = AGND = PGND = 0V, CGH = CGL = 3.3nF, 4.7µF at VCC-AGND. Limits applying over the full operating temperature range are denoted by a "•"

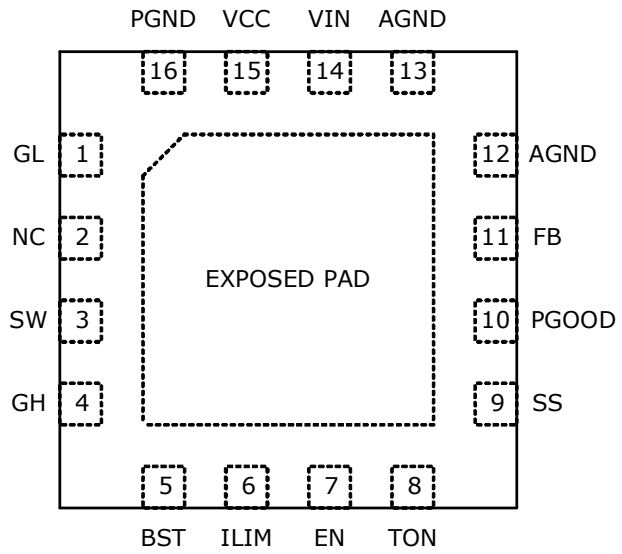
Symbol	Parameter	Conditions		Min	Typ	Max	Units
Power Supply Characteristics							
V_{IN}	Input voltage range	VCC regulating	•	5.5		40	V
I_{VIN}	VIN input supply current	Not switching, V_{IN} = 24V, VFB = 0.7V	•		0.7	2	mA
		f = 300kHz, RON = 215k, VFB = 0.58V			11		mA
I_{OFF}	Shutdown current	Enable = 0V, V_{IN} = 24V			0.1		µA
Enable and Under-Voltage Lock-Out UVLO							
V_{IH_EN}	EN pin rising threshold		•	1.8	1.9	2.0	V
V_{EN_HYS}	EN pin hysteresis				50		mV
V_{IH_EN}	EN pin rising threshold for DCM/CCM operation		•	2.9	3.0	3.1	V
V_{EN_HYS}	EN pin hysteresis				100		mV
	VCC UVLO start threshold, rising edge		•	4.00	4.25	4.50	V

Symbol	Parameter	Conditions		Min	Typ	Max	Units
	VCC UVLO hysteresis				200		mV
Reference Voltage							
V_{REF}	Reference voltage	V_{IN} = 5.5V to 40V		0.597	0.600	0.603	V
			•	0.594	0.600	0.606	V
	DC line regulation	CCM, closed loop, V_{IN} = 5.5V-30V, applies to any C_{OUT}			±0.3		%
	DC load regulation	CCM, closed loop, I_{OUT} = 0A-10A, applies to any C_{OUT}			±0.15		%
Programmable Constant On-Time							
	Maximum recommended on-time	R_{ON} = 237kΩ, V_{IN} = 40V			2.0		µs
	On-time 1	R_{ON} = 237kΩ, V_{IN} = 40V	•	1.7	2.0	2.3	µs
	f corresponding to on-time 1	V_{IN} = 40V, V_{OUT} = 24V		261	300	353	kHz
	Minimum programmable on-time	R_{ON} = 14kΩ, V_{IN} = 40V			120		ns
		R_{ON} = 14kΩ, V_{IN} = 24V			200	230	ns
	On-time 2	R_{ON} = 14kΩ, V_{IN} = 24V	•	170	200	230	ns
	f corresponding to on-time 2	V_{OUT} = 5V		906	1042	1225	kHz
		V_{OUT} = 3.3V		598	688	809	kHz
	On-time 3	R_{ON} = 35.7kΩ, V_{IN} = 24V	•	430	506	582	ns
	Minimum off-time		•		250	350	ns
Diode Emulation Mode							
	Zero crossing threshold	DC value measured during test		-4	-1	2	mV
Soft-start							
	SS charge current		•	-14	-10	-6	µA
	SS discharge current	Fault present	•	1			mA
VCC Linear Regulator							
	VCC output voltage	V_{IN} = 6V to 40V, I_{LOAD} = 0 to 30mA	•	4.8	5.0	5.2	V
		V_{IN} = 5.5V, I_{LOAD} = 0 to 20mA	•	4.8	5.0	5.2	V
Power Good Output							
	Power Good threshold			-10	-7.5	-5	%
	Power Good hysteresis				2	4	%
	Power Good sink current			1			mA
Protection: OCP, OTP, Short-Circuit							
	Hiccup timeout				110		ms
	ILIM pin source current			45	50	55	µA
	ILIM current temperature coefficient				0.4		%/°C

Symbol	Parameter	Conditions		Min	Typ	Max	Units
	OCP comparator offset		•	-8	0	+8	mV
	Current limit blanking	GL rising>1V			100		ns
	Thermal shutdown threshold[1]	Rising temperature			150		°C
	Thermal hysteresis[1]				15		°C
	VSCTH feedback pin short-circuit threshold	Percent of VREF, short circuit is active after PGOOD is up	•	50	60	70	%
Output Gate Drivers							
	GH pull-down resistance	IGH = 200mA			1.35	2.0	Ω
	GH pull-up resistance	IGH = 200mA			1.8	2.8	Ω
	GL pull-down resistance	IGL = 200mA			1.35	1.9	Ω
	GL pull-up resistance	IGL = 200mA			1.7	2.7	Ω
	GH and GL pull-down resistance				50		kΩ
	GH and GL rise time	10% to 90%			35	50	ns
	GH and GL fall time	90% to 10%			30	40	ns
	GL to GH non-overlap time	Measured GL falling edge = 1V to GH rising edge = 1V, BST = VCC, SW = 0V			30	60	ns
	GH to GL non-overlap time	Measured GH falling edge = 1V to GL rising edge = 1V			20	40	ns

Note 1: Guaranteed by design.

Pin Configuration

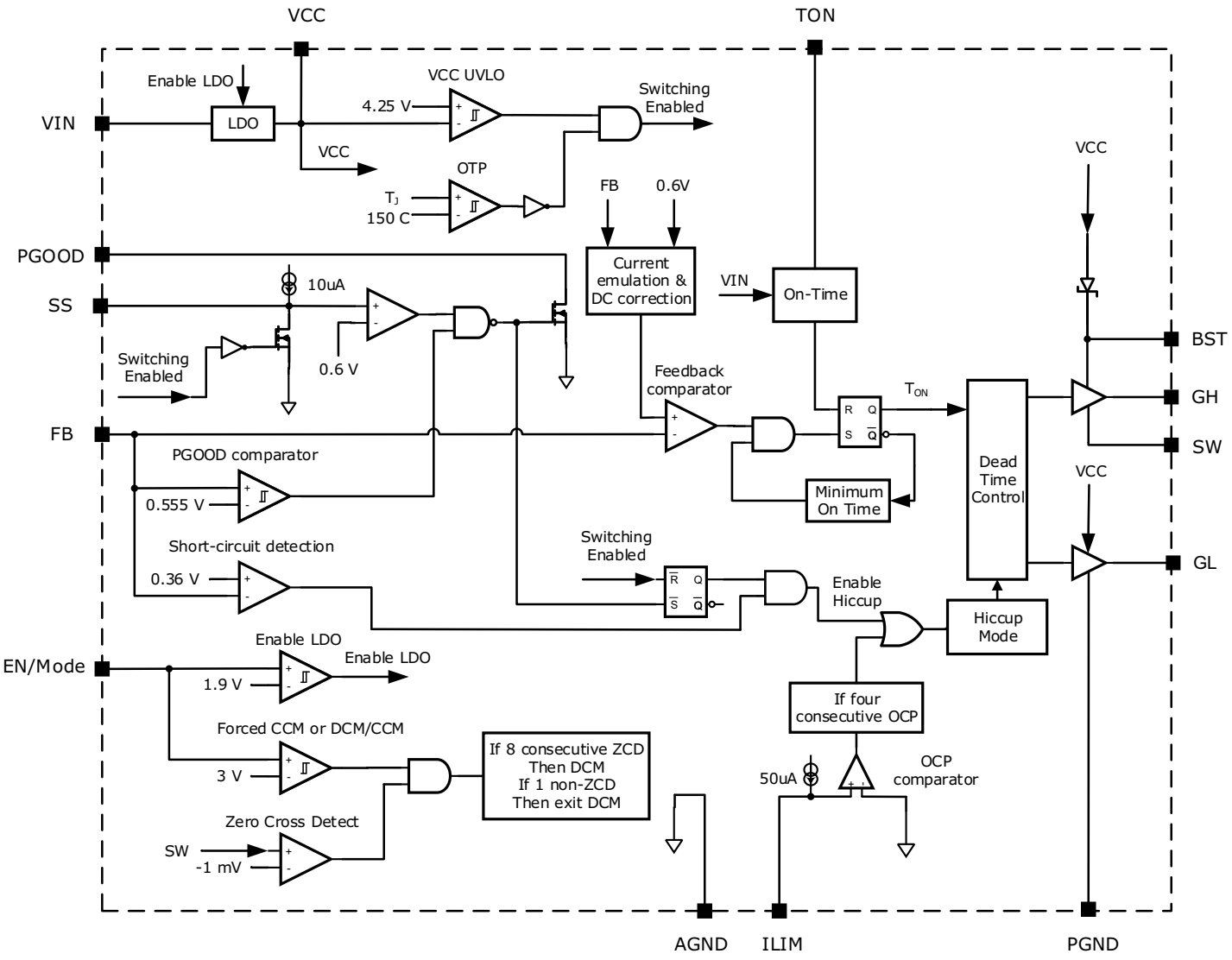


Pin Assignments

Pin No.	Pin Name	Type	Description
1	GL	O	Driver output for low-side N-channel synchronous MOSFET.
2	NC		Internally not connected. Leave this pin floating.
3	SW	A	Lower supply rail for high-side gate driver GH. Connect this pin to the junction between the two external N-channel MOSFETs.
4	GH	O	Driver output for high-side N-channel switching MOSFET.
5	BST	A	High-side driver supply pin. Connect a 0.1µF bootstrap capacitor between BST and SW.
6	ILIM	A	Over-current protection programming. Connect with a resistor to the drain of the low-side MOSFET.
7	EN/MODE	I	Precision enable pin. Pulling this pin above 1.9V will turn the IC on and it will operate in Forced CCM. If the voltage is raised above 3.0V, then the IC will operate in DCM or CCM depending on load.
8	TON	A	Constant on-time programming pin. Connect with a resistor to AGND.
9	SS	A	Soft-start pin. Connect an external capacitor between SS and AGND to program the soft-start rate based on the 10µA internal source current.
10	PGOOD	OD	Power-good output. This open-drain output is pulled low when VOUT is outside the regulation.
11	FB	A	Feedback input to feedback comparator. Connect with a set of resistors to VOUT and GND in order to program VOUT.
12, 13	AGND	A	Analog ground. Control circuitry of the IC is referenced to this pin.
14	VIN	PWR	IC supply input. Provides power to internal LDO.
15	VCC	PWR	The output of LDO. For operation using a 5V rail, VCC should be shorted to VIN.
16	PGND	PWR	Low side driver ground.
	Exposed Pad	A	Thermal pad for heat dissipation. Connect to AGND with a short trace.

Type: A = Analog, I = Input, O = Output, I/O = Input/Output, PWR = Power, OD = Open-Drain

Functional Block Diagram



Typical Performance Characteristics

Unless otherwise noted: V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 10A, f = 500kHz, T_A = 25°C. Schematic from the application information section.

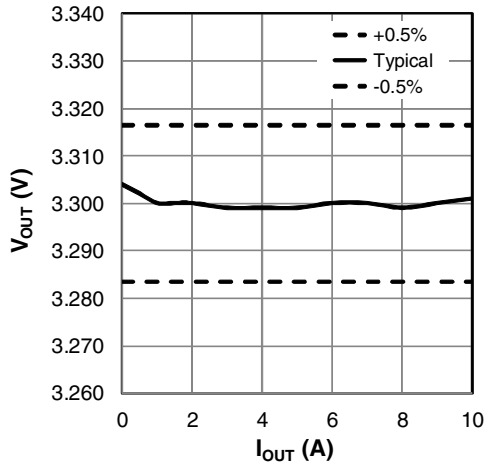


Figure 1: Load Regulation

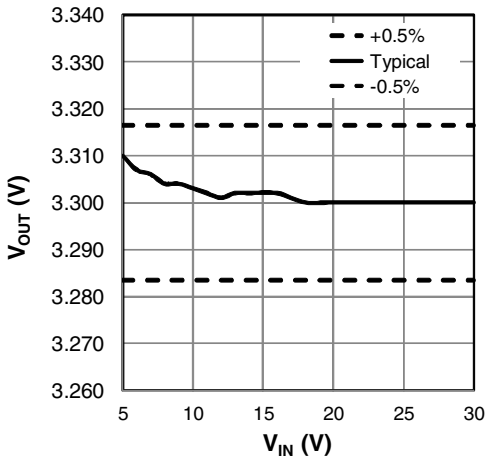


Figure 2: Line Regulation

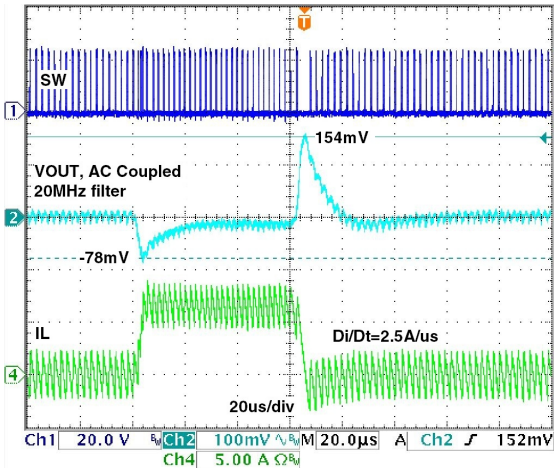


Figure 3: Load Step, Forced CCM, 0A - 6.5A - 0A

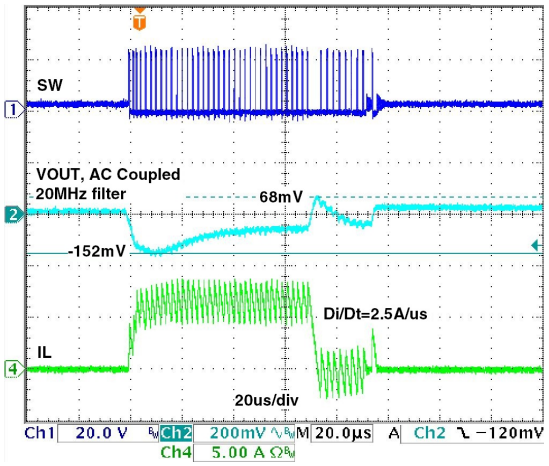


Figure 4: Load Step, DCM / CCM, 0A - 6.5A - 0A

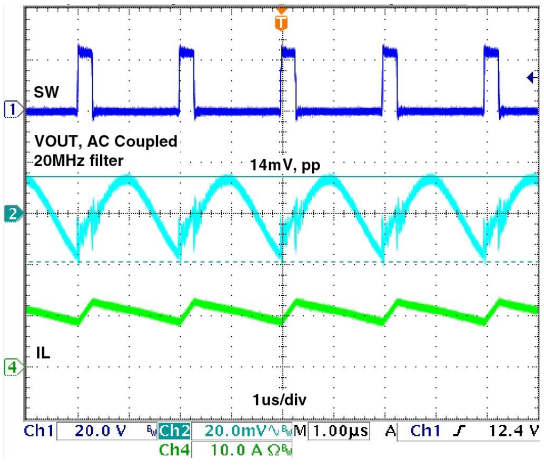


Figure 5: Steady State, $V_{OUT,ripple}$ = 14mV, I_{OUT} = 10A

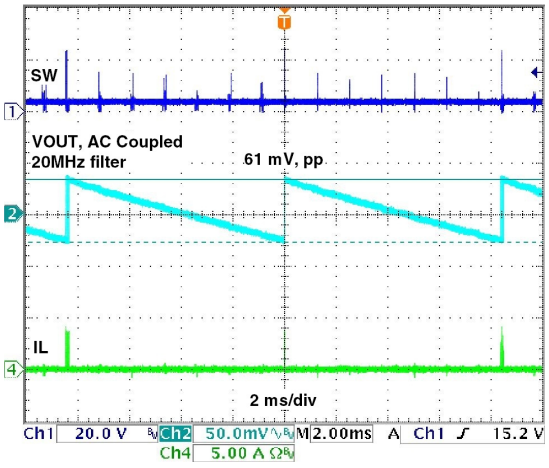


Figure 6: Steady State, DCM, $V_{OUT,ripple}$ = 61mV, I_{OUT} = 0A

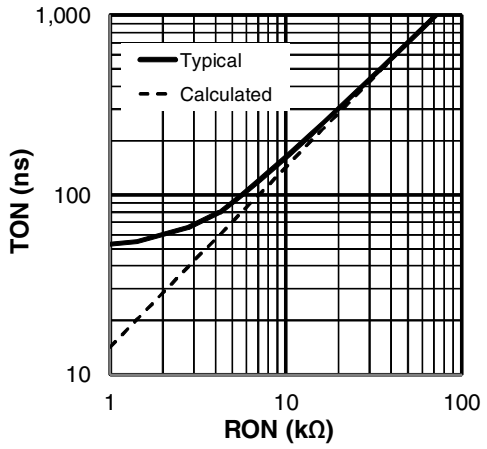


Figure 7: TON versus RON, V_{IN} = 24V

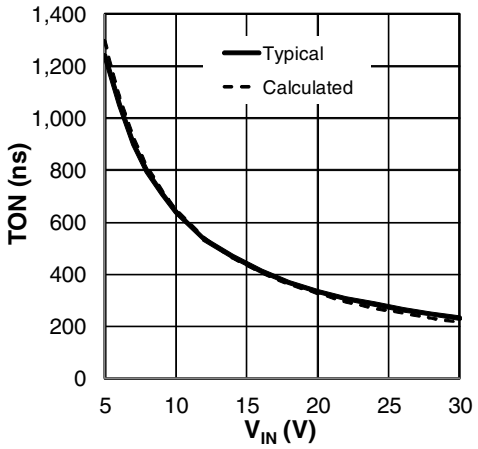


Figure 8: TON versus V_{IN}, RON = 19.1kΩ

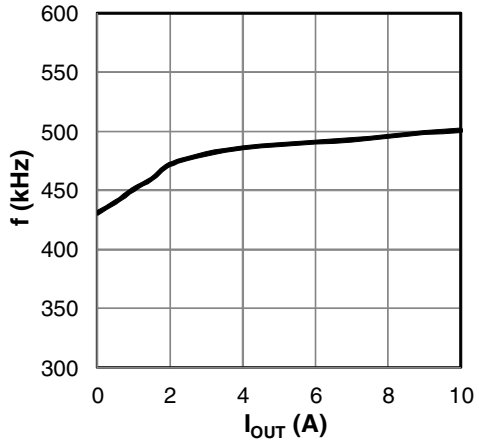


Figure 9: Frequency versus I_{OUT}, V_{IN} = 24V

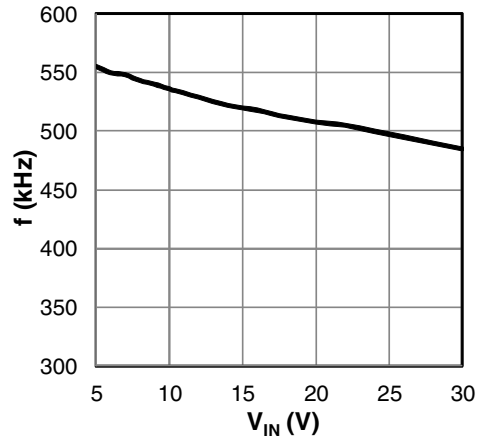


Figure 10: Frequency versus V_{IN}, I_{OUT} = 10A

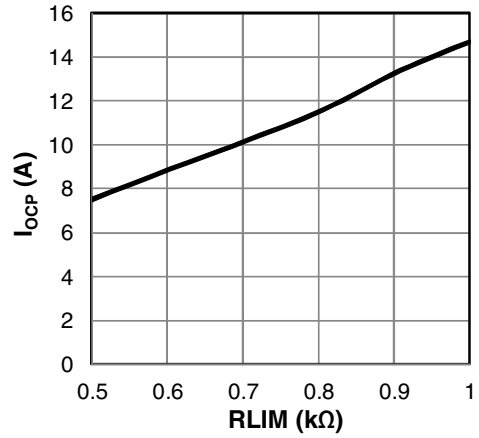


Figure 11: I_{OCP} versus RLIM

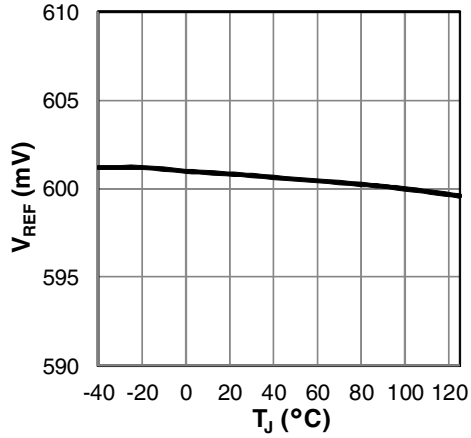


Figure 12: V_{REF} versus Temperature

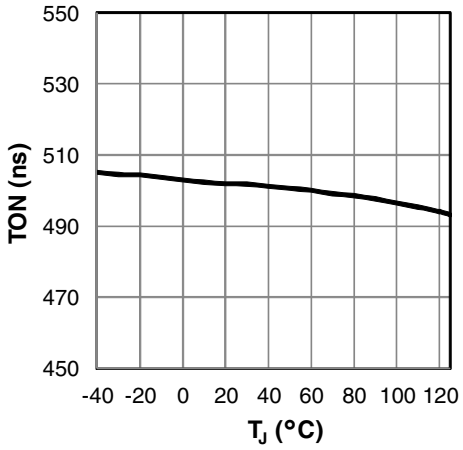


Figure 13: TON versus Temperature

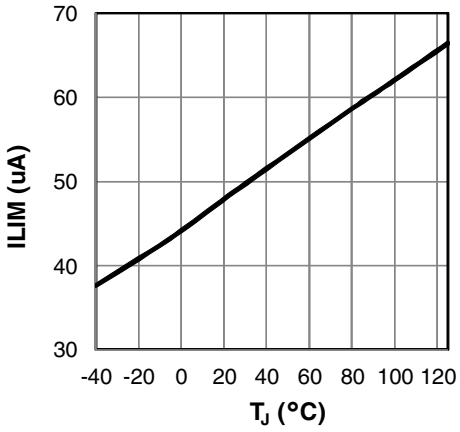


Figure 14: ILIM versus Temperature

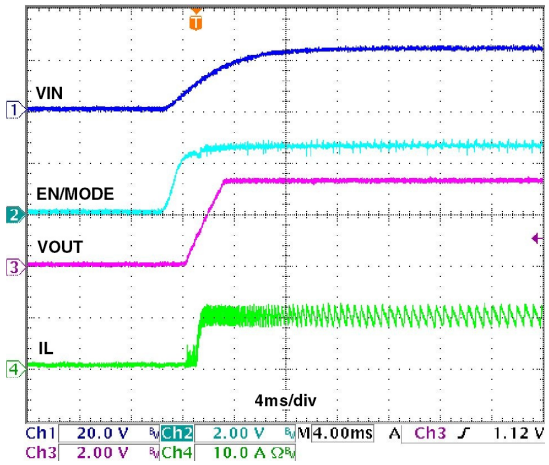


Figure 15: Power-up, Forced CCM

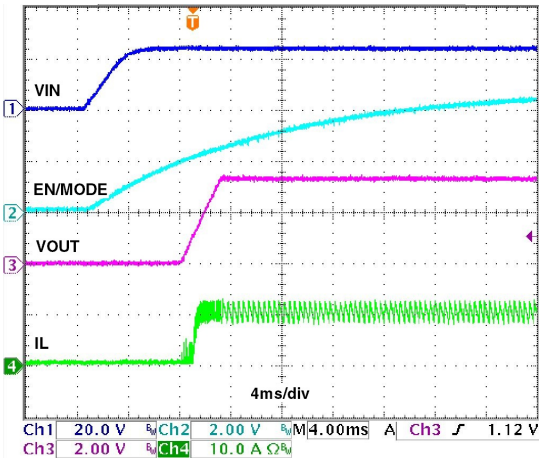


Figure 16: Power-up, DCM / CCM

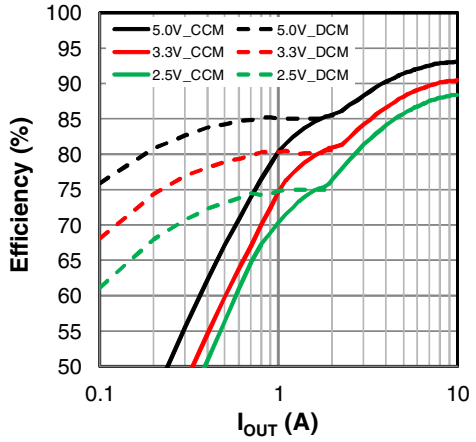


Figure 17: Efficiency, V_{IN} = 24V, f = 500kHz

Functional Description

XR75100 is a synchronous step-down, proprietary emulated current-mode Constant On-Time (COT) controller. The on-time, which is programmed via R_{ON}, is inversely proportional to V_{IN} and maintains a nearly constant frequency. The emulated current-mode control is stable with ceramic output capacitors.

Each switching cycle begins with GH signal turning on the high-side (control) FET for a preprogrammed time. At the end of the on-time, the high-side FET is turned off and the low - side (synchronous) FET is turned on for a preset minimum time (250ns nominal). This parameter is termed Minimum Off-Time. After the Minimum Off-Time, the voltage at the feedback pin FB is compared to an internal voltage ramp at the feedback comparator. When V_{FB} drops below the ramp voltage, the high-side FET is turned on and the cycle repeats. This voltage ramp constitutes an emulated current ramp and makes the use of ceramic capacitors possible, in addition to other capacitor types, for output filtering.

Enable/Mode Input (EN/MODE)

EN/MODE pin accepts a tri-level signal that is used to control turn on and off. It also selects between two modes of operation: 'Forced CCM' and 'DCM / CCM'. If EN is pulled below 1.8V, the controller shuts down. A voltage between 2.0V and 2.9V selects the Forced CCM mode, which will run the converter in continuous conduction at all times. A voltage higher than 3.1V selects the DCM / CCM mode, which will run the converter in discontinuous conduction at light loads.

Selecting the Forced CCM Mode

In order to set the controller to operate in Forced CCM, a voltage between 2.0V and 2.9V must be applied to EN/MODE. This can be achieved with an external control signal that meets the above voltage requirement. Where an external control is not available, the EN/MODE can be derived from V_{IN}. If V_{IN} is well regulated, use a resistor divider and set the voltage to 2.5V. If V_{IN} varies over a wide range, the circuit shown in Figure 18 can be used to generate the required voltage. Note that at V_{IN} of 5.5V and 40V, the nominal Zener voltage is 4.0V and 5.0V respectively. Therefore for V_{IN} in the range of 5.5V to 40V, the circuit shown in Figure 18 will generate V_{EN} required for Forced CCM.

Selecting the DCM/CCM Mode

In order to set the controller operation to DCM / CCM, a voltage between 3.1V and 5.5V must be applied to EN/MODE. If an external control signal is available, it can be directly connected to EN/MODE. In applications where an external control is not available, the EN/MODE input can be derived from V_{IN}. If V_{IN} is well regulated, use a resistor divider and set the voltage to 4V. If V_{IN} varies over a wide range, the circuit shown in Figure 19 can be used to generate the required voltage.

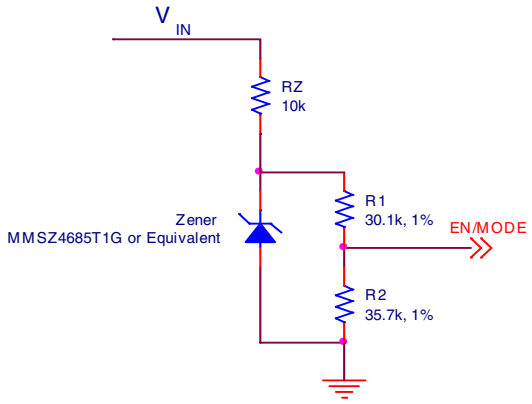


Figure 18: Selecting Forced CCM by Deriving EN/MODE from VIN

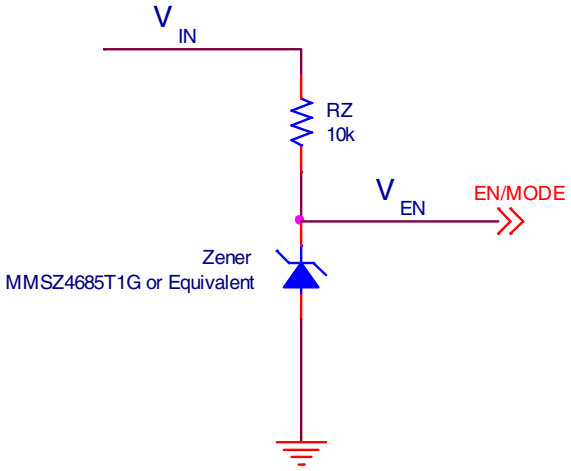


Figure 19: Selecting DCM / CCM by Deriving EN/MODE from VIN

DCM Operation

When DCM operation is enabled, the Zero Cross Detect comparator in the XR75100 senses when the current in the inductor reaches 0Amps and turns off the low side MOSFET. The low side MOSFET is operated to emulate the operation of a diode preventing the inductor current from flowing in the negative direction. In this mode, the device is now operating in Pulse Frequency Modulation (PFM) control. As the load reduces, the frequency reduces and thus the switching losses are reduced, resulting in

much better efficiency at light load. The Zero Cross comparator monitors the voltage across the low side MOSFET to determine the correct time to turn it off. Ideally, this threshold is -1mV, meaning there is still positive current in the inductor (positive inductor current refers to current from SW to VOUT). However, there is a range to the sensed voltage from -4mV to +2mV. In the case where a very low RDSON low side MOSFET is used, a higher negative inductor current is required to reach the +2mV. For instance, a 2mΩ MOSFET would require a negative 1A inductor valley current before the XR75100 recognizes the signal to turn off the low side MOSFET. As a result, the XR75100 will not enter PFM until the load reduces further. It should be noted that the net power saving between ideal zero cross detection and the -4mV to +2mV range of the XR75100 is minor. The operating frequency will have changed little from what one would have in the ideal case.

One important feature added to the DCM detection is a counter which allows 8 switching cycles to trigger in the zero cross comparator before enabling DCM operation. This ensures that during large unloading events, the XR75100 will respond quickly. This operation can be seen during the unloading event in Figure 4 in the Typical Performance Characteristics section above.

Programming the On-Time

The On-Time T_{ON} is programmed via resistor RON according to following equation:

$$RON = \frac{V_{IN} \times TON}{3.4 \times 10^{-10}}$$

where TON is calculated from:

$$TON = \frac{V_{OUT}}{V_{IN} \times f}$$

As an example, the calculated TON for the application circuit is 275ns. An RON of 19.4kΩ is required in order to set TON to 275ns. A graph of typical TON versus RON is shown in Figure 7.

Over-Current Protection (OCP)

If load current exceeds the programmed over-current I_{OCP} for four consecutive switching cycles, then the IC enters hiccup mode of operation. In hiccup mode, the MOSFET gates are turned off for 110ms (hiccup timeout). Following the hiccup timeout, a soft-start is attempted. If OCP persists, hiccup timeout will repeat. The IC will remain in hiccup mode until load current is reduced below the programmed I_{OCP}. In order to program over-current protection, use the following equation:

$$RLIM = \frac{(I_{OCP} \times RDS) + 8mV}{ILIM}$$

Where:

RLIM is resistor value for programming I_{OCP}

I_{OCP} is the over-current threshold to be programmed

RDS is the MOSFET rated on resistance

8mV is the OCP comparator offset

ILIM is the internal current that generates the necessary OCP comparator threshold (use 45µA).

Note that ILIM has a positive temperature coefficient of 0.4%/°C. This is meant to roughly match and compensate for the positive temperature coefficient of the synchronous FET RDS. In order for this feature to be effective, the temperature rise of the IC should approximately match the temperature rise of the FET. A graph of typical I_{OCP} versus RLIM is shown in Figure 11.

Short-Circuit Protection (SCP)

If the output voltage drops below 60% of its programmed value, the IC will enter hiccup mode. Hiccup will persist until the short-circuit is removed. The SCP circuit becomes active after PGOOD asserts high.

Over-Temperature (OTP)

OTP triggers at a nominal die temperature of 150°C. The gate of the switching FET and synchronous FET are turned off. When die temperature cools down to 135°C, soft-start is initiated and operation resumes.

Programming the Output Voltage

Use an external voltage divider as shown in the application circuit to program the output voltage V_{OUT}.

$$R1 = R2 \times \left(\frac{V_{OUT}}{0.6} - 1\right)$$

where R2 has a nominal value of 2kΩ.

Programming the Soft-start

Place a capacitor CSS between the SS and GND pins to program the soft-start. In order to program a soft-start time of TSS, calculate the required capacitance CSS from the following equation:

$$CSS = TSS \times \left(\frac{10\mu A}{0.6V}\right)$$

Feed-Forward Capacitor (C_{FF})

A feed - forward capacitor (C_{FF}) may be necessary, depending on the Equivalent Series Resistance (ESR) of C_{OUT}. If only ceramic output capacitors are used for C_{OUT}, then a C_{FF} is necessary. Calculate C_{FF} from:

$$C_{FF} = \frac{1}{2 \times \pi \times R1 \times 7 \times f_{LC}}$$

where:

R1 is the resistor that C_{FF} is placed in parallel with

f_{LC} is the frequency of output filter double-pole

f_{LC} must be less than 11kHz when using a ceramic C_{OUT}. If necessary, increase C_{OUT} and / or L in order to meet this constraint.

When using capacitors with higher ESR, such as PANASONIC TPE series, a C_{FF} is not required provided following conditions are met:

1. The frequency of output filter LC double-pole f_{LC} should be less than 10kHz.

2. The frequency of ESR Zero $f_{Zero,ESR}$ should be at least five times larger than f_{LC}.

Note that if $f_{Zero,ESR}$ is less than $5xf_{LC}$, then it is recommended to set the f_{LC} at less than 2kHz. C_{FF} is still not required.

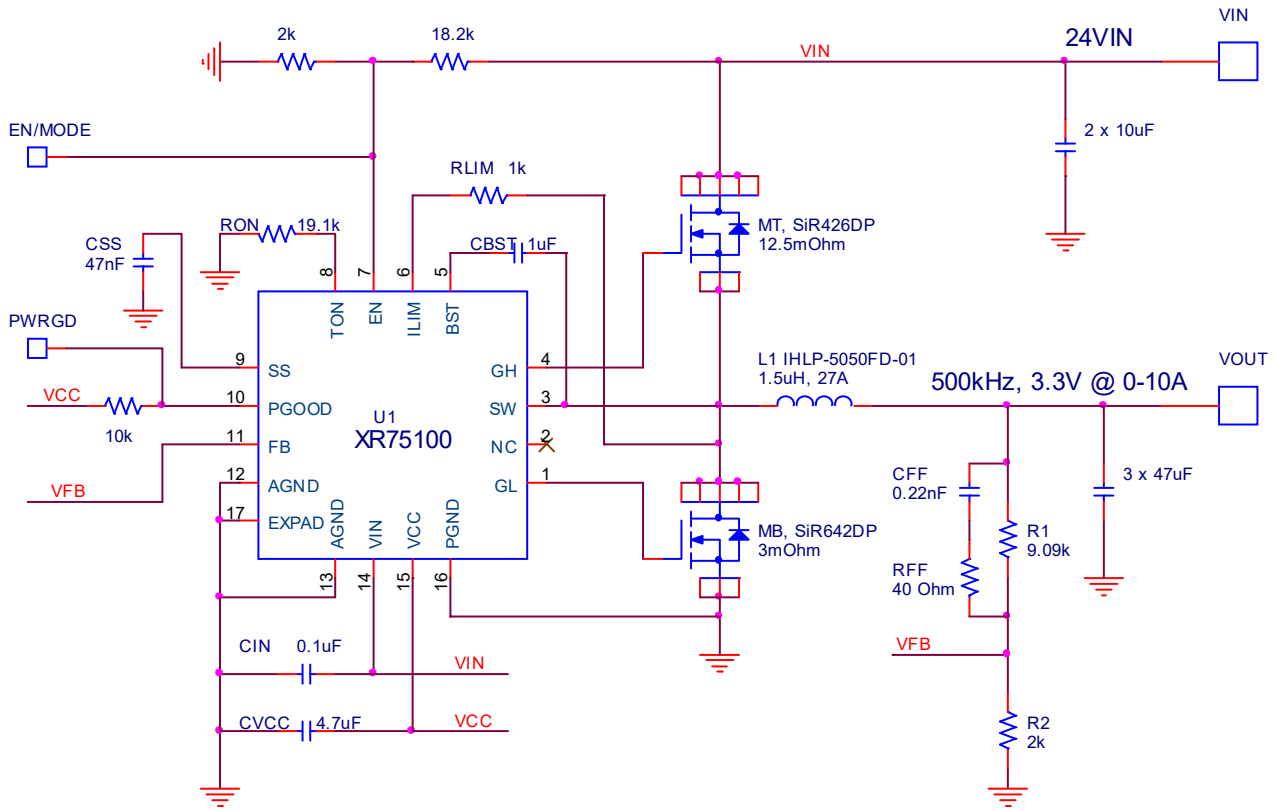
Feed-Forward Resistor (R_{FF})

Poor PCB layout and / or extremely fast switching FETs can cause switching noise at the output and may couple to the FB pin via C_{FF}. Excessive noise at FB will cause poor load regulation. To solve this problem, place a resistor R_{FF} in series with C_{FF}. An R_{FF} value up to 2% of R1 is acceptable.

Maximum Allowable Voltage Ripple at FB pin

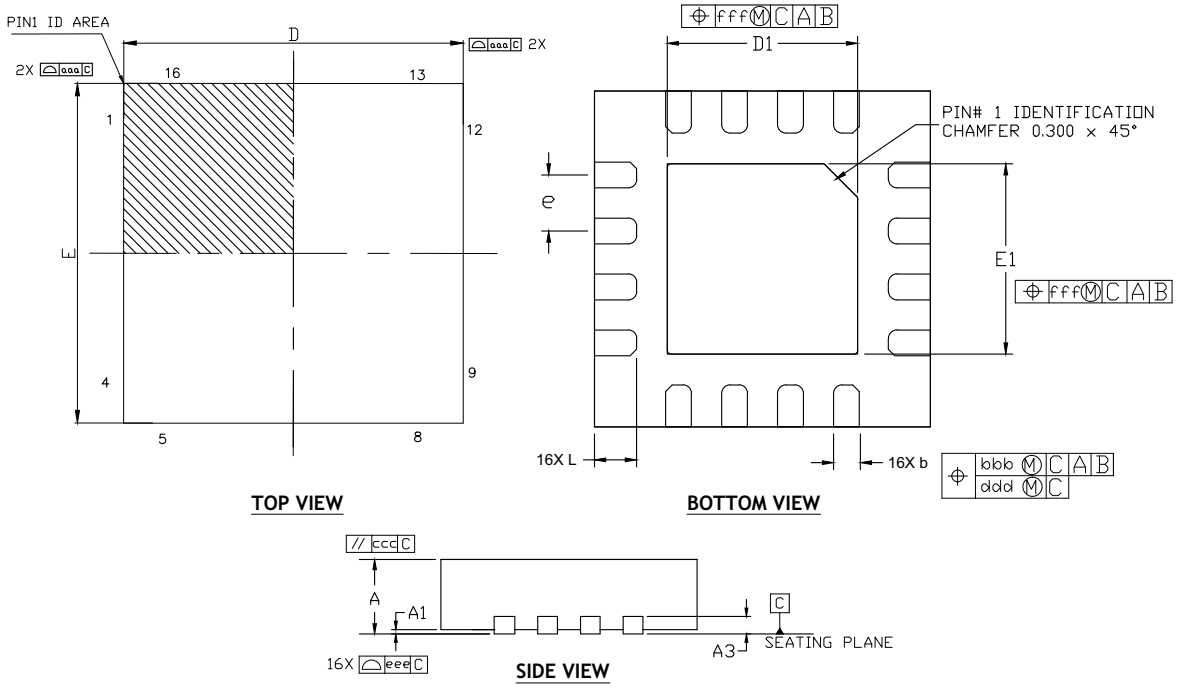
Note that the steady-state voltage ripple at feedback pin FB ($V_{FB,RIPPLE}$) must not exceed 50mV in order for the Module to function correctly. If $V_{FB,RIPPLE}$ is larger than 50mV, then C_{OUT} should be increased as necessary in order to keep the $V_{FB,RIPPLE}$ below 50mV.

Application Circuit



Mechanical Dimensions

16-Pin QFN



DIMENSION TABLE			
SYMBOL	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20Ref	
b	0.18	0.25	0.30
D		3.00 BSC	
E		3.00 BSC	
e		0.50 BSC	
D1	1.50	1.65	1.80
E1	1.50	1.65	1.80
L	0.20	0.30	0.40
K	0.20	–	–
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	
N		16	

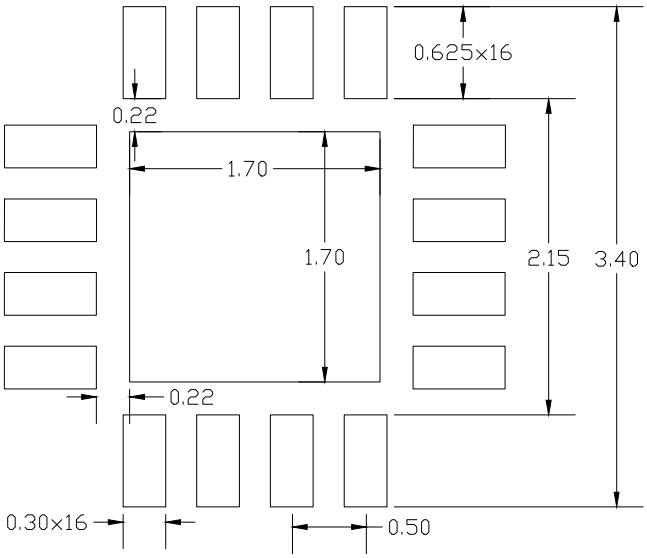
TERMINAL DETAILS

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS AND TOLERANCE PER JEDEC MO-220.

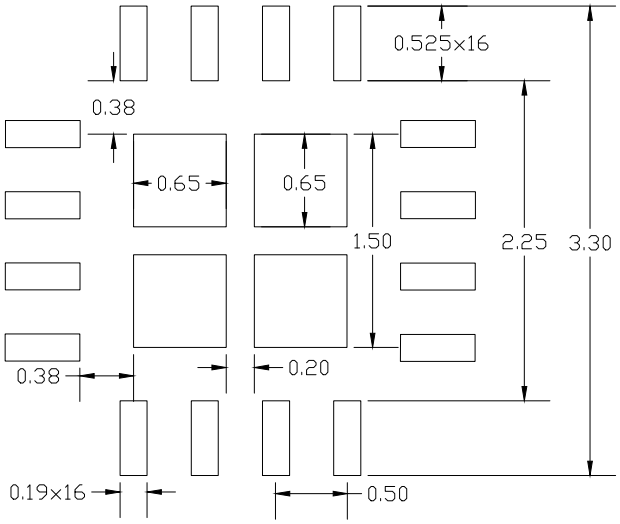
Drawing No.: POD- 00000138

Revision: A

Recommended Land Pattern and Stencil



TYPICAL RECOMMENDED LAND PATTERN



TYPICAL RECOMMENDED STENCIL

Drawing No.: POD- 00000138

Revision: A

Ordering Information[1]

Part Number	Operating Temperature Range	Package	Packaging Method	Lead-Free[2]
XR75100EL-F	-40°C ≤ T_J ≤ +125°C	16-pin QFN 3 x 3	Bulk	Yes
XR75100ELTR-F	-40°C ≤ T_J ≤ +125°C	16-pin QFN 3 x 3	Reel	Yes
XR75100EVB	Evaluation Board			

NOTES:

1. Refer to www.maxlinear.com/XR75100 for most up-to-date Ordering Information

2. Visit www.maxlinear.com for additional information on Environmental Rating.

Revision History

Revision	Date	Description
1A	June 2014	Initial release
1B	March 2015	Modified Functional Block Diagram, Application Circuit, figure 18 and 19. Changed the description of “Selecting the Forced CCM Mode”, “Selecting the DCM/CCM Mode”, “Feed-Forward Capacitor”, Feed-Forward Resistor”, Added “Maximum Allowable Voltage Ripple at FB PIN”.
1C	May 2016	Add limits to zero cross and clarify operating temperature range.
1D	May 2018	Update to MaxLinear logo. Update format and Ordering Information. Added Revision History.
1E	October 2019	Correct block diagram by changing the input gate into the Hiccup Mode from an AND gate to an OR gate. Update ordering information.

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