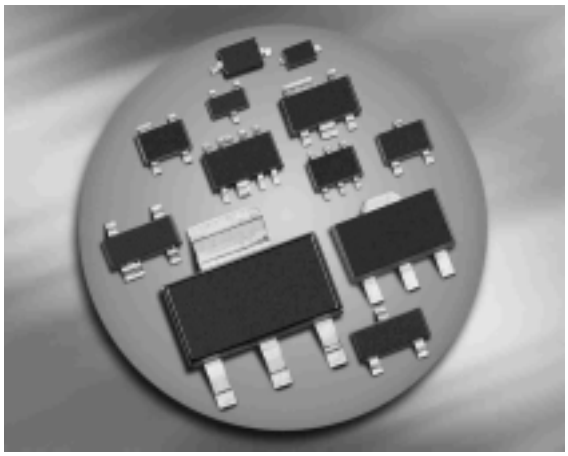
THE DATASHEET OF

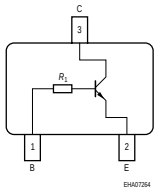
BCR119W E6327

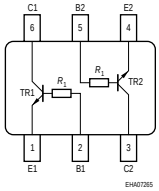
NPN silicon Digital Transistor



- Switching circuit, inverter, interface circuit, driver circuit
- Built in resistor (R_1=4.7 kΩ)
- BCR119S: Two internally isolated transistors with good matching in one multichip package
- BCR119S: For orientation in reel see package information below
- Pb-free (RoHS compliant) package [1)]
- Qualified according AEC Q101

BCR119/F/W **BCR119S**





Type	Marking	Pin Configuration						Package
BCR119	WKs	1=B	2=E	3=C	-	-	-	SOT23
BCR119F	WKs	1=B	2=E	3=C	-	-	-	TSFP-3
BCR119S	WKs	1=E1	2=B1	3=C2	4=E2	5=B2	6=C1	SOT363
BCR119W	WKs	1=B	2=E	3=C	-	-	-	SOT323

[1]Pb-containing package may be available upon special request

Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage	V_{CEO}	50	V
Collector-base voltage	V_{CBO}	50	
Input forward voltage	$V_{i(fwd)}$	30	
Input reverse voltage	$V_{i(rev)}$	5	
DC collector current	I_E	100	mA
Total power dissipation-	P_{tot}		mW
BCR119, $T_S \leq 102°C$		200	
BCR119F, $T_S \leq 128°C$		250	
BCR119S, $T_S \leq 115°C$		250	
BCR119W, $T_S \leq 124°C$		250	
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	-65 ... 150	

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction - soldering point[1)]	R_{thJS}		K/W
BCR119		≤ 240	
BCR119F		≤ 90	
BCR119S		≤ 140	
BCR119W		≤ 105	

[1]For calculation of R_{thJA} please refer to Application Note Thermal Resistance

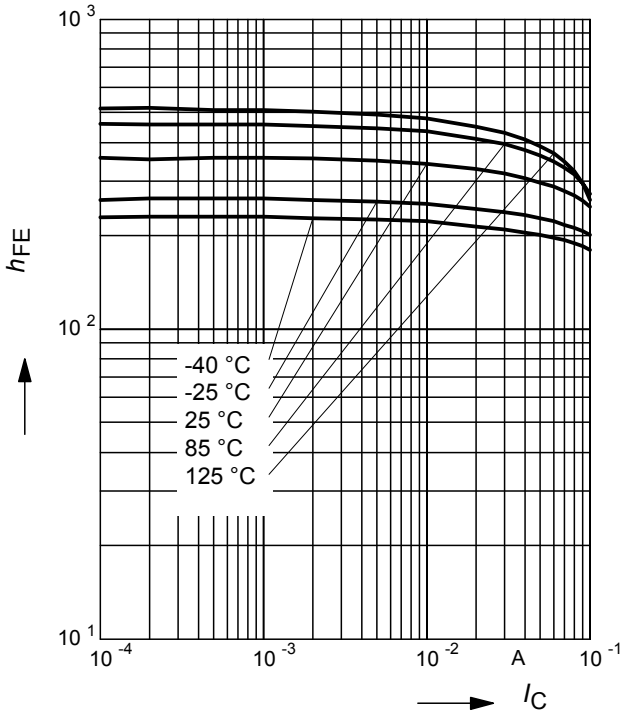
Electrical Characteristics at T_A = 25°C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics					
Collector-emitter breakdown voltage I_C = 100 µA, I_B = 0	$V_{(BR)CEO}$	50	-	-	V
Collector-base breakdown voltage I_C = 10 µA, I_E = 0	$V_{(BR)CBO}$	50	-	-	
Collector-base cutoff current V_{CB} = 40 V, I_E = 0	I_{CBO}	-	-	100	nA
Emitter-base cutoff current V_{EB} = 5 V, I_C = 0	I_{EBO}	-	-	100	nA
DC current gain[1)] I_C = 5 mA, V_{CE} = 5 V	h_{FE}	120	-	630	-
Collector-emitter saturation voltage[1)] I_C = 10 mA, I_B = 0.5 mA	V_{CEsat}	-	-	0.3	V
Input off voltage I_C = 100 µA, V_{CE} = 5 V	$V_{i(off)}$	0.4	-	0.8	
Input on voltage I_C = 2 mA, V_{CE} = 0.3 V	$V_{i(on)}$	0.5	-	1.1	
Input resistor	R_1	3.2	4.7	6.2	kΩ
AC Characteristics					
Transition frequency I_C = 10 mA, V_{CE} = 5 V, f = 100 MHz	f_T	-	150	-	MHz
Collector-base capacitance V_{CB} = 10 V, f = 1 MHz	C_{cb}	-	3	-	pF

[1]Pulse test: t < 300µs; D < 2%

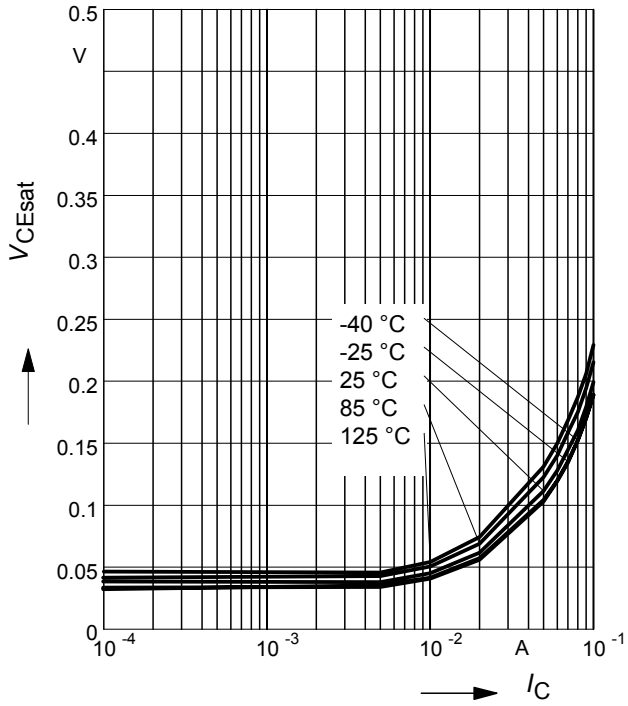
DC current gain $h_{FE} = f(I_C)$

V_{CE} = 5V (common emitter configuration)



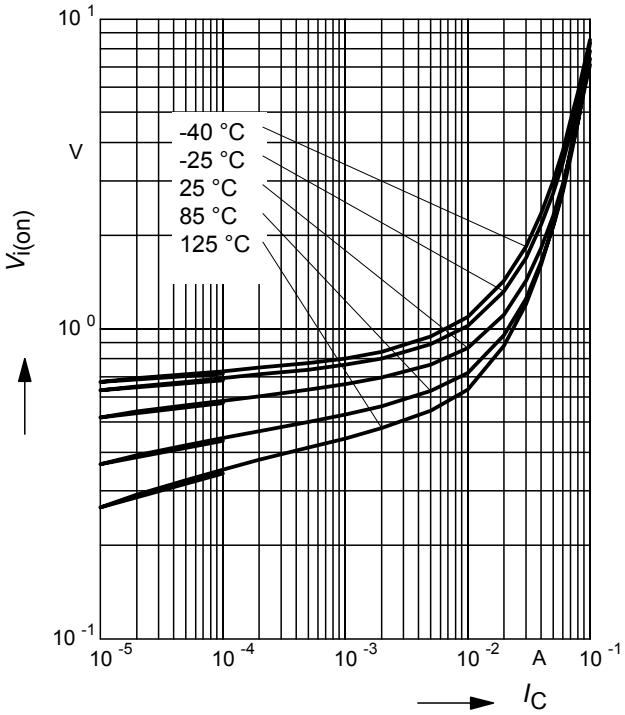
Collector-emitter saturation voltage

$V_{CEsat} = f(I_C)$, I_C/I_B = 20



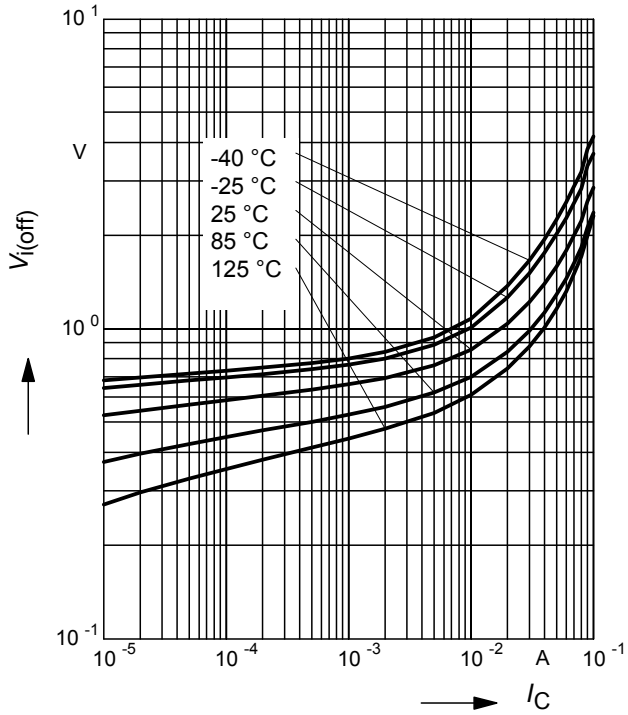
Input on Voltage $V_{i(on)} = f(I_C)$

V_{CE} = 0.3V (common emitter configuration)

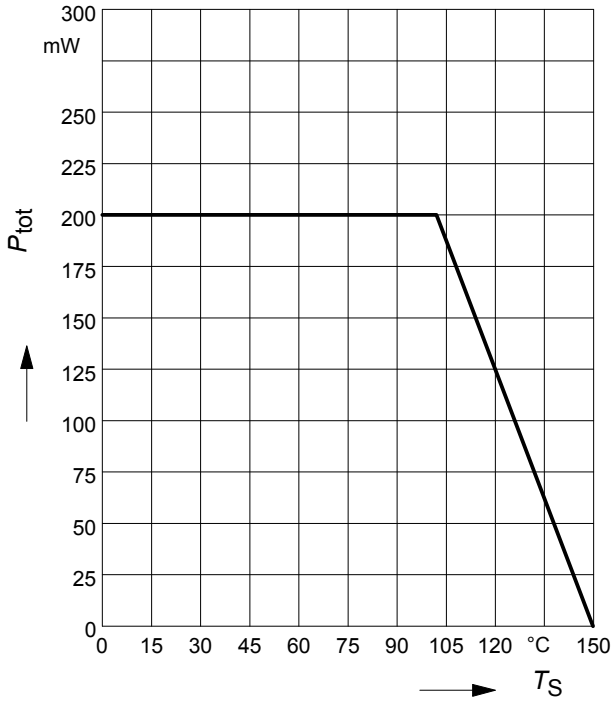


Input off voltage $V_{i(off)} = f(I_C)$

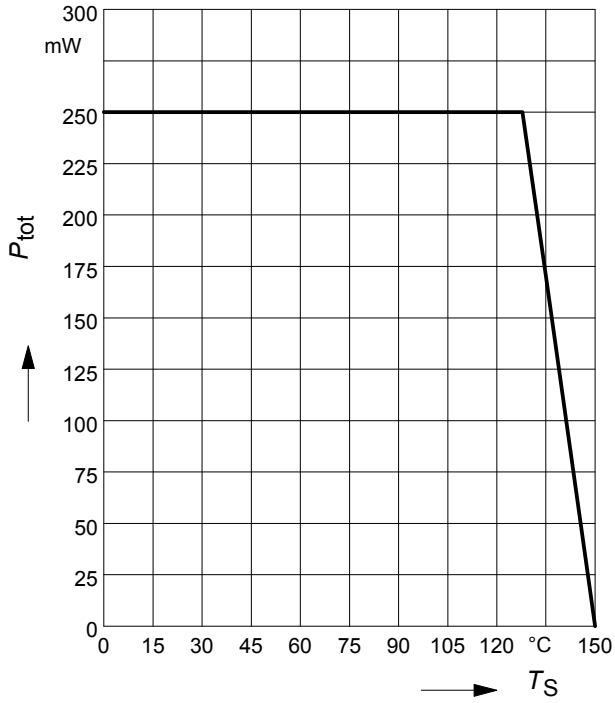
V_{CE} = 5V (common emitter configuration)



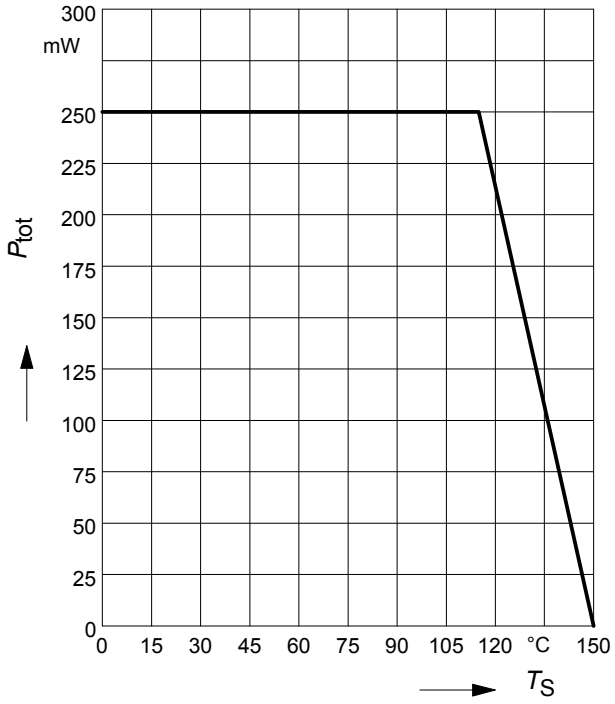
Total power dissipation $P_{tot} = f(T_S)$
BCR119



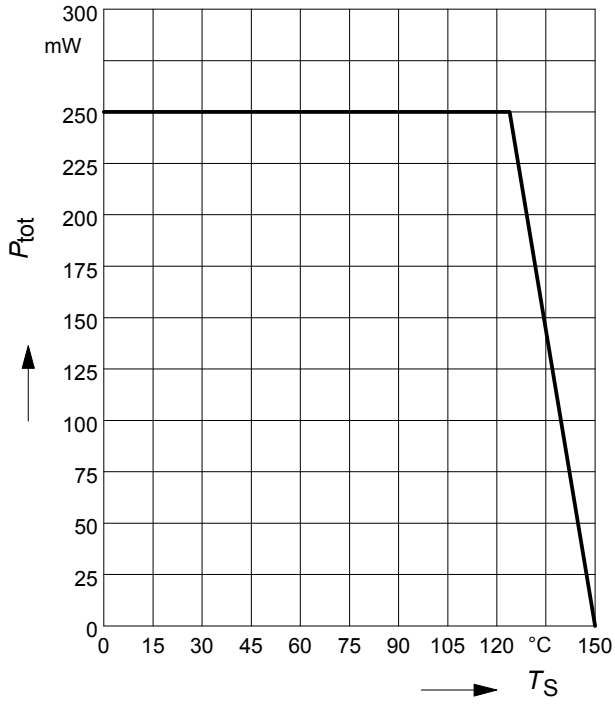
Total power dissipation $P_{tot} = f(T_S)$
BCR119F



Total power dissipation $P_{tot} = f(T_S)$
BCR119S

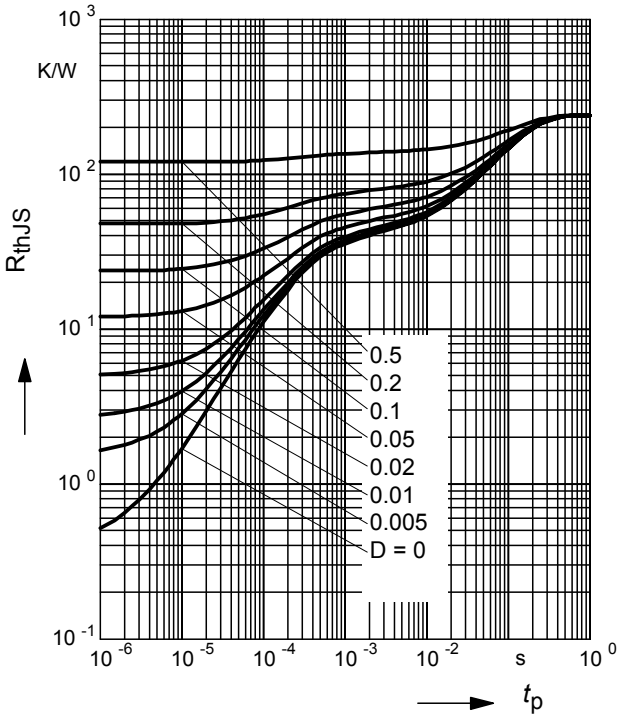


Total power dissipation $P_{tot} = f(T_S)$
BCR119W



Permissible Pulse Load $R_{thJS} = f(t_p)$

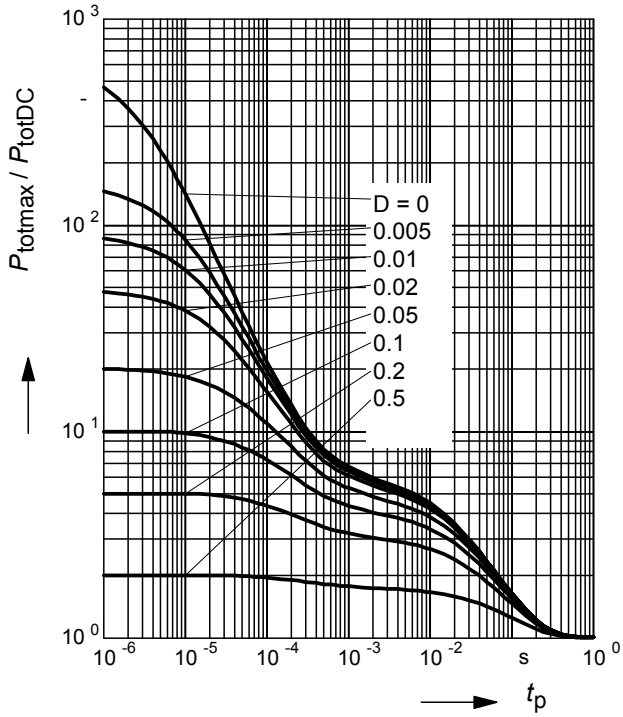
BCR119



Permissible Pulse Load

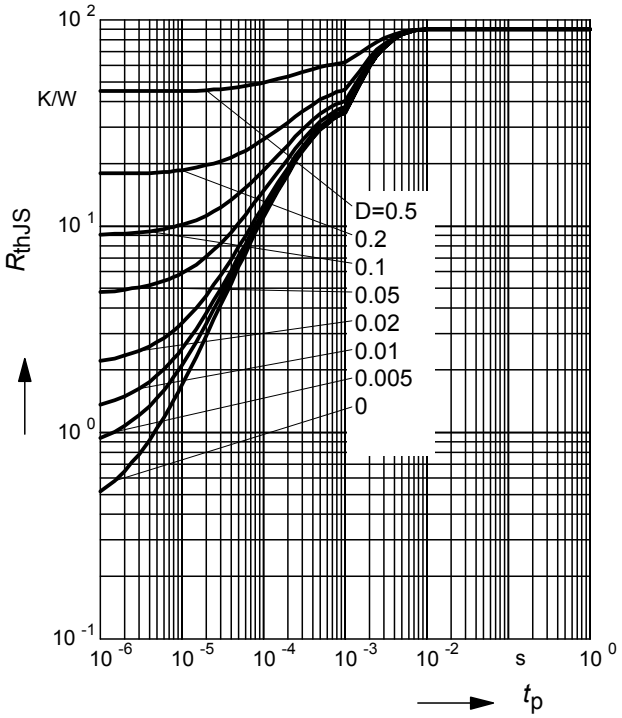
$P_{totmax}/P_{totDC} = f(t_p)$

BCR119



Permissible Puls Load $R_{thJS} = f(t_p)$

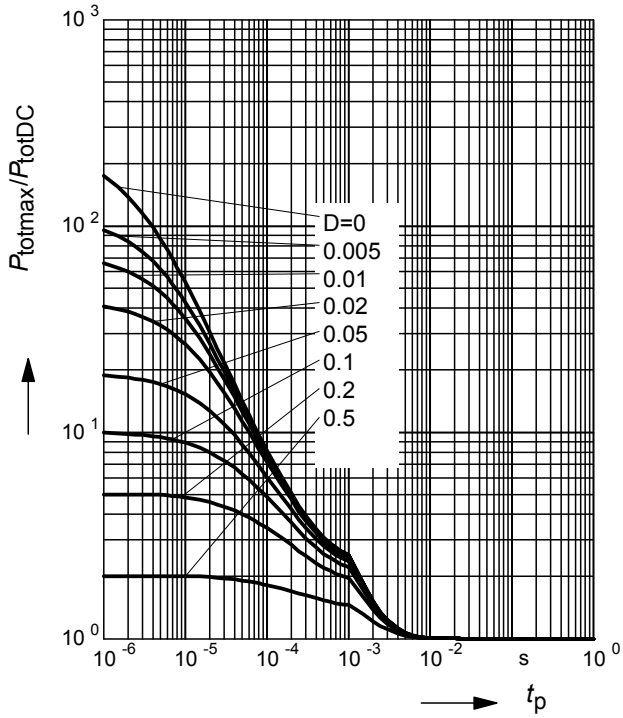
BCR119F



Permissible Pulse Load

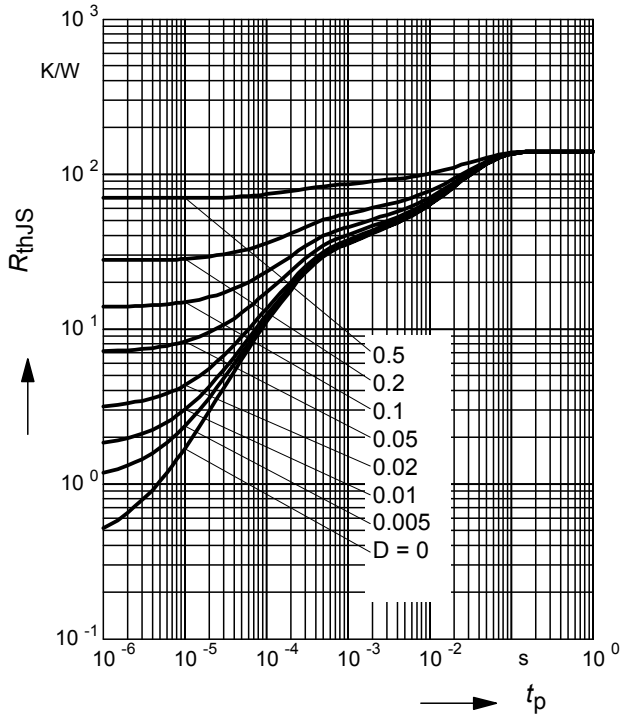
$P_{totmax}/P_{totDC} = f(t_p)$

BCR119F



Permissible Puls Load $R_{thJS} = f(t_p)$

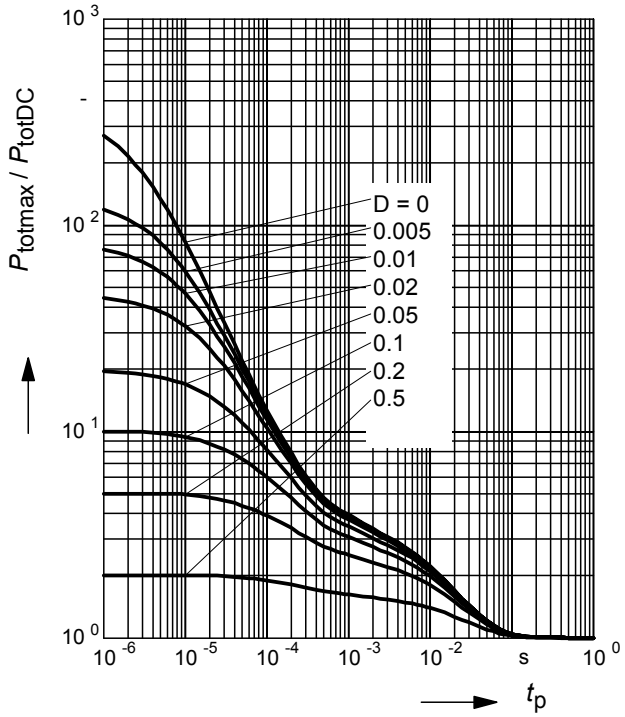
BCR119S



Permissible Pulse Load

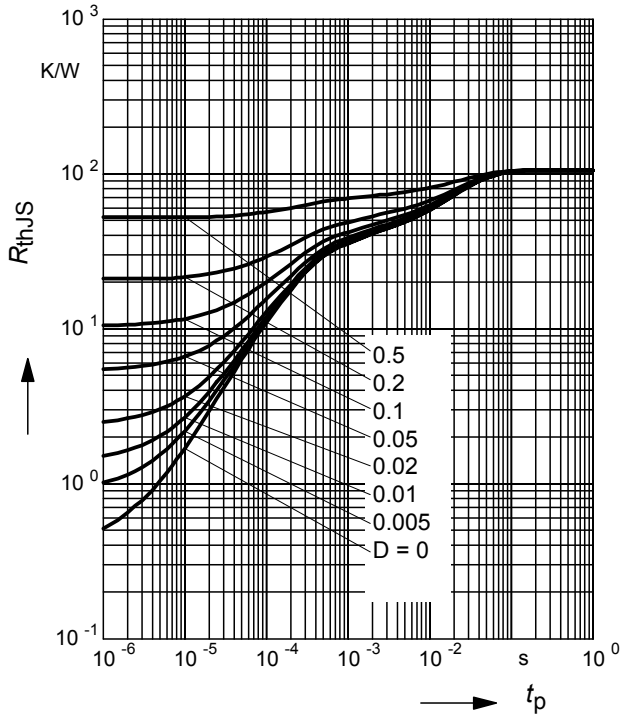
$P_{totmax}/P_{totDC} = f(t_p)$

BCR119S



Permissible Puls Load $R_{thJS} = f(t_p)$

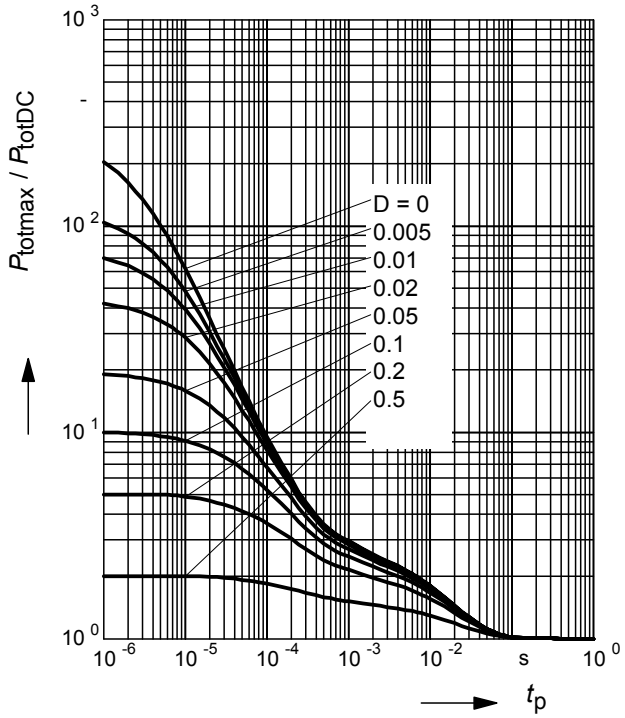
BCR119W



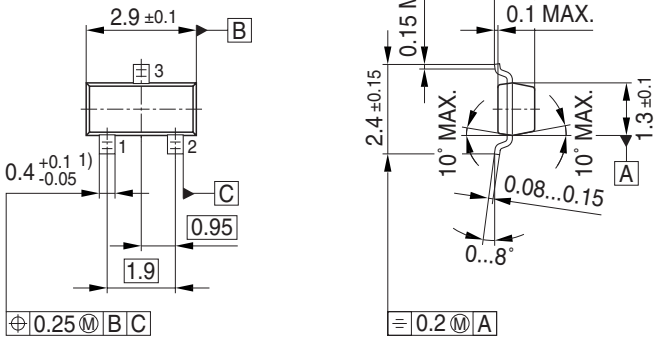
Permissible Pulse Load

$P_{totmax}/P_{totDC} = f(t_p)$

BCR119W

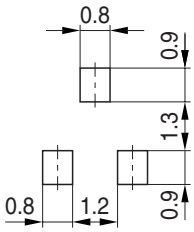


Package Outline

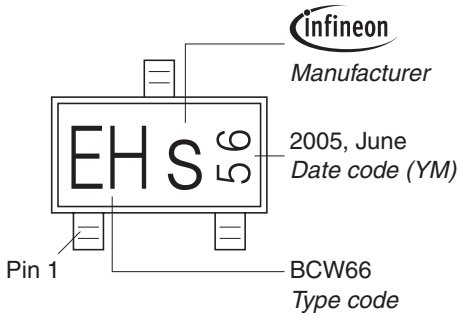


1) Lead width can be 0.6 max. in dambar area

Foot Print

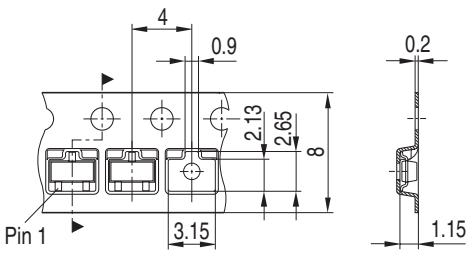


Marking Layout (Example)

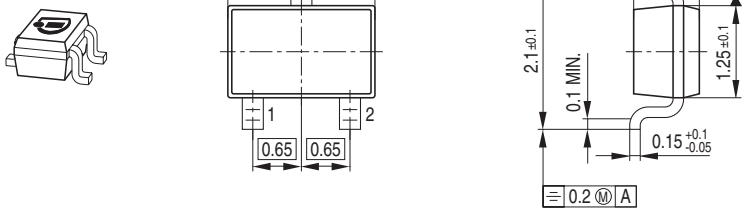


Standard Packing

Reel ø180 mm = 3.000 Pieces/Reel
Reel ø330 mm = 10.000 Pieces/Reel



Package Outline



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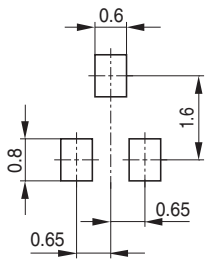
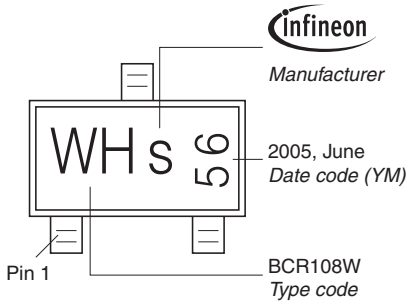


Marking Layout (Example)



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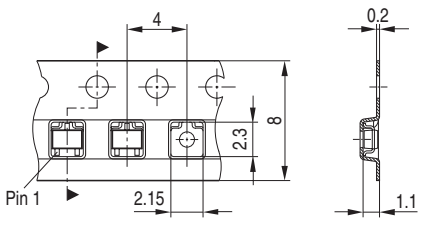

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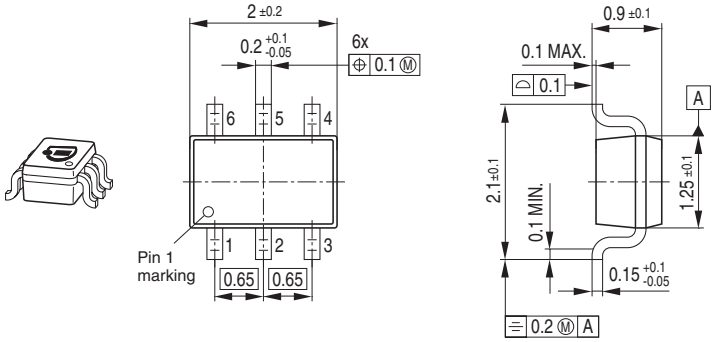

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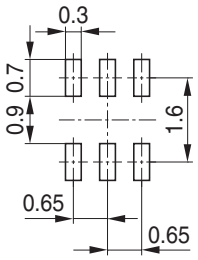
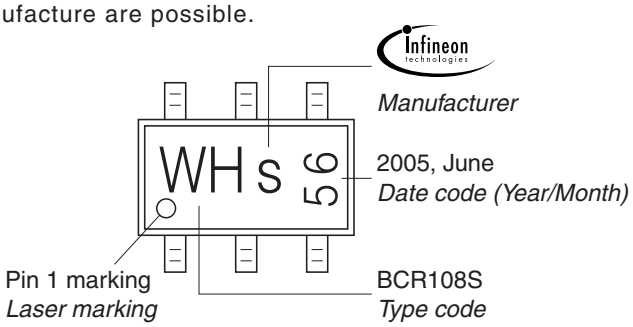


Marking Layout (Example)

Small variations in positioning of
Date code, Type code and Manufacture are possible.



Standard Packing

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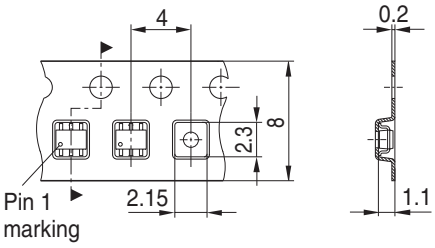
For symmetric types no defined Pin 1 orientation in reel.



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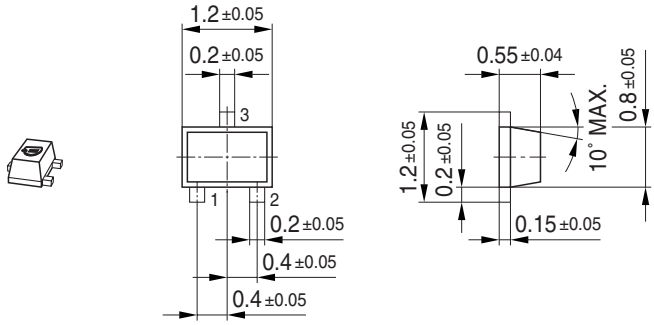

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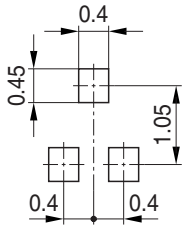
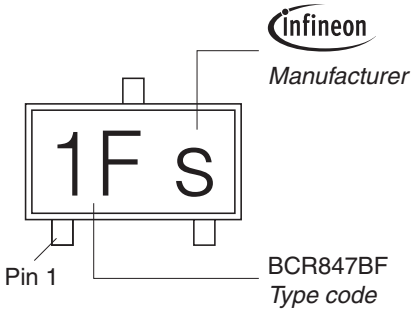


Marking Layout (Example)



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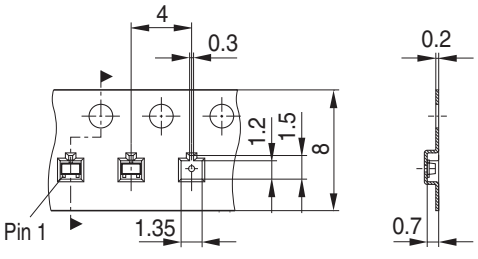

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