



**THE DATASHEET OF
74FCT162245ATPVG8**



FEATURES:

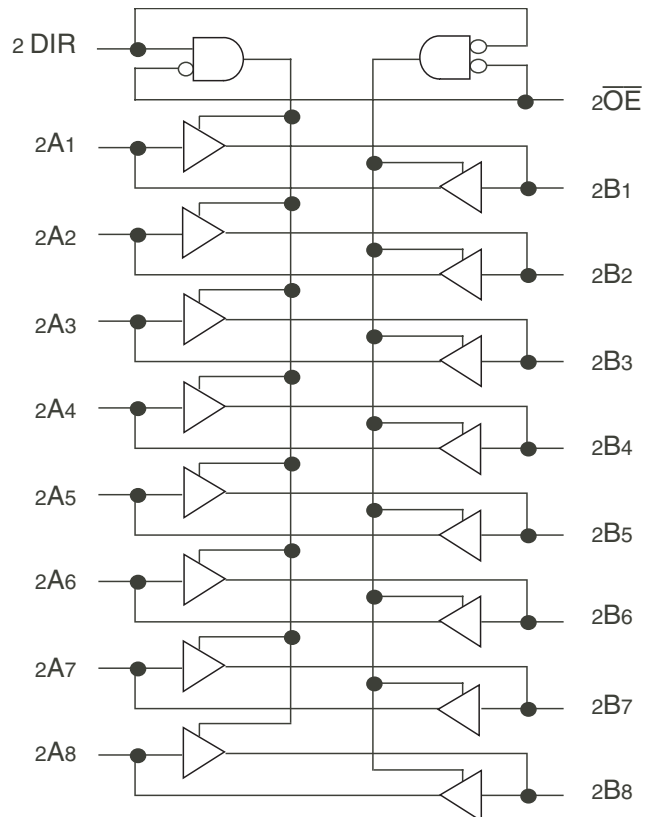
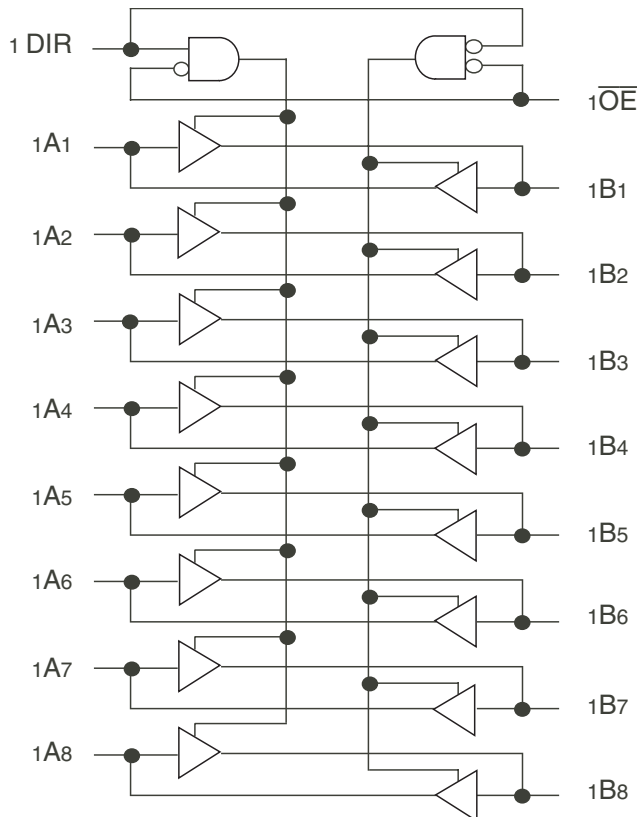
- 0.5 MICRON CMOS Technology
- High-speed, low-power CMOS replacement for ABT functions
- Typical $t_{sk(o)}$ (Output Skew) < 250ps
- Low input and output leakage $\leq 1\mu A$ (max.)
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- **Balanced Output Drivers:**
 - $\pm 24mA$ (industrial)
 - $\pm 16mA$ (military)
- Reduced system switching noise
- Typical V_{OLP} (Output Ground Bounce) < 0.6V at $V_{CC} = 5V$, $T_A = 25^\circ C$
- Available in the following packages:
 - Industrial: SSOP, TSSOP
 - Military: CERPACK

DESCRIPTION:

The FCT162245T 16-bit transceiver is built using advanced dual metal CMOS technology. These high-speed, low-power transceivers are ideal for synchronous communication between two buses (A and B). The Direction and Output Enable controls operate these devices as either two independent 8-bit transceivers or one 16-bit transceiver. The direction control pin (\overline{xDIR}) controls the direction of data flow. The output enable pin (\overline{xOE}) overrides the direction control and disables both ports. All inputs are designed with hysteresis for improved noise margin.

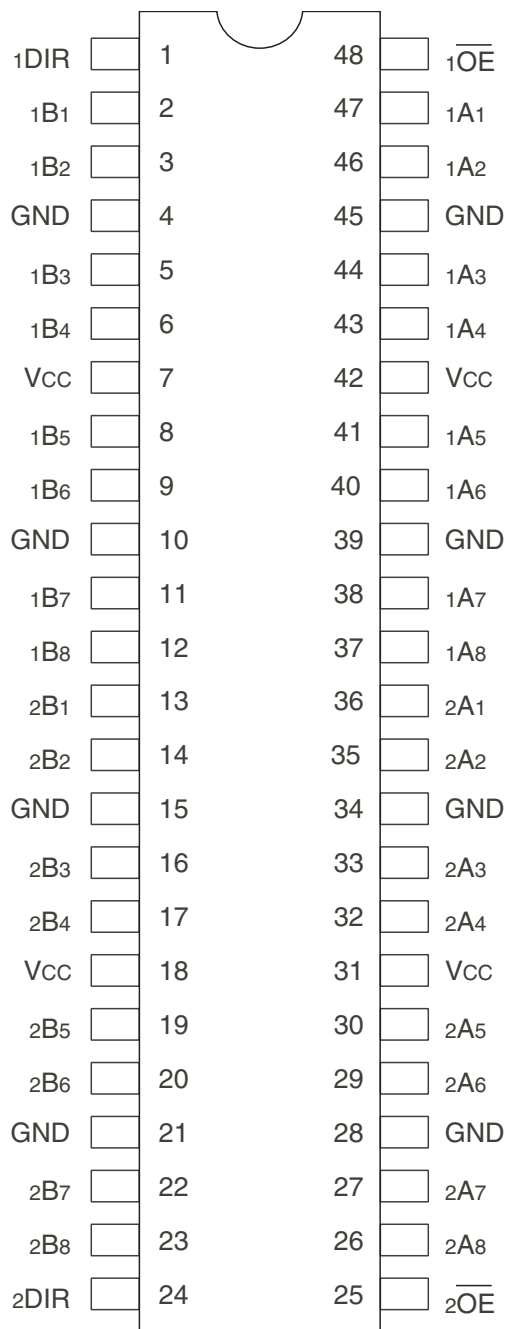
The FCT162245T has balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times—reducing the need for external series terminating resistors. The FCT162245T is a plug-in replacement for the FCT16245T and ABT16245 for on-board interface applications.

FUNCTIONAL BLOCK DIAGRAM



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PIN CONFIGURATION



SSOP/ TSSOP/ CERPACK
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Description | Max | Unit |
|----------------------------------|--------------------------------------|------------------------------|------|
| V _{TERM} ⁽²⁾ | Terminal Voltage with Respect to GND | -0.5 to +7 | V |
| V _{TERM} ⁽³⁾ | Terminal Voltage with Respect to GND | -0.5 to V _{CC} +0.5 | V |
| T _{STG} | Storage Temperature | -65 to +150 | °C |
| I _{OUT} | DC Output Current | -60 to +120 | mA |

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXXT AND FCT166XXXT (A-Port) Output and I/O terminals.
- Output and I/O terminals for FCT162XXXT AND FCT166XXXT (A-Port).

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

| Symbol | Parameter ⁽¹⁾ | Conditions | Typ. | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 3.5 | 6 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0V | 3.5 | 8 | pF |

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

| Pin Names | Description |
|-------------------|-----------------------------------|
| x \overline{OE} | Output Enable Inputs (Active LOW) |
| xDIR | Direction Control Input |
| xAx | Side A Inputs or 3-State Outputs |
| xBx | Side B Inputs or 3-State Outputs |

FUNCTION TABLE⁽¹⁾

| Inputs | | Outputs |
|-------------------|------|---------------------|
| x \overline{OE} | xDIR | |
| L | L | Bus B Data to Bus A |
| L | H | Bus A Data to Bus B |
| H | X | High Z State |

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$; Military: $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

| Symbol | Parameter | Test Conditions ⁽¹⁾ | | Min. | Typ. ⁽²⁾ | Max. | Unit |
|-------------------------------------|---|--|---------------------|------|---------------------|---------|---------------|
| V_{IH} | Input HIGH Level | Guaranteed Logic HIGH Level | | 2 | — | — | V |
| V_{IL} | Input LOW Level | Guaranteed Logic LOW Level | | — | — | 0.8 | V |
| I_{IH} | Input HIGH Current (Input pins) ⁽⁵⁾ | $V_{CC} = \text{Max.}$ | $V_I = V_{CC}$ | — | — | ± 1 | μA |
| | Input HIGH Current (I/O pins) ⁽⁵⁾ | | | — | — | ± 1 | |
| I_{IL} | Input LOW Current (Input pins) ⁽⁵⁾ | | $V_I = \text{GND}$ | — | — | ± 1 | |
| | Input LOW Current (I/O pins) ⁽⁵⁾ | | | — | — | ± 1 | |
| I_{OZH} | High Impedance Output Current (3-State Output pins) ⁽⁵⁾ | $V_{CC} = \text{Max.}$ | $V_O = 2.7\text{V}$ | — | — | ± 1 | μA |
| I_{OZL} | | | $V_O = 0.5\text{V}$ | — | — | ± 1 | |
| V_{IK} | Clamp Diode Voltage | $V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$ | | — | -0.7 | -1.2 | V |
| I_{OS} | Short Circuit Current | $V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$ | | -80 | -140 | -250 | mA |
| V_H | Input Hysteresis | — | | — | 100 | — | mV |
| I_{CCL} I_{CCH} I_{CCZ} | Quiescent Power Supply Current | $V_{CC} = \text{Max.}$ $V_{IN} = \text{GND or } V_{CC}$ | | — | 5 | 500 | μA |

OUTPUT DRIVE CHARACTERISTICS

| Symbol | Parameter | Test Conditions ⁽¹⁾ | | Min. | Typ. ⁽²⁾ | Max. | Unit |
|-----------|---------------------|---|--|------|---------------------|------|------|
| I_{ODL} | Output LOW Current | $V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_O = 1.5\text{V}^{(3)}$ | | 60 | 115 | 200 | mA |
| I_{ODH} | Output HIGH Current | $V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_O = 1.5\text{V}^{(3)}$ | | -60 | -115 | -200 | mA |
| V_{OH} | Output HIGH Voltage | $V_{CC} = \text{Min}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$ | $I_{OH} = -16\text{mA MIL}$ $I_{OH} = -24\text{mA IND}$ | 2.4 | 3.3 | — | V |
| V_{OL} | Output LOW Voltage | $V_{CC} = \text{Min}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$ | $I_{OH} = 16\text{mA MIL}$ $I_{OH} = 24\text{mA IND}$ | — | 0.3 | 0.55 | V |

NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- Duration of the condition can not exceed one second.
- This test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^{\circ}\text{C}$.

POWER SUPPLY CHARACTERISTICS

| Symbol | Parameter | Test Conditions ⁽¹⁾ | | Min. | Typ. ⁽²⁾ | Max. | Unit |
|-----------------|---|--|--|------|---------------------|---------------------|--------------------------|
| ΔI_{CC} | Quiescent Power Supply Current TTL Inputs HIGH | $V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$ | | — | 0.5 | 1.5 | mA |
| I_{CCD} | Dynamic Power Supply Current ⁽⁴⁾ | $V_{CC} = \text{Max.}$ Outputs Open $\overline{xOE} = xDIR = \text{GND}$ One Input Toggling 50% Duty Cycle | $V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$ | — | 60 | 100 | $\mu\text{A}/\text{MHz}$ |
| I_C | Total Power Supply Current ⁽⁶⁾ | $V_{CC} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{xOE} = xDIR = \text{GND}$ One Bits Toggling | $V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$ | — | 0.6 | 1.5 | mA |
| | | | $V_{IN} = 3.4V$ $V_{IN} = \text{GND}$ | — | 0.9 | 2.3 | |
| | | $V_{CC} = \text{Max.}$ Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle $\overline{xOE} = xDIR = \text{GND}$ Sixteen Bits Toggling | $V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$ | — | 2.4 | 4.5 ⁽⁵⁾ | |
| | | | $V_{IN} = 3.4V$ $V_{IN} = \text{GND}$ | — | 6.4 | 16.5 ⁽⁵⁾ | |

NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, +25°C ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} \cdot DH_{NT} + I_{CCD} (f_{CP}N_{CP}/2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ})$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (} V_{IN} = 3.4V)$
 $DH = \text{Duty Cycle for TTL Inputs High}$
 $NT = \text{Number of TTL Inputs at } DH$
 $I_{CCD} = \text{Dynamic Current caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

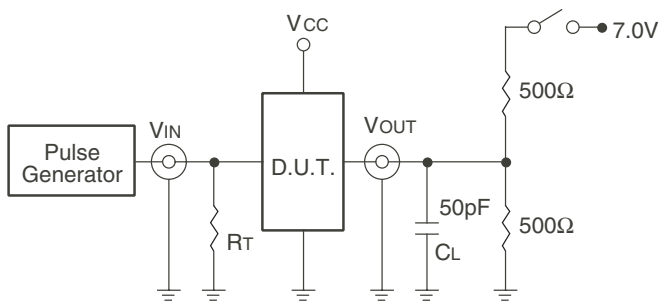
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

| Symbol | Parameter | Condition ⁽¹⁾ | 54FCT162445T | | 54/74FCT162245AT | | | | 54/74FCT162245CT | | | | Unit |
|-------------|---------------------------------|--|---------------------|------|---------------------|------|---------------------|------|---------------------|------|---------------------|------|------|
| | | | Mil. | | Ind. | | Mil. | | Ind. | | Mil. | | |
| | | | Min. ⁽²⁾ | Max. | Min. ⁽²⁾ | Max. | Min. ⁽²⁾ | Max. | Min. ⁽²⁾ | Max. | Min. ⁽²⁾ | Max. | |
| t_{PLH} | Propagation Delay | $C_L = 50\text{pF}$ $R_L = 500\Omega$ | 1.5 | 7.5 | 1.5 | 4.6 | 1.5 | 4.9 | 1.5 | 3.5 | 1.5 | 4.5 | ns |
| t_{PHL} | A to B, B to A | | | | | | | | | | | | |
| t_{PZH} | Output Enable Time | | 1.5 | 10 | 1.5 | 6.2 | 1.5 | 6.5 | 1.5 | 4.4 | 1.5 | 6.2 | ns |
| t_{PZL} | \overline{xOE} to A or B | | | | | | | | | | | | |
| t_{PHZ} | Output Disable Time | | 1.5 | 10 | 1.5 | 5 | 1.5 | 6 | 1.5 | 4 | 1.5 | 5.2 | ns |
| t_{PLZ} | \overline{xOE} to A or B | | | | | | | | | | | | |
| t_{PZH} | Output Enable Time | | 1.5 | 10 | 1.5 | 6.2 | 1.5 | 6.5 | 1.5 | 4.8 | 1.5 | 6.2 | ns |
| t_{PZL} | $xDIR$ to A or B ⁽⁴⁾ | | | | | | | | | | | | |
| t_{PHZ} | Output Disable Time | 1.5 | 10 | 1.5 | 5 | 1.5 | 6 | 1.5 | 4 | 1.5 | 5.2 | ns | |
| t_{PLZ} | $xDIR$ to A or B ⁽⁴⁾ | | | | | | | | | | | | |
| $t_{SK(o)}$ | Output Skew ⁽³⁾ | | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | — | 0.5 | ns |

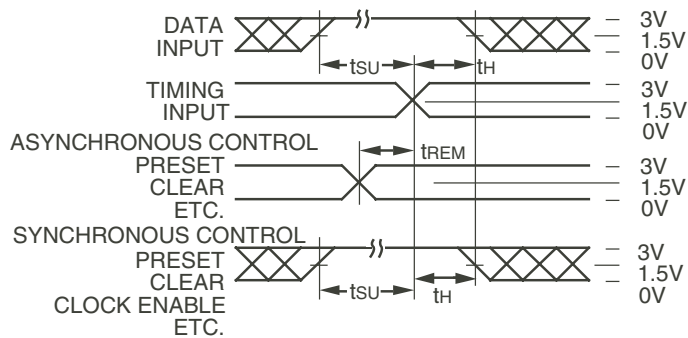
NOTES:

- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
- This parameter is guaranteed but not tested.

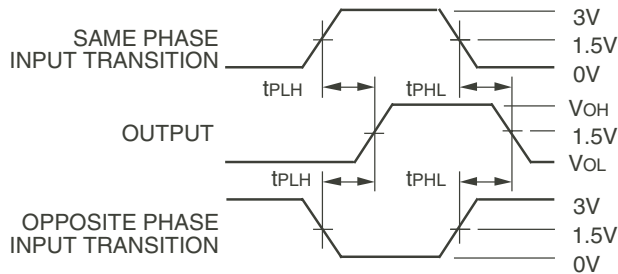
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Waveforms



Set-up, Hold, and Release Times



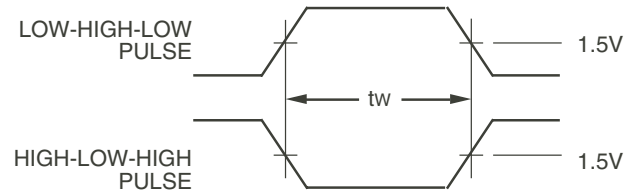
Propagation Delay

SWITCH POSITION

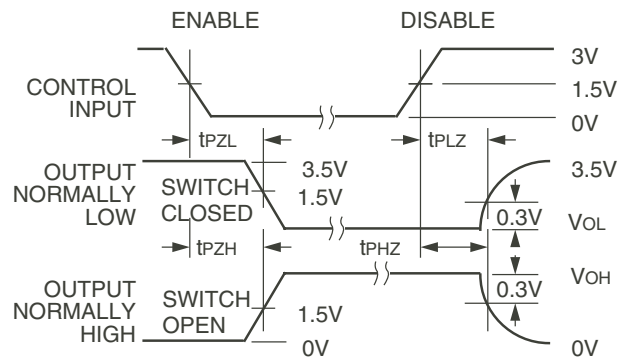
| Test | Switch |
|---|--------|
| Open Drain Disable Low Enable Low | Closed |
| All Other Tests | Open |

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to Zout of the Pulse Generator.



Pulse Width

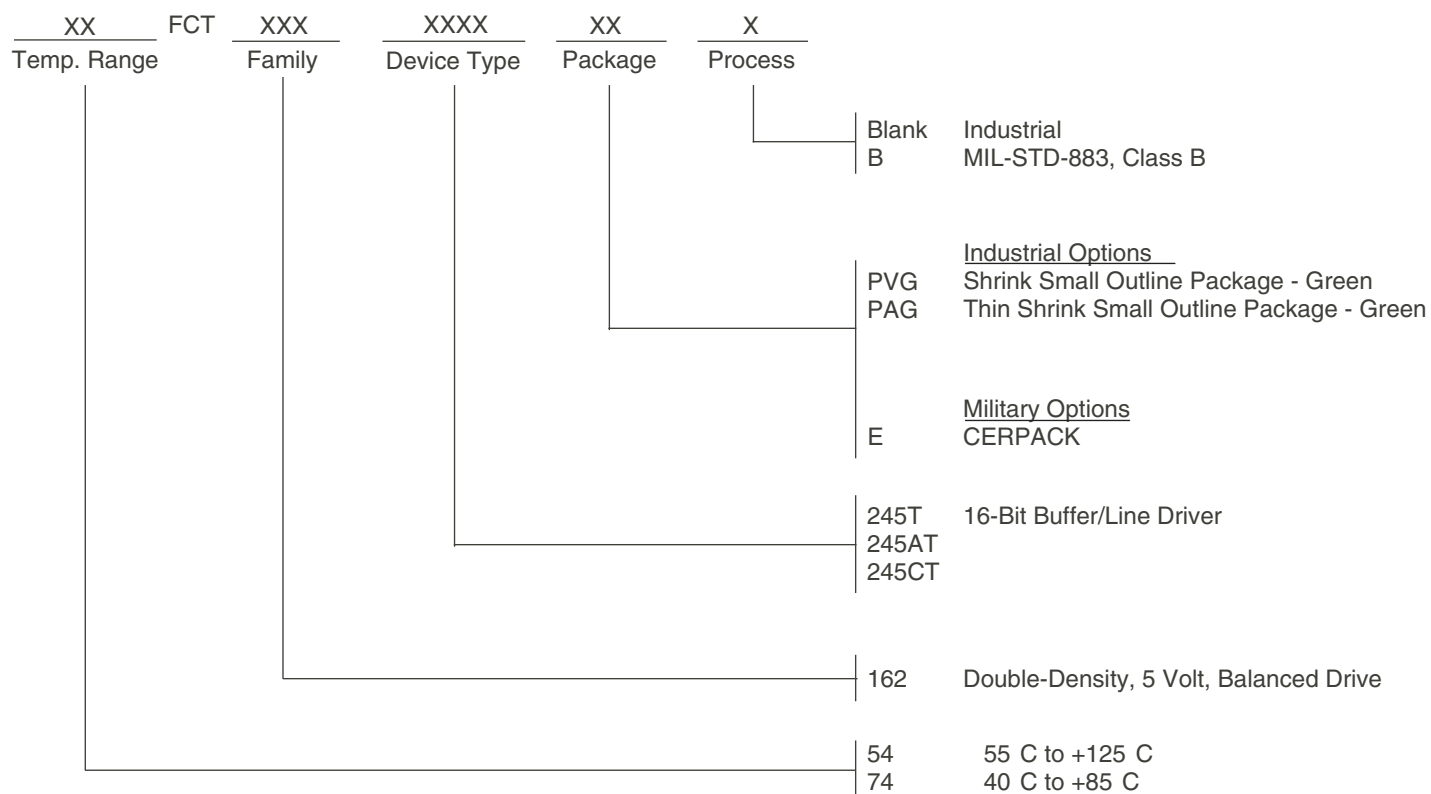


Enable and Disable Times

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$.

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