



**THE DATASHEET OF
74FCT3244SOG**



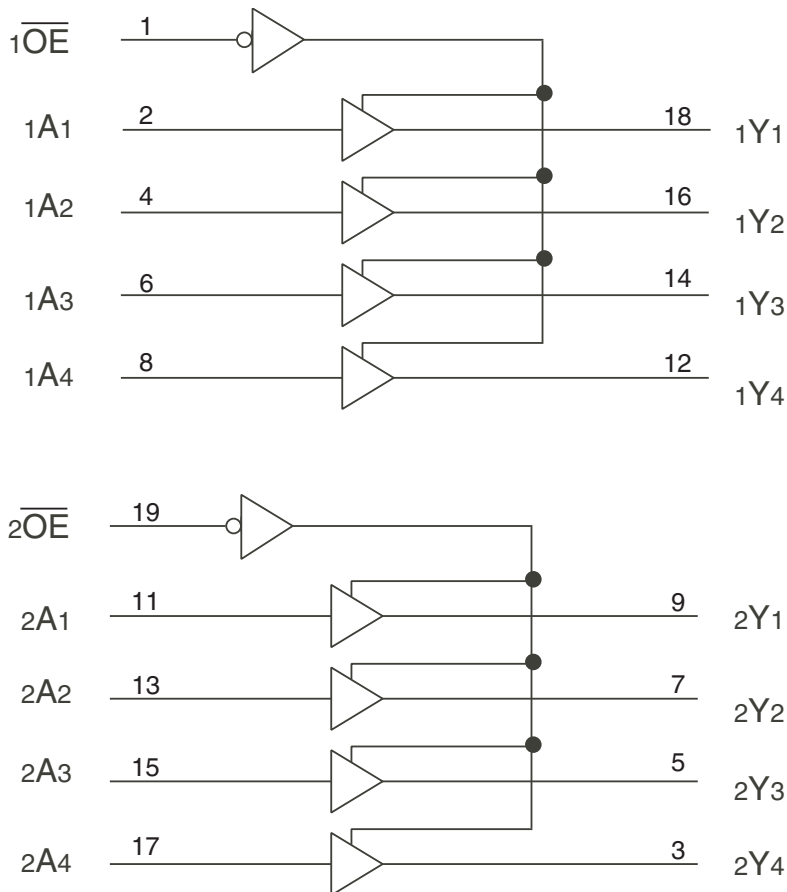
FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range
- $V_{CC} = 2.7V$ to $3.6V$, Extended Range
- CMOS power levels ($0.4\mu W$ typ. static)
- Rail-to-Rail output swing for increased noise margin
- Available in QSOP, SOIC, SSOP, and TSSOP packages

DESCRIPTION:

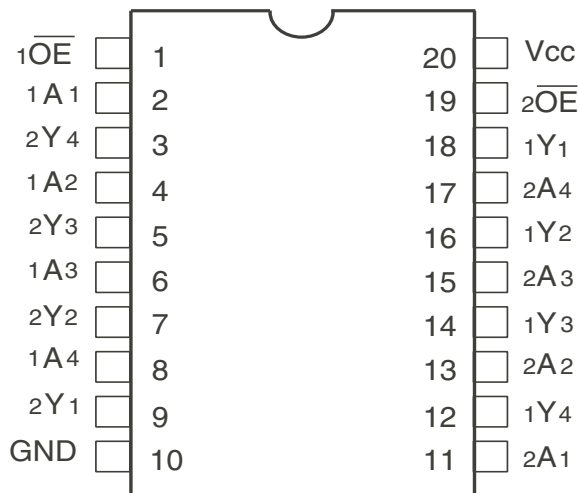
The FCT3244/A octal buffer/line drivers are built using advanced dual metal CMOS technology. These high-speed, low-power buffers are designed to be used as memory data and address drivers, clock drivers, and bus-oriented transmitter/receivers. The three-state controls are designed to operate these devices in a dual-nibble or single-byte mode. All inputs are designed with hysteresis for improved noise margin.

FUNCTIONAL BLOCK DIAGRAM



INDUSTRIAL TEMPERATURE RANGE

PIN CONFIGURATION



TOP VIEW

| Package Type | Package Code | Order Code |
|--------------|--------------|------------|
| QSOP | PCG20 | QG |
| SOIC | PSG20 | SOG |
| TSSOP | PGG20 | PGG |
| SSOP | PYG20 | PYG |

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Description | Max | Unit |
|----------------------|--------------------------------------|------------------------------|------|
| VTERM ⁽²⁾ | Terminal Voltage with Respect to GND | -0.5 to +4.6 | V |
| VTERM ⁽³⁾ | Terminal Voltage with Respect to GND | -0.5 to +7 | V |
| VTERM ⁽⁴⁾ | Terminal Voltage with Respect to GND | -0.5 to V _{CC} +0.5 | V |
| TSTG | Storage Temperature | -65 to +150 | °C |
| I _{OUT} | DC Output Current | -60 to +60 | mA |

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- Input terminals.
- Outputs and I/O terminals.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

| Symbol | Parameter ⁽¹⁾ | Conditions | Typ. | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 3.5 | 6 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0V | 4 | 8 | pF |

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

| Pin Names | Description |
|-------------------|---|
| x \overline{OE} | 3-State Output Enable Inputs (Active LOW) |
| xAx | Data Inputs |
| xYx | 3-State Outputs |

FUNCTION TABLE⁽¹⁾

| Inputs | | Outputs |
|-------------------|-----|---------|
| x \overline{OE} | xAx | xYx |
| L | L | L |
| L | H | H |
| H | X | Z |

NOTE:

- H = HIGH Voltage Level
X = Don't Care
L = LOW Voltage Level
Z = High Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 2.7\text{V}$ to 3.6V

| Symbol | Parameter | Test Conditions ⁽¹⁾ | | Min. | Typ. ⁽²⁾ | Max. | Unit |
|--|--|---|----------------------------------|----------------------|---------------------|----------------------|------|
| V _{IH} | Input HIGH Level (Input pins) | Guaranteed Logic HIGH Level | | 2 | — | 5.5 | V |
| | Input HIGH Level (I/O pins) | | | 2 | — | V _{CC} +0.5 | |
| V _{IL} | Input LOW Level (Input and I/O pins) | Guaranteed Logic LOW Level | | -0.5 | — | 0.8 | V |
| I _{IH} | Input HIGH Current (Input pins) | V _{CC} = Max. | V _I = 5.5V | — | — | ±1 | μA |
| | Input HIGH Current (I/O pins) | | V _I = V _{CC} | — | — | ±1 | |
| I _{IL} | Input LOW Current (Input pins) | | V _I = GND | — | — | ±1 | |
| | Input LOW Current (I/O pins) | | V _I = GND | — | — | ±1 | |
| I _{OZH} | High Impedance Output Current (3-State Output pins) | V _{CC} = Max. | V _O = V _{CC} | — | — | ±1 | μA |
| | | | V _O = GND | — | — | ±1 | |
| V _{IK} | Clamp Diode Voltage | V _{CC} = Min., I _{IN} = -18mA | | — | -0.7 | -1.2 | V |
| I _{ODH} | Output HIGH Current | V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V ⁽³⁾ | | -36 | -60 | -110 | mA |
| I _{ODL} | Output LOW Current | V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V ⁽³⁾ | | 50 | 90 | 200 | mA |
| V _{OH} | Output HIGH Voltage | V _{CC} = Min. V _{IN} = V _{IH} or V _{IL} | I _{OH} = -0.1mA | V _{CC} -0.2 | — | — | V |
| | | | I _{OH} = -3mA | 2.4 | 3 | — | |
| | | V _{CC} = 3V V _{IN} = V _{IH} or V _{IL} | I _{OH} = -8mA | 2.4 ⁽⁵⁾ | 3 | — | |
| V _{OL} | Output LOW Voltage | V _{CC} = Min. V _{IN} = V _{IH} or V _{IL} | I _{OL} = 0.1mA | — | — | 0.2 | V |
| | | | I _{OL} = 16mA | — | 0.2 | 0.4 | |
| | | | I _{OL} = 24mA | — | 0.3 | 0.55 | |
| | | V _{CC} = 3V V _{IN} = V _{IH} or V _{IL} | I _{OL} = 24mA | — | 0.3 | 0.5 | |
| I _{OS} | Short Circuit Current ⁽⁴⁾ | V _{CC} = Max., V _O = GND ⁽³⁾ | | -60 | -135 | -240 | mA |
| V _H | Input Hysteresis | — | | — | 150 | — | mV |
| I _{CC1} I _{CC2} I _{CC3} | Quiescent Power Supply Current | V _{CC} = Max., V _{IN} = GND or V _{CC} | | — | 0.1 | 10 | μA |

NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 3.3V, +25°C ambient and maximum loading.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- V_{OH} = V_{CC} - 0.6V at rated current.

POWER SUPPLY CHARACTERISTICS

| Symbol | Parameter | Test Conditions ⁽¹⁾ | | Min. | Typ. ⁽²⁾ | Max. | Unit |
|------------------|---|---|---|------|---------------------|--------------------|------------|
| I _{CC} | Quiescent Power Supply Current | V _{CC} = Max. | V _{IN} = V _{CC} - 0.6V | — | 2 | 30 | μA |
| I _{CCD} | Dynamic Power Supply Current ⁽⁴⁾ | V _{CC} = Max. Outputs Open x $\overline{O\bar{E}}$ = GND One Input Toggling 50% Duty Cycle | V _{IN} = V _{CC} V _{IN} = GND | — | 60 | 85 | μA/ MHz |
| I _C | Total Power Supply Current ⁽⁶⁾ | V _{CC} = Max. Outputs Open f _i = 10MHz 50% Duty Cycle x $\overline{O\bar{E}}$ = GND One Bit Toggling | V _{IN} = V _{CC} V _{IN} = GND | — | 0.6 | 0.9 | mA |
| | | | V _{IN} = V _{CC} - 0.6V V _{IN} = GND | — | 0.6 | 0.9 | |
| | | V _{CC} = Max. Outputs Open f _i = 2.5MHz 50% Duty Cycle x $\overline{O\bar{E}}$ = GND Eight Bits Toggling | V _{IN} = V _{CC} V _{IN} = GND | — | 1.2 | 1.7 ⁽⁵⁾ | |
| | | | V _{IN} = V _{CC} - 0.6V V _{IN} = GND | — | 1.2 | 1.8 ⁽⁵⁾ | |

NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 3.3V, +25°C ambient.
- Per TTL driven input. All other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of ΔI_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$
 I_{CC} = Quiescent Current (I_{CC}, I_{CCH}, and I_{CCZ})
 ΔI_{CC} = Power Supply Current for a TTL High Input
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for register devices (zero for non-register devices)
 N_{CP} = Number of clock inputs at f_{CP}
 f_i = Input Frequency
 N_i = Number of Inputs at f_i

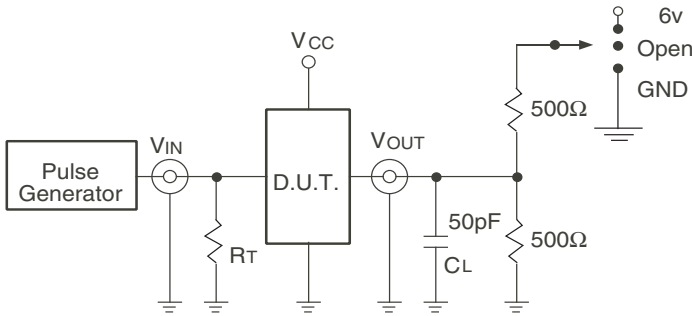
SWITCHING CHARACTERISTICS OVER OPERATING RANGE⁽¹⁾

| Symbol | Parameter | Condition ⁽²⁾ | 74FCT3244 | | 74FCT3244A | | Unit |
|------------------|---------------------|--|---------------------|------|---------------------|------|------|
| | | | Min. ⁽³⁾ | Max. | Min. ⁽³⁾ | Max. | |
| t _{PLH} | Propagation Delay | C _L = 50pF R _L = 500Ω | 1.5 | 6.5 | 1.5 | 4.8 | ns |
| t _{PHL} | xAx to xYx | | | | | | |
| t _{PZH} | Output Enable Time | | 1.5 | 8 | 1.5 | 6.2 | |
| t _{PZL} | | | | | | | |
| t _{PHZ} | Output Disable Time | 1.5 | 7 | 1.5 | 5.6 | ns | |
| t _{PLZ} | | | | | | | |

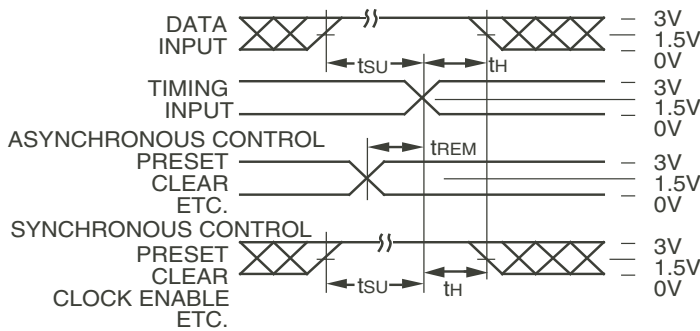
NOTES:

- Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, Normal Range. For V_{CC} = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.

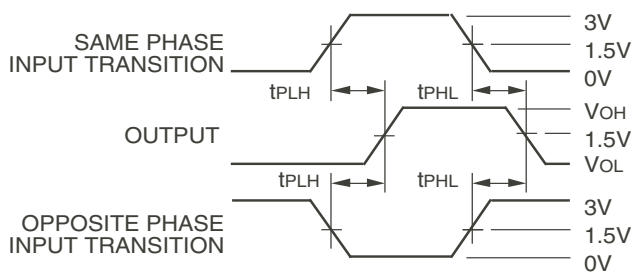
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-Up, Hold, and Release Times



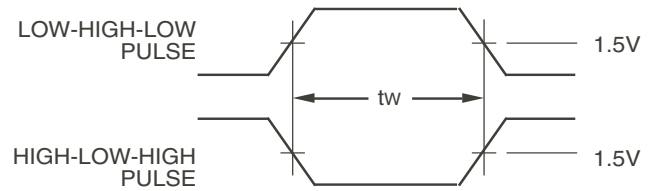
Propagation Delay

SWITCH POSITION

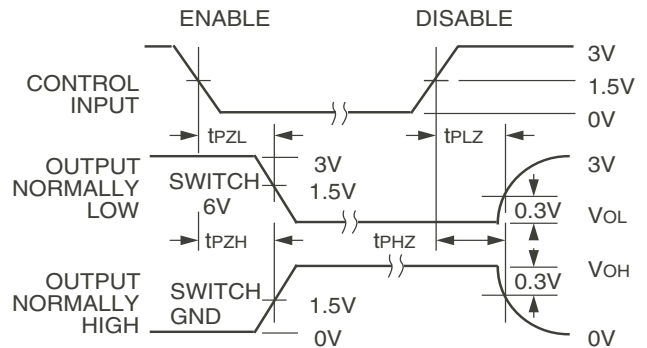
| Test | Switch |
|---|--------|
| Open Drain Disable Low Enable Low | 6V |
| Disable High Enable High | GND |
| All Other Tests | Open |

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width

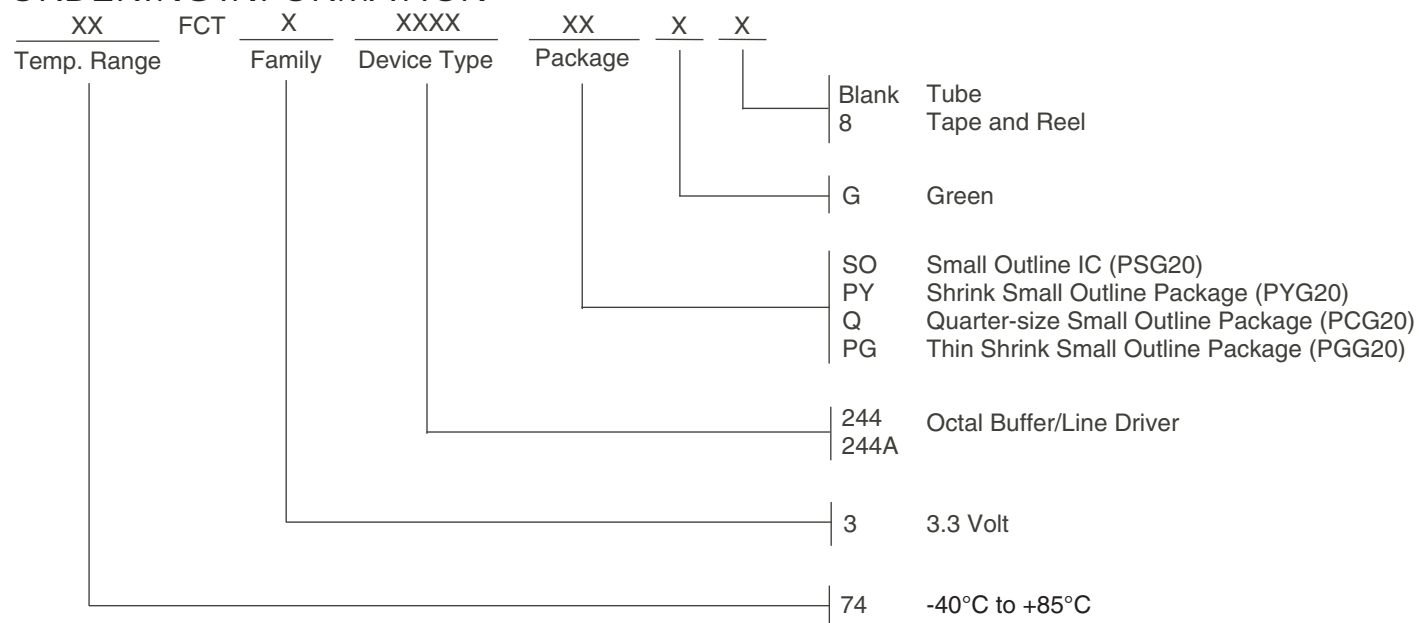


Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $Z_o \leq 50\Omega$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$.
3. If Vcc is below 3V, input voltage swings should be adjusted not to exceed Vcc.

ORDERING INFORMATION



Orderable Part Information

| Speed (ns) | Orderable Part ID | Pkg. Code | Pkg. Type | Temp. Grade |
|------------|-------------------|-----------|-----------|-------------|
| A | 74FCT3244APGG | PGG20 | TSSOP | I |
| | 74FCT3244APGG8 | PGG20 | TSSOP | I |
| | 74FCT3244APYG | PYG20 | SSOP | I |
| | 74FCT3244APYG8 | PYG20 | SSOP | I |
| | 74FCT3244AQG | PCG20 | QSOP | I |
| | 74FCT3244AQG8 | PCG20 | QSOP | I |
| | 74FCT3244ASOG | PSG20 | SOIC | I |
| | 74FCT3244ASOG8 | PSG20 | SOIC | I |

| Speed (ns) | Orderable Part ID | Pkg. Code | Pkg. Type | Temp. Grade |
|------------|-------------------|-----------|-----------|-------------|
| | 74FCT3244PGG | PGG20 | TSSOP | I |
| | 74FCT3244PGG8 | PGG20 | TSSOP | I |
| | 74FCT3244PYG | PYG20 | SSOP | I |
| | 74FCT3244PYG8 | PYG20 | SSOP | I |
| | 74FCT3244QG | PCG20 | QSOP | I |
| | 74FCT3244QG8 | PCG20 | QSOP | I |
| | 74FCT3244SOG | PSG20 | SOIC | I |
| | 74FCT3244SOG8 | PSG20 | SOIC | I |

Datasheet Document History

| | | |
|------------|-----------|--|
| 09/30/2009 | Pg. 6 | Updated the ordering information by removing the "IDT" notation and non RoHS part. |
| 08/31/2011 | Pg. 6 | Added PGG to ordering information. |
| 07/31/2017 | Pgs. 2, 6 | Added table under pin configuration diagram with detailed package information. Updated the ordering information diagram adding Tube, Tape and Reel. Added new table of orderable part information. |
| 05/23/2018 | Pg. 6 | Updated new table of orderable part information. |
| 02/11/2020 | Pgs. 1-7 | Rebranded as Renesas datasheet. |

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