THE DATASHEET OF

8535AG-01LF

Low Skew, 1-to-4 LVCMOS/LVTTL-to-3.3V LVPECL Fanout Buffer

ICS8535-01

DATA SHEET

General Description

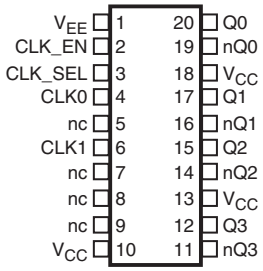
The ICS8535-01 is a low skew, high performance 1-to-4 LVCMOS/LVTTL-to-3.3V LVPECL fanout buffer. The ICS8535- 01 has two single ended clock inputs. the single ended clock input accepts LVCMOS or LVTTL input levels and translate them to 3.3V LVPECL levels. The clock enable is internally synchronized to eliminate runt clock pulses on the output during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the ICS8535-01 ideal for those applications demanding well defined performance and repeatability.

Features

- Four differential 3.3V LVPECL outputs
- Selectable CLK0 or CLK1 inputs for redundant and multiple frequency fanout applications
- CLK0 or CLK1 can accept the following input levels: LVCMOS or LVTTL
- Maximum output frequency: 266MHz
- Translates LVCMOS and LVTTL levels to 3.3V LVPECL levels
- Output skew: 30ps (maximum)
- Part-to-part skew: 250ps (maximum)
- Propagation delay: 1.9ns (maximum)
- Additive phase jitter, RMS: < 0.09ps (typical)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Lead-free (RoHS 6) packaging

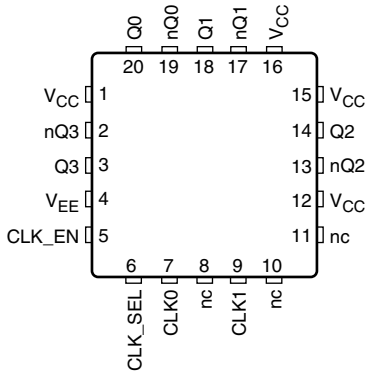
Pin Assignment



ICS8535-01

20-Lead TSSOP
4.4mm x 6.5mm x 0.92 body package
G Package

Top View

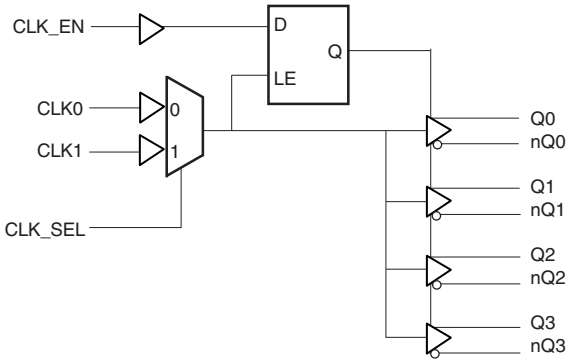


ICS8535-01

20-Lead VFQFN
4mm x 4mm x 0.9 body package
K Package

Top View

Block Diagram



Pin Descriptions and Characteristics

Table 1. Pin Descriptions[1]

Name	Type		Description
V_{EE}	Power		Negative supply pin.
CLK_EN	Input	Pullup	Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, Q outputs are forced low, nQ outputs are forced high. LVCMOS / LVTTL interface levels.
CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1 input. When LOW, selects CLK0 input. LVCMOS / LVTTL interface levels.
CLK0	Input	Pulldown	LVCMOS / LVTTL clock input.
CLK1	Input	Pulldown	LVCMOS / LVTTL clock input.
nc	Unused		No connect
V_{CC}	Power		Positive supply pins
nQ3, Q3	Output		Differential output pair. LVPECL interface levels.
nQ2, Q2	Output		Differential output pair. LVPECL interface levels.
nQ1, Q1	Output		Differential output pair. LVPECL interface levels.
nQ0, Q0	Output		Differential output pair. LVPECL interface levels.

NOTE 1: *Pullup* and *Pulldown* refers to internal input resistors. See *Table 2*, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Table 3A. Control Input Function Table

Inputs			Outputs	
CLK_EN	**CLK_SEL**	**Selected Source**	**Q0:Q3**	**nQ0:nQ3**
0	0	CLK0	Disabled; LOW	Disabled; HIGH
0	1	CLK1	Disabled; LOW	Disabled; HIGH
1	0	CLK0	Enabled	Enabled
1	1	CLK1	Enabled	Enabled

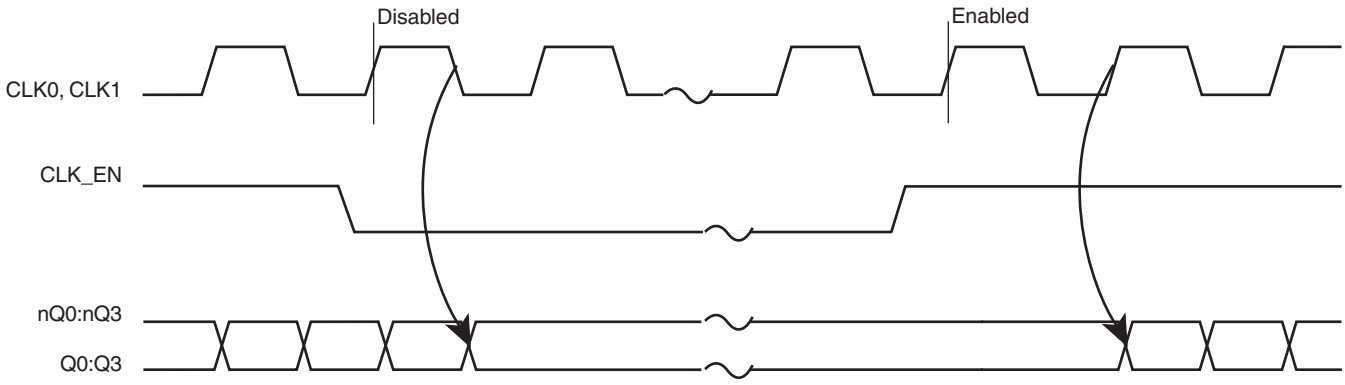


Figure 1. CLK_EN Timing Diagram

Table 3B. Clock Input Function Table

Inputs	Outputs	
CLK0 or CLK1	**Q0:Q3**	**nQ0:nQ3**
0	LOW	HIGH
1	HIGH	LOW

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Electrical Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA} 20-Lead TSSOP 20-Lead VFQFN	 73.2°C/W (0 lfps) 60.4°C/W (0mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V±5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				50	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{CC} = 3.3V±5%, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK0, CLK1		2		V_{CC} + 0.3	V
		CLK_EN, CLK_SEL		2		V_{CC} + 0.3	v
V_{IL}	Input Low Voltage	CLK0, CLK1		-0.3		1.3	V
		CLK_EN, CLK_SEL		-0.3		0.8	V
I_{IH}	Input High Current	CLK0, CLK1, CLK_SEL	V_{IN} = V_{CC} = 3.465V			150	µA
		CLK_EN	V_{IN} = V_{CC} = 3.465V			5	µA
I_{IL}	Input Low Current	CLK0, CLK1, CLK_SEL	V_{IN} = 0V, V_{CC} = 3.465V	-5			µA
		CLK_EN	V_{IN} = 0V, V_{CC} = 3.465V	-150			µA

Table 4C. LVPECL DC Characteristics, V_{CC} = 3.3V±5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage[1]		V_{CC} – 1.4		V_{CC} – 0.9	V
V_{OL}	Output Low Voltage[1]		V_{CC} – 2.0		V_{CC} – 1.7	V
V_{SWING}	Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC}– 2.

AC Characteristics

Table 5. AC Characteristics, V_{CC} = 3.3V±5%, T_A = 0°C to 70°C[1]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				266	MHz
t_{PD}	Propagation Delay[2]	$f \leq$ 266MHz	1.0		1.9	ns
tsk(o)	Output Skew[3, 4]			11	30	ps
tsk(pp)	Part-to-Part Skew[4, 5]				250	ps
t_{jit}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section[6]			0.09		ps
t_R / t_F	Output Rise/Fall Time	20% to 80% @ 50MHz	300		700	ps
odc	Output Duty Cycle		48	50	52	%

NOTE 1: All parameters measured at 266MHz unless noted otherwise. The cycle-to-cycle jitter on the input will equal the jitter on the output. The part does not add jitter.

NOTE 2: Measured from the V CC /2 of the input to the differential output crosspoint.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential crosspoints

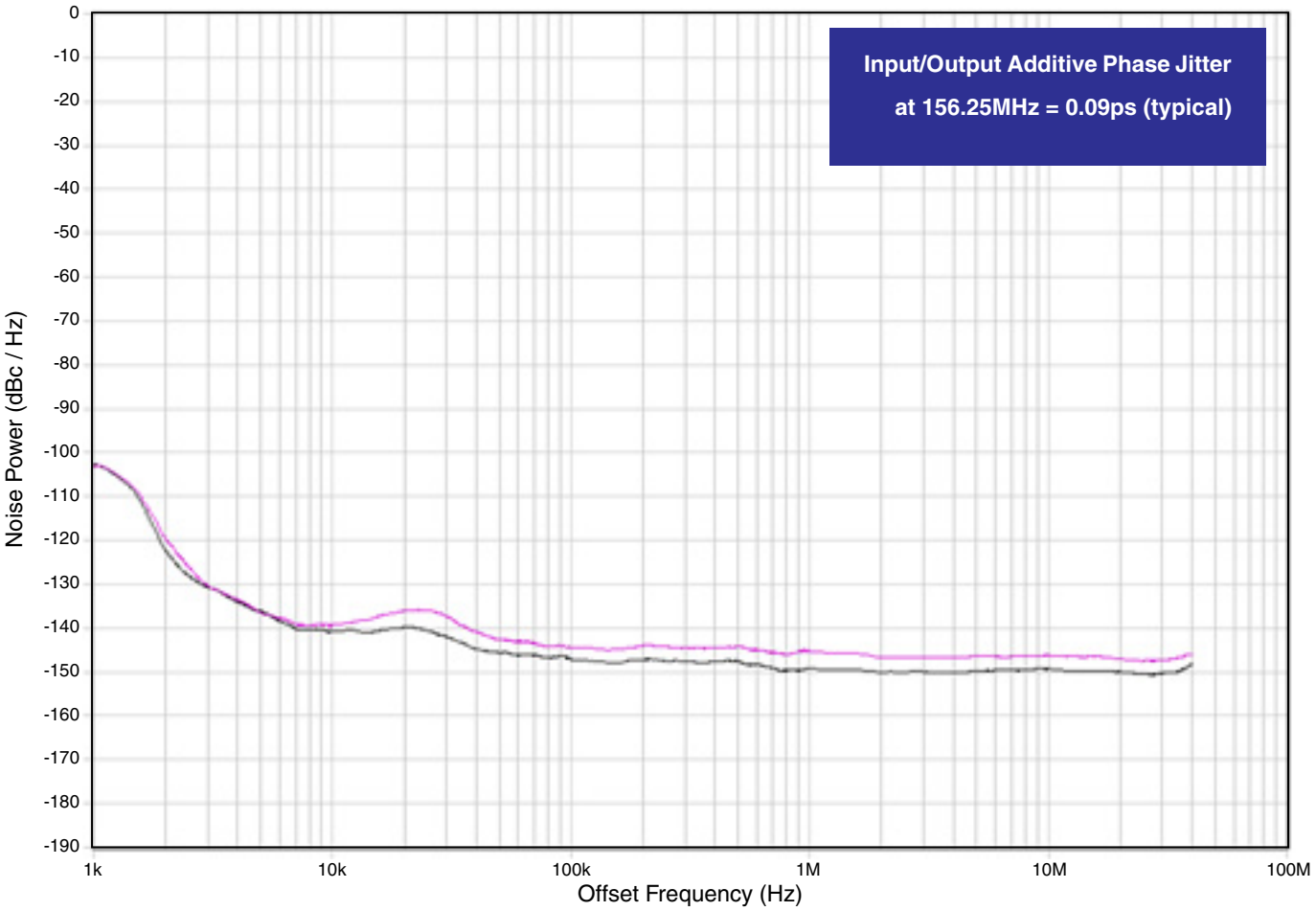
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoints.

NOTE 6: Driving only one input clock.

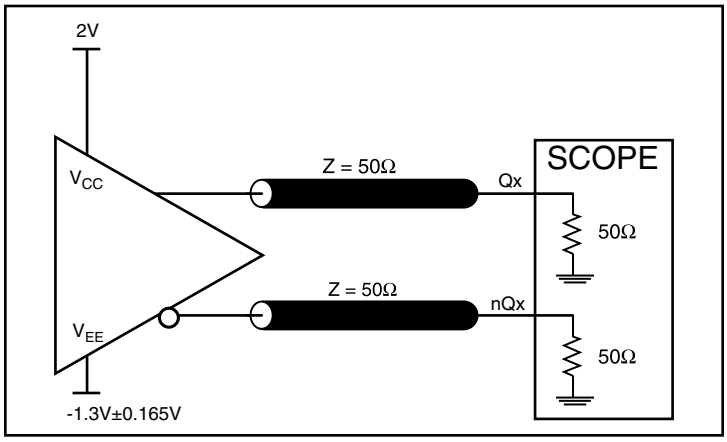
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise.** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

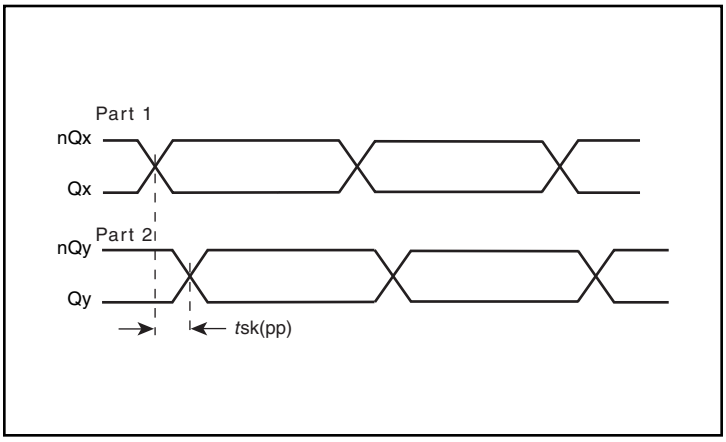


As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

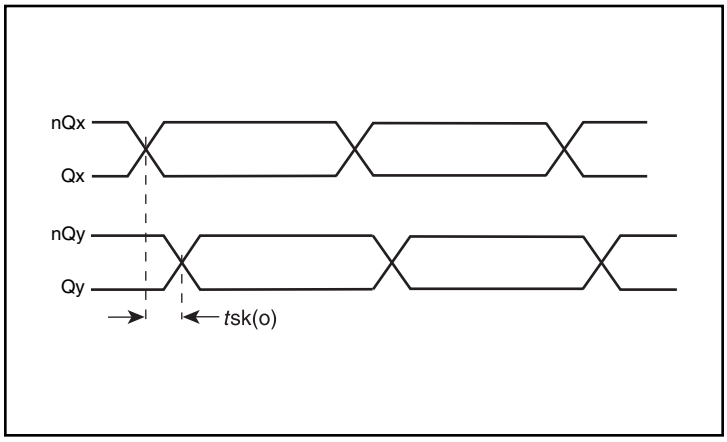
Parameter Measurement Information



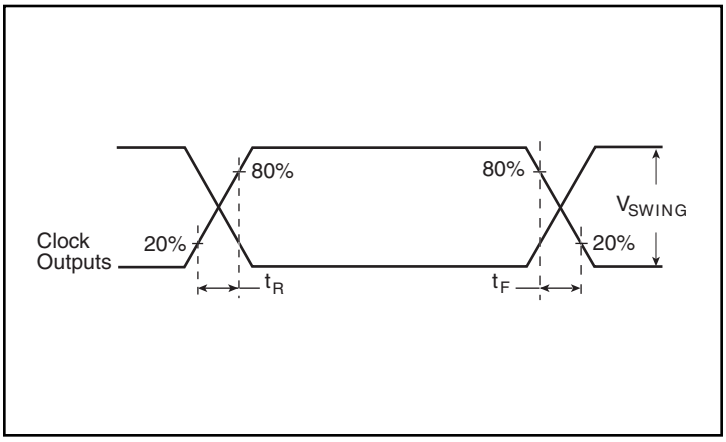
3.3V Output Load Test Circuit



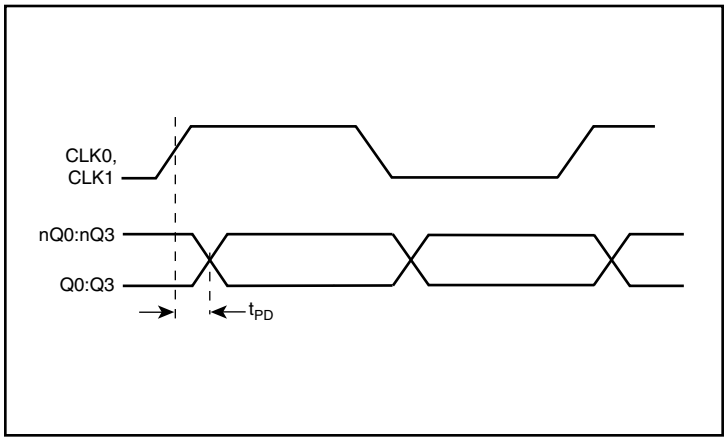
Part-to-Part Skew



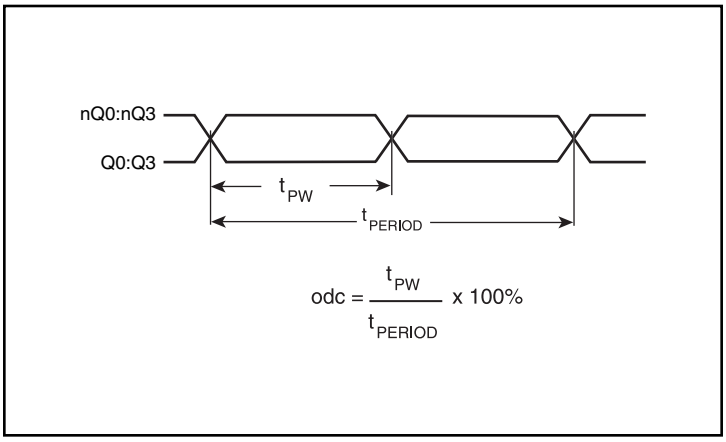
Output Skew



Output Rise/Fall Time



Propagation Delay



Output Duty Cycle/Pulse Width/Period

Applications Information

Recommendations for Unused Input Pins

Inputs:

CLK Input

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

LVCMOS Control Pins

All control pins have internal pullups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential output is a low impedance follower output that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figure 2A* and *Figure 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

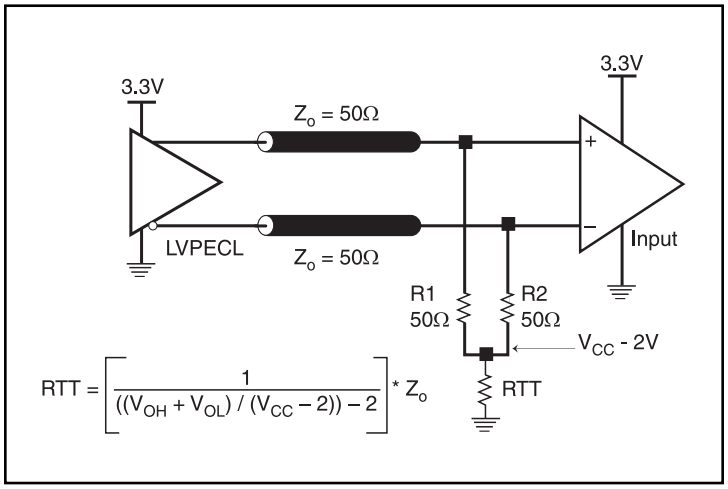


Figure 2A. 3.3V LVPECL Output Termination

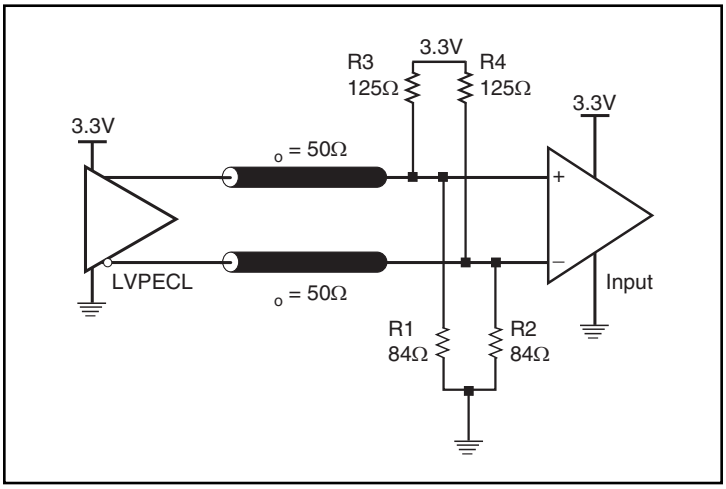


Figure 2B. 3.3V LVPECL Output Termination

Schematic Example

Figure 3 shows a schematic example of the ICS8535-01. In this example, the CLK0 input is selected. The decoupling capacitors should be physically located near the power pin. For ICS8535-01, the unused clock outputs can be left floating

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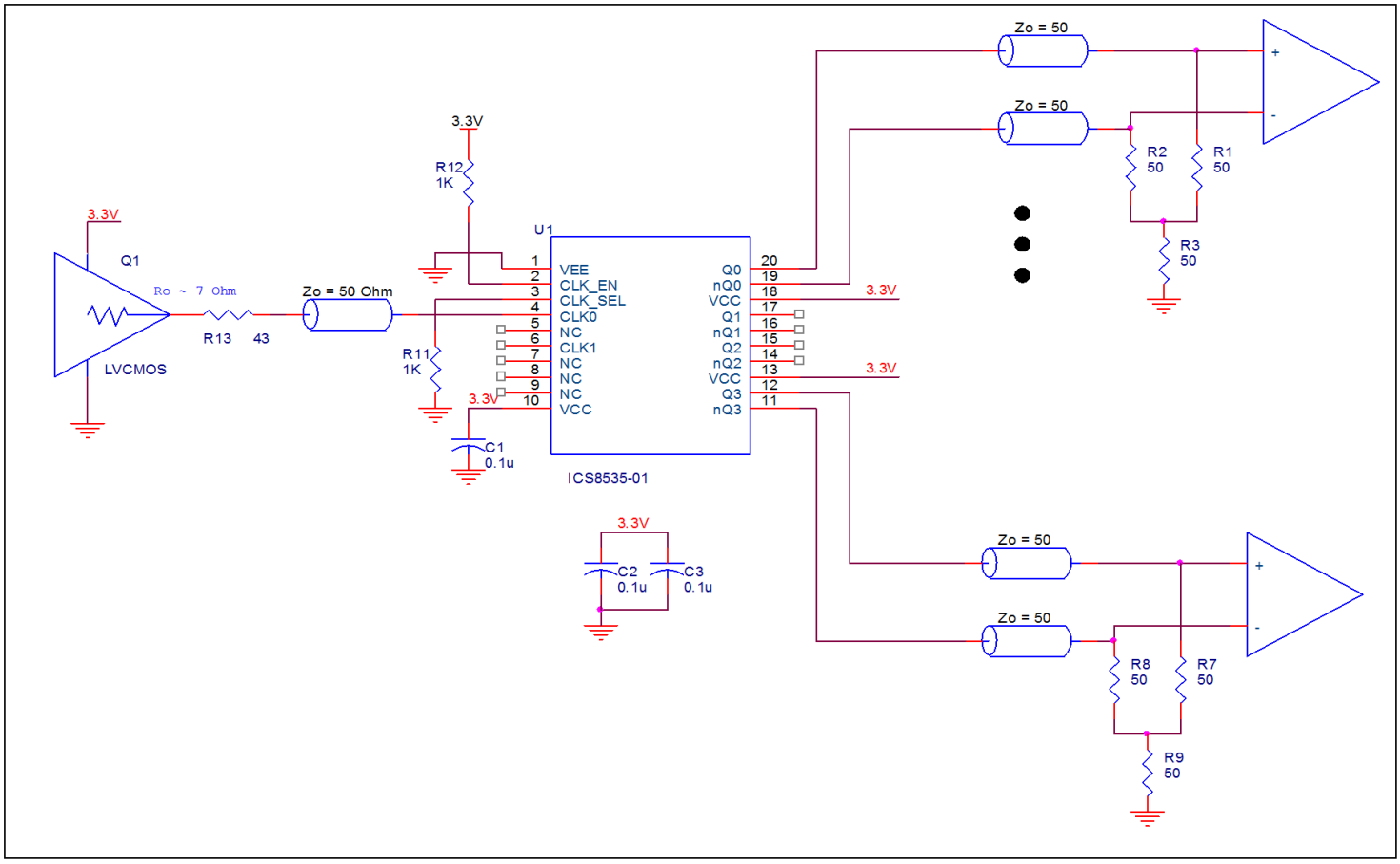

Figure 3. ICS8535-01 Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8535-01.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8535-01 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 50mA = **173.25mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 30mW = **120mW**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 173.25mW + 120mW = **293.25mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per *Table 6A* below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.293W * 66.6°C/W = 89.5°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 6A. Thermal Resistance θ_{JA} for 20-Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Table 6B. θ_{JA} vs. Air Flow Table for 20-Lead VFQFN

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**3**
Multi-Layer PCB, JEDEC Standard Test Boards	60.4°C/W	52.8°C/W	46.0°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 4.*

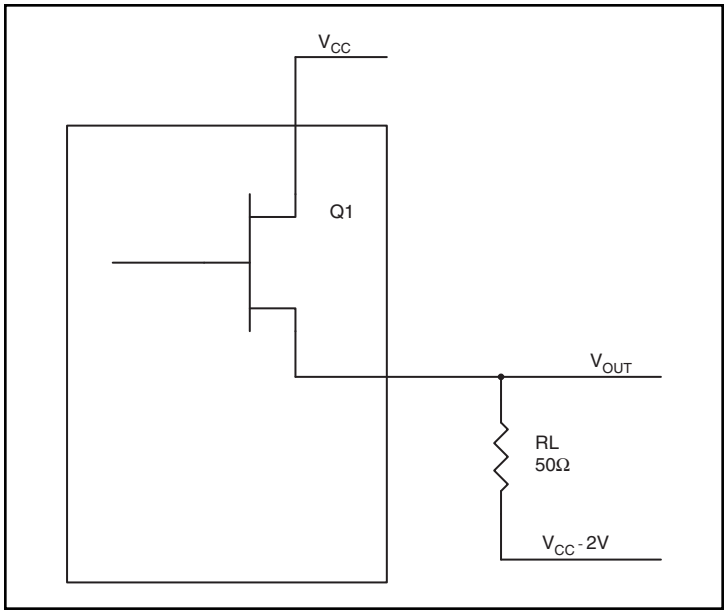

Figure 4. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} – 0.9V}$
  $(V_{CC\_MAX} – V_{OH\_MAX}) = \mathbf{0.9V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CO\_MAX} – 1.7V}$
  $(V_{CC\_MAX} – V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 7A. θ_{JA} vs. Air Flow Table for a 20-Lead TSSOP

θ_{JA} by Velocity			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Table 7B. θ_{JA} vs. Air Flow Table for 20-Lead VFQFN

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**3**
Multi-Layer PCB, JEDEC Standard Test Boards	60.4°C/W	52.8°C/W	46.0°C/W

Transistor Count

The transistor count for the IS8535-01 is 412.

Package Outline and Package Dimensions

Package Outline - G Suffix for 20-Lead TSSOP

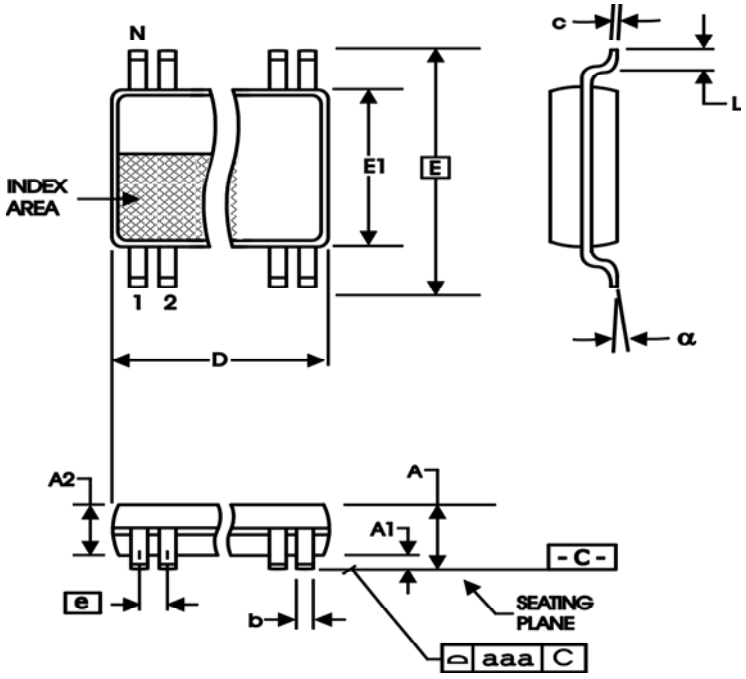

Table 8A. Package Dimensions for TSSOP

Symbol	Millimeters	
	Minimum	Maximum
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

Package Outline and Package Dimensions (continued)

Package Outline - K Suffix for 20-Lead VFQFN

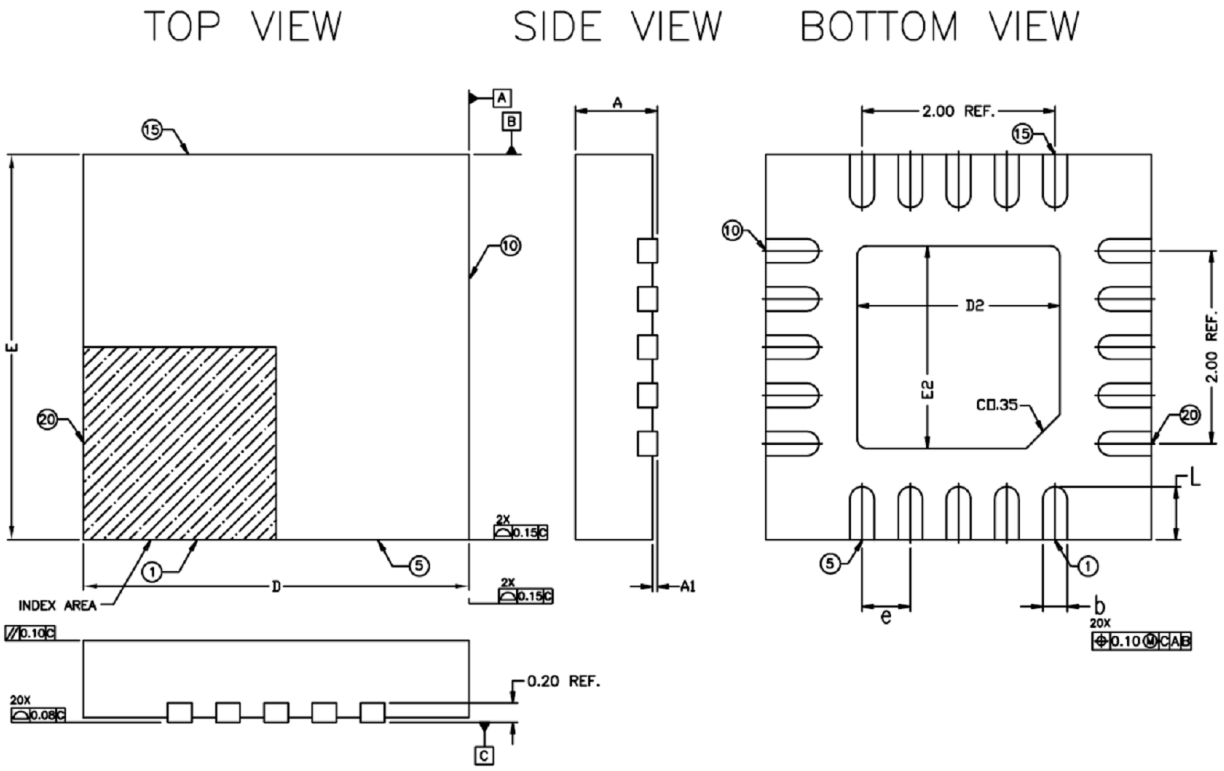

Table 9. Package Dimensions for 20-Lead VFQFN

JEDEC Variation: All Dimensions in Millimeters			
Symbol	**Minimum**	**Nom**	**Maximum**
b	0.20	0.25	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	1.95	2.10	2.25
E2	1.95	2.10	2.25
L	0.45	0.55	0.65
e	0.50 BSC		
N	20		
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	0.2 REF		

Reference Document: JEDEC Publication 95, MO-220

NOTE:

The drawing and dimension data originate from IDT package outline drawing PSC-4170, rev03.

1. Dimensions and tolerances conform to ASME Y14.5M-1994
2. All dimensions are in millimeters. All angles are in degrees.
3. N is the total number of terminals.
4. All specifications comply with JEDEC MO-220.

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8535AG-01LF	ICS8535A01LF	“Lead-Free” 20-Lead TSSOP	Tube	0°C to 70°C
8535AG-01LFT	ICS8535A01LF	“Lead-Free” 20-Lead TSSOP	Tape & Reel	0°C to 70°C
8535AK-01LF	35A01L	“Lead-Free” 20-Lead VFQFN	Tube	0°C to 70°C
8535AK-01LFT	35A01L	“Lead-Free” 20-Lead VFQFN	Tape & Reel	0°C to 70°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B		3	Updated Figure 1 - CLK_EN Timing Diagram.	10/16/01
B		3	Updated Figure 1 - CLK_EN Timing Diagram.	10/29/01
B		8	Added Termination for LVPECL Outputs section.	5/29/02
B		6	Output Load Test Circuit - corrected V_{EE} equation to read "V_{EE} = -0.5V ± 0.165V" from "VEE = -0.5V ± 0.135V".	10/4/02
C	T5	5	AC Characteristics table - changed tsk(pp) from 150ps max. to 250ps. max. Update format.	12/13/02
D		8 4 4	Added Schematic layout in the Application Section. LVCMOS Table - changed V_{IH} 3.765V Max. to V_{CC} + 0.3V Max. LVPECL Table - changed V_{SWING} 0.85V Max. to 1.0V Max.	1/20/03
D		8	Schematic Example, changed sentence to read "In this example, the XTAL input is selected." to "..., The CLK1 input is selected." Corrected schematic example.	4/1/03
E	T2 T5	1 2 4 5 6 8	Added RMS Jitter to Features section. Pin Characteristics Table - changed C_{IN} from 4pF max. to 4pF typical. Revised Absolute Maximum Ratings Output. AC Characteristics Table - added RMS Jitter. Added Additive Phase Jitter Section. Revised LVPECL Output Termination diagrams.	9/19/03
E		14	Added "Lead-Free" Part/Order Number rows.	11/13/03
E		14	Corrected "Lead-Free" marking and order/part numbers.	12/4/03
E	T5	1 5	Added Lead-Free bullet in the Features section. AC Characteristics table - added Note 5.	6/17/04
E	T9	14	Corrected Lead-Free marking in Ordering Information Table.	9/17/04
E	T7B T8B T9	1 12 14 15	Pin Assignment - added 20-Lead VFQFN package information. Added 20-Lead VFQFN Reliability Information. Added 20-Lead VFQFN Package Outline and Dimensions. Ordering Information Table - added 20-Lead VFQFN ordering information.	10/7/04
E	T9	15	Ordering Information Table - added "Lead-Free/Annealed" part number.	10/11/04
E		1	Pin Assignment - corrected letter package for 20-Lead VFQFN from "G Package" to "K Package".	12/8/04
E	T9	15	Ordering Information Table - corrected marking on TSSOP Lead-Free package and added Lead-Free note.	5/24/05
E	T9	8 15	Added Recommendations for Unused Input and Output Pins. Ordering Information Table - corrected 20-Lead VFQFN marking and added Lead-Free 20-Lead VFQFN part number.	9/16/05
E	T9	15	Ordering Information Table - corrected 20-Lead VFQFN Shipping Packaging.	3/21/06
E	T6B T7B	4 10 12	Absolute Maximum Ratings - corrected 20-Lead VFQFN Package Thermal Impedance. Corrected 20-Lead VFQFN Theta JA. Corrected 20-Lead VFQFN Theta JA.	10/02/06

Rev	Table	Page	Description of Change	Date
F	T4C	4 10 - 11	LVPECL DC Characteristics Table -corrected V_{OH} max. from V_{CC} - 1.0V to V_{CC} - 0.9V. Power Considerations - corrected power dissipation to reflect V_{OH} max in Table 4C.	4/12/07
F		1	NRND - Not Recommended For New Designs	5/20/13
F		1	Removed NRND marking from datasheet	5/28/13
F	 T8B	 14 14	Updated datasheet format. Updated Package Outline Updated package dimensions to reflect tighter tolerances.	8/7/14

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