



**THE DATASHEET OF  
A1162LLETR-T**



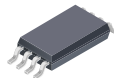
## Programmable Precision Hall-Effect Switch with Advanced Diagnostics

### FEATURES AND BENEFITS

- User-programmable unipolar switch points
- Integrated diagnostics for enhanced system safety and reliability
  - Enabled on demand
  - Integrated electromagnetic coils test the entire sensor signal path
  - Designed for ISO 26262/Quality Managed (QM) product
- Chopper stabilized
  - Resistant to physical stress
  - Superior temperature stability
- Internal regulator for wide operating voltage range
  - 3.8 to 24 V
- Automotive-grade ruggedness
  - Solid-state reliability
  - Reverse-battery protection
  - Output short-circuit protection
  - AEC-Q100 qualified
- Small surface-mount package

### PACKAGE:

8-Pin eTSSOP (Suffix LE)



Not to scale

### DESCRIPTION

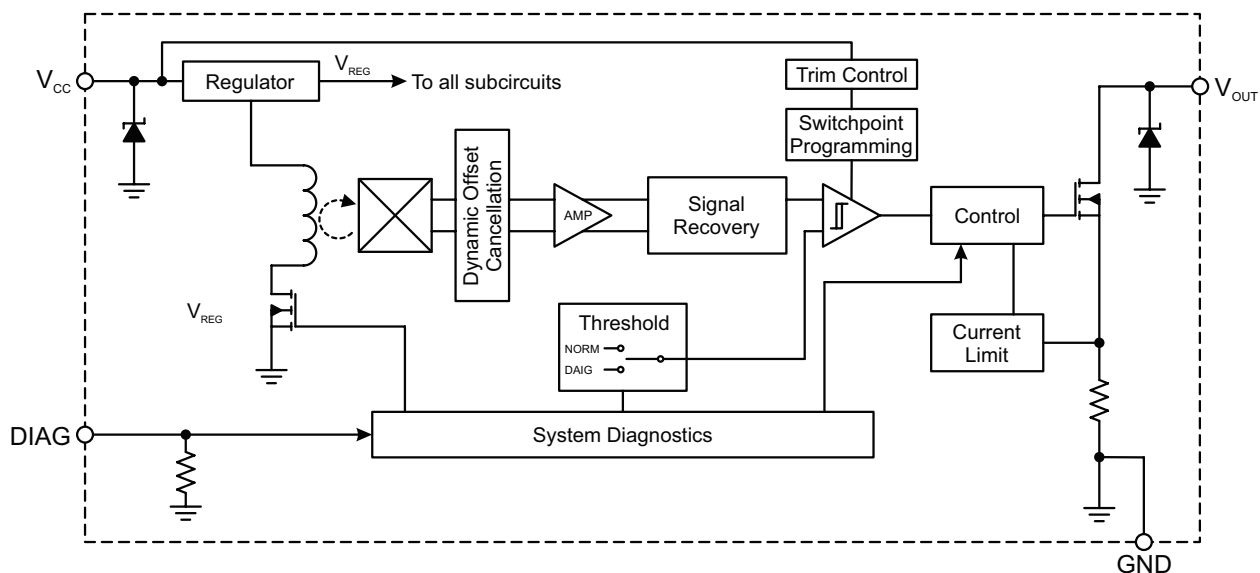
The A1162 is a unipolar Hall-effect switch with an externally enabled diagnostic function and user-programmable switch points. On-chip electromagnetic coils are used to implement self-test of the sensor's entire magnetic and electrical signal chain. It is designed for systems where precise magnet switch points and safety, reliability, or both, are critical, such as those designed to meet the requirements of ISO 26262.

In normal operating mode, the A1162 functions as a standard unipolar Hall-effect switch. The device output transistor turns on (output signal switches low) in the presence of sufficient magnetic field ( $>B_{OP\ max}$ ). The output transistor of the A1162 switches off (output signal switches high) when the magnetic field is removed ( $<B_{RP\ min}$ ).

When the diagnostic feature is enabled, the output of the A1162 provides a square wave output which confirms the device is properly sensing the internally generated magnetic field. Therefore, use of the A1162 either eliminates the need for redundant sensors in safety-critical applications or increases robustness in safety-critical applications that might otherwise require redundant sensors (drive-by-wire systems, etc.).

This monolithic IC integrates a voltage regulator, Hall voltage generator, small-signal amplifier, chopper stabilization, Schmitt trigger, and short-circuit-protected open-collector output able to sink up to 25 mA. The on-board regulator permits operation

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Functional Block Diagram

## DESCRIPTION (CONTINUED)

with supply voltages of 3.8 to 24 V. It is temperature-stable and stress-resistant, making it especially suited for operation over temperature ranges up to 150°C (L temperature range). Superior high-temperature performance is made possible through advanced dynamic offset cancellation techniques, which reduce the residual offset voltage normally caused by device overmolding, temperature dependencies, and thermal stress.

The A1162 is a Quality Managed (QM) product that has been developed according to the automotive quality requirements of IATF16949 and contains features targeted for automotive safety applications. This product can be qualified for use in accordance with ISO 26262 in compliant safety systems by ensuring a robust integration of the component into the system design. Safety documentation will be provided to support and guide the integration process.



## SPECIFICATIONS

### SELECTION GUIDE

Part Number	Packing	Package	Temperature Range, $T_A$ (°C)	Output in South Polarity Field	Magnetic Operate Point, $B_{OP}$ (G)
A1162LLETR-00-T	4000 pieces / reel	8-pin TSSOP	-40 to 150	Low	Programmable

### ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	$V_{CC}$		30	V
Reverse Supply Voltage	$V_{RCC}$		-18	V
Forward Diagnostic Enable Voltage	$V_{DIAG}$		6.5	V
Reverse Diagnostic Enable Voltage	$V_{RDIAG}$		-0.5	V
Output Off Voltage	$V_{OUT}$		30	V
Continuous Output Current	$I_{OUT}$		25	mA
Reverse Output Current	$I_{OUTR}$		50	mA
Operating Ambient Temperature	$T_A$	Range L	-40 to 150	°C
Maximum Junction Temperature	$T_{J(max)}$		165	°C
Storage Temperature	$T_{stg}$		-65 to 170	°C



Package LE, 8-Pin eTSSOP Pinouts

### Terminal List Table

Pin #	Symbol	Description
1	NC/GND	Connected to ground internally. May be left floating or connected to ground.
2	VOUT	Output from circuit
3	GND	Ground
4	GND	Ground
5	VCC	Connects power supply to chip
6	DIAG	Diagnostic Enable
7	NC/GND	Connected to ground internally. May be left floating or connected to ground.
8	NC/GND	Connected to ground internally. May be left floating or connected to ground.

**OPERATING CHARACTERISTICS:** Valid over full operating voltage and ambient temperature ranges, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
<b>ELECTRICAL CHARACTERISTICS</b>						
Supply Voltage	$V_{CC}$	Operating, $T_J < 165^\circ\text{C}$	3.8	–	24	V
Output Leakage Current	$I_{OUTOFF}$	$V_{OUT} = 24\text{ V}$ , $B < B_{RP}$	–	–	10	$\mu\text{A}$
Output Saturation Voltage	$V_{OUT(SAT)}$	$I_{OUT} = 20\text{ mA}$ , $B > B_{OP}$	–	185	400	mV
Output Current Limit	$I_{OM}$	$B > B_{OP}$	30	–	60	mA
Power-On Time [2]	$t_{ON}$	$V_{CC} > 3.8\text{ V}$ , $B < B_{RPmin} - 10\text{ G}$ , $B > B_{OPmax} + 10\text{ G}$	–	–	25	$\mu\text{s}$
Chopping Frequency	$f_C$		–	400	–	kHz
Output Rise Time [2][3]	$t_r$	$R_{LOAD} = 820\ \Omega$ , $C_L = 20\text{ pF}$	–	0.2	2	$\mu\text{s}$
Output Fall Time [2][3]	$t_f$	$R_{LOAD} = 820\ \Omega$ , $C_L = 20\text{ pF}$	–	0.1	2	$\mu\text{s}$
Supply Current	$I_{CC(ON)}$	$B > B_{OP}$	–	–	5	mA
	$I_{CC(OFF)}$	$B < B_{RP}$	–	–	5	mA
	$I_{CC(DIAG)}$	DIAG = 1, $T_J < T_{J(MAX)}$	–	16	25	mA
Reverse-Battery Current	$I_{RCC}$	$V_{RCC} = -18\text{ V}$	–	–	-10	mA
Supply Zener Clamp Voltage	$V_{ZSUP}$	$I_{CC} = 8\text{ mA}$ , $T_A = 25^\circ\text{C}$	30	–	–	V
Output Zener Voltage	$V_{ZOUT}$	$I_{OUT} = 3\text{ mA}$ , $T_A = 25^\circ\text{C}$	28	–	–	V
<b>DIAGNOSTIC CHARACTERISTICS</b>						
PWM Carrier Frequency	$f_{PWMout}$	With diagnostic mode enabled	–	3	–	kHz
Duty Cycle (Diagnostic Mode) [4]	$DC_{FAIL}$	DIAG = 1, Device Malfunction	–	0	40	%
	$DC_{FAIL}$	DIAG = 1, Device Malfunction	60	100	–	%
	$DC_{PASS}$	DIAG = 1, Device Normal	40	50	60	%
DIAG Pin Input Resistance	$R_{DIAG}$	DIAG pin pulled low	–	1	–	M $\Omega$
DIAG Pin Input Low Voltage Threshold	$V_{IL}$	Device in Normal Mode	–	–	0.6	V
DIAG Pin Input High Voltage Threshold	$V_{IH}$	Device in Diagnostic Mode	1.5	–	5	V
Diagnostic Time	$t_D$	The diagnostics feature should be enabled for at least $t_D$ in order to obtain an accurate PWM signal.	1	–	–	ms
Diagnostic Disable Time	$t_{DIS}$	Time from when DIAG pin is released (High to Low transition) to valid device output	–	–	25	$\mu\text{s}$

Continued on next page...

[1] Typical data is at  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 12\text{ V}$  and it is for design information only.

[2] Power-on time, Rise time and Fall time are guaranteed through device characterization and not final test.

[3]  $C_L$  = oscilloscope probe capacitance.

[4] When the DUT passes the diagnostic tests, the output will be a 50% duty cycle signal. Any other output indicates the DUT failed the test. See the application notes for more information.

**OPERATING CHARACTERISTICS (continued):** Valid over full operating voltage and ambient temperature ranges, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
<b>MAGNETIC CHARACTERISTICS [5]</b>						
Magnetic Step Size		B <sub>OP</sub> programming step size	–	5	–	G
Operate Point	B <sub>OP</sub>	Programmable	B <sub>RPmin</sub> + B <sub>HYS</sub>	–	250	G
Release Point	B <sub>RP</sub>	Programmable	–5	–	B <sub>OPmax</sub> – B <sub>HYS</sub>	G
Hysteresis (B <sub>OP</sub> – B <sub>RP</sub> )	B <sub>HYS00</sub>	B <sub>HYS</sub> register = 00	5	–	30	G
	B <sub>HYS01</sub>	B <sub>HYS</sub> register = 01	7	–	40	G
	B <sub>HYS10</sub>	B <sub>HYS</sub> register = 10	10	–	60	G
	B <sub>HYS11</sub>	B <sub>HYS</sub> register = 11	15	–	65	G
Maximum External Field in Diagnostic Mode [6]	B <sub>EXT(DIAG)</sub>		800	10,000	–	G
<b>DRIFT DETECTION THRESHOLD</b>						
Operate Point Drift	B <sub>OP(DRIFT)</sub>	Programmable	0.25 × B <sub>OP</sub>	–	1.75 × B <sub>OP</sub>	G
Release Point Drift	B <sub>RP(DRIFT)</sub>	Programmable	0.25 × B <sub>RP</sub>	–	1.75 × B <sub>RP</sub>	G

[1] Typical data is at T<sub>A</sub> = 25°C and V<sub>CC</sub> = 12 and it is for design information only.

[5] Magnetic flux density (B) is indicated as a negative value for north-polarity magnetic fields, and is a positive value for south-polarity magnetic fields.

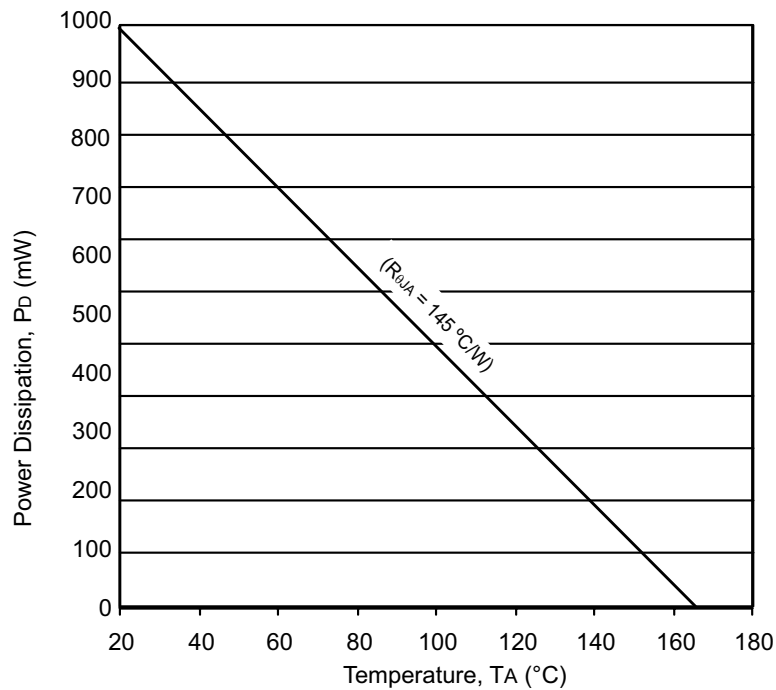
[6] 800 G is the maximum test capability due to practical equipment limitations. Design simulations show that a 10,000 G external field will not adversely affect the sensor in diagnostic mode.

**THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information**

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard JESD51-7	145	$^{\circ}\text{C}/\text{W}$

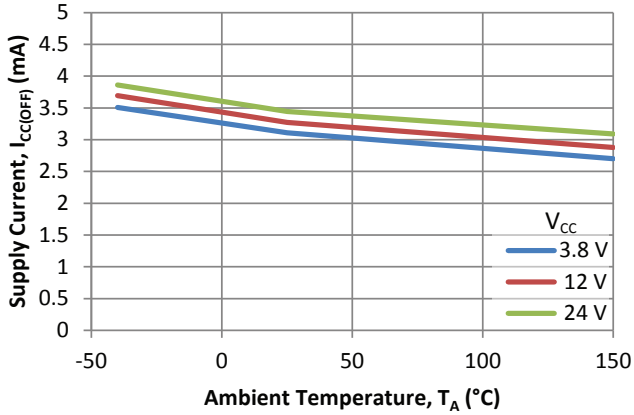
\*Additional thermal information available on the Allegro website

**Maximum Power Dissipation vs. Ambient Temperature**

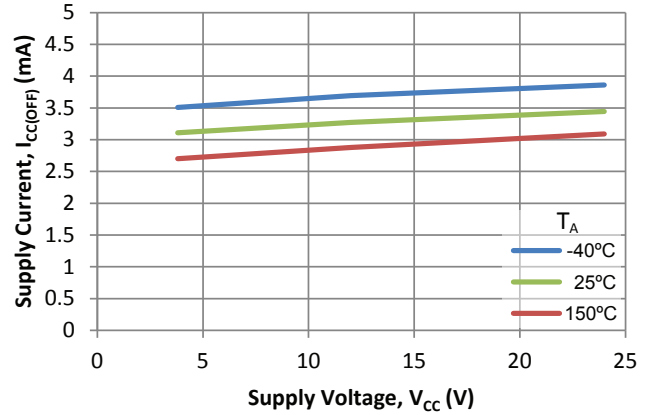


## CHARACTERISTIC PERFORMANCE

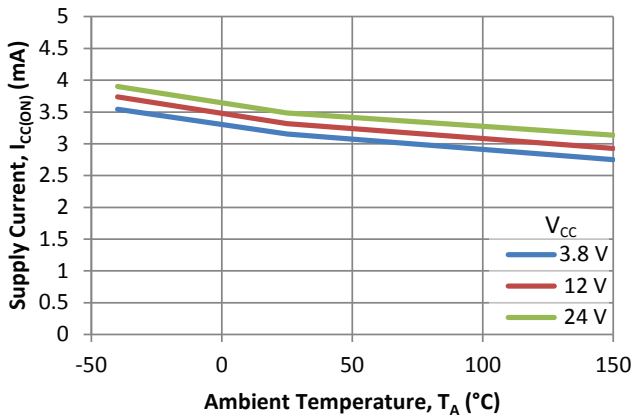
$I_{CC(OFF)}$  vs.  $T_A$



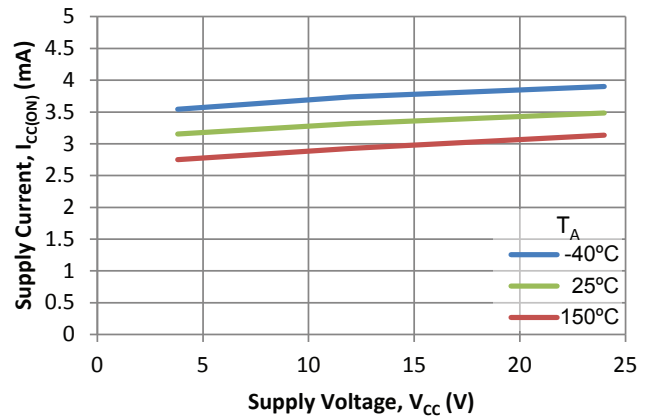
$I_{CC(OFF)}$  vs.  $V_{CC}$



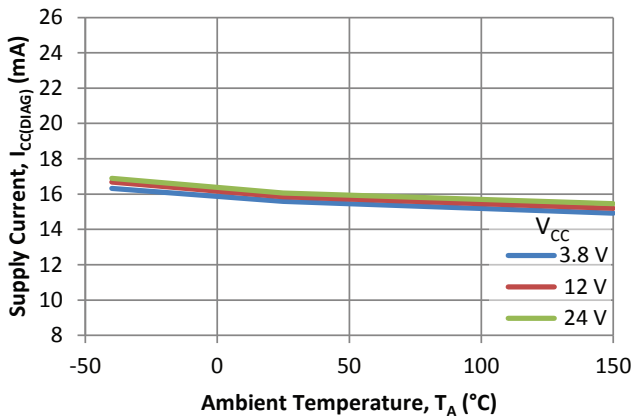
$I_{CC(ON)}$  vs.  $T_A$



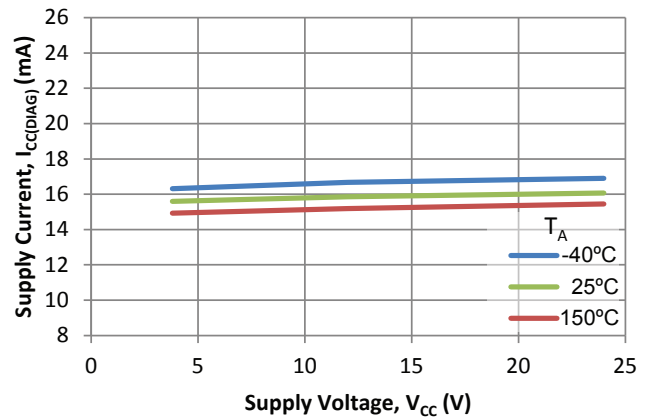
$I_{CC(ON)}$  vs.  $V_{CC}$

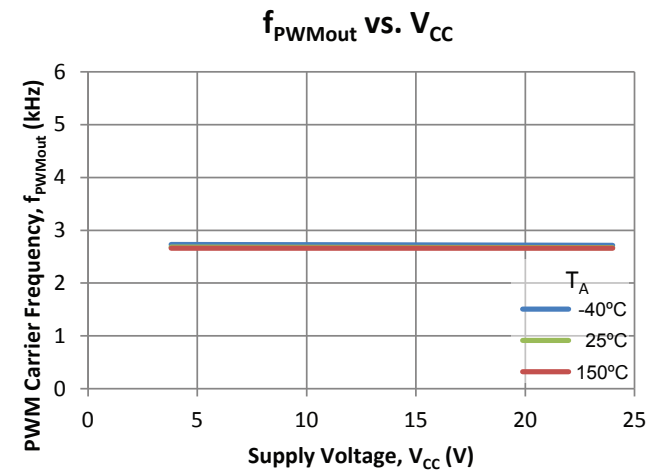
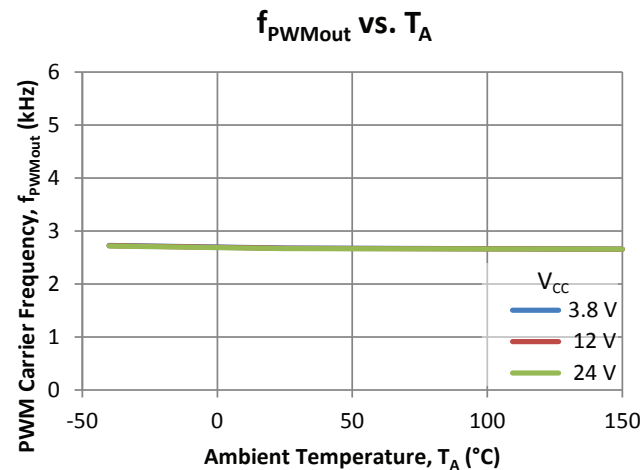
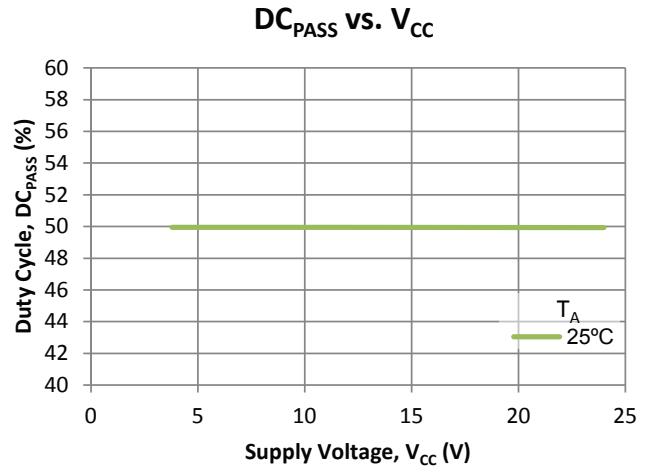
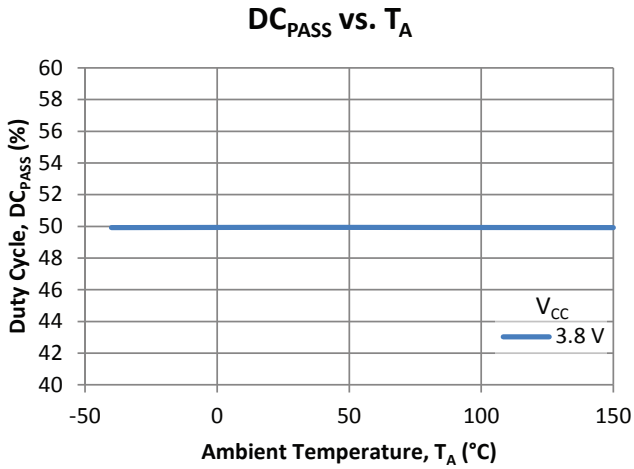
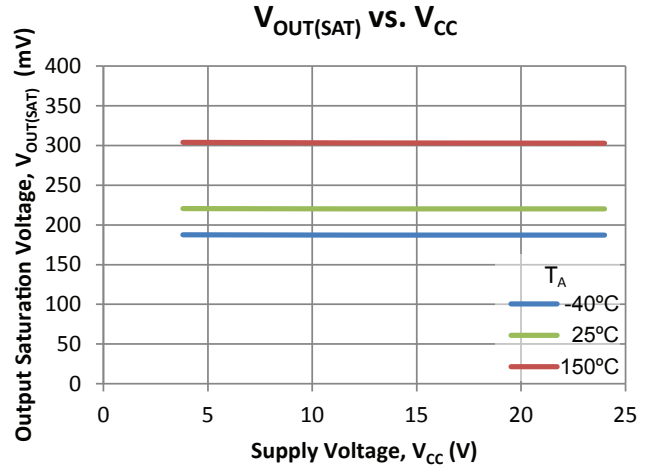
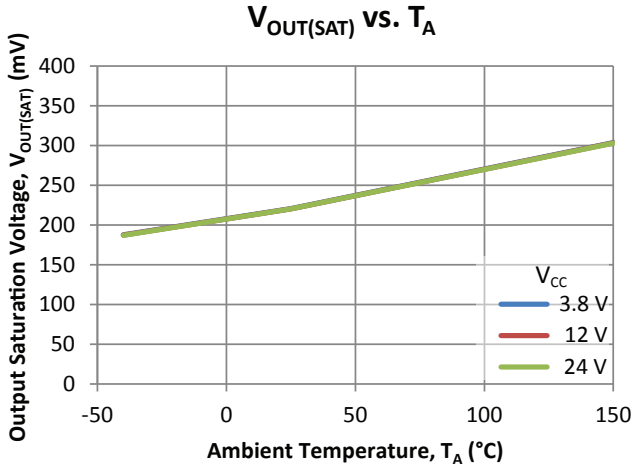


$I_{CC(DIAG)}$  vs.  $T_A$

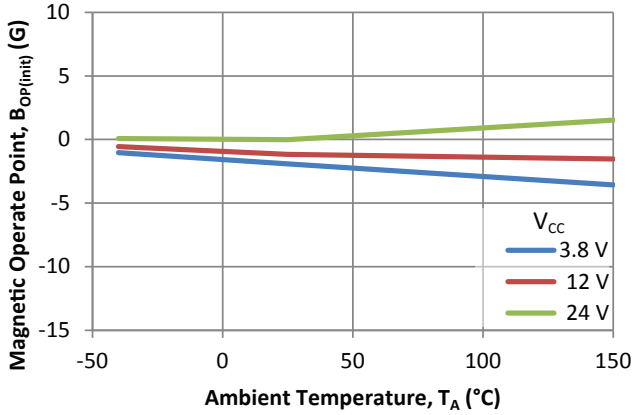


$I_{CC(DIAG)}$  vs.  $V_{CC}$

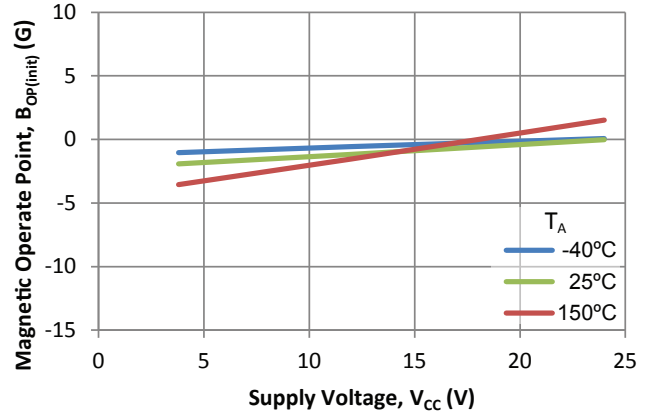




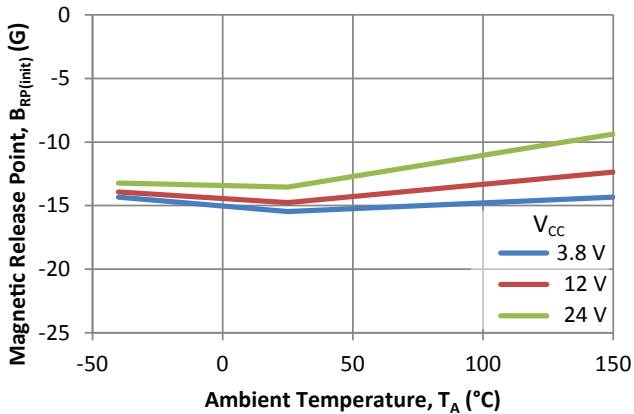
**$B_{OP(init)}$  vs.  $T_A$**



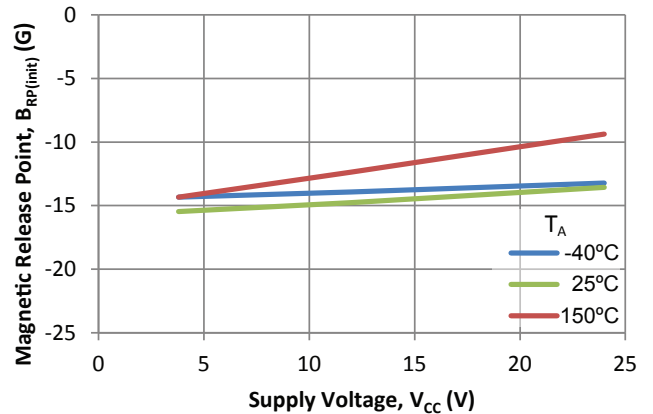
**$B_{OP(init)}$  vs.  $V_{CC}$**



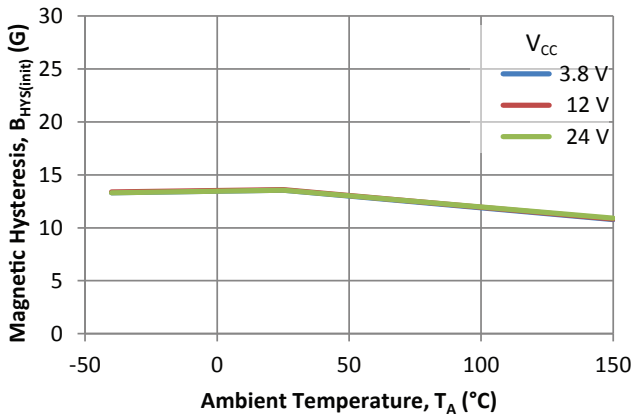
**$B_{RP(init)}$  vs.  $T_A$**



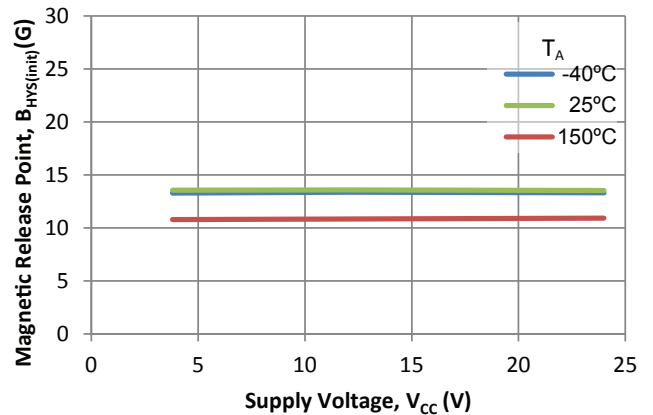
**$B_{RP(init)}$  vs.  $V_{CC}$**



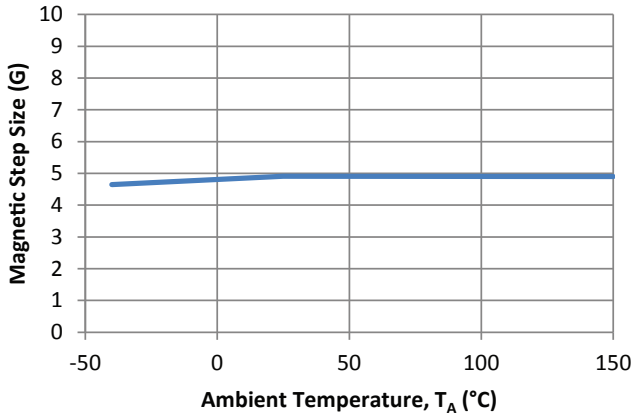
**$B_{HYS(init)}$  vs.  $T_A$**



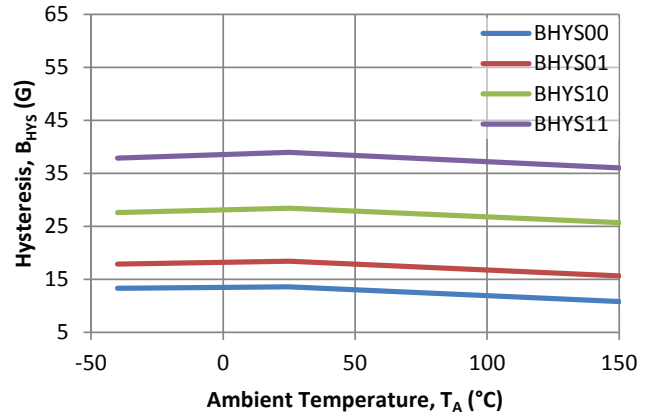
**$B_{HYS(init)}$  vs.  $V_{CC}$**



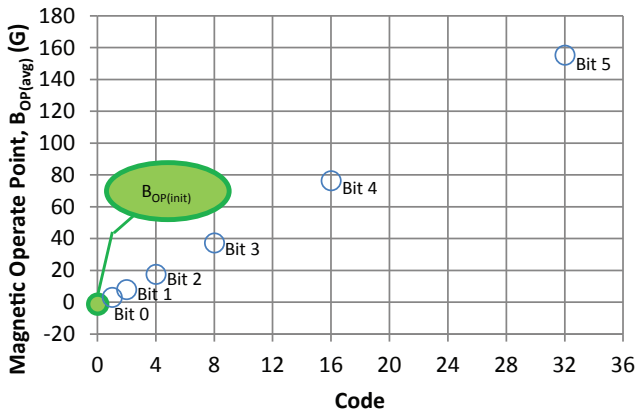
**B<sub>OP</sub> Programming Step Size vs. T<sub>A</sub>**



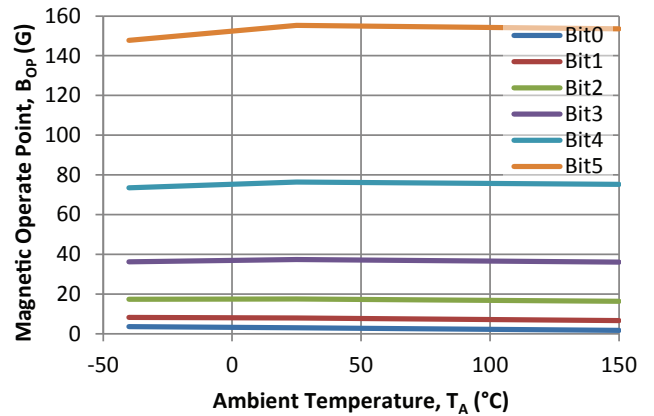
**B<sub>HYS</sub> vs. T<sub>A</sub>**



**B<sub>OP(avg)</sub> vs. Code**



**B<sub>OP</sub> Bit Weight vs. T<sub>A</sub>**



FUNCTIONAL DESCRIPTION

Operation

The output of these devices switches low (turns on) when a magnetic field perpendicular to the Hall sensor exceeds the operate point threshold,  $B_{OP}$  (see Figure 1). After turn-on, the output is capable of sinking 25 mA and the output voltage is  $V_{OUT(SAT)}$ . When the magnetic field is reduced below the release point ( $B_{RP}$ ) the device output goes high (turns off). The difference in the magnetic operate and release points is the hysteresis ( $B_{HYS}$ ) of the device. This built-in hysteresis allows clean switching of the output, even in the presence of external mechanical vibration and electrical noise.

Powering-on the device in the hysteresis range, less than  $B_{OP}$  and higher than  $B_{RP}$ , results in a HIGH output state. The correct state is attained after the first excursion beyond  $B_{OP}$  or  $B_{RP}$ . The output will not switch until there is a valid transition beyond  $B_{OP}$  or  $B_{RP}$ .

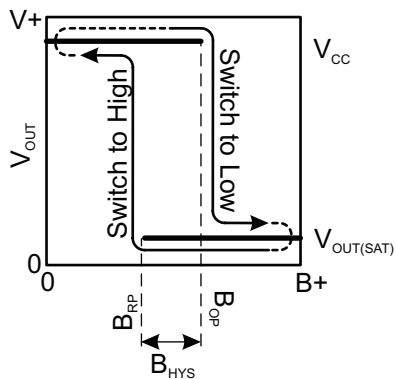


Figure 1: Switching Behavior of Unipolar Switches

On the horizontal axis, the B+ direction indicates increasing south polarity magnetic field strength.

Power-On Sequence and Timing

The output states are only valid when the supply voltage is within the specified operating range ( $V_{CC(MIN)} \leq V_{CC} \leq V_{CC(MAX)}$ ) and the power-on time has elapsed ( $t > t_{ON}$ ). Refer to Figure 2 for an illustration of the power-on sequence.

Once the supply voltage is within the operational range, the output will be in the low state (power-on state), irrespective of the magnetic field. The output will remain low until the sensor is fully powered on ( $t > t_{ON}$ ), at which point, the output will respond to the corresponding magnetic field presented to the sensor.

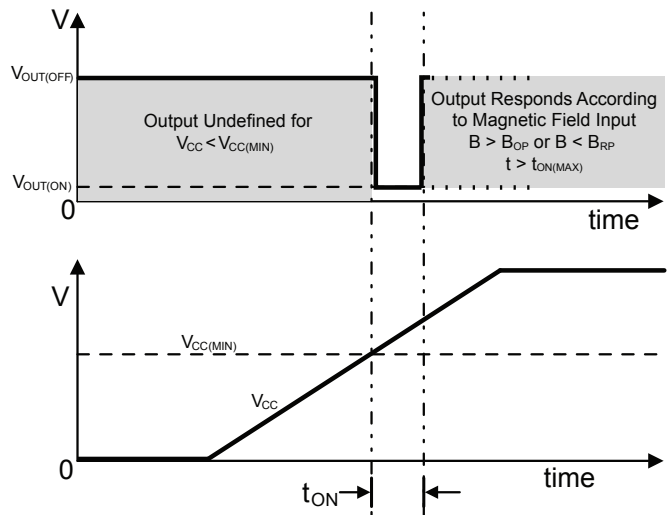


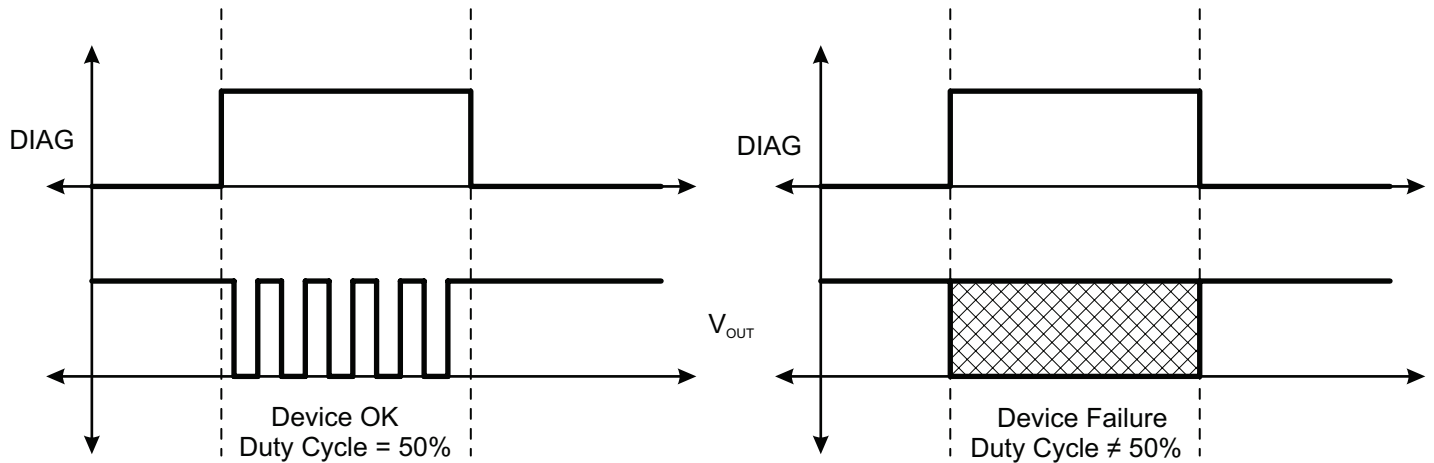
Figure 2: Power-On Sequence and Timing

**Diagnostic Mode of Operation**

The diagnostic mode is accessed by applying a voltage higher than  $V_{IH}$  on the diagnostic enable pin. The diagnostic mode uses an internally generated magnetic signal to exercise the signal path. This signal is compared to two reference signals in the Schmitt Trigger block (refer to Figure 3).

If the diagnostic signal is between the two reference signals, the part is considered to be working within specifications and a 50% PWM signal is set at the output pin, as shown in Figure 3. If the diagnostic signal is above the upper reference or below the lower reference, the output is set at a fixed value (High/Low).

The diagnostic mode of operation not only detects catastrophic failures but also drifts in the magnetic switch points. If  $B_{OP}$  or  $B_{RP}$  drift to values below or above the values stated in the Drift Detection Threshold table, the output is set at a fixed value when in the diagnostic mode of operation.



**Figure 3: Diagnostic Functional Diagram**

When the device passes, there will be a 50% duty-cycle signal sent out. In the event of a failure, the output will typically be forced either high or low. Diagnostic mode is only active when DIAG is pulled high.

## Applications

It is strongly recommended that an external capacitor be connected (in close proximity to the Hall sensor) between the supply and ground of the device to reduce both external noise and noise generated by the chopper stabilization technique. As shown in Figure 4, a 0.1  $\mu\text{F}$  capacitor is typical.

Note that pins 3 and 4 are the primary ground return for all sensor functions. These pins should be connected together close to the IC. Pins 1, 7, and 8 are connected to ground internally, but these pins may be connected to ground or left floating. They must not be connected to VCC or any other signal.

Extensive applications information on magnets and Hall-effect sensors is available in:

- *Hall-Effect IC Applications Guide, AN27701*
- *Soldering Methods for Allegro's Products – SMT and Through-Hole, AN26009*
- *Guideline for Designing Subassemblies Using Hall-Effect Devices, AN27703.1*
- *ASEK-02 Allegro Sensor Evaluation Kit Technical Guide*

All are provided on the Allegro website:

[www.allegromicro.com](http://www.allegromicro.com)

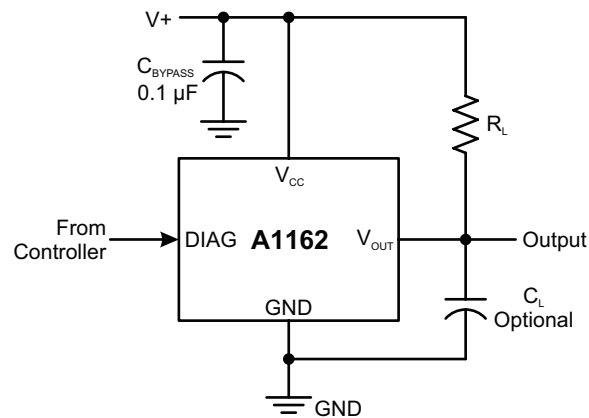


Figure 4: Typical Application Circuit

## PROGRAMMING GUIDELINES

### Overview

Programming is accomplished by sending a series of input voltage pulses serially through the VCC (supply) pin of the device. A unique combination of different voltage level pulses controls the internal programming logic of the device to select a desired programmable parameter and change its value. There are three voltage levels that must be taken into account when programming. These levels are referred to as *high* ( $V_{PH}$ ), *mid* ( $V_{PM}$ ), and *low* ( $V_{PL}$ ).

The A1162 features three programmable modes, Try mode, Blow mode, and Read mode:

- In Try mode, programmable parameter values are set and measured simultaneously. A parameter value is stored temporarily, and is reset after cycling the supply voltage.
- In Blow mode, the value of a programmable parameter may be permanently set by blowing solid-state fuses internal to the device. Device-locking is also accomplished in this mode.
- In Read mode, each bit may be verified as blown or not blown.

The programming sequence is designed to help prevent the device from being programmed accidentally—for example, as a result of noise on the supply line. Note that, for all programming modes, no parameter programming registers are accessible after the device-level LOCK bit is set. The only function that remains accessible is the overall Fuse Checking feature.

Although any programmable variable power supply can be used to generate the pulse waveforms, for design evaluations, Allegro highly recommends using the ASEK-20 Allegro Sensor IC Evaluation Kit. The ASEK-20 kit provides a graphical user interface (GUI) for programming various Allegro field-programmable

Hall-effect devices. In addition, a low-voltage interface board is required—contact your local FAE regarding availability.

The ASEK-20 kit is intended for use as a benchtop engineering tool, for learning about, evaluating, and characterizing Allegro sensors, for programming/calibrating devices in small volumes, and for developing code and procedures for use in production. Note that this kit is not recommended for production purposes.

See <https://www.allegromicro.com/en/design-support/evaluation-kits-and-demo-boards/asek-20-sensor-evaluation-kit> for more details. Contact your local Allegro FAE regarding availability or purchase the kit from Digi-Key (Part Number 620-1629-ND).

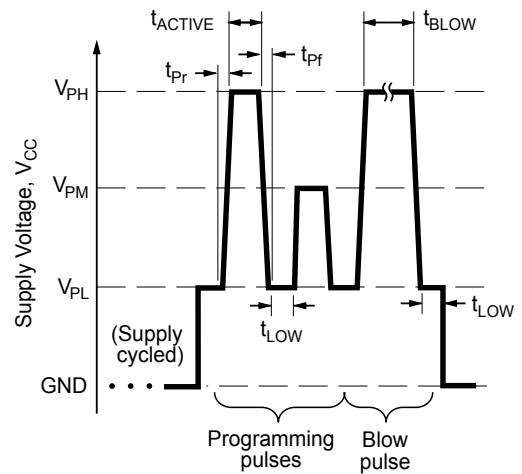


Figure 5: Programming Pulse Definitions (see Table 1)

Table 1: Programming Pulse Requirements, Protocol at  $T_A = 25^\circ\text{C}$

Characteristics	Symbol	Notes	Min.	Typ.	Max.	Unit
Programming Voltage	$V_{PL}$	Measured at the VCC pin	4.5	5	5.5	V
	$V_{PM}$		12.5	–	14	V
	$V_{PH}$		21	–	27	V
Programming Current	$I_{PP}$	$V_{CC} = 5 \rightarrow 26\text{ V}$ , $C_{BLOW} = 0.1\ \mu\text{F}$ (min); minimum supply current required to ensure proper fuse blowing.	175	–	–	mA
Pulse Width	$t_{LOW}$	Duration of $V_{PL}$ separating pulses at $V_{PM}$ or $V_{PH}$	20	–	–	$\mu\text{s}$
	$t_{ACTIVE}$	Duration of pulses at $V_{PM}$ or $V_{PH}$ for key/code selection	20	–	–	$\mu\text{s}$
	$t_{BLOW}$	Duration of pulse at $V_{PH}$ for fuse blowing	90	100	–	$\mu\text{s}$
Pulse Rise Time	$t_{Pr}$	$V_{PL}$ to $V_{PM}$ or $V_{PL}$ to $V_{PH}$	5	–	100	$\mu\text{s}$
Pulse Fall Time	$t_{Pf}$	$V_{PM}$ to $V_{PL}$ or $V_{PH}$ to $V_{PL}$	5	–	100	$\mu\text{s}$
Blow Pulse Slew Rate	$SR_{BLOW}$		0.375	–	–	V/ $\mu\text{s}$

## Definition of Terms

**Register** The section of the programming logic that controls the choice of programmable modes and parameters.

**Bit Field** The internal fuses unique to each register, represented as a binary number. Changing the bit field settings of a particular register causes its programmable parameter to change, based on the internal programming logic.

**Key** A series of voltage pulses used to select a register or mode

**Code** The number used to identify the combination of fuses activated in a bit field, expressed as the decimal equivalent of the binary value. The LSB of a bit field is denoted as code 1, or bit 0.

**Addressing** Increasing the bit field code of a selected register by serially applying a pulse train through the VCC pin of the device. Each parameter can be measured during the addressing process, but the internal fuses must be blown before the programming code (and parameter value) becomes permanent.

**Fuse Blowing** Applying a high-voltage pulse of sufficient duration to permanently set an addressed bit by blowing a fuse internal to the device. Once a bit (fuse) has been blown, it cannot be reset.

**Blow Pulse** A high-voltage pulse of sufficient duration to blow the addressed fuse.

**Cycling the Supply** Powering-down, and then powering-up the supply voltage. Cycling the supply is used to clear the programming settings in Try mode.

## Programming Procedure

Programming involves selection of a register and mode, and then setting values for parameters in the register for evaluation or fuse blowing. Figure 10 provides an overview state diagram.

## REGISTER SELECTION

Each programmable parameter can be accessed through a specific register. To select a register, from the Initial state, a sequence of voltage pulses consisting of one  $V_{PH}$  pulse, one  $V_{PM}$  pulse, and then a unique combination of  $V_{PH}$  and  $V_{PM}$  pulses, is applied serially to the VCC pin (with no  $V_{CC}$  supply interruptions). This

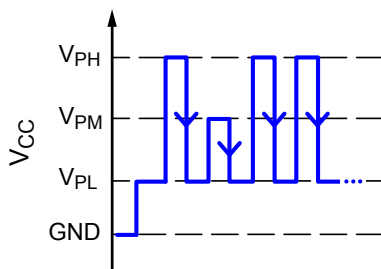


Figure 6: Example of Try Mode Register Selection Pulses, for the  $B_{OP}$  Negative Trim, Up-Counting Register.

sequence of pulses is called the *key*, and uniquely identifies each register. An example register selection key is shown in Figure 6.

To simplify Try mode, the A1162 provides a set of virtual registers for each combination of:  $B_{OP}$  selection (BOPSEL),  $B_{HYS}$  selection, and a facility for transiting  $B_{OP}$  magnitude values in an increasing or decreasing sequence. These registers also allow wrapping back to the beginning of the register after transiting the register.

## MODE SELECTION

The same physical registers are used for all programming modes. To distinguish Blow mode and Read mode, when selecting the registers, an additional pulse sequence consisting of eleven  $V_{PM}$  pulses followed by one  $V_{PH}$  pulse is added to the key. The combined register and mode keys are shown in Table 3.

## TRY MODE

In Try mode, the bit field addressing is accomplished by applying a series of  $V_{PM}$  pulses to the VCC pin of the device, as shown in Figure 7. Each pulse increases the total bit field value of the selected parameter, increasing by one on the falling edge of each additional  $V_{PM}$  pulse. When addressing a bit field in Try mode, the number of  $V_{PM}$  pulses is represented by a decimal number called a *code*. Addressing activates the corresponding fuse locations in the given bit field by increasing the binary value of an internal DAC, up to the maximum possible code. As the value of the bit field code increases, the value of the programmable parameter changes. Measurements can be taken after each  $V_{PM}$  pulse to determine if the desired result for the programmable parameter has been reached. Cycling the supply voltage resets all the locations in the bit field that have un-blown fuses to their initial states. This should also be done before selection of a different register in Try mode.

When addressing a parameter in Try mode, the bit field address (code) defaults to the value 1, on the falling edge of the final register selection key  $V_{PH}$  pulse (see Figure 5). A complete example is shown in Figure 8. Note that, in the four  $B_{OP}$  selection virtual registers, after the maximum code is entered, the next  $V_{PM}$  pulse wraps back to the beginning of the register, and selects code 0.

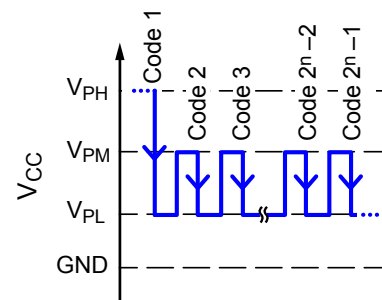
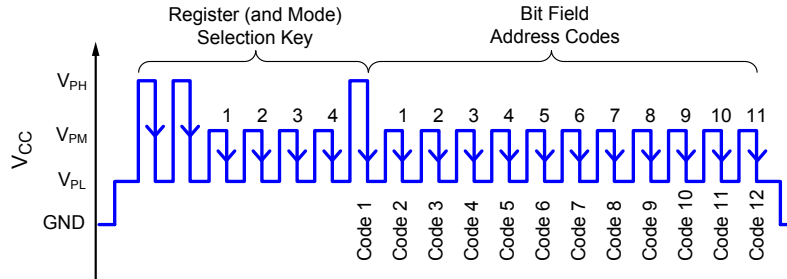


Figure 7: Try Mode Bit Field Addressing Pulses.



**Figure 8: Example of Try Mode Programming Pulses Applied to the VCC Pin**

In this example, B<sub>OP</sub> Trim, Down-Counting register is addressed to code 12 by the eleven V<sub>PM</sub> pulses (code 1 is selected automatically at the falling edge of the register-mode selection key).

The B<sub>OP</sub> selecting virtual register allows the programmer to adjust the B<sub>OP</sub> parameter from low to high, or from high to low. Figure 9 shows the relationship between the B<sub>OP</sub> parameter and the different Try mode registers.

### BLOW MODE

After the required code is determined for a given parameter, its value can be set permanently by blowing individual fuses in the appropriate register bit field. Blowing is accomplished by selecting the register and mode selection key, followed by the appropriate bit field address, and ending the sequence with a Blow pulse. The Blow mode selection key is a sequence of eleven V<sub>PM</sub> pulses followed by one V<sub>PH</sub> pulse. The Blow pulse consists of a V<sub>PH</sub> pulse of sufficient duration (t<sub>BLOW</sub>) to permanently set an addressed bit by blowing a fuse internal to the device. The device power must be cycled after each individual fuse is blown.

Due to power requirements, a 0.1 μF blowing capacitor (C<sub>BLOW</sub>) must be mounted between the VCC pin and the GND pin during programming, to ensure enough current is available to blow fuses. If programming in the application, C<sub>BYPASS</sub> (see Figure 1) can serve the same purpose.

The fuse for each bit in the bit field must be blown individually. The A1162 built-in circuitry allows only one fuse at a time to be blown. During Blow mode, the bit field can be considered a “one-hot” shift register. Table 2 illustrates how to relate the number of V<sub>PM</sub> pulses to the binary and decimal value for Blow mode bit field addressing. It should be noted that the simple relationship between the number of V<sub>PM</sub> pulses and the required code is:

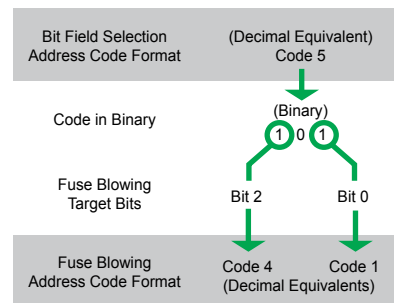
$$2^n = Code,$$

where n is the number of V<sub>PM</sub> pulses, and the bit field has an initial state of decimal code 1 (binary 00000001). To correctly blow

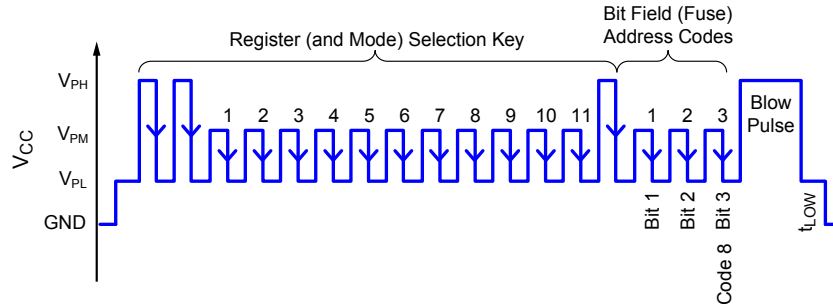
the required fuses, the code representing the required parameter value must be translated to a binary number. For example, as shown in Figure 9, decimal code 5 is equivalent to the binary number 101. Therefore bit 2 must be addressed and blown, the device power supply cycled, and then bit 0 must be addressed and blown. The order of blowing bits, however, is not important. Blowing bit 0 first, and then bit 2 is acceptable. A complete example is shown in Figure 10.

**Table 2: Blow Mode Bit Field Addressing**

Quantity of V <sub>PM</sub> Pulses	Binary Register Bit Field	Decimal Equivalent Code
0	0000 0001	1
1	0000 0010	2
2	0000 0100	4
3	0000 1000	8
4	0001 0000	16
5	0010 0000	32
6	0100 0000	64



**Figure 9: Example of Code 5 Broken into Its Binary Components**



**Figure 10: Example of Blow Mode Programming Pulses Applied to the VCC Pin**

In this example, the  $B_{OP}$  Magnitude Selection register (BOPSEL) is addressed to code 8 (bit 3, or 3  $V_{PM}$  pulses) and its value is permanently blown.

Note: After blowing, the programming is not reversible, even after cycling the supply power. Although a register bit field fuse cannot be reset after it is blown, additional bits within the same register can be blown at any time until the device is locked. For example, if bit 1 (binary 10) has been blown, it is still possible to blow bit 0. The end result would be binary 11 (decimal code 3).

## LOCKING THE DEVICE

After the required code for each parameter is programmed, the device can be locked to prevent further programming of any parameters. To do so, perform the following steps:

1. Ensure that the  $C_{BLOW}$  capacitor is mounted.
2. Select the Output/Lock Bit register key.
3. Select Blow mode selection key.
4. Address bit 4 (10000) by sending four  $V_{PM}$  pulses.

5. Send one Blow pulse, at  $I_{PP}$  and  $SR_{BLOW}$ , and sustain it for  $t_{BLOW}$ .
6. Delay for a  $t_{LOW}$  interval, then power-down.
7. Optionally check all fuses.

## FUSE CHECKING

Incorporated in the A1162 is circuitry to simultaneously check the integrity of the fuse bits. The fuse-checking feature is enabled by using the Fuse Checking registers, and while in Try mode, applying the codes shown in Table 3. The register is only valid in Try mode and is available before or after the programming LOCK bit is set.

Selecting the Fuse Threshold High register checks that all blown fuses are properly blown. Selecting the Fuse Threshold Low register checks all un-blown fuses are properly intact. The supply current ( $I_{CC}$ ) increases by  $250 \mu A$  if a marginal fuse is detected. If all fuses are correctly blown or fully intact, there will be no change in supply current.

**Table 3: Programming Logic Table**

Register Name (Selection Key)	Bit Field Address (Code)		Notes
	Binary (MSB → LSB)	Decimal Equivalent	
<b>TRY MODE REGISTER SELECTION: any VPM pulse after the register selection sequence will move the counter and change the selected register code</b>			
B <sub>OP</sub> Trim Up-Counting [2 × V <sub>PH</sub> ]	000000 111111	0 63	Increases B <sub>OP</sub> . Code 1 automatically selected when register entered; wraps back to code 0.
B <sub>OP</sub> Trim Down-Counting [2 × V <sub>PH</sub> → 4 × V <sub>PM</sub> → V <sub>PH</sub> ]	111111 000000	63 0	Decreases B <sub>OP</sub> . Code 63 automatically selected when register entered; wraps back to code 0.
B <sub>OP</sub> Trim Up-Counting, Bit Wise [2 × V <sub>PH</sub> → 9 × V <sub>PM</sub> → V <sub>PH</sub> ]	000000 000001 000010 000100 001000 010000 100000	0 1 2 4 8 16 32	Bit 1 automatically selected when register entered.
B <sub>HYS</sub> Trim [V <sub>PH</sub> → 3 × V <sub>PM</sub> → V <sub>PH</sub> ]	00 11	0 3	Code 1 automatically selected when register entered.
Parity Bit [V <sub>PH</sub> → V <sub>PM</sub> → V <sub>PH</sub> ]	0	0	Code 1 automatically selected when register entered.
Fuse Threshold Low [V <sub>PH</sub> → 3 × V <sub>PM</sub> → V <sub>PH</sub> → 7 × V <sub>PM</sub> ]			Checks un-blown fuses.
Fuse Threshold High [V <sub>PH</sub> → 3 × V <sub>PM</sub> → V <sub>PH</sub> → 8 × V <sub>PM</sub> ]			Checks blown fuses.
<b>BLOW MODE REGISTER SELECTION</b>			
B <sub>OP</sub> Selection [2 × V <sub>PH</sub> → 11 × V <sub>PM</sub> → V <sub>PH</sub> → (n) × V <sub>PM</sub> → V <sub>PH_BLOW</sub> ]	000000 111111	0 63	B <sub>OP</sub> magnitude selection. Code 0 = B <sub>OP(min)</sub> (default – no fuse blowing required.) Code 63 = B <sub>OP(max)</sub>
B <sub>HYS</sub> Selection [V <sub>PH</sub> → 3 × V <sub>PM</sub> → V <sub>PH</sub> → 11 × V <sub>PM</sub> → V <sub>PH</sub> → (n) × V <sub>PM</sub> → V <sub>PH_BLOW</sub> ]	00 11	0 3	B <sub>HYS</sub> magnitude selection. Code 0 = B <sub>HYS(min)</sub> (default – no fuse blowing required) Code 3 = B <sub>HYS(max)</sub>
Parity Bit [V <sub>PH</sub> → V <sub>PM</sub> → V <sub>PH</sub> → 11 × V <sub>PM</sub> → V <sub>PH</sub> → V <sub>PH_BLOW</sub> ]	0	0	Blow decision is made automatically.
Lock Bit [V <sub>PH</sub> → 3 × V <sub>PM</sub> → V <sub>PH</sub> → 11 × V <sub>PM</sub> → V <sub>PH</sub> → 4 × V <sub>PM</sub> → V <sub>PH_BLOW</sub> ]			Locks access to B <sub>OP</sub> and B <sub>HYS</sub> selection registers.

## ADDITIONAL GUIDELINES

The additional guidelines in this section should be followed to ensure the proper behavior of these devices:

- The power supply used for programming must be capable of delivering at least  $V_{PH}$  and 175 mA.
- Be careful to observe the  $t_{LOW}$  delay time before powering down the device after blowing each bit.
- Set the LOCK bit (only after all other parameters have been programmed and validated) to prevent any further programming of the device.

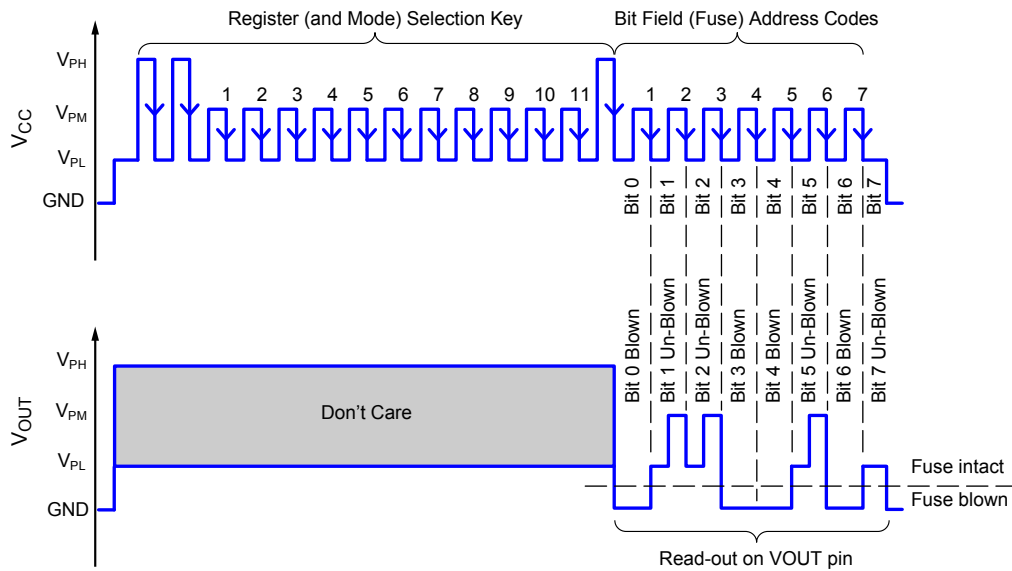
## READ MODE

The A1162 features a Read mode that allows the status of each programmable fuse to be read back individually. The status, blown or not blown, of the addressed fuse is determined by moni-

toring the state of the VOUT pin. A complete example is shown in Figure 11.

Read mode uses the same register selection keys as Blow mode (see Table 3), allowing direct addressing of the individual fuses in the BOPSEL register (do not inadvertently send a Blow pulse while in Read mode). After sending the register and mode selection keys, that is, after the falling edge of the final  $V_{PH}$  pulse in the key, the first bit (the LSB) is selected. Each additional  $V_{PM}$  pulse addresses the next bit in the selected register, up to the MSB. Read mode is available only before the LOCK bit has been set.

After the final  $V_{PH}$  key pulse, and after each  $V_{PM}$  address pulse, if  $V_{OUT}$  is low, the corresponding fuse can be considered blown. If the output state is high, the fuse can be considered un-blown. During Read mode VOUT must be pulled high using a pull-up resistor (see  $R_{LOAD}$  in the Typical Application Circuit diagram).



**Figure 11: Read Mode Example**

Pulse sequence for accessing the  $B_{OP}$  Selection register (BOPSEL) and reading back the status of each of the eight bit fields. In this example, the code (blown fuses) is  $2^0 + 2^3 + 2^4 + 2^6 = 89$  (0101 1001). After each address pulse is sent, the voltage on the VOUT pin will be at GND for blown fuses and at  $V_{CC}$  (at  $V_{PL}$  or  $V_{PM}$ ) for un-blown fuses.

## B<sub>OP</sub> SELECTION

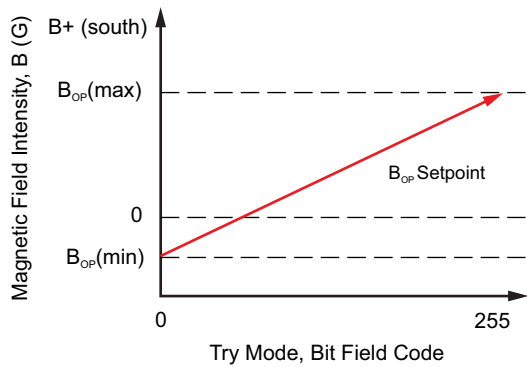
The A1162 allows accurate trimming of the magnetic operate point (B<sub>OP</sub>) within the application. This programmable feature reduces effects due to mechanical placement tolerances and improves performance when used in proximity or vane sensing applications.

B<sub>OP</sub> can be set to any value within the range allowed by the BOPSEL registers. However, switching is recommended only within the Programmable B<sub>OP</sub> Range, specified in the Operating Characteristics table.

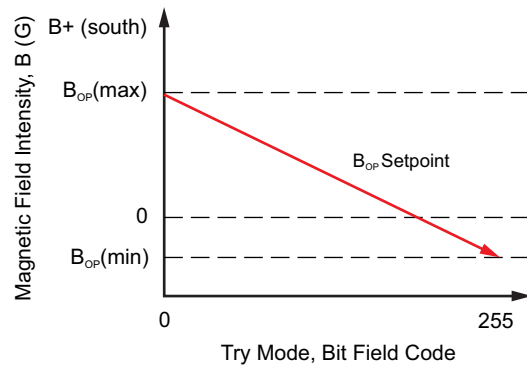
Trimming of B<sub>OP</sub> is typically done in two stages. In the first

stage, B<sub>OP</sub> is adjusted temporarily using the Try mode programming features, to find the fuse value that corresponds to the optimum B<sub>OP</sub>. After a value is determined, then it can be permanently set using the Blow mode features.

As an aid to programming, the A1162 has two options available in Try Mode for adjusting the B<sub>OP</sub> parameter. As shown in Figure 12, this allows the B<sub>OP</sub> parameter to either trim-up (i.e., start at the B<sub>OP</sub> minimum value and increase to the maximum value) or trim-down (i.e., start at the B<sub>OP</sub> maximum value and decrease to the minimum value).



(A) B<sub>OP</sub>, Trim Up-Counting Register



(B) B<sub>OP</sub>, Trim Down-Counting Register

**Figure 12: B<sub>OP</sub> Profiles for Each of the B<sub>OP</sub> Selection Virtual Registers Available in Try Mode.**

## Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for switch point accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionately small relative to the offset that can be produced at the output of the Hall sensor IC. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges. Chopper stabilization is a proven approach used to minimize Hall offset on the chip.

The Allegro technique, namely Dynamic Quadrature Offset Cancellation, removes key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain through modulation.

The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum at baseband, while the DC offset becomes a high-frequency signal. The magnetic signal then can pass through a low-pass filter, while the modulated DC offset is suppressed. The chopper stabilization technique uses a high frequency clock, generally at hundreds of kilohertz. A sample-and-hold technique is used for demodulation, where the sampling is performed at

twice the chopper frequency. This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.

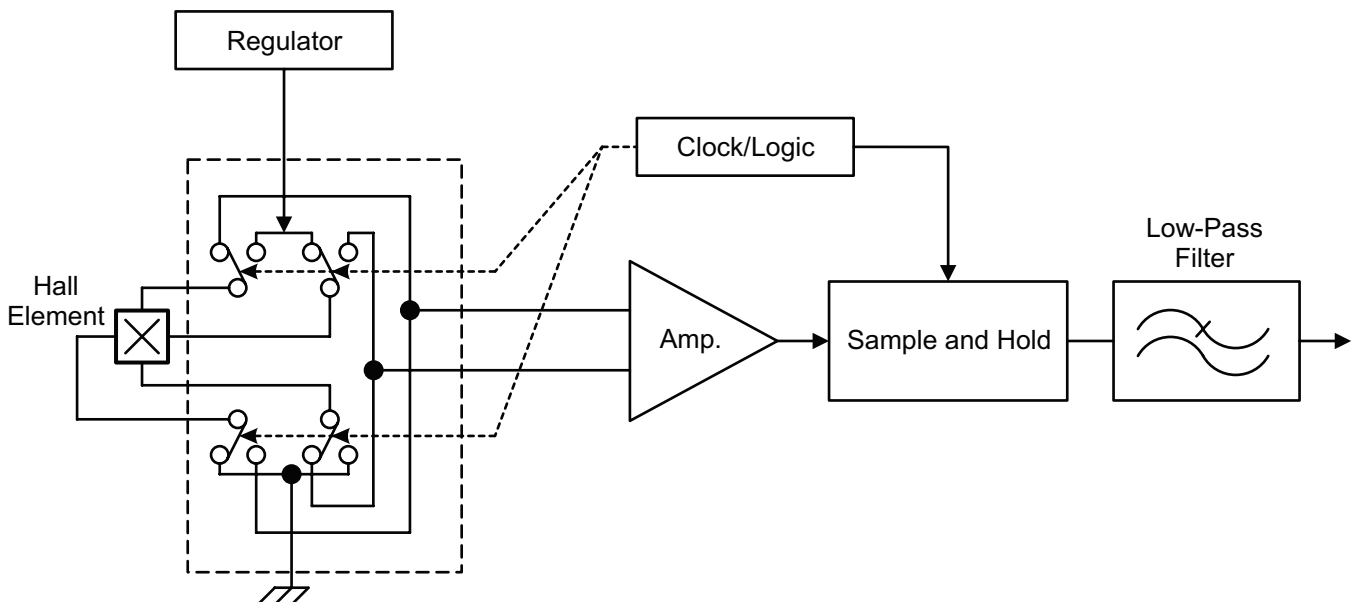


Figure 13: Model of Chopper Stabilization Circuit

## POWER DERATING

The device must be operated below the maximum junction temperature of the device ( $T_{J(max)}$ ). Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating  $T_J$ . (Thermal data is also available on the Allegro MicroSystems website.)

The Package Thermal Resistance ( $R_{\theta JA}$ ) is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity (K) of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case ( $R_{\theta JC}$ ) is a relatively small component of  $R_{\theta JA}$ . Ambient air temperature ( $T_A$ ) and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation,  $P_D$ ), can be estimated. The following formulas represent the fundamental relationships used to estimate  $T_J$ , at  $P_D$ .

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as:  $T_A = 25^\circ C$ ,  $V_{IN} = 12 V$ ,  $I_{IN} = 5 mA$ , and  $R_{\theta JA} = 145^\circ C/W$ , then:

$$P_D = V_{IN} \times I_{IN} = 12 V \times 5 mA = 60 mW$$

$$\Delta T = P_D \times R_{\theta JA} = 60 mW \times 145^\circ C/W = 8.7^\circ C$$

$$T_J = T_A + \Delta T = 25^\circ C + 8.7^\circ C = 33.7^\circ C$$

For 5 V  $\pm 5\%$  systems, in diagnostic mode:  $R_{\theta JA} = 145^\circ C/W$ ,  $T_{J(max)} = 165^\circ C$ ,  $V_{CC} = 5.25 V$ , and  $I_{CC(DIAG)max} = 25 mA$ .

Calculate the maximum allowable power level with equation 1:

$$P_{D(max)} = V_{CC} \times I_{CC(DIAG)max} = 5.25 V \times 25 mA = 131.25 mW$$

Then determine the allowable increase to temperature with equation 2:

$$\Delta T_{max} = P_{D(max)} \times R_{\theta JA} = 131.25 mW \times 145^\circ C/W = 19^\circ C$$

Finally, inverting equation 3 results in the maximum ambient temperature:

$$T_{A(max)} = T_{J(max)} - \Delta T_{max} = 165^\circ C - 19^\circ C = 146^\circ C$$

A worst-case estimate,  $P_{D(max)}$ , represents the maximum allowable power level, without exceeding  $T_{J(max)}$ , at a selected  $R_{\theta JA}$  and  $T_A$ .

*Example:* Reliability for  $V_{CC}$  at  $T_A = 150^\circ C$ , package LE, using a 4-layer PCB.

Observe the worst-case ratings for the device, specifically:  $R_{\theta JA} = 145^\circ C/W$ ,  $T_{J(max)} = 165^\circ C$ ,  $V_{CC(max)} = 24 V$ , and  $I_{CC(max)} = 5 mA$ .

Calculate the maximum allowable power level ( $P_{D(max)}$ ). First, invert equation 3:

$$\Delta T_{max} = T_{J(max)} - T_A = 165^\circ C - 150^\circ C = 15^\circ C$$

This provides the allowable increase to  $T_J$  resulting from internal power dissipation. Then, invert equation 2:

$$P_{D(max)} = \Delta T_{max} \div R_{\theta JA} = 15^\circ C \div 145^\circ C/W = 103 mW$$

Finally, invert equation 1 with respect to voltage:

$$V_{CC(est)} = P_{D(max)} \div I_{CC(max)} = 103 mW \div 5 mA = 20.6 V$$

The result indicates that, at  $T_A$ , the application and device can dissipate adequate amounts of heat at voltages  $\leq V_{CC(est)}$ .

Compare  $V_{CC(est)}$  to  $V_{CC(max)}$ . If  $V_{CC(est)} \leq V_{CC(max)}$ , then reliable operation between  $V_{CC(est)}$  and  $V_{CC(max)}$  requires enhanced  $R_{\theta JA}$ . If  $V_{CC(est)} \geq V_{CC(max)}$ , then operation between  $V_{CC(est)}$  and  $V_{CC(max)}$  is reliable under these conditions.

## PACKAGE OUTLINE DRAWING

### For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000381, Rev. 1 and JEDED MO-153AA)

Dimensions in millimeters - NOT TO SCALE

Dimensions exclusive of mold flash, gate burrs, and dambar protrusions

Exact case and lead configuration at supplier discretion within limits shown

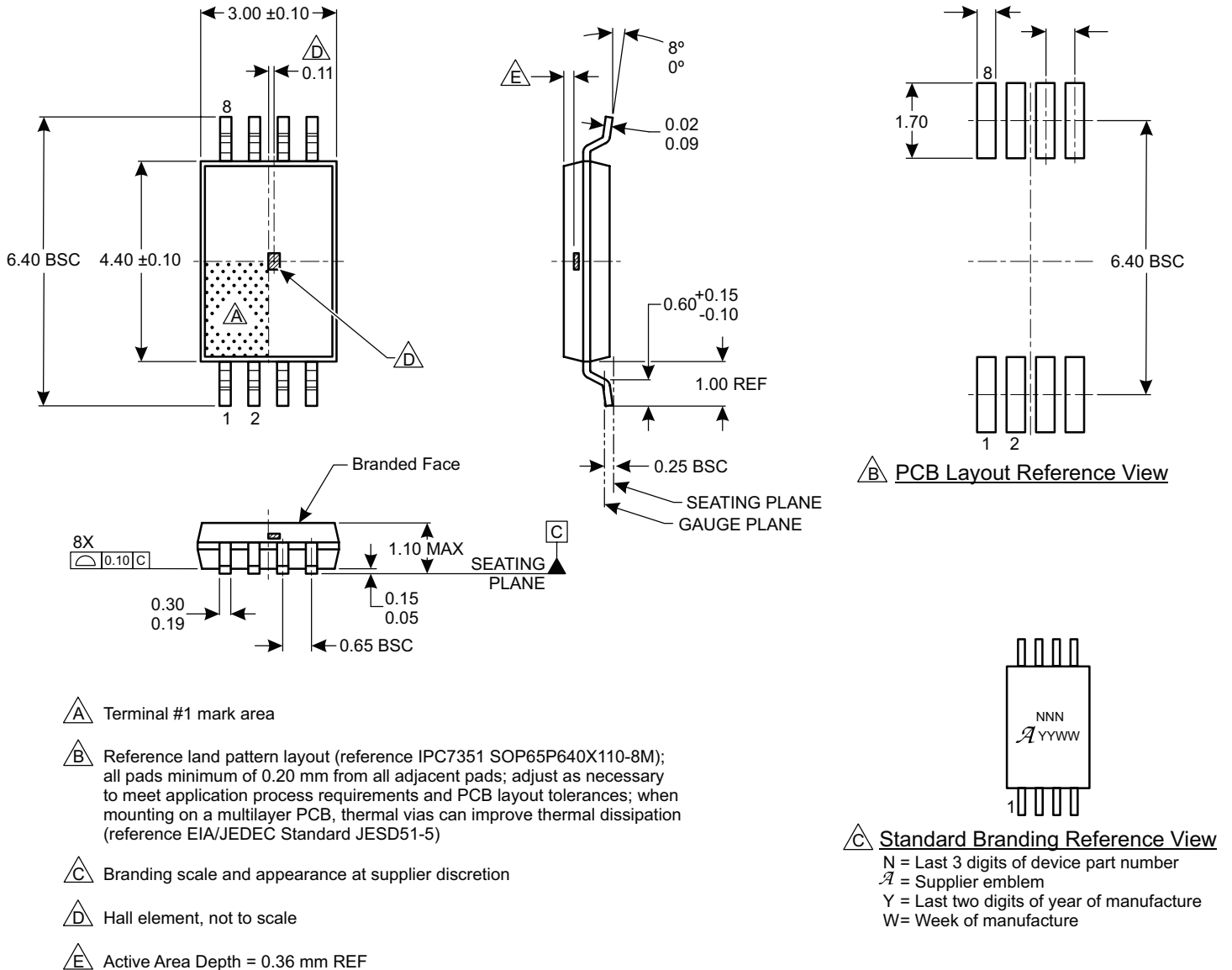


Figure 14: Package LE, 8-Pin eTSSOP

## Revision History

Revision	Revision Date	Description of Revision
–	January 27, 2016	Initial Release
1	February 4, 2019	Minor editorial updates
2	February 21, 2020	Minor editorial updates
3	February 18, 2022	Updated package drawing reference number (page 22) and other minor editorial updates
4	September 11, 2023	Removed ASIL (page 1); fixed broken links (pages 12-13)

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