



**THE DATASHEET OF  
A1193LLHLT-T**



## Programmable, Chopper-Stabilized, Two-Wire Hall-Effect Switches

### FEATURES AND BENEFITS

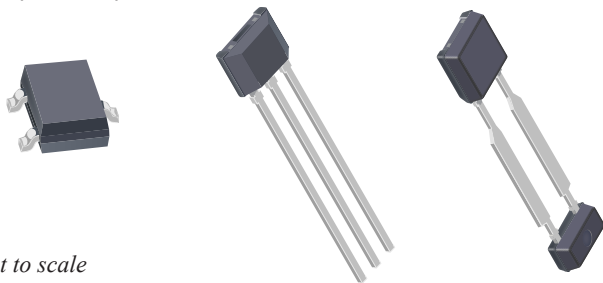
- Choice of factory-set temperature coefficient (TC) for use with ferrite or rare-earth magnets
- Field programmable for optimized switchpoints
- AEC-Q100 automotive qualified
  - On-board voltage regulator: 3 to 24 V operation
- High-speed, 4-phase chopper stabilization
  - Low switchpoint drift throughout temperature range
  - Low sensitivity to thermal and mechanical stresses
- On-chip protection
  - Supply transient protection
  - Reverse-battery protection
  - Industry-leading ISO 7637-2 performance through use of proprietary, 40 V clamping structure
- Solid-state reliability
- Robust EMC and ESD performance
- UB package with integrated 0.1  $\mu\text{F}$  bypass capacitor

### PACKAGES

**3-pin SOT23-W**  
2 mm × 3 mm × 1 mm (suffix LH)

**3-pin ultramini SIP**  
1.5 mm × 4 mm × 3 mm (suffix UA)

**2-pin ultramini SIP**  
1.5 mm × 4 mm × 4 mm (suffix UB)



Not to scale

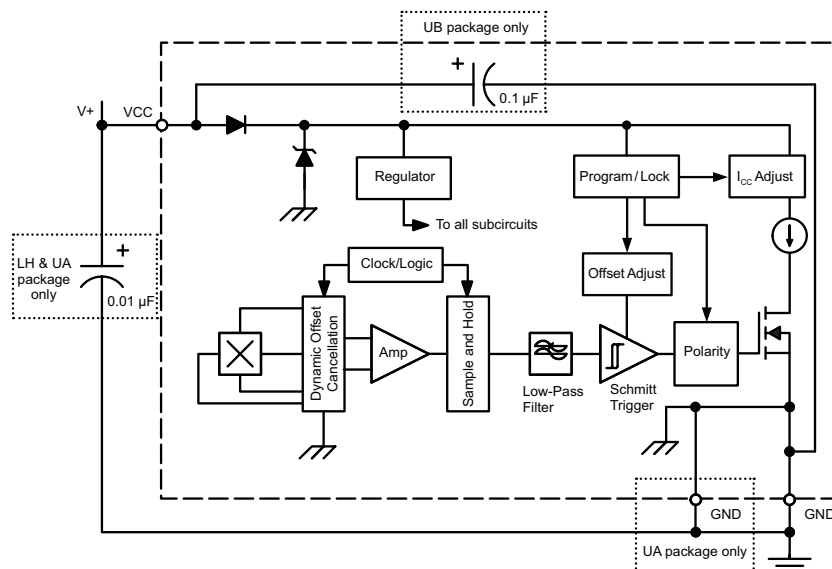
### DESCRIPTION

The A119x and A119x-F comprise a family of two-wire, unipolar, Hall-effect switches, which can be trimmed by the user at end-of-line to optimize magnetic switchpoint accuracy in the application. The latter (-F option) are temperature-compensated for use with ferrite magnets. These devices are produced on the Allegro™ advanced BiCMOS wafer fabrication process, which implements a high-frequency, 4-phase, chopper stabilization technique. This technique achieves magnetic stability over the full operating temperature range, and eliminates offsets inherent in devices with a single Hall element that are exposed to harsh application environments.

The A119x and A119x-F family has a number of automotive applications. These include sensing seat track position, seat belt buckle presence, hood/trunk latching, and shift selector position.

Two-wire unipolar switches are particularly advantageous in cost-sensitive applications because they require one less wire for operation versus the more traditional open-collector output switches. Additionally, the system designer inherently gains diagnostics because there is always output current flowing, which should be in either of two narrow ranges. Any current level not within these ranges indicates a fault condition.

All family members are offered in three package styles. The LH is a SOT-23W style, miniature, low-profile package for surface-mount applications. The UA is a 3-pin, ultra-mini, single inline package (SIP) for through-hole mounting. The UB is a 2-pin single inline package (SIP) for through-hole mounting that integrates the power supply decoupling capacitor. All three packages are lead (Pb) free, with 100% matte-tin leadframe plating.



Functional Block Diagram

## SELECTION GUIDE

Part Number	Package	Packing [1]	Temperature Coefficient	Output ( $I_{CC}$ ) in South Polarity Field	Supply Current at $I_{CC(L)}$ (mA)	Magnetic Operate Point, $B_{OP}$ (G)
A1190LLHLT-T [2]	LH (3-pin SOT23-W surface-mount)	7-in. reel, 3000 pieces/reel	SmCo	Low	2 to 5	10 to 200
A1190LLHLX-T	LH (3-pin SOT23-W surface-mount)	13-in. reel, 10000 pieces/reel	SmCo			
A1190LUA-T [3]	UA (3-pin SIP through-hole)	Bulk, 500 pieces/bag	SmCo			
A1190LUBTN-T	UB (2-pin SIP through-hole)	13-in. reel, 4000 pieces/reel	SmCo			
A1192LLHLT-T [2]	LH (3-pin SOT23-W surface-mount)	7-in. reel, 3000 pieces/reel	SmCo			
A1192LLHLT-F-T [2]	LH (3-pin SOT23-W surface-mount)	7-in. reel, 3000 pieces/reel	Ferrite			
A1192LLHLX-T	LH (3-pin SOT23-W surface-mount)	13-in. reel, 10000 pieces/reel	SmCo		5 to 6.9	
A1192LLHLX-F-T	LH (3-pin SOT23-W surface-mount)	13-in. reel, 10000 pieces/reel	Ferrite			
A1192LUA-T [3]	UA (3-pin SIP through-hole)	Bulk, 500 pieces/bag	SmCo			
A1192LUA-F-T [3]	UA (3-pin SIP through-hole)	Bulk, 500 pieces/bag	Ferrite			
A1192LUBTN-T	UB (2-pin SIP through-hole)	13-in. reel, 4000 pieces/reel	SmCo			
A1192LUBTN-F-T	UB (2-pin SIP through-hole)	13-in. reel, 4000 pieces/reel	Ferrite			
A1193LLHLT-T [2]	LH (Surface mount)	7-in. reel, 3000 pieces/reel	SmCo	High	5 to 6.9	
A1193LLHLT-F-T [2]	LH (Surface mount)	7-in. reel, 3000 pieces/reel	Ferrite			
A1193LLHLX-T	LH (Surface mount)	13-in. reel, 10000 pieces/reel	SmCo			
A1193LLHLX-F-T	LH (Surface mount)	13-in. reel, 10000 pieces/reel	Ferrite			
A1193LUA-T [3]	UA (3-pin SIP through-hole)	Bulk, 500 pieces/bag	SmCo			
A1193LUA-F-T [3]	UA (3-pin SIP through-hole)	Bulk, 500 pieces/bag	Ferrite			
A1193LUBTN-T	UB (2-pin SIP through-hole)	13-in. reel, 4000 pieces/reel	SmCo			
A1193LUBTN-F-T	UB (2-pin SIP through-hole)	13-in. reel, 4000 pieces/reel	Ferrite			

[1] Contact Allegro™ for additional packing options.

[2] These variants available only through authorized distributors.

[3] Contact factory for availability.



## SPECIFICATIONS

## ABSOLUTE MAXIMUM RATINGS

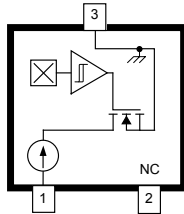
Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	$V_{CC}$		28	V
Reverse Supply Voltage	$V_{RCC}$		-18	V
Magnetic Flux Density	B		Unlimited	G
Operating Ambient Temperature	$T_A$	Range L	-40 to 150	°C
Maximum Junction Temperature	$T_J(\text{max})$		165	°C
Storage Temperature	$T_{\text{stg}}$		-65 to 170	°C

## INTERNAL DISCRETE CAPACITOR RATINGS (UB PACKAGE ONLY)

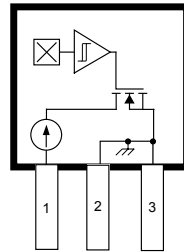
Characteristic	Symbol	Notes	Rating	Unit
Rated Normal Capacitance	$C_{\text{SUPPLY}}$	Connected between VCC and GND	0.1	$\mu\text{F}$
Rated Voltage	$V_{\text{CSUPPLY}}$		50	V
Rated Capacitor Tolerance			$\pm 10$	%
Temperature Designator			X7R	-

PINOUT DIAGRAMS AND TERMINAL LIST TABLE

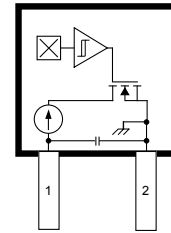
Pinout Diagrams



LH Package [1]



UA Package



UB Package

Terminal List Table

Number	Name			Function
	LH package [1]	UA package	UB package	
1	VCC	VCC	VCC	Connects power supply to chip; used to apply programming signal
2	NC	GND	GND	LH package: no connection, it is highly recommended that this pin be tied to GND UA, UB package: ground terminal
3	GND	GND	–	Ground terminal

[1] Package style LH pin 2 is not internally connected to the IC ground and therefore should not be used as a ground reference pin. For maximum EMC and ESD robustness it is highly recommended that this pin be tied to ground.

PROGRAMMABLE PARAMETERS

Name	Functional Description	Quantity of Bits
B <sub>OP</sub> Trim	Fine trim of Programmable Magnetic Operating Point	6
Programming Lock	Lock access to programming	1

**ELECTRICAL CHARACTERISTICS:** Valid at  $T_A = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ,  $T_J < T_J(\text{max})$ , through operating supply voltage range, unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Supply Voltage <sup>[1]</sup>	$V_{CC}$	Operating, $T_J \leq 165^\circ\text{C}$		3	–	24	V
Supply Current	$I_{CC(L)}$	A1190	$B > B_{OP}$	2	–	5	mA
		A1192, A1192-F	$B > B_{OP}$	5	–	6.9	mA
		A1193, A1193-F	$B < B_{RP}$	5	–	6.9	mA
	$I_{CC(H)}$	A1190, A1192, A1192-F	$B < B_{RP}$	12	–	17	mA
		A1193, A1193-F	$B > B_{OP}$	12	–	17	mA
Supply Zener Clamp Voltage	$V_{Z(sup)}$	$I_{CC} = I_{CC(L)}(\text{max}) + 3 \text{ mA}$ , $T_A = 25^\circ\text{C}$		28	–	–	V
Supply Zener Clamp Current	$I_{Z(sup)}$	$V_{Z(sup)} = 28 \text{ V}$		–	–	$I_{CC(L)}(\text{max}) + 3 \text{ mA}$	mA
Reverse Supply Current	$I_{RCC}$	$V_{RCC} = -18 \text{ V}$		–	–	-1.6	mA
Output Slew Rate	di/dt	LH, UA package (no bypass capacitor <sup>[2]</sup> ); capacitance of probe $C_S = 20 \text{ pF}$		–	90	–	mA/ $\mu\text{s}$
		UB package (integrated capacitor <sup>3</sup> ); capacitance of probe $C_S = 20 \text{ pF}$		–	0.22	–	mA/ $\mu\text{s}$
Chopping Frequency	$f_C$			–	700	–	kHz
Power-Up Time <sup>[4]</sup>	$t_{on}$	LH, UA packages: A1190, A1192, A1192-F	$C_{BYP} = 0.01 \mu\text{F}$ , $B > B_{OP} + 10 \text{ G}$	–	–	25	$\mu\text{s}$
		UB package <sup>3</sup> : A1190, A1192, A1192-F	$B > B_{OP} + 10 \text{ G}$	–	–	25	$\mu\text{s}$
		LH, UA packages: A1193, A1193-F	$C_{BYP} = 0.01 \mu\text{F}$ , $B < B_{RP} - 10 \text{ G}$	–	–	25	$\mu\text{s}$
		UB package <sup>3</sup> : A1193, A1193-F	$B < B_{RP} - 10 \text{ G}$	–	–	25	$\mu\text{s}$
Power-Up State <sup>[5][6]</sup>	POS	$t_{on} < t_{on}(\text{max})$ , $V_{CC}$ slew rate $> 25 \text{ mV}/\mu\text{s}$		–	$I_{CC(H)}$	–	–

<sup>[1]</sup>  $V_{CC}$  represents the generated voltage between the VCC pin and the GND pin.

<sup>[2]</sup> Measured without bypass capacitor between VCC pin and the GND pin. Use of a bypass capacitor results in slower current change.

<sup>[3]</sup> Measured with internal bypass capacitor (0.1  $\mu\text{F}$ ) between VCC and GND. Additional bypass capacitance results in slower current change.

<sup>[4]</sup> Guaranteed by characterization and design.

<sup>[5]</sup> Power-Up State as defined is true only with a  $V_{CC}$  slew rate of 25 mV/ $\mu\text{s}$  or greater.

<sup>[6]</sup> For  $t > t_{on}$  and  $B_{RP} < B < B_{OP}$ , Power-Up State is not defined.

**MAGNETIC CHARACTERISTICS** <sup>[1]</sup>: Valid at  $T_A = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ,  $T_J \leq T_J(\text{max})$ , unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit <sup>[2]</sup>
Initial Operate Point	$B_{OP(\text{init})}$			–	-14	10	G
Programmable Magnetic Operating Point	$B_{OP}$	$T_A = 25^\circ\text{C}$		10	–	200	G
Average Magnetic Step Size <sup>[3]</sup>	$\text{STEP}_{BOP}$	$T_A = 25^\circ\text{C}$ , $V_{CC} = 5 \text{ V}$		3	4.8	7.5	G
Switchpoint Temperature Drift	$\Delta B_{OP}$	A1190, A1192, A1193		–	$\pm 20$	–	G
		A1192-F, A1193-F	10 to 200 G	–	-0.25	–	%/ $^\circ\text{C}$
Hysteresis	$B_{HYS}$			5	–	30	G

<sup>[1]</sup> Relative values of B use the algebraic convention, where positive values indicate south magnetic polarity, and negative values indicate north magnetic polarity; therefore greater B values indicate a stronger south polarity field (or a weaker north polarity field, if present).

<sup>[2]</sup> 1 G (gauss) = 0.1 mT (millitesla).

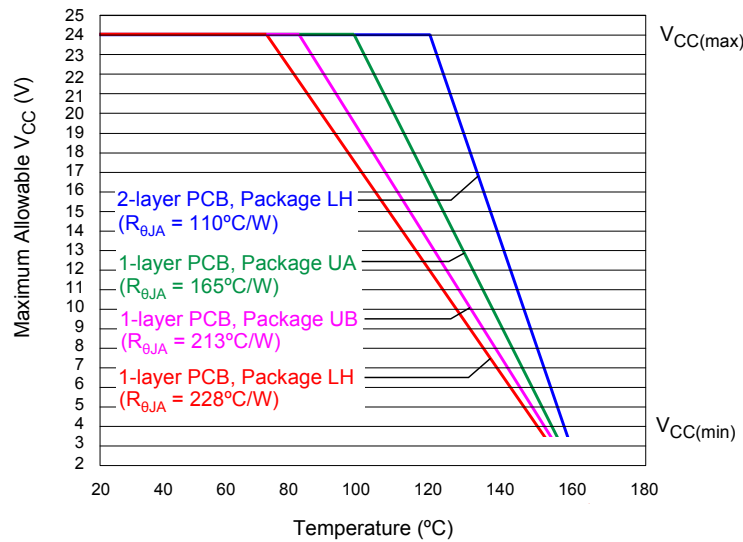
<sup>[3]</sup>  $\text{STEP}_{BOP}$  is a calculated average from the cumulative programmed bits.

**THERMAL CHARACTERISTICS:** May require derating at maximum conditions; see application information

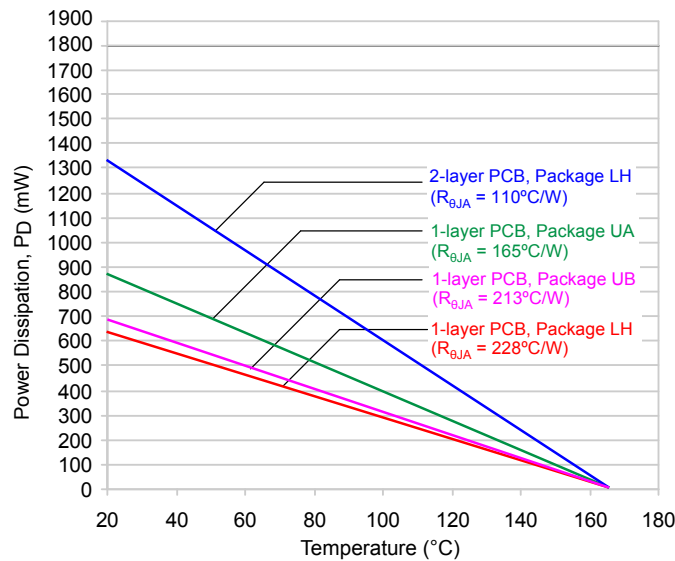
Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	Package LH, on 1-layer PCB based on JEDEC standard	228	°C/W
		Package LH, on 2-layer PCB with 0.463 in. <sup>2</sup> of copper area each side	110	°C/W
		Package UA, on 1-layer PCB with copper limited to solder pads	165	°C/W
		Package UB, on 1-layer PCB with copper limited to solder pads	213	°C/W

\*Additional thermal information available on the Allegro website.

**Power Derating Curve**

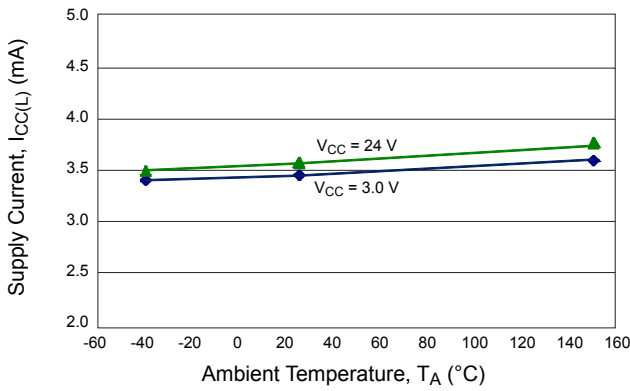


**Power Dissipation vs. Ambient Temperature**

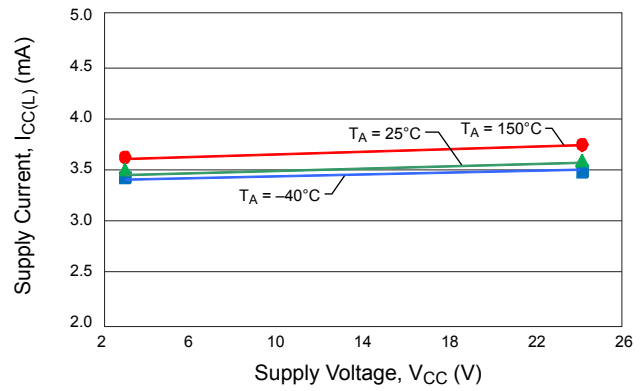


## CHARACTERISTIC PERFORMANCE

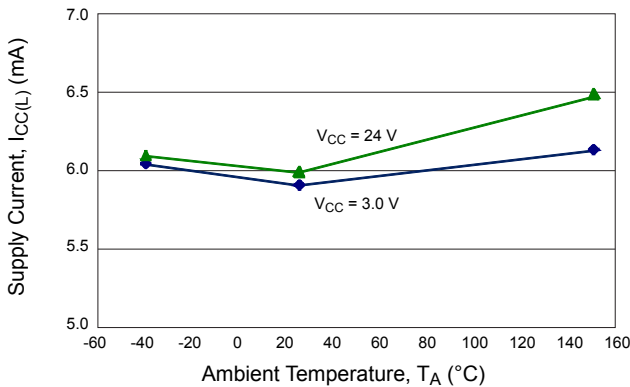
**A1190**  
**Average Supply Current (Low) versus Temperature**



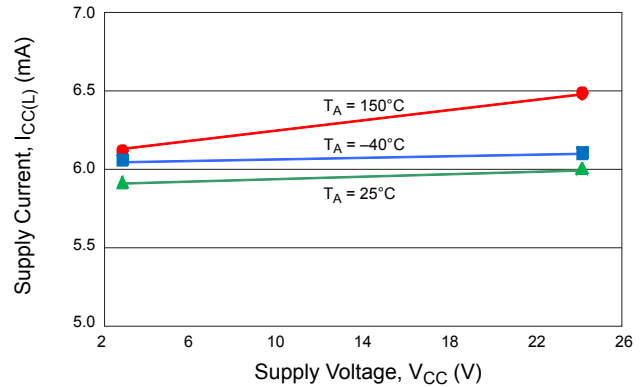
**A1190**  
**Average Supply Current (Low) versus Supply Voltage**



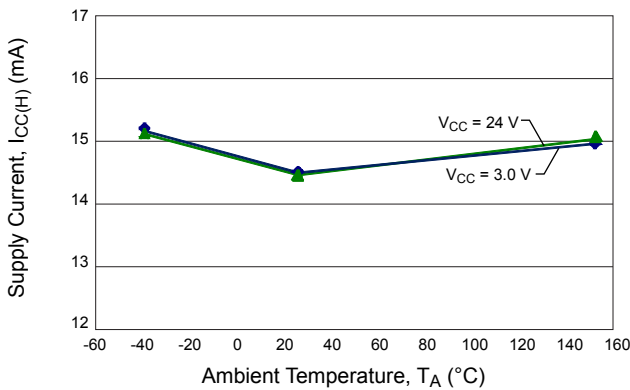
**A1192, A1193**  
**Average Supply Current (Low) versus Temperature**



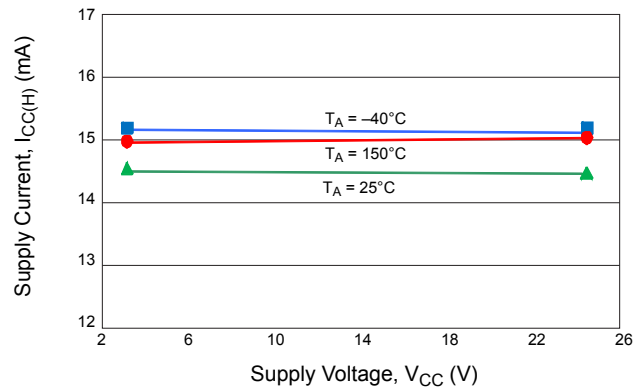
**A1192, A1193**  
**Average Supply Current (Low) versus Supply Voltage**



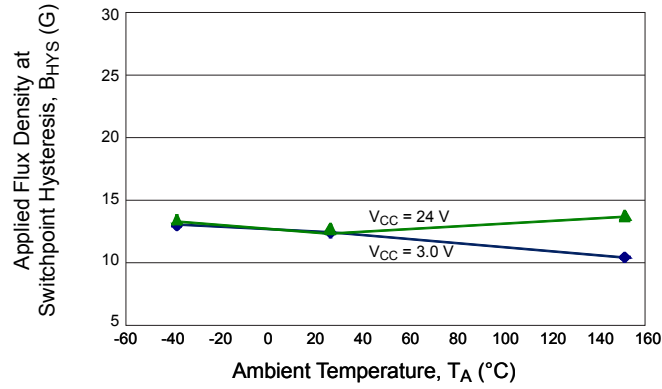
**A1190, A1192, A1193**  
**Average Supply Current (High) versus Temperature**



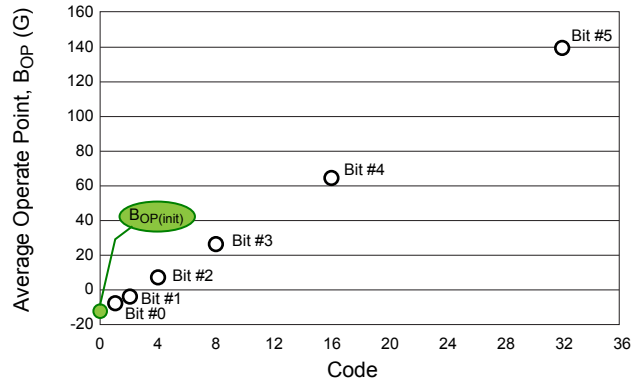
**A1190, A1192, A1193**  
**Average Supply Current (High) versus Supply Voltage**



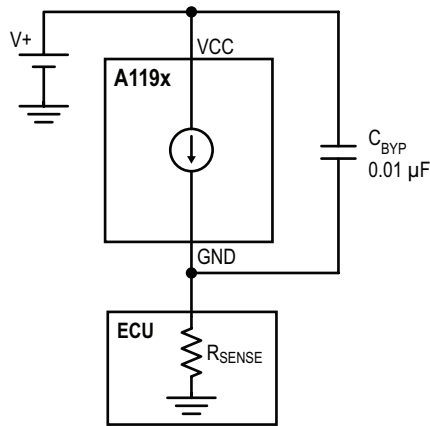
A1190, A1192, A1193  
Average Switchpoint Hysteresis versus Temperature



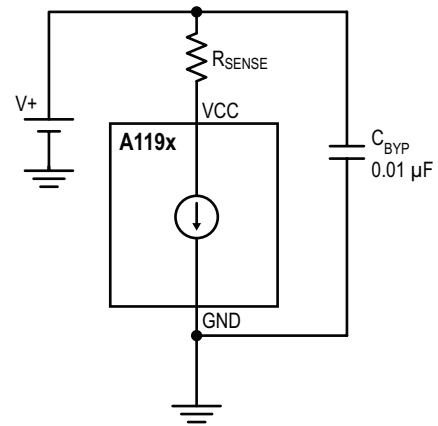
A1190, A1192, A1193  
Average Operate Point versus Code



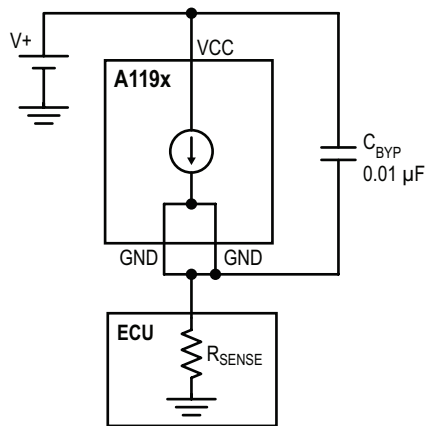




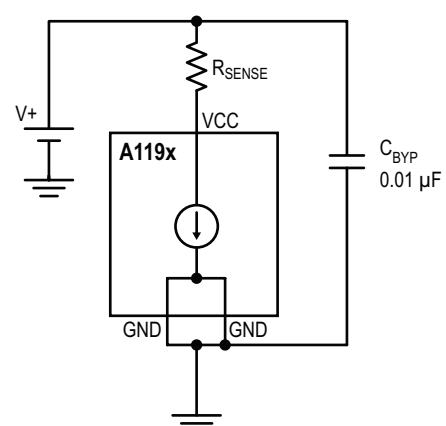
(A) Low-Side Sensing (LH package)



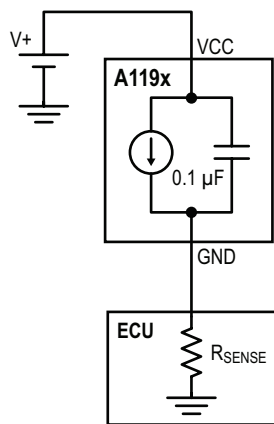
(B) High-Side Sensing (LH package)



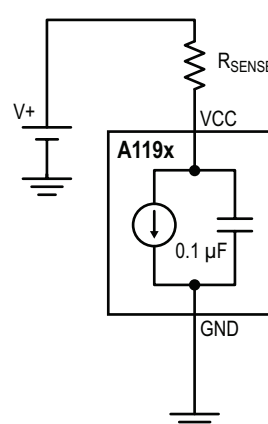
(C) Low-Side Sensing (UA package)



(D) High-Side Sensing (UA package)



(E) Low-Side Sensing (UB package)



(F) High-Side Sensing (UB package)

Figure 2. Typical application circuits

### Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for switchpoint accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionately small relative to the offset that can be produced at the output of the Hall sensor IC. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges. Chopper stabilization is a unique approach used to minimize Hall offset on the chip. The Allegro technique, namely Dynamic Quadrature Offset Cancellation, removes key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum

at base band, while the DC offset becomes a high-frequency signal. The magnetic-sourced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed. The chopper stabilization technique uses a 350 kHz high frequency clock. For demodulation process, a sample and hold technique is used, where the sampling is performed at twice the chopper frequency. This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.

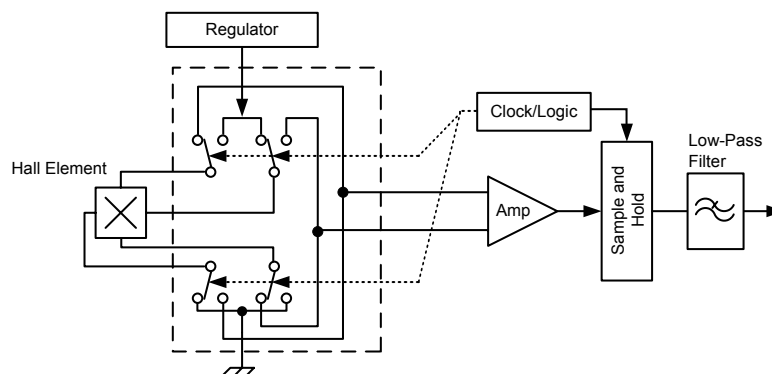


Figure 3. Chopper stabilization circuit (Dynamic Quadrature Offset Cancellation)

## PROGRAMMING GUIDELINES

### Overview

Programming is accomplished by sending a series of input voltage pulses serially through the VCC (supply) pin of the device. A unique combination of different voltage level pulses controls the internal programming logic of the device to select a desired programmable parameter and change its value. There are three voltage levels that must be taken into account when programming. These levels are referred to as *high* ( $V_{PH}$ ), *mid* ( $V_{PM}$ ), and *low* ( $V_{PL}$ ) (see figure 1 and table 1).

The A119x family features two programmable modes, Try mode and Blow mode.

- In Try mode, programmable parameter values are set and measured. A parameter value is stored temporarily, and reset after cycling the supply voltage.
- In Blow mode, the value of a programmable parameter may be permanently set by blowing solid-state fuses internal to the device. Device locking is also accomplished in this mode.

The programming sequence is designed to help prevent the device from being programmed accidentally; for example, as a result of noise on the supply line. Although any programmable variable power supply can be used to generate the pulse waveforms, Allegro highly recommends using the Allegro Sensor IC Evaluation Kit, available through your local Allegro sales representative. The manual for the kit provides additional information on programming these devices, and is available for download on the Allegro MicroSystems website.

### Definition of Terms

**Register.** The section of the programming logic that controls the choice of programmable modes and parameters.

**Bit Field.** The internal fuses unique to each register, represented as a binary number. Changing the bit field selection in a particular register causes its programmable parameter to change, based on the internal programming logic.

**Key.** A series of  $V_{PM}$  voltage pulses used to select a register or mode.

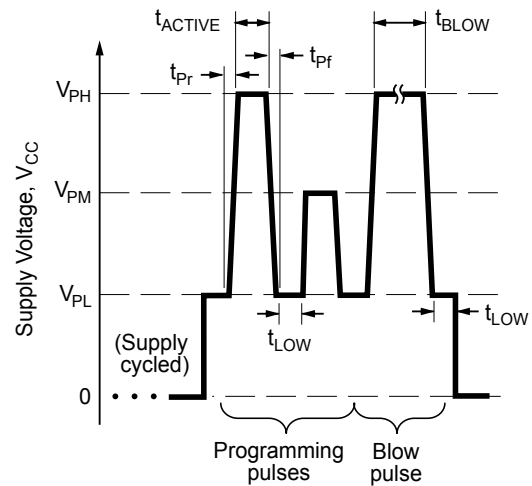


Figure 4. Programming pulse definition (see table 1)

**Table 1. Programming Pulse Requirements, Protocol at  $T_A = 25^\circ\text{C}$  (refer also to figure 4)**

Characteristic	Symbol	Notes	Min.	Typ.	Max.	Unit
Programming Voltage	$V_{PL}$	Measured at the VCC pin.	4.5	5	5.5	V
	$V_{PM}$		12.5	–	14	V
	$V_{PH}$		21	–	27	V
Programming Current	$I_{PP}$	$t_{Pr} = 11 \mu\text{s}$ , $V_{CC} = 5 \rightarrow 26 \text{ V}$ , $C_{BLOW} = 0.1 \mu\text{F}$ (min). Minimum supply current required to ensure proper fuse blowing. $C_{BLOW}$ must be connected between the VCC and GND pins during programming to provide the current necessary for fuse blowing.	175	–	–	mA
Pulse Width	$t_{LOW}$	Duration at $V_{PL}$ separating pulses at $V_{PM}$ or $V_{PH}$ .	20	–	–	$\mu\text{s}$
	$t_{ACTIVE}$	Duration of pulses at $V_{PM}$ or $V_{PH}$ for key/code selection.	20	–	–	$\mu\text{s}$
	$t_{BLOW}$	Duration of pulse at $V_{PH}$ for fuse blowing.	90	100	–	$\mu\text{s}$
Pulse Rise Time	$t_{Pr}$	$V_{PL}$ to $V_{PM}$ , or $V_{PL}$ to $V_{PH}$ .	5	–	100	$\mu\text{s}$
Pulse Fall Time	$t_{Pf}$	$V_{PH}$ to $V_{PL}$ , or $V_{PM}$ to $V_{PL}$ .	5	–	100	$\mu\text{s}$
Blow Pulse Slew Rate	$SR_{BLOW}$		375	–	–	mV/ $\mu\text{s}$

**Code.** The number used to identify the combination of fuses activated in a bit field, expressed as the decimal equivalent of the binary value. The LSB of a bit field is denoted as code 1, or bit 0.

**Addressing.** Setting the bit field code in a selected register by serially applying a pulse train through the VCC pin of the device. Each parameter can be measured during the addressing process, but the internal fuses must be blown before the programming code (and parameter value) becomes permanent.

**Fuse Blowing.** Applying a  $V_{PH}$  pulse of sufficient duration to permanently set an addressed bit by blowing a fuse internal to the device. Once a bit (fuse) has been blown, it cannot be reset.

**Blow Pulse.** A  $V_{PH}$  pulse of sufficient duration to blow the addressed fuse.

**Cycling the Supply.** Powering-down, and then powering-up the supply voltage. Cycling the supply is used to clear the programming settings in Try mode.

## Programming Procedure

Programming involves selection of a register, a mode, and then setting values for parameters in the register for evaluation or for fuse blowing. Figure 10 provides an overview state diagram.

**Register Selection** Each programmable parameter can be accessed through a specific register. To select a register, a sequence of voltage pulses consisting of a  $V_{PH}$  pulse, a series of  $V_{PM}$  pulses, and a  $V_{PH}$  pulse (with no  $V_{CC}$  supply interruptions) must be applied serially to the VCC pin. The quantity of  $V_{PM}$  pulses is called the *key*, and uniquely identifies each register. The pulses for selection of register key 1, is shown in figure 5. No  $V_{PM}$  pulse is sent for key 0. The register selections are shown in table 2.

**Mode Selection** After register selection, the mode is selected, either Try or Blow mode. Try mode is selected by default. To select Blow mode, that mode selection key must be sent.

**Table 2. Programming Logic Table**

Register		Bit Field Address (Code)		Description
Key	Name	Binary Format [MSB → LSB]	Decimal Equivalent	
<b>TRY MODE</b>				
0	B <sub>OP</sub> Trim Up Counting	000000	0	Initial value (below minimum  B <sub>OP</sub>   ) (Try mode sequence starts with code 1); Code corresponds to bit field value (code 1 selects bit field value 000001)
		111111	63	Maximum selectable value (above maximum  B <sub>OP</sub>   )
1	B <sub>OP</sub> Trim Down Counting	111111	0	Initial value (above maximum  B <sub>OP</sub>   ) (Try mode sequence starts with code 1); Code is automatically inverted (code 1 selects bit field value 111110)
		000000	63	Minimum selectable value (below minimum  B <sub>OP</sub>  )
7	Fuse Check	000111	7	Check integrity of all fuse bits versus low threshold
		001111	15	Check integrity of all fuse bits versus high threshold
<b>BLOW MODE</b>				
0	B <sub>OP</sub> Trim	000000	0	Initial value (below minimum  B <sub>OP</sub>   ); (Only allows selection of 1 bit per sequence)
		111111	63	Maximum selectable value (above maximum  B <sub>OP</sub>   ); (Only allows selection of 1 bit per sequence)
7	Programming Lock	001000	8	Locks out access to all registers except Fuse Check

**Try Mode** In Try mode, bit field addressing is accomplished by applying a series of  $V_{PM}$  pulses to the VCC pin of the device, as shown in figure 6. Each pulse increases the bit field value for the selected parameter, increasing by one on the falling edge of each additional  $V_{PM}$  pulse. When addressing the bit field in Try mode, the quantity of  $V_{PM}$  pulses is represented by a decimal number called the *code*. Addressing activates the corresponding fuse locations in the given bit field by increasing the binary value of an internal DAC, up to the maximum possible code. As the value of the bit field code increases, the value of the programmable parameter changes. Measurements can be taken after each  $V_{PM}$  pulse to determine if the required result for the programmable parameter has been reached. Cycling the supply voltage resets all the locations in the bit field that have un-blown fuses to their initial states.

When setting the  $B_{OP}$  Trim parameter, as an aid to programming, values can be traversed from low to high, or from high to low. To accommodate this direction selection, the value of the bit field (and code) defaults to the value 1, on the falling edge of the final register selection  $V_{PH}$  pulse (see figure 5). A complete example is provided in figure 11.

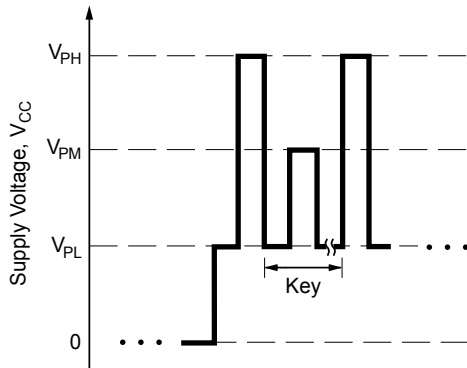


Figure 5. Register selection pulse sequence

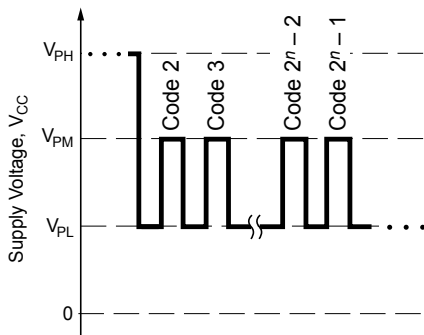


Figure 6. Try mode bit field addressing pulses

**Blow Mode** After the required code is determined for a given parameter, its value can be set permanently by blowing individual fuses in the appropriate register bit field. Blowing is accomplished by selecting the register, then the Blow mode selection key, followed by the appropriate bit field address, and ending the sequence with the Blow pulse. The Blow mode selection key is a sequence of nine  $V_{PM}$  pulses followed by one  $V_{PH}$  pulse. A complete example is provided in figure 12.

The Blow pulse consists of a  $V_{PH}$  pulse of sufficient duration,  $t_{BLOW}$ , to permanently set an addressed bit by blowing a fuse internal to the device. Due to power requirements, the fuse for each bit in the bit field must be blown individually. The A119x family built-in circuitry allows only one fuse at a time to be blown. During Blow mode, the bit field can be considered a “one-hot” shift register. Table 3 relates the quantity of  $V_{PM}$  pulses to the binary and decimal values for Blow mode bit field addressing. It should be noted that the simple relationship between the quantity of  $V_{PM}$  pulses and the corresponding code is:

$$2^n = \text{Code},$$

where n is the quantity of  $V_{PM}$  pulses. The bit field has an initial state of decimal code 0 (binary 000000).

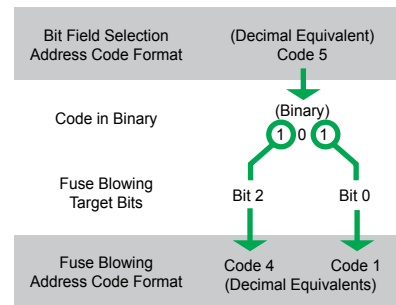


Figure 7. Example of code 5 broken into its binary components

**Table 3. Blow Mode Bit Field Addressing**

Quantity of $V_{PM}$ Pulses	Binary Register Setting	Equivalent Code
1	000001	1
2	000010	2
3	000100	4
4	001000	8
5	010000	16
6	100000	32

To correctly address the fuses to be blown, the code representing the required parameter value must be translated into a binary number. For example, as shown in figure 7, decimal code 5 is equivalent to the binary number 101. Therefore bit 2 must be addressed and blown, the device power supply cycled, and then bit 0 must be addressed and blown. The order of blowing bits, however, is not important. Blowing bit 0 first, and then bit 2 is acceptable.

Note: After blowing, the programming is not reversible, even after cycling the supply power. Although a register bit field fuse cannot be reset after it is blown, additional bits within the same register can be blown at any time until the device is locked. For example, if bit 1 (binary 10) has been blown, it is still possible to blow bit 0. The end result would be binary 11 (decimal code 3).

## Locking the Device

After the required code for each parameter is programmed, the device can be locked to prevent further programming of any parameters. To do so, perform the following steps:

1. Ensure that the  $C_{\text{BLOW}}$  capacitor is mounted.
2. Select the Programming Lock register (key 7).
3. Select Blow mode (key 9).
4. Address bit 3 (001000) by sending four  $V_{\text{PM}}$  pulses.
5. Send one Blow pulse, at  $I_{\text{PP}}$  and  $SR_{\text{BLOW}}$ , and sustain it for  $t_{\text{BLOW}}$ .
6. Delay for a  $t_{\text{LOW}}$  interval, then power-down.
7. Optionally check all fuses.

## Fuse Checking

Incorporated in the A119x family is circuitry to simultaneously check the integrity of the fuse bits. The fuse checking feature is enabled by using the Fuse Check register (selection key 7), and while in Try mode, applying the codes shown in table 2. The register is only valid in Try mode and is available before or after the Programming Lock bit is set.

Setting the fuse threshold high checks that all blown fuses are properly blown. Setting fuse threshold low checks all un-blown fuses are properly intact. The supply current increases by  $250 \mu\text{A}$  if a marginal fuse is detected. If all fuses are correctly blown or fully intact, there will be no change in supply current.

## Additional Guidelines

The additional guidelines in this section should be followed to ensure the proper behavior of these devices:

- A  $0.1 \mu\text{F}$  blowing capacitor,  $C_{\text{BLOW}}$ , must be mounted between the VCC pin and the GND pin during programming, to ensure enough current is available to blow fuses.
- The power supply used for programming must be capable of delivering at least  $V_{\text{PH}}$  and 175 mA.
- Be careful to observe the  $t_{\text{LOW}}$  delay time before powering down the device after blowing each bit.
- Lock the device (only after all other parameters have been programmed and validated) to prevent any further programming of the device.

## $B_{\text{OP}}$ Selection

Selecting  $B_{\text{OP}}$  should be done in two stages. First, Try mode should be used to adjust  $B_{\text{OP}}$  and monitor the output state. Then the optimum  $B_{\text{OP}}$  is set permanently using Blow mode.

Use the  $B_{\text{OP}}$  Trim Up Counting register to increase the  $B_{\text{OP}}$  selection by one Magnetic Step Size,  $\text{Step}_{\text{BOP}}$ , increment with each bit field pulse (see figure 8). Use the  $B_{\text{OP}}$  Trim Down Counting register to decrease the  $B_{\text{OP}}$  selection by one  $\text{Step}_{\text{BOP}}$  with each bit field pulse (see figure 9). As an aid to programming, when using down-counting method, the A119x automatically inverts the bit field selection (code 0 in down-counting sets the bit field value 111111, and the actual bit field value decreases until code 63 sets bit field value 000000).

Note that the release point,  $B_{\text{RP}}$ , is a value below  $B_{\text{OP}}$ . The difference is specified by the Hysteresis,  $B_{\text{HYS}}$ , which is not programmable.

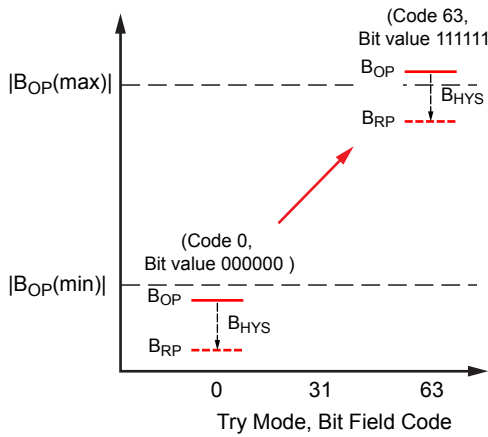


Figure 8.  $B_{OP}$  Selection Up-Counting

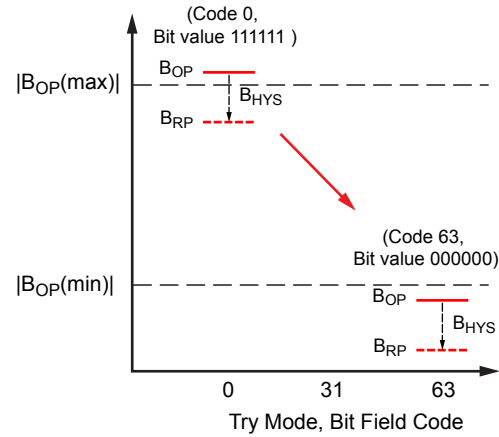


Figure 9.  $B_{OP}$  Selection Down-Counting

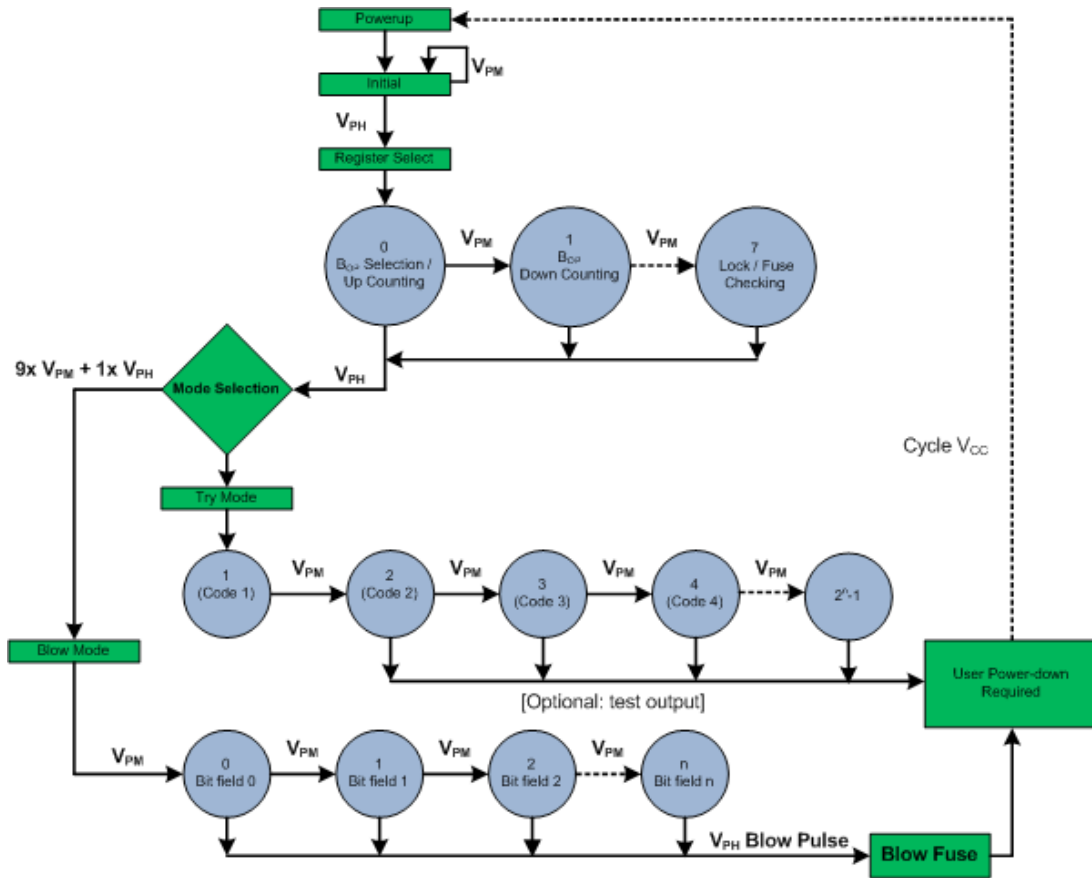


Figure 10. Programming state diagram

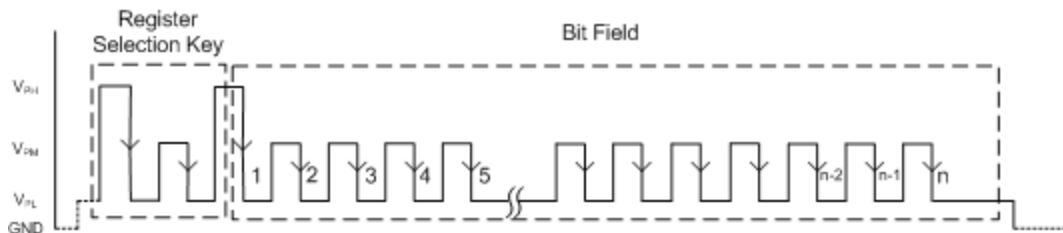


Figure 11. Example of Try mode pulse sequence, Register Key = B<sub>OP</sub> selection down counting

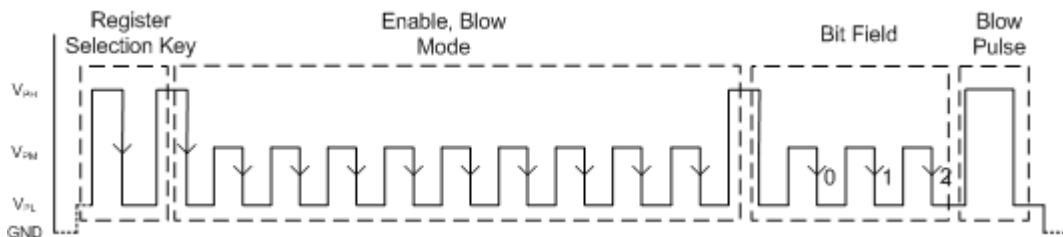


Figure 12. Example of Blow mode pulse sequence, Register Key = B<sub>OP</sub> selection bit field 2 (code 4)

## Power Derating

The device must be operated below the maximum junction temperature of the device,  $T_J(\text{max})$ . Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating  $T_J$ . (Thermal data is also available on the Allegro MicroSystems Web site.)

The Package Thermal Resistance,  $R_{\theta JA}$ , is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity,  $K$ , of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case,  $R_{\theta JC}$ , is relatively small component of  $R_{\theta JA}$ . Ambient air temperature,  $T_A$ , and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation,  $P_D$ ), can be estimated. The following formulas represent the fundamental relationships used to estimate  $T_J$ , at  $P_D$ .

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as:  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 12\text{ V}$ ,  $I_{CC} = 4\text{ mA}$ , and  $R_{\theta JA} = 140\text{ }^\circ\text{C/W}$ , then:

$$P_D = V_{CC} \times I_{CC} = 12\text{ V} \times 4\text{ mA} = 48\text{ mW}$$

$$\Delta T = P_D \times R_{\theta JA} = 48\text{ mW} \times 140\text{ }^\circ\text{C/W} = 7^\circ\text{C}$$

$$T_J = T_A + \Delta T = 25^\circ\text{C} + 7^\circ\text{C} = 32^\circ\text{C}$$

A worst-case estimate,  $P_D(\text{max})$ , represents the maximum allowable power level ( $V_{CC}(\text{max})$ ,  $I_{CC}(\text{max})$ ), without exceeding  $T_J(\text{max})$ , at a selected  $R_{\theta JA}$  and  $T_A$ .

*Example:* Reliability for  $V_{CC}$  at  $T_A = 150^\circ\text{C}$ , package UA, using a low-K PCB.

Observe the worst-case ratings for the device, specifically:  $R_{\theta JA} = 165\text{ }^\circ\text{C/W}$ ,  $T_J(\text{max}) = 165^\circ\text{C}$ ,  $V_{CC}(\text{max}) = 24\text{ V}$ , and  $I_{CC}(\text{max}) = 17\text{ mA}$ .

Calculate the maximum allowable power level,  $P_D(\text{max})$ . First, invert equation 3:

$$\Delta T_{\text{max}} = T_J(\text{max}) - T_A = 165^\circ\text{C} - 150^\circ\text{C} = 15^\circ\text{C}$$

This provides the allowable increase to  $T_J$  resulting from internal power dissipation. Then, invert equation 2:

$$P_D(\text{max}) = \Delta T_{\text{max}} \div R_{\theta JA} = 15^\circ\text{C} \div 165\text{ }^\circ\text{C/W} = 91\text{ mW}$$

Finally, invert equation 1 with respect to voltage:

$$V_{CC(\text{est})} = P_D(\text{max}) \div I_{CC}(\text{max}) = 91\text{ mW} \div 17\text{ mA} = 5\text{ V}$$

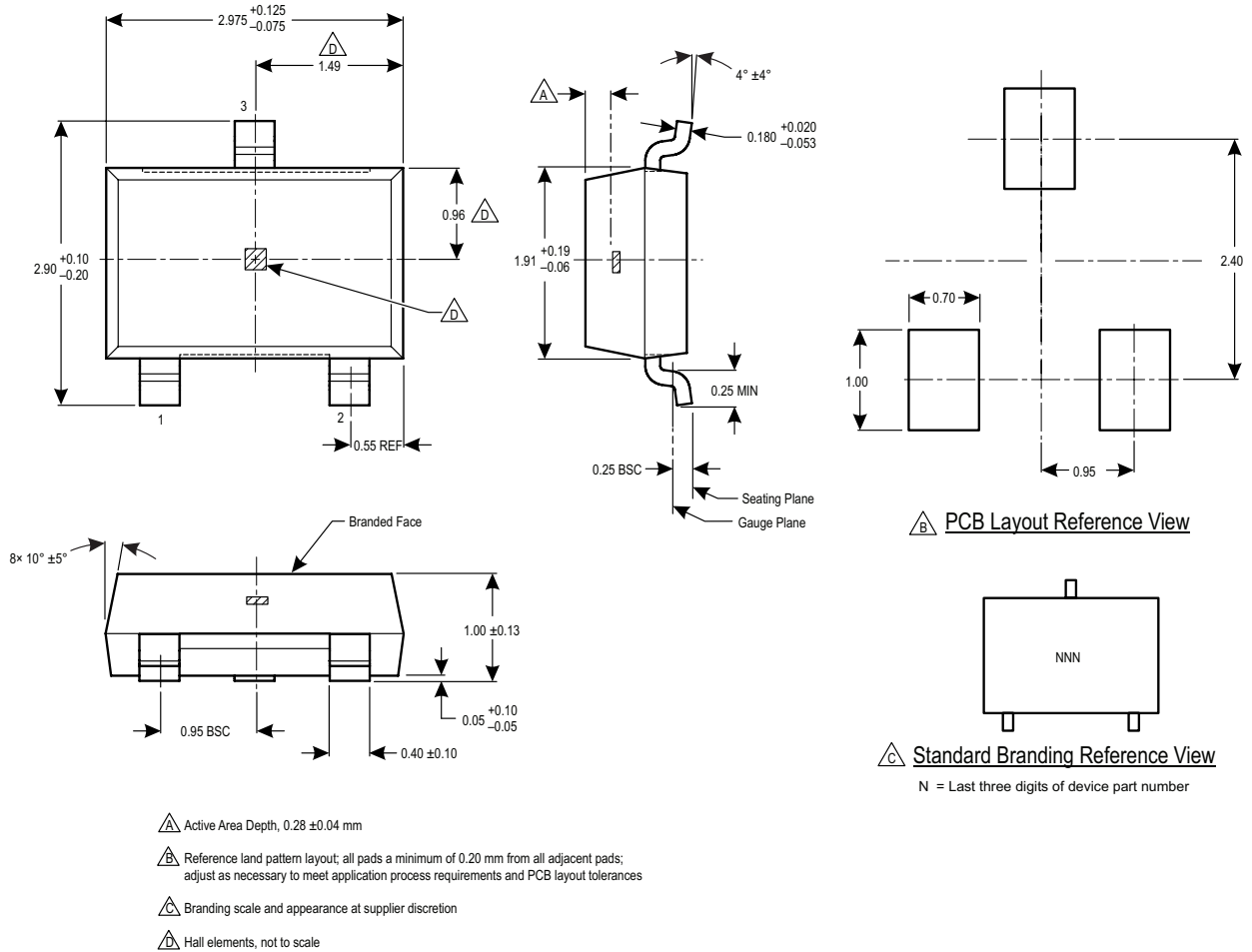
The result indicates that, at  $T_A$ , the application and device can dissipate adequate amounts of heat at voltages  $\leq V_{CC(\text{est})}$ .

- (1) Compare  $V_{CC(\text{est})}$  to  $V_{CC}(\text{max})$ . If  $V_{CC(\text{est})} \leq V_{CC}(\text{max})$ , then reliable operation between  $V_{CC(\text{est})}$  and  $V_{CC}(\text{max})$  requires enhanced  $R_{\theta JA}$ .
- (2) If  $V_{CC(\text{est})} \geq V_{CC}(\text{max})$ , then operation between  $V_{CC(\text{est})}$  and  $V_{CC}(\text{max})$  is reliable under these conditions.

## PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use

(Reference DWG-0000628)  
Dimensions in millimeters – NOT TO SCALE  
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions  
Exact case and lead configuration at supplier discretion within limits shown



## Package LH, 3-Pin SOT23W

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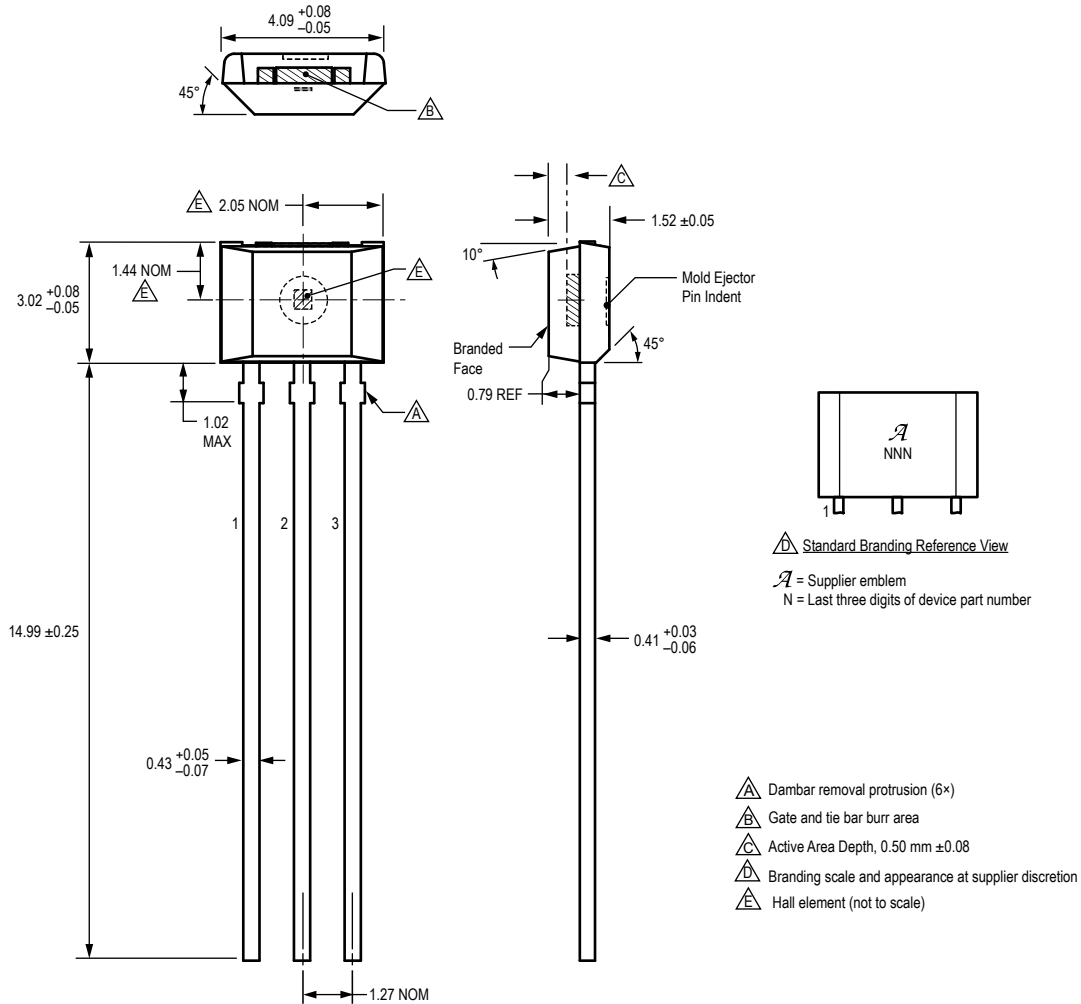
(Reference DWG-0000404, Rev. 1)

NOT TO SCALE

Dimensions in millimeters

Dimensions exclusive of mold flash, gate burrs, and dambar protrusions

Exact case and lead configuration at supplier discretion within limits shown



## Package UA, 3-Pin SIP, Gate Relief

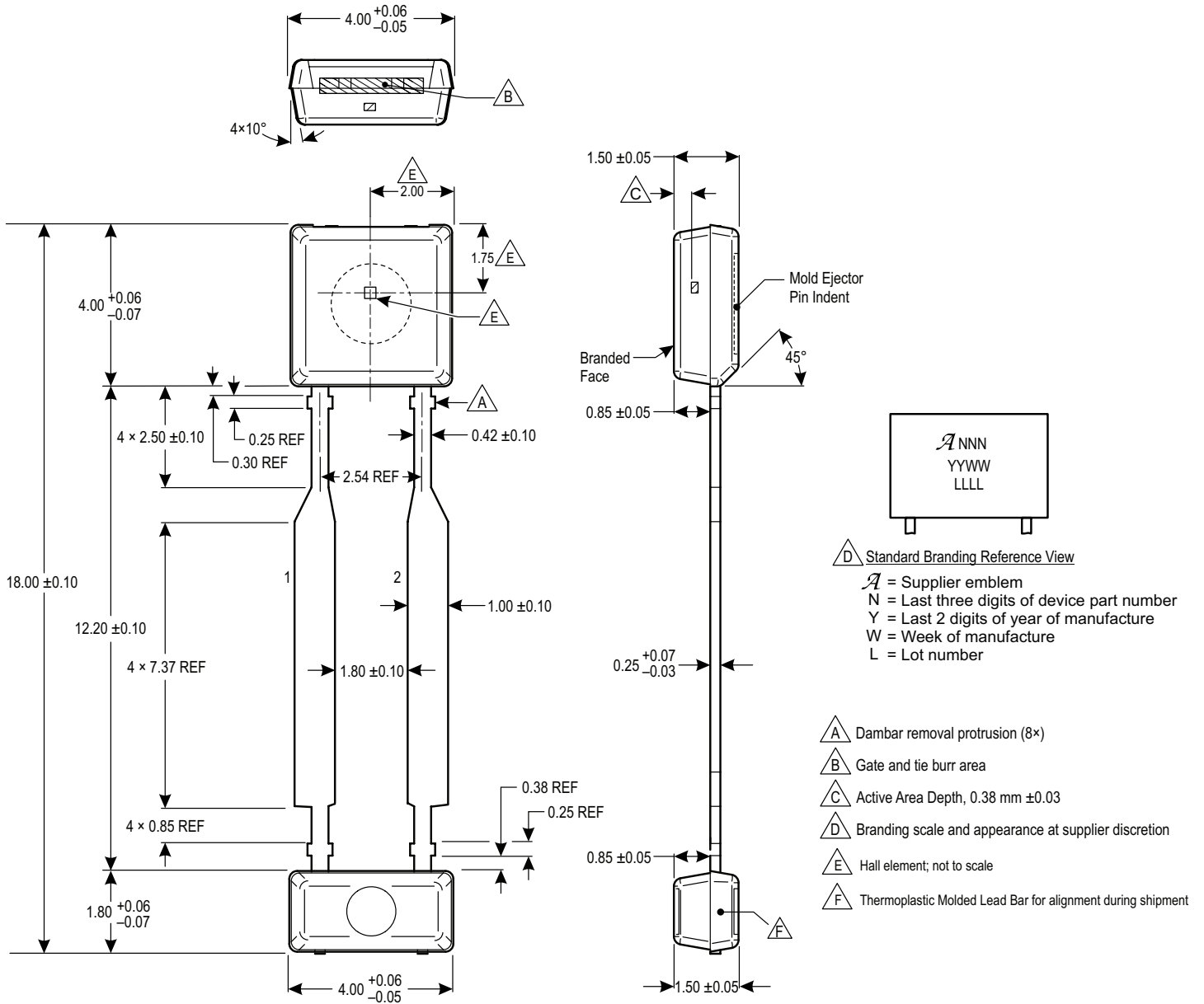
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(Reference DWG-0000408, Rev. 3)

Dimensions in millimeters – NOT TO SCALE

Dimensions exclusive of mold flash, gate burrs, and dambar protrusions

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**Package UB, 2-Pin SIP**

## REVISION HISTORY

Number	Date	Description
4	May 24, 2013	Update application information
5	September 21, 2015	Added AEC-Q100 qualification under Features and Benefits
6	February 3, 2016	Added UB package option; added -F part option.
7	February 25, 2016	Removed A1190-F part option.
8	August 9, 2018	Added footnote to LH package (page 3)
9	September 19, 2019	Updated LH, UA, and UB package drawings, and minor editorial updates

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